Rockchip
RK3588
Technical Reference Manual

Revision History

Date	Revision	Description
2022-03-09	1.0	Initial Release

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Chapter 1 Interconnect

1.1 Overview

The chip-level interconnect enables communication among the modules and subsystems in the device. It supports the following features:

- Cross-bar exchange network
- Four embedded DDR schedulers for transaction reorder to maximum DDR efficiency
- Priority management for quality of service (QoS), especially for real-time IP
- Transaction statistics for bandwidth analysis

1.2 Block Diagram

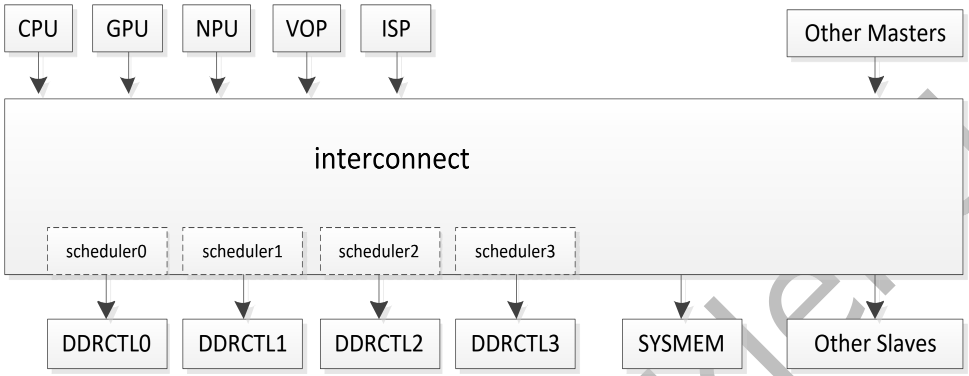


Fig. 1-1 Interconnect Diagram

1.3 Function Description

1.3.1 DDR Scheduler

There are four DDR schedulers in system, their address range size are 8K bytes and their base address are shown as follows.

Table 1-1 DDR scheduler address map

DDRSCH	Base Address
Channel0 DDRSCH	0xFE000000
Channel1 DDRSCH	0xFE002000
Channel2 DDRSCH	0xFE004000
Channel3 DDRSCH	0xFE006000

The DDR scheduler is an interface to DDR controllers. The scheduler is a special unit case multiplexing several transport interfaces feeding a single DDR controller target, with a special arbitration scheme, configurable for optimizing DRAM bandwidth efficiency from the DDR controller.

The scheduler optimizes DRAM efficiency by choosing the best transaction to execute inside each port input queue: the scheduler can reorder requests across queues, and within a queue as long as they do not have conflicting addresses or ordering constraints. The process for choosing the next transaction to issue to the controller is based on a model of the DRAM behavior (in terms of timings for pages, banks, bank groups, and data bus), a user configuration of arbitration criteria, and a DDR configuration setup representing the current assignment of DRAM banks, bank groups, and page bits to the incoming addresses. It also makes sure that output queues never overflow.

The scheduler arbitration criteria take into account the priority characteristics of the transactions, providing a trade-off between QoS requirements of each data flow, and the global DDR efficiency: for example, an urgent read request may take precedence over less urgent write requests, even though there may be a global efficiency loss due to DRAM bus turnaround.

The DDR scheduler is connected to DDR controller, through a simple, ordered interface. A simple DDR controller BIU converts the generic interface output of the scheduler to the appropriate DDR controller protocol, and optionally provides access to DDR controller registers. It is the responsibility of the controller to fully handle the DRAM state machine.

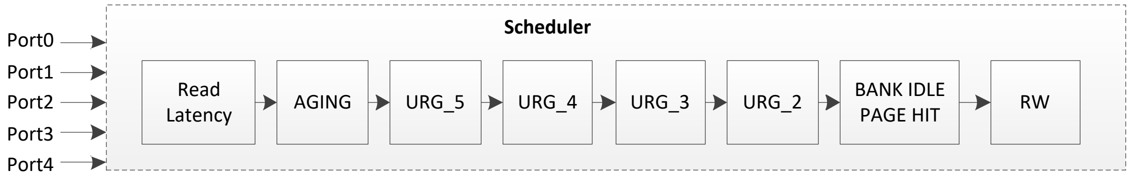


Fig. 1-2 DDR Scheduler Diagram

The arbitration criteria is shown above.

Read Latency: The scheduler monitors the latency of read accesses sent to DDR controller, and uses this latency in a feedback loop to control scheduler behavior. When the ceiling is exceeded, the scheduler stalls requests until it obtains the responses of previous reads from the controller. This mechanism thus prevents scheduler–controller misalignment and maintains scheduler–controller system stability, for example, when a DRAM refresh occurs.

AGING: Biases arbitration towards requests that exceed the aging threshold set by register Aging(n) for port (n).

URG5, URG4, URG3, URG2: Biases arbitration in favor of urgency bits in packets. Three bits QoS level will be map to seven bits Urgency level in packets as Table 1-2. URG5 means the packets with fifth bit of Urgency field(Urgency[4]) is 1’b1 will be chosen by this arbiter stage.

Table 1-2 QoS and Urgency map

QoS generator(internal) Press/Hurry(external)	Urgency
3'b0	7’b0000000
3'b1	7’b0000001
3'b2	7’b0000011
3'b3	7’b0000111
3'b4	7’b0001111
3'b5	7’b0011111
3'b6	7’b0111111
3'b7	7’b1111111

***Note**: There is a command queue in DDR controller, although the high priority request will be sent to DDR controller first, it does not mean that it can be served by DDR immediately. The request in DDR controller command queue will be executed in order taking no account of priority.*

BANK_IDLE_PAGE_HIT: Biases arbitration in favor of requests whose target bank is idle or whose target row is equal to the active row of the selected bank. The following method is used to estimate the state of the bank: Two counters *ActCnt* and *CmdCnt* are associated with each DDR bank, the bank number being obtained from the address using the "B" bits in the selected DDR configuration, set by register ‘DeviceConf’. These counters are decremented at each DDR scheduler clock cycle and saturated at 0. A bank is considered idle when both counters are null. The ActCnt counter is loaded with ActToAct – 1 each time a new page is accessed in that bank. The CmdCnt counter is loaded with:
RdtoMiss + max(BurstLen, N) – BurstLen – 1 each time an N-word read is sent, and with WrtoMiss + max(BurstLen, N) – 1 each time an N-word write is sent.
When the DDR configuration contains bank groups, also known as "G" bits, the following counters are added to each bank group in a device:
***Note: CcdLCnt** —— The counter is loaded with the result of tCCD_L−1 each time a new request is granted, and decremented every clock cycle by 1. **RrdCntL** —— The counter is loaded with the result of tRRD_L – 1*

each time a new page is accessed, and decremented every clock cycle by 1.

RW: Biases arbitration in favor of requests whose RD or WR opcode type matches the type in the last-issued requests. The criterion is used to estimate the importance of keeping RD and WR transactions together, according to the following method:
Counter *RdWrCnt* and bit PrvOpc are used to represent the DDR read–write state. The counter is decremented at each scheduler clock cycle and saturated at 0.
Arbitration is biased in favor of WR when:
PrvOpc = WR or (PrvOpc = RD and RdWrCnt > RdToWr)
The counter is then loaded with:
WrToRr + max(BurstLen, N) – 1
where N is the number of words of the WR request.
Arbitration is biased in favor of RD when:
PrvOpc = RD or (PrvOpc = WR and RdWrCnt > WrToRd)
The counter is then loaded with WrToRd + max(BurstLen, N) – 1, where N is the number of words of the RD request.

When the DDR configuration contains bank groups, also known as "G" bits, counter *RdWrCntL* is added to each device and bank group. The counter is loaded with the result of RdToWr + max(BurstLen, N) – 1 each time a read request is granted, and with WrToRdL + max(BurstLen, N) – 1 each time a write is granted. The counter is decremented every clock cycle by 1.

1.3.2 Priority Management

As mentioned above, the DDR scheduler will consider the priority of each request to ensure desired quality of service. The priority of each request is configurable through the internal QoS generator in each master BIU. The QoS generator address of each master BIU and default priority are shown below. When configuring the register of QoS generator of a certain master BIU，the corresponding clock of the master BIU should be alive.

Table 1-3 Master BIU information

Master		**MID**	**PORT**	**PROBE ID**	**default QoS**	**QoS generator base address**	**Shaping base address**	**Ext priority**
VI	ISP0_MWO	7'h1d	2	1	2	0xfdf40500	0xfdf40580	YES
	ISP0_MRO	7'h1d	3	0	2	0xfdf40400	0xfdf40480	YES
	ISP1_MWO	7'h1e	3	1	2	0xfdf41000	0xfdf41080	YES
	ISP1_MRO	7'h1e	2	0	2	0xfdf41100	0xfdf41180	YES
	VICAP_M0	7'h44	1	1	2	0xfdf40600	0xfdf40680	YES
	VICAP_M1	7'h45	0	0	2	0xfdf40800	0xfdf40880	YES
	FISHEYE0	7'h0f	1	0	0	0xfdf40000	0xfdf40080	YES
	FISHEYE1	7'h10	0	0	0	0xfdf40200	0xfdf40280	YES
VO	VOP_M0	7'h46	0	1	2	0xfdf82000	0xfdf82080	YES
	VOP_M1	7'h47	1	1	2	0xfdf82200	0xfdf82280	YES
RKVDEC	RKVDEC0	7'h34	2	0	0	0xfdf62000	0xfdf62080	YES
	RKVDEC1	7'h35	3	0	0	0xfdf63000	0xfdf63080	YES
AV1	AV1	7'h00	2	0	0	0xfdf64000	0xfdf64080	NO
RKVENC	RKVENC0_M0RO	7'h36	1	0	0	0xfdf60000	0xfdf60080	YES
	RKVENC0_M1RO	7'h37	0	0	0	0xfdf60200	0xfdf60280	YES
	RKVENC0_M2WO	7'h38	0	0	0	0xfdf60400	0xfdf60480	YES
	RKVENC1_M0RO	7'h39	0	0	0	0xfdf61000	0xfdf61080	YES
	RKVENC1_M1RO	7'h3a	1	0	0	0xfdf61200	0xfdf61280	YES
	RKVENC1_M2WO	7'h3b	1	0	0	0xfdf61400	0xfdf61480	YES
CPU	DSU_M0	NA	4	0,1,2,3	0	0xfe008000	NA	NO
	DSU_M1	NA	4	0,1,2,3	0	0xfe008800	NA	NO
	DSU_MP	7'h0d	3	0	0	0xfdf34200	0xfdf34280	NO
	DEBUG	7'h04	3	0	0	0xfdf34400	0xfdf34480	NO

Master		MID	PORT	PROBE ID	default QoS	QoS generator base address	Shaping base address	Ext priority
GPU	GPU_M0	7'h15	2	0	0	0xfdf35000	0xfdf35080	NO
	GPU_M1	7'h16	3	0	0	0xfdf35200	0xfdf35280	NO
	GPU_M2	7'h17	0	0	0	0xfdf35400	0xfdf35480	NO
	GPU_M3	7'h18	1	0	0	0xfdf35600	0xfdf35680	NO
NPU	NPU1	7'h2e	3	0	0	0xfdf70000	0xfdf70080	YES
	NPU0_MRO	7'h2d	2	0	0	0xfdf72200	0xfdf72280	YES
	NPU2	7'h2f	0	0	0	0xfdf71000	0xfdf71080	YES
	NPU0_MWR	7'h2c	1	1	0	0xfdf72000	0xfdf72080	YES
	MCU_NPU	7'h27	0	0	3	0xfdf72400	0xfdf72480	NO
VDPU	JPEG_DEC	7'h1f	3	0	0	0xfdf66200	0xfdf66280	NO
	JPEG_ENC0	7'h20	2	0	0	0xfdf66400	0xfdf66480	NO
	JPEG_ENC1	7'h21	2	0	0	0xfdf66600	0xfdf66680	NO
	JPEG_ENC2	7'h22	3	0	0	0xfdf66800	0xfdf66880	NO
	JPEG_ENC3	7'h23	3	0	0	0xfdf66a00	0xfdf66a80	NO
	RGA2_MRO	7'h30	3	0	0	0xfdf66c00	0xfdf66c80	NO
	RGA2_MWO	7'h31	3	0	0	0xfdf66e00	0xfdf66e80	NO
	RGA3_0	7'h32	2	0	0	0xfdf67000	0xfdf67080	YES
	VDPU	7'h43	2	0	0	0xfdf67200	0xfdf67280	NO
	IEP	7'h1c	3	0	0	0xfdf66000	0xfdf66080	NO
RGA3_1	RGA3_1	7'h33	1	0	0	0xfdf36000	0xfdf36080	YES
VO0	HDCP0	7'h19	2	0	5	0xfdf80000	0xfdf80080	NO
VO1	HDCP1	7'h1a	2	0	5	0xfdf81000	0xfdf81080	NO
	HDMIRX	7'h1b	2	0	2	0xfdf81200	0xfdf81280	NO
PHP	GIC600_M0	7'h12	3	0	0	0xfdf3a000	0xfdf3a080	NO
	GIC600_M1	7'h13	2	0	0	0xfdf3a200	0xfdf3a280	NO
	MMU600PCIE_TCU	7'h29	3	0	0	0xfdf3a400	0xfdf3a480	NO
	MMU600PHP_TBU	7'h2a	3	0	0	0xfdf3a600	0xfdf3a680	NO
	MMU600PHP_TCU	7'h2b	3	0	0	0xfdf3a800	0xfdf3a880	NO
USB	USB3_0	7'h40	2	0	4	0xfdf3e200	0xfdf3e280	NO
	USB3_1	7'h41	2	0	4	0xfdf3e000	0xfdf3e080	NO
	USB2HOST_0	7'h3e	2	0	4	0xfdf3e400	0xfdf3e480	NO
	USB2HOST_1	7'h3f	2	0	4	0xfdf3e600	0xfdf3e680	NO
NVM	EMMC	7'h0e	3	0	4	0xfdf38200	0xfdf38280	NO
	FSPI	7'h11	3	0	4	0xfdf38000	0xfdf38080	NO
	SDIO	7'h3c	3	0	4	0xfdf39000	0xfdf39080	NO
BUS	DECOM	7'h05	1	0	0	0xfdf32000	0xfdf32080	NO
	DMAC0	7'h08	1	0	0	0xfdf32200	0xfdf32280	NO
	DMAC1	7'h09	1	0	4	0xfdf32400	0xfdf32480	NO
	DMAC2	7'h0a	1	0	4	0xfdf32600	0xfdf32680	NO
	GIC600M	7'h14	1	0	0	0xfdf32800	0xfdf32880	NO
center	DMA2DDR	7'h07	0	0	0	0xfdf52000	0xfdf52080	NO
	MCU_DDR	7'h26	0	0	3	0xfdf52200	0xfdf52280	NO
pmu vad	VAD	7'h42	2	0	0	0xfdf3b200	0xfdf3b080	NO
	MCU_PMU	7'h28	2	0	3	0xfdf3b000	0xfdf3b080	NO
secure	CRYPTOS	7'h02	2	0	0	0xfdf3d200	0xfdf3d280	NO
	CRYPTONS	7'h01	2	0	0	0xfdf3d000	0xfdf3d080	NO
	DCF	7'h03	2	0	0	0xfdf3d400	0xfdf3d480	NO
	SDMMC	7'h3d	2	0	4	0xfdf3d800	0xfdf3d880	NO

Except the internal priority control, some masters can also change their priority dynamic by their internal register according to buffer status. In order to make this work, ExtControl register of the corresponding BIU must be set to 0x1. In this case, the interconnect will choose the highest priority from the external and internal register. It is better to set the internal priority same as the other master BIUs and external priority higher so that the DDR scheduler has more opportunity to optimal DDR efficiency. As shown in Table1-1, because the arbiter stages ordering is: URG5, URG4, URG3, URG2, the valid values of internal and external works in scheduler are 0, 2, 3, 4 and 5.

1.3.3 Shaping

Shaping limits the number of pending packets between master and scheduler. When shaping is applied and the number of packets pending on a route to scheduler reaches the programmed limit, flow control prevents further transmission of request packets to the BIU by de-asserting signal Ready until a complete response packet returns on the route. The default shaping value is 255, and address of the shaping control register for each master is shown in Table1-3.

1.3.4 Probe

The interconnect provides a service called probe to trace packet and compute traffic statics. There are totally 12 probes to monitor the DDR schedule traffic statics, and each can be programmed by their registers. They are listed in Table1-3. Which probe should be used to measure the bandwidth of a certain master can be find in Table1-3. The bandwidth of DSU should be measured by all the probes of Port4, and the sum of the 4 probes is the total bandwidth.

Table 1-4 Bandwidth Probe Base Address

Probe	Base Address
Port0 Probe0	0xfdf50000
Port0 Probe1	0xfdf50400
Port1 Probe0	0xfdf50800
Port1 Probe1	0xfdf50c00
Port2 Probe0	0xfdf51000
Port2 Probe1	0xfdf51400
Port3 Probe0	0xfdf51800
Port3 Probe1	0xfdf51c00
Port4 Probe0	0xfe008c00
Port4 Probe1	0xfe009000
Port4 Probe2	0xfe009400
Port4 Probe3	0xfe009800

1.3.5 Channel Address Space

When work in 4 channels interleave mode, CENTER_GRF_CON4[8:4] should be set to 5’b0000. If not work in interleave mode, CENTER_GRF_CON4[8:4] should be config according to the size of each channel, as showed in Table1-5.

Table 1-5 Channel Address

CENTER_GRF_CON4[8:4]	base address				channel size
	channel 0	channel 1	channel 2	channel 3	
5'b00000	0x0_0000_0000	0x2_0000_0000	0x4_0000_0000	0x6_0000_0000	8GB
5'b00101	0x0_0000_0000	0x1_8000_0000	0x3_0000_0000	0x4_8000_0000	6GB
5'b00001	0x0_0000_0000	0x1_0000_0000	0x2_0000_0000	0x3_0000_0000	4GB
5'b00110	0x0_0000_0000	0x0_C000_0000	0x1_8000_0000	0x2_4000_0000	3GB
5'b00010	0x0_0000_0000	0x0_8000_0000	0x1_0000_0000	0x1_8000_0000	2GB
5'b01000	0x0_0000_0000	0x0_6000_0000	0x0_C000_0000	0x1_2000_0000	1.5GB
5'b00011	0x0_0000_0000	0x0_4000_0000	0x0_8000_0000	0x0_C000_0000	1GB
5'b00100	0x0_0000_0000	0x0_2000_0000	0x0_4000_0000	0x0_6000_0000	0.5GB
5'b00111	0x0_0000_0000	0x0_1000_0000	0x0_2000_0000	0x0_3000_0000	0.25GB
5'b10000	NA	NA	0x0_0000_0000	0x2_0000_0000	8GB

5'b10101	NA	NA	0x0_0000_0000	0x1_8000_0000	6GB
5'b10001	NA	NA	0x0_0000_0000	0x1_0000_0000	4GB
5'b10110	NA	NA	0x0_0000_0000	0x0_C000_0000	3GB
5'b10010	NA	NA	0x0_0000_0000	0x0_8000_0000	2GB
5'b11000	NA	NA	0x0_0000_0000	0x0_6000_0000	1.5GB
5'b10011	NA	NA	0x0_0000_0000	0x0_4000_0000	1GB
5'b10100	NA	NA	0x0_0000_0000	0x0_2000_0000	0.5GB
5'b10111	NA	NA	0x0_0000_0000	0x0_1000_0000	0.25GB

1.4 Register Description

1.4.1 DDRSCH Registers Summary

Name	Offset	Size	Reset Value	Description
DDRSCH_Id_CoreId	0x0000	W	0x215FB002	Core id
DDRSCH_Id_RevisionId	0x0004	W	0x3C9D4E00	Revision id
DDRSCH_DeviceConf	0x0008	W	0x00000000	Register DeviceConf stores selectors to the predefined list of DDR configuration to be programmed at initialization phase.
DDRSCH_DeviceSize	0x000C	W	0x00004040	Register DeviceSize is used to set the size of DDR ranks.
DDRSCH_DdrTimingA	0x0010	W	0xFF361D33	Register DdrTimingA of timing register bank n stores timing settings used by DDR schedulers to compute bank and page states.
DDRSCH_DdrTimingB	0x0014	W	0x1B081306	Register DdrTimingB of timing register bank n stores timing settings used by DDR schedulers to compute penalties pertaining to bank and page states.
DDRSCH_DdrTimingC	0x0018	W	0x00000006	Register DdrTimingC of timing register bank n: Stores timing settings used by DDR schedulers to compute penalties pertaining to DRAM commands. It is used to configure the clock of the register bank.
DDRSCH_DdrTimingL	0x001C	W	0x00000000	Long timing for DDR4 Bank Group support
DDRSCH_DevToDev	0x0020	W	0x00000663	Register DevToDev of timing register bank n contains supplementary timing penalties that are incurred when changing data-bus ownership of up to four devices. The penalties are expressed in scheduler clock cycles.
DDRSCH_DdrMode	0x0024	W	0x0000002C	Register DdrMode stores the controller behaviour description.
DDRSCH_AgingX	0x002C	W	0x00000004	Aging threshold multiplicator
DDRSCH_Aging0	0x0030	W	0x000000FF	AGING slice threshold for port0
DDRSCH_Aging1	0x0034	W	0x000000FF	AGING slice threshold for port1
DDRSCH_Aging2	0x0038	W	0x000000FF	AGING slice threshold for port2

Name	Offset	Size	Reset Value	Description
DDRSCH_Aging3	0x003C	W	0x000000FF	AGING slice threshold for port3
DDRSCH_Aging4	0x0040	W	0x000000FF	AGING slice threshold for port4

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.2 DDRSCH Detail Registers Description

DDRSCH_Id_CoreId

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x215fb0	CoreChecksum Field containing a checksum of the parameters of the IP.
7:0	RO	0x02	CoreTypeId Field identifying the type of IP.

DDRSCH_Id_RevisionId

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RW	0x3c9d4e	BuildId Field containing the build revision of the software used to generate the IP HDL code.
7:0	RW	0x00	UserId Field containing a user defined value, not used anywhere inside the IP itself.

DDRSCH_DeviceConf

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	DeviceConf Selector of predefined ddrConf configuration. 6'h0: D_RRRR_RRRR_RRRR_RRRR_RRBB_BCCC_CCCC_---- 6'h1: D_RRRR_RRRR_RRRR_RRRR_RBBB_BCCC_CCCC_---- 6'h2: D_RRRR_RRRR_RRRR_RRRR_RBBG_CCCC_CCGC_---- 6'h3: D_RRRR_RRRR_RRRR_RRRR_RBBG_GCCC_CCCC_---- 6'h4: R_RRRR_RRRR_RRRR_RRRR_RDBB_BCCC_CCCC_---- 6'h5: R_RRRR_RRRR_RRRR_RRRR_DBBB_BCCC_CCCC_---- 6'h6: R_RRRR_RRRR_RRRR_RRRR_DBBG_CCCC_CCGC_---- 6'h7: R_RRRR_RRRR_RRRR_RRRR_DBBG_GCCC_CCCC_---- Others: Reserved R: Indicates Row bits B: Indicates Bank bits C: Indicates Column bits G: Indicates Bank Group bits

DDRSCH_DeviceSize

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x40	Rank1 Rank1 size. The granule size is 64MB.
7:0	RW	0x40	Rank0 Rank0 size. The granule size is 64MB.

DDRSCH_DdrTimingA

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	ReadLatency Maximum delay between a read request and the first data response. 0 delay disable the Read Latency control.
23	RO	0x0	reserved
22:16	RW	0x36	WrToMiss Minimum number of scheduler clock cycles between the last DRAM Write command and a new Read or Write command in another page of the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: (WL*tCkD + tWR + tRP + tRCD) / tCkG
15:14	RO	0x0	reserved
13:8	RW	0x1d	RdToMiss Minimum number of scheduler clock cycles between the last DRAM Read command and a new Read or Write command in another page of the same bank. The field must be set to the following value, round to an integer number of scheduler clock cycles: (tRTP + tRP + tRCD - BL*tCkD/2) / tCkG
7	RO	0x0	reserved
6:0	RW	0x33	ActToAct Minimum number of scheduler clock cycles between two consecutive DRAM Activate commands on the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tRC / tCkG

DDRSCH_DdrTimingB

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x1b	Faw Number of cycle of the FAW period. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tFAW / tCkG
23:20	RO	0x0	reserved
19:16	RW	0x8	Rrd Number of cycle between two consecutive Activate commands on different Banks of the same device. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tRRD / tCkG
15:13	RO	0x0	reserved
12:8	RW	0x13	WrToRd Minimum number of scheduler clock cycles between the last DRAM Write command and a Read command. The field must be set to the following value, rounded to an integer of scheduler clock cycles: ((WL + 1)*tCkD + tWTR) / tCkG, for LPDDR4 memories.
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x06	RdToWr Minimum number of scheduler clock cycles between the last DRAM Read command and a Write command. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: (RL + RoundUp(tDQSCK(max) / tCKD) + tRPST - WL + tWPRE) tCkD / tCKG, for LPDDR4 memories.

DDRSCH_DdrTimingC
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	WrToMwr Number of scheduler clock cycles between the last write data to the first data of a masked write command on the same bank. This field must be set to 3xBurstPenalty for LPDDR4, and must be set to zero for the other DRAM.
7:4	RO	0x0	reserved
3:0	RW	0x6	BurstPenalty DRAM burst duration on the DRAM data bus in scheduler clock cycles. The field must be set to Nd /Ns, where: Nd is the number of DRAM cycles needed to process a DRAM burst of determined size, expressed in bytes. Ns is the minimum number of scheduler cycles to process a DRAM burst of the same size.

DDRSCH_DdrTimingL
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	RrdL Register field RrdL sets the minimum time, expressed in scheduler clock cycles of the tRRD timing for LPDDR4 devices. This is the timing of access to the same bank group for RD after RD.
7:3	RW	0x00	WrToRdL Register field WrToRdL sets the minimum time, expressed in scheduler clock cycles, of the tWrToRd timing for LPDDR4 devices. This is the timing of access to the same bank group, WR to RD.
2:0	RW	0x0	CcdL Register field CcdL sets the minimum time, expressed in scheduler clock cycles of the tCCD LPDDR4 devices. This is the timing of access to the same bank group.

DDRSCH_DevToDev
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x0	BusWrToWr Number of cycle between the last write data to a device and the first write data of another device.
11:8	RW	0x6	BusWrToRd Number of cycle between the last write data to a device and the first read data of another device.

Bit	Attr	Reset Value	Description
7:4	RW	0x6	BusRdToWr Number of cycle between the last read data of a device and the first write data to another device.
3	RO	0x0	reserved
2:0	RW	0x3	BusRdToRd Number of cycle between the last read data of a device and the first read data of another device.

DDRSCH_DdrMode

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ForceOrderState Force execution order internal state.
15:8	RW	0x00	ForceOrder When bit n of register field ForceOrder is set to 1, DRAM commands are executed in the order they arrive at scheduler port n. When field bits are set to 1, and BypassFiltering is also set to 1, command execution order is guaranteed for the corresponding scheduler port.
7	RO	0x0	reserved
6:5	RW	0x1	MwrSize Register MwrSize sets LPDDR4 and LPDDR5 data width, which is used for masked-write split control. The following table shows the field values according to DDR type. 2'b00: Reserved 2'b01: LPDDR4 & LPDDR5, 16 bits. 2'b10: LPDDR4 & LPDDR5, 32 bits. 2'b11: LPDDR4 & LPDDR5, 32 bits. Identical to value 2'b10.
4:3	RW	0x1	BurstSize Register field Burst Size sets the DDR burst size, in bytes, as shown by the following table. 2'b00: 16 2'b01: 32 2'b10: 64 2'b11: 128 NOTE: For LPDDR4 memories, the field must be set to the number of bytes required by BL16 transactions.
2	RW	0x1	FawBank Register field FawBank indicates the number of banks of a given device involved in the FAW period during which four banks can be active. It must be set to 0 for 2-bank memories, and 1 for memories with four banks or more.

Bit	Attr	Reset Value	Description
1	RW	0x0	BypassFiltering When register field BypassFiltering is set to 1, arbiter filters are bypassed and timing register outputs are internally set to an idle value. The field can be useful during DRAM initialization, when training or calibration sequences are performed, and scheduler arbitration is not needed. When the field is set to 0, scheduler arbitration is fully functional, this is the functional usage mode. NOTE: When the field is set to 1, the final arbitration level continues to elect transactions among those presented to the arbiter. Set field ForceOrder to ensure that transactions are executed in order, for instance during DRAM initialization.
0	RW	0x0	AutoPrecharge When set to one, pages are automatically closed after each access, when set to zero, pages are left opened until an access in a different page occurs.

DDRSCH_AgingX

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x4	AgingX Aging threshold multiplicator.

DDRSCH_Aging0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	Aging0 Aging slice threshold for port 0.

DDRSCH_Aging1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	Aging1 Aging slice threshold for port 1.

DDRSCH_Aging2

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	Aging2 Aging slice threshold for port 2.

DDRSCH_Aging3

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	Aging3 Aging slice threshold for port 3.

DDRSCH_Aging4

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	Aging4 Aging slice threshold for port 4.

1.4.3 QoS Generator Registers Summary

Name	Offset	Size	Reset Value	Description
QoSGenerator_Id_CoreId	0x0000	W	0x67B76E04	Core ID and checksum
QoSGenerator_Id_RevisionId	0x0004	W	0x3C9D4E00	Revision ID
QoSGenerator_Priority	0x0008	W	0x80000000	Priority register
QoSGenerator_Mode	0x000C	W	0x00000003	QoS generate mode
QoSGenerator_Bandwidth	0x0010	W	0x00000000	bandwidth threshold
QoSGenerator_Saturation	0x0014	W	0x00000040	Saturation counter
QoSGenerator_ExtControl	0x0018	W	0x00000000	External control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.4 QoS Generator Detail Registers Description

QoSGenerator_Id_CoreId

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x67b76e	CoreChecksum Field containing a checksum of the parameters of the IP. Reset value is different for each QoS generator.
7:0	RO	0x04	CoreTypeId Field identifying the type of IP.

QoSGenerator_Id_RevisionId

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x3c9d4e	BuildId Field containing the build revision of the software used to generate the IP HDL code.
7:0	RO	0x00	UserId Field containing a user defined value, not used anywhere inside the IP itself.

QoSGenerator_Priority

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x1	Mark Backward compatibility marker when 0.
30:11	RO	0x00000	reserved
10:8	RW	0x0	P1 In Regulator mode, defines the HIGH hurry level. In Fixed/Limiter mode, defines the Urgency level for READ transactions.
7:3	RO	0x00	reserved
2:0	RW	0x0	P0 In Regulator mode, defines the LOW hurry level. In Fixed/Limiter mode, defines the Urgency level for WRITE transactions.

QoSGenerator_Mode

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x3	Mode Functional Mode 2'b00: Fixed 2'b01: Limiter 2'b10: Bypass 2'b11: Regulator

QoSGenerator_Bandwidth

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	Bandwidth Defines the bandwidth threshold in 1/256th-byte-per-cycle units. In other words, the desired rate in MBps is divided by frequency in MHz of the BIU, and then multiplied by 256. Reset value is different for each QoS generator.

QoSGenerator_Saturation

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x040	Saturation Defines the size of the bandwidth counter, that is, the measurement window, in 16-byte units. In other words, the desired number of bytes divided by 16.

QoSGenerator_ExtControl

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ExtLimitEn When register field ExtLimitEn is set, the bandwidth limiter is enabled when input signal ExtThr is asserted. When the signal is not asserted, the limiter is disabled: bandwidth is not limited, and the counter is stuck to 0. When the bit is cleared, the limiter operates normally and ignores ExtThr.
2	RW	0x0	IntClkEn When set to 1, register field IntClkEn causes the QoS generator to use the BIU clock for bandwidth calculation. When set to 0, and if configuration parameter useExternalReference is set to True, an external reference clock at the socket is used for bandwidth calculation.
1	RW	0x0	ExtThrEn When register field ExtThrEn is set, internal signals Urgency, Press and Hurry are driven, when input signal ExtThr is low, by the value in register Priority field P0. When ExtThr is high, they are driven by the value in register Priority field P1.
0	RW	0x0	SocketQosEn Register field SocketQosEn determines how priority levels are driven when QoS generators and socket interfaces alternatively drive the levels for Urgency, Pressure, and Hurry signals: When set to 0, the QoS generator drives the levels. When set to 1, internal signals Pressure and Hurry are driven by the greater of the two levels from the socket interface or the QoS generator.

1.4.5 Shaping Registers Summary

Name	Offset	Size	Reset Value	Description
Shaper_NbPktMax0	0x0008	W	0x000000FF	Max pending packet number register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.6 Shaping Detail Registers Description

Shaper_NbPktMax0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xFF	NbPktMax0 Max transport packet pending for route to scheduler.

1.4.7 Probe Registers Summary

Name	Offset	Size	Reset Value	Description
Probe_Id_CoreId	0x0000	W	0x194C4006	Stores the Core Id and core checksum.
Probe_Id_RevisionId	0x0004	W	0x3C9D4E00	Revision ID
Probe_MainCtl	0x0008	W	0x00000000	Register MainCtl contains probe global control bits.
Probe_CfgCtl	0x000C	W	0x00000000	Stores global enable and active bits.
Probe_FilterLut	0x0014	W	0x00000000	Controls the filter look-up table (LUT), which is used to select which filters are used and in what logical combination.
Probe_TraceAlarmEn	0x0018	W	0x00000000	Enables hits from either trace filters or the LUT to be recorded in the trace alarm status register TraceAlarmStatus.
Probe_TraceAlarmStatus	0x001C	W	0x00000000	Register TraceAlarmStatus is a read-only register that indicates which LUT or filter has been matched by a packet.
Probe_TraceAlarmClr	0x0020	W	0x00000000	Setting a bit to 1 in register TraceAlarmClr clears the corresponding bit in register TraceAlarmStatus.
Probe_StatPeriod	0x0024	W	0x00000000	Register StatPeriod is a 5-bit register that sets a period ranging from 2 cycles to 2 gigacycles of the probe clock, during which statistics are collected before being dumped automatically.
Probe_StatGo	0x0028	W	0x00000000	Writing to the 1-bit pulse register StatGo generates a statistics dump.
Probe_StatAlarmMin	0x002C	W	0x00000000	Register StatAlarmMin specifies the lower threshold used to trigger the statistics alarm.
Probe_StatAlarmMax	0x0034	W	0x00000000	Register StatAlarmMax specifies the upper threshold used to trigger the statistics alarm.

Name	Offset	Size	Reset Value	Description
Probe_StatAlarmStatus	0x003C	W	0x00000000	StatAlarmStatus is a 2-bit read-only register relative to statistics counter.
Probe_StatAlarmClr	0x0040	W	0x00000000	State alarm clear register.
Probe_StatAlarmEn	0x0044	W	0x00000001	StatAlarm output signals enable register.
Probe_Filters_0_RouteIdBase	0x0080	W	0x00000000	Specifies which value of RouteId should be used to filter packets.
Probe_Filters_0_RouteIdMask	0x0084	W	0x00000000	Specifies the mask used on RouteId to filter packets.
Probe_Filters_0_AddrBase_Low	0x0088	W	0x00000000	Specifies the values of the lower transport address bits, used in conjunction with register Filters_N_WindowSize, to filter packets.
Probe_Filters_0_AddrBase_High	0x008C	W	0x00000000	Specifies the values of the upper transport address bits, used in conjunction with register Filters_N_WindowSize to filter packets.
Probe_Filters_0_WindowSize	0x0090	W	0x00000000	Specifies the encoded address mask used to filter packets.
Probe_Filters_0_SecurityBase	0x0094	W	0x00000000	Specifies, for filter n, the values to be matched against bits in the packet header field Security of transport packets.
Probe_Filters_0_SecurityMask	0x0098	W	0x00000000	Specifies, for filter n, which bits of packet header field Security are used to filter transport packets.
Probe_Filters_0_Opcode	0x009C	W	0x00000000	Contains four fields that control which packet opcodes are used to select packets by Filter N.
Probe_Filters_0_Status	0x00A0	W	0x00000000	A 2-bit register that sets criteria for filter n based on packet status type.
Probe_Filters_0_Length	0x00A4	W	0x00000000	Register Filters_N_Length is 4-bit register that selects candidate packets if the number of bytes is less than or equal to 2*FILTERS_N_LENGTH.
Probe_Filters_0_Urgency	0x00A8	W	0x00000000	Specifies the minimum urgency level used to filter packets.
Probe_Filters_0_UserBase	0x00AC	W	0x00000000	Specifies, for filter n, the values to be matched against the lower bits in the packet header field User of transport packets.
Probe_Filters_0_UserMask	0x00B0	W	0x00000000	Specifies, for filter n, which lower bits of packet header field User are used to filter transport packets.
Probe_Filters_1_RouteIdBase	0x00E0	W	0x00000000	Specifies which value of RouteId should be used to filter packets.
Probe_Filters_1_RouteIdMask	0x00E4	W	0x00000000	Specifies the mask used on RouteId to filter packets.

Name	Offset	Size	Reset Value	Description
Probe_Filters_1_AddrBase_Low	0x00E8	W	0x00000000	Specifies the values of the lower transport address bits, used in conjunction with register Filters_N_WindowSize, to filter packets.
Probe_Filters_1_AddrBase_High	0x00EC	W	0x00000000	Specifies the values of the upper transport address bits, used in conjunction with register Filters_N_WindowSize to filter packets.
Probe_Filters_1_WindowSize	0x00F0	W	0x00000000	Specifies the encoded address mask used to filter packets.
Probe_Filters_1_SecurityBase	0x00F4	W	0x00000000	Specifies, for filter n, the values to be matched against bits in the packet header field Security of transport packets.
Probe_Filters_1_SecurityMask	0x00F8	W	0x00000000	Specifies, for filter n, which bits of packet header field Security are used to filter transport packets.
Probe_Filters_1_Opcode	0x00FC	W	0x00000000	Contains four fields that control which packet opcodes are used to select packets by Filter N.
Probe_Filters_1_Status	0x0100	W	0x00000000	A 2-bit register that sets criteria for filter n based on packet status type.
Probe_Filters_1_Length	0x0104	W	0x00000000	Register Filters_N_Length is 4-bit register that selects candidate packets if the number of bytes is less than or equal to 2*FILTERS_N_LENGTH.
Probe_Filters_1_Urgency	0x0108	W	0x00000000	Specifies the minimum urgency level used to filter packets.
Probe_Filters_1_UserBase	0x010C	W	0x00000000	Specifies, for filter n, the values to be matched against the lower bits in the packet header field User of transport packets.
Probe_Filters_1_UserMask	0x0110	W	0x00000000	Specifies, for filter n, which lower bits of packet header field User are used to filter transport packets.
Probe_Filters_2_RouteIdBase	0x0140	W	0x00000000	Specifies which value of RouteId should be used to filter packets.
Probe_Filters_2_RouteIdMask	0x0144	W	0x00000000	Specifies the mask used on RouteId to filter packets.
Probe_Filters_2_AddrBase_Low	0x0148	W	0x00000000	Specifies the values of the lower transport address bits, used in conjunction with register Filters_N_WindowSize, to filter packets.
Probe_Filters_2_AddrBase_High	0x014C	W	0x00000000	Specifies the values of the upper transport address bits, used in conjunction with register Filters_N_WindowSize to filter packets.

Name	Offset	Size	Reset Value	Description
Probe_Filters_2_WindowSize	0x0150	W	0x00000000	Specifies the encoded address mask used to filter packets.
Probe_Filters_2_SecurityBase	0x0154	W	0x00000000	Specifies, for filter n, the values to be matched against bits in the packet header field Security of transport packets.
Probe_Filters_2_SecurityMask	0x0158	W	0x00000000	Specifies, for filter n, which bits of packet header field Security are used to filter transport packets.
Probe_Filters_2_Opcode	0x015C	W	0x00000000	Contains four fields that control which packet opcodes are used to select packets by Filter N.
Probe_Filters_2_Status	0x0160	W	0x00000000	A 2-bit register that sets criteria for filter n based on packet status type.
Probe_Filters_2_Length	0x0164	W	0x00000000	Register Filters_N_Length is 4-bit register that selects candidate packets if the number of bytes is less than or equal to 2*FILTERS_N_LENGTH.
Probe_Filters_2_Urgency	0x0168	W	0x00000000	Specifies the minimum urgency level used to filter packets.
Probe_Filters_2_UserBase	0x016C	W	0x00000000	Specifies, for filter n, the values to be matched against the lower bits in the packet header field User of transport packets.
Probe_Filters_2_UserMask	0x0170	W	0x00000000	Specifies, for filter n, which lower bits of packet header field User are used to filter transport packets.
Probe_Filters_3_RouteIdBase	0x01A0	W	0x00000000	Specifies which value of RouteId should be used to filter packets.
Probe_Filters_3_RouteIdMask	0x01A4	W	0x00000000	Specifies the mask used on RouteId to filter packets.
Probe_Filters_3_AddrBase_Low	0x01A8	W	0x00000000	Specifies the values of the lower transport address bits, used in conjunction with register Filters_N_WindowSize, to filter packets.
Probe_Filters_3_AddrBase_High	0x01AC	W	0x00000000	Specifies the values of the upper transport address bits, used in conjunction with register Filters_N_WindowSize to filter packets.
Probe_Filters_3_WindowSize	0x01B0	W	0x00000000	Specifies the encoded address mask used to filter packets.
Probe_Filters_3_SecurityBase	0x01B4	W	0x00000000	Specifies, for filter n, the values to be matched against bits in the packet header field Security of transport packets.
Probe_Filters_3_SecurityMask	0x01B8	W	0x00000000	Specifies, for filter n, which bits of packet header field Security are used to filter transport packets.

Name	Offset	Size	Reset Value	Description
Probe_Filters_3_Opcode	0x01BC	W	0x00000000	Contains four fields that control which packet opcodes are used to select packets by Filter N.
Probe_Filters_3_Status	0x01C0	W	0x00000000	A 2-bit register that sets criteria for filter n based on packet status type.
Probe_Filters_3_Length	0x01C4	W	0x00000000	Register Filters_N_Length is 4-bit register that selects candidate packets if the number of bytes is less than or equal to 2*FILTERS_N_LENGTH.
Probe_Filters_3_Urgency	0x01C8	W	0x00000000	Specifies the minimum urgency level used to filter packets.
Probe_Filters_3_UserBase	0x01CC	W	0x00000000	Specifies, for filter n, the values to be matched against the lower bits in the packet header field User of transport packets.
Probe_Filters_3_UserMask	0x01D0	W	0x00000000	Specifies, for filter n, which lower bits of packet header field User are used to filter transport packets.
Probe_Counters_0_Src	0x0204	W	0x00000000	Specifies, for counter m, the type of event source used to increment the counter.
Probe_Counters_0_Alarm Mode	0x0208	W	0x00000000	Defines statistics alarm counter behavior.
Probe_Counters_0_Val	0x020C	W	0x00000000	Contain the statistics counter values.
Probe_Counters_1_Src	0x0214	W	0x00000000	Specifies, for counter m, the type of event source used to increment the counter.
Probe_Counters_1_Alarm Mode	0x0218	W	0x00000000	Defines statistics alarm counter behavior.
Probe_Counters_1_Val	0x021C	W	0x00000000	Contain the statistics counter values.
Probe_Counters_2_Src	0x0224	W	0x00000000	Specifies, for counter m, the type of event source used to increment the counter.
Probe_Counters_2_Alarm Mode	0x0228	W	0x00000000	Defines statistics alarm counter behavior.
Probe_Counters_2_Val	0x022C	W	0x00000000	Contain the statistics counter values.
Probe_Counters_3_Src	0x0234	W	0x00000000	Specifies, for counter m, the type of event source used to increment the counter.
Probe_Counters_3_Alarm Mode	0x0238	W	0x00000000	Defines statistics alarm counter behavior.
Probe_Counters_3_Val	0x023C	W	0x00000000	Contain the statistics counter values.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.8 Probe Detail Registers Description

Probe_Id_CoreId

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x194c40	CoreChecksum Field containing a checksum of the parameters of the IP. Reset value is different for each probe.
7:0	RO	0x06	CoreTypeId Field identifying the type of IP.

Probe_Id_RevisionId
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x3c9d4e	BuildId Field containing the build revision of the software used to generate the IP HDL code.
7:0	RO	0x00	UserId Field containing a user defined value, not used anywhere inside the IP itself.

Probe_MainCtl
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	FiltByteAlwaysChainableEn When set to 0, filters are mapped to all statistic counters when counting bytes or enabled bytes. Therefore, only filter events mapped to even counters can be counted using a pair of chained counters. When set to 1, filters are mapped only to even statistic counters when counting bytes or enabled bytes. Thus events from any filter can be counted using a pair of chained counters.
6	RW	0x0	IntrusiveMode When set to 1, register field IntrusiveMode enables trace operation in Intrusive flow-control mode. When set to 0, the register enables trace operation in Overflow flow-control mode.
5	RW	0x0	StatCondDump When set, register field StatCondDump enables the dump of a statistics frame to the range of counter values set for registers StatAlarmMin, StatAlarmMax, and AlarmMode. This field also renders register StatAlarmStatus inoperative. When parameter statisticsCounterAlarm is set to False, the StatCondDump register bit is reserved.
4	RW	0x0	AlarmEn When set, register field AlarmEn enables the probe to collect alarm-related information. When the register field bit is null, both TraceAlarm and StatAlarm outputs are driven to 0.
3	RW	0x0	StatEn When set to 1, register field StatEn enables statistics profiling. The probe sends statistics results to the output for signal ObsTx. All statistics counters are cleared when the StatEn bit goes from 0 to 1. When set to 0, counters are disabled.
2	RW	0x0	PayloadEn Register field PayloadEn, when set to 1, enables traces to contain headers and payload. When set to 0, only headers are reported.
1	RW	0x0	TraceEn Register field TraceEn enables the probe to send filtered packets (Trace) on the ObsTx observation output.

Bit	Attr	Reset Value	Description
0	RW	0x0	ErrEn Register field ErrEn enables the probe to send on the ObsTx output any packet with Error status, independently of filtering mechanisms, thus constituting a simple supplementary global filter.

Probe_CfgCtl

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	Active Register field Active is used to inform software that the probe is active. Probe configuration is not allowed during the active state. This bit is raised when bit GlobalEn is set, and is cleared a few cycles after setting GlobalEn to zero (probe is Idle).
0	RW	0x0	GlobalEn Enables or disables the tracing and statistics collection subsystems of the packet probe.

Probe_FilterLut

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	FilterLut Register FilterLut contains a look-up table that is used to combine filter outputs in order to trace packets. Packet tracing is enabled when the FilterLut bit of index (FNout ... F0out) is equal to 1. The number of bits in register FilterLut is determined by the setting for parameter nFilter, calculated as 2**nFilter. When parameter nFilter is set to None, FilterLut is reserved.

Probe_TraceAlarmEn

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	TraceAlarmEn Register TraceAlarmEn controls which lookup table or filter can set the TraceAlarm signal output once the trace alarm status is set. The number of bits in register TraceAlarmEn is determined by the value set for parameter nFilter + 1. Bit nFilter controls the lookup table output, and bits (nFilter-1:0) control the corresponding filter output. When parameter nFilter is set to None, TraceAlarmEn is reserved.

Probe_TraceAlarmStatus

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RO	0x00	TraceAlarmStatus Register TraceAlarmStatus is a read-only register that indicates which lookup table or filter has been matched by a packet, independently of register TraceAlarmEn bit configuration. The number of bits in TraceAlarmStatus is determined by the value set for parameter nFilter + 1. When nFilter is set to None, TraceAlarmStatus is reserved.

Probe_TraceAlarmClr

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	TraceAlarmClr Setting a bit to 1 in register TraceAlarmClr clears the corresponding bit in register TraceAlarmStatus. The number of bits in register TraceAlarmClr is equal to (nFilter + 1). When nFilter is set to 0, TraceAlarmClr is reserved. NOTE: The written value is not stored in TraceAlarmClr. A read always returns 0.

Probe_StatPeriod

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	StatPeriod Register StatPeriod is a 5-bit register that sets a period, within a range of 2 cycles to 2 gigacycles, during which statistics are collected before being dumped automatically. Setting the register implicitly enables automatic mode operation for statistics collection. The period is calculated with the formula: N_Cycle = 2**StatPeriodWhen register StatPeriod is set to its default value 0, automatic dump mode is disabled, and register StatGo is activated for manual mode operation. Note: When parameter statisticsCollection is set to False, StatPeriod is reserved.

Probe_StatGo

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	StatGo Writing a 1 to the 1-bit pulse register StatGo generates a statistics dump. The register is active when statistics collection operates in manual mode, that is, when register StatPeriod is set to 0. The written value is not stored in StatGo. A read always returns 0.

Probe_StatAlarmMin

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	StatAlarmMin Register StatAlarmMin contains the minimum count value used in statistics alarm comparisons.

Probe_StatAlarmMax

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	StatAlarmMax Register StatAlarmMax contains the maximum count value used in statistics alarm comparisons.

Probe_StatAlarmStatus

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	StatAlarmStatus Register StatAlarmStatus is a read-only 1-bit register indicating that at least one statistics counter has exceeded the programmed values for registers StatAlarmMin or StatAlarmMax. Output signal StatAlarm is equal to the values stored in register MainCtl fields StatAlarmStatus and AlarmEn.

Probe_StatAlarmClr
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	StatAlarmClr Register StatAlarmClr is a 1-bit register. Writing a 1 to this register clears the StatAlarmStatus register bit. When parameter statisticsCounterAlarm is set to False, StatAlarmClr is reserved. NOTE The written value is not stored in StatAlarmClr. A read always returns 0.

Probe_StatAlarmEn
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	StatAlarmEn Register StatAlarmEn is a 1-bit register. When set to 0 it masks StatAlarm and CtiTrigOut(1) signal interrupts.

Probe_Filters_0_RouteIdBase
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	Filters_0_RouteIdBase Register RouteIdBase contains the RouteId-lsbFilterRouteId bits base used to filter packets.

Probe_Filters_0_RouteIdMask
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	Filters_0_RouteIdMask Register RouteIdMask contains the RouteId-lsbFilterRouteId mask used to filter packets. A packet is a candidate when packet.RouteId>>lsbFilterRouteId & RouteIdMask = RouteIdBase & RouteIdMask.

Probe_Filters_0_AddrBase_Low
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filters_0_AddrBase_Low Address LSB register.

Probe_Filters_0_AddrBase_High
Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	Filters_0_AddrBase_High Address MSB register.

Probe_Filters_0_WindowSize

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	Filters_0_WindowSize Register WindowSize contains the encoded address mask used to filter packets. The effective Mask value is equal to ~(2max(WindowSize, packet.Len) - 1). A packet is a candidate when packet.Addr & Mask = AddrBase & Mask. This allows filtering of packets having an intersection with the AddrBase/WindowSize burst aligned region, even if the region is smaller than the packet.

Probe_Filters_0_SecurityBase

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_0_SecurityBase Register SecurityBase contains the security base used to filter packets.

Probe_Filters_0_SecurityMask

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_0_SecurityMask Register SecurityMask is contains the security mask used to filter packets. A packet is a candidate when: packet. Security & SecurityMask = SecurityBase & SecurityMasks.

Probe_Filters_0_Opcode

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	UrgEn Selects URG packets (urgency).
2	RW	0x0	LockEn Selects RDX-WR, RDL, WRC and Linked sequence.
1	RW	0x0	WrEn Selects WR packets.
0	RW	0x0	RdEn Selects RD packets.

Probe_Filters_0_Status

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	RspEn Selects RSP and FAIL-CONT status packets.

Bit	Attr	Reset Value	Description
0	RW	0x0	ReqEn Selects REQ status packets.

Probe_Filters_0_Length
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	Filters_0_Length Register Length is 4-bit register that selects candidate packets if their number of bytes is less than or equal to 2**Length.

Probe_Filters_0_Urgency
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	Filters_0_Urgency Register Urgency contains the minimum urgency level used to filter packets. A packet is a candidate when its socket urgency is greater than or equal to the urgency specified in the register.

Probe_Filters_0_UserBase
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	Filters_0_UserBase Register UserBase is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user base value that is employed in filtering packets.

Probe_Filters_0_UserMask
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	Filters_0_UserMask Register UserMask is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user mask that is employed in filtering packets. A packet is a candidate for trace or statistic collection when packet.User & UserMask = UserBase & UserMask.

Probe_Filters_1_RouteIdBase
Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	Filters_1_RouteIdBase Register RouteIdBase contains the RouteId-IsbFilterRouteId bits base used to filter packets.

Probe_Filters_1_RouteIdMask
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

Bit	Attr	Reset Value	Description
25:0	RW	0x0000000	Filters_1_RouteIdMask Register RouteIdMask contains the RouteId-lsbFilterRouteId mask used to filter packets. A packet is a candidate when packet.RouteId>>lsbFilterRouteId & RouteIdMask = RouteIdBase & RouteIdMask.

Probe_Filters_1_AddrBase_Low
Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filters_1_AddrBase_Low Address LSB register.

Probe_Filters_1_AddrBase_High
Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	Filters_1_AddrBase_High Address MSB register.

Probe_Filters_1_WindowSize
Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	Filters_1_WindowSize Register WindowSize contains the encoded address mask used to filter packets. The effective Mask value is equal to ~(2max(WindowSize, packet.Len) - 1). A packet is a candidate when packet.Addr & Mask = AddrBase & Mask. This allows filtering of packets having an intersection with the AddrBase/WindowSize burst aligned region, even if the region is smaller than the packet.

Probe_Filters_1_SecurityBase
Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_1_SecurityBase Register SecurityBase contains the security base used to filter packets.

Probe_Filters_1_SecurityMask
Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_1_SecurityMask Register SecurityMask is contains the security mask used to filter packets. A packet is a candidate when: packet.Security & SecurityMask = SecurityBase & SecurityMasks.

Probe_Filters_1_Opcode
Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	UrgEn Selects URG packets (urgency).
2	RW	0x0	LockEn Selects RDX-WR, RDL, WRC and Linked sequence.
1	RW	0x0	WrEn Selects WR packets.
0	RW	0x0	RdEn Selects RD packets.

Probe_Filters_1_Status
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	RspEn Selects RSP and FAIL-CONT status packets.
0	RW	0x0	ReqEn Selects REQ status packets.

Probe_Filters_1_Length
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	Filters_1_Length Register Length is 4-bit register that selects candidate packets if their number of bytes is less than or equal to 2**Length.

Probe_Filters_1_Urgency
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	Filters_1_Urgency Register Urgency contains the minimum urgency level used to filter packets. A packet is a candidate when its socket urgency is greater than or equal to the urgency specified in the register.

Probe_Filters_1_UserBase
Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	Filters_1_UserBase Register UserBase is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user base value that is employed in filtering packets.

Probe_Filters_1_UserMask
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	Filters_1_UserMask Register UserMask is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user mask that is employed in filtering packets. A packet is a candidate for trace or statistic collection when packet.User & UserMask = UserBase & UserMask.

Probe_Filters_2_RouteIdBase

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	Filters_2_RouteIdBase Register RouteIdBase contains the RouteId-lsbFilterRouteId bits base used to filter packets.

Probe_Filters_2_RouteIdMask

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	Filters_2_RouteIdMask Register RouteIdMask contains the RouteId-lsbFilterRouteId mask used to filter packets. A packet is a candidate when packet.RouteId>>lsbFilterRouteId & RouteIdMask = RouteIdBase & RouteIdMask.

Probe_Filters_2_AddrBase_Low

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filters_2_AddrBase_Low Address LSB register.

Probe_Filters_2_AddrBase_High

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_2_AddrBase_High Address MSB register.

Probe_Filters_2_WindowSize

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_2_WindowSize Register WindowSize contains the encoded address mask used to filter packets. The effective Mask value is equal to ~(2max(WindowSize, packet.Len) - 1). A packet is a candidate when packet.Addr & Mask = AddrBase & Mask. This allows filtering of packets having an intersection with the AddrBase/WindowSize burst aligned region, even if the region is smaller than the packet.

Probe_Filters_2_SecurityBase

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_2_SecurityBase Register SecurityBase contains the security base used to filter packets.

Probe_Filters_2_SecurityMask
Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_2_SecurityMask Register SecurityMask is contains the security mask used to filter packets. A packet is a candidate when: packet.Security & SecurityMask = SecurityBase & SecurityMasks.

Probe_Filters_2_Opcode
Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	UrgEn Selects URG packets (urgency).
2	RW	0x0	LockEn Selects RDX-WR, RDL, WRC and Linked sequence.
1	RW	0x0	WrEn Selects WR packets.
0	RW	0x0	RdEn Selects RD packets.

Probe_Filters_2_Status
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	RspEn Selects RSP and FAIL-CONT status packets.
0	RW	0x0	ReqEn Selects REQ status packets.

Probe_Filters_2_Length
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	Filters_2_Length Register Length is 4-bit register that selects candidate packets if their number of bytes is less than or equal to 2**Length.

Probe_Filters_2_Urgency
Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	Filters_2_Urgency Register Urgency contains the minimum urgency level used to filter packets. A packet is a candidate when its socket urgency is greater than or equal to the urgency specified in the register.

Probe_Filters_2_UserBase

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	Filters_2_UserBase Register UserBase is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user base value that is employed in filtering packets.

Probe_Filters_2_UserMask

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	Filters_2_UserMask Register UserMask is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user mask that is employed in filtering packets. A packet is a candidate for trace or statistic collection when packet.User & UserMask = UserBase & UserMask.

Probe_Filters_3_RouteIdBase

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	Filters_3_RouteIdBase Register RouteIdBase contains the RouteId-lsbFilterRouteId bits base used to filter packets.

Probe_Filters_3_RouteIdMask

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	Filters_3_RouteIdMask Register RouteIdMask contains the RouteId-lsbFilterRouteId mask used to filter packets. A packet is a candidate when packet.RouteId>>lsbFilterRouteId & RouteIdMask = RouteIdBase & RouteIdMask.

Probe_Filters_3_AddrBase_Low

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filters_3_AddrBase_Low Address LSB register.

Probe_Filters_3_AddrBase_High

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	Filters_3_AddrBase_High Address MSB register.

Probe_Filters_3_WindowSize

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	Filters_3_WindowSize Register WindowSize contains the encoded address mask used to filter packets. The effective Mask value is equal to ~(2max(WindowSize, packet.Len) - 1). A packet is a candidate when packet.Addr & Mask = AddrBase & Mask. This allows filtering of packets having an intersection with the AddrBase/WindowSize burst aligned region, even if the region is smaller than the packet.

Probe_Filters_3_SecurityBase

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_3_SecurityBase Register SecurityBase contains the security base used to filter packets.

Probe_Filters_3_SecurityMask

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Filters_3_SecurityMask Register SecurityMask is contains the security mask used to filter packets. A packet is a candidate when: packet.Security & SecurityMask = SecurityBase & SecurityMasks.

Probe_Filters_3_Opcode

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	UrgEn Selects URG packets (urgency).
2	RW	0x0	LockEn Selects RDX-WR, RDL, WRC and Linked sequence.
1	RW	0x0	WrEn Selects WR packets.
0	RW	0x0	RdEn Selects RD packets.

Probe_Filters_3_Status

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	RspEn Selects RSP and FAIL-CONT status packets.
0	RW	0x0	ReqEn Selects REQ status packets.

Probe_Filters_3_Length

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	Filters_3_Length Register Length is 4-bit register that selects candidate packets if their number of bytes is less than or equal to 2**Length.

Probe_Filters_3_Urgency
Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	Filters_3_Urgency Register Urgency contains the minimum urgency level used to filter packets. A packet is a candidate when its socket urgency is greater than or equal to the urgency specified in the register.

Probe_Filters_3_UserBase
Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	Filters_3_UserBase Register UserBase is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user base value that is employed in filtering packets.

Probe_Filters_3_UserMask
Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	Filters_3_UserMask Register UserMask is available when parameter useUserFilter is set to True. Register size is determined by parameter wUser. The register stores a user mask that is employed in filtering packets. A packet is a candidate for trace or statistic collection when packet.User & UserMask = UserBase & UserMask.

Probe_Counters_0_Src
Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event 5'h00: OFF, counter disabled. 5'h01: CYCLE, probe clock cycles. 5'h02: IDLE, idle cycles during which no packet data is observed. 5'h03: XFER, transfer cycles during which packet data is transferred. 5'h04: BUSY, busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05: WAIT, wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06: PKT, packets. 5'h07: LUT, packets selected by the LUT. 5'h08: BYTE, total number of payload bytes. 5'h09: PRESS, clock cycles with pressure level > 0. 5'h0A: PRESS, clock cycles with pressure level > 1. 5'h0B: PRESS, clock cycles with pressure level > 2. 5'h0C: FILT0, packets selected by Filter 0. 5'h0D: FILT1, packets selected by Filter 1. 5'h0E: FILT2, packets selected by Filter 2. 5'h0F: FILT3, packets selected by Filter 3. 5'h10: CHAIN, carry from counter 2m to counter 2m + 1. 5'h11: LUT_BYTE_EN, enabled payload byte in packets selected by the LUT. 5'h12: LUT_BYTE, total number of payload bytes in packets selected by the LUT. 5'h13: FILT_BYTE_EN, enabled payload byte in packets selected by the associated filter. 5'h14: FILT_BYTE, total number of payload bytes in packets selected by the associated filter. Others: Reserved

Probe_Counters_0_AlarmMode

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	Counters_0_AlarmMode Register AlarmMode is a 2-bit register that defines the statistics-alarm behavior of the counter. 2'b00: OFF, the comparison is disabled. 2'b01: MIN, if the value of the counter is less than the StatAlarmMin register at the dump period, the StatAlarmStatus bit is set. 2'b10: MAX, if the value of the counter is greater than the StatAlarmMax register at the dump period, the StatAlarmStatus bit is set. 2'b11: MIN_MAX, if the value of the counter is less than the StatAlarmMin register or greater than the StatAlarmMax register at the dump period, the corresponding StatAlarmStatus bit is set.

Probe_Counters_0_Val

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	Counters_0_Val Register Val contains the statistics counter value either pending StatAlarm output, or when statistics collection is suspended subsequent to triggers or signal statSuspend.

Probe_Counters_1_Src

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	IntEvent Internal packet event 5'h00: OFF, counter disabled. 5'h01: CYCLE, probe clock cycles. 5'h02: IDLE, idle cycles during which no packet data is observed. 5'h03: XFER, transfer cycles during which packet data is transferred. 5'h04: BUSY, busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05: WAIT, wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06: PKT, packets. 5'h07: LUT, packets selected by the LUT. 5'h08: BYTE, total number of payload bytes. 5'h09: PRESS, clock cycles with pressure level > 0. 5'h0A: PRESS, clock cycles with pressure level > 1. 5'h0B: PRESS, clock cycles with pressure level > 2. 5'h0C: FILT0, packets selected by Filter 0. 5'h0D: FILT1, packets selected by Filter 1. 5'h0E: FILT2, packets selected by Filter 2. 5'h0F: FILT3, packets selected by Filter 3. 5'h10: CHAIN, carry from counter 2m to counter 2m + 1. 5'h11: LUT_BYTE_EN, enabled payload byte in packets selected by the LUT. 5'h12: LUT_BYTE, total number of payload bytes in packets selected by the LUT. 5'h13: FILT_BYTE_EN, enabled payload byte in packets selected by the associated filter. 5'h14: FILT_BYTE, total number of payload bytes in packets selected by the associated filter. Others: Reserved

Probe_Counters_1_AlarmMode

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	Counters_1_AlarmMode Register AlarmMode is a 2-bit register that defines the statistics-alarm behavior of the counter. 2'b00: OFF, the comparison is disabled. 2'b01: MIN, if the value of the counter is less than the StatAlarmMin register at the dump period, the StatAlarmStatus bit is set. 2'b10: MAX, if the value of the counter is greater than the StatAlarmMax register at the dump period, the StatAlarmStatus bit is set. 2'b11: MIN_MAX, if the value of the counter is less than the StatAlarmMin register or greater than the StatAlarmMax register at the dump period, the corresponding StatAlarmStatus bit is set.

Probe_Counters_1_Val
Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	Counters_1_Val Register Val contains the statistics counter value either pending StatAlarm output, or when statistics collection is suspended subsequent to triggers or signal statSuspend.

Probe_Counters_2_Src
Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event 5'h00: OFF, counter disabled. 5'h01: CYCLE, probe clock cycles. 5'h02: IDLE, idle cycles during which no packet data is observed. 5'h03: XFER, transfer cycles during which packet data is transferred. 5'h04: BUSY, busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05: WAIT, wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06: PKT, packets. 5'h07: LUT, packets selected by the LUT. 5'h08: BYTE, total number of payload bytes. 5'h09: PRESS, clock cycles with pressure level > 0. 5'h0A: PRESS, clock cycles with pressure level > 1. 5'h0B: PRESS, clock cycles with pressure level > 2. 5'h0C: FILT0, packets selected by Filter 0. 5'h0D: FILT1, packets selected by Filter 1. 5'h0E: FILT2, packets selected by Filter 2. 5'h0F: FILT3, packets selected by Filter 3. 5'h10: CHAIN, carry from counter 2m to counter 2m + 1. 5'h11: LUT_BYTE_EN, enabled payload byte in packets selected by the LUT. 5'h12: LUT_BYTE, total number of payload bytes in packets selected by the LUT. 5'h13: FILT_BYTE_EN, enabled payload byte in packets selected by the associated filter. 5'h14: FILT_BYTE, total number of payload bytes in packets selected by the associated filter. Others: Reserved

Probe_Counters_2_AlarmMode

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	Counters_2_AlarmMode Register AlarmMode is a 2-bit register that defines the statistics-alarm behavior of the counter. 2'b00: OFF, the comparison is disabled. 2'b01: MIN, if the value of the counter is less than the StatAlarmMin register at the dump period, the StatAlarmStatus bit is set. 2'b10: MAX, if the value of the counter is greater than the StatAlarmMax register at the dump period, the StatAlarmStatus bit is set. 2'b11: MIN_MAX, if the value of the counter is less than the StatAlarmMin register or greater than the StatAlarmMax register at the dump period, the corresponding StatAlarmStatus bit is set.

Probe_Counters_2_Val

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	Counters_2_Val Register Val contains the statistics counter value either pending StatAlarm output, or when statistics collection is suspended subsequent to triggers or signal statSuspend.

Probe_Counters_3_Src

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	IntEvent Internal packet event 5'h00: OFF, counter disabled. 5'h01: CYCLE, probe clock cycles. 5'h02: IDLE, idle cycles during which no packet data is observed. 5'h03: XFER, transfer cycles during which packet data is transferred. 5'h04: BUSY, busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05: WAIT, wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06: PKT, packets. 5'h07: LUT, packets selected by the LUT. 5'h08: BYTE, total number of payload bytes. 5'h09: PRESS, clock cycles with pressure level > 0. 5'h0A: PRESS, clock cycles with pressure level > 1. 5'h0B: PRESS, clock cycles with pressure level > 2. 5'h0C: FILT0, packets selected by Filter 0. 5'h0D: FILT1, packets selected by Filter 1. 5'h0E: FILT2, packets selected by Filter 2. 5'h0F: FILT3, packets selected by Filter 3. 5'h10: CHAIN, carry from counter 2m to counter 2m + 1. 5'h11: LUT_BYTE_EN, enabled payload byte in packets selected by the LUT. 5'h12: LUT_BYTE, total number of payload bytes in packets selected by the LUT. 5'h13: FILT_BYTE_EN, enabled payload byte in packets selected by the associated filter. 5'h14: FILT_BYTE, total number of payload bytes in packets selected by the associated filter. Others: Reserved

Probe_Counters_3_AlarmMode

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	Counters_3_AlarmMode Register AlarmMode is a 2-bit register that defines the statistics-alarm behavior of the counter. 2'b00: OFF, the comparison is disabled. 2'b01: MIN, if the value of the counter is less than the StatAlarmMin register at the dump period, the StatAlarmStatus bit is set. 2'b10: MAX, if the value of the counter is greater than the StatAlarmMax register at the dump period, the StatAlarmStatus bit is set. 2'b11: MIN_MAX, if the value of the counter is less than the StatAlarmMin register or greater than the StatAlarmMax register at the dump period, the corresponding StatAlarmStatus bit is set.

Probe_Counters_3_Val
Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	Counters_3_Val Register Val is a read-only register that is always present. The register contains the statistics counter value either pending StatAlarm output, or when statistics collection is suspended subsequent to triggers or signal statSuspend.

1.5 Application Notes

1.5.1 Idle Request

The main interconnect supports flushing the ongoing transaction when the software need to do so. If the GPU power domain needs to disconnect from the main interconnect, Idle request has to be sent to GPU BIU, the BIU will respond an "ACK", and when it's ready to be disconnect, one Idle signal will be sent out. Then, if GPU still has transaction to be sent to the DDR scheduler, it will be stalled by the BIU.

If the GPU system power domain is disconnected as the above flow, then CPU wants to access to the GPU system, it will response error or held to CPU according to the corresponding GRF register setting.

The sequence is like following figure shows:

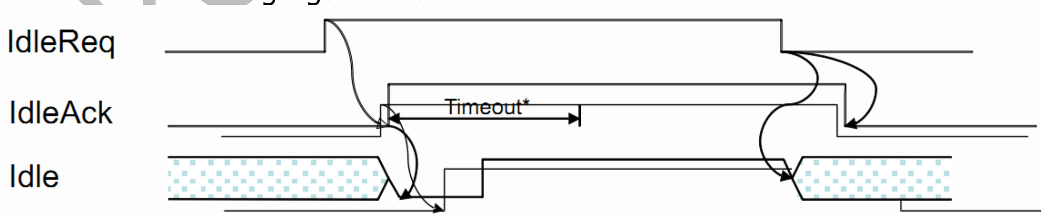


Fig. 1-3 Idle request

The idle request is controlled by PMU.

1.5.2 Counting Packets Over a Fixed Period

The following programming sequence counts packets at a given probe point using statistic counter 0.

- Select the interesting probe listed in Table 1-3.
- Set field *StatEn* to 1 in register *MainCtl.*
- Set register *Counters_0_Src* to 0x6 (PKT) to count packets.
- Specify the period during which the packets should be counted by setting register StatPeriod to: $\log_2$(interval expressed in number of probe clock cycles).
- Set field *GlobalEn* of register *CfgCtl* to 1 to enable packet counting.

Once time $2^{StatPeriod}$ has elapsed, the number of packets counted is dumped to the observer and can be read from *Counters_0_Val.*

1.5.3 Configuring and Managing the Statistics Alarm

The following programming sequence asserts the statistics alarm signal StatAlarm if the number of packets exceeds a specified threshold when the statistics dump occurs.

- Set register StatAlarmMax to the number of packets that should trigger the statistics alarm.
- Set the counter alarm mode to MAX by setting register Counters_0_AlarmMode to 2. This triggers the alarm if the count value is greater than StatAlarmMax.
- Set field StatCondDump to 0 in register MainCtl to generate a statistics alarm event and freeze the statistic counter value if the statistic counter exceeds the value of StatAlarmMax when a statistics dump occurs.
- Set field AlarmEn to 1 in register MainCtl and ensure that bit 0 of register StatAlarmEn is set to its default value of 1 to activate signal StatAlarm in the event of a statistics alarm. In the event that StatAlarm is asserted when the statistics dump period expires, the interrupt service routine should:
  1. Read the number of packets contained in register Counters_0_Val.
  2. Clear the statistics alarm by setting bit 0 to 1 in register StatAlarmClr.

Alternatively, the statistics alarm function can be configured to not drive signal StatAlarm when a statistics alarm event occurs. This signal can be disabled by clearing bit 0 of register StatAlarmEn to 0.

1.5.4 Counting Filtered Packets Over a Fixed Period

The following programming sequence counts hits from packet filter 2 using statistic counter 0.

- Set field StatEn to 1 in register MainCtl.
- Set register Counters_0_Src to 0xE (FILT2) to count packets from filter 2.
- Specify the period during which the packets should be counted by setting register StatPeriod to: $\log_2$(interval expressed in number of probe clock cycles).
- Set field GlobalEn of register CfgCtl to 1 to enable packet counting.

Once time $2^{StatPeriod}$ has elapsed, the number of packets counted is dumped to the observer and can be read from Counters_0_Val.

1.5.5 Measuring Bandwidth

The following programming sequence example shows how a packet probe can be used to measure bandwidth at a probe point.

Some important points to note about this example are:

- Statistics counters are chained together to support the maximum theoretical bandwidth. Counter 0 is configured to count bytes; counter 1 increments when counter 0 rolls over.
- The counter values are dumped to an observer after time $2^{StatPeriod}$.
- A maximum bandwidth threshold is defined. A statistics alarm signal is asserted if this threshold is exceeded when statistics data is dumped. The comparison is made against the concatenated value of the two counters.

The programming sequence is as follows:

- Select the interested probe listed in Table 1-3.
- Set field StatEn to 1 in register MainCtl.
- Set register *Counters_0_Src* to 0x8 (BYTES) to count bytes.
- Set register *Counters_1_Src* to 0x10 (CHAIN) to increment when counter 0 wraps.
- Specify the period during which the bytes should be counted by setting register *StatPeriod* to: $\log_2$(interval expressed in number of probe clock cycles).
- Set register Counters_0_AlarmMode to 0x2 (MAX) and Counters_1_AlarmMode to 0x0 (OFF). A statistics alarm will be raised if the combined count of counter 0 and counter 1 is greater than the value specified in register StatAlarmMax.
- Set register StatAlarmMax to a value corresponding to the upper bandwidth limit required to trigger the statistics alarm.

- Set field AlarmEn to 1 in register MainCtl. Ensure bit 0 of register StatAlarmEn is set to 1 (default value) if the alarm output signal StatAlarm is required.
- Set field *GlobalEn* of register *CfgCtl* to 1 to enable the counting of bytes.

In the event that StatAlarm is asserted, the interrupt service routine should:

- Optionally read the number of packets contained in registers Counters_0_Val and Counters_1_Val.
- Clear the statistics alarm by setting bit 0 to 1 in StatAlarmClr. The signal StatAlarm will be de-asserted.

Measuring bandwidth of certain master

If a certain master's bandwidth needs to be measured, the probe corresponding to this master can be find in Table 1-3.

- The register Counters_0_Src should be set to 0x14 (FILT_BYTE) to count payload bytes in packets selected by the associated filter: Filter_0.
- Filters_0_opcode should be set to 0xf to enable all kinds of operation packets.
- Filters_0_status should be set to 0x3 to enable request and response packets.
- Filters_0_length should be set to 0xf to enable all packets whose payload length is less than 2**16 bytes.
- Filters_0_usemask should be set to 0x7f to match the MID field in the packets.
- Filters_0_usebase should be set to the MID value of the master, the MID value of each master can be find in Table 1-3.

1.5.6 Address Hash and DDR Channel Interleave

The interleave granule and address hash control of DSU can be configured by setting DSU_SGRF registers: SGRF_DDR_HASH_CON0 - SGRF_DDR_HASH_CON7. The interleave granule and address hash control of other masters except DSU can be configured by setting BUS_SGRF registers: DDR_BANK_HASH_CTRL - DDR_RANK_MASK0.

Chapter 2 Dynamic Memory Interface (DMC)

2.1 Overview

The DMC includes LPDDR4/4X/5 controller (DDRCTL) and DDRPHY which are a complete memory interface solution for DDR memory subsystems.
The DDRCTL SoC application bus interface supports AXI interface, with flexible address mapper logic allow application-specific mapping of row, column, bank, bank group and rank bits to achieve industry leading high-efficiency, low-latency and high-performance from memory interface.
The DDRPHY provides control features to ease the customer implementation of digitally controlled features of the PHY such as CBT, DQS clean, read training, write training, dvfs training, periodic training and programmable configuration controls.
The DMC supports the following features:

- Support LPDDR4/4X/5
- Support LPDDR4 protocol up to LPDDR4-4267 speed grade and LPDDR5 protocol up to LPDDR5-5500
- Support up to 4-channel interleaving with a maximum of 32GB capacity in total, 2 ranks for each channel
- Support optional 2-channel interleaving with a maximum of 16GB capacity in total, 2 ranks for each channel
- Support scalable and software-controlled 1:2:2(LPDDR4/4X) or 1:1:2/1:1:4 (LPDDR5) frequency ratio
- Support 64-bit DDR data bus width for 4-channel interleaving
- Support 32-bit DDR data bus width for 2-channel interleaving
- Support up to 8-type address mapping
- Support burst16 for LPDDR4/4X/5
- Support different CL/WL latency
- Support 16 bank mode and BG mode for LPDDR5
- Support Link ECC for LPDDR5
- Support open, close, intelligent pre-charge paging policy
- Support advance refresh control
- Support LPDDR4/4X/5 software controlled frequency change
- Support DFI PHY master interface
- Support MC-initiated requests and PHY-initiated requests interface
- Support DFI data low power and ctrl low power interface
- Support hardware low power interface to gate DDRCTL core clock and AXI clock
- Support auto or SW issue entry or exit clock stop/power-down/self-refresh/deep sleep mode
- Support PMU controlled ddrphy entry or exit retention mode
- Support scrambling and descrambling of data written to or read from DDR SDRAM
- Support DDR monitor for following features
  - AMBA 32-bit APB slave interface
  - Each DDR channel embedded with one DDR monitor module
  - Support to monitor DDR read or write address within 8GB address range for each channel
  - Support to observe whether DDR access address within a specified range
  - Support to do the following statistics during a programmed number of time through hardware mode or software mode
    - Statistics about DDR idle cycles
    - Statistics about SR/PD/CKSTOP/SRPD/DFI data low power/DFI ctrl low power for LPDDR4/4X
    - Statistics about SR/PD/CKSTOP/SRPD/DFIDLP/DFICLP/DSM for LPDDR5
    - Statistics about number of activate, read and write cycles for a designated rank or bank
    - Statistics about number of activate, read and write cycles for all banks and ranks in one DDR channel
    - Statistics about read to read, read to write, write to write and write to read page

hit or page miss for a designated rank or bank
- Support monitor interrupt

2.2 Block Diagram

Following is the 4-channel interleaving DMC block diagram.

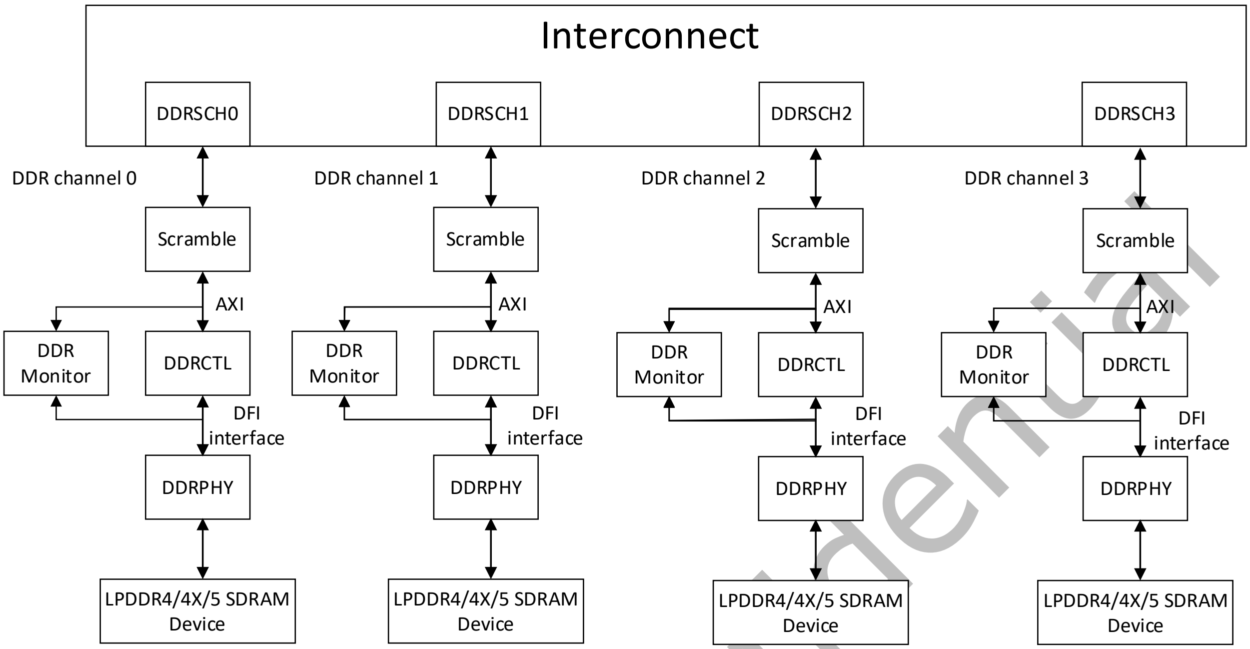


Fig. 2-1 DMC Block Diagram

Please refer to the other chapter for more information about interconnect.

2.3 Function Description

2.3.1 DDRCTL

DDRCTL supports only one AXI Port, it receives AXI transactions from memory schedule (DDRSCH0~3) of interconnect directly or from Scramble module. These transactions are queued internally and scheduled for access in order to the SDRAM while satisfying SDRAM protocol timing requirements. It in turn issues commands on the DFI interface to the DDRPHY block which launches and captures data to and from the SDRAM.

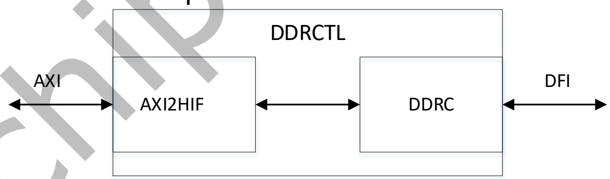


Fig. 2-2 DDRCTL Block Diagram

DDRCTL contains the following main components.

- AXI2HIF block: This block provides the AXI interface to system level and HIF interface to DDRC block. It provides bus protocol handing, data buffering, data bus size conversion and memory burst alignment. Read is stored in a SRAM, read re-order buffer and return in order to the AXI Port.
- DDRC block: This block issues the read/write commands in order, carries out the DRAM page management, issues DRAM maintenance commands, and implement the DFI interface. Write data is stored in an SRAM until its associated command is issued to the PHY. Read data is handled by the response engine in the DDRC and is returned in order on the HIF.

2.3.2 DDRPHY

DDRPHY supports LPDDR4/4X/5 SDRAM and provides physical interface solutions for DDRCTL requiring access to JEDEC compatible SDRAM devices. It is optimized for low power and high speed (up to 4267Mbps for LPDDR4/4X and up to 5500Mbps for LPDDR5) applications with robust timing and small silicon area in14nm process. It supports all JEDEC DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM components in the market. The PHY components contain DDR specialized functional and utility SSTL I/Os up to 2133MHz in SMIC 14nm, critical timing synchronization module (TSM) and a low power/jitter DLLs with programmable fine-grain control for any SDRAM interface.

2.3.3 Scramble

The function of Scramble module is to scramble and descramble data written to or read from DDR SDRAM. This module is defaultly bypassed. If it is enabled, it receives data from DDR memory scheduler (DDRSCH0~3), scramble written data and then send it to the AXI port of DDRCTL. It also descrambles date received from AXI port of DDRCTL and send it back to DDR memory scheduler.

2.4 Register Description

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.1 Registers Summary For DDRCTL

Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG0_FREQ0	0x0000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ0	0x0004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ0	0x0008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ0	0x000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ0	0x0010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ0	0x0014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG6_FREQ0	0x0018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ0	0x001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ0	0x0020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ0	0x0024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG12_FREQ0	0x0030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ0	0x0034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG14_FREQ0	0x0038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ0	0x005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG24_FREQ0	0x0060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ0	0x0064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ0	0x0078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1

Name	Offset	Size	Reset Value	Description
DDRCTL_INITMR0_FREQ0	0x0500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ0	0x0504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ0	0x0508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ0	0x050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ0	0x0580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ0	0x0584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ0	0x0588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ0	0x0590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ0	0x0594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFILPTMG0_FREQ0	0x05A0	W	0x00000000	DFI Low Power Timing Register 0
DDRCTL_DFILPTMG1_FREQ0	0x05A4	W	0x00000700	DFI Low Power Timing Register 1
DDRCTL_DFIUPDTMG0_FREQ0	0x05A8	W	0x00400003	DFI Update Timing Register 0
DDRCTL_DFIUPDTMG1_FREQ0	0x05AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_DFIMSGTMG0_FREQ0	0x05B0	W	0x00000004	DFI MC-PHY Message Timing Register 0
DDRCTL_RFSHSET1TMG0_FREQ0	0x0600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG1_FREQ0	0x0604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ0	0x0608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ0	0x0610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1
DDRCTL_ZQSET1TMG0_FREQ0	0x0800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ0	0x0804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ0	0x0A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ0	0x0B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ0	0x0B04	W	0x050F0504	Temperature Derate Timing Register 0
DDRCTL_DERATEVAL1_FREQ0	0x0B08	W	0x00000014	Temperature Derate Timing Register 1

Name	Offset	Size	Reset Value	Description
DDRCTL_HWLPTMG0_FREQ0	0x0B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ0	0x0C00	W	0x00000000	Scheduler Control Register
DDRCTL_PERFHPR1_FREQ0	0x0C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ0	0x0C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ0	0x0C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ0	0x0D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ0	0x0D04	W	0x00000606	Rank Control Timing 0
DDRCTL_RANKTMG1_FREQ0	0x0D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ0	0x0D0C	W	0x00400010	Low Power Timing Register
DDRCTL_MSTR0	0x10000	W	0x03040000	Master Register0
DDRCTL_MSTR2	0x10008	W	0x00000000	Master Register2
DDRCTL_MSTR4	0x10010	W	0x00000000	Master Register4
DDRCTL_STAT	0x10014	W	0x00000000	Operating Mode Status Register
DDRCTL_MRCTRL0	0x10080	W	0x00000030	Mode Register Read/Write Control Register 0.
DDRCTL_MRCTRL1	0x10084	W	0x00000000	Mode Register Read/Write Control Register 1
DDRCTL_MRSTAT	0x10090	W	0x00000000	Mode Register Read/Write Status Register
DDRCTL_MRRDATA0	0x10094	W	0x00000000	Mode Register Read Data 0
DDRCTL_MRRDATA1	0x10098	W	0x00000000	Mode Register Read Data 1
DDRCTL_DERATECTL0	0x10100	W	0x00000018	Temperature Derate Control Register 0
DDRCTL_DERATECTL1	0x10104	W	0x00000000	Temperature Derate Control Register 1
DDRCTL_DERATECTL2	0x10108	W	0x00000000	Temperature Derate Control Register 2
DDRCTL_DERATECTL5	0x10114	W	0x00000001	Temperature Derate Control Register 5
DDRCTL_DERATECTL6	0x10118	W	0x00000000	Temperature Derate Control Register 6
DDRCTL_DERATESTAT0	0x1011C	W	0x00000000	Temperature Derate Status Register 0
DDRCTL_DERATEDBGCTL	0x10124	W	0x00000000	Temperature Derate Debug Contrl Register

Name	Offset	Size	Reset Value	Description
DDRCTL_DERATEDBGSTAT	0x10128	W	0x00000000	Temperature Derate Debug Status Register
DDRCTL_PWRCTL	0x10180	W	0x00000000	Low Power Control Register
DDRCTL_HWLPCTL	0x10184	W	0x00000003	Hardware Low Power Control Register
DDRCTL_CLKGATECTL	0x1018C	W	0x0000003F	clock gate control
DDRCTL_RFSHMOD0	0x10200	W	0x00000000	Refresh Mode Register 0
DDRCTL_RFSHCTL0	0x10208	W	0x00000000	Refresh Control Register 0
DDRCTL_ZQCTL0	0x10280	W	0x00000000	ZQ Control Register 0
DDRCTL_ZQCTL1	0x10284	W	0x00000000	ZQ Control Register 1
DDRCTL_ZQCTL2	0x10288	W	0x00000000	ZQ Control Register 2
DDRCTL_ZQSTAT	0x1028C	W	0x00000000	ZQ Status Register
DDRCTL_DQSOSCRUNTIME	0x10300	W	0x00400040	DQS/WCK Oscillator Runtime Register
DDRCTL_DQSOSCSTAT0	0x10304	W	0x00000000	DQS/WCK Oscillator Status Register 0
DDRCTL_DQSOSCCFG0	0x10308	W	0x00000000	DQSOSC Config Register 0
DDRCTL_SCHED0	0x10380	W	0x0001101D	Scheduler Control Register 0
DDRCTL_SCHED1	0x10384	W	0x00002000	Scheduler Control Register 1
DDRCTL_SCHED3	0x1038C	W	0x04040208	Scheduler Control Register 3
DDRCTL_SCHED4	0x10390	W	0x08400810	Scheduler Control Register 4
DDRCTL_SCHED5	0x10394	W	0x10000204	Scheduler Control Register 5.
DDRCTL_DFILPCFG0	0x10500	W	0x00100000	DFI Low Power Configuration Register 0
DDRCTL_DFIUPD0	0x10508	W	0x00008000	DFI Update Register 0
DDRCTL_DFIMISC	0x10510	W	0x00000001	DFI Miscellaneous Control Register
DDRCTL_DFISTAT	0x10514	W	0x00000000	DFI Status Register
DDRCTL_DFIPHYMSTR	0x10518	W	0x80000001	DFI PHY Master
DDRCTL_DFI0MSGCTL0	0x10520	W	0x00000000	DFI0 Message Control Register 0.
DDRCTL_DFI0MSGSTAT0	0x10524	W	0x00000000	DFI0 Message Status Register 0
DDRCTL_POISONCFG	0x10580	W	0x00110011	AXI Poison Configuration Register. Common for all AXI ports
DDRCTL_POISONSTAT	0x10584	W	0x00000000	AXI Poison Status Register
DDRCTL_ECCCFG0	0x10600	W	0x013F7F40	ECC Configuration Register 0
DDRCTL_ECCCFG1	0x10604	W	0x000003B0	ECC Configuration Register 1
DDRCTL_ECCSTAT	0x10608	W	0x00000000	SECDED ECC Status Register
DDRCTL_ECCCTL	0x1060C	W	0x00000700	ECC Clear Register
DDRCTL_ECCERRCNT	0x10610	W	0x00000000	ECC Error Counter Register
DDRCTL_ECCCADDR0	0x10614	W	0x00000000	ECC Corrected Error Address Register 0
DDRCTL_ECCCADDR1	0x10618	W	0x00000000	ECC Corrected Error Address Register 1

Name	Offset	Size	Reset Value	Description
DDRCTL_ECCCSYN0	0x1061C	W	0x00000000	ECC Corrected Syndrome Register 0
DDRCTL_ECCCSYN1	0x10620	W	0x00000000	ECC Corrected Syndrome Register 1
DDRCTL_ECCCSYN2	0x10624	W	0x00000000	ECC Corrected Syndrome Register 2
DDRCTL_ECCBITMASK0	0x10628	W	0x00000000	ECC Corrected Data Bit Mask Register 0
DDRCTL_ECCBITMASK1	0x1062C	W	0x00000000	ECC Corrected Data Bit Mask Register 1
DDRCTL_ECCBITMASK2	0x10630	W	0x00000000	ECC Corrected Data Bit Mask Register 2
DDRCTL_ECCUADDR0	0x10634	W	0x00000000	ECC Uncorrected Error Address Register 0
DDRCTL_ECCUADDR1	0x10638	W	0x00000000	ECC Uncorrected Error Address Register 1
DDRCTL_ECCUSYN0	0x1063C	W	0x00000000	ECC Uncorrected Syndrome Register 0
DDRCTL_ECCUSYN1	0x10640	W	0x00000000	ECC Uncorrected Syndrome Register 1
DDRCTL_ECCUSYN2	0x10644	W	0x00000000	ECC Uncorrected Syndrome Register 2
DDRCTL_ECCPOISONADDR0	0x10648	W	0x00000000	ECC Data Poisoning Address Register 0.
DDRCTL_ECCPOISONADDR1	0x1064C	W	0x00000000	ECC Data Poisoning Address Register 1.
DDRCTL_ECCAPSTAT	0x10664	W	0x00000000	Address protection within ECC Status Register
DDRCTL_LNKECCCTL0	0x10980	W	0x00000000	Link-ECC Control Register 0
DDRCTL_LNKECCCTL1	0x10984	W	0x00000000	Link-ECC Control Register 1
DDRCTL_LNKECCPOISONCTL0	0x10988	W	0x00000000	Link-ECC Poison Control Register 0
DDRCTL_LNKECCPOISONSTAT	0x1098C	W	0x00000000	Link-ECC Poison Status Register
DDRCTL_LNKECCINDEX	0x10990	W	0x00000000	Link-ECC Index Register
DDRCTL_LNKECCERRCNT0	0x10994	W	0x00000000	Link-ECC Error Status Register 0
DDRCTL_LNKECCERRSTAT	0x10998	W	0x00000000	Link-ECC Error Status Register 1
DDRCTL_OPCTRL0	0x10B80	W	0x00000000	Operation Control Register 0
DDRCTL_OPCTRL1	0x10B84	W	0x00000000	Operation Control Register 1
DDRCTL_OPCTRLCAM	0x10B88	W	0x00000000	CAM Operation Control Register

Name	Offset	Size	Reset Value	Description
DDRCTL_OPCTRLCMD	0x10B8C	W	0x00000000	Command Operation Control Register
DDRCTL_OPCTRLSTAT	0x10B90	W	0x00000000	Status Operation Control Register
DDRCTL_OPCTRLCAM1	0x10B94	W	0x00000000	CAM Operation Control Register 1
DDRCTL_OPREFCTRL0	0x10B98	W	0x00000000	Refresh Operation Control Register 0
DDRCTL_OPREFSTAT0	0x10BA0	W	0x00000000	Refresh Operation Status Register 0
DDRCTL_SWCTL	0x10C80	W	0x00000001	Software Register Programming Control Enable
DDRCTL_SWSTAT	0x10C84	W	0x00000001	Software Register Programming Control Status
DDRCTL_RANKCTL	0x10C90	W	0x0000000F	Rank Control Register
DDRCTL_DBICTL	0x10C94	W	0x00000001	DM/DBI Control Register
DDRCTL_ODTMAP	0x10C9C	W	0x00002211	ODT/Rank Map Register
DDRCTL_DATACTL0	0x10CA0	W	0x00000000	Data Control register 0
DDRCTL_SWCTLSTATIC	0x10CA4	W	0x00000000	Static Registers Write Enable
DDRCTL_INITTMG0	0x10D00	W	0x0002004E	SDRAM Initialization Timing Register 0
DDRCTL_INITTMG1	0x10D04	W	0x00000000	SDRAM Initialization Timing Register 1
DDRCTL_DDRCTL_VER_NUMBER	0x10FF8	W	0x3130312A	DDRCTL Version Number Register
DDRCTL_DDRCTL_VER_TYPE	0x10FFC	W	0x6C633031	DDRCTL Version Type Register
DDRCTL_PCCFG	0x20000	W	0x00000000	Port Common Configuration Register.
DDRCTL_PCFGR	0x20004	W	0x0000501F	Configuration Read Register
DDRCTL_PCFGW	0x20008	W	0x0000501F	Configuration Write Register
DDRCTL_PCTRL	0x20090	W	0x00000000	Port Control Register
DDRCTL_PCFGQOS0	0x20094	W	0x00000000	Port n Read QoS Configuration Register 0
DDRCTL_PCFGQOS1	0x20098	W	0x00000000	Port n Read QoS Configuration Register 1
DDRCTL_PCFGWQOS0	0x2009C	W	0x00000E00	Port n Write QoS Configuration Register 0
DDRCTL_PCFGWQOS1	0x200A0	W	0x00000000	Port n Write QoS Configuration Register 1
DDRCTL_SBRCTL	0x200E0	W	0x1000FF10	Scrubber Control Register
DDRCTL_SBRSTAT	0x200E4	W	0x00000000	Scrubber Status Register
DDRCTL_SBRWDATA0	0x200E8	W	0x00000000	Scrubber Write Data Pattern0
DDRCTL_SBRSTART0	0x200F0	W	0x00000000	Scrubber Start Address Mask Register 0

Name	Offset	Size	Reset Value	Description
DDRCTL_SBRSTART1	0x200F4	W	0x00000000	Scrubber Start Address Mask Register 1
DDRCTL_SBRRANGE0	0x200F8	W	0x00000000	Scrubber Address Range Mask Register 0
DDRCTL_SBRRANGE1	0x200FC	W	0x00000000	Scrubber Address Range Mask Register 1
DDRCTL_PSTAT	0x20114	W	0x00000000	Port Status Register
DDRCTL_ADDRMAP1	0x30004	W	0x00000000	Address Map Register 1
DDRCTL_ADDRMAP3	0x3000C	W	0x00000000	Address Map Register 3
DDRCTL_ADDRMAP4	0x30010	W	0x00000000	Address Map Register 4
DDRCTL_ADDRMAP5	0x30014	W	0x00000000	Address Map Register 5
DDRCTL_ADDRMAP6	0x30018	W	0x00000000	Address Map Register 6
DDRCTL_ADDRMAP7	0x3001C	W	0x00000000	Address Map Register 7
DDRCTL_ADDRMAP8	0x30020	W	0x00000000	Address Map Register 8
DDRCTL_ADDRMAP9	0x30024	W	0x00000000	Address Map Register 9
DDRCTL_ADDRMAP10	0x30028	W	0x00000000	Address Map Register 10
DDRCTL_ADDRMAP11	0x3002C	W	0x00000000	Address Map Register 11
DDRCTL_ADDRMAP12	0x30030	W	0x00000000	Address Map Register 12
DDRCTL_DRAMSET1TMG0_FREQ1	0x100000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ1	0x100004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ1	0x100008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ1	0x10000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ1	0x100010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ1	0x100014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG6_FREQ1	0x100018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ1	0x10001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ1	0x100020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ1	0x100024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG12_FREQ1	0x100030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ1	0x100034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1

Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG14_FREQ1	0x100038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ1	0x10005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG24_FREQ1	0x100060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ1	0x100064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ1	0x100078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1
DDRCTL_INITMR0_FREQ1	0x100500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ1	0x100504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ1	0x100508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ1	0x10050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ1	0x100580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ1	0x100584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ1	0x100588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ1	0x100590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ1	0x100594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFIUPDTMG1_FREQ1	0x1005AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_RFSHSET1TMG0_FREQ1	0x100600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG1_FREQ1	0x100604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ1	0x100608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ1	0x100610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1
DDRCTL_ZQSET1TMG0_FREQ1	0x100800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ1	0x100804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ1	0x100A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ1	0x100B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ1	0x100B04	W	0x050F0504	Temperature Derate Timing Register 0

Name	Offset	Size	Reset Value	Description
DDRCTL_DERATEVAL1_FREQ1	0x100B08	W	0x00000014	Temperature Derate Timing Register 1
DDRCTL_HWLPTMG0_FREQ1	0x100B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ1	0x100C00	W	0x00000000	Scheduler Control Register
DDRCTL_PERFHPR1_FREQ1	0x100C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ1	0x100C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ1	0x100C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ1	0x100D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ1	0x100D04	W	0x00000606	Rank Control Timing 0
DDRCTL_RANKTMG1_FREQ1	0x100D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ1	0x100D0C	W	0x00400010	Low Power Timing Register
DDRCTL_DRAMSET1TMG0_FREQ2	0x200000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ2	0x200004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ2	0x200008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ2	0x20000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ2	0x200010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ2	0x200014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG6_FREQ2	0x200018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ2	0x20001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ2	0x200020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ2	0x200024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG12_FREQ2	0x200030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ2	0x200034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1

Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG14_FREQ2	0x200038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ2	0x20005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG24_FREQ2	0x200060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ2	0x200064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ2	0x200078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1
DDRCTL_INITMR0_FREQ2	0x200500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ2	0x200504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ2	0x200508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ2	0x20050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ2	0x200580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ2	0x200584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ2	0x200588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ2	0x200590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ2	0x200594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFIUPDTMG1_FREQ2	0x2005AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_RFSHSET1TMG0_FREQ2	0x200600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG1_FREQ2	0x200604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ2	0x200608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ2	0x200610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1
DDRCTL_ZQSET1TMG0_FREQ2	0x200800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ2	0x200804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ2	0x200A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ2	0x200B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ2	0x200B04	W	0x050F0504	Temperature Derate Timing Register 0

Name	Offset	Size	Reset Value	Description
DDRCTL_DERATEVAL1_FREQ2	0x200B08	W	0x00000014	Temperature Derate Timing Register 1
DDRCTL_HWLPTMG0_FREQ2	0x200B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ2	0x200C00	W	0x00000000	Scheduler Control Register
DDRCTL_PERFHPR1_FREQ2	0x200C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ2	0x200C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ2	0x200C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ2	0x200D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ2	0x200D04	W	0x00000606	Rank Control Timing 0
DDRCTL_RANKTMG1_FREQ2	0x200D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ2	0x200D0C	W	0x00400010	Low Power Timing Register
DDRCTL_DRAMSET1TMG0_FREQ3	0x300000	W	0x0F101B0F	SDRAM Timing Register 0 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG1_FREQ3	0x300004	W	0x00080414	SDRAM Timing Register 1 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG2_FREQ3	0x300008	W	0x0305060D	SDRAM Timing Register 2 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG3_FREQ3	0x30000C	W	0x00040404	SDRAM Timing Register 3 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG4_FREQ3	0x300010	W	0x05040405	SDRAM Timing Register 4 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG5_FREQ3	0x300014	W	0x05050403	SDRAM Timing Register 5 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG6_FREQ3	0x300018	W	0x00000005	SDRAM Timing Register 6 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG7_FREQ3	0x30001C	W	0x00000000	SDRAM Timing Register 7 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG8_FREQ3	0x300020	W	0x00004405	SDRAM Timing Register 8 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG9_FREQ3	0x300024	W	0x0004040D	SDRAM Timing Register 9 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG12_FREQ3	0x300030	W	0x00020000	SDRAM Timing Register 12 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG13_FREQ3	0x300034	W	0x1C200004	SDRAM Timing Register 13 belonging to Timing Set 1

Name	Offset	Size	Reset Value	Description
DDRCTL_DRAMSET1TMG14_FREQ3	0x300038	W	0x000800A0	SDRAM Timing Register 14 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG23_FREQ3	0x30005C	W	0x00000000	SDRAM Timing Register 23 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG24_FREQ3	0x300060	W	0x000F0F0F	SDRAM Timing Register 24 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG25_FREQ3	0x300064	W	0x00000000	SDRAM Timing Register 25 belonging to Timing Set 1
DDRCTL_DRAMSET1TMG30_FREQ3	0x300078	W	0x00000000	SDRAM Timing Register 30 belonging to Timing Set 1
DDRCTL_INITMR0_FREQ3	0x300500	W	0x00000510	SDRAM Initialization MR Setting Register 0
DDRCTL_INITMR1_FREQ3	0x300504	W	0x00000000	SDRAM Initialization MR Setting Register 1
DDRCTL_INITMR2_FREQ3	0x300508	W	0x00000000	SDRAM Initialization MR Setting Register 2
DDRCTL_INITMR3_FREQ3	0x30050C	W	0x00000000	SDRAM Initialization MR Setting Register 3
DDRCTL_DFITMG0_FREQ3	0x300580	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1_FREQ3	0x300584	W	0x00000404	DFI Timing Register 1
DDRCTL_DFITMG2_FREQ3	0x300588	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG4_FREQ3	0x300590	W	0x00000000	DFI Timing Register 4
DDRCTL_DFITMG5_FREQ3	0x300594	W	0x00000000	DFI Timing Register 5
DDRCTL_DFIUPDTMG1_FREQ3	0x3005AC	W	0x00010001	DFI Update Timing Register 1
DDRCTL_RFSHSET1TMG0_FREQ3	0x300600	W	0x02100062	Refresh Timing Register 0 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG1_FREQ3	0x300604	W	0x0000008C	Refresh Timing Register 1 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG2_FREQ3	0x300608	W	0x8C8C0000	Refresh Timing Register 2 belonging to Timing Set 1
DDRCTL_RFSHSET1TMG4_FREQ3	0x300610	W	0x00000000	Refresh Timing Register 4 belonging to Timing Set 1
DDRCTL_ZQSET1TMG0_FREQ3	0x300800	W	0x00400200	ZQ Timing Register 0 belonging to DRAM ZQ timing set 1
DDRCTL_ZQSET1TMG1_FREQ3	0x300804	W	0x02000100	ZQ Timing Register 1 belonging to DRAM ZQ timing set 1
DDRCTL_DQSOSCCTL0_FREQ3	0x300A80	W	0x00000070	DQS/WCK Oscillator Control Register 0
DDRCTL_DERATEINT_FREQ3	0x300B00	W	0x00800000	Temperature Derate Interval Register
DDRCTL_DERATEVAL0_FREQ3	0x300B04	W	0x050F0504	Temperature Derate Timing Register 0

Name	Offset	Size	Reset Value	Description
DDRCTL_DERATEVAL1_FREQ3	0x300B08	W	0x00000014	Temperature Derate Timing Register 1
DDRCTL_HWLPTMG0_FREQ3	0x300B80	W	0x00000000	Hardware Low Power Control Register
DDRCTL_SCHEDTMG0_FREQ3	0x300C00	W	0x00000000	Scheduler Control Register
DDRCTL_PERFHPR1_FREQ3	0x300C80	W	0x0F000001	High Priority Read CAM Register 1
DDRCTL_PERFLPR1_FREQ3	0x300C84	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1_FREQ3	0x300C88	W	0x0F00007F	Write CAM Register 1
DDRCTL_TMGCFG_FREQ3	0x300D00	W	0x00000000	Timing Configuration Register
DDRCTL_RANKTMG0_FREQ3	0x300D04	W	0x00000606	Rank Control Timing 0
DDRCTL_RANKTMG1_FREQ3	0x300D08	W	0x00000F0F	Rank Timing Register 1
DDRCTL_PWRTMG_FREQ3	0x300D0C	W	0x00400010	Low Power Timing Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2 Detail Register Description For DDRCTL

DDRCTL_DRAMSET1TMG0_FREQ0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. For DDR5, add one extra cycle when CRCPARCTL1.wr_crc_enable = 1. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset: 0x10 Volatile: true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset: 0x1b Volatile: true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset: 0xf Volatile: true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved Field:Yes
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. DDR4 (C/A parity not enabled): tXP DDR4 (C/A parity enabled): (tXP+PL) DDR5: tXP DDR5 RDIMM: max (tXP, tRPDX) LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. DDR4: Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). DDR5: tRTP LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved Field:Yes
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. In addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x06	rd2wr DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL DDR5: CL - CWL + BL/2 + 2 - (Read DQS offset) + (RD_POSTAMBLE-0.5) + WR_PREAMBLE LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR4, if derating is enabled (DERATECTL0.derate_enable=1), derated tDQSCKmax must be used. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0d	wr2rd DDR4: CWL + PL + BL/2 + tWTR_L DDR5: CWL + BL/2 + tWTR_L LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) In DDR4, minimum time from write command to read command for same bank group. In others, minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ0

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command DDR4: Set this to the larger of tMOD + AL and tMRD. If C/A parity is enabled, tMOD_PAR(tMOD+PL) + AL and tMRD_PAR(tMOD+PL) and used instead. If CAL mode is enabled, tCAL must be added to the above. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using LRDIMM, the minimum value of this register is tMRD_L2. DDR5: Set this to the larger of tMRR, tMRW, tMRWPD, tMRD and tMPC_DELAY. LPDDR4:Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5:Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Note: For DDR5, it is recommended to set this value as multiple of MEMC_FREQ_RATIO to improve the performance. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. DDR4: tCCD_L LPDDR4: tCCD LPDDR5: BL/n Don't Care for DDR5 (see DRAMSET1TMG26.t_ccd_r/t_ccd_w in DDR5). Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_rrd For DDR4/DDR5/LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". DDR4/5: tRRD_L LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ0

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH DDR4: tCKSRX DDR5: tCKSRX Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

Bit	Attr	Reset Value	Description
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK DDR4: tCKSRE (+ PL(parity latency)(*)) DDR5: tCKLCS (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: max(tCKE, tSR) LPDDR5: tSR DDR4: tCKESR (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD DDR4: tPD (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG6_FREQ0

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ0
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ0
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x44 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG9_FREQ0
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved1 Reserved Field:Yes
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting DDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting DDR4/DDR5/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support DDR SDRAM memories or LPDDR5 SDRAM memories. DDR4/DDR5 designs: CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Where: CWL = CAS write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. WTR_S must be increased by one if DDR4 2tCK write preamble is used. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: max(tESCKE, tCMDCKE) LPDDR5: max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_DRAMSET1TMG13_FREQ0
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x1c Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved1 Reserved Field:Yes
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x20 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes
3:0	RW	0x4	t_ppd LPDDR4/5 and DDR5: tPPD: This is the minimum time from precharge to precharge command. Note: This register is not applicable for DDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ0
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset:0xa0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ0

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ0

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 00: 4 Banks/ 4 Bank groups 01: 8 Banks (Reserved) 10: 16 Banks 11: Reserved Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ0

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved Field:Yes
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 DDR4: WL + BL/2 + WR Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP DDR4: RTP Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ0

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ0

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR4: Value loaded into MR0 register. DDR5: Don't care LPDDR4: Value to write to MR1 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

Bit	Attr	Reset Value	Description
15:0	RW	0x0510	emr DDR4: Value to write to MR1 register Set bit 7 to 0. DDR5: Don't care LPDDR4 - Value to write to MR2 register Value After Reset:0x510 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ0
Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR4: Value to write to MR2 register DDR5: Don't care LPDDR4: Value to write to MR3 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR4: Value to write to MR3 register DDR5: Don't care LPDDR4: Value to write to MR13 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ0
Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4: Value to be loaded into SDRAM MR4 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4: Value to be loaded into SDRAM MR5 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ0
Address: Operational Base + offset (0x050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 DDR4 Value to be loaded into SDRAM MR6 registers. DDR5: Don't care LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ0

Address: Operational Base + offset (0x0580)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Volatile:true Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG1_FREQ0

Address: Operational Base + offset (0x0584)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When TMGCFG.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When TMGCFG.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ0

Address: Operational Base + offset (0x0588)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved2 Reserved Field:Yes
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on th DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ0
Address: Operational Base + offset (0x0590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ0
Address: Operational Base + offset (0x0594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFILPTMG0_FREQ0

Address: Operational Base + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20:16	RW	0x00	dfi_lp_wakeup_dsm Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Deep Sleep Mode is entered. Determines the DFI's tlp_wakeup time: 0x00 - 1 cycle 0x01 - 2 cycles 0x02 - 4 cycles 0x03 - 8 cycles 0x04 - 16 cycles 0x05 - 32 cycles 0x06 - 64 cycles 0x07 - 128 cycles 0x08 - 256 cycles 0x09 - 512 cycles 0x0A - 1024 cycles 0x0B - 2048 cycles 0x0C - 4096 cycles 0x0D - 8192 cycles 0x0E - 16384 cycles 0x0F - 32768 cycles 0x10 - 65536 cycles 0x11 - 131072 cycles 0x12 - 262144 cycles 0x13 - Unlimited This is only present for designs supporting LPDDR5 devices. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x00	dfi_lp_wakeup_sr Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Self Refresh mode is entered. Determines the DFI's tlp_wakeup time: 0x00 - 1 cycle 0x01 - 2 cycles 0x02 - 4 cycles 0x03 - 8 cycles 0x04 - 16 cycles 0x05 - 32 cycles 0x06 - 64 cycles 0x07 - 128 cycles 0x08 - 256 cycles 0x09 - 512 cycles 0x0A - 1024 cycles 0x0B - 2048 cycles 0x0C - 4096 cycles 0x0D - 8192 cycles 0x0E - 16384 cycles 0x0F - 32768 cycles 0x10 - 65536 cycles 0x11 - 131072 cycles 0x12 - 262144 cycles 0x13 - Unlimited Note: This field can only be set to 0x01~0x0F for DDR5 SDRAM. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x00	dfi_lp_wakeup_pd Indicates the value in DFI clock cycles to drive on dfi_lp_ctrl_wakeup and dfi_lp_data_wakeup signals when Power Down mode is entered. Determines the DFI's tlp_wakeup time: 0x00 - 1 cycle 0x01 - 2 cycles 0x02 - 4 cycles 0x03 - 8 cycles 0x04 - 16 cycles 0x05 - 32 cycles 0x06 - 64 cycles 0x07 - 128 cycles 0x08 - 256 cycles 0x09 - 512 cycles 0x0A - 1024 cycles 0x0B - 2048 cycles 0x0C - 4096 cycles 0x0D - 8192 cycles 0x0E - 16384 cycles 0x0F - 32768 cycles 0x10 - 65536 cycles 0x11 - 131072 cycles 0x12 - 262144 cycles 0x13 - Unlimited Note: This field can only be set to 0x01~0x0F for DDR5 SDRAM. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_DFILPTMG1_FREQ0

Address: Operational Base + offset (0x05A4)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12:8	RW	0x07	dfi_tlp_resp Setting in DFI clock cycles for DFI's tlp_resp time. Same value is used for both Power Down, Self Refresh, Deep Sleep Mode and Maximum Power Saving modes. Refer to PHY databook for recommended values Unit: DFI clock cycles. Value After Reset:0x7 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x00	dfi_lp_wakeup_data Indicates the value in DFI clock cycles to drive on dfi_lp_data_wakeup signal when data bus is idle. Determines the DFI's tlp_wakeup time: 0x00 - 1 cycle 0x01 - 2 cycles 0x02 - 4 cycles 0x03 - 8 cycles 0x04 - 16 cycles 0x05 - 32 cycles 0x06 - 64 cycles 0x07 - 128 cycles 0x08 - 256 cycles 0x09 - 512 cycles 0x0A - 1024 cycles 0x0B - 2048 cycles 0x0C - 4096 cycles 0x0D - 8192 cycles 0x0E - 16384 cycles 0x0F - 32768 cycles 0x10 - 65536 cycles 0x11 - 131072 cycles 0x12 - 262144 cycles 0x13 - Unlimited Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_DFIUPDTMG0_FREQ0
Address: Operational Base + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	dfi_t_ctrlup_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Lowest value to assign to this variable is 0x40. Unit: DFI clock cycles. Value After Reset:0x40 Programming Mode:Static
15:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x003	dfi_t_ctrlup_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The DDRCTL expects the PHY to respond within this time. If the PHY does not respond, the DDRCTL will de-assert dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x1. Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Static

DDRCTL_DFIUPDTMG1_FREQ0
Address: Operational Base + offset (0x05AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static
15:8	RW	0x00	Reserved0 Reserved Field:Yes
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static

DDRCTL_DFIMSGTMG0_FREQ0

Address: Operational Base + offset (0x05B0)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7:0	RW	0x04	dfi_t_ctrlmsg_resp This is the maximum amount in DFI clock cycles between the assertion of the dfi{0/1}_ctrlmsg_req signal to the assertion of the dfi{0/1}_ctrlmsg_ack signal. If the PHY does not acknowledge the request within dfi_t_ctrlmsg_resp cycles, the PHY must not acknowledge the request at all. In this case, the controller should de-assert the corresponding dfi{0/1}_ctrlmsg_req signal. The timing values might vary based on the frequency ratio and user must reprogram if there is any change in the frequency ratio. Refer to PHY databook for recommended values Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Static

DDRCTL_RFSHSET1TMG0_FREQ0

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used, 1 - x1 register values are used. This applies only when per-bank refresh is enabled (RFSHMOD0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved2 Reserved Field:Yes
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32 * 32 if RFSHSET1TMG0.t_refi_x1_sel = 0. If RFSHSET1TMG0.t_refi_x1_sel = 1, internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related
23:22	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this RFSHSET1TMG0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) or DDR5 same-bank refresh (REFsb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. For non-DDR5, this should be programmed to tREFI based value in controller's current refresh mode. For DDR5, this should be always programmed to tREFI1 based value even in FGR mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR4, 3.9us for DDR5. See JEDEC specification for LPDDR4). set this register to RoundDown(tREFI/tCK) if RFSHSET1TMG0.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: if using all-bank refreshes (RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations if using per-bank refreshes (RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations For DDR controller, tREFI value is different depending on FGR mode. In DDR4 mode, if using FGR 1x mode (RFSHMOD1.fgr_mode = 000), use tREFI1 in the above calculations In DDR4 mode, if using FGR 2x mode (RFSHMOD1.fgr_mode = 001), use tREFI2 in the above calculations In DDR4 mode, if using FGR 4x mode (RFSHMOD1.fgr_mode = 010), use tREFI4 in the above calculations In DDR5 mode, always use tREFI1 in the above calculations Note that: RFSHSET1TMG0.t_refi_x1_x32 must be greater than 0x1. if RFSHSET1TMG0.t_refi_x1_sel == 1, RFSHSET1TMG0.t_refi_x1_x32 must be greater than RFSHSET1TMG1.t_rfc_min if RFSHSET1TMG0.t_refi_x1_sel == 0, RFSHSET1TMG0.t_refi_x1_x32 * 32 must be greater than RFSHSET1TMG1.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0xFFE. In DDR4 Fixed 2x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x7FF. In DDR4 Fixed 4x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x3FF. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ0

Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller: if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4/DDR5 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user must program the appropriate value from the spec based on the 'fgr_mode' and the device density that is used. Unit: DRAM clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ0
Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (RFSHMOD0.per_bank_refresh == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_RFSHSET1TMG4_FREQ0
Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ0
Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	t_zq_short_nop tZQCS for DD4, tZQLAT for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x40 Programming Mode:Static
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:0	RW	0x0200	t_zq_long_nop tZQoper for DDR4, tZQCAL for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset:0x200 Programming Mode:Static

DDRCTL_ZQSET1TMG1_FREQ0
Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x20 Programming Mode:Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR4/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x100 Programming Mode:Static

DDRCTL_DQSOSCCTL0_FREQ0
Address: Operational Base + offset (0x0A80)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved2 Reserved Field:Yes
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset:0x7 Programming Mode:Dynamic
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval.The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1: x2K DFI clock cycles 0: x32K DFI clock cycles Value After Reset:0x0 Programming Mode:Dynamic
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1: Enable DQS Oscillator 0: Disable DQS Oscillator Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATEINT_FREQ0
Address: Operational Base + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset:0x800000 Volatile:true Programming Mode:Static

DDRCTL_DERATEVAL0_FREQ0

Address: Operational Base + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ0
Address: Operational Base + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ0
Address: Operational Base + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Volatile:true Programming Mode:Static
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_SCHEDTMG0_FREQ0
Address: Operational Base + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static
7:0	RW	0x00	pageclose_timer This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_PERFHPR1_FREQ0

Address: Operational Base + offset (0x0C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ0

Address: Operational Base + offset (0x0C84)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFWR1_FREQ0

Address: Operational Base + offset (0x0C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ0
Address: Operational Base + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved1 Reserved Field:Yes
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset:0x0 Programming Mode:Dynamic
7:1	RW	0x00	Reserved0 Reserved Field:Yes
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For DDR4/DDR5/LPDDR4: 0: 1:2 Mode 1: 1:4 Mode For LPDDR5: 0: 1:1:2 Mode 1: 1:1:4 Mode Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ0
Address: Operational Base + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. If write preamble is set to 2tCK(DDR4 only), must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

Bit	Attr	Reset Value	Description
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TRDRD timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ0
Address: Operational Base + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ0

Address: Operational Base + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x40 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:7	RW	0x000	Reserved0 Reserved Field:Yes
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_MSTR0

Address: Operational Base + offset (0x10000)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved5 Reserved Field:Yes

Bit	Attr	Reset Value	Description
25:24	RW	0x3	active_ranks Only present for multi-rank configurations. Each bit represents one rank. For two-rank configurations, only bits[25:24] are present. 1 - populated 0 - unpopulated LSB is the lowest rank number. For 2 ranks following combinations are legal: 01 - One rank 11 - Two ranks Others - Reserved. For 4 ranks following combinations are legal: 0001 - One rank 0011 - Two ranks 0101 - Two ranks are populated in Rank0 and Rank2 (DDR5 Only). 1111 - Four ranks Note: the four rank populated config 4'b0101 can only be supported with heterogenous rank support enable. Value After Reset:0x3 Programming Mode:Static
23:21	RW	0x0	Reserved4 Reserved Field:Yes
20:16	RW	0x04	burst_rdwr SDRAM burst length used: 00100 - Burst length of 8 01000 - Burst length of 16 All other values are reserved. This controls the burst size used to access the SDRAM. This must match the burst length mode register setting in the SDRAM. For DDR4, this must be set to 0x00100 (BL8). For LPDDR4/LPDDR5/DDR5, this must be set to 0x01000 (BL16). Value After Reset:0x4 Programming Mode:Static
15:14	RW	0x0	Reserved3 Reserved Field:Yes
13:12	RW	0x0	data_bus_width Selects proportion of DQ bus width that is used by the SDRAM 00 - Full DQ bus width to SDRAM 01 - Half DQ bus width to SDRAM 10 - Quarter DQ bus width to SDRAM 11 - Reserved. Note that half bus width mode is only supported when the SDRAM bus width is a multiple of 16, and quarter bus width mode is only supported when the SDRAM bus width is a multiple of 32 and the configuration parameter MEMC_QBUS_SUPPORT is set. Bus width refers to DQ bus width (excluding any ECC width). Value After Reset:0x0 Programming Mode:Static
11:4	RW	0x00	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
3	RW	0x0	lpddr5 Select LPDDR5 SDRAM 1 - LPDDR5 SDRAM device in use. 0 - non-LPDDR5 device in use Present only in designs configured to support LPDDR5 SDRAM memories. Value After Reset:0x0 Programming Mode:Static
2	RW	0x0	Reserved1 Reserved Field:Yes
1	RW	0x0	lpddr4 Select LPDDR4 SDRAM 1 - LPDDR4 SDRAM device in use. 0 - non-LPDDR4 device in use Present only in designs configured to support LPDDR4 SDRAM memories. Value After Reset:0x0 Programming Mode:Static
0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_MSTR2

Address: Operational Base + offset (0x10008)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1:0	RW	0x0	target_frequency This field specifies the target frequency. 0 - Frequency 0/Normal 1 - Frequency 1/FREQ1 2 - Frequency 2/FREQ2 3 - Frequency 3/FREQ3 All other values are reserved. Note: If the target frequency can be changed through Hardware Low Power Interface only, this field is not needed. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_MSTR4

Address: Operational Base + offset (0x10010)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	wck_on WCK always ON mode 0: WCK Always On mode disabled 1: WCK Always On mode enabled In case of multi-rank system, the controller issues CAS-WS_FS to all ranks to sets DRAM in sync state simultaneously. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_STAT

Address: Operational Base + offset (0x10014)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved3 Reserved Field:Yes
16	RO	0x0	selfref_cam_not_empty Self refresh with CAMs not empty. Set to 1 when Self Refresh is entered but CAMs are not drained. Cleared after exiting Self Refresh. Value After Reset:0x0 Programming Mode:Static
15	RW	0x0	Reserved2 Reserved Field:Yes
14:12	RO	0x0	selfref_state Self refresh state. This indicates self refresh or self refresh power down state or Deep Sleep Mode (LPDDR5 only). This register is used for frequency change and MRR/MRW access during self refresh. 000 - SDRAM is not in Self Refresh. 001 - Self refresh 1 010 - Self refresh power down 011 - Self refresh 2 100 - Deep Sleep Mode (LPDDR5 only) Value After Reset:0x0 Programming Mode:Static
11:6	RW	0x00	Reserved1 Reserved Field:Yes
5:4	RO	0x0	selfref_type Flags if Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5) is entered and if it was under Automatic Self Refresh control only or not. 00 - SDRAM is not in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5). If CA parity retry is enabled by RETRYCTL0.capar_retry_enable, this also indicates SRE command is still in parity error window or retry is in-progress. 11 - SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was caused by Automatic Self Refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 10 - SDRAM is in Self Refresh (except LPDDR4/5) or SR-Powerdown (LPDDR4/5), which was not caused solely under Automatic Self Refresh control. It could have been caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. 01 - SDRAM is in Self Refresh, which was caused by PHY Master Request. For LPDDR54 and DDR4, only bit[5:4] are used. For DDR5, self-refresh per rank control is supported. bit[5:4] - rank 0 selfref_type bit[7:6] - rank 1 selfref_type bit[9:8] - rank 2 selfref_type bit[11:10] - rank 3 selfref_type Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
2:0	RO	0x0	operating_mode Operating mode. DDR4/DDR5 designs: 000 - Init 001 - Normal 010 - Power-down (For DDR4, this means all ranks are in power-down state. For DDR5, this means at least one rank is in power-down state, check powerdown_state for details) 011 - Self refresh (For DDR4/DDR5, this means all ranks are in self refresh state, check selfref_type for details) 1XX - Maximum Power Saving Mode (For DDR4 only) LPDDR4/LPDDR5designs: 000 - Init 001 - Normal 010 - Power-down 011 - Self refresh / Self refresh power-down Value After Reset:0x0 Programming Mode:Static

DDRCTL_MRCTRL0

Address: Operational Base + offset (0x10080)

Bit	Attr	Reset Value	Description
31	RW	0x0	mr_wr Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the DDRCTL automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down or MPSM operating modes. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
30:25	RW	0x00	Reserved3 Reserved Field:Yes
24	RW	0x0	mrr_done_clr If this bit is set, mrr_done will be cleared by the controller. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
23:16	RW	0x00	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
15:12	RW	0x0	mr_addr Address of the mode register that is to be written to. 0000 - MR0 0001 - MR1 0010 - MR2 0011 - MR3 0100 - MR4 0101 - MR5 0110 - MR6 0111 - MR7 This signal is also used for writing to control words of the register chip on RDIMMs/LRDIMMs. In that case, it corresponds to the bank address bits sent to the RDIMM/LRDIMM. In case of DDR4, the bit[3:2] corresponds to the bank group bits. Therefore, the bit[3] as well as the bit[2:0] must be set to an appropriate value which is considered both the Address Mirroring of UDIMMs/RDIMMs/LRDIMMs and the Output Inversion of RDIMMs/LRDIMMs. Don't Care for LPDDR4/5 (see MRCTRL1.mr_data for mode register addressing in LPDDR4/5). Don't Care for DDR5 (see CMDCTL.cmd_ctrl for MRW/MRR access in DDR5). Value After Reset:0x0 Programming Mode:Dynamic
11:6	RW	0x00	Reserved1 Reserved Field:Yes
5:4	RW	0x3	mr_rank Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits must be set to 1. However, for multi-rank UDIMMs/RDIMMs/LRDIMMs which implement address mirroring, it may be necessary to access ranks individually. Examples (assume DDRCTL is configured for 4 ranks): 0x1 - select rank 0 only 0x2 - select rank 1 only 0x5 - select ranks 0 and 2 0xA - select ranks 1 and 3 0xF - select ranks 0, 1, 2 and 3 Don't Care for DDR5. Value After Reset:0x3 Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
3	RW	0x0	sw_init_int Indicates whether Software intervention is allowed via MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For DDR4, this bit can be used to initialize the DDR4 RCD (MR7) before automatic SDRAM initialization. For LPDDR4/5, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. In LPDDR4 dual channel mode, note that this must be programmed to both channels beforehand. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine will not re-start. 0 - Software intervention is not allowed 1 - Software intervention is allowed Don't Care for DDR5. Value After Reset:0x0 Programming Mode:Dynamic
2:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	mr_type Indicates whether the mode register operation is read or write. 0 - Write 1 - Read Only used for LPDDR4/LPDDR5/DDR4. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MRCTRL1
Address: Operational Base + offset (0x10084)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved Field:Yes
17:0	RW	0x00000	mr_data Mode register write data for DDR4 mode. For LPDDR4/5, MRCTRL1[15:0] are interpreted as [15:8] MR Address [7:0] MR data for writes, don't care for read This is 18-bit wide in configurations with DDR4 support and 16-bits for the LPDDR5/4 controller. Don't Care for DDR5 (see CMDCTL.cmd_ctrl for MRW access in DDR5). Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MRSTAT
Address: Operational Base + offset (0x10090)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
16	RO	0x0	mr_done This signal goes high when the controller received MRR data which is triggered by MRCTRL0.mr_wr. This signal is cleared by mrr_done_clr Value After Reset:0x0 Programming Mode:Dynamic
15:1	RW	0x0000	Reserved0 Reserved Field:Yes
0	RO	0x0	mr_wr_busy The SoC core may initiate a MR write operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the MRW/MRR request. It goes low when the MRW/MRR command is issued to the SDRAM. It is recommended not to perform MRW/MRR commands when 'MRSTAT.mr_wr_busy' is high. 0 - Indicates that the SoC core can initiate a mode register write operation 1 - Indicates that mode register write operation is in progress Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MRRDATA0

Address: Operational Base + offset (0x10094)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data_lwr MRR data for DQ[31:0] This register is updated when the controller issued MRR command triggered by MRCTRL register. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MRRDATA1

Address: Operational Base + offset (0x10098)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data_upr MRR data for DQ[63:32] This register is updated when the controller issued MRR command triggered by MRCTRL register. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATECTL0

Address: Operational Base + offset (0x10100)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4	RW	0x1	dis_trefi_x0125 Disables 0.125 x tREFI refresh rate for derating. When this register filed is set to 1, controller behaves like 0.25 x tREFI refresh rate mode although in 0.125 x tREFI refresh rate mode. And controller asserts interrupt signal "derate_temp_limit_intr" when receives MR4 OP[4:0] = 01110 or 01111. 0 - Enable 0.125 x tREFI refresh rate 1 - Disable 0.125 x tREFI refresh rate Note: This register field is only applicable for designs supporting LPDDR5 SDRAM. This register bit is required to set 1 if per-bank refresh "RFSHMOD0.per_bank_refresh=1" and derating "DERATECTL0.derate_enable=1" are enabled. Value After Reset:0x1 Programming Mode:Static
3	RW	0x1	dis_trefi_x6x8 Disables 8x tREFI and 6x tREFI refresh rate for derating.When this register filed is set to 1, controller behaves like 4x tREFI refresh rate mode even though in 8x tREFI and 6x tREFI mode. 0 - Enable 6x tREFI and 8x tREFI refresh rate 1 - Disable 6x tREFI and 8x tREFI refresh rate Note: This register field is only applicable for designs supporting LPDDR5 SDRAM. This register bit is required to set 1 if LPDDR5 is used. Value After Reset:0x1 Programming Mode:Dynamic - Refresh Related
2	RW	0x0	derate_mr4_pause_fc Pauses automatic MRR to MR4. For more details, see description of DERATECTL0.derate_enable. Value After Reset:0x0 Programming Mode:Dynamic
1	RW	0x0	lpddr4_refresh_mode Selects the LPDDR4 refresh mode 0 - Legacy refresh mode 1 - Modified refresh mode (Unsupported) Value After Reset:0x0 Programming Mode:Static
0	RW	0x0	derate_enable Enables derating 0 - Timing parameter derating is disabled 1 - Timing parameter derating is enabled using MR4 read value. Note that, once DERATECTL0.derate_enable is set to 1, it has to keep 1. Otherwise, the refresh rate and other timing parameters revert to their nominal values. To stop automatic MRR to MR4 temporarily after setting DERATECTL0.derate_enable =1, DERATECTL0.derate_mr4_pause_fc needs to be set to 1 without changing DERATECTL0.derate_enable. Setting DERATECTL0.derate_mr4_pause_fc=0 without changing DERATECTL0.derate_enable restarts automatic MRR to MR4. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATECTL1
Address: Operational Base + offset (0x10104)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	active_derate_byte_rank0 Indicates which byte of the MRR data is used for derating in rank0. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them This register only supports LPDDR4, LPDDR5 and DDR5. For LPDDR4 and LPDDR5: Valid width is MEMC_DRAM_DATA_WIDTH/8. This bit[n]=1 means that DQ[8*n+:8] is valid MRR data. All "0"s is invalid, if DERATECTL0.derate_enable=1. For DDR5: Valid width is MEMC_DRAM_TOTAL_DATA_WIDTH/device DQ width. Device DQ width is based on MSTR0.device_config register value. Value After Reset:0x0 Programming Mode:Static

DDRCTL_DERATECTL2

Address: Operational Base + offset (0x10108)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	active_derate_byte_rank1 Indicates which byte of the MRR data is used for derating in rank1. The each bit corresponds each byte. If the multiple register bits are enabled, controller compares refresh rate of the corresponding devices and chooses the worst refresh rate among them. This register only supports LPDDR4, LPDDR5 and DDR5. For LPDDR4 and LPDDR5: Valid width is MEMC_DRAM_DATA_WIDTH/8. This bit[n]=1 means that DQ[8*n+:8] is valid MRR data. All "0"s is invalid, if DERATECTL0.derate_enable=1. For DDR5: Valid width is MEMC_DRAM_TOTAL_DATA_WIDTH/device DQ width. Device DQ width is based on MSTR0.device_config register value. Value After Reset:0x0 Programming Mode:Static

DDRCTL_DERATECTL5

Address: Operational Base + offset (0x10114)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2	RW	0x0	derate_temp_limit_intr_force Interrupt force bit for derate_temp_limit_intr. Setting this register to 1 will cause the derate_temp_limit_intr output pin to be asserted. At the end of the interrupt force operation, the DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
1	RW	0x0	derate_temp_limit_intr_clr Interrupt clear bit for derate_temp_limit_intr. At the end of the interrupt clear operation, the DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
0	RW	0x1	derate_temp_limit_intr_en Interrupt enable bit for derate_temp_limit_intr output pin. 1 Enabled 0 Disabled Value After Reset:0x1 Programming Mode:Dynamic

DDRCTL_DERATECTL6
Address: Operational Base + offset (0x10118)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	derate_mr4_tuf_dis Disable use of MR4 TUF flag (MR4[7]) bit. 0 - Use MR4 TUF flag (MR4[7]) 1 - Do not use MR4 TUF Flag (MR4[7]) It is recommended to set this register to 1. This affects both the periodic refresh rate update and asserting interrupt signal derate_temp_limit_intr. (i.e. In derate_mr4_tuf_dis==1, the contoller can update the refresh rate, and assert the derate_temp_limit_intr if it exceeds the thresholds irrespective of tha value of TUF flag.) Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DERATESTAT0
Address: Operational Base + offset (0x1011C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	derate_temp_limit_intr Derate temperature interrupt indicating SDRAM temperature operating limit is exceeded. In LPDDR4, this register field is set to 1 when the value read from MR4[2:0] is 3'b000 or 3'b111. In LPDDR5, this register field is set to 1 when the value read from MR4[4:0] is 5'b00000 or 5'b11111 or invalid value. In DDR5, this register field is set to 1 when the value read from MR4[2:0] is the thresholds programmed by DERATECTL2.derate_low_temp_limit and DERATECTL2.derate_high_temp_limit. Cleared by register DERATECTL1.derate_temp_limit_intr_clr. Value After Reset:0x0 Testable:readOnly Programming Mode:Static

DDRCTL_DERATEDBGCTL

Address: Operational Base + offset (0x10124)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved1 Reserved Field:Yes
5:4	RW	0x0	dbg_mr4_rank_sel MR4 rank select in case of multi ranks Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x0	dbg_mr4_grp_sel MR4 data group select based on 4 device MRR read data Value After Reset:0x0 Programming Mode:Static

DDRCTL_DERATEDBGSTAT

Address: Operational Base + offset (0x10128)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	dbg_mr4_byte3 Byte 3 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5: It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1) Value After Reset:0x0 Programming Mode:Dynamic
23:16	RO	0x00	dbg_mr4_byte2 Byte 2 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5: It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1) Value After Reset:0x0 Programming Mode:Dynamic
15:8	RO	0x00	dbg_mr4_byte1 Byte 1 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5: It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1) Value After Reset:0x0 Programming Mode:Dynamic
7:0	RO	0x00	dbg_mr4_byte0 Byte 0 of selected 32 bits MR4 data. LPDDR4/LPDDR5 use 5 bits and DDR5 uses 8 bits. This register is updated when the controller issues MRR for MR4 automatically. For LPDDR4 and LPDDR5: It is occurred only if derating is enabled. (DERATECTL0.derate_enable=1) Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_PWRCTL

Address: Operational Base + offset (0x10180)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved4 Reserved Field:Yes
18	RW	0x0	dsm_en A value of 1 to this register causes system to move to Deep Sleep Mode state immediately. 1 - Entry to Deep Sleep Mode 0 - Exit from Deep Sleep Mode Value After Reset:0x0 Programming Mode:Dynamic
17	RW	0x0	lpddr4_sr_allowed Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register field cannot be modified while PWRCTL.selfref_sw==1. 0 - SR-PD -> SR -> SR-PD not allowed 1 - SR-PD -> SR -> SR-PD allowed Value After Reset:0x0 Programming Mode:Dynamic
16	RW	0x0	dis_cam_drain_selfref Indicates whether skipping CAM draining is allowed when entering Self-Refresh. This register field cannot be modified while PWRCTL.selfref_sw==1. 0 - CAMs must be empty before entering SR 1 - CAMs are not emptied before entering SR (unsupported) Note, PWRCTL.dis_cam_drain_selfref=1 is unsupported in this release. PWRCTL.dis_cam_drain_selfref=0 is required. Value After Reset:0x0 Programming Mode:Dynamic
15	RW	0x0	stay_in_selfref Self refresh state is an intermediate state to enter to Self refresh power down state or exit Self refresh power down state for LPDDR4/5. This register controls transition from the Self refresh state. 1 - Prohibit transition from Self refresh state 0 - Allow transition from Self refresh state Value After Reset:0x0 Programming Mode:Dynamic
14:12	RW	0x0	Reserved3 Reserved Field:Yes
11	RW	0x0	selfref_sw A value of 1 to this register causes system to move to Self Refresh state immediately, as long as it is not in INIT or DPD/MPSM operating mode. This is referred to as Software Entry/Exit to Self Refresh. 1 - Software Entry to Self Refresh 0 - Software Exit from Self Refresh Value After Reset:0x0 Programming Mode:Dynamic
10	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
9	RW	0x0	en_dfi_dram_clk_disable Enable the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows: In DDR4, can be asserted in following: in Self Refresh in Maximum Power Saving Mode In LPDDR4, can be asserted in following: in Self Refresh Power Down in Power Down during Normal operation (Clock Stop) In DDR5, can be asserted in following: in Self Refresh In DDR5 RDIMM, the value of this field need to be same as DIMMCTL.dimm_selfref_clock_stop_mode. Value After Reset:0x0 Programming Mode:Dynamic
8:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x0	powerdown_en If true then the DDRCTL goes into power-down after a programmable number of cycles "maximum idle clocks before power down" (PWRTMG.powerdown_to_x32). This register bit may be re-programmed during the course of normal operation. For LPDDR4/5 and DDR4, only bit[4] is used. For DDR5, powerdown per rank enable is supported. bit[4] - rank 0 powerdown_en bit[5] - rank 1 powerdown_en bit[6] - rank 2 powerdown_en bit[7] - rank 3 powerdown_en Value After Reset:0x0 Programming Mode:Dynamic
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	selfref_en If true then the DDRCTL puts the SDRAM per rank into Self Refresh after a programmable number of cycles "maximum idle clocks before Self Refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation. For LPDDR4/5 and DDR4, only bit[0] is used. For DDR5, self-refresh per rank enable is provided. Current self-refresh need to be enabled for all ranks. For DDR5 RDIMM, self-refresh need to be enabled for all ranks of both channels. bit[0] - rank 0 selfref_en bit[1] - rank 1 selfref_en bit[2] - rank 2 selfref_en bit[3] - rank 3 selfref_en Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_HWLPCTL

Address: Operational Base + offset (0x10184)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x1	hw_lp_exit_idle_en When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it will not cause exit of Self-Refresh that was caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). Value After Reset:0x1 Testable:readOnly Programming Mode:Static
0	RW	0x1	hw_lp_en Enable for Hardware Low Power Interface. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_CLKGATECTL

Address: Operational Base + offset (0x1018C)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved Field:Yes
5:0	RW	0x3f	bsm_clk_on Indicates whether the output signal bsm_clk_en [MEMC_NUM_RANKS-1:0] become 0 for each corresponding DDRCTL internal state: 0: bsm_clk_en become 0 in case where DDRCTL is in corresponding state described below 1: bsm_clk_en remain 1 in case where DDRCTL is in corresponding state The bsm_clk_en [MEMC_NUM_RANKS-1:0] indicates that clock can be removed when corresponding rank of this signal is 0. Each corresponding DDRCTL internal state is as follows: [0] Unpopulated rank control [1] Controller initialization state (until dfi0_init_start/dfi0_init_complete handshake is done) [2] Self Refresh mode [3] Self Refresh Powerdown mode [4] Powerdown mode [5] Deep Sleep Mode (LPDDR5 Only) bit[5:1] indicates behavior of the bsm_clk_en for each corresponding DDRCTL internal state. For example, if this field is set to 6'b00_0100, bsm_clk_en becomes 1 when it is in self refresh mode. This implies that bsm_clk is not removed while it is in self refresh mode, but the bsm_clk is removed by external clock gating logic in other modes above. If bit 0 (Unpopulated rank control) is set to 1, behavior of the bsm_clk_en is determined by other fields in this register irrespective of MSTR.active_ranks. If the bsm_clk_en[1]=0 is needed in case of single rank (MSTR.active_ranks=1), bit 0 has to be set to 0. To maximize power-saving, this field needs to be set to 6'b00_0000. Value After Reset:0x3f Programming Mode:Static

DDRCTL_RFSHMOD0

Address: Operational Base + offset (0x10200)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes
8	RW	0x0	per_bank_refresh 1 - Per bank refresh 0 - All bank refresh Per bank refresh allows traffic to flow to other banks. Value After Reset:0x0 Programming Mode:Static
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. 0 - single refresh 1 - burst-of-2 refresh 7 - burst-of-8 refresh In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. In DDR5 mode, according to Fine Granularity feature, 4 refreshes can be postponed in 1X mode and 8 refreshes can be postponed in 2X mode. In DDR5 mode, if self-refresh operation is expected, then this field shall not be set to the maximum number, for example, according to Fine Granularity feature, it should be smaller than 8 in 2X mode. In per-bank refresh mode of LPDDR4/5 (RFSHMOD0.per_bank_refresh = 1), 64 refreshes can be postponed. If using PHY-initiated updates, care must be taken in the setting of RFSHMOD0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst was due. In this situation, the refresh burst will be delayed until the PHY-initiated update is complete. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHCTL0

Address: Operational Base + offset (0x10208)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4	RW	0x0	refresh_update_level Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that the refresh register(s) have been updated. refresh_update_level must not be toggled when the DDRC is in reset (core_ddrc_rstn = 0). In DDR5 mode, this can be toggled during self-refresh mode and MPSM in OPS state. The refresh register(s) are automatically updated when exiting reset. Value After Reset:0x0 Programming Mode:Dynamic
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dis_auto_refresh When '1', disable auto-refresh generated by the DDRCTL. When auto-refresh is disabled, the SoC core must generate refreshes using the registers OPREFCTRL*.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the DDRCTL. If DDR4 CA parity retry is enabled (RETRYCTL0.capar_retry_enable = 1), disable auto-refresh is not supported, and this bit must be set to '0'. If FGR mode is enabled (RFSHMOD1.fgr_mode > 0), disable auto-refresh is not supported, and this bit must be set to '0'. This register field is changeable on the fly in non-DDR5 mode, and changeable during INIT/DBG/BIST state or self-refresh mode and MPSM during OPS state in DDR5 mode. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_ZQCTL0

Address: Operational Base + offset (0x10280)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1 - Disable DDRCTL generation of ZQCS/MPC(ZQ calibration) command. Register OPCTRLCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module. 0 - Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQSET1TMG1.t_zq_short_interval_x1024. This register field only applys to DDR4, LPDDR4, and LPDDR5. For DDR5, see PASCTL7~PASCTL10 registers Value After Reset:0x0 Programming Mode:Dynamic
30	RW	0x0	Reserved1 Reserved Field:Yes
29	RW	0x0	zq_resistor_shared 1 - Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap. 0 - ZQ resistor is not shared. If LPDDR5 is used, this register needs to be set to "0". Value After Reset:0x0 Programming Mode:Static

Bit	Attr	Reset Value	Description
28:0	RW	0x00000000	Reserved0 Reserved Field:Yes

DDRCTL_ZQCTL1
Address: Operational Base + offset (0x10284)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	zq_reset Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the DDRCTL automatically clears this bit. It is recommended NOT to set this register bit if in Init, in SR-Powerdown or Deep Sleep Modes. For SR-Powerdown it will be scheduled after SRPD has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

DDRCTL_ZQCTL2
Address: Operational Base + offset (0x10288)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	dis_srx_zqcl 1 - Disable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. 0 - Enable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. This is only present for designs supporting DDR4 or DDR5 or LPDDR4 or LPDDR5 devices. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_ZQSTAT
Address: Operational Base + offset (0x1028C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	zq_reset_busy SoC core may initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high. 0 - Indicates that the SoC core can initiate a ZQ Reset operation 1 - Indicates that ZQ Reset operation is in progress Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DQSOSCRUNTIME

Address: Operational Base + offset (0x10300)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x40	wck2dqo_runtime WCK2DQO interval timer run time setting as programmed in MR40 for LPDDR5.This field must be non zero. 0x0 - Interval timer stop via MPC command (not supported) 0x1 - Interval timer stops automatically at 16th clocks after timer start 0x2 - Interval timer stops automatically at 32nd clocks after timer start 0x3 - Interval timer stops automatically at 48th clocks after timer start 0x4 - Interval timer stops automatically at 64th clocks after timer start ----- Thru ---------- 0x3F - Interval timer stops automatically at (63x16)th clocks after timer start 0x40 to 0x7F - Interval timer stops automatically at 2048th clocks after timer start 0x80 to 0xBF - Interval timer stops automatically at 4096th clocks after timer start 0xC0 to 0xFF - Interval timer stops automatically at 8192nd clocks after timer start This register field is only applicable for designs supporting LPDDR5 SDRAM memories. It is don't care for LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x40 Volatile:true Programming Mode:Quasi-dynamic Group 2
15:8	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7:0	RW	0x40	dqsosc_runtime DQS interval timer run time setting as programmed in MR23 for LPDDR4; WCK2DQI interval timer run time setting as programmed in MR37 for LPDDR5; DQS interval timer run time setting as programmed in MR45 for DDR5. This field must be non zero. 0x0 - Interval timer stop via MPC command (not supported) 0x1 - Interval timer stops automatically at 16th clocks after timer start 0x2 - Interval timer stops automatically at 32nd clocks after timer start 0x3 - Interval timer stops automatically at 48th clocks after timer start 0x4 - Interval timer stops automatically at 64th clocks after timer start ----- Thru ---------- 0x3F - Interval timer stops automatically at (63x16)th clocks after timer start 0x40 to 0x7F - Interval timer stops automatically at 2048th clocks after timer start 0x80 to 0xBF - Interval timer stops automatically at 4096th clocks after timer start 0xC0 to 0xFF - Interval timer stops automatically at 8192nd clocks after timer start Unit: DRAM clock cycles. Value After Reset:0x40 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_DQSOSCSTAT0

Address: Operational Base + offset (0x10304)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved1 Reserved Field:Yes
5:4	RO	0x0	dqsosc_per_rank_stat DQS/WCK Oscillator per rank status. This bit is set to 0 when DQSOSCCTL0.dqsosc_enable is set to 1, and set to 1 when the DQS Oscillator command sequence is started for the corresponding active rank. Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RO	0x0	dqsosc_state DQS/WCK Oscillator Control State Status. 000 - DQSOSC_IDLE 001 - DQSOSC_START: Sending MPC 010 - DQSOSC_RUNTIME: Waiting for runtime passed 011 - DQSOSC_GET_RESULT1: Sending first MRR 100 - DQSOSC_WAIT1: Waiting for tMRR for sending next MRR 101 - DQSOSC_GET_RESULT2: Sending second MRR 110 - DQSOSC_WAIT2: Waiting for tMRR or rank gap Value After Reset:0x0 Programming Mode:Static

DDRCTL_DQSOSCCFG0

Address: Operational Base + offset (0x10308)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	dis_dqsosc_srx 1 - Disable issuing of DQSOSC command sequences at Self-Refresh/SR-Powerdown exit. 0 - Enable issuing of DQSOSC command sequences at Self-Refresh/SR-Powerdown exit. This is only present for designs supporting LPDDR4 or LPDDR5 or DDR5 devices. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_SCHED0

Address: Operational Base + offset (0x10380)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30	RW	0x0	dis_speculative_act Disable speculative Activate. In enhanced read write switching mode, activate commands can be issued to the other direction speculatively. This may have side-effect that the page opened for RD/WR proactively may be required to be closed to serve WR/RD respectively and it can have negative impact on performance due to command bus congestion.This register can limit such a speculative activate for the other direction. 0 Allow speculatibe activates (default) 1 Limit the speculative activates This regitser is effective only DDR4, LPDDR4 and LPDDR5. In this version, the value 1 is not fully verified hence this register must be set to 0. Value After Reset:0x0 Volatile:true Programming Mode:Static
29:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RW	0x1	lpddr5_opt_act_timing Optimized ACT timing control for LPDDR5. This register is to be used for debug purpose. In LPDDR5, ACTIVATE command is composed of two commands, ACT-1 and ACT-2. When this register is set, ACT-1 can be issued "tRRD-2" cycle after previous ACT-2. If ACT-1 is issued at this timing, the controller does not issue ACT-2 at next cycle due to tRRD. 0 - Disable (only for debug purpose) 1 - Enable (Default) This register is ignored when MSTR0.lpddr5==0. This register field is only applicable for LPDDR5 mode. Value After Reset:0x1 Volatile:true Programming Mode:Static

Bit	Attr	Reset Value	Description
15	RW	0x0	lpddr4_opt_act_timing Optimized ACT timing control for LPDDR4. In LPDDR4, RD/WR/ACT takes 4 cycle. To stream Read/Write, there are only 4 cycle space between Reads/Writes. If ACT is scheduled-out after RD/WR with 1, 2 or 3 cycle gap, next RD/WR may be pushed by 1, 2 or 3 cycle and create a gap on DQ. When this register is set, ACT is not scheduled-out with the gap = 1, 2 and 3 cycle. If enabled, there could be performance impact especially for random traffic. (Latency/Utilization) 1 - Enable this feature 0 - Disable this feature This register is ignored when MSTR0.lpddr4==0. This register field is only applicable for LPDDR4 mode. Value After Reset:0x0 Volatile:true Programming Mode:Static
14:13	RW	0x0	Reserved0 Reserved Field:Yes
12:8	RW	0x10	lpr_num_entries Number of entries in the low priority transaction store is this value + 1. (MEMC_NO_OF_ENTRY - (SCHED.lpr_num_entries + 1)) is the number of entries available for the high priority transaction store. Setting this to maximum value allocates all entries to low priority transaction store. Setting this to 0 allocates 1 entry to low priority transaction store and the rest to high priority transaction store. Note: In ECC configurations, the numbers of write and low priority read credits issued is one less than in the non-ECC case. One entry each is reserved in the write and low-priority read CAMs for storing the RMW requests arising out of single bit error correction RMW operation. Value After Reset:0x10 Volatile:true Programming Mode:Static
7	RW	0x0	autopre_rmw Select behavior of hif_cmd_autopre if a RMW is received on HIF with hif_cmd_autopre=1 1: Apply Autopre only for write part of RMW 0: Apply Autopre for both read and write parts of RMW Value After Reset:0x0 Volatile:true Programming Mode:Static
6	RW	0x0	dis_opt_ntt_by_pre Disable optimized NTT update by Precharge command. This register is debug purpose only. For normal operation, This register must be set to 0. 1: disabled 0: enabled Value After Reset:0x0 Volatile:true Programming Mode:Static

Bit	Attr	Reset Value	Description
5	RW	0x0	dis_opt_ntt_by_act Disable optimized NTT update by Activate command. This register is debug purpose only. For normal operation, This register must be set to 0. 1: disabled 0: enabled Value After Reset:0x0 Volatile:true Programming Mode:Static
4	RW	0x1	opt_wrcam_fill_level Enable the feature of optimized write CAM fill level by switching to write when write CAM reaches certain fill level set in SCHED3.wrcam_highthresh. 1: enabled 0: disabled If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. It is recommended that w_max_starve is programmed as >0 value when opt_wrcam_fill_level=1 to avoid starving extremely. Value After Reset:0x1 Volatile:true Programming Mode:Static
3	RW	0x1	rdwr_switch_policy_sel Select read write switching policy. 1: select "enhanced" read write switching policy 0: select "original" read write switching policy For DDR5, only "enhanced" read write switching policy is supported. Value After Reset:0x1 Volatile:true Programming Mode:Static
2	RW	0x1	pageclose If true, bank is kept open only while there are page hit transactions available in the CAM to that bank. The last read or write command in the CAM with a bank and page hit will be executed with auto-precharge if SCHEDTMG0.pageclose_timer=0. Even if this register set to 1 and SCHEDTMG0.pageclose_timer is set to 0, explicit precharge (and not auto-precharge) may be issued in some cases where there is a mode switch between Write and Read or between LPR and HPR. The Read and Write commands that are executed as part of the ECC scrub requests are also executed without auto-precharge. If false, the bank remains open until there is a need to close it (to open a different page, or for page timeout or refresh timeout) - also known as open page policy. The open page policy can be overridden by setting the per-command-autopre bit on the HIF interface (hif_cmd_autopre). The pageclose feature provids a midway between Open and Close page policies. FOR PERFORMANCE ONLY. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
1	RW	0x0	prefer_write If set then the bank selector prefers writes over reads. FOR DEBUG ONLY. Value After Reset:0x0 Programming Mode:Static
0	RW	0x1	dis_opt_wrecc_collision_flush In this release, this register bit is required to set to 1 in software. Value After Reset:0x1 Volatile:true Programming Mode:Static

DDRCTL_SCHED1

Address: Operational Base + offset (0x10384)

Bit	Attr	Reset Value	Description
31	RW	0x0	opt_hit_gt_hpr Optimize the priority between Page-hit LPR and Page-miss HPR 0 - Page-miss HPR has priority (default) 1 - Page-hit LPR has priority This is to choose trade-off between HPR latency and total utilization. If set to 0, HPR latency can be better than 1 because HPR has priority over LPR. If set to 1, DRAM utilization can be better than 0 because number of ACT-PRE is reduced. When this register is set to 1, recommend to enable page-hit limiter so that once page-hit limiter is expired, HPR can have priority. Value After Reset:0x0 Programming Mode:Static
30:28	RW	0x0	page_hit_limit_rd Page-Hit limiter for read. When certain number of read commands are scheduled out without ACT for a bank (schedule page-hit commands), all entries belonging to the bank priority are increased equal to page-hit entry even if these are page-miss so that oldest entry belonging to the bank can be served regardless of page-hit/page-miss. The priority is reset once any ACT/PRE/AP is served to the bank. 0 - Disable this feature 1 - 4 commands 2 - 8 commands 3 - 16 commands 4 - 32 commands else reserved Value After Reset:0x0 Volatile:true Programming Mode:Static
27	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
26:24	RW	0x0	page_hit_limit_wr Page-Hit limiter for write. When certain number of write commands are scheduled out without ACT for a bank (schedule page-hit commands), all entries belonging to the bank priority are increased equal to page-hit entry even if these are page-miss so that oldest entry belonging to the bank can be served regardless of page-hit/page-miss. The priority is reset once any ACT/PRE/AP is served to the bank. 0 - Disable this feature 1 - 4 commands 2 - 8 commands 3 - 16 commands 4 - 32 commands else reserved Value After Reset:0x0 Volatile:true Programming Mode:Static
23:16	RW	0x00	Reserved1 Reserved Field:Yes
15:12	RW	0x2	delay_switch_write delay_switch_write indicates number of cycles to delay switching read to write mode when write page-hit request is there and no read page-hit request is there. Setting higher value may reduce number of read to write switching but increase read to write turn-around time. The register indicates the number of cycles: 0: no delay 1: 2 cycles delay 2: 4 cycles delay 3: 6 cycles delay 4: 8 cycles delay ... 15:30 cycles delay If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset:0x2 Volatile:true Programming Mode:Static
11:0	RW	0x000	Reserved0 Reserved Field:Yes

DDRCTL_SCHED3

Address: Operational Base + offset (0x1038C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x04	rd_pghit_num_thresh Switch to read mode once number of read page-hit request exceeds the threshold set in the register during waiting tW2R. Set to 0 will disable the feature. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x04	wr_pghit_num_thresh Switch to write mode once number of write page-hit request exceeds threshold set in this register during waiting delay_switch_write timeout. Set to 0 will disable the feature. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 3
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x02	wrcam_highthresh The high threshold used in optimized write CAM fill level. When (MEMC_NO_OF_ENTRY - (number of loaded entries) < wrcam_highthresh), switch to write mode and prepare banks for write direction if no Exp-VPR or read collision is there. wrcam_highthresh must be set to a smaller value than wrcam_lowthresh. Note: In Sideband ECC configuration, the number of write entries is (MEMC_NO_OF_ENTRY-1) - except if MEMC_INLINE_ECC=1 is also set, where number of entries is MEMC_NO_OF_ENTRY for Inline ECC mode, otherwise, (MEMC_NO_OF_ENTRY-1). This feature is enabled when opt_wrcam_fill_level is 1. Value After Reset:0x2 Volatile:true Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x08	wrcam_lowthresh The low threshold used in optimized write CAM fill level. When (MEMC_NO_OF_ENTRY - (number of loaded entries) < wrcam_lowthresh), keep to write mode and stop to prepare banks for read direction if no Exp-VPR or read collision is there. Note: In Sideband ECC configuration, the number of write entries is (MEMC_NO_OF_ENTRY-1) - except if MEMC_INLINE_ECC=1 is also set, where number of entries is MEMC_NO_OF_ENTRY for Inline ECC mode, otherwise, (MEMC_NO_OF_ENTRY-1). This feature is enabled when opt_wrcam_fill_level is 1. Value After Reset:0x8 Volatile:true Programming Mode:Static

DDRCTL_SCHED4
Address: Operational Base + offset (0x10390)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	wr_page_exp_cycles wr_page_exp_cycles indicates number of cycles to keep the bank opened for write direction in read mode when both directions has request to the bank. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 3
23:16	RW	0x40	rd_page_exp_cycles rd_page_exp_cycles indicates number of cycles to keep the bank opened for read direction in write mode when both directions has request to the bank. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset:0x40 Volatile:true Programming Mode:Quasi-dynamic Group 3
15:8	RW	0x08	wr_act_idle_gap wr_act_idle_gap indicates number of cycles when write direction has no request to start preparing bank for read direction. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 3
7:0	RW	0x10	rd_act_idle_gap rd_act_idle_gap indicates number of cycles when read direction has no request to start preparing bank for write direction. The register indicates the number of cycle. If MEMC_RDWR_SWITCH_POL_SEL==1 && rdwr_switch_policy_sel==0, this register will be ignored. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_SCHED5
Address: Operational Base + offset (0x10394)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes
29	RW	0x0	dis_opt_valid_wrecc_cam_fill_level In this release, this register bit, dis_opt_valid_wrecc_cam_fill_level, is required to set to 0 in software. Value After Reset:0x0 Volatile:true Programming Mode:Static

Bit	Attr	Reset Value	Description
28	RW	0x1	dis_opt_loaded_wrecc_cam_fill_level In this release, this register bit, dis_opt_loaded_wrecc_cam_fill_level, is required to set to 0 in software. Value After Reset:0x1 Volatile:true Programming Mode:Static
27:12	RW	0x0000	Reserved1 Reserved Field:Yes
11:8	RW	0x2	wrecc_cam_highthresh The high threshold used in optimized write ECC CAM fill level. When (MEMC_NO_OF_ENTRY/2 - (number of loaded entries) < wrecc_cam_highthresh), switch to write mode and prepare banks for write direction if no Exp-VPR or read collision is there. This feature is enabled when opt_wrcam_fill_level is 1. Value After Reset:0x2 Volatile:true Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RW	0x4	wrecc_cam_lowthresh The low threshold used in optimize write ECC CAM fill level. When (MEMC_NO_OF_ENTRY/2 - (number of loaded entries) < wrecc_cam_lowthresh), keep to write mode and stop to prepare banks for read direction if no Exp-VPR or read collision is there. This feature is enabled when opt_wrcam_fill_level is 1. Value After Reset:0x4 Volatile:true Programming Mode:Static

DDRCTL_DFILPCFG0

Address: Operational Base + offset (0x10500)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved4 Reserved Field:Yes
20	RW	0x1	dfi_lp_data_req_en Enables DFI Data Low Power interface. 0 - Disabled. dfi_lp_data_req is not asserted. 1 - Enabled Value After Reset:0x1 Programming Mode:Static
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16	RW	0x0	dfi_lp_en_data Enables DFI Data Low Power interface handshaking during data bus idle. 0 - Disabled 1 - Enabled Value After Reset:0x0 Programming Mode:Static
15:9	RW	0x00	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
8	RW	0x0	dfi_lp_en_dsm Enables DFI Low Power interface handshaking during Deep Sleep Mode Entry/Exit. 0 - Disabled 1 - Enabled This is only present for designs supporting LPDDR5 devices. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x0	dfi_lp_en_sr Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit. 0 - Disabled 1 - Enabled Value After Reset:0x0 Programming Mode:Static
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit. 0 - Disabled 1 - Enabled Value After Reset:0x0 Programming Mode:Static

DDRCTL_DFIUPD0
Address: Operational Base + offset (0x10508)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_ctrlupd 0 - DDRCTL issues dfi_ctrlupd_req periodically. 1 - Disable the automatic dfi_ctrlupd_req generation by the DDRCTL. The core must issue the dfi_ctrlupd_req signal using register OPCTRLCMD.ctrlupd. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
30	RW	0x0	dis_auto_ctrlupd_srx 0 - DDRCTL issues a dfi_ctrlupd_req before or after exiting self refresh, depending on DFIUPD0.ctrlupd_pre_srx. 1 - Disable the automatic dfi_ctrlupd_req generation by the DDRCTL at self-refresh exit. Value After Reset:0x0 Volatile:true Programming Mode:Static
29	RW	0x0	ctrlupd_pre_srx Selects dfi_ctrlupd_req requirements at SRX: 0 : send ctrlupd after SRX 1 : send ctrlupd before SRX If DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req will be issued when SRX. Value After Reset:0x0 Programming Mode:Static

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	Reserved1 Reserved Field:Yes
15	RW	0x1	dfi_phyupd_en Enables the support for acknowledging PHY-initiated updates: 0 - Disabled 1 - Enabled Value After Reset:0x1 Programming Mode:Static
14:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_DFIMISC

Address: Operational Base + offset (0x10510)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved3 Reserved Field:Yes
17:16	RW	0x0	dfi_channel_mode This field controls how internal DFI data is connected to dfi0_*data* and dfi1_*data*. This must be set to 2'b00. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved2 Reserved Field:Yes
12:8	RW	0x00	dfi_frequency Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1
7	RW	0x0	lp_optimized_write If this bit is 1, LPDDR4 write DQ is set to 8'hF8 if masked write with enabling DBI; otherwise, that value is set to 8'hFF Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
6	RW	0x0	Reserved1 Reserved Field:Yes
5	RW	0x0	dfi_init_start PHY init start request signal.When asserted it triggers the PHY init start request Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
4:3	RW	0x0	Reserved0 Reserved Field:Yes
2	RW	0x0	dfi_data_cs_polarity Defines polarity of dfi_wrdata_cs and dfi_rddata_cs signals. 0: Signals are active low 1: Signals are active high Value After Reset:0x0 Programming Mode:Static

Bit	Attr	Reset Value	Description
1	RW	0x0	phy_dbi_mode DBI implemented in DDRC or PHY. 0 - DDRC implements DBI functionality. 1 - PHY implements DBI functionality. Present only in designs configured to support DDR4 and LPDDR4. Value After Reset:0x0 Programming Mode:Static
0	RW	0x1	dfi_init_complete_en PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialisation Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_DFISTAT

Address: Operational Base + offset (0x10514)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2	RO	0x0	dfi_lp_data_ack_stat Stores the value of the dfi_lp_data_ack input to the controller. Value After Reset:0x0 Programming Mode:Dynamic
1	RO	0x0	dfi_lp_ctrl_ack_stat Stores the value of the dfi_lp_ctrl_ack input to the controller. Value After Reset:0x0 Programming Mode:Dynamic
0	RO	0x0	dfi_init_complete The status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DFIPHYMSTR

Address: Operational Base + offset (0x10518)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	dfi_phymstr_blk_ref_x32 The programmed value x32 is the maximum number of DFI clock cycles that allows to send pending refreshes before starting self-refresh entry process. - 0x00 - 0 DFI clock cycles, no delay - 0x01 - 32 DFI clock cycles - ... - 0xFF - 8160 DFI clock cycles Unit: Multiples of 32 DFI clock cycles. Note: Use as default value (0x80). Value After Reset:0x80 Programming Mode:Static
23:1	RW	0x000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
0	RW	0x1	dfi_phymstr_en Enables the PHY Master Interface: 0 - Disabled 1 - Enabled Value After Reset:0x1 Programming Mode:Static

DDRCTL_DFI0MSGCTL0

Address: Operational Base + offset (0x10520)

Bit	Attr	Reset Value	Description
31	RW	0x0	dfi0_ctrlmsg_req Setting this register bit to 1 triggers a DFI controller message transmission operation. DDRCTL automatically clear this bit when the DFI controller message request (dfi0_ctrlmsg_req) is asserted at the DFI MC to PHY Message port interface. This bit must be programmed separately after programming other register fields appropriately of this register. Note: DFI controller message request can be issued only if DFIPHYMSTR.dfi_phymstr_en = 1 DFI controller message request must not be set during DFI LP mode due to software controlled low power entry. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
30:25	RW	0x00	Reserved0 Reserved Field:Yes
24	RW	0x0	dfi0_ctrlmsg_tout_clr If this bit is set, DFI0MSGSTAT0.dfi0_ctrlmsg_resp_tout is cleared by the controller. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
23:16	RW	0x00	dfi0_ctrlmsg_cmd DFI0 controller message command. Value After Reset:0x0 Programming Mode:Dynamic
15:0	RW	0x0000	dfi0_ctrlmsg_data DFI0 controller message data. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DFI0MSGSTAT0

Address: Operational Base + offset (0x10524)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RO	0x0	dfi0_ctrlmsg_resp_tout This bit is set if dfi0_ctrlmsg_ack is not asserted by PHY within dfi_t_ctrlmsg_resp after asserting dfi0_ctrlmsg_req Value After Reset:0x0 Programming Mode:Dynamic
15:1	RW	0x0000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
0	RO	0x0	dfi0_ctrlmsg_req_busy The SoC must trigger DFI controller message request only if this signal is low. This signal goes high in the clock after the DDRCTL accepts software triggered DFI controller message request by writing into DFI0MSGCTRL0.dfi0_ctrlmsg_req. It goes low when PHY deasserts dfi0_ctrlmsg_ack or dfi0_ctrlmsg_resp_tout event has triggered. 0 - Indicates that the SoC core can initiate a DFI controller message request operation 1 - Indicates that DFI controller message request operation is in progress Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_POISONCFG

Address: Operational Base + offset (0x10580)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved5 Reserved Field:Yes
24	RW	0x0	rd_poison_intr_clr Interrupt clear for read transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
23:21	RW	0x0	Reserved4 Reserved Field:Yes
20	RW	0x1	rd_poison_intr_en If set to 1, enables interrupts for read transaction poisoning Value After Reset:0x1 Programming Mode:Dynamic
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16	RW	0x1	rd_poison_slverr_en If set to 1, enables SLVERR response for read transaction poisoning Value After Reset:0x1 Programming Mode:Dynamic
15:9	RW	0x00	Reserved2 Reserved Field:Yes
8	RW	0x0	wr_poison_intr_clr Interrupt clear for write transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x1	wr_poison_intr_en If set to 1, enables interrupts for write transaction poisoning Value After Reset:0x1 Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x1	wr_poison_slverr_en If set to 1, enables SLVERR response for write transaction poisoning Value After Reset:0x1 Programming Mode:Dynamic

DDRCTL_POISONSTAT

Address: Operational Base + offset (0x10584)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RO	0x0	rd_poison_intr_0 Read transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Value After Reset:0x0 Programming Mode:Dynamic
15:1	RW	0x0000	Reserved0 Reserved Field:Yes
0	RO	0x0	wr_poison_intr_0 Write transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCCFG0

Address: Operational Base + offset (0x10600)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	ecc_region_map_granu Granularity of Selectable Protected Region. Define one region size for ECCCFG0.ecc_region_map 0 - 1/8 of memory spaces 1 - 1/16 of memory spaces 2 - 1/32 of memory spaces 3 - 1/64 of memory spaces Value After Reset:0x0 Programming Mode:Static

Bit	Attr	Reset Value	Description
29	RW	0x0	ecc_region_map_other When ECCCFG0.ecc_region_map_granu>0, there is a region which is not controlled by ecc_region_map. This register defines the region to be protected or non-protected for Inline ECC. 0 - Non-Protected 1 - Protected This register is valid only when ECCCFG0.ecc_region_map_granu>0 && ECCCFG0.ecc_mode=4. Value After Reset:0x0 Programming Mode:Static
28:26	RW	0x0	Reserved3 Reserved Field:Yes
25:24	RW	0x1	ecc_ap_err_threshold Set threshold for address parity error. ECCAPSTAT.ecc_ap_err is asserted if number of ECC errors (correctable/uncorrectable) within one burst exceeds this threshold. This register value must be less than "Total number of ECC checks within one burst" when this feature is used, "Total number of ECC check within one burst" is calculated by (DRAM Data width) x (DRAM BL) / 64. Value After Reset:0x1 Programming Mode:Static
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x3f	blk_channel_idle_time_x32 Indicates the number of cycles on HIF interface with no access to protected regions which will cause flush of all the block channels. In order to flush block channel, DDRCTL injects write ECC command (when there is no incoming HIF command) if there is any write in the block and then stop tracking the block address. 0 indicates no timeout (feature is disabled, not supported with this version) 1 indicates 32 cycles 2 indicates 2*32 cycles, etc. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x3f Volatile:true Programming Mode:Quasi-dynamic Group 3
15	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
14:8	RW	0x7f	ecc_region_map Selectable Protected Region setting. Memory space is divided to 8/16/32/64 regions which is determined by ECCCFG0.ecc_region_map_granu. Note: Highest 1/8 memory space is always ECC region. Lowest 7 regions are Selectable Protected Regions. The Selectable Protected Regions can be protected/non-protected selectively by ECCCFG0.ecc_region_map[6:0]. Other upper regions are non-protected region if any. Each bit of ECCCFG0.ecc_region_map[6:0] correspond to each of lowest 7 regions respectively. In order to protect a region with ECC, set the corresponding bit to 1, otherwise set to 0. All "0"s is invalid - there must be at least one protected region if inline ECC is enabled via ECCCFG0.ecc_mode register. All regions are protected with the following setting. ecc_region_map=7'b1111111 ecc_region_map_granu=0 Only first 1/64 region is protected with the following setting. ecc_region_map=7'b0000001 ecc_region_map_granu=3 Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3
7	RW	0x0	ecc_region_remap_en Enables remapping ECC region feature. Only supported when inline ECC is enabled. 0 - Disable 1 - Enable Value After Reset:0x0 Programming Mode:Static
6	RW	0x1	ecc_ap_en Enable address protection feature. Only supported when inline ECC is enabled. 0: disable 1: enable Value After Reset:0x1 Programming Mode:Static
5:3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x0	ecc_mode ECC mode indicator 000 - ECC disabled 100 - ECC enabled - SEC/DED 101 - ECC enabled - Advanced ECC (Illegal value when MEMC_INLINE_ECC=1) all other settings are reserved for future use Value After Reset:0x0 Programming Mode:Static

DDRCTL_ECCCFG1

Address: Operational Base + offset (0x10604)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x03	active_blk_channel Number of active block channels. Total number of ECC block channels are defined by MEMC_NO_OF_BLK_CHANNEL hardware parameter. This register can limit the number of available channels. For example, if set to 0, only one channel is active and therefore block interleaving is disabled. The valid range is from 0 to MEMC_NO_OF_BLK_CHANNEL-1. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 3
7	RW	0x1	blk_channel_active_term Block Channel active terminate enable. If enabled, block channel is terminated when full block write or full block read is performed (all address within block are written or read) 0 - Disable (only for debug purpose) 1 - Enable (default) This is debug register, and this must be set to 1 for normal operation. Value After Reset:0x1 Volatile:true Programming Mode:Static
6	RW	0x0	Reserved1 Reserved Field:Yes
5	RW	0x1	ecc_region_waste_lock Locks the remaining waste parts of the ECC region (hole) that are not locked by ecc_region_parity_lock. 1: Locked; if this region is accessed, error response is generated. 0: Unlocked; this region can be accessed normally, similar to non-ECC protected region. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3
4	RW	0x1	ecc_region_parity_lock Locks the parity section of the ECC region (hole) which is the highest system address part of the memory that stores ECC parity for protected region. 1: Locked; if this region is accessed, error response is generated. 0: Unlocked; this region can be accessed normally, similar to non-ECC protected region. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	data_poison_bit Selects whether to poison 1 or 2 bits - if 0 -> 2-bit (uncorrectable) data poisoning, if 1 -> 1-bit (correctable) data poisoning, if ECCCFG1.data_poison_en=1. Valid only when MEMC_ECC_SUPPORT==1 or 3 (in SECDED ECC mode i.e ECCCFG0.ecc_mode=3'b100) Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
0	RW	0x0	data_poison_en Enable ECC data poisoning - introduces ECC errors on writes to address specified by the ECCPOISONADDR0/1 registers This field must be set to 0 if ECC is disabled (ECCCFG0.ecc_mode = 0). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_ECCSTAT

Address: Operational Base + offset (0x10608)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved3 Reserved Field:Yes
25	RO	0x0	sbr_read_ecc_ue Indicates the uncorrectable error interrupt is due to read operation by scrubber. This bit is cleared on ECCCTL.ecc_uncorrected_err_clr 0 - Mainline/Demand read uncorrectable error interrupt 1 - Scrubber read uncorrectable error interrupt Value After Reset:0x0 Programming Mode:Static
24	RO	0x0	sbr_read_ecc_ce Indicates the correctable error interrupt is due to read operation by scrubber. This bit is cleared on ECCCTL.ecc_corrected_err_clr 0 - Mainline/Demand read correctable error interrupt 1 - Scrubber read correctable error interrupt Value After Reset:0x0 Programming Mode:Static
23:17	RW	0x00	Reserved2 Reserved Field:Yes
16	RO	0x0	ecc_uncorrected_err Double-bit error indicator. In sideband ECC mode, 1 bit per ECC lane. In inline ECC mode, the register always is 1 bit to indicate uncorrectable error on any lane. Value After Reset:0x0 Programming Mode:Static
15:9	RW	0x00	Reserved1 Reserved Field:Yes
8	RO	0x0	ecc_corrected_err Single-bit error indicator. In sideband ECC mode, 1 bit per ECC lane. In inline ECC mode, the register always is 1 bit to indicate correctable error on any lane. Value After Reset:0x0 Programming Mode:Static
7	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
6:0	RO	0x00	ecc_corrected_bit_num Bit number corrected by single-bit ECC error. See ECC section of architecture chapter for encoding of this field. If more than one data lane has an error, the lower data lane is selected. This register is 7 bits wide in order to handle 72 bits of the data present in a single lane. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ECCCTL
Address: Operational Base + offset (0x1060C)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved2 Reserved Field:Yes
18	RW	0x0	ecc_ap_err_intr_force Interrupt force bit for ecc_ap_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
17	RW	0x0	ecc_uncorrected_err_intr_force Interrupt force bit for ecc_uncorrected_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
16	RW	0x0	ecc_corrected_err_intr_force Interrupt force bit for ecc_corrected_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
15:11	RW	0x00	Reserved1 Reserved Field:Yes
10	RW	0x1	ecc_ap_err_intr_en Interrupt enable bit for ecc_ap_err_intr. 1: Enabled 0: Disabled Value After Reset:0x1 Programming Mode:Dynamic
9	RW	0x1	ecc_uncorrected_err_intr_en Interrupt enable bit for ecc_uncorrected_err_intr. 1: Enabled 0: Disabled Value After Reset:0x1 Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
8	RW	0x1	ecc_corrected_err_intr_en Interrupt enable bit for ecc_corrected_err_intr. 1 Enabled 0 Disabled Value After Reset:0x1 Programming Mode:Dynamic
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4	RW	0x0	ecc_ap_err_intr_clr Interrupt clear bit for ecc_ap_err. If this bit is set, the ECCAPSTAT.ecc_ap_err/ecc_ap_err_intr will be cleared. DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
3	RW	0x0	ecc_uncorr_err_cnt_clr Setting this register bit to 1 clears the currently stored uncorrected ECC error count. The ECCERRCNT.ecc_uncorr_err_cnt register is cleared by this operation. DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
2	RW	0x0	ecc_corr_err_cnt_clr Setting this register bit to 1 clears the currently stored corrected ECC error count. The ECCERRCNT.ecc_corr_err_cnt register is cleared by this operation. DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
1	RW	0x0	ecc_uncorrected_err_clr Setting this register bit to 1 clears the currently stored uncorrected ECC error. The following registers are cleared: ECCSTAT.ecc_uncorrected_err ECCSTAT.sbr_read_ecc_ue ADVECCSTAT.sbr_read_advecc_ue ADVECCSTAT.advecc_uncorr_err_kbd_stat ADVECCSTAT.advecc_uncorrected_err ECCUSYN0 ECCUSYN1 ECCUSYN2 ECCUDATA0 ECCUDATA1 ECCSYMBOL.ecc_uncorr_sym_71_64 DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
0	RW	0x0	ecc_corrected_err_clr Setting this register bit to 1 clears the currently stored corrected ECC error. The following registers are cleared: ECCSTAT.ecc_corrected_err ECCSTAT.sbr_read_ecc_ce ADVECCSTAT.sbr_read_advecc_ce ADVECCSTAT.advecc_corr_err_kbd_stat ADVECCSTAT.advecc_corrected_err ADVECCSTAT.advecc_num_err_symbol ADVECCSTAT.advecc_err_symbol_pos ADVECCSTAT.advecc_err_symbol_bits ECCCSYN0 ECCCSYN1 ECCCSYN2 ECCBITMASK0 ECCBITMASK1 ECCBITMASK2 ECCCDATA0 ECCCDATA1 ECCSYMBOL.ecc_corr_sym_71_64 DDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

DDRCTL_ECCERRCNT
Address: Operational Base + offset (0x10610)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ecc_uncorr_err_cnt Number of uncorrectable ECC errors detected. It will saturates at 0xFFFF Value After Reset:0x0 Programming Mode:Dynamic
15:0	RO	0x0000	ecc_corr_err_cnt Number of correctable ECC errors detected. It will saturates at 0xFFFF Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCCADDR0
Address: Operational Base + offset (0x10614)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes
24	RO	0x0	ecc_corr_rank Indicates the rank number of a read resulting in a corrected ECC error Value After Reset:0x0 Programming Mode:Dynamic
23:18	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
17:0	RO	0x00000	ecc_corr_row Indicates the page/row number of a read resulting in a corrected ECC error. This is 18-bits wide in configurations with DDR4 support and 16-bits in all other configurations. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCCADDR1
Address: Operational Base + offset (0x10618)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved2 Reserved Field:Yes
25:24	RO	0x0	ecc_corr_bg Bank Group number of a read resulting in a corrected ECC error. Value After Reset:0x0 Programming Mode:Dynamic
23:19	RW	0x00	Reserved1 Reserved Field:Yes
18:16	RO	0x0	ecc_corr_bank Bank number of a read resulting in a corrected ECC error. Value After Reset:0x0 Programming Mode:Dynamic
15:11	RW	0x00	Reserved0 Reserved Field:Yes
10:0	RO	0x000	ecc_corr_col Block number of a read resulting in a corrected ECC error (lowest bit not assigned here). Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCCSYN0
Address: Operational Base + offset (0x1061C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ecc_corr_syndromes_31_0 Data pattern that resulted in a corrected error. For 16-bit ECC, only bits [15:0] are used. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. This field will be cleared when ecc_corrected_err_clr is set. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCCSYN1
Address: Operational Base + offset (0x10620)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ecc_corr_syndromes_63_32 Data pattern that resulted in a corrected error. For 32-bit ECC and 16-bit ECC, this register is not used. However, for multi-beat ECC, it represents the data pattern of odd SDRAM data beat (ECC lane). This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. This field will be cleared when ecc_corrected_err_clr is set. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCCSYN2

Address: Operational Base + offset (0x10624)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RO	0x00	ecc_corr_syndromes_71_64 Indicates the data pattern that resulted in a corrected error one for each ECC lane, all concatenated together. This register refers to the ECC byte, which is bits [71:64] for 64-bit ECC, [39:32] for 32-bit ECC, or [23:16] for 16-bit ECC. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. This field will be cleared when ecc_corrected_err_clr is set. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCBITMASK0

Address: Operational Base + offset (0x10628)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ecc_corr_bit_mask_31_0 Mask for the corrected data portion 1 on any bit indicates that the bit has been corrected by the ECC logic 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. For 16-bit ECC, only bits [15:0] are used Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCBITMASK1

Address: Operational Base + offset (0x1062C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ecc_corr_bit_mask_63_32 Mask for the corrected data portion 1 on any bit indicates that the bit has been corrected by the ECC logic 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. For 32-bit ECC and 16-bit ECC, this register is not used. However, for multi-beat ECC, it represents the ECC errors of odd SDRAM data beat (ECC lane). Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCBITMASK2

Address: Operational Base + offset (0x10630)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7:0	RO	0x00	ecc_corr_bit_mask_71_64 Mask for the corrected data portion 1 on any bit indicates that the bit has been corrected by the ECC logic 0 on any bit indicates that the bit has not been corrected by the ECC logic This register accumulates data over multiple ECC errors, to give an overall indication of which bits are being fixed. It is cleared by writing a 1 to ECCCTL.ecc_corrected_err_clr. This register refers to the ECC byte, which is bits [71:64] for 64-bit ECC, [39:32] for 32-bit ECC, or [23:16] for 16-bit ECC Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCUADDR0
Address: Operational Base + offset (0x10634)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes
24	RO	0x0	ecc_uncorr_rank Rank number of a read resulting in an uncorrected ECC error. Value After Reset:0x0 Programming Mode:Dynamic
23:18	RW	0x00	Reserved0 Reserved Field:Yes
17:0	RO	0x00000	ecc_uncorr_row Page/row number of a read resulting in an uncorrected ECC error. This is 18-bits wide in configurations with DDR4 support and 16-bits in all other configurations. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCUADDR1
Address: Operational Base + offset (0x10638)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved2 Reserved Field:Yes
25:24	RO	0x0	ecc_uncorr_bg Bank Group number of a read resulting in an uncorrected ECC error Value After Reset:0x0 Programming Mode:Dynamic
23:19	RW	0x00	Reserved1 Reserved Field:Yes
18:16	RO	0x0	ecc_uncorr_bank Bank number of a read resulting in an uncorrected ECC error Value After Reset:0x0 Programming Mode:Dynamic
15:11	RW	0x00	Reserved0 Reserved Field:Yes
10:0	RO	0x000	ecc_uncorr_col Block number of a read resulting in an uncorrected ECC error (lowest bit not assigned here) Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCUSYN0
Address: Operational Base + offset (0x1063C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ecc_uncorr_syndromes_31_0 Data pattern that resulted in an uncorrected error, one for each ECC lane, all concatenated together. For 16-bit ECC, only bits [15:0] are used. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCUSYN1
Address: Operational Base + offset (0x10640)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ecc_uncorr_syndromes_63_32 Data pattern that resulted in an uncorrected error, one for each ECC lane, all concatenated together. For 32-bit ECC and 16-bit ECC, this register is not used. However, for multi-beat ECC, it represents the data pattern of odd SDRAM data beat (ECC lane). This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCUSYN2
Address: Operational Base + offset (0x10644)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RO	0x00	ecc_uncorr_syndromes_71_64 Data pattern that resulted in an uncorrected error one for each ECC lane, all concatenated together. This register refers to the ECC byte, which is bits [71:64] for 64-bit ECC, [39:32] for 32-bit ECC, or [23:16] for 16-bit ECC. This field can be masked by setting the dis_regs_ecc_syndrome input to value 1. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ECCPOISONADDR0
Address: Operational Base + offset (0x10648)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes
24	RW	0x0	ecc_poison_rank Rank address for ECC poisoning Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
23:12	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x000	ecc_poison_col Indicates the column address for ECC poisoning. Note that this column address must be burst aligned: In full bus width mode, ecc_poison_col[2:0] must be set to 0 In half bus width mode, ecc_poison_col[3:0] must be set to 0 In quarter bus width mode, ecc_poison_col[4:0] must be set to 0 Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_ECCPOISONADDR1

Address: Operational Base + offset (0x1064C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes
29:28	RW	0x0	ecc_poison_bg Bank Group address for ECC poisoning Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
27	RW	0x0	Reserved1 Reserved Field:Yes
26:24	RW	0x0	ecc_poison_bank Bank address for ECC poisoning Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
23:18	RW	0x00	Reserved0 Reserved Field:Yes
17:0	RW	0x00000	ecc_poison_row Row address for ECC poisoning. This is 18-bits wide in configurations with DDR4 support and 16-bits in all other configurations. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_ECCAPSTAT

Address: Operational Base + offset (0x10664)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	ecc_ap_err Indicates the number of ECC errors (correctable/uncorrectable) within one burst exceeded the threshold.(ECCCFG0.ecc_ap_err_threshold) Value After Reset:0x0 Programming Mode:Static

DDRCTL_LNKECCCTL0

Address: Operational Base + offset (0x10980)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
1	RW	0x0	rd_link_ecc_enable Enable LPDDR5 Read Link ECC feature. 0 - Disabel LPDDR5 Read Link ECC 1 - Enable LPDDR5 Read Link ECC When non-LPDDR5 devices are used, this register must be set to 0. Value After Reset:0x0 Volatile:true Programming Mode:Static
0	RW	0x0	wr_link_ecc_enable Enable LPDDR5 Write Link ECC feature. 0 - Disabel LPDDR5 Write Link ECC 1 - Enable LPDDR5 Write Link ECC When non-LPDDR5 devices are used, this register must be set to 0. Value After Reset:0x0 Volatile:true Programming Mode:Static

DDRCTL_LNKECCCTL1

Address: Operational Base + offset (0x10984)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7	RW	0x0	rd_link_ecc_uncorr_intr_force Interrupt force bit for rd_linkecc_uncorr_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
6	RW	0x0	rd_link_ecc_uncorr_cnt_clr Clear all Read Link-ECC uncorrectable error count. If this bit set, LNKECCERRCNT0.rd_link_ecc_uncorr_cnt will be cleared. LPDDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
5	RW	0x0	rd_link_ecc_uncorr_intr_clr Clear Read Link-ECC uncorrectable error interrupt. If this bit set, rd_linkecc_uncorr_err_intr will be cleared. LPDDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
4	RW	0x0	rd_link_ecc_uncorr_intr_en Interrupt enable bit for Read Link-ECC uncorrectable error. Value After Reset:0x0 Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
3	RW	0x0	rd_link_ecc_corr_intr_force Interrupt force bit for rd_linkecc_corr_err_intr. Setting this register will cause the output interrupt to be asserted. DDRCTL automatically clears this bit. There is no interaction between functionally triggering an interrupt and forcing an interrupt (they are mutually exclusive). Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
2	RW	0x0	rd_link_ecc_corr_cnt_clr Clear all Read Link-ECC correctable error count. If this bit set,LNKECCERRCNT0.rd_link_ecc_corr_cnt will be cleared. LPDDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
1	RW	0x0	rd_link_ecc_corr_intr_clr Clear Read Link-ECC correctable error interrupt. If this bit set, rd_linkecc_corr_err_intr will be cleared. LPDDRCTL automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
0	RW	0x0	rd_link_ecc_corr_intr_en Interrupt enable bit for Read Link-ECC correctable error. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_LNKECCPOISONCTL0
Address: Operational Base + offset (0x10988)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved2 Reserved Field:Yes
25:24	RW	0x0	linkecc_poison_byte_sel Select target byte(s) of Data for Write Link ECC poisoning. This is bit map indicator. Bit N corresponding to Data[N*8+:8]. Value After Reset:0x0 Programming Mode:Dynamic
23:18	RW	0x00	Reserved1 Reserved Field:Yes
17:16	RW	0x0	linkecc_poison_dmi_sel Select target DMI(s) of Data for Write Link ECC poisoning. This is bit map indicator. Bit N corresponding to DMI[N]. Value After Reset:0x0 Programming Mode:Dynamic
15:3	RW	0x0000	Reserved0 Reserved Field:Yes
2	RW	0x0	linkecc_poison_rw Indicates whether the Link-ECC poisoning operation is Read or Write. 0 - Write 1 - Read Value After Reset:0x0 Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
1	RW	0x0	linkecc_poison_type Indicates whether the Link-ECC poisoning operation is Single-bit error or Double bit error. 0 - Single bit Error 1 - Double bit Error Value After Reset:0x0 Programming Mode:Dynamic
0	RW	0x0	linkecc_poison_inject_en Setting this register bit to 1 triggers the Link-ECC poisoning. Once Link-ECC is poisoned to a ECC code, the ECC poisoning is completed automatically and LNKECCPOISONSTAT.linkecc_poison_complete becomes 1. Please make sure that LNKECCPOISONSTAT.linkecc_poison_complete==0 before writing this register to 1. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_LNKECCPOISONSTAT

Address: Operational Base + offset (0x1098C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	linkecc_poison_complete Indicates Link-ECC poisoning operation is done. 0 - Link-ECC poisoning is not completed 1 - Link-ECC poisoning is completed Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_LNKECCINDEX

Address: Operational Base + offset (0x10990)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved1 Reserved Field:Yes
5:4	RW	0x0	rd_link_ecc_err_rank_sel Select of which rank status output to LNKECCERRCNT.rd_link_ecc_uncorr_cnt, rd_link_ecc_corr_cnt and rd_link_ecc_err_syndrome. The value must be less than MEMC_NUM_RANKS. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x0	rd_link_ecc_err_byte_sel Select of which data byte status output to LNKECCERRCNT.rd_link_ecc_uncorr_cnt, rd_link_ecc_corr_cnt and rd_link_ecc_err_syndrome. The value must be less than MEMC_DRAM_DATA_WIDTH/8. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1

DDRCTL_LNKECCERRCNT0

Address: Operational Base + offset (0x10994)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	rd_link_ecc_uncorr_cnt Indicates double bit error count. Value After Reset:0x0 Programming Mode:Dynamic
23:16	RO	0x00	rd_link_ecc_corr_cnt Indicates single bit error count. Value After Reset:0x0 Programming Mode:Dynamic
15:9	RW	0x00	Reserved0 Reserved Field:Yes
8:0	RO	0x000	rd_link_ecc_err_syndrome Indicates ECC syndrome from most recent single bit error. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_LNKECCERRSTAT

Address: Operational Base + offset (0x10998)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved1 Reserved Field:Yes
11:8	RO	0x0	rd_link_ecc_uncorr_err_int Indicates double bit error for Read Link-ECC. If double bit error happens, this interrupt bit is set. It remains set until cleared by LNKECCCTL1.rd_link_ecc_uncorr_intr_clr. Each bit represents one rank. (LSB is the lowest rank number.) Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RO	0x0	rd_link_ecc_corr_err_int Indicates single bit error for Read Link-ECC. If signle bit error happens, this interrupt bit is set. It remains set until cleared by LNKECCCTL1.rd_link_ecc_corr_intr_clr. Each bit represents one rank. (LSB is the lowest rank number.) Value After Reset:0x0 Programming Mode:Static

DDRCTL_OPCTRL0

Address: Operational Base + offset (0x10B80)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved2 Reserved Field:Yes
7	RW	0x0	dis_max_rank_wr_opt Disable optimized max_rank_wr and max_logical_rank_wr feature. This register is debug purpose only. For normal operation, This register must be set to 0. Value After Reset:0x0 Volatile:true Programming Mode:Static

Bit	Attr	Reset Value	Description
6	RW	0x0	dis_max_rank_rd_opt Disable optimized max_rank_rd and max_logical_rank_rd feature. This register is debug purpose only. For normal operation, This register must be set to 0. Value After Reset:0x0 Volatile:true Programming Mode:Static
5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x0	dis_collision_page_opt When this is set to '0', auto-precharge is disabled for the flushed command in a collision case. Collision cases are write followed by read to same address, read followed by write to same address, or write followed by write to same address with OPCTRL0.dis_wc bit = 1 (where same address comparisons exclude the two address bits representing critical word). FOR DEBUG ONLY. CAN ONLY BE SET TO 1. Value After Reset:0x0 Programming Mode:Static
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dis_wc When 1, disable write combine. FOR DEBUG ONLY Value After Reset:0x0 Programming Mode:Static

DDRCTL_OPCTRL1

Address: Operational Base + offset (0x10B84)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x0	dis_hif When 1, DDRCTL asserts the HIF command signal hif_cmd_stall. DDRCTL will ignore the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. Value After Reset:0x0 Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
0	RW	0x0	dis_dq When 1, DDRCTL will not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the DDRCTL, which makes it safe to modify certain register fields associated with reads and writes (see Programming Chapter for details). After setting this bit, it is strongly recommended to poll OPCTRLCAM.wr_data_pipeline_empty and OPCTRLCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This will ensure that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly. Note: This bit is not applicable for designs working in DDR5 mode. In DDR5 mode, use sofeware command interface command DisDqRef to achieve the same funtion as this bit. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_OPCTRLCAM
Address: Operational Base + offset (0x10B88)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved4 Reserved Field:Yes
29	RO	0x0	wr_data_pipeline_empty This bit indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. Value After Reset:0x0 Reset Mask:0x0 Volatile:true Programming Mode:Dynamic
28	RO	0x0	rd_data_pipeline_empty This bit indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting OPCTRL1.dis_dq, to ensure that all remaining commands/data have completed. Value After Reset:0x0 Reset Mask:0x0 Volatile:true Programming Mode:Dynamic
27	RW	0x0	Reserved3 Reserved Field:Yes

Bit	Attr	Reset Value	Description
26	RO	0x0	dbg_wr_q_empty When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. Value After Reset:0x0 Reset Mask:0x0 Volatile:true Programming Mode:Dynamic
25	RO	0x0	dbg_rd_q_empty When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters Self-Refresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. Value After Reset:0x0 Reset Mask:0x0 Volatile:true Programming Mode:Dynamic
24	RO	0x0	dbg_stall Stall FOR DEBUG ONLY Value After Reset:0x0 Programming Mode:Dynamic
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RO	0x00	dbg_w_q_depth Write queue depth The last entry of WR queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Value After Reset:0x0 Programming Mode:Dynamic
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RO	0x00	dbg_lpr_q_depth Low priority read queue depth The last entry of Lpr queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Value After Reset:0x0 Programming Mode:Dynamic
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RO	0x00	dbg_hpr_q_depth High priority read queue depth Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_OPCTRLCMD

Address: Operational Base + offset (0x10B8C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved1 Reserved Field:Yes
17	RW	0x0	ctrlupd Setting this register bit to 1 indicates to the DDRCTL to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Note: This field is not applicable for DDR5. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
16	RW	0x0	zq_calib_short Setting this register bit to 1 indicates to the DDRCTL to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the DDRCTL, the bit is automatically cleared. This operation can be performed only when ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init, in Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) or Deep Sleep Mode or Maximum Power Saving Mode. For Self-Refresh(except LPDDR4/5) or SR-Powerdown(LPDDR4/5) it will be scheduled after SR(except LPDDR4/5) or SRPD(LPDDR4/5) has been exited. For Deep Sleep Mode, it will be scheduled after DSM and/or SRPD has been exited. For Maximum Power Saving Mode, it will not be scheduled, although OPCTRLSTAT.zq_calib_short_busy will be de-asserted. Note: This field is not applicable for DDR5. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_OPCTRLSTAT

Address: Operational Base + offset (0x10B90)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved1 Reserved Field:Yes
17	RO	0x0	ctrlupd_busy SoC core may initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the DDRCTL. It is recommended not to perform ctrlupd operations when this signal is high. 0 - Indicates that the SoC core can initiate a ctrlupd operation 1 - Indicates that ctrlupd operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. Value After Reset:0x0 Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
16	RO	0x0	zq_calib_short_busy SoC core may initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the DDRCTL accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the DDRCTL. It is recommended not to perform ZQCS operations when this signal is high. 0 - Indicates that the SoC core can initiate a ZQCS operation 1 - Indicates that ZQCS operation has not been initiated yet in the DDRCTL Note: This field is not applicable for DDR5. Value After Reset:0x0 Programming Mode:Dynamic
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_OPCTRLCAM1
Address: Operational Base + offset (0x10B94)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved Field:Yes
5:0	RO	0x00	dbg_wrecc_q_depth Write ECC queue depth FOR DEBUG ONLY Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_OPREFCTRL0
Address: Operational Base + offset (0x10B98)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x0	rank1_refresh Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 1. Writing to this bit causes OPREFSTAT0.rank1_refresh_busy to be set. When OPREFSTAT0.rank1_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 1. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

Bit	Attr	Reset Value	Description
0	RW	0x0	rank0_refresh Setting this register bit to 1 indicates to the DDRCTL to issue a refresh to rank 0. Writing to this bit causes OPREFSTAT0.rank0_refresh_busy to be set. When OPREFSTAT0.rank0_refresh_busy is cleared, the command has been stored in the DDRCTL. For 3DS configuration, refresh is sent to logical rank index 0. This operation can be performed only when RFSHCTL0.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Maximum Power Saving Mode. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

DDRCTL_OPREFSTAT0

Address: Operational Base + offset (0x10BA0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RO	0x0	rank1_refresh_busy SoC core may initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the DDRCTL. It is recommended not to perform rank1_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank1_refresh operation 1 - Indicates that rank1_refresh operation has not been stored yet in the DDRCTL Value After Reset:0x0 Programming Mode:Dynamic
0	RO	0x0	rank0_refresh_busy SoC core may initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after OPREFCTRL0.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the DDRCTL. It is recommended not to perform rank0_refresh operations when this signal is high. - 0 - Indicates that the SoC core can initiate a rank0_refresh operation 1 - Indicates that rank0_refresh operation has not been stored yet in the DDRCTL Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SWCTL

Address: Operational Base + offset (0x10C80)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
0	RW	0x1	sw_done Enable quasi-dynamic register programming outside reset. Program register to 0 to enable quasi-dynamic programming. Set back register to 1 once programming is done. Value After Reset:0x1 Programming Mode:Dynamic

DDRCTL_SWSTAT
Address: Operational Base + offset (0x10C84)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x1	sw_done_ack Register programming done. This register is the echo of SWCTL.sw_done. Wait for sw_done value 1 to propagate to sw_done_ack at the end of the programming sequence to ensure that the correct registers values are propagated to the destination clock domains. Value After Reset:0x1 Programming Mode:Static

DDRCTL_RANKCTL
Address: Operational Base + offset (0x10C90)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved1 Reserved Field:Yes
15:12	RW	0x0	max_rank_wr Only present for multi-rank configurations. Background: Writes to the same rank can be performed back-to-back. Writes to different ranks require additional gap dictated by the register RANKCTL.diff_rank_wr_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_wr_gap register) in which only writes from the same rank are eligible to be scheduled. This prevents writes from other ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same rank. After this number is reached, - DDR4/LPDDR: a delay equal to RANKCTL.diff_rank_wr_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. - DDR5: writes to the same rank are blocked until read-write mode turn around or writes are issued to other ranks. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

Bit	Attr	Reset Value	Description
11:4	RW	0x00	Reserved0 Reserved Field:Yes
3:0	RW	0xf	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The DDRCTL arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, - DDR4/LPDDR: a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. - DDR5: reads to the same rank are blocked until read-write mode turn around or reads are issued to other ranks. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. FOR PERFORMANCE ONLY. Value After Reset:0xf Programming Mode:Static

DDRCTL_DBICTL

Address: Operational Base + offset (0x10C94)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2	RW	0x0	rd_dbi_en Read DBI enable signal in DDRC. 0 - Read DBI is disabled. 1 - Read DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A12. When x4 devices are used, this signal must be set to 0. DDR5: This signal must be set to 0. LPDDR4/LPDDR5: MR3[6]. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1

Bit	Attr	Reset Value	Description
1	RW	0x0	wr_dbi_en Write DBI enable signal in DDRC. 0 - Write DBI is disabled. 1 - Write DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A11. When x4 devices are used, this signal must be set to 0. DDR5: This signal must be set to 0. LPDDR4/LPDDR5: MR3[7]. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1
0	RW	0x1	dm_en DM enable signal in DDRC. 0 - DM is disabled. 1 - DM is enabled. This signal must be set the same logical value as DRAM's mode register. DDR4: Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0. DDR5: Set this to same value as MR5[5]. When x4 devices are used, this signal must be set to 0. LPDDR4/LPDDR5: Set this to inverted value of MR13[5] which is opposite polarity from this signal. Value After Reset:0x1 Volatile:true Programming Mode:Static

DDRCTL_ODTMAP

Address: Operational Base + offset (0x10C9C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved3 Reserved Field:Yes
13:12	RW	0x2	rank1_rd_odt Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks Value After Reset:0x2 Programming Mode:Static
11:10	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
9:8	RW	0x2	rank1_wr_odt Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks Value After Reset:0x2 Programming Mode:Static
7:6	RW	0x0	Reserved1 Reserved Field:Yes
5:4	RW	0x1	rank0_rd_odt Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Value After Reset:0x1 Programming Mode:Static
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1:0	RW	0x1	rank0_wr_odt Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Value After Reset:0x1 Programming Mode:Static

DDRCTL_DATACTL0

Address: Operational Base + offset (0x10CA0)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved1 Reserved Field:Yes
18	RW	0x0	wr_data_x_en Write Data X 1: Enable Write X 0: Write X This feature is not supported at present. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2

Bit	Attr	Reset Value	Description
17	RW	0x0	wr_data_copy_en Write Data Copy 1: Enable Write Data Copy X 0: Disable Write Data Copy X This feature is not supported at present. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2
16	RW	0x0	rd_data_copy_en Read Data Copy 1: Enable Read Data Copy X 0: Disable Read Data Copy X This feature is not supported at present. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_SWCTLSTATIC
Address: Operational Base + offset (0x10CA4)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	sw_static_unlock Enables static register programming outside reset. Program this register to 1 to enable static register programming. Set register back to 0 once programming is done. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_INITTMG0
Address: Operational Base + offset (0x10D00)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	skip_dram_init If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed 00 - SDRAM Initialization routine is run after power-up 01 - SDRAM Initialization routine is skipped after power-up. Controller starts up in Normal Mode 11 - SDRAM Initialization routine is skipped after power-up. Controller starts up in Self-refresh Mode 10 - Reserved. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2
29:26	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
25:16	RW	0x002	post_cke_x1024 Cycles to wait after driving CKE (CS in DDR5) high to start the SDRAM initialization sequence. DDR5: tINIT4 of 2 us (min) - simulation only. LPDDR4 typically requires this to be programmed for a delay of 2 us. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x2 Programming Mode:Static
15:13	RW	0x0	Reserved0 Reserved Field:Yes
12:0	RW	0x004e	pre_cke_x1024 Cycles to wait after reset before driving CKE (CS in DDR5) high to start the SDRAM initialization sequence. DDR5: tINIT3 of 4 ms (min) - simulation only. LPDDR4: tINIT3 of 2 ms (min) For DDR4 RDIMMs, this must include the time needed to satisfy tSTAB. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x4e Programming Mode:Static

DDRCTL_INITTMG1

Address: Operational Base + offset (0x10D04)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x000	dram_rstn_x1024 Number of cycles to assert SDRAM reset signal during init sequence. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Static
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_DDRCTL_VER_NUMBER

Address: Operational Base + offset (0x10FF8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3130312a	ver_number Indicates the Device Version Number value. This is in ASCII format, with each byte corresponding to a character of the version number Value After Reset:0x3130312a Programming Mode:Static

DDRCTL_DDRCTL_VER_TYPE
Address: Operational Base + offset (0x10FFC)

Bit	Attr	Reset Value	Description
31:0	RO	0x6c633031	ver_type Indicates the Device Version Type value. This is in ASCII format, with each byte corresponding to a character of the version type Value After Reset:0x6c633031 Programming Mode:Static

DDRCTL_PCCFG
Address: Operational Base + offset (0x20000)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	RW	0x0	pagematch_limit Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. Value After Reset:0x0 Programming Mode:Static
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	go2critical_en If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_PCFGR
Address: Operational Base + offset (0x20004)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved3 Reserved Field:Yes
23:20	RW	0x0	rrb_lock_threshold Specifies the RRB lock threshold in configurations that disable read data interleaving. Threshold is specified in terms of the HIF bursts that belong to the same AXI transaction. RRB locks onto VC only when this specified number of HIF bursts are returned by DDRC. RRB lock occurs earlier in cases where the axi transaction itself is shorter and the total number of corresponding HIF bursts are below the programmed threshold and all of them are returned by DDRC. When N is programmed in this field, the threshold will be set to N+1 bursts. Max thresholding is up to 16 bursts. Value After Reset:0x0 Programming Mode:Static
19:17	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
16	RW	0x0	rdwr_ordered_en Enable ordered read/writes. If set to 1, preserves the ordering between read transaction and write transaction issued to the same address, on a given port. In other words, the controller ensures that all same address read and write commands from the application port interface are transported to the DFI interface in the order of acceptance. This feature is useful in cases where software coherency is desired for masters issuing back-to-back read/write transactions without waiting for write/read responses. Note that this register has an effect only if necessary logic is instantiated via the UMCTL2_RDWR_ORDERED_n parameter. Value After Reset:0x0 Volatile:true Programming Mode:Static
15	RW	0x0	Reserved1 Reserved Field:Yes
14	RW	0x1	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. Value After Reset:0x1 Programming Mode:Static
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset:0x0 Programming Mode:Static
12	RW	0x1	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Value After Reset:0x1 Programming Mode:Static
11:10	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
9:0	RW	0x01f	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority (2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset:0x1f Programming Mode:Static

DDRCTL_PCFGW

Address: Operational Base + offset (0x20008)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. Value After Reset:0x1 Programming Mode:Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset:0x0 Programming Mode:Static
12	RW	0x1	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Value After Reset:0x1 Programming Mode:Static
11:10	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
9:0	RW	0x01f	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset:0x1f Programming Mode:Static

DDRCTL_PCTRL

Address: Operational Base + offset (0x20090)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	port_en Enables AXI port n. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_PCFGQOS0

Address: Operational Base + offset (0x20094)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved2 Reserved Field:Yes
21:20	RW	0x0	rqos_map_region1 This bitfield indicates the traffic class of region 1. Valid values are: 0 : LPR 1: VPR 2: HPR For dual address queue configurations, region1 maps to the blue address queue. In this case, valid values are 0: LPR 1: VPR only When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region 1 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
19:18	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
17:16	RW	0x0	rqos_map_region0 This bitfield indicates the traffic class of region 0. Valid values are: 0: LPR 1: VPR 2: HPR For dual address queue configurations, region 0 maps to the blue address queue. In this case, valid values are: 0: LPR and 1: VPR only. When VPR support is disabled (UMCTL2_VPR_EN = 0) and traffic class of region0 is set to 1 (VPR), VPR traffic is aliased to LPR traffic. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
15:4	RW	0x000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	rqos_map_level1 Separation level1 indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 (for dual RAQ) or 0 to 14 (for single RAQ) which corresponds to arqos. Note that for PA, arqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PCFGQOS1

Address: Operational Base + offset (0x20098)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RW	0x0	rqos_map_timeoutr Specifies the timeout value for transactions mapped to the red address queue. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
15:1	RW	0x0000	Reserved0 Reserved Field:Yes
0	RW	0x0	rqos_map_timeoutb Specifies the timeout value for transactions mapped to the blue address queue. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PCFGWQOS0

Address: Operational Base + offset (0x2009C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved4 Reserved Field:Yes

Bit	Attr	Reset Value	Description
25:24	RW	0x0	wqos_map_region2 This bit field indicates the traffic class of region 2. Valid values are: 0: NPW, 1: VPW. When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 2 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
23:22	RW	0x0	Reserved3 Reserved Field:Yes
21:20	RW	0x0	wqos_map_region1 This bit field indicates the traffic class of region 1. Valid values are: 0: NPW, 1: VPW. When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 1 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
19:18	RW	0x0	Reserved2 Reserved Field:Yes
17:16	RW	0x0	wqos_map_region0 This bit field indicates the traffic class of region 0. Valid values are: 0: NPW, 1: VPW. When VPW support is disabled (UMCTL2_VPW_EN = 0) and traffic class of region 0 is set to 1 (VPW), VPW traffic is aliased to NPW traffic. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
15:12	RW	0x0	Reserved1 Reserved Field:Yes
11:8	RW	0xe	wqos_map_level2 Separation level2 indicating the end of region1 mapping; start of region1 is (level1 + 1). Possible values for level2 are (level1 + 1) to 14 which corresponds to awqos. Region2 starts from (level2 + 1) up to 15. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset:0xe Volatile:true Programming Mode:Quasi-dynamic Group 3
7:4	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
3:0	RW	0x0	wqos_map_level1 Separation level indicating the end of region0 mapping; start of region0 is 0. Possible values for level1 are 0 to 13 which corresponds to awqos. Note that for PA, awqos values are used directly as port priorities, where the higher the value corresponds to higher port priority. All of the map_level* registers must be set to distinct values. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PCFGWQOS1
Address: Operational Base + offset (0x200A0)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RW	0x0	wqos_map_timeout2 Specifies the timeout value for write transactions in region 2. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3
15:1	RW	0x0000	Reserved0 Reserved Field:Yes
0	RW	0x0	wqos_map_timeout1 Specifies the timeout value for write transactions in region 0 and 1. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_SBRCTL
Address: Operational Base + offset (0x200E0)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved4 Reserved Field:Yes

Bit	Attr	Reset Value	Description
30:28	RW	0x1	scrub_burst_length_lp Scrub burst length in Low Power mode - Determines the number of back-to-back scrub read commands that can be issued together when the controller is in one of the HW controlled low power modes with Sideband ECC and Inline ECC. - During these modes, the period of the scrub burst becomes "scrub_burst_length_lp*scrub_interval" cycles. Valid values are (Sideband ECC): 1: 1 read, 2: 4 reads, 3: 16 reads, 4: 64 reads, 5: 256 reads, 6: 1024 reads. (Inline ECC): 1: 8 reads, 2: 16 reads, 3: 32 reads. To program a new value to this register field, first disable Scrubber by setting SBRCTL.scrub_en = 0. Program the new value.Enable Scrubber by setting SBRCTL.scrub_en = 1. Value After Reset:0x1 Programming Mode:Dynamic
27:26	RW	0x0	Reserved3 Reserved Field:Yes
25:24	RW	0x0	scrub_cmd_type This field determines the kind of traffic scrubber must generate. 00: Read - Only periodic reads will be generated 01: Write - Only back to back initialization writes will be generated. SBRCTL.scrub_interval must be programmed to 0. 10: Read Modify Write - only periodic RMWs will be generated.Periodic RMW transactions are currently supported only if Debug DFI Sideband Signals are enabled in the configuration. 11: reserved. Value After Reset:0x0 Programming Mode:Dynamic
23:21	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20:8	RW	0x00ff	scrub_interval Scrub interval. (N x scrub_interval) number of clock cycles between two scrub read commands, where N is the granularity. If set to 0, scrub commands are issued back-to-back. This mode of operation (scrub_interval=0) can typically be used for scrubbing the full range of memory at once before or after SW controlled low power operations. After completing the full range of scrub while scrub_interval=0, scrub_done register is set and sbr_done_intr interrupt signal is asserted. This mode can't be used with Inline ECC: If MEMC_INLINE_ECC is 1 and scrub_interval is programme to 0, then RMW logic inside scrubber is disabled. New programmed value will take effect only after scrubber is disabled by programming scrub_en to 0. Unit: Multiples of 256 sbr_clk cycles in Sideband ECC configurations and 512 sbr_clk cycles in Inline ECC Configurations. Value After Reset:0xff Programming Mode:Dynamic
7	RW	0x0	Reserved1 Reserved Field:Yes
6:4	RW	0x1	scrub_burst_length_nm Scrub burst length in normal mode. - Determines the number of back-to-back scrub read commands that can be issued together when the controller is in normal operation in Inline ECC & Sideband ECC. - The period of the scrub burst becomes "scrub_burst_length_nm*scrub_interval" cycles. During normal operation mode of the controller with Sideband ECC (not in power-down or self refresh), scrub_burst_length_nm is ignored and only one scrub command is generated. Valid values are (Sideband ECC): 1: 1 read (Inline ECC): 1: 8 reads, 2: 16 reads, 3: 32 reads. In Sideband ECC, software must ensure that the scrub_burst_length_nm is programmed to the value of 1. Other values are not supported. To program a new value to this register field, first disable Scrubber by setting SBRCTL.scrub_en = 0. Program the new value.Enable Scrubber by setting SBRCTL.scrub_en = 1. Value After Reset:0x1 Programming Mode:Dynamic
3:2	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
1	RW	0x0	scrub_during_lowpower Continue scrubbing during low power. If set to 1, burst of scrubs will be issued in HW controlled low power modes. There are two such modes: automatically initiated by idleness or initiated by Hardware low power interface. If set to 0, the scrubber will not attempt to send commands while the DDRC is in HW controlled low power modes. In this case, the scrubber will remember the last address issued and will automatically continue from there when the DDRC exits the LP mode. Value After Reset:0x0 Programming Mode:Dynamic
0	RW	0x0	scrub_en Enable ECC scrubber. If set to 1, enables the scrubber to generate background read commands after the memories are initialized. If set to 0, disables the scrubber, resets the address generator to 0 and clears the scrubber status. This bit field must be accessed separately from the other bitfields in this register. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SBRSTAT

Address: Operational Base + offset (0x200E4)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RO	0x0	scrub_done Scrubber done. Controller sets this bit to 1, after full range of addresses are scrubbed once while scrub_interval is set to 0. Cleared if scrub_en is set to 0 (scrubber disabled) or scrub_interval is set to a non-zero value for normal scrub operation. The interrupt signal, sbr_done_intr, is equivalent to this status bitfield. Value After Reset:0x0 Programming Mode:Dynamic
0	RO	0x0	scrub_busy Scrubber busy. Controller sets this bit to 1 when the scrubber logic has outstanding read commands being executed. Cleared when there are no active outstanding scrub reads in the system. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SBRWDATA0

Address: Operational Base + offset (0x200E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	scrub_pattern0 ECC Scrubber write data pattern for data bus[31:0] Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SBRSTART0

Address: Operational Base + offset (0x200F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbr_address_start_mask_0 sbr_address_start_mask_0 holds the bits [31:0] of the starting address the ECC scrubber generates. The register must be programmed as explained in Address Configuration in ECC Scrub and Scrubber. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SBRSTART1

Address: Operational Base + offset (0x200F4)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	sbr_address_start_mask_1 sbr_address_start_mask_1 holds bits [MEMC_HIF_ADDR_WIDTH_MAX-1:32] of the starting address the ECC scrubber generates.The register must be programmed as explained in Address Configuration in ECC Scrub and Scrubber. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SBRRANGE0

Address: Operational Base + offset (0x200F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbr_address_range_mask_0 sbr_address_range_mask_0 holds the bits [31:0] of the scrubber address range mask. The scrubber address range mask limits the address range that the ECC scrubber can generate.The register must be programmed as explained in Address Configuration in ECC Scrub and Scrubber. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SBRRANGE1

Address: Operational Base + offset (0x200FC)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7:0	RW	0x00	sbr_address_range_mask_1 sbr_address_range_mask_1 holds the bits [MEMC_HIF_ADDR_WIDTH_MAX-1:32] of the scrubber address range mask. The scrubber address range mask limits the address range that the ECC scrubber can generate.The register must be programmed as explained in Address Configuration in ECC Scrub and Scrubber. The scrubber address registers are changed only when the scrubber is disabled (SBRCTL.scrub_en = 0) and there are no scrubber commands in progress (SBRSTAT.scrub_busy = 0). Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_PSTAT

Address: Operational Base + offset (0x20114)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RO	0x0	wr_port_busy_0 Indicates if there are outstanding writes for AXI/CHI port 0. Value After Reset:0x0 Programming Mode:Dynamic
15:1	RW	0x0000	Reserved0 Reserved Field:Yes
0	RO	0x0	rd_port_busy_0 Indicates if there are outstanding reads for AXI/CHI port 0. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_ADDRMAP1

Address: Operational Base + offset (0x30004)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved Field:Yes
5:0	RW	0x00	addrmap_cs_bit0 Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 33, and 63 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then rank address bit 0 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP3

Address: Operational Base + offset (0x3000C)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x00	addrmap_bank_b2 Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 34, and 63 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Value After Reset:0x0 Programming Mode:Static
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x00	addrmap_bank_b1 Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 35, and 63 Internal Base: 4 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Value After Reset:0x0 Programming Mode:Static
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x00	addrmap_bank_b0 Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 36, and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP4

Address: Operational Base + offset (0x30010)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved1 Reserved Field:Yes
13:8	RW	0x00	addrmap_bg_b1 Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 35, and 63 Internal Base: 4 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. Value After Reset:0x0 Programming Mode:Static
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x00	addrmap_bg_b0 Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 36, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP5

Address: Operational Base + offset (0x30014)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x00	addrmap_col_b10 Selects the HIF address bit used as column address bit 10. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 10 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 10 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 10 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
23:21	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20:16	RW	0x00	addrmap_col_b9 Selects the HIF address bit used as column address bit 9. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 9 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 9 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 9 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x00	addrmap_col_b8 Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 8 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 8 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x00	addrmap_col_b7 Selects the HIF address bit used as column address bit 7. Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 7 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP6

Address: Operational Base + offset (0x30018)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x0	addrmap_col_b6 Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, x and 15. x indicates a valid value in the inline ECC configuration. Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x0	addrmap_col_b5 Selects the HIF address bit used as column address bit 5. Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
15:12	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_col_b4 Full bus width mode: Selects the HIF address bit used as column address bit 4. Half bus width mode: Selects the HIF address bit used as column address bit 5. Quarter bus width mode: Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RW	0x0	addrmap_col_b3 Selects the HIF address bit used as column address bit 3. Valid Range: 0 to 7. Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. Note : In LPDDR4/5 or DDR5, it is required to program this to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP7

Address: Operational Base + offset (0x3001C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x00	addrmap_row_b17 Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 16, and 31 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 17 is set to 0. Value After Reset:0x0 Programming Mode:Static
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x00	addrmap_row_b16 Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 16, and 31 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 16 is set to 0. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x00	addrmap_row_b15 Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 16, and 31 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 15 is set to 0. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x00	addrmap_row_b14 Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 16, and 31 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 14 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP8

Address: Operational Base + offset (0x30020)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x00	addrmap_row_b13 Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 16, and 31 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 13 is set to 0. Value After Reset:0x0 Programming Mode:Static
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x00	addrmap_row_b12 Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 16, and 31 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then row address bit 12 is set to 0. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x00	addrmap_row_b11 Selects the HIF address bit used as row address bit 11. Valid Range: 0 to 16 Internal Base: 17 The selected HIF address bit is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x00	addrmap_row_b10 Selects the HIF address bits used as row address bit 10. Valid Range: 0 to 16 Internal Base: 16 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP9

Address: Operational Base + offset (0x30024)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x00	addrmap_row_b9 Selects the HIF address bits used as row address bit 9. Valid Range: 0 to 16 Internal Base: 15 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x00	addrmap_row_b8 Selects the HIF address bits used as row address bit 8. Valid Range: 0 to 16 Internal Base: 14 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x00	addrmap_row_b7 Selects the HIF address bits used as row address bit 7. Valid Range: 0 to 16 Internal Base: 13 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x00	addrmap_row_b6 Selects the HIF address bits used as row address bit 6. Valid Range: 0 to 16 Internal Base: 12 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP10

Address: Operational Base + offset (0x30028)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x00	addrmap_row_b5 Selects the HIF address bits used as row address bit 5. Valid Range: 0 to 16 Internal Base: 11 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x00	addrmap_row_b4 Selects the HIF address bits used as row address bit 4. Valid Range: 0 to 16 Internal Base: 10 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x00	addrmap_row_b3 Selects the HIF address bits used as row address bit 3. Valid Range: 0 to 16 Internal Base: 9 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x00	addrmap_row_b2 Selects the HIF address bits used as row address bit 2. Valid Range: 0 to 16 Internal Base: 8 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP11

Address: Operational Base + offset (0x3002C)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12:8	RW	0x00	addrmap_row_b1 Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 16 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x00	addrmap_row_b0 Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 16 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP12

Address: Operational Base + offset (0x30030)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2:0	RW	0x0	nonbinary_device_density Indicates what type of SDRAM device is in use. 3'b000: All addresses are valid 3'b001: Every address having row[13:12]==2'b11 is considered as invalid 3'b010: Every address having row[14:13]==2'b11 is considered as invalid 3'b011: Every address having row[15:14]==2'b11 is considered as invalid 3'b100: Every address having row[16:15]==2'b11 is considered as invalid 3'b101: Every address having row[17:16]==2'b11 is considered as invalid Value After Reset:0x0 Programming Mode:Static

DDRCTL_DRAMSET1TMG0_FREQ1

Address: Operational Base + offset (0x100000)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. For DDR5, add one extra cycle when CRCPARCTL1.wr_crc_enable = 1. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset:0x1b Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ1

Address: Operational Base + offset (0x100004)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. DDR4 (C/A parity not enabled): tXP DDR4 (C/A parity enabled): (tXP+PL) DDR5: tXP DDR5 RDIMM: max (tXP, tRPDX) LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. DDR4: Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). DDR5: tRTP LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ1

Address: Operational Base + offset (0x100008)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved Field:Yes
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
23	RW	0x0	Reserved0 Reserved Field:Yes
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. In addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x06	rd2wr DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL DDR5: CL - CWL + BL/2 + 2 - (Read DQS offset) + (RD_POSTAMBLE-0.5) + WR_PREAMBLE LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR4, if derating is enabled (DERATECTL0.derate_enable=1), derated tDQSCKmax must be used. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0d	wr2rd DDR4: CWL + PL + BL/2 + tWTR_L DDR5: CWL + BL/2 + tWTR_L LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) In DDR4, minimum time from write command to read command for same bank group. In others, minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ1

Address: Operational Base + offset (0x10000C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command DDR4: Set this to the larger of tMOD + AL and tMRD. If C/A parity is enabled, tMOD_PAR(tMOD+PL) + AL and tMRD_PAR(tMOD+PL) and used instead. If CAL mode is enabled, tCAL must be added to the above. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using LRDIMM, the minimum value of this register is tMRD_L2. DDR5: Set this to the larger of tMRR, tMRW, tMRWPD, tMRD and tMPC_DELAY. LPDDR4:Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5:Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ1

Address: Operational Base + offset (0x100010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Note: For DDR5, it is recommended to set this value as multiple of MEMC_FREQ_RATIO to improve the performance. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. DDR4: tCCD_L LPDDR4: tCCD LPDDR5: BL/n Don't Care for DDR5 (see DRAMSET1TMG26.t_ccd_r/t_ccd_w in DDR5). Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_rrd For DDR4/DDR5/LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". DDR4/5: tRRD_L LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ1

Address: Operational Base + offset (0x100014)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH DDR4: tCKSRX DDR5: tCKSRX Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

Bit	Attr	Reset Value	Description
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK DDR4: tCKSRE (+ PL(parity latency)(*)) DDR5: tCKLCS (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: max(tCKE, tSR) LPDDR5: tSR DDR4: tCKESR (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD DDR4: tPD (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG6_FREQ1

Address: Operational Base + offset (0x100018)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ1
Address: Operational Base + offset (0x10001C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ1
Address: Operational Base + offset (0x100020)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x44 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG9_FREQ1
Address: Operational Base + offset (0x100024)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved1 Reserved Field:Yes
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting DDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting DDR4/DDR5/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support DDR SDRAM memories or LPDDR5 SDRAM memories. DDR4/DDR5 designs: CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Where: CWL = CAS write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. WTR_S must be increased by one if DDR4 2tCK write preamble is used. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ1

Address: Operational Base + offset (0x100030)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: max(tESCKE, tCMDCKE) LPDDR5: max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_DRAMSET1TMG13_FREQ1

Address: Operational Base + offset (0x100034)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x1c Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved1 Reserved Field:Yes
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x20 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes
3:0	RW	0x4	t_ppd LPDDR4/5 and DDR5: tPPD: This is the minimum time from precharge to precharge command. Note: This register is not applicable for DDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ1

Address: Operational Base + offset (0x100038)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset:0xa0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ1

Address: Operational Base + offset (0x10005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ1

Address: Operational Base + offset (0x100060)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 00: 4 Banks/ 4 Bank groups 01: 8 Banks (Reserved) 10: 16 Banks 11: Reserved Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ1
Address: Operational Base + offset (0x100064)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved Field:Yes
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 DDR4: WL + BL/2 + WR Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP DDR4: RTP Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ1

Address: Operational Base + offset (0x100078)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ1

Address: Operational Base + offset (0x100500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR4: Value loaded into MR0 register. DDR5: Don't care LPDDR4: Value to write to MR1 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

Bit	Attr	Reset Value	Description
15:0	RW	0x0510	emr DDR4: Value to write to MR1 register Set bit 7 to 0. DDR5: Don't care LPDDR4 - Value to write to MR2 register Value After Reset:0x510 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ1

Address: Operational Base + offset (0x100504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR4: Value to write to MR2 register DDR5: Don't care LPDDR4: Value to write to MR3 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR4: Value to write to MR3 register DDR5: Don't care LPDDR4: Value to write to MR13 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ1

Address: Operational Base + offset (0x100508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4: Value to be loaded into SDRAM MR4 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4: Value to be loaded into SDRAM MR5 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ1

Address: Operational Base + offset (0x10050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 DDR4 Value to be loaded into SDRAM MR6 registers. DDR5: Don't care LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ1

Address: Operational Base + offset (0x100580)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Volatile:true Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value.Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG1_FREQ1

Address: Operational Base + offset (0x100584)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When TMGCFG.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When TMGCFG.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ1

Address: Operational Base + offset (0x100588)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved2 Reserved Field:Yes
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on th DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ1
Address: Operational Base + offset (0x100590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ1
Address: Operational Base + offset (0x100594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFIUPDTMG1_FREQ1

Address: Operational Base + offset (0x1005AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static
15:8	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static

DDRCTL_RFSHSET1TMG0_FREQ1

Address: Operational Base + offset (0x100600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used, 1 - x1 register values are used. This applies only when per-bank refresh is enabled (RFSHMOD0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32 * 32 if RFSHSET1TMG0.t_refi_x1_sel = 0. If RFSHSET1TMG0.t_refi_x1_sel = 1, internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related
23:22	RW	0x0	Reserved1 Reserved Field:Yes
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this RFSHSET1TMG0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) or DDR5 same-bank refresh (REFsb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. For non-DDR5, this should be programmed to tREFI based value in controller's current refresh mode. For DDR5, this should be always programmed to tREFI1 based value even in FGR mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR4, 3.9us for DDR5. See JEDEC specification for LPDDR4). set this register to RoundDown(tREFI/tCK) if RFSHSET1TMG0.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: if using all-bank refreshes (RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations if using per-bank refreshes (RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations For DDR controller, tREFI value is different depending on FGR mode. In DDR4 mode, if using FGR 1x mode (RFSHMOD1.fgr_mode = 000), use tREFI1 in the above calculations In DDR4 mode, if using FGR 2x mode (RFSHMOD1.fgr_mode = 001), use tREFI2 in the above calculations In DDR4 mode, if using FGR 4x mode (RFSHMOD1.fgr_mode = 010), use tREFI4 in the above calculations In DDR5 mode, always use tREFI1 in the above calculations Note that: RFSHSET1TMG0.t_refi_x1_x32 must be greater than 0x1. if RFSHSET1TMG0.t_refi_x1_sel == 1, RFSHSET1TMG0.t_refi_x1_x32 must be greater than RFSHSET1TMG1.t_rfc_min if RFSHSET1TMG0.t_refi_x1_sel == 0, RFSHSET1TMG0.t_refi_x1_x32 * 32 must be greater than RFSHSET1TMG1.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0xFFE. In DDR4 Fixed 2x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x7FF. In DDR4 Fixed 4x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x3FF. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ1

Address: Operational Base + offset (0x100604)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller: if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4/DDR5 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user must program the appropriate value from the spec based on the 'fgr_mode' and the device density that is used. Unit: DRAM clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ1

Address: Operational Base + offset (0x100608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (RFSHMOD0.per_bank_refresh == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_RFSHSET1TMG4_FREQ1

Address: Operational Base + offset (0x100610)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ1

Address: Operational Base + offset (0x100800)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	t_zq_short_nop tZQCS for DD4, tZQLAT for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x40 Programming Mode:Static
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:0	RW	0x0200	t_zq_long_nop tZQoper for DDR4, tZQCAL for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset:0x200 Programming Mode:Static

DDRCTL_ZQSET1TMG1_FREQ1

Address: Operational Base + offset (0x100804)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x20 Programming Mode:Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR4/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x100 Programming Mode:Static

DDRCTL_DQSOSCCTL0_FREQ1
Address: Operational Base + offset (0x100A80)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved2 Reserved Field:Yes
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset:0x7 Programming Mode:Dynamic
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval.The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1: x2K DFI clock cycles 0: x32K DFI clock cycles Value After Reset:0x0 Programming Mode:Dynamic
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1: Enable DQS Oscillator 0: Disable DQS Oscillator Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATEINT_FREQ1
Address: Operational Base + offset (0x100B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset:0x800000 Volatile:true Programming Mode:Static

DDRCTL_DERATEVAL0_FREQ1
Address: Operational Base + offset (0x100B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ1
Address: Operational Base + offset (0x100B08)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ1
Address: Operational Base + offset (0x100B80)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Volatile:true Programming Mode:Static
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_SCHEDTMG0_FREQ1
Address: Operational Base + offset (0x100C00)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static
7:0	RW	0x00	pageclose_timer This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_PERFHPR1_FREQ1

Address: Operational Base + offset (0x100C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ1

Address: Operational Base + offset (0x100C84)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFWR1_FREQ1

Address: Operational Base + offset (0x100C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ1

Address: Operational Base + offset (0x100D00)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved1 Reserved Field:Yes
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset:0x0 Programming Mode:Dynamic
7:1	RW	0x00	Reserved0 Reserved Field:Yes
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For DDR4/DDR5/LPDDR4: 0: 1:2 Mode 1: 1:4 Mode For LPDDR5: 0: 1:1:2 Mode 1: 1:1:4 Mode Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ1

Address: Operational Base + offset (0x100D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. If write preamble is set to 2tCK(DDR4 only), must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

Bit	Attr	Reset Value	Description
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TRDRD timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ1

Address: Operational Base + offset (0x100D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ1

Address: Operational Base + offset (0x100D0C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x40 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:7	RW	0x000	Reserved0 Reserved Field:Yes
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DRAMSET1TMG0_FREQ2

Address: Operational Base + offset (0x200000)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. For DDR5, add one extra cycle when CRCPARCTL1.wr_crc_enable = 1. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset:0x1b Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ2

Address: Operational Base + offset (0x200004)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. DDR4 (C/A parity not enabled): tXP DDR4 (C/A parity enabled): (tXP+PL) DDR5: tXP DDR5 RDIMM: max (tXP, tRPDX) LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. DDR4: Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). DDR5: tRTP LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ2

Address: Operational Base + offset (0x200008)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved Field:Yes
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
23	RW	0x0	Reserved0 Reserved Field:Yes
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. In addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x06	rd2wr DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL DDR5: CL - CWL + BL/2 + 2 - (Read DQS offset) + (RD_POSTAMBLE-0.5) + WR_PREAMBLE LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR4, if derating is enabled (DERATECTL0.derate_enable=1), derated tDQSCKmax must be used. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0d	wr2rd DDR4: CWL + PL + BL/2 + tWTR_L DDR5: CWL + BL/2 + tWTR_L LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) In DDR4, minimum time from write command to read command for same bank group. In others, minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ2

Address: Operational Base + offset (0x20000C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command DDR4: Set this to the larger of tMOD + AL and tMRD. If C/A parity is enabled, tMOD_PAR(tMOD+PL) + AL and tMRD_PAR(tMOD+PL) and used instead. If CAL mode is enabled, tCAL must be added to the above. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using LRDIMM, the minimum value of this register is tMRD_L2. DDR5: Set this to the larger of tMRR, tMRW, tMRWPD, tMRD and tMPC_DELAY. LPDDR4:Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5:Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ2

Address: Operational Base + offset (0x200010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Note: For DDR5, it is recommended to set this value as multiple of MEMC_FREQ_RATIO to improve the performance. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. DDR4: tCCD_L LPDDR4: tCCD LPDDR5: BL/n Don't Care for DDR5 (see DRAMSET1TMG26.t_ccd_r/t_ccd_w in DDR5). Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_rrd For DDR4/DDR5/LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". DDR4/5: tRRD_L LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ2

Address: Operational Base + offset (0x200014)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH DDR4: tCKSRX DDR5: tCKSRX Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

Bit	Attr	Reset Value	Description
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK DDR4: tCKSRE (+ PL(parity latency)(*)) DDR5: tCKLCS (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: max(tCKE, tSR) LPDDR5: tSR DDR4: tCKESR (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD DDR4: tPD (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG6_FREQ2

Address: Operational Base + offset (0x200018)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ2

Address: Operational Base + offset (0x20001C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ2

Address: Operational Base + offset (0x200020)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x44 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG9_FREQ2

Address: Operational Base + offset (0x200024)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved1 Reserved Field:Yes
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting DDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting DDR4/DDR5/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support DDR SDRAM memories or LPDDR5 SDRAM memories. DDR4/DDR5 designs: CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Where: CWL = CAS write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. WTR_S must be increased by one if DDR4 2tCK write preamble is used. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ2

Address: Operational Base + offset (0x200030)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: max(tESCKE, tCMDCKE) LPDDR5: max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_DRAMSET1TMG13_FREQ2
Address: Operational Base + offset (0x200034)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x1c Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved1 Reserved Field:Yes
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x20 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes
3:0	RW	0x4	t_ppd LPDDR4/5 and DDR5: tPPD: This is the minimum time from precharge to precharge command. Note: This register is not applicable for DDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ2
Address: Operational Base + offset (0x200038)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset:0xa0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ2

Address: Operational Base + offset (0x20005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ2

Address: Operational Base + offset (0x200060)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 00: 4 Banks/ 4 Bank groups 01: 8 Banks (Reserved) 10: 16 Banks 11: Reserved Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ2

Address: Operational Base + offset (0x200064)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved Field:Yes
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 DDR4: WL + BL/2 + WR Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP DDR4: RTP Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ2

Address: Operational Base + offset (0x200078)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ2

Address: Operational Base + offset (0x200500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR4: Value loaded into MR0 register. DDR5: Don't care LPDDR4: Value to write to MR1 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

Bit	Attr	Reset Value	Description
15:0	RW	0x0510	emr DDR4: Value to write to MR1 register Set bit 7 to 0. DDR5: Don't care LPDDR4 - Value to write to MR2 register Value After Reset:0x510 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ2
Address: Operational Base + offset (0x200504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR4: Value to write to MR2 register DDR5: Don't care LPDDR4: Value to write to MR3 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR4: Value to write to MR3 register DDR5: Don't care LPDDR4: Value to write to MR13 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ2
Address: Operational Base + offset (0x200508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4: Value to be loaded into SDRAM MR4 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4: Value to be loaded into SDRAM MR5 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ2
Address: Operational Base + offset (0x20050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 DDR4 Value to be loaded into SDRAM MR6 registers. DDR5: Don't care LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ2

Address: Operational Base + offset (0x200580)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Volatile:true Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value.Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG1_FREQ2

Address: Operational Base + offset (0x200584)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When TMGCFG.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When TMGCFG.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ2

Address: Operational Base + offset (0x200588)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved2 Reserved Field:Yes
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on th DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ2
Address: Operational Base + offset (0x200590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ2
Address: Operational Base + offset (0x200594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFIUPDTMG1_FREQ2

Address: Operational Base + offset (0x2005AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static
15:8	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static

DDRCTL_RFSHSET1TMG0_FREQ2
Address: Operational Base + offset (0x200600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used, 1 - x1 register values are used. This applies only when per-bank refresh is enabled (RFSHMOD0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32 * 32 if RFSHSET1TMG0.t_refi_x1_sel = 0. If RFSHSET1TMG0.t_refi_x1_sel = 1, internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related
23:22	RW	0x0	Reserved1 Reserved Field:Yes
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this RFSHSET1TMG0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) or DDR5 same-bank refresh (REFsb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. For non-DDR5, this should be programmed to tREFI based value in controller's current refresh mode. For DDR5, this should be always programmed to tREFI1 based value even in FGR mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR4, 3.9us for DDR5. See JEDEC specification for LPDDR4). set this register to RoundDown(tREFI/tCK) if RFSHSET1TMG0.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: if using all-bank refreshes (RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations if using per-bank refreshes (RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations For DDR controller, tREFI value is different depending on FGR mode. In DDR4 mode, if using FGR 1x mode (RFSHMOD1.fgr_mode = 000), use tREFI1 in the above calculations In DDR4 mode, if using FGR 2x mode (RFSHMOD1.fgr_mode = 001), use tREFI2 in the above calculations In DDR4 mode, if using FGR 4x mode (RFSHMOD1.fgr_mode = 010), use tREFI4 in the above calculations In DDR5 mode, always use tREFI1 in the above calculations Note that: RFSHSET1TMG0.t_refi_x1_x32 must be greater than 0x1. if RFSHSET1TMG0.t_refi_x1_sel == 1, RFSHSET1TMG0.t_refi_x1_x32 must be greater than RFSHSET1TMG1.t_rfc_min if RFSHSET1TMG0.t_refi_x1_sel == 0, RFSHSET1TMG0.t_refi_x1_x32 * 32 must be greater than RFSHSET1TMG1.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0xFFE. In DDR4 Fixed 2x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x7FF. In DDR4 Fixed 4x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x3FF. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ2

Address: Operational Base + offset (0x200604)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller: if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4/DDR5 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user must program the appropriate value from the spec based on the 'fgr_mode' and the device density that is used. Unit: DRAM clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ2
Address: Operational Base + offset (0x200608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (RFSHMOD0.per_bank_refresh == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_RFSHSET1TMG4_FREQ2
Address: Operational Base + offset (0x200610)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ2
Address: Operational Base + offset (0x200800)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	t_zq_short_nop tZQCS for DD4, tZQLAT for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x40 Programming Mode:Static
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:0	RW	0x0200	t_zq_long_nop tZQoper for DDR4, tZQCAL for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset:0x200 Programming Mode:Static

DDRCTL_ZQSET1TMG1_FREQ2
Address: Operational Base + offset (0x200804)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x20 Programming Mode:Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR4/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x100 Programming Mode:Static

DDRCTL_DQSOSCCTL0_FREQ2
Address: Operational Base + offset (0x200A80)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved2 Reserved Field:Yes
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset:0x7 Programming Mode:Dynamic
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval.The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1: x2K DFI clock cycles 0: x32K DFI clock cycles Value After Reset:0x0 Programming Mode:Dynamic
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1: Enable DQS Oscillator 0: Disable DQS Oscillator Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATEINT_FREQ2
Address: Operational Base + offset (0x200B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset:0x800000 Volatile:true Programming Mode:Static

DDRCTL_DERATEVAL0_FREQ2

Address: Operational Base + offset (0x200B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ2
Address: Operational Base + offset (0x200B08)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ2
Address: Operational Base + offset (0x200B80)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Volatile:true Programming Mode:Static
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_SCHEDTMG0_FREQ2
Address: Operational Base + offset (0x200C00)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static
7:0	RW	0x00	pageclose_timer This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_PERFHPR1_FREQ2

Address: Operational Base + offset (0x200C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ2

Address: Operational Base + offset (0x200C84)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFWR1_FREQ2

Address: Operational Base + offset (0x200C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ2

Address: Operational Base + offset (0x200D00)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved1 Reserved Field:Yes
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset:0x0 Programming Mode:Dynamic
7:1	RW	0x00	Reserved0 Reserved Field:Yes
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For DDR4/DDR5/LPDDR4: 0: 1:2 Mode 1: 1:4 Mode For LPDDR5: 0: 1:1:2 Mode 1: 1:1:4 Mode Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ2

Address: Operational Base + offset (0x200D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. If write preamble is set to 2tCK(DDR4 only), must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

Bit	Attr	Reset Value	Description
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TRDRD timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ2

Address: Operational Base + offset (0x200D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ2
Address: Operational Base + offset (0x200D0C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x40 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:7	RW	0x000	Reserved0 Reserved Field:Yes
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DRAMSET1TMG0_FREQ3
Address: Operational Base + offset (0x300000)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR4/5 for this parameter. For DDR5, add one extra cycle when CRCPARCTL1.wr_crc_enable = 1. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x10	t_faw tFAW: At most 4 banks must be activated in a rolling window of tFAW cycles. Unit: DRAM clock cycles. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). Unit: 1024 DRAM clock cycles. Value After Reset:0x1b Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG1_FREQ3

Address: Operational Base + offset (0x300004)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. DDR4 (C/A parity not enabled): tXP DDR4 (C/A parity enabled): (tXP+PL) DDR5: tXP DDR5 RDIMM: max (tXP, tRPDX) LPDDR4 (tCKELPD is defined in spec): larger of tXP and tCKELPD instead. LPDDR4 (tCKELPD is not defined in spec): tXP. LPDDR5: tXP + tCSH Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. DDR4: Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). DDR5: tRTP LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 LPDDR5(BG mode): BL/n_min + RU(tRBTP/tCK) LPDDR5(16B mode): BL/n + RU(tRBTP/tCK) (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. Unit: DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG2_FREQ3

Address: Operational Base + offset (0x300008)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved Field:Yes
30:24	RW	0x03	write_latency Set to WL Time from write command to write data on SDRAM interface. This must be set to WL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
23	RW	0x0	Reserved0 Reserved Field:Yes
22:16	RW	0x05	read_latency Set to RL Time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. In addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x06	rd2wr DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL DDR5: CL - CWL + BL/2 + 2 - (Read DQS offset) + (RD_POSTAMBLE-0.5) + WR_PREAMBLE LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (BG mode && DQ ODT is Disabled): RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (BG mode && DQ ODT is Enabled) : RL + BL/n_max + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 LPDDR5 (16B mode && DQ ODT is Disabled): RL + BL/n + RU(tWCKDQO(max)/tCK) - WL LPDDR5 (16B mode && DQ ODT is Enabled) : RL + BL/n + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1 Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_POSTAMBLE = 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. For LPDDR4, if derating is enabled (DERATECTL0.derate_enable=1), derated tDQSCKmax must be used. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0d	wr2rd DDR4: CWL + PL + BL/2 + tWTR_L DDR5: CWL + BL/2 + tWTR_L LPDDR4: WL + BL/2 + tWTR + 1 LPDDR5(BG mode): WL + BL/n_max + RU(tWTR_L/tCK) LPDDR5(16B mode): WL + BL/n + RU(tWTR/tCK) In DDR4, minimum time from write command to read command for same bank group. In others, minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what must be included here. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Add one extra cycle for LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG3_FREQ3

Address: Operational Base + offset (0x30000C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22:16	RW	0x04	t_mr Time from MRW/MRS to valid command DDR4: Set this to the larger of tMOD + AL and tMRD. If C/A parity is enabled, tMOD_PAR(tMOD+PL) + AL and tMRD_PAR(tMOD+PL) and used instead. If CAL mode is enabled, tCAL must be added to the above. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using LRDIMM, the minimum value of this register is tMRD_L2. DDR5: Set this to the larger of tMRR, tMRW, tMRWPD, tMRD and tMPC_DELAY. LPDDR4:Set this to the larger of tMRR, tMRW, tMRWCKEL and tMRD. LPDDR5:Set this to the larger of tMRR, tMRW, tMRWPD and tMRD. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x04	rd2mr Time from Read to MRW/MRR command. LPDDR4: RL + BL/2 + RU(tDQSCKmax/tCK) + RD(tRPST) + max(RU(7.5ns/tCK),8nCK) + nRTP - 8 LPDDR5: RL + RU(tWCKDQO(max)/tCK)) + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nRBTP Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x04	wr2mr Time from Write to MRW/MRR command. LPDDR4: WL + 1 + BL/2 + max(RU(7.5ns/tCK),8nCK) + nWR LPDDR5: WL + BL/n_max + MAX[RU(7.5ns/tCK),4nCK] + nWR Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG4_FREQ3
Address: Operational Base + offset (0x300010)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. Note: For DDR5, it is recommended to set this value as multiple of MEMC_FREQ_RATIO to improve the performance. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
21:16	RW	0x04	t_ccd This is the minimum time between two reads or two writes. DDR4: tCCD_L LPDDR4: tCCD LPDDR5: BL/n Don't Care for DDR5 (see DRAMSET1TMG26.t_ccd_r/t_ccd_w in DDR5). Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_rrd For DDR4/DDR5/LPDDR5(BG mode): Minimum time between activates from bank "a" to bank "b" for same bank group. For LPDDR4/LPDDR5(16B mode): Minimum time between activates from bank "a" to bank "b". DDR4/5: tRRD_L LPDDR4: RU(tRRD/tCK) LPDDR5(BG mode): RU(tRRD_L/tCK) LPDDR5(16B mode): RU(tRRD/tCK) Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_rp tRP: Minimum time from single-bank precharge to activate of same bank. t_rp must be set to RoundUp(tRP/tCK). Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG5_FREQ3

Address: Operational Base + offset (0x300014)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes
29:24	RW	0x05	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: LPDDR4: tCKCKEH LPDDR5: tCKCSH DDR4: tCKSRX DDR5: tCKSRX Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

Bit	Attr	Reset Value	Description
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x05	t_cksre This is the time after Self Refresh Down Entry/Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE/PDE. Recommended settings: LPDDR4: tCKELCK LPDDR5: tCSLCK DDR4: tCKSRE (+ PL(parity latency)(*)) DDR5: tCKLCS (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: LPDDR4: max(tCKE, tSR) LPDDR5: tSR DDR4: tCKESR (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x03	t_cke Delay time between PDE and PDX. LPDDR4: tCKE LPDDR5: tCSPD DDR4: tPD (+ PL(parity latency)(*)) DDR5: Don't care (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. Unit: DRAM clock cycles. Value After Reset:0x3 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG6_FREQ3

Address: Operational Base + offset (0x300018)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x05	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: LPDDR4/5: tXP + 2 This is only present for designs supporting LPDDR devices. Unit: DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG7_FREQ3

Address: Operational Base + offset (0x30001C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	t_csh CS High Pulse width at PDX LPDDR5: tCSH Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG8_FREQ3

Address: Operational Base + offset (0x300020)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x44 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. Note: Used only for DDR4 and DDR5 SDRAMs. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG9_FREQ3

Address: Operational Base + offset (0x300024)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved1 Reserved Field:Yes
20:16	RW	0x04	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. Note: This register field is only applicable for designs supporting DDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:8	RW	0x04	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. Note: This register field is only applicable for designs supporting DDR4/DDR5/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Applicable only in designs configured to support DDR SDRAM memories or LPDDR5 SDRAM memories. DDR4/DDR5 designs: CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Where: CWL = CAS write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. WTR_S must be increased by one if DDR4 2tCK write preamble is used. LPDDR5 designs: WL + BL/n_min +RU(tWTR_S/tCK) Where: WL = Write Latency BL/n_min = Effective Burst Length tWTR_S = internal write to read command delay for different bank group. Unit: DRAM clock cycles. Value After Reset:0xd Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG12_FREQ3

Address: Operational Base + offset (0x300030)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to PDE LPDDR4: max(tESCKE, tCMDCKE) LPDDR5: max(tESPD, tCMDPD) Unit: DRAM clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_DRAMSET1TMG13_FREQ3

Address: Operational Base + offset (0x300034)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. Note: This register field is only applicable for designs supporting LPDDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x1c Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved1 Reserved Field:Yes
22:16	RW	0x20	t_ccd_mw This is the minimum time from write or masked write to masked write command for same bank. LPDDR4: tCCDMW LPDDR5(BG mode): 4*BL/n_max LPDDR5(16B mode): 4*BL/n Note: This register field is only applicable for designs supporting LPDDR4/LPDDR5 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x20 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes
3:0	RW	0x4	t_ppd LPDDR4/5 and DDR5: tPPD: This is the minimum time from precharge to precharge command. Note: This register is not applicable for DDR4 SDRAM memories. Unit: DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG14_FREQ3

Address: Operational Base + offset (0x300038)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes
24:16	RW	0x008	t_osco tosco: Minimum time from DQS Oscillator stop to Mode register readout. LPDDR4 : max(40ns,8nck) LPDDR5A: tOSCODQI=tOSCODQO=max(40ns,8nck) Unit: DRAM clock cycles. Value After Reset:0x8 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. The value 0xfff is illegal for this register field. Unit: DRAM clock cycles. Value After Reset:0xa0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMSET1TMG23_FREQ3
Address: Operational Base + offset (0x30005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	t_xsr_dsm_x1024 Delay from Deep Sleep Mode Exit to SRX. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	t_pdn Minimum interval between Deep Sleep Mode Entry and Exit. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_DRAMSET1TMG24_FREQ3
Address: Operational Base + offset (0x300060)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
25:24	RW	0x0	bank_org Select Bank/ Bank group organization: 00: 4 Banks/ 4 Bank groups 01: 8 Banks (Reserved) 10: 16 Banks 11: Reserved Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:16	RW	0x0f	rd2wr_s Minimum time from read command to write command for different bank group. Includes time for bus turnaround, recovery times and all per-bank, per-rank and global constraints. LPDDR5(DQ ODT is disabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL LPDDR5(DQ ODT is enabled): RL + BL/n_min + RU(tWCKDQO(max)/tCK) + RD(tRPST/tCK) - ODTLon - RD(tODTon(min)/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:8	RW	0x0f	max_rd_sync Minimum time from read command to WCK2CK sync OFF. RL + BL/n_max + RU(tRPST/tCK) Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x0f	max_wr_sync Minimum time from write command to WCK2CK sync OFF. WL + BL/n_max Unit: DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG25_FREQ3

Address: Operational Base + offset (0x300064)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved Field:Yes
18:16	RW	0x0	lpddr4_diff_bank_rwa2pre Set the timing constraint between different bank RD/WR/MWR/ACT and PRE in LPDDR4. LPDDR4 JESD209-4A requires 4 cycles LPDDR4 JESD209-4B requires 2 cycles Value of 1, 3, 5, 6, and 7 are illegal. Don't care for LPDDR5. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
15:8	RW	0x00	wra2pre Time between write with AP and precharge to same bank. LPDDR4: WL + BL/2 + nWR + 1 LPDDR5: WL + BL/n_min + nWR + 1 DDR4: WL + BL/2 + WR Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:0	RW	0x00	rda2pre Time between read with AP and precharge to same bank. LPDDR4: nRTP LPDDR5: BL/n_min + nRBTP DDR4: RTP Don't care for DDR5. Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMSET1TMG30_FREQ3

Address: Operational Base + offset (0x300078)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	mrr2mrw MRR to MRW delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:8	RW	0x00	mrr2wr MRR to WR delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:0	RW	0x00	mrr2rd MRR to RD delay Unit: DRAM clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR0_FREQ3

Address: Operational Base + offset (0x300500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR4: Value loaded into MR0 register. DDR5: Don't care LPDDR4: Value to write to MR1 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

Bit	Attr	Reset Value	Description
15:0	RW	0x0510	emr DDR4: Value to write to MR1 register Set bit 7 to 0. DDR5: Don't care LPDDR4 - Value to write to MR2 register Value After Reset:0x510 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_INITMR1_FREQ3

Address: Operational Base + offset (0x300504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR4: Value to write to MR2 register DDR5: Don't care LPDDR4: Value to write to MR3 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR4: Value to write to MR3 register DDR5: Don't care LPDDR4: Value to write to MR13 register Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INITMR2_FREQ3

Address: Operational Base + offset (0x300508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4: Value to be loaded into SDRAM MR4 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR11 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4: Value to be loaded into SDRAM MR5 registers. DDR5: Don't care LPDDR4: Value to be loaded into SDRAM MR12 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_INITMR3_FREQ3

Address: Operational Base + offset (0x30050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 Value to be loaded into SDRAM MR22 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 DDR4 Value to be loaded into SDRAM MR6 registers. DDR5: Don't care LPDDR4 Value to be loaded into SDRAM MR14 registers (not applicable for initialization, but this is used when HWFFC is performed). Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG0_FREQ3

Address: Operational Base + offset (0x300580)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DRAM clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Volatile:true Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DRAM data clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value.Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycle(s) of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG1_FREQ3

Address: Operational Base + offset (0x300584)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For LPDDR5, this should be set to "twck_delay + BL/n_max - BL/n_min" instead of twrdata_delay. twck_delay specifies the time from dfi_wck_en deassertion to when WCK transfer completes on the DRAM bus and is defined by the PHY Refer to PHY specification for correct value. When TMGCFG.frequency_ratio is set to 0(1:2 Mode), divided the value by 2 and round it up to the next integer value. When TMGCFG.frequency_ratio is set to 1(1:4 Mode), divided the value by 4 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DRAM clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFITMG2_FREQ3

Address: Operational Base + offset (0x300588)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved2 Reserved Field:Yes
21:16	RW	0x00	dfi_twck_delay Number of DFI PHY clock cycles from dfi_wck_en is de-asserted to when the WCK transfer completes on th DRAM bus. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Unit: DRAM data clock cycles. Value After Reset:0x2 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG4_FREQ3
Address: Operational Base + offset (0x300590)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_en_rd WCK Enable Read Timing. Defines the timing from the CAS-WS_RD command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_en_wr WCK Enable Read Timing. Defines the timing from the CAS-WS_WR command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_en_fs WCK Enable Fast Sync Timing. Defines the timing from the CAS-WS_FS command to driving of the dfi_wck_en=ENABLED. Unit: WCK cycles Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_dis WCK Off Timing. Defines the timing from the last command opportunity to the deassertion of dfi_wck_en and dfi_wck_toggle_en assuming that no command is being sent. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFITMG5_FREQ3
Address: Operational Base + offset (0x300594)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dfi_twck_fast_toggle Defines the number of clock cycles between the dfi_wck_signal being driven to TOGGLE to when the dfi_wck_signal is driven to FAST_TOGGLE. This timing is only applicable when the WCK transitions from the slow to fast toggle. Otherwise, this timing parameter must be set to 0x0. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
23:16	RW	0x00	dfi_twck_toggle WCK Toggle Enable Timing. Defines the timing from dfi_wck_en assertion to dfi_wck_toggle_en assertion. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
15:8	RW	0x00	dfi_twck_toggle_cs Defines the number of clock cycles between a read or write command to when the dfi_wck_cs signal must be stable. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4
7:0	RW	0x00	dfi_twck_toggle_post Defines the number of clock cycles after a read or write command data burst completion during which the WCK must remain in the current toggle state. Unit: WCK cycles Value After Reset:0x0 Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_DFIUPDTMG1_FREQ3

Address: Operational Base + offset (0x3005AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between DDRCTL initiated DFI update requests (which is executed whenever the DDRCTL is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the DDRCTL is idle. Minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static
15:8	RW	0x00	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between DDRCTL initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x1 Programming Mode:Static

DDRCTL_RFSHSET1TMG0_FREQ3

Address: Operational Base + offset (0x300600)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_refi_x1_sel Specifies whether RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used, 1 - x1 register values are used. This applies only when per-bank refresh is enabled (RFSHMOD0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR4/5. For such configurations, the value of this register field can be assumed to be 0, so that RFSHSET1TMG0.t_refi_x1_x32 and RFSHSET1TMG0.refresh_to_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
27:24	RW	0x2	refresh_margin Threshold value in number of DRAM clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_refi/32. Note that internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32 * 32 if RFSHSET1TMG0.t_refi_x1_sel = 0. If RFSHSET1TMG0.t_refi_x1_sel = 1, internally used t_refi is equal to RFSHSET1TMG0.t_refi_x1_x32. Note that, internally used t_refi may be divided by four if derating or TCR is enabled. Unit: Multiples of 32 DRAM clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related
23:22	RW	0x0	Reserved1 Reserved Field:Yes
21:16	RW	0x10	refresh_to_x1_x32 If the refresh timer has expired at least once (i.e. >tREFI period elapses, and there are postponed refreshes), then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When there are no transactions pending in the CAM for a period of time determined by this RFSHSET1TMG0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the DDRCTL. This is also used for non speculative refresh when LPDDR per-bank refresh (REFpb) or DDR5 same-bank refresh (REFsb) is enabled. The controller observes the period of time determined by this for each bank, and a priority of bank address is determined. For non-DDR5, this should be programmed to tREFI based value in controller's current refresh mode. For DDR5, this should be always programmed to tREFI1 based value even in FGR mode. The controller calculates this according to current refresh mode. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x062	t_refi_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR4, 3.9us for DDR5. See JEDEC specification for LPDDR4). set this register to RoundDown(tREFI/tCK) if RFSHSET1TMG0.t_refi_x1_sel = 0, divide the above result by 32 and round down. For LPDDR controller: if using all-bank refreshes (RFSHMOD0.per_bank_refresh = 0), use tREFIab in the above calculations if using per-bank refreshes (RFSHMOD0.per_bank_refresh = 1), use tREFIpb in the above calculations For DDR controller, tREFI value is different depending on FGR mode. In DDR4 mode, if using FGR 1x mode (RFSHMOD1.fgr_mode = 000), use tREFI1 in the above calculations In DDR4 mode, if using FGR 2x mode (RFSHMOD1.fgr_mode = 001), use tREFI2 in the above calculations In DDR4 mode, if using FGR 4x mode (RFSHMOD1.fgr_mode = 010), use tREFI4 in the above calculations In DDR5 mode, always use tREFI1 in the above calculations Note that: RFSHSET1TMG0.t_refi_x1_x32 must be greater than 0x1. if RFSHSET1TMG0.t_refi_x1_sel == 1, RFSHSET1TMG0.t_refi_x1_x32 must be greater than RFSHSET1TMG1.t_rfc_min if RFSHSET1TMG0.t_refi_x1_sel == 0, RFSHSET1TMG0.t_refi_x1_x32 * 32 must be greater than RFSHSET1TMG1.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0xFFE. In DDR4 Fixed 2x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x7FF. In DDR4 Fixed 4x mode: RFSHSET1TMG0.t_refi_x1_x32 must be less than or equal to 0x3FF. Unit: DRAM clock cycles or multiples of 32 DRAM clock cycles, depending on RFSHSET1TMG0.t_refi_x1_sel. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG1_FREQ3

Address: Operational Base + offset (0x300604)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min must be set to RoundUp(tRFCmin/tCK). In LPDDR controller: if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4/DDR5 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user must program the appropriate value from the spec based on the 'fgr_mode' and the device density that is used. Unit: DRAM clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHSET1TMG2_FREQ3
Address: Operational Base + offset (0x300608)

Bit	Attr	Reset Value	Description
31:24	RW	0x8c	t_pbr2act Time from REFpb to activate command to different bank than REFpb. LPDDR5: tpbr2act Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
23:16	RW	0x8c	t_pbr2pbr LPDDR4: tpbR2pbR Per-bank Refresh to Per-bank refresh different bank Time. Program this to RoundUp(tpbR2pbR/tCK). The tpbR2pbR value in the above equations is different depending on the device density. The user must program the appropriate value from the spec. Register is valid only in LPDDR4 per-bank refresh mode (RFSHMOD0.per_bank_refresh == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_RFSHSET1TMG4_FREQ3
Address: Operational Base + offset (0x300610)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_ZQSET1TMG0_FREQ3
Address: Operational Base + offset (0x300800)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	t_zq_short_nop tZQCS for DD4, tZQLAT for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x40 Programming Mode:Static
15:14	RW	0x0	Reserved0 Reserved Field:Yes
13:0	RW	0x0200	t_zq_long_nop tZQoper for DDR4, tZQCAL for DDR5/LPDDR4/LPDDR5: Number of DRAM clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. If using LPDDR5, this register needs to be programmed to tZQCAL + 10 cycles. Unit: DRAM clock cycles. Value After Reset:0x200 Programming Mode:Static

DDRCTL_ZQSET1TMG1_FREQ3
Address: Operational Base + offset (0x300804)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DRAM clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. Unit: DRAM clock cycles. Value After Reset:0x20 Programming Mode:Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR4/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. Unit: Multiples of 1024 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x100 Programming Mode:Static

DDRCTL_DQSOSCCTL0_FREQ3

Address: Operational Base + offset (0x300A80)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved2 Reserved Field:Yes
15:4	RW	0x007	dqsosc_interval DQS Oscillator interval, specifies the time between two DQS oscillator sequences. Minimum programmable value is 1. The value can be changed while DQSOSCCTL0.dqsosc_enable=0 Unit: DFI clock cycles Value After Reset:0x7 Programming Mode:Dynamic
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	dqsosc_interval_unit DQS/WCK Oscillator Interval unit. Specifies the unit for counting DQS oscillator interval.The value can be changed while DQSOSCCTL0.dqsosc_enable=0 1: x2K DFI clock cycles 0: x32K DFI clock cycles Value After Reset:0x0 Programming Mode:Dynamic
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dqsosc_enable DQS/WCK Oscillator Enable 1: Enable DQS Oscillator 0: Disable DQS Oscillator Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATEINT_FREQ3

Address: Operational Base + offset (0x300B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. This register must not be set to zero. Unit: DRAM clock cycles. Value After Reset:0x800000 Volatile:true Programming Mode:Static

DDRCTL_DERATEVAL0_FREQ3

Address: Operational Base + offset (0x300B04)

Bit	Attr	Reset Value	Description
31:24	RW	0x05	derated_t_rcd Derated value for tRCD. For LPDDR4, the required period with derating is tRCD + 1.875ns For LPDDR5, the required period with derating is tRCD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
23:16	RW	0x0f	derated_t_ras_min Derated value for tRAS. For LPDDR4, the required period with derating is tRAS + 1.875ns For LPDDR5, the required period with derating is tRAS + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x05	derated_t_rp Derated value for tRP. For LPDDR4, the required period with derating is tRP + 1.875ns For LPDDR5, the required period with derating is tRP + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x5 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
5:0	RW	0x04	derated_t_rrd Derated value for tRRD. For LPDDR4, the required period with derating is tRRD + 1.875ns For LPDDR5, the required period with derating is tRRD + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x4 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DERATEVAL1_FREQ3
Address: Operational Base + offset (0x300B08)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x14	derated_t_rc Derated value for tRC. For LPDDR4, the required period with derating is tRC + 3.75ns For LPDDR5, the required period with derating is tRC + TBD ns This timing parameter must be rounded up to the next integer value. Unit:DRAM clock cycles. Value After Reset:0x14 Volatile:true Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_HWLPTMG0_FREQ3
Address: Operational Base + offset (0x300B80)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value when the controller is in 1:2 mode. hw_lp_idle_x32=1/2/3 are illegal values when the controller is in 1:4 mode. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x0 Volatile:true Programming Mode:Static
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_SCHEDTMG0_FREQ3
Address: Operational Base + offset (0x300C00)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14:8	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static
7:0	RW	0x00	pageclose_timer This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Unit: DRAM clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_PERFHPR1_FREQ3

Address: Operational Base + offset (0x300C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	hpr_xact_run_length Number of transactions that are serviced once the HPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x0001	hpr_max_starve Number of DRAM clocks that the HPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x1 Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFLPR1_FREQ3

Address: Operational Base + offset (0x300C84)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	lpr_max_starve Number of DRAM clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFWR1_FREQ3

Address: Operational Base + offset (0x300C88)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 3

Bit	Attr	Reset Value	Description
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	w_max_starve Number of DRAM clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function must not be disabled as it will cause excessive latencies. FOR PERFORMANCE ONLY. Unit: DRAM clock cycles. Value After Reset:0x7f Volatile:true Programming Mode:Quasi-dynamic Group 3

DDRCTL_TMGCFG_FREQ3
Address: Operational Base + offset (0x300D00)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved1 Reserved Field:Yes
9:8	RW	0x0	dfi_freq_fsp This register value propergates to dfi_freq_fsp pin directly. Value After Reset:0x0 Programming Mode:Dynamic
7:1	RW	0x00	Reserved0 Reserved Field:Yes
0	RW	0x0	frequency_ratio Selects the Frequency Ratio For DDR4/DDR5/LPDDR4: 0: 1:2 Mode 1: 1:4 Mode For LPDDR5: 0: 1:1:2 Mode 1: 1:1:4 Mode Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG0_FREQ3
Address: Operational Base + offset (0x300D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
15:8	RW	0x06	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, must be increased by 1. If write preamble is set to 2tCK(DDR4 only), must be increased by 1. Write preamble is always set to 2tCK for LPDDR4, refer to PHY databook to see if this is already factored into tphy_wrcsgap value or if it needs to be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), must be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

Bit	Attr	Reset Value	Description
7:0	RW	0x06	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Program this to the larger of PHY requirement or ODT requirement. After PHY has completed training the value programmed may need to be increased. Refer to relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TRDRD timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles. Value After Reset:0x6 Volatile:true Programming Mode:Quasi-dynamic Group 2

DDRCTL_RANKTMG1_FREQ3

Address: Operational Base + offset (0x300D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:8	RW	0x0f	rd2wr_dr Minimum time from read command to write command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. The value must be larger than or equal to the value of DRAMSET1TMG2.rd2wr. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

Bit	Attr	Reset Value	Description
7:0	RW	0x0f	wr2rd_dr Minimum time from write command to read command for different rank. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. For LPDDR5, Please set to "JEDEC formula + tphy_wckcsgap + board delay" Please see PHY databook for the value of tphy_wckcsgap Unit: DRAM clock cycles Value After Reset:0xf Volatile:true Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_PWRTMG_FREQ3

Address: Operational Base + offset (0x300D0C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25:16	RW	0x040	selfref_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x40 Volatile:true Programming Mode:Quasi-dynamic Group 4
15:7	RW	0x000	Reserved0 Reserved Field:Yes
6:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the DDRCTL automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DRAM clock cycles. Please refer to "Note 1" from "Notes on Timing Registers" at the start of "Register Descriptions" chapter for details on how to program this register field. Value After Reset:0x10 Volatile:true Programming Mode:Quasi-dynamic Group 4

2.4.3 Registers Summary For DDRPHY

Name	Offset	Size	Reset Value	Description
DDRPHY_GNR_CON0	0x0000	W	0x44005011	GENERAL Control Register 0
DDRPHY_CAL_CON0	0x0004	W	0x789606C0	CALIBRATION Control Register 0
DDRPHY_CAL_CON1	0x0008	W	0x20142001	CALIBRATION Control Register 1
DDRPHY_CAL_CON2	0x000C	W	0x42001300	CALIBRATION Control Register 2

Name	Offset	Size	Reset Value	Description
DDRPHY_CAL_CON3	0x0010	W	0xFC7F9000	CALIBRATION Control Register 3
DDRPHY_CAL_CON4	0x0014	W	0x0083806F	CALIBRATION Control Register 4
DDRPHY_LP_CON0	0x0018	W	0x000C4403	Low Power Control Register 0
DDRPHY_GATE_CON0	0x001C	W	0x0300F00F	GATE Control Register 0
DDRPHY_OFFSETR_CON0	0x0020	W	0x00000000	READ Code Control Register 0
DDRPHY_OFFSETW_CON0	0x0030	W	0x00000000	OFFSET WRITE Code Control Register 0
DDRPHY_OFFSET_DQ_CON0	0x003C	W	0x00000000	READ DQ Code Control Register
DDRPHY_OFFSETC_CON0	0x0040	W	0x00000000	GATE Code Control Register 0
DDRPHY_SHIFTC_CON0	0x004C	W	0x00000000	GATE Code Shift Control Register 0
DDRPHY_OFFSETD_CON0	0x0050	W	0x00000000	CMD Code Control Register
DDRPHY_OFFSETO_CON0	0x0058	W	0x00000000	DQ/DM OEN Code Control Register 0
DDRPHY_WR_LVL_CON0	0x006C	W	0x00000000	Write Leveling Control Register 0
DDRPHY_WR_LVL_CON1	0x0070	W	0x01E80473	Write Leveling Control Register 1
DDRPHY_WR_LVL_CON2	0x0074	W	0x40465580	Write Leveling Control Register 2
DDRPHY_WR_LVL_CON3	0x0078	W	0x00000B00	Write Leveling Control Register 3
DDRPHY_CA_DESKEW_CON0	0x007C	W	0x00000000	CA Deskew Control Register 0
DDRPHY_CA_DESKEW_CON1	0x0080	W	0x00000000	CA Deskew Control Register 1
DDRPHY_CA_DESKEW_CON2	0x0084	W	0x00000000	CA Deskew Control Register 2
DDRPHY_CA_DESKEW_CON3	0x0088	W	0x00000000	CA Deskew Control Register 3
DDRPHY_CA_DESKEW_CON4	0x008C	W	0x00000000	CA Deskew Control Register 2
DDRPHY_CA_DESKEW_CON5	0x0090	W	0x00000000	CA Deskew Control Register 2
DDRPHY_CA_DESKEW_CON6	0x0094	W	0x00000000	CA Deskew Control Register 2
DDRPHY_CAL_WR_PATTERN_CON0	0x0098	W	0x00FF00FF	Write Calibration Pattern Register 0
DDRPHY_CAL_WR_PATTERN_CON1	0x009C	W	0x00FF00FF	Write Calibration Pattern Register 1
DDRPHY_CAL_WR_PATTERN_CON2	0x00A0	W	0x00FF00FF	Write Calibration Pattern Register 2
DDRPHY_CAL_WR_PATTERN_CON3	0x00A4	W	0x00FF00FF	Write Calibration Pattern Register 3
DDRPHY_CAL_WR_PATTERN_CON4	0x00A8	W	0x00005555	Write Calibration Pattern Register 4

Name	Offset	Size	Reset Value	Description
DDRPHY_CAL_RD_PATTERN_CON0	0x00AC	W	0x55555A3C	Read Calibration Pattern Register 0
DDRPHY_MDLL_CON0	0x00B0	W	0x2000017E	MDLL Control Register 0
DDRPHY_MDLL_CON1	0x00B4	W	0x00200100	MDLL Control Register 1
DDRPHY_DVFS_CON	0x00B8	W	0x00002640	DVFS Control Register 0
DDRPHY_DVFS0_CON0	0x00BC	W	0x64080C06	DVFS Control Register 1
DDRPHY_DVFS1_CON0	0x00C0	W	0x64080C06	DVFS Control Register 2
DDRPHY_DVFS0_CON1	0x00C4	W	0x30800000	DVFS Control Register 3
DDRPHY_DVFS1_CON1	0x00C8	W	0x30800000	DVFS Control Register 4
DDRPHY_DVFS0_CON2	0x00CC	W	0x60062001	DVFS Control Register 5
DDRPHY_DVFS1_CON2	0x00D0	W	0x60062001	DVFS Control Register 6
DDRPHY_DVFS0_CON3	0x00D4	W	0x0003FFFF	DVFS Control Register 7
DDRPHY_DVFS1_CON3	0x00D8	W	0x0003FFFF	DVFS Control Register 8
DDRPHY_DVFS0_CON4	0x00DC	W	0x00243F3F	DVFS Control Register 9
DDRPHY_DVFS1_CON4	0x00E0	W	0x00243F3F	DVFS Control Register 10
DDRPHY_CAL_WRLVL_STAT	0x00E4	W	0x00000000	Write leveling fail Status Register
DDRPHY_CAL_FAIL_STAT0	0x00E8	W	0x00000000	Calibration Fail Status Register 1
DDRPHY_CAL_FAIL_STAT1	0x00EC	W	0x00000000	Calibration Fail Status Register 2
DDRPHY_CAL_GT_CS0_VWMC0	0x00F0	W	0x00000000	Calibration Gate Training Centering Code 0
DDRPHY_CAL_GT_CS0_CYC	0x00FC	W	0x00000000	Calibration Gate Training Cycle
DDRPHY_CAL_RD_VWMC0	0x0100	W	0x00000000	Calibration Read Center Code 0
DDRPHY_CAL_RD_VWML0	0x0110	W	0x00000000	Calibration Read Left Code 0
DDRPHY_CAL_RD_VWMR0	0x0120	W	0x00000000	Calibration Read Right Code 0
DDRPHY_CAL_WR_VWMC0	0x0130	W	0x00000000	Calibration Write Center Code 0
DDRPHY_CAL_WR_VWML0	0x0140	W	0x00000000	Calibration Write Left Code 0
DDRPHY_CAL_WR_VWMR0	0x0150	W	0x00000000	Calibration Write Right Code 0
DDRPHY_CAL_CON5	0x0160	W	0x00000000	CALIBRATION Control Register 5
DDRPHY_DVFS_UPD_CON0	0x0164	W	0x003F3F3F	DVFS DLL update Control Register
DDRPHY_DVFS_UPD_CON1	0x0168	W	0x003F3F3F	DVFS DLL update Control Register
DDRPHY_RD_DESKEW_CENTER_CS0_CON_DM	0x018C	W	0x00000000	READ DE-SKEW CS0 CONTROL DM
DDRPHY_RD_DESKEW_CENTER_CS0_CON0	0x0190	W	0x00000000	READ DE-SKEW CS0 CONTROL 0

Name	Offset	Size	Reset Value	Description
DDRPHY_RD_DESKEW_CENTER_CS0_CON1	0x019C	W	0x00000000	READ DE-SKEW CS0 CONTROL 1
DDRPHY_RD_DESKEW_CENTER_CS0_CON2	0x01A8	W	0x00000000	READ DE-SKEW CS0 CONTROL 2
DDRPHY_RD_DESKEW_CENTER_CS0_CON3	0x01B4	W	0x00000000	READ DE-SKEW CS0 CONTROL 3
DDRPHY_RD_DESKEW_CENTER_CS0_CON4	0x01C0	W	0x00000000	READ DE-SKEW CS0 CONTROL 4
DDRPHY_RD_DESKEW_CENTER_CS0_CON5	0x01CC	W	0x00000000	READ DE-SKEW CS0 CONTROL 5
DDRPHY_RD_DESKEW_CENTER_CS0_CON6	0x01D8	W	0x00000000	READ DE-SKEW CS0 CONTROL 6
DDRPHY_RD_DESKEW_CENTER_CS0_CON7	0x01E4	W	0x00000000	READ DE-SKEW CS0 CONTROL 7
DDRPHY_WR_DESKEWC_CS0_CON0	0x01F0	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 0
DDRPHY_WR_DESKEWC_CS0_CON1	0x01FC	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 1
DDRPHY_WR_DESKEWC_CS0_CON2	0x0208	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 2
DDRPHY_WR_DESKEWC_CS0_CON3	0x0214	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 3
DDRPHY_WR_DESKEWC_CS0_CON4	0x0220	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 4
DDRPHY_WR_DESKEWC_CS0_CON5	0x022C	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 5
DDRPHY_WR_DESKEWC_CS0_CON6	0x0238	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 6
DDRPHY_WR_DESKEWC_CS0_CON7	0x0244	W	0x00000000	WRITE DE-SKEW CS0 Center CONTROL 7
DDRPHY_DM_DESKEWC_CS0_CON0	0x0250	W	0x00000000	DM DE-SKEW CS0 Center CONTROL 7
DDRPHY_ECC_DESKEWC_CS0_CON0	0x0254	W	0x00000000	ECC DE-SKEW CS0 Center CONTROL 7
DDRPHY_VWMC_STAT0	0x025C	W	0x00000000	VWMC STAT 0
DDRPHY_VWMC_STAT3	0x0268	W	0x00000000	VWMC STAT 3
DDRPHY_VWMC_STAT6	0x0274	W	0x00000000	VWMC STAT 6
DDRPHY_VWMC_STAT9	0x0280	W	0x00000000	VWMC STAT 9
DDRPHY_VWMC_STAT12	0x028C	W	0x00000000	VWMC STAT 12
DDRPHY_VWMC_STAT15	0x0298	W	0x00000000	VWMC STAT 15
DDRPHY_VWMC_STAT18	0x02A4	W	0x00000000	VWMC STAT 18
DDRPHY_VWMC_STAT21	0x02B0	W	0x00000000	VWMC STAT 21

Name	Offset	Size	Reset Value	Description
DDRPHY_DM_VWMC_STAT0	0x02BC	W	0x00000000	DM VWMC 0
DDRPHY_VWML_STAT0	0x02C8	W	0x00000000	VWML STAT 0
DDRPHY_VWML_STAT3	0x02D4	W	0x00000000	VWML STAT 3
DDRPHY_VWML_STAT6	0x02E0	W	0x00000000	VWML STAT 6
DDRPHY_VWML_STAT9	0x02EC	W	0x00000000	VWML STAT 9
DDRPHY_VWML_STAT12	0x02F8	W	0x00000000	VWML STAT 12
DDRPHY_VWML_STAT15	0x0304	W	0x00000000	VWML STAT 15
DDRPHY_VWML_STAT18	0x0310	W	0x00000000	VWML STAT 18
DDRPHY_VWML_STAT21	0x031C	W	0x00000000	VWML STAT 21
DDRPHY_DM_VWML_STAT0	0x0328	W	0x00000000	DM VWML 0
DDRPHY_VWMR_STAT0	0x0334	W	0x00000000	VWMR STAT 0
DDRPHY_VWMR_STAT3	0x0340	W	0x00000000	VWMR STAT 3
DDRPHY_VWMR_STAT6	0x034C	W	0x00000000	VWMR STAT 6
DDRPHY_VWMR_STAT9	0x0358	W	0x00000000	VWMR STAT 9
DDRPHY_VWMR_STAT12	0x0364	W	0x00000000	VWMR STAT 12
DDRPHY_VWMR_STAT15	0x0370	W	0x00000000	VWMR STAT 15
DDRPHY_VWMR_STAT18	0x037C	W	0x00000000	VWMR STAT 18
DDRPHY_VWMR_STAT21	0x0388	W	0x00000000	VWMR STAT 21
DDRPHY_DM_VWMR_STAT0	0x0394	W	0x00000000	DM VWMR 0
DDRPHY_DQ_IO_RDATA0	0x03A0	W	0x00000000	DQ I/O Read Data STAT 0
DDRPHY_VERSION_INFO_STAT0	0x03AC	W	0x09080005	Version Information
DDRPHY_ZQ_CON0	0x03C8	W	0xFF807404	ZQ Control Register 0
DDRPHY_ZQ_CON1	0x03CC	W	0x00140000	ZQ Control Register 1
DDRPHY_ZQ_CON2	0x03D0	W	0x001E0002	ZQ Control Register 2
DDRPHY_ZQ_CON3	0x03D4	W	0x003F3F3F	ZQ Control Register 3
DDRPHY_ZQ_CON5	0x03DC	W	0x073F003F	ZQ Control Register 5
DDRPHY_ZQ_CON6	0x03E0	W	0x00002121	ZQ Control Register 6
DDRPHY_ZQ_CON9	0x03EC	W	0x00001414	ZQ Control Register 9
DDRPHY_ZQ_CON12	0x03F8	W	0x00000707	ZQ Control Register 12
DDRPHY_TESTIRCV_CON0	0x0400	W	0x00080000	ZQ Control Register 14
DDRPHY_WR_DESKEWC_CS1_CON0	0x0410	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL0
DDRPHY_WR_DESKEWC_CS1_CON1	0x041C	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL1
DDRPHY_WR_DESKEWC_CS1_CON2	0x0428	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL2
DDRPHY_WR_DESKEWC_CS1_CON3	0x0434	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL3

Name	Offset	Size	Reset Value	Description
DDRPHY_WR_DESKEWC_CS1_CON4	0x0440	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL4
DDRPHY_WR_DESKEWC_CS1_CON5	0x044C	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL5
DDRPHY_WR_DESKEWC_CS1_CON6	0x0458	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL6
DDRPHY_WR_DESKEWC_CS1_CON7	0x0464	W	0x00000000	WRITE DE-SKEW CS1 Center CONTROL7
DDRPHY_DM_DESKEWC_CS1_CON0	0x0470	W	0x00000000	WRITE DM DE-SKEW CS1 Center CONTROL0
DDRPHY_ECC_DESKEWC_CS1_CON0	0x0474	W	0x00000000	WRITE ECC DE-SKEW CS1 Center CONTROL0
DDRPHY_WR_DESKEWL_CS0_CON0	0x0490	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL0
DDRPHY_WR_DESKEWL_CS0_CON1	0x049C	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL1
DDRPHY_WR_DESKEWL_CS0_CON2	0x04A8	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL2
DDRPHY_WR_DESKEWL_CS0_CON3	0x04B4	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL3
DDRPHY_WR_DESKEWL_CS0_CON4	0x04C0	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL4
DDRPHY_WR_DESKEWL_CS0_CON5	0x04CC	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL5
DDRPHY_WR_DESKEWL_CS0_CON6	0x04D8	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL6
DDRPHY_WR_DESKEWL_CS0_CON7	0x04E4	W	0x00000000	WRITE DE-SKEW CS0 LEFT CONTROL7
DDRPHY_DM_DESKEWL_CS0_CON0	0x04F0	W	0x00000000	WRITE DM DE-SKEW CS0 LEFT CONTROL0
DDRPHY_ECC_DESKEWL_CS0_CON0	0x04F4	W	0x00000000	WRITE ECC DE-SKEW CS0 LEFT CONTROL0
DDRPHY_WR_DESKEWL_CS1_CON0	0x0500	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL0
DDRPHY_WR_DESKEWL_CS1_CON1	0x050C	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL1
DDRPHY_WR_DESKEWL_CS1_CON2	0x0518	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL2
DDRPHY_WR_DESKEWL_CS1_CON3	0x0524	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL3
DDRPHY_WR_DESKEWL_CS1_CON4	0x0530	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL4

Name	Offset	Size	Reset Value	Description
DDRPHY_WR_DESKEWL_CS1_CON5	0x053C	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL5
DDRPHY_WR_DESKEWL_CS1_CON6	0x0548	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL6
DDRPHY_WR_DESKEWL_CS1_CON7	0x0554	W	0x00000000	WRITE DE-SKEW CS1 LEFT CONTROL7
DDRPHY_DM_DESKEWL_CS1_CON0	0x0560	W	0x00000000	WRITE DM DE-SKEW CS1 LEFT CONTROL0
DDRPHY_ECC_DESKEWL_CS1_CON0	0x0564	W	0x00000000	WRITE ECC DE-SKEW CS1 LEFT CONTROL0
DDRPHY_RD_DQS_VWML_CS0_CON0	0x0574	W	0x00000000	Read DQS Left Code CS0 CON0
DDRPHY_RD_DQS_VWMC_CS0_CON0	0x0580	W	0x00000000	Read DQS Centering CS0 Code CON0
DDRPHY_GT_STATUS_CON0	0x058C	W	0x00000000	Gate Status Register 0
DDRPHY_GT_STATUS_CON1	0x0590	W	0x00000000	Gate Status Register 1
DDRPHY_GT_FSM_STATUS_CON1	0x0594	W	0x00000000	Gate FSM Status Register 1
DDRPHY_CAL_GT_CS1_VWMC0	0x05E4	W	0x00000000	Gate Training CS1 Center Code CON0
DDRPHY_CAL_GT_CS1_CYC	0x05F0	W	0x00000000	Gate Training CS1 Cycle Control
DDRPHY_CBT_CON5	0x05F4	W	0x000D340A	Command Bus Training CON4
DDRPHY_CBT_CMD	0x05FC	W	0x0008043F	Command Bus Training CMD
DDRPHY_CBT_CON0	0x0600	W	0x0003E24D	Command Bus Training CON0
DDRPHY_CBT_CON2	0x0608	W	0x00006300	Command Bus Training CON2
DDRPHY_CBT_CON3	0x060C	W	0x00C80000	Command Bus Training CON2
DDRPHY_RD_DESKEW_LEFT_CS0_CON_DM	0x0610	W	0x00000000	Read Deskew Left CS0 register DM
DDRPHY_RD_DESKEW_LEFT_CS0_CON0	0x0614	W	0x00000000	Read Deskew Left CS0 register 0
DDRPHY_RD_DESKEW_LEFT_CS0_CON1	0x0620	W	0x00000000	Read Deskew Left CS0 register 1
DDRPHY_RD_DESKEW_LEFT_CS0_CON2	0x062C	W	0x00000000	Read Deskew Left CS0 register 2
DDRPHY_RD_DESKEW_LEFT_CS0_CON3	0x0638	W	0x00000000	Read Deskew Left CS0 register 3
DDRPHY_RD_DESKEW_LEFT_CS0_CON4	0x0644	W	0x00000000	Read Deskew Left CS0 register 4
DDRPHY_RD_DESKEW_LEFT_CS0_CON5	0x0650	W	0x00000000	Read Deskew Left CS0 register 5

Name	Offset	Size	Reset Value	Description
DDRPHY_RD_DESKEW_LEFT_CS0_CON6	0x065C	W	0x00000000	Read Deskew Left CS0 register 6
DDRPHY_RD_DESKEW_LEFT_CS0_CON7	0x0668	W	0x00000000	Read Deskew Left CS0 register 7
DDRPHY_FREQ_OFFSET_CON	0x0680	W	0x00000000	Frequency offset register
DDRPHY_PRBS_CON0	0x0684	W	0x00050000	PRBS training register 0
DDRPHY_PRBS_CON1	0x0688	W	0x0542010C	PRBS training register 1
DDRPHY_PRBS_CON2	0x068C	W	0x00000000	PRBS training register 2
DDRPHY_PRBS_CON3	0x0690	W	0x00000000	PRBS training register 3
DDRPHY_PRBS_CON4	0x0694	W	0x00000000	PRBS training register 4
DDRPHY_PRBS_CON5	0x0698	W	0x00000000	PRBS training register 5
DDRPHY_PRBS_CON6	0x069C	W	0x00000000	PRBS training register 6
DDRPHY_PRBS_CON7	0x06A0	W	0x00000000	PRBS training register 7
DDRPHY_PRBS_CON8	0x06A4	W	0x800B0000	PRBS training register 8
DDRPHY_PRBS_CON9	0x06A8	W	0x00FF00FF	PRBS training register 9
DDRPHY_PRBS_CON10	0x06AC	W	0x0F0F0F0F	PRBS training register 10
DDRPHY_PRBS_CON11	0x06B0	W	0x5A5A5A5A	PRBS training register 11
DDRPHY_PRBS_CON12	0x06B4	W	0xFF00FF00	PRBS training register 12
DDRPHY_PRBS_CON13	0x06B8	W	0x00000055	PRBS training register 13
DDRPHY_DUTY_CAL0	0x06BC	W	0x00000000	DUTY training register 0
DDRPHY_MON_CON0	0x0700	W	0x00020000	Debug mode register 0
DDRPHY_MON_CON1	0x0704	W	0x00000000	Debug mode register 1
DDRPHY_MON_CON2	0x0708	W	0x00000000	Debug mode register 2
DDRPHY_MON_CON3	0x070C	W	0x00000000	Debug mode register 3
DDRPHY_MON_CON4	0x0710	W	0x00000000	Debug mode register 4
DDRPHY_MON_CON5	0x0714	W	0x00000000	Debug mode register 5
DDRPHY_MON_CON6	0x0718	W	0x00000000	Debug mode register 6
DDRPHY_MON_CON7	0x071C	W	0x00000000	Debug mode register 7
DDRPHY_WR_TRAIN_MON0	0x0720	W	0x00000000	Write training monitor register 0
DDRPHY_LOCK_VAL0	0x0728	W	0x001FFC01	Master DLL status register 0
DDRPHY_LOCK_VAL1	0x072C	W	0x001FFC01	Master DLL status register 1
DDRPHY_LOCK_VAL2	0x0730	W	0x001FFC01	Master DLL status register 2
DDRPHY_WR_CHECK_CON0	0x0750	W	0x00000000	FIFO status register 0
DDRPHY_WR_CHECK_CON1	0x0754	W	0x00000000	FIFO status register 1
DDRPHY_WR_CHECK_CON2	0x0760	W	0x00000000	FIFO status register 2
DDRPHY_RD_DQS_VWML_CS1_CON0	0x0764	W	0x00000000	Read DQS Left Code CS1 CON0

Name	Offset	Size	Reset Value	Description
DDRPHY_RD_DQS_VWMC_CS1_CON0	0x0768	W	0x00000000	Read DQS Centering CS1 Code CON0
DDRPHY_RD_DESKEW_CENTER_CS1_CON_DM	0x076C	W	0x00000000	READ DE-SKEW CS1 CONTROL DM
DDRPHY_RD_DESKEW_CENTER_CS1_CON0	0x0770	W	0x00000000	READ DE-SKEW CS1 CONTROL 0
DDRPHY_RD_DESKEW_CENTER_CS1_CON1	0x0774	W	0x00000000	READ DE-SKEW CS1 CONTROL 1
DDRPHY_RD_DESKEW_CENTER_CS1_CON2	0x0778	W	0x00000000	READ DE-SKEW CS1 CONTROL 2
DDRPHY_RD_DESKEW_CENTER_CS1_CON3	0x077C	W	0x00000000	READ DE-SKEW CS1 CONTROL 3
DDRPHY_RD_DESKEW_CENTER_CS1_CON4	0x0780	W	0x00000000	READ DE-SKEW CS1 CONTROL 4
DDRPHY_RD_DESKEW_CENTER_CS1_CON5	0x0784	W	0x00000000	READ DE-SKEW CS1 CONTROL 5
DDRPHY_RD_DESKEW_CENTER_CS1_CON6	0x0788	W	0x00000000	READ DE-SKEW CS1 CONTROL 6
DDRPHY_RD_DESKEW_CENTER_CS1_CON7	0x078C	W	0x00000000	READ DE-SKEW CS1 CONTROL 7
DDRPHY_RD_DESKEW_LEFT_CS1_CON_DM	0x0790	W	0x00000000	READ DE-SKEW Left CS1 CONTROL DM
DDRPHY_RD_DESKEW_LEFT_CS1_CON0	0x0794	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 0
DDRPHY_RD_DESKEW_LEFT_CS1_CON1	0x0798	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 1
DDRPHY_RD_DESKEW_LEFT_CS1_CON2	0x079C	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 2
DDRPHY_RD_DESKEW_LEFT_CS1_CON3	0x07A0	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 3
DDRPHY_RD_DESKEW_LEFT_CS1_CON4	0x07A4	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 4
DDRPHY_RD_DESKEW_LEFT_CS1_CON5	0x07A8	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 5
DDRPHY_RD_DESKEW_LEFT_CS1_CON6	0x07AC	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 6
DDRPHY_RD_DESKEW_LEFT_CS1_CON7	0x07B0	W	0x00000000	READ DE-SKEW Left CS1 CONTROL 7
DDRPHY_SW_RD_DQS_VWML_CS0_CON0	0x07C0	W	0x00000000	SW Read DQS Left Code CS0 CON0
DDRPHY_SW_RD_DQS_VWMC_CS0_CON0	0x07C4	W	0x00000000	SW Read DQS Centering CS0 Code CON0

Name	Offset	Size	Reset Value	Description
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON_DM	0x07C8	W	0x00000000	SW Read DE-SKEW CS0 CONTROL DM
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON0	0x07CC	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 0
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON1	0x07D0	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 1
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON2	0x07D4	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 2
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON3	0x07D8	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 3
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON4	0x07DC	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 4
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON5	0x07E0	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 5
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON6	0x07E4	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 6
DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON7	0x07E8	W	0x00000000	SW Read DE-SKEW CS0 CONTROL 7
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON_DM	0x07F0	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL DM
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON0	0x07F4	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 0
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON1	0x07F8	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 1
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON2	0x07FC	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 2
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON3	0x0800	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 3
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON4	0x0804	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 4
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON5	0x0808	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 5
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON6	0x080C	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 6
DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON7	0x0810	W	0x00000000	SW Read DE-SKEW Left CS0 CONTROL 7
DDRPHY_SW_RD_DQS_VWML_CS1_CON0	0x0814	W	0x00000000	SW Read DQS Left Code CS1 CON0
DDRPHY_SW_RD_DQS_VWMC_CS1_CON0	0x0818	W	0x00000000	SW Read DQS Centering CS1 Code CON0

Name	Offset	Size	Reset Value	Description
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON_DM	0x0820	W	0x00000000	SW Read DE-SKEW CS1 CONTROL DM
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON0	0x0824	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 0
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON1	0x0828	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 1
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON2	0x082C	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 2
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON3	0x0830	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 3
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON4	0x0834	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 4
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON5	0x0838	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 5
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON6	0x083C	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 6
DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON7	0x0840	W	0x00000000	SW Read DE-SKEW CS1 CONTROL 7
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON_DM	0x0850	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL DM
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON0	0x0854	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 0
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON1	0x0858	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 1
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON2	0x085C	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 2
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON3	0x0860	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 3
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON4	0x0864	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 4
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON5	0x0868	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 5
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON6	0x086C	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 6
DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON7	0x0870	W	0x00000000	SW Read DE-SKEW Left CS1 CONTROL 7
DDRPHY_SW_WR_DESKEWC_CS0_CON0	0x0880	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 0
DDRPHY_SW_WR_DESKEWC_CS0_CON1	0x0884	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 1
DDRPHY_SW_WR_DESKEWC_CS0_CON2	0x0888	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 2

Name	Offset	Size	Reset Value	Description
DDRPHY_SW_WR_DESKEWC_CS0_CON3	0x088C	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 3
DDRPHY_SW_WR_DESKEWC_CS0_CON4	0x0890	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 4
DDRPHY_SW_WR_DESKEWC_CS0_CON5	0x0894	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 5
DDRPHY_SW_WR_DESKEWC_CS0_CON6	0x0898	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 6
DDRPHY_SW_WR_DESKEWC_CS0_CON7	0x089C	W	0x00000000	SW Write DE-SKEW CS0 Center CONTROL 7
DDRPHY_SW_DM_DESKEWC_CS0_CON0	0x08A0	W	0x00000000	SW Write DM DE-SKEW CS0 Center CONTROL 0
DDRPHY_SW_ECC_DESKEWC_CS0_CON0	0x08A4	W	0x00000000	SW Write ECC DE-SKEW CS0 Center CONTROL 0
DDRPHY_SW_WR_DESKEWL_CS0_CON0	0x08B0	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL0
DDRPHY_SW_WR_DESKEWL_CS0_CON1	0x08B4	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL1
DDRPHY_SW_WR_DESKEWL_CS0_CON2	0x08B8	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL2
DDRPHY_SW_WR_DESKEWL_CS0_CON3	0x08BC	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL3
DDRPHY_SW_WR_DESKEWL_CS0_CON4	0x08C0	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL4
DDRPHY_SW_WR_DESKEWL_CS0_CON5	0x08C4	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL5
DDRPHY_SW_WR_DESKEWL_CS0_CON6	0x08C8	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL6
DDRPHY_SW_WR_DESKEWL_CS0_CON7	0x08CC	W	0x00000000	SW Write DE-SKEW CS0 LEFT CONTROL7
DDRPHY_SW_WR_DM_DESKEWL_CS0_CON0	0x08D0	W	0x00000000	SW Write DM DE-SKEW CS0 LEFT CONTROL0
DDRPHY_SW_WR_ECC_DESKEWL_CS0_CON0	0x08D4	W	0x00000000	SW Write ECC DE-SKEW CS0 LEFT CONTROL0
DDRPHY_SW_WR_DESKEWC_CS1_CON0	0x08E0	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 0
DDRPHY_SW_WR_DESKEWC_CS1_CON1	0x08E4	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 1
DDRPHY_SW_WR_DESKEWC_CS1_CON2	0x08E8	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 2
DDRPHY_SW_WR_DESKEWC_CS1_CON3	0x08EC	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 3

Name	Offset	Size	Reset Value	Description
DDRPHY_SW_WR_DESKEWC_CS1_CON4	0x08F0	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 4
DDRPHY_SW_WR_DESKEWC_CS1_CON5	0x08F4	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 5
DDRPHY_SW_WR_DESKEWC_CS1_CON6	0x08F8	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 6
DDRPHY_SW_WR_DESKEWC_CS1_CON7	0x08FC	W	0x00000000	SW Write DE-SKEW CS1 Center CONTROL 7
DDRPHY_SW_WR_DM_DESKEWC_CS1_CON0	0x0900	W	0x00000000	SW Write DM DE-SKEW CS1 Center CONTROL 0
DDRPHY_SW_WR_ECC_DESKEWC_CS1_CON0	0x0904	W	0x00000000	SW Write ECC DE-SKEW CS1 Center CONTROL 0
DDRPHY_SW_ECC_DESKEWL_CS1_CON0	0x090C	W	0x00000000	SW Write ECC DE-SKEW CS1 LEFT CONTROL0
DDRPHY_SW_WR_DESKEWL_CS1_CON0	0x0910	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL0
DDRPHY_SW_WR_DESKEWL_CS1_CON1	0x0914	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL1
DDRPHY_SW_WR_DESKEWL_CS1_CON2	0x0918	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL2
DDRPHY_SW_WR_DESKEWL_CS1_CON3	0x091C	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL3
DDRPHY_SW_WR_DESKEWL_CS1_CON4	0x0920	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL4
DDRPHY_SW_WR_DESKEWL_CS1_CON5	0x0924	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL5
DDRPHY_SW_WR_DESKEWL_CS1_CON6	0x0928	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL6
DDRPHY_SW_WR_DESKEWL_CS1_CON7	0x092C	W	0x00000000	SW Write DE-SKEW CS1 LEFT CONTROL7
DDRPHY_SW_DM_DESKEWL_CS1_CON0	0x0930	W	0x00000000	SW Write DM DE-SKEW CS1 LEFT CONTROL0
DDRPHY_DVFS0_CON5	0x0934	W	0x00000040	DVFS0_CON5
DDRPHY_DVFS1_CON5	0x0938	W	0x00000040	DVFS1_CON5
DDRPHY_CAL_WR_PATTERN_CON5	0x093C	W	0x00FF00FF	Write Calibration Pattern Register 0
DDRPHY_CAL_WR_PATTERN_CON6	0x0940	W	0x00FF00FF	Write Calibration Pattern Register 1
DDRPHY_CAL_WR_PATTERN_CON7	0x0944	W	0x00FF00FF	Write Calibration Pattern Register 2
DDRPHY_CAL_WR_PATTERN_CON8	0x0948	W	0x00FF00FF	Write Calibration Pattern Register 3

Name	Offset	Size	Reset Value	Description
DDRPHY_CAL_WR_PATTERN_CON9	0x094C	W	0x00FF00FF	Write Calibration Pattern Register 0
DDRPHY_CAL_WR_PATTERN_CON10	0x0950	W	0x00FF00FF	Write Calibration Pattern Register 1
DDRPHY_CAL_WR_PATTERN_CON11	0x0954	W	0x00FF00FF	Write Calibration Pattern Register 11
DDRPHY_CAL_WR_PATTERN_CON12	0x0958	W	0x00FF00FF	Write Calibration Pattern Register 12
DDRPHY_CAL_WR_PATTERN_CON13	0x095C	W	0x00FF00FF	Write Calibration Pattern Register 13
DDRPHY_CAL_WR_PATTERN_CON14	0x0960	W	0x00FF00FF	Write Calibration Pattern Register 14
DDRPHY_CAL_WR_PATTERN_CON15	0x0964	W	0x00FF00FF	Write Calibration Pattern Register 15
DDRPHY_CAL_WR_PATTERN_CON16	0x0968	W	0x00FF00FF	Write Calibration Pattern Register 16
DDRPHY_CAL_WR_PATTERN_CON17	0x096C	W	0x00005555	Write Calibration Pattern Register 17
DDRPHY_CAL_WR_PATTERN_CON18	0x0970	W	0x00005555	Write Calibration Pattern Register 18
DDRPHY_CAL_WR_PATTERN_CON19	0x0974	W	0x00005555	Write Calibration Pattern Register 19
DDRPHY_READ_DQ_OFFSET_CTRL0	0x0978	W	0x37373737	Read DQ offset control register 0 for RANK0
DDRPHY_READ_DQ_OFFSET_CTRL1	0x097C	W	0x37373737	Read DQ offset control register 1
DDRPHY_READ_DQ_OFFSET_CTRL2	0x0980	W	0x00000037	Read DQ offset control register 2
DDRPHY_READ_DQ_OFFSET_CTRL3	0x0984	W	0x37373737	Read DQ offset control register 3
DDRPHY_READ_DQ_OFFSET_CTRL4	0x0988	W	0x37373737	Read DQ offset control register 4
DDRPHY_READ_DQ_OFFSET_CTRL5	0x098C	W	0x00000037	Read DQ offset control register 5
DDRPHY_READ_DQ_OFFSET_CTRL0_CS1	0x0990	W	0x37373737	Reserved
DDRPHY_READ_DQ_OFFSET_CTRL1_CS1	0x0994	W	0x37373737	Reserved
DDRPHY_READ_DQ_OFFSET_CTRL2_CS1	0x0998	W	0x00000037	Reserved
DDRPHY_READ_DQ_OFFSET_CTRL3_CS1	0x099C	W	0x37373737	Reserved

Name	Offset	Size	Reset Value	Description
DDRPHY_READ_DQ_OFFSET_CTRL4_CS1	0x09A0	W	0x37373737	Reserved
DDRPHY_READ_DQ_OFFSET_CTRL5_CS1	0x09A4	W	0x00000037	Reserved
DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL0	0x09A8	W	0x00000000	Write DQ DLL duty control register 0
DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL1	0x09AC	W	0x00000000	Write DQ DLL duty control register 1
DDRPHY_READ_DQ_DLINE_DUTY_CTRL0	0x09B0	W	0x00000000	DLL duty control register 0
DDRPHY_READ_DQ_DLINE_DUTY_CTRL1	0x09B4	W	0x00000000	DLL duty control register 1
DDRPHY_READ_DQ_DLINE_DUTY_CTRL2	0x09B8	W	0x00000000	DLL duty control register 2
DDRPHY_READ_DQ_DLINE_DUTY_CTRL3	0x09BC	W	0x00000000	DLL duty control register 3
DDRPHY_WRITE_DQS_DLINE_DUTY_CTRL0	0x09C0	W	0x00000000	WDQS DLL duty control register 0
DDRPHY_DQ_SEL_CTRL0	0x09C4	W	0x02492492	DQ DLL SEL control register 0
DDRPHY_DQ_SEL_CTRL1	0x09C8	W	0x02492492	DQ DLL SEL control register 1
DDRPHY_DQ_SEL_CTRL2	0x09CC	W	0x02492492	DQ DLL SEL control register 2
DDRPHY_DQ_SEL_CTRL3	0x09D0	W	0x02492492	DQ DLL SEL control register 3
DDRPHY_DQ_SEL_CTRL4	0x09D4	W	0x02492492	DQ DLL SEL control register 4
DDRPHY_DQ_SEL_CTRL5	0x09D8	W	0x02492492	DQ DLL SEL control register 5
DDRPHY_DQ_SEL_CTRL6	0x09DC	W	0x02492492	DQ DLL SEL control register 6
DDRPHY_DQ_SEL_CTRL7	0x09E0	W	0x02492492	DQ DLL SEL control register 7
DDRPHY_CK_DLINE_DUTY_CTRL0	0x09E4	W	0x00000000	CK DLL Duty control register 0
DDRPHY_IO_DUTY_CTRL0	0x09E8	W	0x2DB6DB6D	IO duty control register 0
DDRPHY_IO_DUTY_CTRL1	0x09EC	W	0x2DB6DB6D	IO duty control register 1
DDRPHY_IO_DUTY_CTRL2	0x09F0	W	0x1B6DB6DB	IO duty control register 2
DDRPHY_IO_DUTY_CTRL3	0x09F4	W	0x1B6DB6DB	IO duty control register 3
DDRPHY_IO_DUTY_CTRL4	0x09F8	W	0x00000000	IO duty control register 4
DDRPHY_IO_DUTY_CTRL5	0x09FC	W	0x0000001D	IO duty control register 5
DDRPHY_DVFS0_CON6	0x0A00	W	0x003F0000	DVFS Control Register 11
DDRPHY_DVFS1_CON6	0x0A04	W	0x003F0000	DVFS Control Register 12
DDRPHY_DQOENDESKEWCODE0	0x0A08	W	0x00000000	DVFS Control Register 12

Name	Offset	Size	Reset Value	Description
DDRPHY_DQOENDESKEWCODE1	0x0A0C	W	0x00000000	DVFS Control Register 12
DDRPHY_DQSOENDESKEWCODE	0x0A10	W	0x00000000	DVFS Control Register 12
DDRPHY_DTB	0x0A14	W	0x00000000	DTB Control Register
DDRPHY_GTCC_CON0	0x0A18	W	0x00000000	GATE Center Control Register 0
DDRPHY_RANK1_CON0	0x0A1C	W	0x00020820	Rank1 RL Register 0
DDRPHY_SCHD_CON0	0x0A20	W	0x00000040	SCHEDULER Control Register
DDRPHY_SCHD_TRAIN_CON0	0x0A24	W	0x00000000	SCHEDULER Training Enable Control Register 0
DDRPHY_SCHD_TRAIN_CON1	0x0A28	W	0x000403F5	SCHEDULER Training Enable Control Register 1
DDRPHY_SCHD_TIME_CON0	0x0A2C	W	0x005A01D2	SCHEDULER CMD Timing Parameter Register 0
DDRPHY_SCHD_TIME_CON1	0x0A30	W	0x640D1008	SCHEDULER CMD Timing Parameter Register 1
DDRPHY_SCHD_TIME_CON2	0x0A34	W	0x03C74780	SCHEDULER CMD Timing Parameter Register 2
DDRPHY_SCHD_TIME_CON3	0x0A38	W	0x00000080	SCHEDULER CMD Timing Parameter Register 3
DDRPHY_DVFS0_SCHD_TIME_CON0	0x0A3C	W	0x005A01D2	DVFS0 SCHEDULER CMD Timing Parameter Register 0
DDRPHY_DVFS0_SCHD_TIME_CON1	0x0A40	W	0x640D1008	DVFS0 SCHEDULER CMD Timing Parameter Register 1
DDRPHY_DVFS0_SCHD_TIME_CON2	0x0A44	W	0x03C74780	DVFS0 SCHEDULER CMD Timing Parameter Register 2
DDRPHY_DVFS0_SCHD_TIME_CON3	0x0A48	W	0x04000001	DVFS0 SCHEDULER CMD Timing Parameter Register 3
DDRPHY_DVFS1_SCHD_TIME_CON0	0x0A4C	W	0x005A01D2	DVFS1 SCHEDULER CMD Timing Parameter Register 0
DDRPHY_DVFS1_SCHD_TIME_CON1	0x0A50	W	0x640D1008	DVFS1 SCHEDULER CMD Timing Parameter Register 1
DDRPHY_DVFS1_SCHD_TIME_CON2	0x0A54	W	0x03C74780	DVFS1 SCHEDULER CMD Timing Parameter Register 2
DDRPHY_DVFS1_SCHD_TIME_CON3	0x0A58	W	0x04000001	DVFS1 SCHEDULER CMD Timing Parameter Register 3
DDRPHY_SCHD_DIRECT_CMD0	0x0A5C	W	0x00000000	SCHEDULER Direct CMD control 0
DDRPHY_SCHD_DIRECT_CMD1	0x0A60	W	0x00000000	SCHEDULER Direct CMD control 1
DDRPHY_SCHD_DIRECT_CMD2	0x0A64	W	0x00000000	SCHEDULER Direct CMD control 2

Name	Offset	Size	Reset Value	Description
DDRPHY_SCHD_DIRECT_CMD3	0x0A68	W	0x00000000	SCHEDULER Direct CMD control 3
DDRPHY_SCHD_DIRECT_CMD4	0x0A6C	W	0x00000000	SCHEDULER Direct CMD control 4
DDRPHY_SCHD_CMD_CON0	0x0A70	W	0x00000001	SCHEDULER Direct CMD control 5
DDRPHY_SCHD_CMD_CON1	0x0A74	W	0x00000000	SCHEDULER Direct CMD control 5
DDRPHY_SCHD_CMD_CON2	0x0A78	W	0x00000000	SCHEDULER Direct CMD control 5
DDRPHY_OP_CODE_RDC	0x0A7C	W	0x5555EEEE	OP CODE
DDRPHY_LP4_MR_OP0	0x0A80	W	0x00000000	LPDDR4 MR OPERAND 0
DDRPHY_LP4_MR_OP1	0x0A84	W	0x00000000	LPDDR4 MR OPERAND 1
DDRPHY_LP5_MR_OP0	0x0A88	W	0x00000000	LPDDR5 MR OPERAND 0
DDRPHY_LP5_MR_OP1	0x0A8C	W	0x00000000	LPDDR5 MR OPERAND 0
DDRPHY_SCHD_FSM	0x0A90	W	0x00000000	Scheduler FSM Monitor
DDRPHY_CLKMODE_CON	0x0A94	W	0x00000009	PHY CLOCK MODE_CON
DDRPHY_CASWIZZLE_CON	0x0A98	W	0x65432100	CA SWIZZLE CONFIGURATION
DDRPHY_TDLL_CON0	0x0A9C	W	0x00000000	TDLL CONFIGURATION0
DDRPHY_TDLL_CON1	0x0AA0	W	0x00000000	TDLL CONFIGURATION1
DDRPHY_TDLL_MON0_DS0	0x0AA4	W	0x00000000	TDLL MONITOR 0 for DS0
DDRPHY_TDLL_MON1_DS0	0x0AA8	W	0x00000000	TDLL MONITOR 1 for DS0
DDRPHY_TDLL_MON0_DS1	0x0AAC	W	0x00000000	TDLL MONITOR 0 for DS1
DDRPHY_TDLL_MON1_DS1	0x0AB0	W	0x00000000	TDLL MONITOR 1 for DS1
DDRPHY_DQRPARITY_LEFT_DS0	0x0AB4	W	0x00000000	DQ Rising PARITY LEFT for Data Slice 0
DDRPHY_DQRPARITY_RIGHT_DS0	0x0AB8	W	0x00000000	DQ Rising PARITY RIGHT for Data Slice 0
DDRPHY_DQFPARITY_LEFT_DS0	0x0ABC	W	0x00000000	DQ Falling PARITY LEFT for Data Slice 0
DDRPHY_DQFPARITY_RIGHT_DS0	0x0AC0	W	0x00000000	DQ Falling PARITY RIGHT for Data Slice 0
DDRPHY_DQRPARITY_LEFT_DS1	0x0AC4	W	0x00000000	DQ Rising PARITY LEFT for Data Slice 1
DDRPHY_DQRPARITY_RIGHT_DS1	0x0AC8	W	0x00000000	DQ Rising PARITY RIGHT for Data Slice 1
DDRPHY_DQFPARITY_LEFT_DS1	0x0ACC	W	0x00000000	DQ Falling PARITY LEFT for Data Slice 1

Name	Offset	Size	Reset Value	Description
DDRPHY_DQFPARITY_RIGHT_DS1	0x0AD0	W	0x00000000	DQ Falling PARITY RIGHT for Data Slice 1
DDRPHY_READCAL_URG_DS0	0x0AD4	W	0x00000000	READ CAL URG DS0
DDRPHY_READCAL_URG_DS1	0x0AD8	W	0x00000000	READ CAL URG DS1
DDRPHY_WCK2CKSYNC_CON0	0x0ADC	W	0x00000000	WCK2CK SYNC CON0
DDRPHY_WCK2CKSYNC_CON1	0x0AE0	W	0x23340758	WCK2CK SYNC CON1
DDRPHY_DVFS0_WCK2CKSYNC_CON1	0x0AE4	W	0x23340758	WCK2CK SYNC CON1 for DVFS0
DDRPHY_DVFS1_WCK2CKSYNC_CON1	0x0AE8	W	0x23340758	WCK2CK SYNC CON1 for DVFS1
DDRPHY_SCHD_CMD_GATING0	0x0AEC	W	0x00000000	SCHEDULER Direct CMD Gating 0
DDRPHY_SCHD_CMD_GATING1	0x0AF0	W	0x00000000	SCHEDULER Direct CMD Gating 1
DDRPHY_DVFS0_WCK2CKSYNC_CON0	0x0AF4	W	0x00000000	DVFS0 WCK2CK SYNC CON0
DDRPHY_DVFS1_WCK2CKSYNC_CON0	0x0AF8	W	0x00000000	DVFS1 WCK2CK SYNC CON0
DDRPHY_MDLL_CON2	0x0AFC	W	0x00000001	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ0	0x0B00	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ1	0x0B04	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ2	0x0B08	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ3	0x0B0C	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ4	0x0B10	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ5	0x0B14	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ6	0x0B18	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ7	0x0B1C	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ8	0x0B20	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ9	0x0B24	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ10	0x0B28	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ11	0x0B2C	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ12	0x0B30	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ13	0x0B34	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ14	0x0B38	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQ15	0x0B3C	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DM0	0x0B40	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DM1	0x0B44	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQS0	0x0B48	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_DQS1	0x0B4C	W	0x000199E0	TEST input port for LP4/5 I/O

Name	Offset	Size	Reset Value	Description
DDRPHY_TESTILP5_CK	0x0B50	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CA0	0x0B54	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CA1	0x0B58	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CA2	0x0B5C	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CA3	0x0B60	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CA4	0x0B64	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CA5	0x0B68	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CA6	0x0B6C	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CS0	0x0B70	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_CS1	0x0B74	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_WCK0	0x0B78	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_TESTILP5_WCK1	0x0B7C	W	0x000199E0	TEST input port for LP4/5 I/O
DDRPHY_DQSDUTY_CON0	0x0B80	W	0x00000000	DQS DUTY CONFIGURATION 0
DDRPHY_DQSDUTY_CON1	0x0B84	W	0x00000000	DQS DUTY CONFIGURATION 1
DDRPHY_DQSDUTY_CON2	0x0B88	W	0x00000000	DQS DUTY CONFIGURATION 2
DDRPHY_DQSDUTY_CON3	0x0B8C	W	0x00000000	DQS DUTY CONFIGURATION 3
DDRPHY_DQSDUTY_CON4	0x0B90	W	0x00000000	DQS DUTY CONFIGURATION 4
DDRPHY_DQSDUTY_CON5	0x0B94	W	0x00000000	DQS DUTY CONFIGURATION 5
DDRPHY_DQSDUTY_CON6	0x0B98	W	0x00000000	DQS DUTY CONFIGURATION 6
DDRPHY_DQSDUTY_CON7	0x0B9C	W	0x00000000	DQS DUTY CONFIGURATION 7
DDRPHY_MON_RCNT0	0x0BA0	W	0x00000000	MONITOR RSTN 0
DDRPHY_MON_RCNT1	0x0BA4	W	0x00000000	MONITOR RSTN 1
DDRPHY_MON_RCNT2	0x0BA8	W	0x00000000	MONITOR RSTN 2
DDRPHY_MON_RCNT3	0x0BAC	W	0x00000000	MONITOR RSTN 3
DDRPHY_CMD_DESKEWC_CODE0	0x0BB0	W	0x00000000	CMD DE-SKEW CENTER CODE
DDRPHY_CMD_DESKEWC_CODE1	0x0BB4	W	0x00000000	CMD DE-SKEW CENTER CODE
DDRPHY_CMD_DESKEWC_CODE2	0x0BB8	W	0x00000000	CMD DE-SKEW CENTER CODE
DDRPHY_CMD_DESKEWC_CODE3	0x0BBC	W	0x00000000	CMD DE-SKEW CENTER CODE
DDRPHY_CMD_DESKEWC_CODE4	0x0BC0	W	0x00000000	CMD DE-SKEW CENTER CODE
DDRPHY_CBT_CAL_STAT0	0x0BC4	W	0x00000000	CBT CAL STATUS
DDRPHY_CMD_LEFT_CODE0	0x0BC8	W	0x00000000	CMD LEFT CODE
DDRPHY_CMD_LEFT_CODE1	0x0BCC	W	0x00000000	CMD LEFT CODE
DDRPHY_CMD_LEFT_CODE2	0x0BD0	W	0x00000000	CMD LEFT CODE
DDRPHY_CMD_LEFT_CODE4	0x0BD8	W	0x00000000	CMD LEFT CODE

Name	Offset	Size	Reset Value	Description
DDRPHY_CMD_RIGHT_CODE0	0x0BDC	W	0x00000000	CMD RIGHT CODE
DDRPHY_CMD_RIGHT_CODE1	0x0BE0	W	0x00000000	CMD RIGHT CODE
DDRPHY_CMD_RIGHT_CODE2	0x0BE4	W	0x00000000	CMD RIGHT CODE
DDRPHY_CMD_RIGHT_CODE4	0x0BEC	W	0x00000000	CMD RIGHT CODE
DDRPHY_DVFS0_CLKMODE_CON	0x0BF0	W	0x00000009	PHY CLOCK MODE_CON for DVFS0
DDRPHY_DVFS1_CLKMODE_CON	0x0BF4	W	0x00000009	PHY CLOCK MODE_CON for DVFS1
DDRPHY_DVFS0_DCC_CON0	0x0BF8	W	0x00000000	DVFS0 DCC CONFIGURATION
DDRPHY_DVFS1_DCC_CON0	0x0BFC	W	0x00000000	DVFS1 DCC CONFIGURATION
DDRPHY_PTC_CON0	0x0C00	W	0x26770000	PTC CONFIGURATION 0
DDRPHY_PTC_CON1	0x0C04	W	0x00000011	PTC CONFIGURATION 1
DDRPHY_PTC_CON2	0x0C08	W	0x10008080	PTC CONFIGURATION 2
DDRPHY_PTC_CON3	0x0C0C	W	0x00000000	PTC CONFIGURATION 3
DDRPHY_PTC_CON4	0x0C10	W	0x00000000	PTC CONFIGURATION 4
DDRPHY_PTC_CON5	0x0C14	W	0x00000000	PTC CONFIGURATION 5
DDRPHY_PTC_CON6	0x0C18	W	0x02021100	PTC CONFIGURATION 6
DDRPHY_PTC_CON7	0x0C1C	W	0x00FF00FF	PTC CONFIGURATION 7
DDRPHY_PTC_CON8	0x0C20	W	0x00FF00FF	PTC CONFIGURATION 8
DDRPHY_PTC_CON9	0x0C24	W	0x00FF00FF	PTC CONFIGURATION 9
DDRPHY_PTC_CON10	0x0C28	W	0x00FF00FF	PTC CONFIGURATION 10
DDRPHY_PTC_CON11	0x0C2C	W	0x80000000	PTC CONFIGURATION 11
DDRPHY_PTC_CON12	0x0C30	W	0x00000000	PTC CONFIGURATION 12
DDRPHY_PTC_CON13	0x0C34	W	0x00000000	PTC CONFIGURATION 13
DDRPHY_PTC_CON14	0x0C38	W	0x00000000	PTC CONFIGURATION 14
DDRPHY_PTC_CON15	0x0C3C	W	0x00000000	PTC CONFIGURATION 15
DDRPHY_PTC_CON16	0x0C40	W	0x00000000	PTC CONFIGURATION 16
DDRPHY_PTC_CON17	0x0C44	W	0x00000000	PTC CONFIGURATION 17
DDRPHY_PTC_CON18	0x0C48	W	0x00000000	PTC CONFIGURATION 18
DDRPHY_PTC_CON19	0x0C4C	W	0x00000000	PTC CONFIGURATION 19
DDRPHY_PTC_CON20	0x0C50	W	0x00000000	PTC CONFIGURATION 20
DDRPHY_PTC_CON21	0x0C54	W	0x00000000	PTC CONFIGURATION 21
DDRPHY_PTC_CON22	0x0C58	W	0x00000000	PTC CONFIGURATION 22
DDRPHY_Periodic_ZQ_CON	0x0C70	W	0x000403F5	Periodic ZQ control Register
DDRPHY_PRBS_LEFT_MARGIN_DQ0	0x0D00	W	0x00000000	PRBS LEFT MARGIN FOR DQ0

Name	Offset	Size	Reset Value	Description
DDRPHY_PRBS_RIGHT_MARGIN_DQ0	0x0D04	W	0x00000000	PRBS RIGHT MARGIN FOR DQ0
DDRPHY_PRBS_LEFT_MARGIN_DQ1	0x0D08	W	0x00000000	PRBS LEFT MARGIN FOR DQ1
DDRPHY_PRBS_RIGHT_MARGIN_DQ1	0x0D0C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ1
DDRPHY_PRBS_LEFT_MARGIN_DQ2	0x0D10	W	0x00000000	PRBS LEFT MARGIN FOR DQ2
DDRPHY_PRBS_RIGHT_MARGIN_DQ2	0x0D14	W	0x00000000	PRBS RIGHT MARGIN FOR DQ2
DDRPHY_PRBS_LEFT_MARGIN_DQ3	0x0D18	W	0x00000000	PRBS LEFT MARGIN FOR DQ3
DDRPHY_PRBS_RIGHT_MARGIN_DQ3	0x0D1C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ3
DDRPHY_PRBS_LEFT_MARGIN_DQ4	0x0D20	W	0x00000000	PRBS LEFT MARGIN FOR DQ4
DDRPHY_PRBS_RIGHT_MARGIN_DQ4	0x0D24	W	0x00000000	PRBS RIGHT MARGIN FOR DQ4
DDRPHY_PRBS_LEFT_MARGIN_DQ5	0x0D28	W	0x00000000	PRBS LEFT MARGIN FOR DQ5
DDRPHY_PRBS_RIGHT_MARGIN_DQ5	0x0D2C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ5
DDRPHY_PRBS_LEFT_MARGIN_DQ6	0x0D30	W	0x00000000	PRBS LEFT MARGIN FOR DQ6
DDRPHY_PRBS_RIGHT_MARGIN_DQ6	0x0D34	W	0x00000000	PRBS RIGHT MARGIN FOR DQ6
DDRPHY_PRBS_LEFT_MARGIN_DQ7	0x0D38	W	0x00000000	PRBS LEFT MARGIN FOR DQ7
DDRPHY_PRBS_RIGHT_MARGIN_DQ7	0x0D3C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ7
DDRPHY_PRBS_LEFT_MARGIN_DQ8	0x0D40	W	0x00000000	PRBS LEFT MARGIN FOR DQ8
DDRPHY_PRBS_RIGHT_MARGIN_DQ8	0x0D44	W	0x00000000	PRBS RIGHT MARGIN FOR DQ8
DDRPHY_PRBS_LEFT_MARGIN_DQ9	0x0D48	W	0x00000000	PRBS LEFT MARGIN FOR DQ9
DDRPHY_PRBS_RIGHT_MARGIN_DQ9	0x0D4C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ9
DDRPHY_PRBS_LEFT_MARGIN_DQ10	0x0D50	W	0x00000000	PRBS LEFT MARGIN FOR DQ10
DDRPHY_PRBS_RIGHT_MARGIN_DQ10	0x0D54	W	0x00000000	PRBS RIGHT MARGIN FOR DQ10

Name	Offset	Size	Reset Value	Description
DDRPHY_PRBS_LEFT_MARGIN_DQ11	0x0D58	W	0x00000000	PRBS LEFT MARGIN FOR DQ11
DDRPHY_PRBS_RIGHT_MARGIN_DQ11	0x0D5C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ11
DDRPHY_PRBS_LEFT_MARGIN_DQ12	0x0D60	W	0x00000000	PRBS LEFT MARGIN FOR DQ12
DDRPHY_PRBS_RIGHT_MARGIN_DQ12	0x0D64	W	0x00000000	PRBS RIGHT MARGIN FOR DQ12
DDRPHY_PRBS_LEFT_MARGIN_DQ13	0x0D68	W	0x00000000	PRBS LEFT MARGIN FOR DQ13
DDRPHY_PRBS_RIGHT_MARGIN_DQ13	0x0D6C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ13
DDRPHY_PRBS_LEFT_MARGIN_DQ14	0x0D70	W	0x00000000	PRBS LEFT MARGIN FOR DQ14
DDRPHY_PRBS_RIGHT_MARGIN_DQ14	0x0D74	W	0x00000000	PRBS RIGHT MARGIN FOR DQ14
DDRPHY_PRBS_LEFT_MARGIN_DQ15	0x0D78	W	0x00000000	PRBS LEFT MARGIN FOR DQ15
DDRPHY_PRBS_RIGHT_MARGIN_DQ15	0x0D7C	W	0x00000000	PRBS RIGHT MARGIN FOR DQ15
DDRPHY_PRBS_LEFT_MARGIN_DM0	0x0D80	W	0x00000000	PRBS LEFT MARGIN FOR DM0
DDRPHY_PRBS_RIGHT_MARGIN_DM0	0x0D84	W	0x00000000	PRBS RIGHT MARGIN FOR DM0
DDRPHY_PRBS_LEFT_MARGIN_DM1	0x0D88	W	0x00000000	PRBS LEFT MARGIN FOR DM1
DDRPHY_PRBS_RIGHT_MARGIN_DM1	0x0D8C	W	0x00000000	PRBS RIGHT MARGIN FOR DM1
DDRPHY_WR_BYTE0_CYC_CS0_CODE	0x0DC0	W	0x00000000	WRITE BYTE0 CYCLE CS0 CODE
DDRPHY_WR_BYTE1_CYC_CS0_CODE	0x0DC4	W	0x00000000	WRITE BYTE1 CYCLE CS0 CODE
DDRPHY_WR_BYTE0_CYC_CS1_CODE	0x0DC8	W	0x00000000	WRITE BYTE0 CYCLE CS1 CODE
DDRPHY_WR_BYTE1_CYC_CS1_CODE	0x0DCC	W	0x00000000	WRITE BYTE1 CYCLE CS1 CODE
DDRPHY_SW_WR_BYTE0_CYC_CS0_CODE	0x0DD0	W	0x00000000	SW WRITE BYTE0 CYCLE CS0 CODE
DDRPHY_SW_WR_BYTE1_CYC_CS0_CODE	0x0DD4	W	0x00000000	SW WRITE BYTE1 CYCLE CS0 CODE
DDRPHY_SW_WR_BYTE0_CYC_CS1_CODE	0x0DD8	W	0x00000000	SW WRITE BYTE0 CYCLE CS1 CODE

Name	Offset	Size	Reset Value	Description
DDRPHY_SW_WR_BYTE1_CYC_CS1_CODE	0x0DDC	W	0x00000000	SW WRITE BYTE1 CYCLE CS1 CODE
DDRPHY_WCKOSC_CON0	0x0DE0	W	0x04373F00	WCKOSC_CON0
DDRPHY_WCKOSC_CON1	0x0DE4	W	0x00000182	WCKOSC_CON1
DDRPHY_WCKOSC_CON2	0x0DE8	W	0x00010001	WCKOSC_CON2
DDRPHY_WCKOSC_CON3	0x0DEC	W	0x80000000	WCKOSC_CON3
DDRPHY_DVFS0_WCKOSC_CON0	0x0DF0	W	0x04373F00	DVFS0_WCKOSC_CON0
DDRPHY_DVFS1_WCKOSC_CON0	0x0DF4	W	0x04373F00	DVFS1_WCKOSC_CON0
DDRPHY_WRTRN_PARA_CON0	0x0DF8	W	0x01200316	WRTRN_PARA_CON0
DDRPHY_DVFS0_WRTRN_PARA_CON0	0x0DFC	W	0x01200316	DVFS0_WRTRN_PARA_CON0
DDRPHY_DVFS1_WRTRN_PARA_CON0	0x0E00	W	0x01200316	DVFS1_WRTRN_PARA_CON0
DDRPHY_DFI_LP_CON0	0x0E04	W	0x00002322	DFI_LP_CON0
DDRPHY_LOCK_CHECK_CON	0x0E08	W	0x00007104	dfi_init_complete control with Lock check
DDRPHY_DFI_RDDATA0	0x0E10	W	0x00000000	dfi_rddata_burst0
DDRPHY_DFI_RDDATA1	0x0E14	W	0x00000000	dfi_rddata_burst1
DDRPHY_DFI_RDDATA2	0x0E18	W	0x00000000	dfi_rddata_burst2
DDRPHY_DFI_RDDATA3	0x0E1C	W	0x00000000	dfi_rddata_burst3
DDRPHY_DFI_RDDATA4	0x0E20	W	0x00000000	dfi_rddata_burst4
DDRPHY_DFI_RDDATA5	0x0E24	W	0x00000000	dfi_rddata_burst5
DDRPHY_DFI_RDDATA6	0x0E28	W	0x00000000	dfi_rddata_burst6
DDRPHY_DFI_RDDATA7	0x0E2C	W	0x00000000	dfi_rddata_burst7
DDRPHY_DFI_RDDATA_DM	0x0E30	W	0x00000000	dfi_rddata_dm_burst
DDRPHY_LP5_MR_OP2	0x0E34	W	0xC6BBC6BB	LP5_MR_OP2
DDRPHY_DVFS0_LP5_MR_OP2	0x0E38	W	0xC6BBC6BB	DVFS0_LP5_MR_OP2
DDRPHY_DVFS1_LP5_MR_OP2	0x0E3C	W	0xC6BBC6BB	DVFS1_LP5_MR_OP2
DDRPHY_PHYUPD_PARA_CON0	0x0E40	W	0x0000103F	PHYUPD_PARA_CON0
DDRPHY_DVFS0_PHYUPD_PARA_CON0	0x0E44	W	0x0000103F	DVFS0_PHYUPD_PARA_CON0
DDRPHY_DVFS1_PHYUPD_PARA_CON0	0x0E48	W	0x0000103F	DVFS1_PHYUPD_PARA_CON0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.4 Detail Registers Description

DDRPHY_GNR_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x1	ctrl_upd_time It controls when DLL is updated. Clock period information from Master DLL will be updated to Slave DLLs by DLL update. 2'b00: Update always. 2'b01: To update depending on "ctrl_flock". 2'b10: To update periodically with interval defined by ctrl_upd_interval. 2'b11: Don't update DLL.
29:28	RW	0x0	ctrl_upd_range It decides how many differences between the new lock value and the current lock value which is used in Slave-DLL is needed for updating lock value. upd_range_ext = 2'b00 (default) 2'b00: Update when difference is greater than 0 tFS. 2'b01: Update when difference is greater than 3 tFS. 2'b10: Update when difference is greater than 7 tFS. 2'b11: Update when difference is greater than 15 tFS. upd_range_ext = 2'b01 2'b00: Update when difference is greater than 5 tFS. 2'b01: Update when difference is greater than 9 tFS. 2'b10: Update when difference is greater than 11 tFS. 2'b11: Update when difference is greater than 13 tFS. upd_range_ext = 2'b10 2'b00: Update when difference is greater than 17 tFS. 2'b01: Update when difference is greater than 19 tFS. 2'b10: Update when difference is greater than 21 tFS. 2'b11: Update when difference is greater than 23 tFS. upd_range_ext = 2'b11 2'b00: Update when difference is greater than 25 tFS. 2'b01: Update when difference is greater than 27 tFS. 2'b10: Update when difference is greater than 29 tFS. 2'b11: Update when difference is greater than 31 tFS.
27	RW	0x0	ctrl_twpst Write postamble length control. Vendor specific option. 1'b0: 0.5tCK 1'b1: 1.5tCK
26	RW	0x1	ctrl_dfdqs DQS I/O Receiver mode setting. 1'b0: Single-ended DQS (io_dqs_se = 2'b11) 1'b1: Differential DQS (io_dqs_se =2'b00)
25:24	RW	0x0	ctrl_ddr_mode 2'b00: LPDDR4 2'b10: LPDDR5 Others: Reserved
23:21	RW	0x0	ctrl_fnc_fb FNC Feedback mode setting. 3'b000: FNC feedback disable 3'b010: External FNC feedback mode 3'b011: Internal FNC feedback mode Others: Reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	dvfs_gate_upd_mode Gate information update mode for DVFS pause. 1'b0: Gate delay information will be restored to the initial training result whenever DVFS pause occurs. 1'b1: Gate delay information will not be restore to the initial training result if DVFS pause occurs without changing dvfs_mode and clock frequency in order to make DLL relock.
19	RW	0x0	wdqs_oen_mode Write DQS Drive state control mode. 1'b0: DQS will be driven except for the read duration. ds_io_pd should be set to 1. 1'b1: DQS will be driven only for write duration.
18	RW	0x0	write_se_dqs Single ended mode enable for write DQS. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for Write DQS. 1'b1: Single ended mode is enabled for Write DQS. Caution: write_se_ck should be enabled using write_se_dqs in LPDDR4.
17	RW	0x0	write_se_ck Single ended mode enable for CK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for CK. 1'b1: Single ended mode is enabled for CK. Caution: write_se_dqs should be enabled using write_se_ck in LPDDR4. Caution: write_se_wck should be enabled using write_se_ck in LPDDR5.
16	RW	0x0	ctrl_pd_width PD (io_dqs_pd, io_dq_pd, io_dm_pd) signal width control. 1'b0: Same width with READ (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read). 1'b1: Longer than READ.
15	RW	0x0	ctrl_twpre Write preamble length control. Refer to DRAM spec for write preamble definition. 1'b0: 2 tCK for higher speeds 1'b1: 1 tCK for lower speeds
14	RW	0x1	ctrl_otf_bl On-the-fly BL enable 1'b0: On-the-fly BL is disabled. 1'b1: On-the-fly BL is enabled.
13:8	RW	0x10	ctrl_bstlen Fixed Burst Length(BL). This field is ignored when ctrl_otf_bl is 1'b1. 6'h10: BL = 16 6'h20: BL = 32 Others: Reserved
7	RW	0x0	ctrl_ckdis Deprecated

Bit	Attr	Reset Value	Description
6	RW	0x0	ctrl_cmosrcv This field controls the input mode of I/O. 1'b0: Differential receiver mode for high speed operation (io_dqs_cmosrcv = 2'b00, io_dm_cmosrcv = 2'b00, io_dq_cmosrcv = 16'h0000). 1'b1: CMOS receiver mode for low speed operation (under 400MHz) (io_dqs_cmosrcv = 2'b11, io_dm_cmosrcv = 2'b11, io_dq_cmosrcv = 16'hffff).
5:0	RW	0x11	ctrl_rdlat_rank0 Read Latency(RL) for RANK0

DDRPHY_CAL_CON0
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RW	0x1	cs_default Default dfi_wrdata_cs setting. This field will set the default value for internally generated dfi_wrdata_cs, which will be used when wr_per_rank_en is disabled.
29	RW	0x1	wr_per_rank_en Per-rank write DQ/DM DLL control enable. If this field is enabled, Write training should be done for both rank0 and rank1 and dfi_wrdata_cs should be properly controlled by the memory controller. If this field is disabled, dfi_wrdata_cs will be controlled internally by PHY, and it will be fixed to the default chip select, which is specified in cs_default. 1'b1: Write DQ DLL code will be controlled per rank. 1'b0: Write DQ DLL code will be fixed for rank-to-rank write.
28	RW	0x1	rd_per_rank_en Per-rank read DQS/DQ/DM DLL control enable. If this field is enabled, Read training should be done for both rank0 and rank1. 1'b1: Read DQS/DQ/DM DLL code will be controlled per rank. 1'b0: Read DQS/DQ/DM DLL code will be fixed for rank-to-rank read.
27	RW	0x1	gate_rdchk_en Gate training read check enable control signal. If this is enabled, PHY will check if the read data from DRAM caused by MPC-RD DQ Calibration from the memory controller is correct or not while finding the read DQS location during gate training. 1'b1: Read check is enabled during gate training. 1'b0: Read check is disabled during gate training.
26	RW	0x0	dvfs_wr_train_en DVFS write training enable. If enabled, write training initiation with dfi_lvl_periodic=0 will be interpreted as DVFS write training. During the initial training, dvfs_wr_train_en should be 0. 1'b1: DVFS write training enabled. Training logic will find tDQS2DQ variation. The start point is determined by dvfs_wr_start_adj. Training will finish when the valid data widow edge is found. 1'b0: DVFS write training disabled.

Bit	Attr	Reset Value	Description
25:24	RW	0x0	avg_window_size Average window size for DLL lock value average. 2'b00: Lock value will be sampled 32 times and averaged(Default). 2'b01: Lock value will be sampled 16 times and averaged. 2'b10: Lock value will be sampled 8 times and averaged. 2'b11: Lock value will be sampled 64 times and averaged.
23	RW	0x1	freq_offset_en Frequency offset calculation enable. When enabled, PHY calculates the required offset based on the frequency information to get more margins at the lower frequencies. It should be set to 1'b0 if DLL is off because the frequency compensation offset will be calculated using the current DLL lock value. Frequency offset will be applied to write DQ/DM and read DQS. 1'b1: Enable frequency offset calculation. 1'b0: Disable frequency offset calculation.
22	RW	0x0	cal_vtc_en VT compensation enable. DLL Delay is updated depending on the latest Master DLL lock value whenever "dfi_ctrlupd_req" or "dfi_phyupd_req" is issued if cal_vtc_en=1. It compensates On-chip VT variation. 1'b1: VT compensation enabled. 1'b0: VT compensation disabled.
21	RW	0x0	ca_swap_mode_dis CA swap disable for LPDDR4 HW CAL CBT mode
20	RW	0x1	wck_vtc_en VT compensation enable for WCK. DLL Delay is updated depending on the latest Master DLL lock value whenever "dfi_ctrlupd_req" or "dfi_phyupd_req" is issued if wck_vtc_en=1. It compensates On-chip VT variation. 1'b1: VT compensation enabled. 1'b0: VT compensation disabled. cal_vtc_en should be 1 for use wck_vtc_en = 1.
19	RW	0x0	Reserved0 Reserved
18	RW	0x1	rdtrn_dbi_cal_en DBI enable for LPDDR4/5 read training. 1'b0: DBI is not calibrated during read training. 1'b1: DBI is calibrated during read training.
17	RW	0x1	wrtrn_dbi_cal_en DBI enable for LPDDR4/5 write training. Set to 0 if Data Mask, Write DBI and Read DBI are all disabled at DRAM. Otherwise, it should be set to 1. 1'b0: DBI is not calibrated during write training. 1'b1: DBI is calibrated during write training.
16	RO	0x0	wrlvl_resp Response after Write Leveling is done.
15	RW	0x0	LP5_16bank_mode LP5 16bank mode 1'b1: 16bank mode 1'b0: 4bg/4bank mode 8 bank mode don't care about this field.

Bit	Attr	Reset Value	Description
14:13	RW	0x0	ctrl_upd_interval DLL update interval. DLL update is done periodically with interval defined by ctrl_upd_interval when ctrl_upd_time = 2'b10. 2'b00: 2us 2'b01: 4us 2'b10: 6us 2'b11: 8us
12:11	RW	0x0	lock_sample_condition Lock value sampling condition setting for lock value averaging. Applied when lock_averge_en = 1. 2'b00: Lock value will be sampled if ctrl_flock = 1. 2'b01: Lock value will be sampled if ctrl_clock = 1. 2'b10: Lock value will be sampled if ctrl_locked = 1.
10:9	RW	0x3	wrtrn_dqs_edge_en DQS edge enable for initial write training. This field can be changed to find the effect of duty cycle error on the initial write training result for debug purpose. For normal operation, use the default value (2'b11). 2'b11: DQ/DM captured at the rising and falling edge of DQS will be used for the initial write training (Default). 2'b01: DQ/DM captured only at the rising edge of DQS will be used for the initial write training. 2'b10: DQ/DM captured only at the falling edge of DQS will be used for the initial write training. 2'b00: Do not use.
8	RW	0x0	wrlvl_start Write Leveling start. It can be enabled when wrlvl_mode = 1. It should be disabled after write leveling response (wrlvl_resp) is asserted.
7:6	RW	0x3	rdlvl_dqs_edge_en DQS edge enable for initial read training. This field can be changed to find the effect of duty cycle error on the initial read training result for debug purpose. For normal operation, use the default value (2'b11). 2'b11: DQ/DM captured at the rising and falling edge of DQS will be used for the initial read training (Default). 2'b01: DQ/DM captured only at the rising edge of DQS will be used for the initial read training. 2'b10: DQ/DM captured only at the falling edge of DQS will be used for the initial read training. 2'b00: Do not use.
5	RW	0x0	wr_cal_mode If it is enabled, PHY will use "SDLL Code" which is calculated during Write training. If disabled, PHY will use "SDLL Code" which is calculated from Master DLL(T/4).
4	RW	0x0	lock_average_en Lock value average enable. If enabled, moving average will be applied to DLL lock value to remove lock value deviation due to power noise. 1'b0: DLL lock value will not be averaged. (Default) 1'b1: DLL lock value will be sampled and averaged. The number of lock value that will be averaged is defined in avg_window_size.

Bit	Attr	Reset Value	Description
3	RW	0x0	rd_cal_mode When rd_cal_mode=1, PHY will use "SDLL Code" which is calculated during Read training. If disabled, PHY will use "SDLL Code" which is calculated from Master DLL (T/4).
2	RW	0x0	ca_cal_mode CBT Mode Enable. For LPDDR4, if ca_cal_mode = 1 and cbt_vref_dqs_en[N] = 1, DQS/DQ/DM pad for Byte N will be set to driver mode. For LPDDR5, if ca_cal_mode = 1 and cbt_bit_dq_en[n] = 0, DQ pad for bit n will be set to driver mode.
1	RW	0x0	gate_cal_mode Gate training mode enable. If gate training is used, this value should be high during operation. 1'b1: PHY will apply gate cycle/offset result(GT_VWMC*_cs0/cs1 and GT_CYC*_cs0/cs1) from gate training to gate signal. 1'b0: PHY will apply ctrl_shiftc to gate signal.
0	RW	0x0	wrlvl_mode Write leveling mode enable. If write leveling is configured(wrlvl_mode = 1), DQ/DM pad will be set to receiver mode (io_dq_en=16'hFFFF, io_dm_en=2'b11) and DQS pad will be set to driver mode (io_pdqs_en=2'b00, io_ndqs_en=2'b00).

DDRPHY_CAL_CON1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RW	0x2	wrtrn_pass_adj This field controls how many times write should be operated well to determine if it goes into VWP(Valid Window Period) or not. For write training, PHY decides that DQ is in the valid window if data check passes *4 times consecutively. The valid range is 0x1~0xF. 4'h1: PHY decides that DQ is in the valid window if data check passes 4 time. 4'h2: PHY decides that DQ is in the valid window if data check passes 8 times consecutively. 4'h3: PHY decides that DQ is in the valid window if data check passes 12 times consecutively. . . 4'hE: PHY decides that DQ is in the valid window if data check passes 56 times consecutively. 4'hF: PHY decides that DQ is in the valid window if data check passes 60 times consecutively.
27	RW	0x0	dfi_error_en Dfi error enable
26:20	RW	0x01	rdlvl_incr_adj Initial training step size (default: 7'h1, fine step delay). It should be smaller than 7'b0F. This is valid only for write/read DQ calibration, gate training and write leveling. bit[26:25]=2'b00: The step value will be "rdlvl_incr_adj[4:0]". bit[26:25]=2'b01: The step value will be "T/4". bit[26:25]=2'b10: The step value will be "T/8". bit[26:25]=2'b11: The step value will be "T/64".

Bit	Attr	Reset Value	Description
19:16	RW	0x4	rdlvl_pass_adj This field controls how many times "Read" should be operated well to determine if it goes into VWP(Valid Window Period) or not. 4'h1: PHY decides that DQS is in the valid window if data check passes 2 time. 4'h2: PHY decides that DQS is in the valid window if data check passes 4 times consecutively. 4'h3: PHY decides that DQS is in the valid window if data check passes 6 times consecutively. 4'h4: PHY decides that DQS is in the valid window if data check passes 8 times consecutively. 4'h5: PHY decides that DQS is in the valid window if data check passes 10 times consecutively. 4'h6: PHY decides that DQS is in the valid window if data check passes 12 times consecutively. 4'h7: PHY decides that DQS is in the valid window if data check passes 14 times consecutively. Others: Do not use.
15:14	RW	0x0	ctrl_rpost_opt LPDDR5 read post-amble toggle option. Refer to read post-amble description in DRAM spec. 2'b00: Read post-amble = 0.5tWCK static. 2'b01: Read post-amble = 2.5tWCK static. 2'b10: Read post-amble = 4.5tWCK static.
13:7	RW	0x40	glvl_periodic_incr_adj Periodic (or short) gate training step size. It should be smaller than 7'h1F. Default value is 7'b1000000(T/4). bit[13:12]=2'b00: The step value will be "glvl_periodic_incr_adj[4:0]". bit[13:12]=2'b01: The step value will be "T/2". bit[13:12]=2'b10: The step value will be "T/4" (default). bit[13:12]=2'b11: The step value will be "T/8". bit[13:7]=7'h00: The step value will be "T/16".
6:0	RW	0x01	rdlvl_periodic_incr_adj Periodic (or short) training step size. It decides the step value of delay line to increase during periodic read and write training. It should be smaller than 7'b0F. Default value is 7'h40(T/32). bit[6:5]=2'b00: The step value will be "rdlvl_periodic_incr_adj[4:0]". bit[6:5]=2'b01: The step value will be "T/16". bit[6:5]=2'b10: The step value will be "T/32" (default). bit[6:5]=2'b11: The step value will be "T/64".

DDRPHY_CAL_CON2

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	ctrl_rpre_opt Read pre-amble toggle option. Refer to read pre-amble description in DRAM spec. For LPDDR4: 1'b1: Read pre-amble = 2nCK toggle. 1'b0: Read pre-amble = 2nCK static. For LPDDR5: 1'b1: Read pre-amble = 2tWCK static + 2tWCK toggle. 1'b0: Read pre-amble = 2tWCK static.
30	RW	0x1	ctrl_rodt_disable Read ODT(On-Die-Termination) disable signal. 1'b1: Read ODT disabled. Drive ctrl_read_p* to 0. If using LPDDR4, ctrl_read_p* will be always 0 by enabling this field. Io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are low. 1'b0: Read ODT enabled. Drive ctrl_read_p* normally. Io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are high only for read duration.
29	RW	0x0	ctrl_shgate This field controls the gate control signal. 1'b0: Gate signal length = "burst length / 2" + N (Apply when DQS Pull-Down is enabled. N is determined by ctrl_gateduradj). 1'b1: Gate signal length = "burst length / 2" ? 1 For LPDDR4, MR1 should be programmed so that read Pre-amble is 2nCK static and read Post-amble is 0.5tCK when shgate is 'h0.
28	RW	0x0	ctrl_gt_fine_disable Gate fine training enable for periodic gate training.
27:24	RW	0x2	ctrl_gateduradj It adjusts the duration cycle of "ctrl_gate" on a clock cycle base. MSB(bit3) controls direction: 1'b1: Subtract duration 1'b0: Add duration Bit[2:0] set duration value.
23:20	RW	0x0	ctrl_gateadj It adjusts the enable time of "ctrl_gate" on a clock cycle base. The reference point is at the end of RL. MSB(bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. When gate training is enabled, it configures the start point of gate training. If gate training is not enabled, it will be used to manually control the position of ctrl_gate.
19:16	RW	0x0	ctrl_readduradj It adjusts the duration cycle of "ctrl_read" on a clock cycle base. "ctrl_read" is the read odt control signal within PHY. MSB(bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.

Bit	Attr	Reset Value	Description
15:12	RW	0x1	ctrl_readadj It adjusts the enable time of "ctrl_read" on a clock cycle base. The reference point is at the end of RL. MSB(bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay. It determines the start cycle of high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.
11	RW	0x0	ctrl_readduradj_ext Default value is 0. This field is used for extend control range of ctrl_readduradj value. ctrl_readduradj_ext = 1'b0 (default) => Non Extended ctrl_readduradj_ext = 1'b1 => ctrl_readduradj[2:0] + 'h8
10	RW	0x0	ctrl_readadj_ext Default value is 0. This field is used for extend control range of ctrl_readadj value. ctrl_readadj_ext = 1'b0 (default) => Non Extended ctrl_readadj_ext = 1'b1 => ctrl_readadj[2:0] + 'h8
9:8	RW	0x3	ctrl_maskdur_adj Single-ended NDQS input glitch masking duration adjustment during read ODT enable timing. 2'b11: SE NDQS Glitch 3.5tCK Masking(default). 2'b10: SE NDQS Glitch 4.5tCK Masking. 2'b00: SE NDQS Glitch 5.5tCK Masking.
7	RW	0x0	ctrl_long_gate_train_mode Gate training mode by long gate(shgate = 0)
6:4	RW	0x0	glvl_start_adj Gate training start point adjustment. This field adjusts the initial code provided to the gate delay line at the beginning of periodic gate training. bit[6:4]=3'b000: The start point code is -T from the first DQS risinge edge. bit[6:4]=3'b001: The start point code is -7T/8 from the first DQS risinge edge. bit[6:4]=3'b010: The start point code is -6T/8 from the first DQS risinge edge. bit[6:4]=3'b011: The start point code is -5T/8 from the first DQS risinge edge. bit[6:4]=3'b100: The start point code is -4T/8 from the first DQS risinge edge. bit[6:4]=3'b101: The start point code is -3T/8 from the first DQS risinge edge. bit[6:4]=3'b110: The start point code is -2T/8 from the first DQS risinge edge. bit[6:4]=3'b111: The start point code is -T/8 from the first DQS risinge edge.

Bit	Attr	Reset Value	Description
3	RW	0x0	ctrl_gateduradj_ext Default value is 0. This field is used for extend control range of ctrl_gateduradj value. ctrl_gateduradj_ext = 1'b0 (default) => Non Extended ctrl_gateduradj_ext = 1'b1 => ctrl_gateduradj[2:0] + 'h8
2	RW	0x0	ctrl_gateadj_ext Default value is 0. This field is used for extend control range of ctrl_gateadj value. ctrl_gateadj_ext = 1'b0 (default) => Non Extended ctrl_gateadj_ext = 1'b1 => ctrl_gateadj[2:0] + 'h8
1:0	RW	0x0	ctrl_read_width The default is 1'b0. We strongly recommend that it should have one more idle cycle between read and write because the variation of data arrival time during read can be greater than 1 cycle. If it is 1'b1, the package and board should be carefully optimized with a short length and it should be used at the low frequency. Please refer to. 1'b0: Termination on (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are driven high) period is (BL/2+1.5) cycle (Default). 1'b1: Termination on period (io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are driven high is (BL/2+1) cycle(Not recommended).

DDRPHY_CAL_CON3

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RW	0x3f	vt_phyupd_req_cycle For debug purpose. For phy-initated update mode. It controls the number of cycle during which cs_phyupd FSM stays at ST_UPD_WAIT state.
25:22	RW	0x1	dvfs_wait_cycle For debug purpose. It controls the number of cycle during which cs_phydvfs FSM stays at ST_DVFS_A state.
21:16	RW	0x3f	vt_mcupd_req_cycle For debug purpose. For mc-initiated update mode. It controls the number of cycle during which cs_phyupd FSM stays at ST_UPD_WAIT state.
15:12	RW	0x9	upd_ack_cycle For debug purpose. It controls the number of cycle during which cs_phyupd FSM stays at ST_UPD_ACK state.
11	RW	0x0	auto_dqs_clean Enable Auto-DQS-Clean mode. Auto-DQS-Clean needs following conditions. 1. Gate training off 2. Use Differential IO with VSSQ-Term 3. ctrl_shgate=1'b0, ctrl_gateduradj=4'b0001 4. tDQSCK(min) =< 2*tCK: ctrl_gateadj = 4'b1001 tDQSCK(min) > 2*tCK: ctrl_gateadj = 4'b0000

Bit	Attr	Reset Value	Description
10	RW	0x0	gt_sw_mode Gate training Register RW mode control for debug purpose. Pcl_pd should be set to 1'b0 to enable write mode. 1'b1: CAL_GT_CS0_VWMC0, CAL_GT_CS1_VWMC0, CAL_GT_CS0_CYC, CAL_GT_CS1_CYC are writable when dvfs_mode = 2'b00 and ctrl_shgate = 1'b1. 1'b0: CAL_GT_CS0_VWMC0, CAL_GT_CS1_VWMC0, CAL_GT_CS0_CYC, CAL_GT_CS1_CYC are read-only.
9	RW	0x0	wr_sw_mode SW Write training code update control. This field will be enabled when restoring the previous write training results. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: SW_WR_DESKEWC_CS0_CON*, SW_WR_DESKEWC_CS1_CON*, SW_WR_DESKEWL_CS0_CON*, SW_WR_DESKEWL_CS1_CON* will be written to internal write training code. 1'b0: SW_WR_DESKEWC_CS0_CON*, SW_WR_DESKEWC_CS1_CON*, SW_WR_DESKEWL_CS0_CON*, SW_WR_DESKEWL_CS1_CON* will not be written to internal write training code.
8	RW	0x0	rd_sw_mode SW Read training code update control. This field will be enabled when restoring the previous read training registers. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: SW_RD_DESKEW_CENTER_CS0_CON_*, SW_RD_DESKEW_LEFT_CS0_CON_*, SW_RD_DQS_VWMC_CS0_CON0, SW_RD_DQS_VWML_CS0_CON0, SW_RD_DESKEW_CENTER_CS1_CON_*, SW_RD_DESKEW_LEFT_CS1_CON_*, SW_RD_DQS_VWMC_CS1_CON0, SW_RD_DQS_VWML_CS1_CON0 will be written to internal read training code. 1'b0: SW_RD_DESKEW_CENTER_CS0_CON_*, SW_RD_DESKEW_LEFT_CS0_CON_*, SW_RD_DQS_VWMC_CS0_CON0, SW_RD_DQS_VWML_CS0_CON0, SW_RD_DESKEW_CENTER_CS1_CON_*, SW_RD_DESKEW_LEFT_CS1_CON_*, SW_RD_DQS_VWMC_CS1_CON0, SW_RD_DQS_VWML_CS1_CON0 will not be written to internal read training code.
7	RW	0x0	wrlvl_sw_mode ctrl_wrlvl_code Register RW mode control for debug purpose. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: Ctrl_wrlvl1_code and ctrl_wrlvl0_code are writable when wrlvl_mode is set and pcfg_mode[2] is high. 1'b0: Ctrl_wrlvl1_code and ctrl_wrlvl0_code are read-only.

Bit	Attr	Reset Value	Description
6	RW	0x0	prbs_sw_mode SW PRBS training code update control. This field will be enabled when restoring the previous PRBS training resisters. pcl_pd should be set to 1'b0 to enable write mode. 1'b1: PRBS_CON4 and PRBS_CON5 will be written to internal PRBS training code. 1'b0: PRBS_CON4 and PRBS_CON5 are not written to internal PRBS training code.
5:4	RW	0x0	min_locktime_adj MDLL lock check timing control after DLL relock start during DVFS pause. 2'b00: Default. 2'b01: MDLL lock check timing will be delayed by 1 DFI cycle. 2'b10: MDLL lock check timing will be delayed by 2 DFI cycle. 2'b11: MDLL lock check timing will be delayed by 3 DFI cycle.
3	RW	0x0	ctrl_link_ecc_mode LP5 link ecc mode for dvfs0 mode 1'b1: ON 1'b0 : OFF
2:0	RW	0x0	pcfg_mode PHY Configuration Register mode control signal to read the information at each data slice for debug. This field should be set to 'h0 for normal operation. bit[2]=1'b1: Read mode enable for debug. VT compensated DLL codes will be read out for RD_DESKEW_CENTER_CS0_CON_DM, RD_DESKEW_CENTER_CS0_CON*, RD_DESKEW_CENTER_CS1_CON_DM, RD_DESKEW_CENTER_CS1_CON*, WR_DESKEWC_CS0_CON*, WR_DESKEWC_CS1_CON*, DM_DESKEWC_CS0_CON*, DM_DESKEWC_CS1_CON*. The original DLL code will be read out for WR_LVL_CON*. bit[2]=1'b0: Read mode disabled. VT compensated DLL codes will be read out for WR_LVL_CON*. The original DLL codes will be read out for RD_DESKEW_CENTER_CS0_CON_DM, RD_DESKEW_CENTER_CS0_CON*, RD_DESKEW_CENTER_CS1_CON_DM, RD_DESKEW_CENTER_CS1_CON*, WR_DESKEWC_CS0_CON*, WR_DESKEWC_CS1_CON*, DM_DESKEWC_CS0_CON*, DM_DESKEWC_CS1_CON*.

DDRPHY_CAL_CON4

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	LP4_High_density_mode LPDDR4 High density mode 1'b1: Support R17/R18 for ACT2. 1'b0: Support 2'b11 command for ACT2. This field should be disabled in LPDDR5.

Bit	Attr	Reset Value	Description
30:24	RW	0x00	glvl_periodic_fine_incr_adj Periodic gate training step size at fine mode. It should be smaller than 7'h1F. Default value is 7'b0000000(T/16). bit[30:29]=2'b00: The step value will be "glvl_periodic_fine_incr_adj[4:0]". bit[30:29]=2'b01: The step value will be "T/32". bit[30:29]=2'b10: The step value will be "T/4". bit[30:29]=2'b11: The step value will be "T/8". bit[30:24]=7'h00: The step value will be "T/16" (default).
23	RW	0x1	glitch_removal_length This field is used for control postamble glitch removal duration. 1'b0: 1.5tCK 1'b1: 1tCK
22	RW	0x0	glitch_removal_en This field is used for postamble glitch removal enable during Auto-DQS-Clean mode. 1'b0: Glitch removal disable 1'b1: Glitch removal enable
21:16	RW	0x03	lock_avg_cnt_number This field determines the Lock value update counter maximum number for moving averaging.
15	RW	0x1	WCK_MASK This field is option for WCK OFF timing on rank2rank operation 1'b1: WCK off timing on rank2rank operation can be allowed as optimized parameter by SMC. 1'b0: WCK off timing on rank2rank operation can be allowed same as WCK off timing on same rank operation.
14	RW	0x0	cmdfifo_wl_ext This field determines command FIFO write latency extention mode for auto dqs clean and ONLY use at LPDDR5. If this field set to 1, PHY can support RL = 21.
13:12	RW	0x0	upd_range_ext Default value is 0. This field is used for extend control range of ctrl_upd_range value. upd_range_ext = 2'b00 (default) 2'b00: Update when difference is greater than 0 tFS. 2'b01: Update when difference is greater than 3 tFS. 2'b10: Update when difference is greater than 7 tFS. 2'b11: Update when difference is greater than 15 tFS. upd_range_ext = 2'b01 2'b00: Update when difference is greater than 5 tFS. 2'b01: Update when difference is greater than 9 tFS. 2'b10: Update when difference is greater than 11 tFS. 2'b11: Update when difference is greater than 13 tFS. upd_range_ext = 2'b10 2'b00: Update when difference is greater than 17 tFS. 2'b01: Update when difference is greater than 19 tFS. 2'b10: Update when difference is greater than 21 tFS. 2'b11: Update when difference is greater than 23 tFS. upd_range_ext = 2'b11 2'b00: Update when difference is greater than 25 tFS. 2'b01: Update when difference is greater than 27 tFS. 2'b10: Update when difference is greater than 29 tFS. 2'b11: Update when difference is greater than 31 tFS.

Bit	Attr	Reset Value	Description
11	RW	0x0	wrtrn_multi_pattern Multi-pattern enable during the initial write training. 1'b0: One BL16 pattern will be asserted at each DLL code during write training. 1'b1: Four BL16 patterns will be asserted at each DLL code during write training.
10:6	RW	0x01	num_repeat The number of DRAM access at each DLL code during the initial read or write training. PHY will collect pass/fail decision for num_repeat times DRAM access at each DLL code. For initial write training, 4*num_repeat DRAM access will occur at each DLL code if wrtrn_multi_pattern is 1. Num_repeat should be greater than 0.
5	RW	0x1	dvfs_wrtrn_mode DVFS write training mode select. 1'b0: DVFS write training starts dvfs_wr_start_adj steps earlier from DQ right side edge. Training code will be increased to find the correct DQ/DBI location. 1'b1: DVFS write training starts at DQ right side edge determined at the initial write training. Training code will be increased or decreased to find the correct DQ/DBI location.
4:0	RW	0x0f	dvfs_wr_start_adj DVFS write training start point. It is valid only when dvfs_wrtrn_mode = 0 (or binary_en = 1, TBD). It determines how early DVFS write training starts from the previous write training code. (T=current lock value) DVFS write training start point = write DQ/DM Left code - (dvfs_wr_start_adj*2)

DDRPHY_LP_CON0

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:18	RW	0x3	ctrl_wck_phy_cg_en_ignore This field support to ignore phy_cg_en for WCK at WCK free running mode. This field should be controlled at WCK free running mode. bit[19] is BYTE1 control, bit[18] is BYTE0 control. 1'b1: Ignore phy_cg_en control for WCK. 1'b0: WCK is contollred by phy_cg_en.
17:16	RW	0x0	ctrl_pulld_dq Active HIGH signal to pull-down the High-Z duration of DQ/DM signals for debug purpose. For normal operation this field should be zero. When bus is idle, it can be set to pull-down or up the bus not to make bus high-z state. 2'b11: DQ/DM pull down enabled. io_dq_pdn and io_dm_pdn will be driven high. io_dq_pup and io_dm_pup will be driven low. 2'b00: DQ/DM pull down disabled. io_dq_pdn and io_dm_pdn will be driven low. io_dq_pup and io_dm_pup will be driven low. Others: Don't use.

Bit	Attr	Reset Value	Description
15	RW	0x0	cs_io_pd Command signal I/O driver power down mode select. If enabled, Command signal I/O driver will be turned on and off dynamically depending on "ctrl_wake_up" to save I/O power. This field should not be changed during the normal operation. 1'b0: Command signal I/O driver will be always on. (io_adct_en is always low) 1'b1: Enable command signal I/O driver dynamic power down. Command signal I/O driver will be turned on (io_adct_en is low) only when ctrl_wake_up is high.
14	RW	0x1	ds_io_pd DQ, DM, DQS I/O receiver power down will be enabled dynamically during normal operation to save I/O power. 1'b0: DQS/DQ/DM receiver power down will be disabled and receivers are always on. (io_dq_pd, io_dqs_pd, io_dm_pd are low) 1'b1: DQS/DQ/DM receiver is on (io_dq_pd, io_dqs_pd, io_dm_pd is low) only for the read duration, off (io_dq_pd, io_dqs_pd, io_dm_pd is high) otherwise.
13	RW	0x0	scheduler_HW_clock_gating_disable PHY scheduler Dynamic clock gating disable signal. 1'b0: HW Dynamic clock gating function enable. 1'b1: HW Dynamic clock gating function ingore.
12	RW	0x0	pcl_pd PHY control logic clock gating enable. This field can be enabled after all the initial (or long) training is done. 1'b0: PHY control logic clock gating off. 1'b1: PHY control logic clock gating on. PHY internal clock will be alive if debug_mode_en is high or if write/read/gate training is on-going. Otherwise, internal clock will be gated.
11	RW	0x0	mdll_cg_en Master DLL dynamic clock gating mode. 1'b0: MDLL dynamic clock gating off. 1'b1: MDLL dynamic clock gating on. MDLL clock gating will be controlled by ctrl_phy_cg_en.
10	RW	0x1	dqs_enable 1'b1: DQS enable 1'b0: DQS disable
9	RW	0x0	wck_enable 1'b1: WCK enable(LPDDR5 option) 1'b0: WCK disable(LPDDR4 option)
8	RW	0x0	ctrl_dqs_drv_off DQS driver off signal. When this field enabled, DQS driver is turned off (io_pdqs_en = 1'b1, io_ndqs_en = 1'b1). This field should be enabled when disabling write link ECC(LPDDR5).
7	RW	0x0	ctrl_dq_rcv_on DQ receiver on signal. When this field enabled, DQ receiver is turned on (io_dq_read = 1'b1, io_dq_pd = 1'b0).
6	RW	0x0	ctrl_scheduler_en PHY scheduler clock enable (LPDDR5 should be enabled). 1'b1: Clock enable 1'b0: Clock disable
5:4	RW	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	write_se_wck Wck single-ended mode 1'b1: Single-ended mode 1'b0: Differential mode Caution: write_se_ck should be enabled using write_se_wck in LPDDR5.
2	RW	0x0	Reserved2 Reserved
1:0	RW	0x3	ctrl_pulld_dqs Active HIGH signal to pull-up or down PDQS/NDQS signals. When using Gate training in LPDDR4, this field can be zero. When bus is idle, it can be set to pull-down or up the bus to avoid high-z state (PDQS/NDQS is pulled-down/up). If not using Gate training, this field should be always set for normal operation to make P/NDQS signals pull-down/up. 2'b11: DQS pull-down enabled. io_pdqs_pdn is set to high. io_ndqs_pup are set to high only if ctrl_dfdqs is high. io_pdqs_pup and io_ndqs_pdn are set to low. 2'b00: DQS pull-down disabled. io_pdqs_pdn and io_ndqs_pup are set to low. io_pdqs_pup and io_ndqs_pdn are set to low.

DDRPHY_GATE_CON0

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:24	RW	0x3	rank_en RANK enable signal for read command decoding and dynamic gate training. 2'b11: Enable RANK0 and RANK1, CS[1:0] used for read command decoding, which is used to generate gate signal. 2'b01: Enable RANK0, CS[0] only used for read command decoding. 2'b10: Enable RANK1, CS[1] only used for read command decoding.
23:14	RW	0x003	Reserved1 Reserved
13:12	RW	0x3	rank1_dsen DQS Cleaning/Gate signal generation enable for RANK1. bit[13]: Enable data_slice1. bit[12]: Enable data_slice0.
11:2	RW	0x003	Reserved2 Reserved
1:0	RW	0x3	rank0_dsen DQS cleaning/gate signal generation enable for RANK0. bit[1]: Enable data_slice1. bit[0]: Enable data_slice0.

DDRPHY_OFFSETR_CON0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	ctrl_offsetr1 This field can be used to give offset to read DQS for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Read DQS offset amount: ctrl_offsetr1[9] = 1: (tFS: fine step delay) Read DQS 90 degree delay amount or Read DQS delay from read training - ctrl_offsetr1[8:0] x tFS ctrl_offsetr1[9] = 0: Read DQS 90 degree delay amount or Read DQS delay from read training + ctrl_offsetr1[8:0] x tFS
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	ctrl_offsetr0 This field can be used to give offset to read DQS for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Read DQS offset amount: ctrl_offsetr0[9]= 1: (tFS: fine step delay) Read DQS 90 degree delay amount or Read DQS delay from read training - ctrl_offsetr0[8:0] x tFS ctrl_offsetr0[9] = 0: Read DQS 90 degree delay amount or Read DQS delay from read training + ctrl_offsetr0[8:0] x tFS

DDRPHY_OFFSETW_CON0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	ctrl_offsetw1 This field can be used to give offset to write DQ/DM in BYTE1 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in master delay Line. Write DQ offset amount : ctrl_offsetw1[9] = 1 : (tFS: fine step delay) Write DQ 270 degree delay amount or Write DQ delay from write training - ctrl_offsetw1[8:0] x tFS ctrl_offsetw1[9] = 0 : Write DQ 270 degree delay amount or Write DQ delay from write training + ctrl_offsetw1[8:0] x tFS
15:10	RW	0x00	Reserved1 Reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	ctrl_offsetw0 This field can be used to give offset to write DQ/DM in BYTE0 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in master delay Line. Write DQ offset amount : ctrl_offsetw0[9] = 1 : (tFS: fine step delay) Write DQ 270 degree delay amount or Write DQ delay from write training - ctrl_offsetw0[8:0] x tFS ctrl_offsetw0[9] = 0 : Write DQ 270 degree delay amount or Write DQ delay from write training + ctrl_offsetw0[8:0] x tFS

DDRPHY_OFFSET_DQ_CON0

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved0 Reserved
13:7	RW	0x00	ctrl_offset_dq_ds1 Offset control for read DQ/DM bits in BYTE1. It is used to impose delay for read DQ/DM before read training, so that DQS is ahead of DQ/DM. Once this field is set, it should not change during operation. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in master delay Line. Read DQ/DM offset amount: ctrl_offset_dq_ds1[6:0] x tFS
6:0	RW	0x00	ctrl_offset_dq_ds0 Offset control for read DQ/DM bits in BYTE0. It is used to impose delay for read DQ/DM before read training, so that DQS is ahead of DQ/DM. Once this field is set, it should not change during operation. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in master delay Line. Read DQ/DM offset amount: ctrl_offset_dq_ds0[6:0] x tFS

DDRPHY_OFFSETC_CON0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	ctrl_offsetc1 Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and ctrl_vtc_en is high and dfi_ctrlupd_req becomes HIGH and LOW. It is used to give offset to gate training result for debug purpose. ctrl_offsetc [9] = 1 : (tFS: fine step delay) Total GATE delay amount - ctrl_offsetc [8:0] x tFS ctrl_offsetc [9] = 0 : Total GATE delay amount + ctrl_offsetc [8:0] x tFS
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	ctrl_offsetc0 Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and dfi_ctrlupd_req becomes HIGH and LOW. It is used to give offset to gate training result for debug purpose. ctrl_offsetc [9] = 1 : (tFS: fine step delay) Total GATE delay amount - ctrl_offsetc [8:0] x tFS ctrl_offsetc [9] = 0 : Total GATE delay amount + ctrl_offsetc [8:0] x tFS

DDRPHY_SHIFTC_CON0

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved
5:3	RW	0x0	ctrl_shiftc1 GATE signal delay amount for DDR. This is used to adjust GATE delay based on DFI PHY clock period. 1. When gate_debug_en[3] = 1 for gate margin control. 2. When gate_cal_mode = 0 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0(0 degree shift) 3'b001: T(365 degree shift) 3'b010: T/2(180 degree shift) 3'b011: T/4(90 degree shift) 3'b100: T/8(45 degree shift) 3'b101: T/16(22.5 degree shift) 3'b111: 3T/4(270 degree shift)

Bit	Attr	Reset Value	Description
2:0	RW	0x0	ctrl_shiftc0 GATE signal delay amount for DDR. This is used to adjust GATE delay based on DFI PHY clock period 1. When gate_debug_en[3] = 1 for gate margin control 2. When gate_cal_mode = 0 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in master delay line. 3'b000: 0(0 degree shift) 3'b001: T(365 degree shift) 3'b010: T/2(180 degree shift) 3'b011: T/4(90 degree shift) 3'b100: T/8(45 degree shift) 3'b101: T/16(22.5 degree shift) 3'b111: 3T/4(270 degree shift)

DDRPHY_OFFSETD_CON0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29	RW	0x0	resync_handshake_mode This field controls SW DLL update policy. 1'b1: SW DLL update by handshaking between ctrl_resync and resync_done_flag*. 1'b0: SW DLL update by ctrl_resync enable and disable.
28	RW	0x0	upd_mode This field controls "PHY Update" mode. 1'b1: MC-Initiated update mode. dfi_phyupd_req is not asserted by PHY. 1'b0: PHY-Initiated update mode. dfi_phyupd_req will be asserted by PHY.
27	RO	0x0	resync_done_flag_cs This field can identify resync is applied for CtrlPHY. 1'b1: Resync is applied. 1'b0: Resync is not applied.
26	RO	0x0	resync_done_flag_ds1 This field can identify resync is applied for DataPHY1. 1'b1: Resync is applied. 1'b0: Resync is not applied.
25	RO	0x0	resync_done_flag_ds0 This field can identify resync is applied for DataPHY0. 1'b1: Resync is applied. 1'b0: Resync is not applied.

Bit	Attr	Reset Value	Description
24	RW	0x0	ctrl_resync Active RISIG-EDGE signal. User should set this signal LOW after setting HIGH for normal operation. When this bit transits from LOW to HIGH, pointers of FIFO within PHY and all of the DLL information (Read/Write/CA/CS DLL) is updated. If PHY is set to PHY-initiated updated mode, dfi_phyupd_req/dfi_phyupd_ack handshake should occur after ctrl_resync transits from LOW to HIGH. If PHY is set to MC-initiated update mode, FIFO reset and DLL update will progress without a handshake after ctrl_resync transits from LOW to HIGH. In general, this bit should be set only during initialization and refresh cycles. Refer to "7.9 DLL Code Update" to use ctrl_resync. NOTE: Invalid command that are not listed in JEDEC command truth table could be interpreted as Read command and it will lead to FIFO/gate signal corruption. For example, vendor specific TMRS is reported to be causing this issue. Please toggle ctrl_resync after sending TMRS so that FIFO and Gate signal can be restored.
23:10	RW	0x0000	Reserved2 Reserved
9:0	RW	0x000	ctrl_offsetd DLL offset control for CA. It can be controlled to adjust delay of CA bus during Command Bus Training. If this field is fixed, this should not be changed during normal operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in master delay line. offset amount for CA: ctrl_offsetd[9] = 1 : (tFS: fine step delay) CA deskew delay - ctrl_offsetd[8:0] x tFS ctrl_offsetd[9] = 0 : CA deskew delay + ctrl_offsetd[8:0] x tFS

DDRPHY_OFFSETO_CON0

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	ctrl_offseto1 This field can be used to give offset to io_dq_en[15:8]/io_dm_en[1], which controls DQ/DM PAD OEN for BYTE1 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Offset amount: ctrl_offseto1[9] = 1 : (tFS: fine step delay) DQ/DM OEN 270 degree delay amount - ctrl_offseto1[8:0] x tFS ctrl_offseto1[9] = 0 : DQ/DM OEN 270 degree delay amount + ctrl_offseto1[8:0] x tFS
15:10	RW	0x00	Reserved1 Reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	ctrl_offseto0 This field can be used to give offset to io_dq_en[7:0]/io_dm_en[0], which controls DQ/DM PAD OEN for BYTE0 for debug purpose. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in master delay line. Offset amount: ctrl_offseto0[9] = 1 : (tFS: fine step delay) DQ/DM OEN 270 degree delay amount - ctrl_offseto0[8:0] x tFS ctrl_offseto0[9] = 0 : DQ/DM OEN 270 degree delay amount + ctrl_offseto0[8:0] x tFS

DDRPHY_WR_LVL_CON0
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RW	0x000	ctrl_wrlvl1_code Write level slave DLL code value for data_slice 1. It will be applied to write DQS DLL code if wrlvl_sw_mode is enabled, wrlvl_mode is set and pcfg_mode[2] is high.
15:10	RO	0x00	Reserved1 Reserved
9:0	RW	0x000	ctrl_wrlvl0_code Write level slave DLL code value for data_slice 0. It will be applied to write DQS DLL code if wrlvl_sw_mode is enabled, wrlvl_mode is set and pcfg_mode[2] is high.

DDRPHY_WR_LVL_CON1
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:20	RW	0x1e	tWLMRD It controls tWLMRD and tWLDQSEN parameter during write leveling. tWLMRD should be set over "clock_ratio*tMOD + WL -3" when ODT enable for DDR4. tWLMRD = DFI PHY clock period * (tWLMRD) tWLDQSEN = DFI PHY clock period * (tWLMRD/2)
19:14	RW	0x20	tWLO It controls tWLO parameter during write leveling. It controls when PHY samples DQ feedback from DRAM during write leveling. tWLO = DFI PHY clock period * tWLO
13:8	RW	0x04	tDQSL It controls tDQSL parameter during write leveling. It controls interval of DQS toggles during write leveling. tDQSL = DFI PHY clock period * tDQSL

Bit	Attr	Reset Value	Description
7:4	RW	0x7	wrlvl_wck_toggle Number of WCK toggle. It controls toggle of WCK when wck2ck leveling and Vref setting on CBT. 4'b0001: 4 WCK Toggle 4'b0011: 6 WCK Toggle 4'b0111: 8 WCK Toggle (default) 4'b1111: 10 WCK Toggle
3:0	RW	0x3	wrlvl_dqs_toggle Number of DQS toggle. It controls toggle of DQS when write leveling and Vref setting on CBT. 4'b0001: 1tCK DQS Toggle 4'b0011: 2tCK DQS Toggle (default) 4'b0111: 3tCK DQS Toggle 4'b1111: 4tCK DQS Toggle

DDRPHY_WR_LVL_CON2

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	twlcal_en Calibration enable duration control. Controls the duration from training enable to the first command trigger in DFI cycle.
23:16	RW	0x46	twlcal_wait For debug purpose
15:12	RW	0x5	NUM_RST_CMD Number of MPC WR/RD FIFO CMD. This controls the number of repetition of MPC WR/RD FIFO CMD that are used to reset MPC FIFO.
11:6	RW	0x16	trden2resp Calibration done check timing control. Controls when to check the training response from each byte in DFI cycle.
5:4	RO	0x0	wlcal_fail It will be enable if there are no pass period after WL calibration. It should be read by zero if calibration is done normally. bit[1]: For Byte 1. bit[0]: For Byte 0.
3:2	RO	0x0	ctrl_dqs_extra Add extra write DQS toggle on postamble. This field will be enabled when wr_sw_mode is enabled. The maximum is 1tCK. 2'b01: +1tCK 2'b00: +0tCK
1:0	RO	0x0	ctrl_dqs_shift Write DQS cycle code for Data Slice. This field will be enabled when wr_sw_mode is enabled. The maxium is 1tCK. bit[1]: DQS for Byte 1 bit[0]: DQS for Byte 0 1'b1: +1tCK 1'b0: +0tCK

DDRPHY_WR_LVL_CON3

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
17:16	RO	0x0	wrlvl_half_over Write level SDLL code information. If write level code is over half of master dll code, "wrlvl_half_over[n]" will be "1" for Data_slice[n]. If it is set to high after write leveling, S/W can see that CK delay is smaller than DQS delay.
15:13	RW	0x0	Reserved1 Reserved
12:8	RW	0x0b	wrlvl_wait It controls tWLO parameter during write leveling. It controls when PHY samples DQ feedback from DRAM during write leveling. tWLO = 4 * DFI PHY clock period * wrlvl_wait
7:3	RW	0x00	Reserved2 Reserved
2	RW	0x0	dfi_wlcal_en Write latency calibration enable. When it is high, CA and CS will be delayed as 1 PHY clock cycle and 1 extra toggle will be added to DQS. If it is set to high, write latency calibration should be done to find proper write latency after write trainining.
1	RW	0x0	ctrl_wrlvl_clear Write level DLL code clear. When it is high, ctrl_wrlvl0_code~ctrl_wrlvl1_code, wrlvl_half_over, wrlvl_fail_status and PHY internal write leveling FSM will be reset.
0	RW	0x0	ctrl_wrlvl_resync Write level DLL code update enable. Active RISIG-EDGE signal. This signal should become LOW after set HIGH for normal operation. When this bit transits from LOW to HIGH, write DQS DLL codes will be updated with the current code. Assert and de-assert ctrl_wrlvl_resync to apply ctrl_wrlvl0_code~ctrl_wrlvl1_code to write DQS DLL.

DDRPHY_CA_DESKEW_CON0

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved
25:16	RW	0x000	CA1DeSkewCode BDLL code for CA[1]. The delay for CA[1] signal will be CA1DeSkew value tFS.
15:10	RW	0x00	Reserved0 Reserved
9:0	RW	0x000	CA0DeSkewCode BDLL code for CA[0]. The delay for CA[0] signal will be CA0DeSkew value tFS.

DDRPHY_CA_DESKEW_CON1

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved
25:16	RW	0x000	CA3DeSkewCode BDLL code for CA[3]. The delay for CA[3] signal will be CA3DeSkew value tFS.
15:10	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	CA2DeSkewCode BDLL code for CA[2]. The delay for CA[2] signal will be CA2DeSkew value tFS.

DDRPHY_CA_DESKEW_CON2

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved
25:16	RW	0x000	CA5DeSkewCode BDLL code for CA[5]. The delay for CA[5] signal will be CA5DeSkew value tFS.
15:10	RW	0x00	Reserved0 Reserved
9:0	RW	0x000	CA4DeSkewCode BDLL code for CA[4]. The delay for CA[4] signal will be CA4DeSkew value tFS.

DDRPHY_CA_DESKEW_CON3

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved0 Reserved
9:0	RW	0x000	RSTDeSkewCode BDLL Code for RST. 0x0 or 0x8: The delay for RST signal will be zero delay. 0x9~0x2B: The delay for RST signal will be RSTDeSkew value - 'h8 tFS. Others: Invalid.

DDRPHY_CA_DESKEW_CON4

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved
25:16	RW	0x000	CKDeSkewCode BDLL code for CK. 0x0 or 0x8: The delay for CK signal will be zero delay. 0x9~0x2B: The delay for CK signal will be CKDeSkew value - 'h8 tFS. Others: Invalid.
15:10	RW	0x00	Reserved0 Reserved
9:0	RW	0x000	CA6DeSkewCode BDLL code for CA[6]. The delay for CA[6] signal will be CA6DeSkew value tFS.

DDRPHY_CA_DESKEW_CON5

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved
25:16	RW	0x000	CS1DeSkewCode BDLL code for CS1. The delay for CS1 signal will be CS1DeSkew value tFS.

Bit	Attr	Reset Value	Description
15:10	RW	0x00	Reserved0 Reserved
9:0	RW	0x000	CS0DeSkewCode BDLL code for CS0. The delay for CS0 signal will be CS0DeSkew value tFS.

DDRPHY_CA_DESKEW_CON6
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved
25:16	RW	0x000	CKE1DeSkewCode BDLL code for CKE1. 0x0 or 0x8: The delay for CKE1 signal will be zero delay. 0x9~0x2B: The delay for CKE1 signal will be CKE1DeSkew value - 'h8 tFS. Others: Invalid.
15:10	RW	0x00	Reserved0 Reserved
9:0	RW	0x000	CKE0DeSkewCode BDLL code for CKE0. 0x0 or 0x8: The delay for CKE0 signal will be zero delay. 0x9~0x2B: The delay for CKE0 signal will be CKE0DeSkew value - 'h8 tFS. Others: Invalid.

DDRPHY_CAL_WR_PATTERN_CON0
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8 This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. Wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8 This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. Wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON1
Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8 This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. Wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8 This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. Wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON2
Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16 This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. Wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16 This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. Wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON3
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16 This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. Wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.

Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16 This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. Wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. Wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON4

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8 This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. Wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8 This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. Wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8 This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. Wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8 This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data of DM[0] and DQ[1] at the 4th valid rising edge of DQS. Wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.

Bit	Attr	Reset Value	Description
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16 This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. Wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16 This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. Wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16 This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. Wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16 This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. Wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. Wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_CAL_RD_PATTERN_CON0

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x55	rdtrn_inv_pattern_ds0 This fields specifies the lower byte invert. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR15 setting(Lower-Byte Invert Register for DQ Calibration).
23:16	RW	0x55	rdtrn_inv_pattern_ds1 This fields specifies the upper byte invert. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR20 setting(Upper-Byte Invert Register for DQ Calibration).

Bit	Attr	Reset Value	Description
15:8	RW	0x5a	rdtrn_rddata_pattern0 This fields specifies the DQ/DMI pattern. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR32 setting(DQ Calibration Pattern "A").
7:0	RW	0x3c	rdtrn_rddata_pattern1 This fields specifies the DQ/DMI pattern. The expected read data pattern is defined with this field for read training or gate training with gate_rdchk_en enabled. The value should be the same as DRAM MR40 setting(DQ Calibration Pattern "B").

DDRPHY_MDLL_CON0

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	ctrl_start_point Initial DLL lock start point. This is the number of delay cells and is the start point where "DLL" start tracing to be locked. Initial delay time is calculated by multiplying the unit delay of delay cell and this value.
23	RW	0x0	clkm_cg_en_sw S/W master DLL clock gating enable for debug purpose. It should be low for normal operation. Its function is the same as ctrl_clkm_cg_en. If ctrl_clkm_cg_en or clkm_cg_en_sw is high, master DLL clock gating is enabled. 1'b0: PHY master DLL clock gating is disabled. 1'b1: PHY master DLL clock gating is enabled.
22:19	RW	0x0	Reserved0 Should be zero
18:8	RW	0x001	ctrl_force This field is used instead of ctrl_lock_value[9:0], which represents one DRAM clock period information found by the DLL only when ctrl_dll_on is LOW, i.e. If the DLL is off, this field is used to generate 270 degrees clock and shift DQS by 90 degrees.
7	RW	0x0	ctrl_half_gtlich_mask_ignore 1'b1: Glitch masking ignore using ctrl_half on DVFS. 1'b0: Glitch masking using ctrl_half on DVFS.
6	RW	0x1	ctrl_start This field is used to start DLL locking. 1'b1: Master DLL locking is enabled. 1'b0: Master DLL reset.
5	RW	0x1	ctrl_dll_on HIGH active start signal to turn on the DLL. This signal should be kept HIGH for normal operation. If this signal becomes LOW, DLL is turned off. This bit should be kept set before ctrl_start is set to turn on the DLL.

Bit	Attr	Reset Value	Description
4:1	RW	0xf	ctrl_ref This field determines the period of time when ctrl_locked is cleared. It is used to make ctrl_locked insensitive to clock jitter. 4'b0000: Don't use. 4'b0001: Ctrl_flock is de-asserted during 16 clock cycles, ctrl_locked is deasserted. 4'b0010: Ctrl_flock is de-asserted during 24 clock cycles, ctrl_locked is deasserted. ... 4'b1110: Ctrl_flock is de-asserted during 120 clock cycles, ctrl_locked is deasserted. 4'b1111: Once ctrl_locked and dfi_init_complete are asserted, those won't be deasserted until rst_n is asserted.
0	RW	0x0	ctrl_half This field controls low speed mode for Master DLL. If this bit is high, DLL can lock at low frequencies (266MHz <= DFI PHY clock frequency < 533MHz).

DDRPHY_MDLL_CON1

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:21	RO	0x001	ctrl_lock_value_init The reference lock_value for VT compensation, which has been read during the initial training. It is updated when dfi_lvl_periodic = 0 and dfi_rdlvl_gate_en/dfi_rdlvl_wr_en/dfi_rdlvl_en changes from 1'b0 to 1'b1.
20	RO	0x0	ctrl_clock Coarse lock information. According to clock jitter, ctrl_clock can be de-asserted.
19	RO	0x0	ctrl_flock Fine lock information. According to clock jitter, ctrl_flock can be de-asserted.
18	RO	0x0	ctrl_locked DLL stable lock information. This field is set after ctrl_flock is set. This field is cleared when ctrl_flock is de-asserted for some period of time specified by ctrl_ref value. This field is required for stable lock status check.
17	RW	0x0	lock_value_init_override Initial lock_value override mode. 1'b1: Ctrl_lock_value_init in read/write mode. If this field is enabled, ctrl_lock_value_init will be written to the PHY internal register. 1'b0: Ctrl_lock_value in read only mode. If this field is disabled, internal initial lock value will be read out.
16:11	RW	0x00	Reserved0 Reserved
10:0	RO	0x100	ctrl_lock_value Locked delay line encoding value. Ctrl_lock_value[10:3]: Number of delay cells for coarse lock. Ctrl_lock_value[2:0]: Control value for fine lock. From ctrl_lock_value[10:0], tFS(fine step delay) can be calculated. tFS = tCK/ctrl_lock_value[10:0], fine step delay.

DDRPHY_DVFS_CON

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	dvfs_mode DVFS mode select. This field controls which DVFS register sets will be used after frequency change. 2'b00: Normal mode 2'b01: DVFS0 mode 2'b10: DVFS1 mode
29:14	RW	0x0000	Reserved0 Reserved
13	RW	0x1	per_dvfs_train_disable Per DVFS Training register control disable. 1'b0: SW_RD*, SW_WR*, PRBS_* register value will be applied to internal training code registers when frequency change occurs. 1'b1: PRBS, read and write training register will not be changed when frequency change occurs.
12	RW	0x0	dvfs_fsbst_en Vref fast boost mode enable during DVFS pause duration. Enable to reduce SOC Vref settling time when SOC Vref level should be changed during DVFS pause. 1'b1: SOC Vref FSBST is enabled. PHY will guarantee that io_zq_ds_vref_fsbst is driven 2'b11 for at least 125ns and then stay at 2'b00 for at least 125ns during frequency change duration via dfi_init_start and dfi_init_complete handshake. 1'b0: Io_zq_ds_vref_fsbst will be determined by zq_ds0_vref_fsbst and zq_ds1_vref_fsbst.
11:0	RW	0x640	freq_train DFI PHY clock frequency for the initial training(read/write/gate training/write leveling/CBT). It is used as a reference for VT compensation and frequency offset compensation. Initial training should be done only at the highest frequency. For example, if the highest frequency is 1600MHz, freq_train should be set to 'd1600. This field should not change during the normal operation.

DDRPHY_DVFS0_CON0

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RW	0x640	dvfs0_freq DFI PHY clock frequency for DVFS0 mode. This field must be properly set to increase data eye margin.
19:14	RW	0x20	dvfs0_rdlat_rank0 This field will be used instead of ctrl_rdlat_rank0 during DVFS0 mode.
13	RW	0x0	dvfs0_twpre Write preamble length for DVFS0 mode. It will be used instead of ctrl_twpre in DVFS0 mode. 1'b0: 2 tCK for higher speeds. 1'b1: 1 tCK for lower speeds.
12	RW	0x0	dvfs0_rpre_opt Read pre-amble toggle option for DVFS0 mode. It will be used instead of ctrl_rpre_opt in DVFS0 mode. 1'b1: Read pre-amble = 2nCK toggle. 1'b0: Read pre-amble = 2nCK static.
11	RW	0x1	dvfs0_wr_per_rank_en Per rank Write DQ/DM DLL control enable in DVFS0 mode. It will be used instead of wr_per_rank_en in DVFS0 mode.

Bit	Attr	Reset Value	Description
10	RW	0x1	dvfs0_rd_per_rank_en Per rank Read DQS/DQ/DM DLL control enable in DVFS0 mode. It will be used instead of rd_per_rank_en in DVFS0 mode.
9	RW	0x0	dvfs0_freq_offset_en Frequency offset calculation enable in DVFS0 mode. It should be set to 1'b0 if DLL is off because the frequency compensation offset will be calculated using the current DLL lock value.
8	RW	0x0	dvfs0_auto_dqs_clean Enable Auto-DQS-Clean mode in DVFS0 mode.
7	RW	0x0	dvfs0_glitch_removal_en This field is used for postamble glitch removal enable during Auto-DQS-Clean mode in DVFS0 mode. 1'b0: Glitch removal disable. 1'b1: Glitch removal enable.
6:5	RW	0x0	dvfs0_rpost_opt Read post-amble toggle option for DVFS0 mode. It will be used instead of ctrl_rpost_opt in DVFS0 mode. 2'b00: Read pre-amble = 0.5tWCK static. 2'b01: Read pre-amble = 2.5tWCK static. 2'b10: Read pre-amble = 4.5tWCK static.
4	RW	0x0	dvfs0_cbt_en LPDDR5 CBT mode enable for DVFS0 mode
3	RW	0x0	dvfs0_link_ecc_mode LP5 link ecc mode for dvfs0 mode 1'b1: ON 1'b0: OFF
2	RW	0x1	dvfs0_rdtrn_dbi_cal_en DBI enable for LPDDR4 read training in DVFS0. 1'b0: DBI is not calibrated during read training. 1'b1: DBI is calibrated during read training.
1	RW	0x1	dvfs0_wrtrn_dbi_cal_en DBI enable for LPDDR4 write training in DVFS0. Set to 0 if Data Mask, Write DBI and Read DBI are all disabled at DRAM. Otherwise, it should be set to 1. 1'b0: DBI is not calibrated during write training. 1'b1: DBI is calibrated during write training.
0	RW	0x0	dvfs0_LP5_16bank_mode LP5 16bank mode 1'b1: 16bank mode 1'b0: 4bg/4bank mode 8 bank mode don't care about this field.

DDRPHY_DVFS1_CON0

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RW	0x640	dvfs1_freq DFI PHY clock frequency for DVFS1 mode. This field must be properly set to increase data eye margin.
19:14	RW	0x20	dvfs1_rdlat_rank0 This field will be used instead of ctrl_rdlat_rank0 during DVFS1 mode.

Bit	Attr	Reset Value	Description
13	RW	0x0	dvfs1_twpre Write preamble length for DVFS1 mode. It will be used instead of ctrl_twpre in DVFS1 mode. 1'b0: 2 tCK for higher speeds 1'b1: 1 tCK for lower speeds
12	RW	0x0	dvfs1_rpre_opt Read pre-amble toggle option for DVFS1 mode. It will be used instead of ctrl_rpre_opt in DVFS1 mode. 1'b1: Read pre-amble = 2nCK toggle. 1'b0: Read pre-amble = 2nCK static.
11	RW	0x1	dvfs1_wr_per_rank_en Per rank Write DQ/DM DLL control enable in DVFS1 mode. It will be used instead of wr_per_rank_en in DVFS1 mode.
10	RW	0x1	dvfs1_rd_per_rank_en Per rank Read DQS/DQ/DM DLL control enable in DVFS1 mode. It will be used instead of rd_per_rank_en in DVFS1 mode.
9	RW	0x0	dvfs1_freq_offset_en Frequency offset calculation enable in DVFS1 mode. It should be set to 1'b0 if DLL is off because the frequency compensation offset will be calculated using the current DLL lock value.
8	RW	0x0	dvfs1_auto_dqs_clean Enable Auto-DQS-Clean mode in DVFS1 mode
7	RW	0x0	dvfs1_glitch_removal_en This field is used for postamble glitch removal enable during Auto-DQS-Clean mode in DVFS1 mode. 1'b0: Glitch removal disable. 1'b1: Glitch removal enable.
6:5	RW	0x0	dvfs1_rpost_opt Read post-amble toggle option for DVFS1 mode. It will be used instead of ctrl_rpost_opt in DVFS1 mode 2'b00: Read pre-amble = 0.5tWCK static. 2'b01: Read pre-amble = 2.5tWCK static. 2'b10: Read pre-amble = 4.5tWCK static.
4	RW	0x0	dvfs1_cbt_en LPDDR5 CBT mode enable for DVFS1 mode
3	RW	0x0	dvfs1_link_ecc_mode LP5 link ecc mode for dvfs1 mode. 1'b1: ON 1'b0: OFF
2	RW	0x1	dvfs1_rdtrn_dbi_cal_en DBI enable for LPDDR4 read training in DVFS1. 1'b0: DBI is not calibrated during read training. 1'b1: DBI is calibrated during read training.
1	RW	0x1	dvfs1_wrtrn_dbi_cal_en DBI enable for LPDDR4 write training in DVFS1. Set to 0 if Data Mask, Write DBI and Read DBI are all disabled at DRAM. Otherwise, it should be set to 1. 1'b0: DBI is not calibrated during write training. 1'b1: DBI is calibrated during write training.
0	RW	0x0	dvfs1_LP5_16bank_mode LP5 16bank mode in DVFS1 mode. 1'b1: 16bank mode 1'b0: 4bg/4bank mode 8 bank mode don't care about this field.

DDRPHY_DVFS0_CON1

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs0_dll_on DLL on/off control during DVFS0 mode. It will be used instead of ctrl_dll_on during DVFS0 mode.
30	RW	0x0	dvfs0_half Low frequency locking enable. It will be used instead of ctrl_half during DVFS0 mode.
29:28	RW	0x3	dvfs0_wck_phy_cg_en_ignore This field support to ignore phy_cg_en for WCK at WCK free running mode in DVFS0. This field should be controlled at WCK free running mode. Bit[27] is for BYTE1 control and bit[26] is for BYTE0 control. 1'b1: Ignore phy_cg_en control for WCK. 1'b0: WCK is contollred by phy_cg_en.
27:26	RW	0x0	Reserved0 Reserved
25:18	RW	0x20	dvfs0_start_point Initial DLL lock start point in DVFS0 mode.
17:9	RW	0x000	dvfs0_offsetr This field will be used instead of ctrl_offsetr* during DVFS0 mode. dvfs0_offsetr[7] = 1 : (tFS: fine step delay) Read delay amount dvfs0_offsetr[6:0] x tFS dvfs0_offsetr[7] = 0 : Read delay amount dvfs0_offsetr[6:0] x tFS Note that "ctrl_force/4" will be the base DLL code for read path if DLL is off and read training is disabled.
8:0	RW	0x000	dvfs0_offsetw Deprecated

DDRPHY_DVFS1_CON1

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs1_dll_on DLL on/off control during DVFS1 mode. It will be used instead of ctrl_dll_on during DVFS1 mode.
30	RW	0x0	dvfs1_half Low frequency locking enable. It will be used instead of ctrl_half during DVFS1 mode.
29:28	RW	0x3	dvfs1_wck_phy_cg_en_ignore This field support to ignore phy_cg_en for WCK at WCK free running mode in DVFS1. This field should be controlled at WCK free running mode. Bit[27] is for BYTE1 control and bit[26] is for BYTE0 control. 1'b1: Ignore phy_cg_en control for WCK. 1'b0: WCK is contollred by phy_cg_en.
27:26	RW	0x0	Reserved0 Reserved
25:18	RW	0x20	dvfs1_start_point Initial DLL lock start point in DVFS1 mode.

Bit	Attr	Reset Value	Description
17:9	RW	0x000	dvfs1_offsetr This field will be used instead of ctrl_offsetr* during DVFS1 mode. dvfs1_offsetr[7] = 1 : (tFS: fine step delay) Read delay amount dvfs1_offsetr[6:0] x tFS dvfs1_offsetr[7] = 0 : Read delay amount dvfs1_offsetr[6:0] x tFS Note that "ctrl_force/4" will be the base DLL code for read path if DLL is off and read training is disabled.
8:0	RW	0x000	dvfs1_offsetw Deprecated

DDRPHY_DVFS0_CON2

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs0_cmosrcv This field will control I/O receiver mode instead of ctrl_cmosrcv during DVFS0 mode.
30	RW	0x1	dvfs0_dfdqs Differential receiver mode enable. This field will be used instead of ctrl_dfdqs in DVFS0 mode. 1'b0: Single-ended DQS 1'b1: Differential DQS
29	RW	0x1	dvfs0_rodt_disable Read ODT(On-Die-Termination) disable signal during DVFS0 mode. It will be used instead of ctrl_rodt_disable during DVFS0 mode. 1'b1: Read ODT disabled. Drive ctrl_read_p* to 0. If using LPDDR4, ctrl_read_p* will be always 0 by enabling this field. Io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are low. 1'b0: Read ODT enabled. Drive ctrl_read_p* normally. Io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are high only for read duration.
28	RW	0x0	dvfs0_write_se_dqs Single ended mode enable for write DQS. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for Write DQS. 1'b1: Single ended mode is enabled for Write DQS Caution: dvfs0_write_se_ck should be enabled using dvfs0_write_se_dqs in LPDDR4.
27	RW	0x0	dvfs0_write_se_ck Single ended mode enable for CK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for CK. 1'b1: Single ended mode is enabled for CK. Caution: dvfs0_write_se_dqs should be enabled using dvfs0_write_se_ck in LPDDR4. Caution: dvfs0_write_se_wck should be enabled using dvfs0_write_se_ck in LPDDR5.

Bit	Attr	Reset Value	Description
26	RW	0x0	dvfs0_write_se_wck Single ended mode enable for LP5 WCK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for WCK. 1'b1: Single ended mode is enabled for WCK. Caution: dvfs0_write_se_ck should be enabled using dvfs0_write_se_wck in LPDDR5
25:24	RW	0x0	dvfs0_pulld_dqs pull-up or down PDQS/NDQS signal control in DVFS0 mode. It will be used instead of ctrl_pulld_dqs in DVFS0 mode. Please refer to ctrl_pulld_dqs description.
23	RW	0x0	dvfs0_gateduradj_ext Default value is 0. This field is used for extend control range of dvfs0_gateduradj value. dvfs0_gateduradj_ext = 1'b0 (default) => Non Extended dvfs0_gateduradj_ext = 1'b1 => dvfs0_gateduradj[2:0] + 'h8
22	RW	0x0	dvfs0_gateadj_ext Default value is 0. This field is used for extend control range of dvfs0_gateadj value. dvfs0_gateadj_ext = 1'b0 (default) => Non Extended dvfs0_gateadj_ext = 1'b1 => dvfs0_gateadj[2:0] + 'h8
21	RW	0x0	dvfs0_readduradj_ext Default value is 0. This field is used for extend control range of dvfs0_readduradj value. dvfs0_readduradj_ext = 1'b0 (default) => Non Extended dvfs0_readduradj_ext = 1'b1 => dvfs0_readduradj[2:0] + 'h8
20	RW	0x0	dvfs0_readadj_ext Default value is 0. This field is used for extend control range of dvfs0_readadj value. dvfs0_readadj_ext = 1'b0 (default) => Non Extended dvfs0_readadj_ext = 1'b1 => dvfs0_readadj[2:0] + 'h8
19	RO	0x0	Reserved0 Reserved
18:17	RW	0x3	dvfs0_ndqs_maskdur_adj Single-ended NDQS input glitch masking duration adjustment during read ODT enable timing in DVFS0 mode. 2'b11: SE NDQS Glitch 3.5tCK Masking(default) 2'b10: SE NDQS Glitch 4.5tCK Masking 2'b00: SE NDQS Glitch 5.5tCK Masking
16	RW	0x0	dvfs0_shgate Gate signal control in DVFS0 mode. It will be used instead of ctrl_shgate in DVFS0 mode For LPDDR4, MR1 should be programmed so that read Pre-amble is 2nCK static and read Post-amble is 0.5tCK when shgate is 'h0.
15:12	RW	0x2	dvfs0_gateduradj This field will be used instead of ctrl_gateduradj during DVFS0 mode.

Bit	Attr	Reset Value	Description
11:8	RW	0x0	dvfs0_gateadj This field will be used instead of ctrl_gateadj during DVFS0 mode.
7:4	RW	0x0	dvfs0_readduradj It adjusts the duration cycle of "ctrl_read" on a clock cycle base in DVFS0 mode. MSB(bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.
3:0	RW	0x1	dvfs0_readadj It adjusts the enable time of "ctrl_read" on a clock cycle base in DVFS0 mode. MSB(bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the start cycle of high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.

DDRPHY_DVFS1_CON2

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	dvfs1_cmosrcv This field will control I/O receiver mode instead of ctrl_cmosrcv during DVFS1 mode.
30	RW	0x1	dvfs1_dfdqs Differential receiver mode enable. This field will be used instead of ctrl_dfdqs in DVFS1 mode. 1'b0: Single-ended DQS 1'b1: Differential DQS
29	RW	0x1	dvfs1_rodt_disable Read ODT(On-Die-Termination) disable signal during DVFS1 mode. It will be used instead of ctrl_rodt_disable during DVFS1 mode. 1'b1: Read ODT disabled. Drive ctrl_read_p* to 0. If using LPDDR4, ctrl_read_p* will be always 0 by enabling this field. Io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are low. 1'b0: Read ODT enabled. Drive ctrl_read_p* normally. Io_pdqs_read, io_ndqs_read, io_dq_read, io_dm_read are high only for read duration.
28	RW	0x0	dvfs1_write_se_dqs Single ended mode enable for write DQS. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for Write DQS. 1'b1: Single ended mode is enabled for Write DQS. Caution: Dvfs1_write_se_ck should be enabled using dvfs1_write_se_dqs in LPDDR4.

Bit	Attr	Reset Value	Description
27	RW	0x0	dvfs1_write_se_ck Single ended mode enable for CK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for CK. 1'b1: Single ended mode is enabled for CK. Caution: Dvfs1_write_se_dqs should be enabled using dvfs1_write_se_ck in LPDDR4. Caution: Dvfs1_write_se_wck should be enabled using dvfs1_write_se_ck in LPDDR5.
26	RW	0x0	dvfs1_write_se_wck Single ended mode enable for LP5 WCK. It can be enabled to reduce power consumption. 1'b0: Single ended mode is disabled for WCK. 1'b1: Single ended mode is enabled for WCK. Caution: Dvfs1_write_se_ck should be enabled using dvfs1_write_se_wck in LPDDR5.
25:24	RW	0x0	dvfs1_pulld_dqs pull-up or down PDQS/NDQS signal control in DVFS1 mode. It will be used instead of ctrl_pulld_dqs in DVFS0 mode. Please refer to ctrl_pulld_dqs description.
23	RW	0x0	dvfs1_gateduradj_ext Default value is 0. This field is used for extend control range of dvfs1_gateduradj value. dvfs1_gateduradj_ext = 1'b0 (default) => Non Extended dvfs1_gateduradj_ext = 1'b1 => dvfs1_gateduradj[2:0] + 'h8
22	RW	0x0	dvfs1_gateadj_ext Default value is 0. This field is used for extend control range of dvfs1_gateadj value. dvfs1_gateadj_ext = 1'b0 (default) => Non Extended dvfs1_gateadj_ext = 1'b1 => dvfs1_gateadj[2:0] + 'h8
21	RW	0x0	dvfs1_readduradj_ext Default value is 0. This field is used for extend control range of dvfs1_readduradj value. dvfs1_readduradj_ext = 1'b0 (default) => Non Extended dvfs1_readduradj_ext = 1'b1 => dvfs1_readduradj[2:0] + 'h8
20	RW	0x0	dvfs1_readadj_ext Default value is 0. This field is used for extend control range of dvfs1_readadj value. dvfs1_readadj_ext = 1'b0 (default) => Non Extended dvfs1_readadj_ext = 1'b1 => dvfs1_readadj[2:0] + 'h8
19	RW	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
18:17	RW	0x3	dvfs1_ndqs_maskdur_adj Single-ended NDQS input glitch masking duration adjustment during read ODT enable timing in DVFS1 mode. 2'b11: SE NDQS Glitch 3.5tCK Masking(default). 2'b10: SE NDQS Glitch 4.5tCK Masking. 2'b00: SE NDQS Glitch 5.5tCK Masking.
16	RW	0x0	dvfs1_shgate Gate signal control in DVFS1 mode. It will be used instead of ctrl_shgate in DVFS1 mode. For LPDDR4, MR1 should be programmed so that read Pre-amble is 2nCK static and read Post-amble is 0.5tCK when shgate is 'h0.
15:12	RW	0x2	dvfs1_gateduradj This field will be used instead of ctrl_gateduradj during DVFS1 mode.
11:8	RW	0x0	dvfs1_gateadj This field will be used instead of ctrl_gateadj during DVFS1 mode.
7:4	RW	0x0	dvfs1_readduradj It adjusts the duration cycle of "ctrl_read" on a clock cycle base in DVFS1 mode. MSB(bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.
3:0	RW	0x1	dvfs1_readadj It adjusts the enable time of "ctrl_read" on a clock cycle base in DVFS1 mode. MSB(bit3) controls direction: 1'b1: Subtract delay 1'b0: Add delay Bit[2:0] set delay value. It determines the start cycle of high duration of io_pdqs_read, io_ndqs_read, io_dq_read and io_dm_read if ctrl_rodt_disable is 0.

DDRPHY_DVFS0_CON3

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	dvfs0_ds1_vref Vref control for data_slice 1 in the internal mode during DVFS0 mode. It will be used instead of zq_ds1_vref in DVFS0 mode. It controls io_zq_ds_vref[11:6] in DVFS0 mode.
25:20	RW	0x00	dvfs0_ds0_vref Vref control for data_slice 0 in the internal mode during DVFS0 mode. It will be used instead of zq_ds0_vref in DVFS0 mode. It controls io_zq_ds_vref[5:0] in DVFS0 mode.
19:18	RW	0x0	Reserved0 Reserved
17:15	RW	0x7	dvfs0_zq_mode_dds Driver pull-down strength control for ctrl_slice in DVFS0 mode. It controls io_zq_mode_dds in DVFS0 mode.
14:12	RW	0x7	dvfs0_zq_mode_pdds Driver pull-up strength control for ctrl_slice in DVFS0 mode. It controls io_zq_mode_pdds in DVFS0 mode.
11:9	RW	0x7	dvfs0_zq_ds1_dds Driver pull-down strength control for data_slice1 in DVFS0 mode. It controls io_zq_ds_dds[5:3] in DVFS0 mode.

Bit	Attr	Reset Value	Description
8:6	RW	0x7	dvfs0_zq_ds1_pdds Driver pull-up strength control for data_slice1 in DVFS0 mode. It controls io_zq_ds_pdds[5:3] in DVFS0 mode.
5:3	RW	0x7	dvfs0_zq_ds0_dds Driver pull-down strength control for data_slice0 in DVFS0 mode. It controls io_zq_ds_dds[2:0] in DVFS0 mode.
2:0	RW	0x7	dvfs0_zq_ds0_pdds Driver pull-up strength control for data_slice0 in DVFS0 mode. It controls io_zq_ds_pdds[2:0] in DVFS0 mode.

DDRPHY_DVFS1_CON3
Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	dvfs1_ds1_vref Vref control for data_slice 1 in the internal mode during DVFS1 mode. It will be used instead of zq_ds1_vref in DVFS1 mode. It controls io_zq_ds_vref[11:6] in DVFS1 mode.
25:20	RW	0x00	dvfs1_ds0_vref Vref control for data_slice 0 in the internal mode during DVFS1 mode. It will be used instead of zq_ds0_vref in DVFS1 mode. It controls io_zq_ds_vref[5:0] in DVFS1 mode.
19:18	RW	0x0	Reserved0 Reserved
17:15	RW	0x7	dvfs1_zq_mode_dds Driver pull-down strength control for ctrl_slice in DVFS1 mode. It controls io_zq_mode_dds in DVFS1 mode.
14:12	RW	0x7	dvfs1_zq_mode_pdds Driver pull-up strength control for ctrl_slice in DVFS1 mode. It controls io_zq_mode_pdds in DVFS1 mode.
11:9	RW	0x7	dvfs1_zq_ds1_dds Driver pull-down strength control for data_slice1 in DVFS1 mode. It controls io_zq_ds_dds[5:3] in DVFS1 mode.
8:6	RW	0x7	dvfs1_zq_ds1_pdds Driver pull-up strength control for data_slice1 in DVFS1 mode. It controls io_zq_ds_pdds[5:3] in DVFS1 mode.
5:3	RW	0x7	dvfs1_zq_ds0_dds Driver pull-down strength control for data_slice0 in DVFS1 mode. It controls io_zq_ds_dds[2:0] in DVFS1 mode.
2:0	RW	0x7	dvfs1_zq_ds0_pdds Driver pull-up strength control for data_slice0 in DVFS1 mode. It controls io_zq_ds_pdds[2:0] in DVFS1 mode.

DDRPHY_DVFS0_CON4
Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved
21:19	RW	0x4	dvfs0_zq_ds1_term On-die-termination(ODT) resistor value selection for data_slice1 in DVFS0 mode. It determines io_zq_ds_mode_term[5:3]. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination

Bit	Attr	Reset Value	Description
18:16	RW	0x4	dvfs0_zq_ds0_term On-die-termination(ODT) resistor value selection for data_slice0 in DVFS0 mode. It determines io_zq_ds_mode_term[2:0]. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
15:14	RW	0x0	Reserved1 Reserved
13:8	RW	0x3f	vt_dvfs0_mcupd_req_cycle MC initiated mode update request cycle in DVFS0 mode for cs_phyupd FSM
7:6	RW	0x0	Reserved2 Reserved
5:0	RW	0x3f	vt_dvfs0_phyupd_req_cycle PHY initiated mode update request cycle in DVFS0 mode for cs_phyupd FSM

DDRPHY_DVFS1_CON4

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved
21:19	RW	0x4	dvfs1_zq_ds1_term On-die-termination(ODT) resistor value selection for data_slice1 in DVFS1 mode. It determines io_zq_ds_mode_term[5:3]. 3'b100 : 60 ohm far end VSSQ termination 3'b010 : 120 ohm far end VSSQ termination 3'b001 : 240 ohm far end VSSQ termination
18:16	RW	0x4	dvfs1_zq_ds0_term On-die-termination(ODT) resistor value selection for data_slice0 in DVFS1 mode. It determines io_zq_ds_mode_term[2:0]. 3'b100 : 60 ohm far end VSSQ termination 3'b010 : 120 ohm far end VSSQ termination 3'b001 : 240 ohm far end VSSQ termination
15:14	RW	0x0	Reserved1 Reserved
13:8	RW	0x3f	vt_dvfs1_mcupd_req_cycle MC initiated mode update request cycle in DVFS1 mode for cs_phyupd FSM
7:6	RW	0x0	Reserved2 Reserved
5:0	RW	0x3f	vt_dvfs1_phyupd_req_cycle PHY initiated mode update request cycle in DVFS1 mode for cs_phyupd FSM.

DDRPHY_CAL_WRLVL_STAT

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	Reserved0 Reserved
17:16	RO	0x0	wrlvl_fail_status It will be enable if there are no pass period after write leveling. It should be read by zero if leveling is done normally. Wrlvl_fail_status[1]: For Slice 1. Wrlvl_fail_status[0]: For Slice 0.

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	Reserved1 Reserved

DDRPHY_CAL_FAIL_STAT0

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved0 Reserved
15:8	RO	0x00	dq_fail_status1 It will be enabled if there is no pass period after Read or Write DQ Calibration. It should be read by zero if Calibration is done normally. (slice1)
7:0	RO	0x00	dq_fail_status0 It will be enabled if there is no pass period after Read or Write DQ Calibration. It should be read by zero if Calibration is done normally. (slice0)

DDRPHY_CAL_FAIL_STAT1

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved0 Reserved
1:0	RO	0x0	dm_fail_status It will be enabled if there is no pass period after Read or Write DM Calibration. It should be read by zero if Calibration is done normally. [1]: DM fail status for slice1 [0]: DM fail status for slice0

DDRPHY_CAL_GT_CS0_VWMC0

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	GT_VWMC1_cs0 Gate training code for data slice 1. It shows the number of fine step delay cells applied to gate signal after gate training.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	GT_VWMC0_cs0 Gate training code for data slice 0. It shows the number of fine step delay cells applied to gate signal after gate training.

DDRPHY_CAL_GT_CS0_CYC

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	Reserved0 Reserved
11:8	RO	0x0	GT_CYC1_cs0 Gate training cycle increment information for data slice 1. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.
7:4	RO	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
3:0	RO	0x0	GT_CYC0_cs0 Gate training cycle increment information for data slice 0. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.

DDRPHY_CAL_RD_VWMC0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	rd_vwmc1 Read DQ Calibration center code for data slice 1. It shows the information for the bit with the maximum center value between DQ[15:8].
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	rd_vwmc0 Read DQ Calibration center code for data slice 0. It shows the information for the bit with the maximum center value between DQ[7:0].

DDRPHY_CAL_RD_VWML0

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	rd_vwml1 Left code value in read valid window margin for Data Slice1. It shows the information for the bit with the maximum center value between DQ[15:8].
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	rd_vwml0 Left code value in read valid window margin for Data Slice0. It shows the information for the bit with the maximum center value between DQ[7:0].

DDRPHY_CAL_RD_VWMR0

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	rd_vwmr1 Right code value in read valid window margin for Data Slice1. It shows the information for the bit with the maximum center value between DQ[15:8].
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	rd_vwmr0 Right code value in read valid window margin for Data Slice0. It shows the information for the bit with the maximum center value between DQ[7:0].

DDRPHY_CAL_WR_VWMC0

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	wr_vwmc1 Write DQ Calibration centering code for data slice 1. It shows the information for the bit with minimum center code between DQ[15:8] and DM[1].
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	wr_vwmc0 Write DQ Calibration centering code for data slice 0. It shows the information for the bit with minimum center code between DQ[7:0] and DM[0].

DDRPHY_CAL_WR_VWML0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	wr_vwml1 Left Code Value in Write Valid Window Margin for Data Slice1. It shows the information for the bit with minimum center code between DQ[15:8] and DM[1].
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	wr_vwml0 Left code value in write valid window margin for Data Slice0. It shows the information for the bit with minimum center code between DQ[7:0] and DM[0].

DDRPHY_CAL_WR_VWMR0

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	wr_vwmr1 Right code value in write valid window margin for Data Slice1. It shows the information for the bit with minimum center code between DQ[15:8] and DM[1].
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	wr_vwmr0 Right code value in write valid window margin for Data Slice0. It shows the information for the bit with minimum center code between DQ[7:0] and DM[0].

DDRPHY_CAL_CON5

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved0 Reserved
10	RW	0x0	binary_en This feature is TBD.

Bit	Attr	Reset Value	Description
9:2	RW	0x00	wrtrn_cyc_th Write training cycle threshold. This is the minimum amount of delay line offset to determine cycle based delay on DQ/DM. For example, the first write training is completed with cycle = 1 and offset = 10 and wrtrn_cyc_th = 15. Because offset < wrtrn_cyc_th, PHY determines that cycle based delay should be reverted to 0, instead of 1. For the second write training cycle will be fixed to 0 and write training will progress increasing delay line code only. This is to guarantee the non-linearity cause by cycle delay not affect training result.
1	RW	0x0	wrtrn_cyc_en Write training cycle delay enable. if enabled, cycle based latency will be used along with DQ/DM delay line. (cycle delay = 0.5/1.0/1.5tCK) Enable this field for LPDDR4. It will reduce the VT calculation error caused by lock value variation as DQ/DM offset is reduced. Disable for other DRAM types.
0	RW	0x0	wrtrn_cyc_mode Cycle based write training mode. 1'b0: Cycle code for left edge and right edge are matched. This improves accuracy in training result but with limited training range (1GHz or over). 1'b1: Cycle code for left edge and right edge are not matched. Use for low frequencies (500MHz~1GHz).

DDRPHY_DVFS_UPD_CON0

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved
21:16	RW	0x3f	dvfs_mcupd_req_cycle For debug purpose. For mc-initiated update mode. It controls the number of cycle during which cs_dvfsupd FSM stays at ST_DVFS_C_VTC state.
15:14	RW	0x0	Reserved1 Reserved
13:8	RW	0x3f	dvfs_dvfs0_mcupd_req_cycle MC initiated mode update request cycle in DVFS0 mode for cs_dvfsupd FSM.
7:6	RW	0x0	Reserved2 Reserved
5:0	RW	0x3f	dvfs_dvfs1_mcupd_req_cycle MC initiated mode update request cycle in DVFS1 mode for cs_dvfsupd FSM.

DDRPHY_DVFS_UPD_CON1

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved
21:16	RW	0x3f	dvfs_phyupd_req_cycle For debug purpose. For phy-initated update mode. It controls the number of cycle during which cs_dvfsupd FSM stays at ST_DVFS_C_VTC state.
15:14	RW	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x3f	dvfs_dvfs0_phyupd_req_cycle PHY initiated mode update request cycle in DVFS0 mode for cs_dvfsupd FSM.
7:6	RW	0x0	Reserved2 Reserved
5:0	RW	0x3f	dvfs_dvfs1_phyupd_req_cycle PHY initiated mode update request cycle in DVFS1 mode for cs_dvfsupd FSM.

DDRPHY_RD_DESKEW_CENTER_CS0_CON_DM

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RDDMDeskewC1_cs0 Read DMI De-Skew center code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RDDMDeskewC0_cs0 Read DMI De-Skew center code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON0

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD0DeskewC1_cs0 Read DQ0 De-Skew center code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD0DeskewC0_cs0 Read DQ0 De-Skew center code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON1

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD1DeskewC1_cs0 Read DQ1 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD1DeskewC0_cs0 Read DQ1 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON2

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD2DeskewC1_cs0 Read DQ2 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved

Bit	Attr	Reset Value	Description
9:0	RO	0x000	RD2DeskewC0_cs0 Read DQ2 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON3
Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD3DeskewC1_cs0 Read DQ3 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD3DeskewC0_cs0 Read DQ3 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON4
Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD4DeskewC1_cs0 Read DQ4 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD4DeskewC0_cs0 Read DQ4 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON5
Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD5DeskewC1_cs0 Read DQ5 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD5DeskewC0_cs0 Read DQ5 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON6
Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD6DeskewC1_cs0 Read DQ6 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD6DeskewC0_cs0 Read DQ6 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS0_CON7
Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD7DeskewC1_cs0 Read DQ7 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD7DeskewC0_cs0 Read DQ7 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON0
Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR0DeskewC1_cs0 Write DQ0 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR0DeskewC0_cs0 Write DQ0 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON1
Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR1DeskewC1_cs0 Write DQ1 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR1DeskewC0_cs0 Write DQ1 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON2
Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR2DeskewC1_cs0 Write DQ2 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR2DeskewC0_cs0 Write DQ2 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON3
Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR3DeskewC1_cs0 Write DQ3 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved

Bit	Attr	Reset Value	Description
9:0	RO	0x000	WR3DeskewC0_cs0 Write DQ3 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON4
Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR4DeskewC1_cs0 Write DQ4 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR4DeskewC0_cs0 Write DQ4 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON5
Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR5DeskewC1_cs0 Write DQ5 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR5DeskewC0_cs0 Write DQ5 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON6
Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR6DeskewC1_cs0 Write DQ6 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR6DeskewC0_cs0 Write DQ6 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS0_CON7
Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR7DeskewC1_cs0 Write DQ7 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR7DeskewC0_cs0 Write DQ7 De-Skew Center Code for Data Slice0.

DDRPHY_DM_DESKEWC_CS0_CON0
Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	DMDeskewC1_cs0 Write DM De-Skew Center Code for Data Slice1. It will be the same as dm_vwmc1 right after the initial write training is done.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	DMDeskewC0_cs0 Write DM De-Skew Center Code for Data Slice0. It will be the same as dm_vwmc0 right after the initial write training is done.

DDRPHY_ECC_DESKEWC_CS0_CON0

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	ECCDeskewC1_cs0 Write ECC De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	ECCDeskewC0_cs0 Write ECC De-Skew Center Code for Data Slice0.

DDRPHY_VWMC_STAT0

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D0_VWMC1 DQ0 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D0_VWMC0 DQ0 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT3

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D1_VWMC1 DQ1 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D1_VWMC0 DQ1 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT6

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D2_VWMC1 DQ2 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D2_VWMC0 DQ2 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT9

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D3_VWMC1 DQ3 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D3_VWMC0 DQ3 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT12

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D4_VWMC1 DQ4 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D4_VWMC0 DQ4 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT15

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D5_VWMC1 DQ5 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D5_VWMC0 DQ5 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT18

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D6_VWMC1 DQ6 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D6_VWMC0 DQ6 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMC_STAT21
Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D7_VWMC1 DQ7 Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D7_VWMC0 DQ7 Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_DM_VWMC_STAT0
Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	DM_VWMC1 DM Center Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	DM_VWMC0 DM Center Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT0
Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D0_VWML1 DQ0 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D0_VWML0 DQ0 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT3
Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D1_VWML1 DQ1 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D1_VWML0 DQ1 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT6

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D2_VWML1 DQ2 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D2_VWML0 DQ2 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT9

Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D3_VWML1 DQ3 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D3_VWML0 DQ3 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT12

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D4_VWML1 DQ4 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D4_VWML0 DQ4 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT15

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D5_VWML1 DQ5 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D5_VWML0 DQ5 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT18

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D6_VWML1 DQ6 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D6_VWML0 DQ6 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWML_STAT21

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D7_VWML1 DQ7 Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D7_VWML0 DQ7 Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_DM_VWML_STAT0

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	DM_VWML1 DM Left Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	DM_VWML0 DM Left Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT0

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D0_VWMR1 DQ0 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D0_VWMR0 DQ0 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT3
Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D1_VWMR1 DQ1 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D1_VWMR0 DQ1 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT6
Address: Operational Base + offset (0x034C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D2_VWMR1 DQ2 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D2_VWMR0 DQ2 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT9
Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D3_VWMR1 DQ3 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D3_VWMR0 DQ3 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT12
Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D4_VWMR1 DQ4 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D4_VWMR0 DQ4 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT15
Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D5_VWMR1 DQ5 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D5_VWMR0 DQ5 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT18
Address: Operational Base + offset (0x037C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D6_VWMR1 DQ6 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D6_VWMR0 DQ6 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_VWMR_STAT21
Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	D7_VWMR1 DQ7 Right Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	D7_VWMR0 DQ7 Right Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_DM_VWMR_STAT0
Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:16	RO	0x000	DM_VWMR1 DM Right Code Code for Data Slice1. The latest read or write training result will be shown.
15:11	RO	0x00	Reserved1 Reserved
10:0	RO	0x000	DM_VWMR0 DM Right Code Code for Data Slice0. The latest read or write training result will be shown.

DDRPHY_DQ_IO_RDATA0
Address: Operational Base + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved0 Reserved
15:8	RO	0x00	DQ_IO_RD1 DQ I/O Read Data for DS1. This register simply mirrors the DQ[15:8] input value through io_dq_in[15:8]. This is used to read DQ during Command Bus training by S/W.
7:0	RO	0x00	DQ_IO_RD0 DQ I/O Read Data for DS0. This register simply mirrors the DQ[7:0] input value through io_dq_in[7:0]. This is used to read DQ during Command Bus training by S/W.

DDRPHY_VERSION_INFO_STAT0
Address: Operational Base + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x09080005	Version_Info Version Information

DDRPHY_ZQ_CON0
Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31	RW	0x1	zq_mode_lp4 VSSQ termination receiver mode selection for ctrl_slice. It controls io_zq_mode_lp4. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init_start falls at the beginning of DLL relocking period. 1'b1: Enable pull-down termination resistor only (Enable VSSQ-TERM mode of I/O) 1'b0: Deselects VSSQ-TERM mode of I/O.
30:28	RW	0x7	zq_mode_pdds Driver strength selection for ctrl_slice. It controls io_zq_mode_pdds. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init_start falls at the begining of DLL relocking period. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver Others: Reserved

Bit	Attr	Reset Value	Description
27	RW	0x1	zq_clk_en ZQ I/O Clock enable. It should be set to high before starting ZQ calibration. 1'b1: Enable io_zq_clk. 1'b0: Disable io_zq_clk.
26:24	RW	0x7	zq_mode_dds Driver strength selection for ctrl_slice. It controls io_zq_mode_dds. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init_start falls at the beginning of DLL relocking period. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver Others: Reserved
23:21	RW	0x4	zq_mode_term On-die-termination(ODT) resistor value selection for ctrl_slice. It controls io_zq_mode_term. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at the beginning of DLL relocking period. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination Others: Reserved
20	RW	0x0	zq_rgddr3 GDDR3 mode enable signal for ctrl_slice(High: GDDR3 mode). It controls io_zq_mode_rgddr3. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at the beginning of DLL relocking period.
19	RW	0x0	zq_mode_noterm Termination disable selection for ctrl_slice. It controls io_zq_mode_noterm. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at the beginning of DLL relocking period. 1'b1: Termination disable. 1'b0: Termination enable. Recommended setting LPDDR4: 1'b0(recommended) or 1'b1(when termination is not used)
18	RW	0x0	zq_clk_div_en Clock dividing enable for io_zq_clk. Divider setting is controlled by ctrl_zq_clk_div.
17:15	RW	0x0	zq_force_impn Immediate control code for pull-down for ctrl_slice. It controls io_zq_force_impn. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at the beginning of DLL relocking period.

Bit	Attr	Reset Value	Description
14:12	RW	0x7	zq_force_impp Immediate control code for pull-up for ctrl_slice. It controls io_zq_force_impp. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at the begining of DLL relocking period.
11:4	RW	0x40	zq_udt_dly ZQ I/O clock enable duration for auto calibration mode. Set zq_manual_str from 1'b0 to 1'b1 after setting this field to make it propagated to I/O. It will also be propagated to I/O during the frequency change duration after dfi_init start falls at the begining of DLL relocking period.
3:2	RW	0x1	zq_manual_mode Manual ZQ calibration mode selection 2'b00: Force calibration 2'b01: Long calibration 2'b10: Reserved for short calibration 2'b11: Reserved
1	RW	0x0	zq_manual_str Manual ZQ calibration start for ZQ pad.
0	RW	0x0	Reserved0 Should be zero.

DDRPHY_ZQ_CON1

Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	zq_cal_fsm zq calibration fsm register.
27:22	RO	0x00	Reserved0 Should be zero.
21:16	RW	0x14	zq_vref Vref control for ctrl_slice in the internal mode. It controls io_zq_vref[5:0]. Please refer to SSTL IO datasheet for use cases.
15:9	RO	0x00	Reserved1 Should be zero.
8:6	RO	0x0	zq_pmon Control code found by auto calibration for pull-up. It shows the result of ZQ calibration from ZQ PAD.
5:3	RO	0x0	zq_nmon Control code found by auto calibration for pull-down. It shows the result of ZQ calibration from ZQ PAD.
2	RO	0x0	zq_mon Calibration fail indication (High: calibration failed) It shows the result of ZQ calibration from ZQ PAD.
1	RO	0x0	zq_pending Auto calibration enable status
0	RO	0x0	zq_done ZQ Calibration is finished. The response for zq_manual_str from ZQ pad.

DDRPHY_ZQ_CON2

Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Should be zero.

Bit	Attr	Reset Value	Description
21:16	RW	0x1e	zq_upd_ack_cycle For debug purpose. This register controls the number of cycle during which cs_phyupd_FSM stays at ST_UPD_ACK stat when ZQ periodic update occurs. It affects the duration of dfi_phyupd_ack = 1.
15:0	RW	0x0002	ctrl_zq_clk_div ZQ Clock(=io_zq_clk) divider setting value. The frequency will be determined by the following formula. This field should be set before the first ZQ calibration and should not be changed afterwards. ctrl_zq_clk_div should be between 1 to 7. "io_zq_clk frequency"(MHz) = "clk_dfi frequency"(MHz) / ((ctrl_zq_clk_div+1)*2)

DDRPHY_ZQ_CON3

Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved
21:19	RW	0x7	zq_ck_dds Driver pull-down strength control for CK pad. It controls io_zq_ck_dds. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
18:16	RW	0x7	zq_ck_pdds Driver pull-up strength control for CK pad. It controls io_zq_ck_pdds.
15:14	RW	0x0	Reserved1 Reserved
13:11	RW	0x7	zq_ds1_dds Driver pull-down strength control for data_slice1. It controls io_zq_ds_dds[5:3]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
10:8	RW	0x7	zq_ds1_pdds Driver pull-up strength control for data_slice1. It controls io_zq_ds_pdds[5:3].
7:6	RW	0x0	Reserved2 Reserved
5:3	RW	0x7	zq_ds0_dds Driver pull-down strength control for data_slice0. It controls io_zq_ds_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
2:0	RW	0x7	zq_ds0_pdds Driver pull-up strength control for data_slice0. It controls io_zq_ds_pdds[2:0].

DDRPHY_ZQ_CON5
Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Should be zero
26:24	RW	0x7	zq_reset_dds Driver pull-down strength control for reset. It controls io_zq_reset_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
23:22	RW	0x0	Reserved1 Should be zero
21:19	RW	0x7	zq_cke1_dds Driver pull-down strength control for cke(rank1). It controls io_zq_cke1_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
18:16	RW	0x7	zq_cke0_dds Driver pull-down strength control for cke(rank0). It controls io_zq_cke0_dds[2:0]. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
15:0	RW	0x003f	Reserved2 Should be zero

DDRPHY_ZQ_CON6
Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved0 Should be zero
13:11	RW	0x4	zq_ds1_term On-die-termination(ODT) resistor value selection for datal_slice1. It determines io_zq_ds_mode_term[5:3]. Please refer to SSTL I/O datasheet for specific termination settings. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
10	RW	0x0	zq_ds1_rgddr3 GDDR3 mode enable signal for data_slice1(High: GDDR3 mode). It controls io_zq_ds_rgddr[1].

Bit	Attr	Reset Value	Description
9	RW	0x0	zq_ds1_noterm Termination disable selection for data_slice1. It controls io_zq_ds_noterm[1]. 1'b1: Termination disable. 1'b0: Termination enable. LPDDR4: 1'b0(recommended) or 1'b1(when termination is not used)
8	RW	0x1	zq_ds1_lp4 VSSQ termination receiver mode selection for data_slice1. It controls io_zq_ds_lp4[1]. 1'b1: Enable pull-down termination resistor only (Enable VSSQ-TERM)
7:6	RW	0x0	Reserved1 Should be zero
5:3	RW	0x4	zq_ds0_term On-die-termination(ODT) resistor value selection for datal_slice0. It determines io_zq_ds_mode_term[2:0]. Please refer to SSTL I/O datasheet for specific termination settings. 3'b100: 60 ohm far end VSSQ termination 3'b010: 120 ohm far end VSSQ termination 3'b001: 240 ohm far end VSSQ termination
2	RW	0x0	zq_ds0_rgddr3 GDDR3 mode enable signal for data_slice0(High: GDDR3 mode). It controls io_zq_ds_rgddr[0].
1	RW	0x0	zq_ds0_noterm Termination disable selection for data_slice0. It controls io_zq_ds_noterm[0]. 1'b1: Termination disable. 1'b0: Termination enable. LPDDR4: 1'b0(recommended) or 1'b1(when termination is not used)
0	RW	0x1	zq_ds0_lp4 VSSQ termination receiver mode selection for data_slice0. It controls io_zq_ds_lp4[0]. 1'b1: Enable pull-down termination resistor only (Enable VSSQ-TERM)

DDRPHY_ZQ_CON9

Address: Operational Base + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved
15	RW	0x0	zq_ds1_vref_pd Vref power down for data_slice1. It controls io_zq_ds_vref_pd[1].
14	RW	0x0	zq_ds1_vref_fsbst Vref fast boost mode control for data_slice1. It controls io_zq_ds_vref_fsbst[1]. 1'b0: Normal mode 1'b1: Fast boost mode
13:8	RW	0x14	zq_ds1_vref Vref control (VSEL5~VSEL0) for data_slice 1 in the internal mode. It controls io_zq_ds_vref[11:6].
7	RW	0x0	zq_ds0_vref_pd Vref power down for data_slice0. It controls io_zq_ds_vref_pd[0].

Bit	Attr	Reset Value	Description
6	RW	0x0	zq_ds0_vref_fsbst Vref fast boost mode control for data_slice0. It controls io_zq_ds_vref_fsbst[0]. 1'b0: Normal mode 1'b1: Fast boost mode
5:0	RW	0x14	zq_ds0_vref Vref control (VSEL5~VSEL0) for data_slice 0 in the internal mode. It controls io_zq_ds_vref[5:0].

DDRPHY_ZQ_CON12
Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved0 Reserved
13:11	RW	0x0	zq_ds1_impn Immediate control code for pull-down for data_slice 1. It controls io_zq_ds_impn[5:3].
10:8	RW	0x7	zq_ds1_impp Immediate control code for pull-up for data_slice 1. It controls io_zq_ds_impp[5:3].
7:6	RW	0x0	Reserved1 Should be zero.
5:3	RW	0x0	zq_ds0_impn Immediate control code for pull-down for data_slice 0. It controls io_zq_ds_impn[2:0].
2:0	RW	0x7	zq_ds0_impp Immediate control code for pull-up for data_slice 0. It controls io_zq_ds_impp[2:0].

DDRPHY_TESTIRCV_CON0
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved0 Reserved
20:18	RW	0x2	zq_mode_testizq zq short cal mode control. It controls U_PHYIO_SLICE/U_IO_SLICE/IMPCNT_IO_DS1/TESTIZQ[1:0]. zq_mode_tetsizq[1] controls i_zctrl_update_opt, zq_mode_testizq[0] controls i_zctrl_short_opt in ZCTRL zq_mode_testizq[2] controls zctrl_tune_opt, Option to control calibration sequence 1'b0: (Default) Pull-Down and Pull-Up are calibrated at the same time. 1'b1: After calibrated Pull-Down, Pull-Up is calibrated. It controls U_PHYIO_SLICE/U_IO_SLICE/IMPCNT_IO_DS1/ZCTRL_PU_MODE_SEL.
17	RW	0x0	zq_ds1_ibias_ctrl_en Impcnt bias current control enable for DS1. Controls io_zq_ds_ibias_ctrl_en[1] under PHYIO_SLICE.
16	RW	0x0	zq_ds0_ibias_ctrl_en Impcnt bias current control enable for DS0. Controls io_zq_ds_ibias_ctrl_en[0] under PHYIO_SLICE.

Bit	Attr	Reset Value	Description
15:14	RW	0x0	zq_ds1_ibias_ctrl Impcnt bias current control for DS1. Controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE.
13:12	RW	0x0	zq_ds0_ibias_ctrl Impcnt bias current control for DS0. Controls io_zq_ds_ibias_ctrl[1:0] under PHYIO_SLICE.
11	RW	0x0	Reserved1 Reserved
10	RW	0x0	zq_mode_ibias_ctrl_en Impcnt bias current control enable for CS. Controls io_zq_mode_ibias_ctrl_en under PHYIO_SLICE.
9:8	RW	0x0	zq_mode_ibias_ctrl Impcnt bias current control for CS. Controls io_zq_mode_ibias_ctrl under PHYIO_SLICE.
7:4	RW	0x0	dqs1_testircv DQS1 receiver test mode control. Controls io_dqs1_testircv under PHYIO_SLICE.
3:0	RW	0x0	dqs0_testircv DQS0 receiver test mode control. Controls io_dqs0_testircv under PHYIO_SLICE.

DDRPHY_WR_DESKEWC_CS1_CON0
Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR0DeskewC1_cs1 Write DQ0 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR0DeskewC0_cs1 Write DQ0 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS1_CON1
Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR1DeskewC1_cs1 Write DQ1 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR1DeskewC0_cs1 Write DQ1 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS1_CON2
Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR2DeskewC1_cs1 Write DQ2 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved

Bit	Attr	Reset Value	Description
9:0	RO	0x000	WR2DeskewC0_cs1 Write DQ2 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS1_CON3
Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR3DeskewC1_cs1 Write DQ3 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR3DeskewC0_cs1 Write DQ3 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS1_CON4
Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR4DeskewC1_cs1 Write DQ4 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR4DeskewC0_cs1 Write DQ4 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS1_CON5
Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR5DeskewC1_cs1 Write DQ5 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR5DeskewC0_cs1 Write DQ5 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS1_CON6
Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR6DeskewC1_cs1 Write DQ6 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR6DeskewC0_cs1 Write DQ6 De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWC_CS1_CON7
Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR7DeskewC1_cs1 Write DQ7 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR7DeskewC0_cs1 Write DQ7 De-Skew Center Code for Data Slice0.

DDRPHY_DM_DESKEWC_CS1_CON0
Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	DMDeskewC1_cs1 Write DM De-Skew Center Code for Data Slice1. It will be the same as dm_vwmc1 right after the initial write training is done.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	DMDeskewC0_cs1 Write DM De-Skew Center Code for Data Slice0. It will be the same as dm_vwmc0 right after the initial write training is done.

DDRPHY_ECC_DESKEWC_CS1_CON0
Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	ECCDeskewC1_cs1 Write ECC De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	ECCDeskewC0_cs1 Write ECC De-Skew Center Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON0
Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR0DeskewL1_cs0 Write DQ0 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR0DeskewL0_cs0 Write DQ0 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON1
Address: Operational Base + offset (0x049C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR1DeskewL1_cs0 Write DQ1 De-Skew Left Code for Data Slice1.

Bit	Attr	Reset Value	Description
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR1DeskewL0_cs0 Write DQ1 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON2
Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR2DeskewL1_cs0 Write DQ2 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR2DeskewL0_cs0 Write DQ2 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON3
Address: Operational Base + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR3DeskewL1_cs0 Write DQ3 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR3DeskewL0_cs0 Write DQ3 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON4
Address: Operational Base + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR4DeskewL1_cs0 Write DQ4 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR4DeskewL0_cs0 Write DQ4 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON5
Address: Operational Base + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR5DeskewL1_cs0 Write DQ5 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR5DeskewL0_cs0 Write DQ5 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON6

Address: Operational Base + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR6DeskewL1_cs0 Write DQ6 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR6DeskewL0_cs0 Write DQ6 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS0_CON7
Address: Operational Base + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR7DeskewL1_cs0 Write DQ7 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR7DeskewL0_cs0 Write DQ7 De-Skew Left Code for Data Slice0.

DDRPHY_DM_DESKEWL_CS0_CON0
Address: Operational Base + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	DMDeskewL1_cs0 Write DM De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	DMDeskewL0_cs0 Write DM De-Skew Left Code for Data Slice0.

DDRPHY_ECC_DESKEWL_CS0_CON0
Address: Operational Base + offset (0x04F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	ECCDeskewL1_cs0 Write ECC De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	ECCDeskewL0_cs0 Write ECC De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON0
Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR0DeskewL1_cs1 Write DQ0 De-Skew Left Code for Data Slice1.

Bit	Attr	Reset Value	Description
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR0DeskewL0_cs1 Write DQ0 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON1
Address: Operational Base + offset (0x050C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR1DeskewL1_cs1 Write DQ1 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR1DeskewL0_cs1 Write DQ1 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON2
Address: Operational Base + offset (0x0518)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR2DeskewL1_cs1 Write DQ2 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR2DeskewL0_cs1 Write DQ2 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON3
Address: Operational Base + offset (0x0524)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR3DeskewL1_cs1 Write DQ3 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR3DeskewL0_cs1 Write DQ3 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON4
Address: Operational Base + offset (0x0530)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR4DeskewL1_cs1 Write DQ4 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR4DeskewL0_cs1 Write DQ4 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON5

Address: Operational Base + offset (0x053C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR5DeskewL1_cs1 Write DQ5 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR5DeskewL0_cs1 Write DQ5 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON6

Address: Operational Base + offset (0x0548)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR6DeskewL1_cs1 Write DQ6 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR6DeskewL0_cs1 Write DQ6 De-Skew Left Code for Data Slice0.

DDRPHY_WR_DESKEWL_CS1_CON7

Address: Operational Base + offset (0x0554)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	WR7DeskewL1_cs1 Write DQ7 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	WR7DeskewL0_cs1 Write DQ7 De-Skew Left Code for Data Slice0.

DDRPHY_DM_DESKEWL_CS1_CON0

Address: Operational Base + offset (0x0560)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	DMDeskewL1_cs1 Write DM De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	DMDeskewL0_cs1 Write DM De-Skew Left Code for Data Slice0.

DDRPHY_ECC_DESKEWL_CS1_CON0

Address: Operational Base + offset (0x0564)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	ECCDeskewL1_cs1 Write ECC De-Skew Left Code for Data Slice1.

Bit	Attr	Reset Value	Description
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	ECCDeskewL0_cs1 Write ECC De-Skew Left Code for Data Slice0.

DDRPHY_RD_DQS_VWML_CS0_CON0
Address: Operational Base + offset (0x0574)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved0 Reserved
24:16	RO	0x000	RDDQSVWML1_cs0 Read DQS Left Code for Data Slice1.
15:9	RO	0x00	Reserved1 Reserved
8:0	RO	0x000	RDDQSVWML0_cs0 Read DQS Left Code for Data Slice0.

DDRPHY_RD_DQS_VWMC_CS0_CON0
Address: Operational Base + offset (0x0580)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved0 Reserved
24:16	RO	0x000	RDDQSVWMC1_cs0 Read DQS Center Code for Data Slice1.
15:9	RO	0x00	Reserved1 Reserved
8:0	RO	0x000	RDDQSVWMC0_cs0 Read DQS Center Code for Data Slice0.

DDRPHY_GT_STATUS_CON0
Address: Operational Base + offset (0x058C)

Bit	Attr	Reset Value	Description
31	RO	0x0	fifo_rd_fail_ds1 Command FIFO Read fail flag for Auto DQS clean mode for DS1. It is set to 1 if FIFO read is asserted when FIFO empty is set.
30	RO	0x0	fifo_rd_fail_ds0 Command FIFO Read fail flag for Auto DQS clean mode for DS0. It is set to 1 if FIFO read is asserted when FIFO empty is set.
29	RO	0x0	fifo_wr_fail_ds1 Command FIFO Write fail flag for Auto DQS clean mode for DS1. It is set to 1 if FIFO write is asserted when FIFO full is set.
28	RO	0x0	fifo_wr_fail_ds0 Command FIFO Write fail flag for Auto DQS clean mode for DS0. It is set to 1 if FIFO write is asserted when FIFO full is set.
27:16	RO	0x000	Reserved0 Reserved
15	RO	0x0	gt_preamble_start_ds1_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank1). Gt_preamble_start means Gate located at read dqs preamble state.

Bit	Attr	Reset Value	Description
14	RO	0x0	gt_highz_start_ds1_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank1). Gt_highz_start means Gate located at highz state.
13	RO	0x0	gt_dqsh_start_ds1_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank1). Gt_dqsh_start means Gate located at dqs high state.
12	RO	0x0	gt_max_cyc_ds1_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank1). Gt_max_cyc means gate training fail.
11	RO	0x0	gt_preamble_start_ds0_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank1). Gt_preamble_start means Gate located at read dqs preamble state.
10	RO	0x0	gt_highz_start_ds0_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank1). Gt_highz_start means Gate located at highz state.
9	RO	0x0	gt_dqsh_start_ds0_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank1). Gt_dqsh_start means Gate located at dqs high state.
8	RO	0x0	gt_max_cyc_ds0_cs1 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank1). Gt_max_cyc means gate training fail.
7	RO	0x0	DQS_RESP1_fall_cs1 DQS response searched by gate fall edge for data_slice1. DQS sampled at ctrl_gate falling edge for data_slice1 to monitor gate training result for rank1.
6:5	RO	0x0	Reserved1 Reserved
4	RO	0x0	DQS_RESP1_cs1 DQS response searched by gate rise edge for data_slice1. DQS sampled at ctrl_gate rising edge for data_slice1 to monitor gate training result for rank1.
3	RO	0x0	DQS_RESP0_fall_cs1 DQS response searched by gate fall edge for data_slice0. DQS sampled at ctrl_gate falling edge for data_slice0 to monitor gate training result for rank1.
2:1	RO	0x0	Reserved2 Reserved

Bit	Attr	Reset Value	Description
0	RO	0x0	DQS_RESP0_cs1 DQS response searched by gate rise edge for data_slice0. DQS sampled at ctrl_gate rising edge for data_slice0 to monitor gate training result for rank1.

DDRPHY_GT_STATUS_CON1

Address: Operational Base + offset (0x0590)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved0 Reserved
15	RO	0x0	gt_preamble_start_ds1_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank0). Gt_preamble_start means Gate located at read dqs preamble state.
14	RO	0x0	gt_highz_start_ds1_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank0). Gt_highz_start means Gate located at highz state.
13	RO	0x0	gt_dqsh_start_ds1_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank0). Gt_dqsh_start means Gate located at dqs high state.
12	RO	0x0	gt_max_cyc_ds1_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 1, rank0). Gt_max_cyc means gate training fail.
11	RO	0x0	gt_preamble_start_ds0_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank0). Gt_preamble_start means Gate located at read dqs preamble state.
10	RO	0x0	gt_highz_start_ds0_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank0). Gt_highz_start means Gate located at highz state.
9	RO	0x0	gt_dqsh_start_ds0_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank0). Gt_dqsh_start means Gate located at dqs high state.
8	RO	0x0	gt_max_cyc_ds0_cs0 This is debug feature for gate training This is a STATUS between Gate and DQS for 1st MPC(read) at DVFS/periodic gate training(Data slice 0, rank0). Gt_max_cyc means gate training fail.

Bit	Attr	Reset Value	Description
7	RO	0x0	DQS_RESP1_fall_cs0 DQS response searched by gate fall edge for data_slice1. DQS sampled at ctrl_gate falling edge for data_slice1 to monitor gate training result for rank0.
6:5	RO	0x0	Reserved1 Reserved
4	RO	0x0	DQS_RESP1_cs0 DQS response searched by gate rise edge for data_slice1 DQS sampled at ctrl_gate rising edge for data_slice1 to monitor gate training result for rank0.
3	RO	0x0	DQS_RESP0_fall_cs0 DQS response searched by gate fall edge for data_slice0. DQS sampled at ctrl_gate falling edge for data_slice0 to monitor gate training result for rank0.
2:1	RO	0x0	Reserved2 Reserved
0	RO	0x0	DQS_RESP0_cs0 DQS response searched by gate rise edge for data_slice0. DQS sampled at ctrl_gate rising edge for data_slice0 to monitor gate training result for rank0.

DDRPHY_GT_FSM_STATUS_CON1

Address: Operational Base + offset (0x0594)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved0 Reserved
30	RO	0x0	GATE_LOFSM_IDLE_ds1 FSM flag of gate signal idle location for slice1
29	RO	0x0	GATE_LOFSM_UNKNOWN_ds1 FSM flag of gate signal unknown location for slice1
28	RO	0x0	GATE_LOFSM_PREAMBLE_ds1 FSM flag of gate signal preamble location for slice1
27:26	RO	0x0	gate_fail_status_ds1 Fail status for gate training at slice1. gate_fail_status_ds1[1] is for rank 1, gate_fail_status_ds1[0] is for rank0. If each bit is set to high, it indicates that dqs rising edge is not found during gate training.
25:24	RO	0x0	GATE_LOCATION_FSM_ds1 FSM of gate signal location for slice1
23	RO	0x0	Reserved2 Reserved
22	RO	0x0	GATE_LOFSM_IDLE_ds0 FSM flag of gate signal idle location for slice0
21	RO	0x0	GATE_LOFSM_UNKNOWN_ds0 FSM flag of gate signal unknown location for slice0
20	RO	0x0	GATE_LOFSM_PREAMBLE_ds0 FSM flag of gate signal preamble location for slice0
19:18	RO	0x0	gate_fail_status_ds0 Fail status for gate training at slice0. gate_fail_status_ds0[1] is for rank 1, gate_fail_status_ds0[0] is for rank0. If each bit is set to high, it indicates that dqs rising edge is not found during gate training.
17:16	RO	0x0	GATE_LOCATION_FSM_ds0 FSM of gate signal location for slice0

Bit	Attr	Reset Value	Description
15	RO	0x0	GATE_FSM_IDLE_DS1 IDLE state flag of Gate Training FSM for slice 1
14	RO	0x0	GATE_FSM_INIT_DS1 Initial state flag of Gate Training FSM for slice 1
13	RO	0x0	GATE_FSM_PERIODIC_DS1 Periodic state flag of Gate Training FSM for slice 1
12	RO	0x0	GATE_FSM_RESP_DS1 Response state flag of Gate Training FSM for slice 1
11	RO	0x0	Reserved4 Reserved
10:8	RO	0x0	GATE_FSM_STATUS_ds1 FSM monitoring signal for slice1. It shows CS_DsRdlvl FSM status in gate_training.
7	RO	0x0	GATE_FSM_IDLE_DS0 IDLE state flag of Gate Training FSM for slice 0
6	RO	0x0	GATE_FSM_INIT_DS0 Initial state flag of Gate Training FSM for slice 0
5	RO	0x0	GATE_FSM_PERIODIC_DS0 Periodic state flag of Gate Training FSM for slice 0
4	RO	0x0	GATE_FSM_RESP_DS0 Response state flag of Gate Training FSM for slice 0
3	RO	0x0	Reserved5 Reserved
2:0	RO	0x0	GATE_FSM_STATUS_ds0 FSM monitoring signal for slice0. It shows CS_DsRdlvl FSM status in gate_training.

DDRPHY_CAL_GT_CS1_VWMC0

Address: Operational Base + offset (0x05E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	GT_VWMC1_cs1 Gate Training code for data slice 1. It shows the number of fine step delay cells applied to gate signal after gate training.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	GT_VWMC0_cs1 Gate Training code for data slice 0. It shows the number of fine step delay cells applied to gate signal after gate training.

DDRPHY_CAL_GT_CS1_CYC

Address: Operational Base + offset (0x05F0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	Reserved0 Reserved
11:8	RO	0x0	GT_CYC1_cs1 Gate training cycle increment information for data slice 1. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.
7:4	RO	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
3:0	RO	0x0	GT_CYC0_cs1 Gate training cycle increment information for data slice 0. It represents how much ctrl_gate signal is delayed by DFI PHY clock cycle.

DDRPHY_CBT_CON5
Address: Operational Base + offset (0x05F4)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved0 Reserved
20:16	RW	0x0d	cbt_tDSTRAIN LPDDR4 CBT : tDStrain(Data setup for VREF training mode) timing parameter setting register. * RU(1/tCK), tCK = Memory clock frequency
15	RW	0x0	Reserved1 Reserved
14:10	RW	0x0d	cbt_tDHTRAIN LPDDR4 CBT : tDHtrain(Data hold for VREF training mode) timing parameter setting register. * RU(1/tCK), tCK = Memory clock frequency
9:0	RW	0x00a	Reserved2 Reserved

DDRPHY_CBT_CMD
Address: Operational Base + offset (0x05FC)

Bit	Attr	Reset Value	Description
31:12	RW	0x00080	Reserved0 Reserved
11:10	RW	0x1	cbt_cs Chip select during Command Bus Training. In one CBT procedure, only one bit of cbt_cs[1:0] should be enabled. 2'b01: rank0 2'b10: rank1
9:8	RW	0x0	Reserved1 Reserved
7:0	RW	0x3f	cbt_ca_pattern Predefined CA pattern that will be used during Command Bus Training. io_adct_out will be set to cbt_ca_pattern.

DDRPHY_CBT_CON0
Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31	RW	0x0	cbt_sw_mode SW Command Bus training code update control. This field will be enabled when restoring the previous command bus training registers. 1'b1: SW_CA*DeSkewCode, SW_CS*DeSkewCode will be written to internal command bus training code. 1'b0: SW_CA*DeSkewCode, SW_CS*DeSkewCode will be not written to internal command bus training code.
30:27	RW	0x0	Reserved4 Reserved

Bit	Attr	Reset Value	Description
26:25	RW	0x0	cbt_vref_dqs_en It is used for S/W CBT CA Vref setting mode. If it is enabled, DQS will be driven for Vref setting during S/W CBT. 2'b01 : In case of CS0 CBT, DS0(DQS[0], DQSB[0]) enable for CA Vref setting 2'b10 : In case of CS1 CBT, DS1(DQS[1], DQSB[1]) enable for CA Vref setting
24:23	RW	0x0	Reserved3 Reserved
22:21	RW	0x0	cbt_vref_dq_en It is used for S/W CBT CA Vref setting mode. If it is enabled, CA Vref setting value will be driven on DQ bus. 2'b01 : In case of CS0 CBT, DS0(DQ[7:0]) enable for CA Vref setting 2'b10 : In case of CS1 CBT, DS1(DQ[15:8]) enable for CA Vref setting
20:12	RO	0x03e	Reserved1 Reserved
11	RW	0x0	cbt_cs_coarse_dis CBT cs coarse disable control.
10:8	RO	0x2	Reserved0 Reserved
7:0	RW	0x4d	cbt_ca_vref CA Vref setting value which will be driven on DQ when Command bus training. Refer to LPDDR4 MR12 register information.

DDRPHY_CBT_CON2

Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31	RW	0x0	cbt_vref_set_en LPDDR5 CBT: CA Vref setting value will be driven after CBT_CON2.cbt_tDSTRAIN_LP5 when the register is enabled .
30	RW	0x0	cbt_dq_rcv_en LPDDR5 CBT: PHY can be receive the captured data from memory with DQ receiver mode if the register is enabled.
29	RW	0x0	cbt_start LPDDR5 CBT: DQ[7] will be high to configure the memory CA calibration state.
28	RW	0x0	cbt_vref_pre_en LPDDR5 CBT: DMI will be low before changing the CA setting value during CBT.
27	RW	0x0	cbt_wck_en LPDDR5 CBT: Enable WCK toggle to set the CA Vref value by DQ bus during CBT mode.
26	RO	0x0	Reserved0 Reserved
25	RW	0x0	cbt_ca_shift_cycle Shift the CA cycle register, if cbt_ca_shift_cycle is enabled, CA is generated after 1cycle. Cbt_ca_shift_cycle should be used with CBT_CON0.cbt_sw_mode.
24	RW	0x0	cbt_cs_shift_cycle Shift the CS cycle register, if cbt_cs_shift_cycle is enabled, CS is generated after 1cycle. Cbt_cs_shift_cycle should be used with CBT_CON0.cbt_sw_mode.

Bit	Attr	Reset Value	Description
23:16	RW	0x00	cbt_dqdm_sel LPDDR5 CBT: DQ[7], DMI select pin cbt_dqdm_sel should be set as 0x80. Other setting is not supported.
15:11	RW	0x0c	cbt_tWCK2DQ7 LPDDR5 CBT : tWCK2DQ7(Set-up margin between DQ7 and WCK) timing parameter setting register. RU(5/tCK), tCK = Memory clock frequency
10:6	RW	0x0c	cbt_tDSTRAIN_LP5 LPDDR5 CBT : tDStrain(Data Setup for Vref Training Mode) timing parameter setting register. RU(5/tCK), tCK = Memory clock frequency
5:0	RO	0x00	Reserved2 Reserved

DDRPHY_CBT_CON3

Address: Operational Base + offset (0x060C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved1 Reserved
23:22	RW	0x3	cbt_cke CKE during command bus training. It controls the value driven on io_cke_out[1:0] during command bus training.
21:20	RW	0x0	cbt_odt_ca CA ODT during command bus training. It controls the value driven on io_odt_out[1:0] during command bus training.
19	RW	0x1	cbt_reset RESET during command bus training. It controls the value driven on io_reset_out during command bus training.
18	RW	0x0	cbt_cmd_cs_vwml Reserved
17	RW	0x0	cbt_cmd_cs_vwmr Command enable for CS VWMR search during command bus training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_patttern, and io_ck_out will be gated until io_cs_out is driven to cbt_cs.
16	RW	0x0	cbt_cmd_ca_vwml Command enable for CA VWML search during command bus training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_patttern for 1 DFI PHY clock cycle. io_cs_out and io_adct_out will be change at the same io_ck_out edge.
15	RW	0x0	cbt_cmd_ca_vwmr Command enable for CA VWMR search during command bus training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_patttern for 1 DFI PHY clock cycle. io_adct_out will be changed 1 DFI PHY clock after io_cs_out is changed.
14	RW	0x0	cbt_cmd_clear Command enable to set the CA feedback from DRAM ~cbt_ca_pattern during Command Bus Training. io_adct_out will be set to ~cbt_ca_pattern when this field is set to high.

Bit	Attr	Reset Value	Description
13	RW	0x0	cbt_cmd_cs_vwml_fine Command enable for CS VWML FINE search during Command Bus Training. CS Fine training is to find the precise location of CS considering CK SSN, which is not applied in the first CS training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_patttern for 1 DFI PHY clock cycle. io_cs_out and io_adct_out will be change at the same io_ck_out edge.
12	RW	0x0	cbt_cmd_cs_vwmr_fine Command enable for CS VWMR FINE search during Command Bus Training. CS Fine training is to find the precise location of CS considering CK SSN, which is not applied in the first CS training. If enabled, io_cs_out[1:0] will be set to cbt_cs for 1 DFI PHY clock cycle and io_adct_out will be set to cbt_ca_patttern for 1 DFI PHY clock cycle. io_adct_out will be changed 1 DFI PHY clock after io_cs_out is changed.
11:2	RO	0x000	Reserved0 Reserved
1	RW	0x0	cbt_hw_cal_start LPDDR4 HW calibration start signal
0	RW	0x0	cbt_en LPDDR5 CBT mode enable

DDRPHY_RD_DESKEW_LEFT_CS0_CON_DM
Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RDDMDeskewLeft1_cs0 Read DMI De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RDDMDeskewLeft0_cs0 Read DMI De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON0
Address: Operational Base + offset (0x0614)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD0DeskewLeft1_cs0 Read DQ0 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD0DeskewLeft0_cs0 Read DQ0 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON1
Address: Operational Base + offset (0x0620)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD1DeskewLeft1_cs0 Read DQ1 De-Skew Left Code for Data Slice1.

Bit	Attr	Reset Value	Description
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD1DeskewLeft0_cs0 Read DQ1 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON2
Address: Operational Base + offset (0x062C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD2DeskewLeft1_cs0 Read DQ2 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD2DeskewLeft0_cs0 Read DQ2 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON3
Address: Operational Base + offset (0x0638)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD3DeskewLeft1_cs0 Read DQ3 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD3DeskewLeft0_cs0 Read DQ3 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON4
Address: Operational Base + offset (0x0644)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD4DeskewLeft1_cs0 Read DQ4 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD4DeskewLeft0_cs0 Read DQ4 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON5
Address: Operational Base + offset (0x0650)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD5DeskewLeft1_cs0 Read DQ5 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD5DeskewLeft0_cs0 Read DQ5 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON6

Address: Operational Base + offset (0x065C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD6DeskewLeft1_cs0 Read DQ6 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD6DeskewLeft0_cs0 Read DQ6 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS0_CON7

Address: Operational Base + offset (0x0668)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD7DeskewLeft1_cs0 Read DQ7 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD7DeskewLeft0_cs0 Read DQ7 De-Skew Left Code for Data Slice0.

DDRPHY_FREQ_OFFSET_CON

Address: Operational Base + offset (0x0680)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	freq_offset Frequency compensation offset read out. It is calculated based on the current frequency and DLL lock value. It will be added to Write DQ/DM center code and Read DQS center code internally to maximize both setup and hold margin at the lower frequencies. freq_offset will be calculated as follows: freq_offset = {current lock value * (Training frequency - current frequency) / Training frequency}/4 (tFS)

DDRPHY_PRBS_CON0

Address: Operational Base + offset (0x0684)

Bit	Attr	Reset Value	Description
31:16	RW	0x0005	prbs_pattern The number of PRBS patterns to use at each DLL code during PRBS training. Do not use 0 and 1.
15:8	RW	0x00	Reserved0 Reserved
7	RW	0x0	prbs_write_cyc_en Write DQ/DM code cycle based control enabled. When enabled, DQ/DM cycle will be controlled if the offset exceeds cycle boundary. Enable this register when LF Write training is initiated with wrtrn_cyc_mode = 1.
6	RW	0x0	read_duty_en_APB read duty training enable register. Should use prbs_per_bit_mode = 1 and prbs_read_start = 1.

Bit	Attr	Reset Value	Description
5	RW	0x0	SET_USER_PATTERN_APB PRBS user pattern setting register. And this field only use Duty training or PRBS debugging. 1'b1: Fix the data pattern by default value of SEED0, SEED1, SEED2 and SEED3. 1'b0: PRBS pattern generation by SEED0, SEED1, SEED2 and SEED3.
4	RW	0x0	PRBS_MPC_MODE_APB PRBS training w/ scheduler through memory RFF/WFF 1'b1: LP5 : WFF/RFF path 1'b0: LP5 cell base training
3	RW	0x0	prbs_per_bit_mode Prbs per bit training mode, 1'b1: Prbs training per bit 1'b0: Prbs training per byte (default)
2	RW	0x0	prbs_write_start PRBS write training start.
1	RW	0x0	prbs_read_start PRBS read training start.
0	RO	0x0	prbs_done PRBS training response.

DDRPHY_PRBS_CON1

Address: Operational Base + offset (0x0688)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26	RW	0x1	prbs_dbi_en DBI function enable during PRBS training. If enabled, DM signal will work as data bus inversion.
25:24	RW	0x1	prbs_cs Rank information for PRBS training. (=Chip Select)
23:18	RW	0x10	prbs_wrlat DRAM write latency setting. (WL)
17:13	RW	0x10	prbs_twr2rd Write to read interval during PRBS training
12:9	RW	0x0	Reserved1 Reserved
8:5	RW	0x8	prbs_trddata_en_adj Trddata_en adjustment for PRBS training
4:0	RW	0x0c	prbs_tresync Resync duration setting for PRBS training

DDRPHY_PRBS_CON2

Address: Operational Base + offset (0x068C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:28	RO	0x0	prbs_rd_vwml_fail1 PRBS read training VWML search fail for byte1. prbs_rd_vwml_fail1[1] is for rank 0, and prbs_rd_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value('h0) while searching VWML.

Bit	Attr	Reset Value	Description
27:26	RO	0x0	prbs_rd_vwmr_fail1 PRBS read training VWMR search fail for byte1. prbs_rd_vwmr_fail1[1] is for rank 0, and prbs_rd_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.
25:16	RO	0x000	prbs_offsetr1 PRBS read training result for byte1. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr1[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr1[8:0] x tFS prbs_offsetr1[9] = 0: Read DQS delay from initial read training + prbs_offsetr1[8:0] x tFS
15:14	RO	0x0	Reserved1 Reserved
13:12	RO	0x0	prbs_rd_vwml_fail0 PRBS read training VWML search fail for byte0. prbs_rd_vwml_fail1[1] is for rank 0, and prbs_rd_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value('h0) while searching VWML.
11:10	RO	0x0	prbs_rd_vwmr_fail0 PRBS read training VWMR search fail for byte0. prbs_rd_vwmr_fail1[1] is for rank 0, and prbs_rd_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.
9:0	RO	0x000	prbs_offsetr0 PRBS read training result for byte0. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr0[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr0[8:0] x tFS prbs_offsetr0[9] = 0: Read DQS delay from initial read training + prbs_offsetr0[8:0] x tFS

DDRPHY_PRBS_CON3

Address: Operational Base + offset (0x0690)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved0 Reserved
30	RO	0x0	prbs_fail_byte1 Debug purpose. Information for prbs training failure at 1st iteration for BYTE1. 1'b1: Prbs training is failed at 1st iteration. 1'b0: Prbs training is not failed at 1st iteration.
29:28	RO	0x0	prbs_wr_vwml_fail1 PRBS write training VWML search fail for byte1. prbs_wr_vwml_fail1[1] is for rank 0, and prbs_wr_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value('h0) while searching VWML.

Bit	Attr	Reset Value	Description
27:26	RO	0x0	prbs_wr_vwmr_fail1 PRBS write training VWMR search fail for byte1. prbs_wr_vwmr_fail1[1] is for rank 0, and prbs_wr_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.
25:16	RO	0x000	prbs_offsetw1 PRBS write training result for byte1. It indicates how much center offset PRBS training has compensated from the initial write training result. prbs_offsetr1[9] = 1: (tFS: fine step delay) write DQ/DM delay from initial write training - prbs_offsetw1[8:0] x tFS prbs_offsetr1[9] = 0: write DQ/DM delay from initial write training + prbs_offsetw1[8:0] x tFS
15	RO	0x0	Reserved1 Reserved
14	RO	0x0	prbs_fail_byte0 Debug purpose. Information for prbs training failure at 1st iteration for BYTE0. 1'b1: Prbs training is failed at 1st iteration. 1'b0: Prbs training is not failed at 1st iteration.
13:12	RO	0x0	prbs_wr_vwml_fail0 PRBS write training VWML search fail for byte0. prbs_wr_vwml_fail1[1] is for rank 0, and prbs_wr_vwml_fail1[0] is for rank 1. If it is set high, it indicates vwml search has failed until DLL code has min value('h0) while searching VWML.
11:10	RO	0x0	prbs_wr_vwmr_fail0 PRBS write training VWMR search fail for byte0. prbs_wr_vwmr_fail1[1] is for rank 0, and prbs_wr_vwmr_fail1[0] is for rank 1. If it is set high, it indicates vwmr search has failed until DLL code has max value while searching VWMR.
9:0	RO	0x000	prbs_offsetw0 PRBS write training result for byte0. It indicates how much center offset PRBS training has compensated from the initial write training result. prbs_offsetw0[9] = 1: (tFS: fine step delay) write DQ/DM delay from initial write training - prbs_offsetw0[8:0] x tFS prbs_offsetw0[9] = 0: write DQ/DM delay from initial write training + prbs_offsetw0[8:0] x tFS

DDRPHY_PRBS_CON4

Address: Operational Base + offset (0x0694)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	sw_prbs_offsetr1 PRBS read training result for byte1. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr1[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr1[8:0] x tFS prbs_offsetr1[9] = 0: Read DQS delay from initial read training + prbs_offsetr1[8:0] x tFS
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	sw_prbs_offsetr0 PRBS read training result for byte0. It indicates how much center offset PRBS training has compensated from the initial read training result. prbs_offsetr0[9] = 1: (tFS: fine step delay) Read DQS delay from initial read training - prbs_offsetr0[8:0] x tFS prbs_offsetr0[9] = 0: Read DQS delay from initial read training + prbs_offsetr0[8:0] x tFS

DDRPHY_PRBS_CON5
Address: Operational Base + offset (0x0698)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	sw_prbs_offsetw1 SW PRBS write training result for byte1.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	sw_prbs_offsetw0 SW PRBS write training result for byte0.

DDRPHY_PRBS_CON6
Address: Operational Base + offset (0x069C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left1 Left margin found during PRBS training for byte1. This field will be updated after each PRBS training.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left0 Left margin found during PRBS training for byte0. This field will be updated after each PRBS training.

DDRPHY_PRBS_CON7
Address: Operational Base + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RO	0x000	prbs_offset_right1 right margin found during PRBS training for byte1. This field will be updated after each PRBS training.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right0 right margin found during PRBS training for byte0. This field will be updated after each PRBS training.

DDRPHY_PRBS_CON8

Address: Operational Base + offset (0x06A4)

Bit	Attr	Reset Value	Description
31	RW	0x1	prbs_dram_act_enable DRAM activate-precharge enable. If enabled, DRAM activate/precharge will be asserted in between MPC-WR FIFO and MPC-RD FIFO commands during PRBS training. Bank will be changed continuously (0~7) for each Activate or Precharge.
30:21	RW	0x000	Reserved0 Reserved
20:16	RW	0x0b	prbs_tRRD Interval between Active commands to different banks during PRBS training with dram_act_enable = 1. tRRD should be set using the following: tRRD = RU((10ns/1tCK)/2) in DFI clock cycle. (1tCK: DRAM clock period)
15:0	RW	0x0000	prbs_row_addr Row address to be used for Activate command during PRBS training when dram_act_enable = 1.

DDRPHY_PRBS_CON9

Address: Operational Base + offset (0x06A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00ff00ff	SEED0 PRBS SEED0

DDRPHY_PRBS_CON10

Address: Operational Base + offset (0x06AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x0f0f0f0f	SEED1 PRBS SEED1

DDRPHY_PRBS_CON11

Address: Operational Base + offset (0x06B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x5a5a5a5a	SEED2 PRBS SEED2

DDRPHY_PRBS_CON12

Address: Operational Base + offset (0x06B4)

Bit	Attr	Reset Value	Description
31:0	RW	0xff00ff00	SEED3 PRBS SEED3

DDRPHY_PRBS_CON13

Address: Operational Base + offset (0x06B8)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved
7:6	RW	0x1	prbs_wrdata_dm_p0_APB PRBS Data Mask pattern for phase0 It should be set to PRBS_MPC_MODE_APB = 1.
5:4	RW	0x1	prbs_wrdata_dm_p1_APB PRBS Data Mask pattern for phase1 It should be set to PRBS_MPC_MODE_APB = 1.
3:2	RW	0x1	prbs_wrdata_dm_p2_APB PRBS Data Mask pattern for phase2 It should be set to PRBS_MPC_MODE_APB = 1.
1:0	RW	0x1	prbs_wrdata_dm_p3_APB PRBS Data Mask pattern for phase3 It should be set to PRBS_MPC_MODE_APB = 1.

DDRPHY_DUTY_CAL0
Address: Operational Base + offset (0x06BC)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved
24:16	RW	0x000	per_burst_duty_mask_en_APB This field mask function each burst data for duty training. [24]: BL16 BL15 DATA MASK [23]: BL14 BL13 DATA MASK [22]: BL12 BL11 DATA MASK [21]: BL10 BL9 DATA MASK [20]: BL8 BL7 DATA MASK [19]: BL6 BL5 DATA MASK [18]: BL4 BL3 DATA MASK [17]: BL2 BL1 DATA MASK 1'b1: DATA MASK 1'b0: DATA UNMASK
15:9	RW	0x00	Reserved0 Reserved
8:0	RW	0x000	per_bit_duty_mask_en_APB This field mask function each bit for duty training. [8]: DM1/DM0 [7]: DQ15/DQ7 [6]: DQ14/DQ6 [5]: DQ13/DQ5 [4]: DQ12/DQ4 [3]: DQ11/DQ3 [2]: DQ10/DQ2 [1]: DQ9/DQ1 [0]: DQ8/DQ0 1'b1: DATA MASK 1'b0: DATA UNMASK

DDRPHY_MON_CON0
Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	dvfs_modei Current dvfs mode status
29:28	RO	0x0	dvfs_modei_prev Previous dvfs mode status

Bit	Attr	Reset Value	Description
27	RW	0x0	debug_mode_en Debug mode enable
26	RO	0x0	dfi_init_start_status dfi_init_start status
25	RO	0x0	dfi_init_complete_status dfi_init_complete status
24:22	RO	0x0	cs_phydvfs Current PHY DVFS state monitor
21:20	RO	0x0	cs_phyupd Current PHY update state monitor
19	RW	0x0	write_drive_en Write data drive enable. If write_drive_en = 1, PHY will drive write data on DQS, DQ and DBI. The values driven on DQ/DBI is determined by write training pattern defined in CAL_WR_PATTERN_CON0~CAL_WR_PATTERN_CON19. Enable this field only for write data eye measurement. Note that write command will not be driven. During the write operation, write DQ/DBI DLL code will be chosen between RANK0 and RANK1 based on cs_default.
18	RO	0x0	ctrl_phy_cg_en_status Current ctrl_phy_cg_en status.
17	RO	0x1	dfi_dram_clk_disable_status Current dfi_dram_clk_disable status.
16	RW	0x0	ReadWriteAccess_mode Enable it before monitoring gate_rise_monitor_ds0, gate_fall_monitor_ds0, gatem_rise_monitor_ds0, gatem_fall_monitor_ds0 registers. It will initialize them to the default values('h0).
15	RW	0x0	mdll_monitor_en Master DLL monitor enable. 1'b1: LOCK_VAL0~LOCK_VAL2 registers will be updated. 1'b0: LOCK_VAL0~LOCK_VAL2 registers will not be updated.
14:11	RW	0x0	gate_debug_en This is optional register for gate training. Gate_debug_en[3]: Gate margin control by shiftc register. Gate_debug_en[2]: Skip gate training iteration fine step for reduce black out time. Gate_debug_en[1]: Skip gate training iteration coarse step for reduce black out time. Gate_debug_en[0]: Cycle update control for gate margin test.
10	RO	0x0	Reserved2 Reserved
9	RO	0x0	rddata_en_phase_err_ds1 dfi_rddata_en phase check flag for DS1. 1'b0: no error 1'b1: dfi_rddata_en_p0~p3 are not enabled at the same time.
8	RO	0x0	rddata_en_phase_err_ds0 dfi_rddata_en phase check flag for DS0. 1'b0: no error 1'b1: dfi_rddata_en_p0~p3 are not enabled at the same time.
7:6	RO	0x0	Reserved3 Reserved

Bit	Attr	Reset Value	Description
5	RO	0x0	read_dur_err_ds1 Read data duration error flag for DS1. If this field is set to 'h1, it indicates that rddata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.
4	RO	0x0	read_dur_err_ds0 Read data duration error flag for DS1. If this field is set to 'h1, it indicates that rddata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.
3:2	RO	0x0	Reserved4 Reserved
1	RO	0x0	write_dur_err_ds1 Write data duration error flag for DS1. If this field is set to 'h1, it indicates that wrdata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.
0	RO	0x0	write_dur_err_ds0 Write data duration error flag for DS1. If this field is set to 'h1, it indicates that wrdata duration is not a multiple of 16 at DLL update step. This field is valid when debug_mode_en is high.

DDRPHY_MON_CON1
Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved0 Reserved
23:20	RO	0x0	wrdata_dur_ds1 dfi_wrdata_en duration counter for DS1. This field is valid when debug_mode_en is high.
19:16	RO	0x0	wrdata_dur_ds0 dfi_wrdata_en duration counter for DS0. This field is valid when debug_mode_en is high.
15:8	RO	0x00	Reserved1 Reserved
7:4	RO	0x0	rddata_dur_ds1 dfi_rddata_en duration counter for DS1. This field is valid when debug_mode_en is high.
3:0	RO	0x0	rddata_dur_ds0 dfi_rddata_en duration counter for DS0. This field is valid when debug_mode_en is high.

DDRPHY_MON_CON2
Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rddata_w0_status dfi_rddata_w0 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_w0 for the previous read operation. dfi_rddata_w0_status mapping is as follows: dfi_rddata_w0_status[31:16] = {dfi_rddata_w0[31:24], dfi_rddata_w0[15:8]} dfi_rddata_w0_status[15:0] = {dfi_rddata_w0[23:16], dfi_rddata_w0[7:0]}

DDRPHY_MON_CON3
Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rddata_w1_status dfi_rddata_w1 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_w1 for the previous read operation. dfi_rddata_w1_status mapping is as follows: dfi_rddata_w1_status[31:16] = {dfi_rddata_w1[31:24], dfi_rddata_w1[15:8]} dfi_rddata_w1_status[15:0] = {dfi_rddata_w1[23:16], dfi_rddata_w1[7:0]}

DDRPHY_MON_CON4
Address: Operational Base + offset (0x0710)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved0 Reserved
27:24	RO	0x0	dfi_rddata_dmi_w0_status dfi_rddata_dmi_w0[3:0] status. This field is valid when debug_mode_en is high. dfi_rddata_dmi_w0 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_dmi_w0 for the previous read operation. dfi_rddata_dmi_w0_status mapping is as follows: dfi_rddata_dmi_w0_status[3:2] = {dfi_rddata_dmi_w0[3], dfi_rddata_dmi_w0[1]} dfi_rddata_dmi_w0_status[1:0] = {dfi_rddata_dmi_w0[2], dfi_rddata_dmi_w0[0]}
23:20	RO	0x0	Reserved1 Reserved
19:16	RO	0x0	dfi_rddata_dmi_w1_status dfi_rddata_dmi_w1[3:0] status. This field is valid when debug_mode_en is high. dfi_rddata_dmi_w1 status. This field is valid when debug_mode_en is high. If debug_mode_en is high, this register shows the last valid dfi_rddata_dmi_w1 for the previous read operation. dfi_rddata_dmi_w1_status mapping is as follows: dfi_rddata_dmi_w1_status[3:2] = {dfi_rddata_dmi_w1[3], dfi_rddata_dmi_w1[1]} dfi_rddata_dmi_w1_status[1:0] = {dfi_rddata_dmi_w1[2], dfi_rddata_dmi_w1[0]}
15:0	RO	0x0000	Reserved2 Reserved

DDRPHY_MON_CON5
Address: Operational Base + offset (0x0714)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved0 Reserved
21	RO	0x0	wrtrn_fsm_idle_rank1_ds1 Idle stat flag of write training for rank1 of data slice1.
20	RO	0x0	wrtrn_fsm_first_rank1_ds1 First state flag of write training for rank1 of data slice1.
19	RO	0x0	wrtrn_fsm_codeinit_rank1_ds1 Code initialization state flag of write training for rank1 of data slice1.

Bit	Attr	Reset Value	Description
18	RO	0x0	wrtrn_fsm_second_rank1_ds1 Second state flag of write training for rank1 of data slice1.
17	RO	0x0	wrtrn_fsm_periodic_rank1_ds1 Periodic state flag of write training for rank1 of data slice1.
16	RO	0x0	wrtrn_fsm_resp_rank1_ds1 Responose state flag of write training for rank1 of data slice1.
15:12	RO	0x0	write_fsm_status_rank1_ds1 FSM monitoring signal for rank1 of data slice1. It shows cs_wrtrn FSM status in write_training.
11:10	RO	0x0	Reserved1 Reserved
9	RO	0x0	wrtrn_fsm_idle_rank1_ds0 Idle stat flag of write training for rank1 of data slice0.
8	RO	0x0	wrtrn_fsm_first_rank1_ds0 First state flag of write training for rank1 of data slice0.
7	RO	0x0	wrtrn_fsm_codeinit_rank1_ds0 Code initialization state flag of write training for rank1 of data slice0.
6	RO	0x0	wrtrn_fsm_second_rank1_ds0 Second state flag of write training for rank1 of data slice0.
5	RO	0x0	wrtrn_fsm_periodic_rank1_ds0 Periodic state flag of write training for rank1 of data slice0.
4	RO	0x0	wrtrn_fsm_resp_rank1_ds0 Responose state flag of write training for rank1 of data slice0.
3:0	RO	0x0	write_fsm_status_rank1_ds0 FSM monitoring signal for rank1 of data slice0. It shows cs_wrtrn FSM status in write_training.

DDRPHY_MON_CON6

Address: Operational Base + offset (0x0718)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved0 Reserved
21	RO	0x0	wrtrn_fsm_idle_rank0_ds1 Idle stat flag of write training for rank0 of data slice1.
20	RO	0x0	wrtrn_fsm_first_rank0_ds1 First state flag of write training for rank0 of data slice1.
19	RO	0x0	wrtrn_fsm_codeinit_rank0_ds1 Code initialization state flag of write training for rank0 of data slice1.
18	RO	0x0	wrtrn_fsm_second_rank0_ds1 Second state flag of write training for rank0 of data slice1.
17	RO	0x0	wrtrn_fsm_periodic_rank0_ds1 Periodic state flag of write training for rank0 of data slice1.
16	RO	0x0	wrtrn_fsm_resp_rank0_ds1 Responose state flag of write training for rank0 of data slice1.
15:12	RO	0x0	write_fsm_status_rank0_ds1 FSM monitoring signal for rank0 of data slice1. It shows cs_wrtrn FSM status in write_training.
11:10	RO	0x0	Reserved1 Reserved
9	RO	0x0	wrtrn_fsm_idle_rank0_ds0 Idle stat flag of write training for rank0 of data slice0.

Bit	Attr	Reset Value	Description
8	RO	0x0	wrtrn_fsm_first_rank0_ds0 First state flag of write training for rank0 of data slice0.
7	RO	0x0	wrtrn_fsm_codeinit_rank0_ds0 Code initialization state flag of write training for rank0 of data slice0.
6	RO	0x0	wrtrn_fsm_second_rank0_ds0 Second state flag of write training for rank0 of data slice0.
5	RO	0x0	wrtrn_fsm_periodic_rank0_ds0 Periodic state flag of write training for rank0 of data slice0.
4	RO	0x0	wrtrn_fsm_resp_rank0_ds0 Responose state flag of write training for rank0 of data slice0.
3:0	RO	0x0	write_fsm_status_rank0_ds0 FSM monitoring signal for rank0 of data slice0. It shows cs_wrtrn FSM status in write_training.

DDRPHY_MON_CON7

Address: Operational Base + offset (0x071C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved0 Reserved
21	RO	0x0	rdlvl_fsm_idle_ds1 Idle stat flag of read training for data slice1.
20	RO	0x0	rdlvl_fsm_fisrt_ds1 First state flag of read training for data slice1.
19	RO	0x0	rdlvl_fsm_codeinit_ds1 Code initialization state flag of read training for data slice1.
18	RO	0x0	rdtrn_fsm_second_ds1 Second state flag of read training for data slice1.
17	RO	0x0	rdlvl_fsm_periodic_ds1 Periodic state flag of read training for data slice1.
16	RO	0x0	rdlvl_fsm_resp_ds1 Responose state flag of read training for data slice1.
15	RO	0x0	Reserved1 Reserved
14:12	RO	0x0	rdlvl_fsm_status_ds1 FSM monitoring signal for data slice1. It shows cs_rdlvl FSM status in read_training.
11:10	RO	0x0	Reserved2 Reserved
9	RO	0x0	rdlvl_fsm_idle_ds0 Idle stat flag of read training for data slice0.
8	RO	0x0	rdlvl_fsm_fisrt_ds0 First state flag of read training for data slice0.
7	RO	0x0	rdlvl_fsm_codeinit_ds0 Code initialization state flag of read training for data slice0.
6	RO	0x0	rdlvl_fsm_second_ds0 Second state flag of read training for data slice0.
5	RO	0x0	rdlvl_fsm_periodic_ds0 Periodic state flag of read training for data slice0.
4	RO	0x0	rdlvl_fsm_resp_ds0 Responose state flag of read training for data slice0.
3	RO	0x0	Reserved3 Reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x0	rdlvl_fsm_status_ds0 FSM monitoring signal for data slice0. It shows cs_rdlvl FSM status in read_training.

DDRPHY_WR_TRAIN_MON0

Address: Operational Base + offset (0x0720)

Bit	Attr	Reset Value	Description
31	RO	0x0	dvfs_wr_start_status1_cs0 DVFS write training start point status for Byte1 at rank0. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
30	RO	0x0	dvfs_wr_start_status0_cs0 DVFS write training start point status for Byte0 at rank0. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
29	RO	0x0	dvfs_wr_start_status1_cs1 DVFS write training start point status for Byte1 at rank1. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
28	RO	0x0	dvfs_wr_start_status0_cs1 DVFS write training start point status for Byte0 at rank1. If this field is high, it indicates that the first access with start point DLL code passed during DVFS write training.
27	RO	0x0	dvfs_wr_max_status1_cs0 DVFS write training max code status for Byte1 at rank0. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
26	RO	0x0	dvfs_wr_max_status0_cs0 DVFS write training max code status for Byte0 at rank0. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
25	RO	0x0	dvfs_wr_max_status1_cs1 DVFS write training max code status for Byte1 at rank1. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
24	RO	0x0	dvfs_wr_max_status0_cs1 DVFS write training max code status for Byte0 at rank1. If this field is high, it indicates that DQ/DM bit DLL code reached max code without access pass during DVFS write training.
23:0	RO	0x000000	Reserved0 Reserved

DDRPHY_LOCK_VAL0

Address: Operational Base + offset (0x0728)

Bit	Attr	Reset Value	Description
31	RO	0x0	dvfs0_locked_release ctrl_locked release indicator for DVFS mode 0. It will be detected locked release after finished relock.
30	RO	0x0	dvfs0_harmonic_err Harmonic lock error indicator for DVFS mode 0. Valid only when the core voltage is not changed.
29:20	RO	0x001	dvfs0_relock_value DLL Re-lock value for DVFS mode 0. If mdll_monitor_en is high, it will be updated to ctrl_lock_value after DLL relocking that occurs during the frequency change with DVFS mode 0.

Bit	Attr	Reset Value	Description
19:10	RO	0x3ff	dvfs0_lock_value_min Minimum lock value for DVFS mode 0. If mdll_monitor_en is high, it shows the minimum ctrl_lock_value during the normal operation with DVFS mode 0, except for the frequency change duration.
9:0	RO	0x001	dvfs0_lock_value_max Maximum lock value for DVFS mode 0. If mdll_monitor_en is high, it shows the maximum ctrl_lock_value during the normal operation with DVFS mode 0, except for the frequency change duration.

DDRPHY_LOCK_VAL1

Address: Operational Base + offset (0x072C)

Bit	Attr	Reset Value	Description
31	RO	0x0	dvfs1_locked_release ctrl_locked release indicator for DVFS mode 1. It will be detected locked release after finished relock.
30	RO	0x0	dvfs1_harmonic_err Harmonic lock error indicator for DVFS mode 1. Valid only when the core voltage is not changed.
29:20	RO	0x001	dvfs1_relock_value DLL Re-lock value for DVFS mode 1. If mdll_monitor_en is high, It will be updated to ctrl_lock_value after DLL relocking that occurs during the frequency change with DVFS mode 1.
19:10	RO	0x3ff	dvfs1_lock_value_min Minimum lock value for DVFS mode 1. If mdll_monitor_en is high, it shows the minimum ctrl_lock_value during the normal operation with DVFS mode 1, except for the frequency change duration.
9:0	RO	0x001	dvfs1_lock_value_max Maximum lock value for DVFS mode 1. If mdll_monitor_en is high, it shows the maximum ctrl_lock_value during the normal operation with DVFS mode 1, except for the frequency change duration.

DDRPHY_LOCK_VAL2

Address: Operational Base + offset (0x0730)

Bit	Attr	Reset Value	Description
31	RO	0x0	locked_release ctrl_locked release indicator for normal mode 1. It will be detected locked release after finished relock.
30	RO	0x0	harmonic_err Harmonic lock error indicator for normal mode. Valid only when the core voltage is not changed.
29:20	RO	0x001	relock_value DLL Re-lock value for normal mode. If mdll_monitor_en is high, it will be updated to ctrl_lock_value after DLL relocking that occurs during the frequency change with normal mode (dvfs_mode = 'h0).
19:10	RO	0x3ff	lock_value_min Minimum lock value for normal mode. If mdll_monitor_en is high, it shows the minimum ctrl_lock_value during the normal operation with normal mode (dvfs_mode = 'h0), except for the frequency change duration.

Bit	Attr	Reset Value	Description
9:0	RO	0x001	lock_value_max Maximum lock value for normal mode. If mdll_monitor_en is high, it shows the maximum ctrl_lock_value during the normal operation with normal mode (dvfs_mode = 'h0), except for the frequency change duration.

DDRPHY_WR_CHECK_CON0

Address: Operational Base + offset (0x0750)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved0 FiFO write pointer in data slice0. This field is valid when debug_mode_en is high
27:24	RO	0x0	wptr_ds0 FiFO write pointer in data slice0. This field is valid when debug_mode_en is high.
23:20	RO	0x0	Reserved1 FiFO read pointer in data slice0. This field is valid when debug_mode_en is high.
19:16	RO	0x0	rptr_ds0 FiFO read pointer in data slice0. This field is valid when debug_mode_en is high.
15:9	RO	0x00	Reserved2 Reserved
8	RO	0x0	fifo_err_ds0 FiFO error status in data slice0. This field is valid when debug_mode_en is high. It will be updated when dfi_ctrlupd_ack rises, dfi_phyupd_ack rises or dfi_init_start rises. It will be asserted high if wptr_h_ds0 != rptr_h_ds0 or wptr_l_ds0 != rptr_l_ds0. If it is asserted high, dfi_init_complete will be set to low.
7:6	RO	0x0	gate_rise_monitor_ds0 GATE detector at dqs rising edge in data slice0. debug_mode_en should be set to high to make this register valid.
5:4	RO	0x0	gate_fall_monitor_ds0 GATE detector at dqs falling edge in data slice0. debug_mode_en should be set to high to make this register valid.
3:0	RO	0x0	Reserved3 Reserved

DDRPHY_WR_CHECK_CON1

Address: Operational Base + offset (0x0754)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved0 FiFO write pointer in data slice1. This field is valid when debug_mode_en is high
27:24	RO	0x0	wptr_ds1 FiFO write pointer in data slice1. This field is valid when debug_mode_en is high.
23:20	RO	0x0	Reserved1 FiFO read pointer in data slice1. This field is valid when debug_mode_en is high
19:16	RO	0x0	rptr_ds1 FiFO read pointer in data slice1. This field is valid when debug_mode_en is high.

Bit	Attr	Reset Value	Description
15:9	RO	0x00	Reserved2 Reserved
8	RO	0x0	fifo_err_ds1 FiFO error status in data slice1. This field is valid when debug_mode_en is high. It will be updated when dfi_ctrlupd_ack rises, dfi_phyupd_ack rises or dfi_init_start rises. It will be asserted high if wptr_h_ds1 != rptr_h_ds1 or wptr_l_ds1 != rptr_l_ds1. If it is asserted high, dfi_init_complete will be set to low.
7:6	RO	0x0	gate_rise_monitor_ds1 GATE detector at dqs rising edge in data slice1. debug_mode_en should be set to high to make this register valid.
5:4	RO	0x0	gate_fall_monitor_ds1 GATE detector at dqs falling edge in data slice1. debug_mode_en should be set to high to make this register valid.
3:0	RO	0x0	Reserved3 Reserved

DDRPHY_WR_CHECK_CON2

Address: Operational Base + offset (0x0760)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Read_command_counter_ds1 Read command counter in data slice1. This field is valid when debug_mode_en is high.
23:16	RO	0x00	Read_command_counter_ds0 Read command counter in data slice0. This field is valid when debug_mode_en is high.
15:0	RO	0x0000	Reserved0 Reserved

DDRPHY_RD_DQS_VWML_CS1_CON0

Address: Operational Base + offset (0x0764)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved0 Reserved
24:16	RO	0x000	RDDQSVWML1_cs1 Read DQS Left Code for Data Slice1.
15:9	RO	0x00	Reserved1 Reserved
8:0	RO	0x000	RDDQSVWML0_cs1 Read DQS Left Code for Data Slice0.

DDRPHY_RD_DQS_VWMC_CS1_CON0

Address: Operational Base + offset (0x0768)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved0 Reserved
24:16	RO	0x000	RDDQSVWMC1_cs1 Read DQS Center Code for Data Slice1.
15:9	RO	0x00	Reserved1 Reserved
8:0	RO	0x000	RDDQSVWMC0_cs1 Read DQS Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON_DM

Address: Operational Base + offset (0x076C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RDDMDeskewC1_cs1 Read DMI De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RDDMDeskewC0_cs1 Read DMI De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON0
Address: Operational Base + offset (0x0770)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD0DeskewC1_cs1 Read DQ0 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD0DeskewC0_cs1 Read DQ0 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON1
Address: Operational Base + offset (0x0774)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD1DeskewC1_cs1 Read DQ1 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD1DeskewC0_cs1 Read DQ1 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON2
Address: Operational Base + offset (0x0778)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD2DeskewC1_cs1 Read DQ2 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD2DeskewC0_cs1 Read DQ2 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON3
Address: Operational Base + offset (0x077C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD3DeskewC1_cs1 Read DQ3 De-Skew Center Code for Data Slice1.

Bit	Attr	Reset Value	Description
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD3DeskewC0_cs1 Read DQ3 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON4
Address: Operational Base + offset (0x0780)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD4DeskewC1_cs1 Read DQ4 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD4DeskewC0_cs1 Read DQ4 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON5
Address: Operational Base + offset (0x0784)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD5DeskewC1_cs1 Read DQ5 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD5DeskewC0_cs1 Read DQ5 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON6
Address: Operational Base + offset (0x0788)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD6DeskewC1_cs1 Read DQ6 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD6DeskewC0_cs1 Read DQ6 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_CENTER_CS1_CON7
Address: Operational Base + offset (0x078C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD7DeskewC1_cs1 Read DQ7 De-Skew Center Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD7DeskewC0_cs1 Read DQ7 De-Skew Center Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON_DM

Address: Operational Base + offset (0x0790)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RDDMDeskewLeft1_cs1 Read DMI De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RDDMDeskewLeft0_cs1 Read DMI De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON0

Address: Operational Base + offset (0x0794)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD0DeskewLeft1_cs1 Read DQ0 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD0DeskewLeft0_cs1 Read DQ0 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON1

Address: Operational Base + offset (0x0798)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD1DeskewLeft1_cs1 Read DQ1 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD1DeskewLeft0_cs1 Read DQ1 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON2

Address: Operational Base + offset (0x079C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD2DeskewLeft1_cs1 Read DQ2 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD2DeskewLeft0_cs1 Read DQ2 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON3

Address: Operational Base + offset (0x07A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD3DeskewLeft1_cs1 Read DQ3 De-Skew Left Code for Data Slice1.

Bit	Attr	Reset Value	Description
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD3DeskewLeft0_cs1 Read DQ3 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON4

Address: Operational Base + offset (0x07A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD4DeskewLeft1_cs1 Read DQ4 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD4DeskewLeft0_cs1 Read DQ4 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON5

Address: Operational Base + offset (0x07A8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD5DeskewLeft1_cs1 Read DQ5 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD5DeskewLeft0_cs1 Read DQ5 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON6

Address: Operational Base + offset (0x07AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD6DeskewLeft1_cs1 Read DQ6 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD6DeskewLeft0_cs1 Read DQ6 De-Skew Left Code for Data Slice0.

DDRPHY_RD_DESKEW_LEFT_CS1_CON7

Address: Operational Base + offset (0x07B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	RD7DeskewLeft1_cs1 Read DQ7 De-Skew Left Code for Data Slice1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	RD7DeskewLeft0_cs1 Read DQ7 De-Skew Left Code for Data Slice0.

DDRPHY_SW_RD_DQS_VWML_CS0_CON0

Address: Operational Base + offset (0x07C0)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved
24:16	RW	0x000	SW_RDDQSVWML1_cs0 SW Read DQS Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:9	RW	0x00	Reserved1 Reserved
8:0	RW	0x000	SW_RDDQSVWML0_cs0 SW Read DQS Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DQS_VWMC_CS0_CON0

Address: Operational Base + offset (0x07C4)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved
24:16	RW	0x000	SW_RDDQSVWMC1_cs0 SW Read DQS Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:9	RW	0x00	Reserved1 Reserved
8:0	RW	0x000	SW_RDDQSVWMC0_cs0 SW Read DQS Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON_DM

Address: Operational Base + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RDDMDeskewC1_cs0 SW Read DMI De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RDDMDeskewC0_cs0 SW Read DMI De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON0

Address: Operational Base + offset (0x07CC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD0DeskewC1_cs0 SW Read DQ0 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD0DeskewC0_cs0 SW Read DQ0 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON1

Address: Operational Base + offset (0x07D0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD1DeskewC1_cs0 SW Read DQ1 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD1DeskewC0_cs0 SW Read DQ1 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON2

Address: Operational Base + offset (0x07D4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD2DeskewC1_cs0 SW Read DQ2 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD2DeskewC0_cs0 SW Read DQ2 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON3

Address: Operational Base + offset (0x07D8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD3DeskewC1_cs0 SW Read DQ3 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD3DeskewC0_cs0 SW Read DQ3 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON4

Address: Operational Base + offset (0x07DC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD4DeskewC1_cs0 SW Read DQ4 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD4DeskewC0_cs0 SW Read DQ4 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON5

Address: Operational Base + offset (0x07E0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD5DeskewC1_cs0 SW Read DQ5 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD5DeskewC0_cs0 SW Read DQ5 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON6

Address: Operational Base + offset (0x07E4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD6DeskewC1_cs0 SW Read DQ6 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD6DeskewC0_cs0 SW Read DQ6 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS0_CON7
Address: Operational Base + offset (0x07E8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD7DeskewC1_cs0 SW Read DQ7 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD7DeskewC0_cs0 SW Read DQ7 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON_DM
Address: Operational Base + offset (0x07F0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RDDMDeskewLeft1_cs0 SW Read DMI De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RDDMDeskewLeft0_cs0 SW Read DMI De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON0
Address: Operational Base + offset (0x07F4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD0DeskewLeft1_cs0 SW Read DQ0 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD0DeskewLeft0_cs0 SW Read DQ0 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON1
Address: Operational Base + offset (0x07F8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD1DeskewLeft1_cs0 SW Read DQ1 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD1DeskewLeft0_cs0 SW Read DQ1 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON2
Address: Operational Base + offset (0x07FC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD2DeskewLeft1_cs0 SW Read DQ2 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD2DeskewLeft0_cs0 SW Read DQ2 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON3
Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD3DeskewLeft1_cs0 SW Read DQ3 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD3DeskewLeft0_cs0 SW Read DQ3 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON4
Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD4DeskewLeft1_cs0 SW Read DQ4 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD4DeskewLeft0_cs0 SW Read DQ4 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON5
Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD5DeskewLeft1_cs0 SW Read DQ5 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD5DeskewLeft0_cs0 SW Read DQ5 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON6
Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD6DeskewLeft1_cs0 SW Read DQ6 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD6DeskewLeft0_cs0 SW Read DQ6 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS0_CON7
Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD7DeskewLeft1_cs0 SW Read DQ7 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD7DeskewLeft0_cs0 SW Read DQ7 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DQS_VWML_CS1_CON0
Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved
24:16	RW	0x000	SW_RDDQSVWML1_cs1 SW Read DQS Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:9	RW	0x00	Reserved1 Reserved
8:0	RW	0x000	SW_RDDQSVWML0_cs1 SW Read DQS Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DQS_VWMC_CS1_CON0
Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
24:16	RW	0x000	SW_RDDQSVWMC1_cs1 SW Read DQS Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:9	RW	0x00	Reserved1 Reserved
8:0	RW	0x000	SW_RDDQSVWMC0_cs1 SW Read DQS Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON_DM

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RDDMDeskewC1_cs1 SW Read DMI De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RDDMDeskewC0_cs1 SW Read DMI De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON0

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD0DeskewC1_cs1 SW Read DQ0 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD0DeskewC0_cs1 SW Read DQ0 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON1

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD1DeskewC1_cs1 SW Read DQ1 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD1DeskewC0_cs1 SW Read DQ1 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON2
Address: Operational Base + offset (0x082C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD2DeskewC1_cs1 SW Read DQ2 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD2DeskewC0_cs1 SW Read DQ2 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON3
Address: Operational Base + offset (0x0830)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD3DeskewC1_cs1 SW Read DQ3 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD3DeskewC0_cs1 SW Read DQ3 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON4
Address: Operational Base + offset (0x0834)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD4DeskewC1_cs1 SW Read DQ4 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD4DeskewC0_cs1 SW Read DQ4 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON5

Address: Operational Base + offset (0x0838)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD5DeskewC1_cs1 SW Read DQ5 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD5DeskewC0_cs1 SW Read DQ5 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON6

Address: Operational Base + offset (0x083C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD6DeskewC1_cs1 SW Read DQ6 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD6DeskewC0_cs1 SW Read DQ6 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_CENTER_CS1_CON7

Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD7DeskewC1_cs1 SW Read DQ7 De-Skew Center Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD7DeskewC0_cs1 SW Read DQ7 De-Skew Center Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON_DM
Address: Operational Base + offset (0x0850)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RDDMDeskewLeft1_cs1 SW Read DMI De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RDDMDeskewLeft0_cs1 SW Read DMI De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON0
Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD0DeskewLeft1_cs1 SW Read DQ0 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD0DeskewLeft0_cs1 SW Read DQ0 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON1
Address: Operational Base + offset (0x0858)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD1DeskewLeft1_cs1 SW Read DQ1 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD1DeskewLeft0_cs1 SW Read DQ1 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON2

Address: Operational Base + offset (0x085C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD2DeskewLeft1_cs1 SW Read DQ2 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD2DeskewLeft0_cs1 SW Read DQ2 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON3

Address: Operational Base + offset (0x0860)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD3DeskewLeft1_cs1 SW Read DQ3 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD3DeskewLeft0_cs1 SW Read DQ3 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON4

Address: Operational Base + offset (0x0864)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD4DeskewLeft1_cs1 SW Read DQ4 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD4DeskewLeft0_cs1 SW Read DQ4 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON5
Address: Operational Base + offset (0x0868)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD5DeskewLeft1_cs1 SW Read DQ5 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD5DeskewLeft0_cs1 SW Read DQ5 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON6
Address: Operational Base + offset (0x086C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_RD6DeskewLeft1_cs1 SW Read DQ6 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD6DeskewLeft0_cs1 SW Read DQ6 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_RD_DESKEW_LEFT_CS1_CON7
Address: Operational Base + offset (0x0870)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_RD7DeskewLeft1_cs1 SW Read DQ7 De-Skew Left Code for Data Slice1. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_RD7DeskewLeft0_cs1 SW Read DQ7 De-Skew Left Code for Data Slice0. Write to this register (1) to restore read training result with rd_sw_mode=1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON0

Address: Operational Base + offset (0x0880)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR0DeskewC1_cs0 SW Write DQ0 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR0DeskewC0_cs0 SW Write DQ0 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON1

Address: Operational Base + offset (0x0884)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR1DeskewC1_cs0 SW Write DQ1 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR1DeskewC0_cs0 SW Write DQ1 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON2

Address: Operational Base + offset (0x0888)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR2DeskewC1_cs0 SW Write DQ2 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR2DeskewC0_cs0 SW Write DQ2 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON3
Address: Operational Base + offset (0x088C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR3DeskewC1_cs0 SW Write DQ3 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR3DeskewC0_cs0 SW Write DQ3 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON4
Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR4DeskewC1_cs0 SW Write DQ4 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR4DeskewC0_cs0 SW Write DQ4 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON5
Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR5DeskewC1_cs0 SW Write DQ5 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR5DeskewC0_cs0 SW Write DQ5 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON6
Address: Operational Base + offset (0x0898)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR6DeskewC1_cs0 SW Write DQ6 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR6DeskewC0_cs0 SW Write DQ6 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS0_CON7
Address: Operational Base + offset (0x089C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR7DeskewC1_cs0 SW Write DQ7 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR7DeskewC0_cs0 SW Write DQ7 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_DM_DESKEWC_CS0_CON0
Address: Operational Base + offset (0x08A0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WRDMDeskewC1_cs0 SW Write DM De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRDMDeskewC0_cs0 SW Write DM De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_ECC_DESKEWC_CS0_CON0
Address: Operational Base + offset (0x08A4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WRECCDeskewC1_cs0 SW Write ECC De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRECCDeskewC0_cs0 SW Write ECC De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON0
Address: Operational Base + offset (0x08B0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR0DeskewL1_cs0 SW Write DQ0 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR0DeskewL0_cs0 SW Write DQ0 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON1
Address: Operational Base + offset (0x08B4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR1DeskewL1_cs0 SW Write DQ1 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR1DeskewL0_cs0 SW Write DQ1 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON2
Address: Operational Base + offset (0x08B8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR2DeskewL1_cs0 SW Write DQ2 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR2DeskewL0_cs0 SW Write DQ2 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON3
Address: Operational Base + offset (0x08BC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR3DeskewL1_cs0 SW Write DQ3 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR3DeskewL0_cs0 SW Write DQ3 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON4
Address: Operational Base + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR4DeskewL1_cs0 SW Write DQ4 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR4DeskewL0_cs0 SW Write DQ4 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON5
Address: Operational Base + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR5DeskewL1_cs0 SW Write DQ5 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR5DeskewL0_cs0 SW Write DQ5 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON6
Address: Operational Base + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR6DeskewL1_cs0 SW Write DQ6 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR6DeskewL0_cs0 SW Write DQ6 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS0_CON7
Address: Operational Base + offset (0x08CC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR7DeskewL1_cs0 SW Write DQ7 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR7DeskewL0_cs0 SW Write DQ7 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DM_DESKEWL_CS0_CON0
Address: Operational Base + offset (0x08D0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WRDMDeskewL1_cs0 SW Write DM De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRDMDeskewL0_cs0 SW Write DM De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_ECC_DESKEWL_CS0_CON0
Address: Operational Base + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WRECCDeskewL1_cs0 SW Write ECC De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRECCDeskewL0_cs0 SW Write ECC De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON0
Address: Operational Base + offset (0x08E0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR0DeskewC1_cs1 SW Write DQ0 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR0DeskewC0_cs1 SW Write DQ0 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON1

Address: Operational Base + offset (0x08E4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR1DeskewC1_cs1 SW Write DQ1 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR1DeskewC0_cs1 SW Write DQ1 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON2

Address: Operational Base + offset (0x08E8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR2DeskewC1_cs1 SW Write DQ2 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR2DeskewC0_cs1 SW Write DQ2 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON3

Address: Operational Base + offset (0x08EC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR3DeskewC1_cs1 SW Write DQ3 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR3DeskewC0_cs1 SW Write DQ3 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON4

Address: Operational Base + offset (0x08F0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR4DeskewC1_cs1 SW Write DQ4 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR4DeskewC0_cs1 SW Write DQ4 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON5

Address: Operational Base + offset (0x08F4)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR5DeskewC1_cs1 SW Write DQ5 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR5DeskewC0_cs1 SW Write DQ5 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON6

Address: Operational Base + offset (0x08F8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR6DeskewC1_cs1 SW Write DQ6 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR6DeskewC0_cs1 SW Write DQ6 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWC_CS1_CON7
Address: Operational Base + offset (0x08FC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR7DeskewC1_cs1 SW Write DQ7 De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR7DeskewC0_cs1 SW Write DQ7 De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DM_DESKEWC_CS1_CON0
Address: Operational Base + offset (0x0900)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WRDMDeskewC1_cs1 SW Write DM De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRDMDeskewC0_cs1 SW Write DM De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_ECC_DESKEWC_CS1_CON0
Address: Operational Base + offset (0x0904)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WRECCDeskewC1_cs1 SW Write ECC De-Skew Center Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRECCDeskewC0_cs1 SW Write ECC De-Skew Center Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_ECC_DESKEWL_CS1_CON0

Address: Operational Base + offset (0x090C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WRECCDeskewL1_cs1 SW Write ECC De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRECCDeskewL0_cs1 SW Write ECC De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON0

Address: Operational Base + offset (0x0910)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR0DeskewL1_cs1 SW Write DQ0 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR0DeskewL0_cs1 SW Write DQ0 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON1

Address: Operational Base + offset (0x0914)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR1DeskewL1_cs1 SW Write DQ1 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR1DeskewL0_cs1 SW Write DQ1 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON2

Address: Operational Base + offset (0x0918)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR2DeskewL1_cs1 SW Write DQ2 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR2DeskewL0_cs1 SW Write DQ2 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON3

Address: Operational Base + offset (0x091C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR3DeskewL1_cs1 SW Write DQ3 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR3DeskewL0_cs1 SW Write DQ3 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON4

Address: Operational Base + offset (0x0920)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR4DeskewL1_cs1 SW Write DQ4 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR4DeskewL0_cs1 SW Write DQ4 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON5
Address: Operational Base + offset (0x0924)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR5DeskewL1_cs1 SW Write DQ5 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR5DeskewL0_cs1 SW Write DQ5 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON6
Address: Operational Base + offset (0x0928)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WR6DeskewL1_cs1 SW Write DQ6 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR6DeskewL0_cs1 SW Write DQ6 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_WR_DESKEWL_CS1_CON7
Address: Operational Base + offset (0x092C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	SW_WR7DeskewL1_cs1 SW Write DQ7 De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WR7DeskewL0_cs1 SW Write DQ7 De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_SW_DM_DESKEWL_CS1_CON0
Address: Operational Base + offset (0x0930)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	SW_WRDMDeskewL1_cs1 SW Write DM De-Skew Left Code for Data Slice1. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	SW_WRDMDeskewL0_cs1 SW Write DM De-Skew Left Code for Data Slice0. Write to this register (1) to restore write training result with wr_sw_mode = 1 (2) before DVFS pause to apply training result for the next DVFS level.

DDRPHY_DVFS0_CON5
Address: Operational Base + offset (0x0934)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:28	RW	0x0	dvfs0_shiftc1 GATE signal delay amount for DDR. This is used to adjust GATE delay based on DFI PHY clock period. 1. When gate_debug_en[3] = 1 for gate margin control 2. When gate_cal_mode = 0 for debug purpose in DVFS0 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. 3'b000: 0(0 degree shift) 3'b001: T(365 degree shift) 3'b010: T/2(180 degree shift) 3'b011: T/4(90 degree shift) 3'b100: T/8(45 degree shift) 3'b101: T/16(22.5 degree shift) 3'b111: 3T/4(270 degree shift)
27	RW	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x0	dvfs0_shiftc0 GATE signal delay amount for DDR. This is used to adjust GATE delay based on DFI PHY clock period. 1. When gate_debug_en[3] = 1 for gate margin control 2. When gate_cal_mode = 0 for debug purpose in DVFS0 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. 3'b000: 0(0 degree shift) 3'b001: T(365 degree shift), 3'b010: T/2(180 degree shift) 3'b011: T/4(90 degree shift) 3'b100: T/8(45 degree shift) 3'b101: T/16(22.5 degree shift) 3'b111: 3T/4(270 degree shift)
23	RW	0x0	Reserved2 Reserved
22:16	RW	0x00	dvfs0_glvl_periodic_fine_incr_adj Periodic (or short) gate training step size at fine mode for DVFS0 mode. It should be smaller than 7'h1F. Default value is 7'b0000000(T/16). [22:21]=2'b00: The step value will be "dvfs0_glvl_periodic_fine_incr_adj[4:0]". [22:21]=2'b01: The step value will be "T/32". [22:21]=2'b10: The step value will be "T/4". [22:21]=2'b11: The step value will be "T/8". [22:16]=7'h00: The step value will be "T/16" (default).
15:14	RW	0x0	Reserved3 Reserved
13	RW	0x0	dvfs0_cmdfifo_wl_ext This field determines command FIFO write latency extention mode for auto dqs clean on DVFS0. ONLY use at LPDDR5. If this field set to 1, PHY can support RL = 21 in LPDDR5
12	RW	0x0	dvfs0_long_gate_train_mode Gate training mode by long gate(shgate =0) for DVFS0 mode
11	RW	0x0	dvfs0_gt_fine_disable Gate training fine mode disable for DVFS0 mode

Bit	Attr	Reset Value	Description
10:8	RW	0x0	dvfs0_glvl_start_adj Gate training start point adjustment for DVFS0 mode. This field adjusts the initial code provided to the gate delay line at the beginning of periodic gate training. [10:8]=2'b000: The start point code is -T from the first DQS risinge edge. [10:8]=2'b001: The start point code is -7T/8 from the first DQS risinge edge. [10:8]=2'b010: The start point code is -6T/8 from the first DQS risinge edge. [10:8]=2'b011: The start point code is -5T/8 from the first DQS risinge edge. [10:8]=2'b100: The start point code is -4T/8 from the first DQS risinge edge. [10:8]=2'b101: The start point code is -3T/8 from the first DQS risinge edge. [10:8]=2'b110: The start point code is -2T/8 from the first DQS risinge edge. [10:8]=2'b111: The start point code is -T/8 from the first DQS risinge edge.
7:0	RW	0x40	dvfs0_glvl_periodic_incr_adj Periodic (or short) gate training step size for DVFS0 mode. It should be smaller than 7'h1F. Default value is 7'b1000000(T/4). [6:5]=2'b00: The step value will be "dvfs0_glvl_periodic_incr_adj[4:0]". [6:5]=2'b01: The step value will be "T/32". [6:5]=2'b10: The step value will be "T/4" (default). [6:5]=2'b11: The step value will be "T/8". [6:0]=7'h00: The step value will be "T/16".

DDRPHY_DVFS1_CON5

Address: Operational Base + offset (0x0938)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:28	RW	0x0	dvfs1_shiftc1 GATE signal delay amount for DDR. This is used to adjust GATE delay based on DFI PHY clock period 1 .when gate_debug_en[3] = 1 for gate margin control 2. when gate_cal_mode = 0 for debug purpose in DVFS1 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. 3'b000: 0(0 degree shift) 3'b001: T(365 degree shift) 3'b010: T/2(180 degree shift) 3'b011: T/4(90 degree shift) 3'b100: T/8(45 degree shift) 3'b101: T/16(22.5 degree shift) 3'b111: 3T/4(270 degree shift)
27	RW	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x0	dvfs1_shiftc0 GATE signal delay amount for DDR. This is used to adjust GATE delay based on DFI PHY clock period 1 .when gate_debug_en[3] = 1 for gate margin control 2. when gate_cal_mode = 0 for debug purpose in DVFS1 mode. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. 3'b000: 0(0 degree shift) 3'b001: T(365 degree shift) 3'b010: T/2(180 degree shift) 3'b011: T/4(90 degree shift) 3'b100: T/8(45 degree shift) 3'b101: T/16(22.5 degree shift) 3'b111: 3T/4(270 degree shift)
23	RW	0x0	Reserved2 Reserved
22:16	RW	0x00	dvfs1_glvl_periodic_fine_incr_adj Periodic gate training step size at fine mode for DVFS1 mode. It should be smaller than 7'h1F. Default value is 7'b0000000(T/16). [22:21]=2'b00: The step value will be "dvfs1_glvl_periodic_fine_incr_adj[4:0]". [22:21]=2'b01: The step value will be "T/32". [22:21]=2'b10: The step value will be "T/4". [22:21]=2'b11: The step value will be "T/8". [22:16]=7'h00: The step value will be "T/16" (default).
15:14	RW	0x0	Reserved3 Reserved
13	RW	0x0	dvfs1_cmdfifo_wl_ext This field determines command FIFO write latency extention mode for auto dqs clean on DVFS1. ONLY use at LPDDR5. If this field set to 1, PHY can support RL = 21 in LPDDR5.
12	RW	0x0	dvfs1_long_gate_train_mode Gate training mode by long gate(shgate =0) for DVFS1 mode
11	RW	0x0	dvfs1_gt_fine_disable Gate training fine mode disable for DVFS1 mode

Bit	Attr	Reset Value	Description
10:8	RW	0x0	dvfs1_glvl_start_adj Gate training start point adjustment for DVFS1 mode. This field adjusts the initial code provided to the gate delay line at the beginning of periodic gate training. [10:8]=2'b000: The start point code is -T from the first DQS risinge edge. [10:8]=2'b001: The start point code is -7T/8 from the first DQS risinge edge. [10:8]=2'b010: The start point code is -6T/8 from the first DQS risinge edge. [10:8]=2'b011: The start point code is -5T/8 from the first DQS risinge edge. [10:8]=2'b100: The start point code is -4T/8 from the first DQS risinge edge. [10:8]=2'b101: The start point code is -3T/8 from the first DQS risinge edge. [10:8]=2'b110: The start point code is -2T/8 from the first DQS risinge edge. [10:8]=2'b111: The start point code is -T/8 from the first DQS risinge edge.
7:0	RW	0x40	dvfs1_glvl_periodic_incr_adj Periodic (or short) gate training step size for DVFS1 mode. It should be smaller than 7'h1F. Default value is 7'b1000000(T/4). [6:5]=2'b00: The step value will be "dvfs1_glvl_periodic_incr_adj[4:0]". [6:5]=2'b01: The step value will be "T/32". [6:5]=2'b10: The step value will be "T/4" (default). [6:5]=2'b11: The step value will be "T/8". [6:0]=7'h00: The step value will be "T/16".

DDRPHY_CAL_WR_PATTERN_CON5

Address: Operational Base + offset (0x093C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8_2nd This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8_2nd This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON6

Address: Operational Base + offset (0x0940)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8_2nd This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8_2nd This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON7

Address: Operational Base + offset (0x0944)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16_2nd This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16_2nd This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON8

Address: Operational Base + offset (0x0948)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16_2nd This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.

Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16_2nd This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON9

Address: Operational Base + offset (0x094C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8_3rd This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8_3rd This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON10

Address: Operational Base + offset (0x0950)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8_3rd This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8_3rd This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON11

Address: Operational Base + offset (0x0954)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16_3rd This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16_3rd This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON12

Address: Operational Base + offset (0x0958)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16_3rd This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16_3rd This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON13

Address: Operational Base + offset (0x095C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst1_8_4th This fields specifies the DQ pattern for BL1 and BL2 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the first valid rising edge of DQS. wrtrn_rddata_adj_w0_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the first valid falling edge of DQS.

Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst1_8_4th This fields specifies the DQ pattern for BL3 and BL4 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase0[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the second valid rising edge of DQS. wrtrn_rddata_adj_w1_phase0[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the second valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON14

Address: Operational Base + offset (0x0960)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst1_8_4th This fields specifies the DQ pattern for BL5 and BL6 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid rising edge of DQS. wrtrn_rddata_adj_w0_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 3rd valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst1_8_4th This fields specifies the DQ pattern for BL7 and BL8 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase1[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase1[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 4th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON15

Address: Operational Base + offset (0x0964)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w0_bst9_16_4th This fields specifies the DQ pattern for BL9 and BL10 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 5th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w1_bst9_16_4th This fields specifies the DQ pattern for BL11 and BL12 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase2[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase2[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 6th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON16

Address: Operational Base + offset (0x0968)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	wrtrn_rddata_adj_w2_bst9_16_4th This fields specifies the DQ pattern for BL13 and BL14 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w0_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid rising edge of DQS. wrtrn_rddata_adj_w0_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 7th valid falling edge of DQS.
15:0	RW	0x00ff	wrtrn_rddata_adj_w3_bst9_16_4th This fields specifies the DQ pattern for BL15 and BL16 during write training. PHY will compare the DQ pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DQ patterns are the same between data_slices. wrtrn_rddata_adj_w1_phase3[7:0] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid rising edge of DQS. wrtrn_rddata_adj_w1_phase3[15:8] represents expected data of DQ[7:0] and DQ[15:8] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON17

Address: Operational Base + offset (0x096C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8_2nd This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8_2nd This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8_2nd This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices.wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.

Bit	Attr	Reset Value	Description
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8_2nd This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data of DM[0] and DQ[1] at the 4th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16_2nd This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16_2nd This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16_2nd This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16_2nd This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON18

Address: Operational Base + offset (0x0970)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8_3rd This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8_3rd This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8_3rd This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices.wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8_3rd This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data of DM[0] and DQ[1] at the 4th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16_3rd This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16_3rd This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.

Bit	Attr	Reset Value	Description
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16_3rd This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16_3rd This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_CAL_WR_PATTERN_CON19

Address: Operational Base + offset (0x0974)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved
15:14	RW	0x1	wrtrn_rddata_dm_adj_w0_bst1_8_4th This fields specifies the DM pattern for BL1 and BL2 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase0[0] represents expected data of DM[0] and DQ[1] at the first valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase0[1] represents expected data of DM[0] and DM[1] at the first valid falling edge of DQS.
13:12	RW	0x1	wrtrn_rddata_dm_adj_w1_bst1_8_4th This fields specifies the DM pattern for BL3 and BL4 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase0[0] represents expected data of DM[0] and DQ[1] at the second valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase0[1] represents expected data of DM[0] and DM[1] at the second valid falling edge of DQS.
11:10	RW	0x1	wrtrn_rddata_dm_adj_w2_bst1_8_4th This fields specifies the DM pattern for BL5 and BL6 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices.wrtrn_rddata_dm_adj_w0_phase1[0] represents expected data of DM[0] and DQ[1] at the 3rd valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase1[1] represents expected data of DM[0] and DM[1] at the 3rd valid falling edge of DQS.

Bit	Attr	Reset Value	Description
9:8	RW	0x1	wrtrn_rddata_dm_adj_w3_bst1_8_4th This fields specifies the DM pattern for BL7 and BL8 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase1[0] represents expected data of DM[0] and DQ[1] at the 4th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase1[1] represents expected data of DM[0] and DM[1] at the 4th valid falling edge of DQS.
7:6	RW	0x1	wrtrn_rddata_dm_adj_w0_bst9_16_4th This fields specifies the DM pattern for BL9 and BL10 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DQ[1] at the 5th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase2[0] represents expected data of DM[0] and DM[1] at the 5th valid falling edge of DQS.
5:4	RW	0x1	wrtrn_rddata_dm_adj_w1_bst9_16_4th This fields specifies the DM pattern for BL11 and BL12 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DQ[1] at the 6th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase2[0] represents expected data of DM[0] and DM[1] at the 6th valid falling edge of DQS.
3:2	RW	0x1	wrtrn_rddata_dm_adj_w2_bst9_16_4th This fields specifies the DM pattern for BL13 and BL14 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DQ[1] at the 7th valid rising edge of DQS. wrtrn_rddata_dm_adj_w0_phase3[0] represents expected data of DM[0] and DM[1] at the 7th valid falling edge of DQS.
1:0	RW	0x1	wrtrn_rddata_dm_adj_w3_bst9_16_4th This fields specifies the DM pattern for BL15 and BL16 during write training. PHY will compare the DM pattern with the read data by MPC-RD FIFO during the initial/periodic write training. DM patterns are the same between data_slices. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DQ[1] at the 8th valid rising edge of DQS. wrtrn_rddata_dm_adj_w1_phase3[0] represents expected data of DM[0] and DM[1] at the 8th valid falling edge of DQS.

DDRPHY_READ_DQ_OFFSET_CTRL0
Address: Operational Base + offset (0x0978)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:24	RW	0x37	RDDQ3OFFSET_DS0 It controls the initial DLL code for Read DQ3 at DS0
23	RW	0x0	Reserved1 Reserved

Bit	Attr	Reset Value	Description
22:16	RW	0x37	RDDQ2OFFSET_DS0 It controls the initial DLL code for Read DQ2 at DS0
15	RW	0x0	Reserved2 Reserved
14:8	RW	0x37	RDDQ1OFFSET_DS0 It controls the initial DLL code for Read DQ1 at DS0
7	RW	0x0	Reserved3 Reserved
6:0	RW	0x37	RDDQ0OFFSET_DS0 It controls the initial DLL code for Read DQ0 at DS0

DDRPHY_READ_DQ_OFFSET_CTRL1

Address: Operational Base + offset (0x097C)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:24	RW	0x37	RDDQ7OFFSET_DS0 It controls the initial DLL code for Read DQ7 at DS0.
23	RW	0x0	Reserved1 Reserved
22:16	RW	0x37	RDDQ6OFFSET_DS0 It controls the initial DLL code for Read DQ6 at DS0.
15	RW	0x0	Reserved2 Reserved
14:8	RW	0x37	RDDQ5OFFSET_DS0 It controls the initial DLL code for Read DQ5 at DS0.
7	RW	0x0	Reserved3 Reserved
6:0	RW	0x37	RDDQ4OFFSET_DS0 It controls the initial DLL code for Read DQ4 at DS0.

DDRPHY_READ_DQ_OFFSET_CTRL2

Address: Operational Base + offset (0x0980)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved0 Reserved
6:0	RW	0x37	RDDM8OFFSET_DS0 It controls the initial DLL code for Read DM at DS0.

DDRPHY_READ_DQ_OFFSET_CTRL3

Address: Operational Base + offset (0x0984)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:24	RW	0x37	RDDQ3OFFSET_DS1 It controls the initial DLL code for Read DQ3 at DS1.
23	RW	0x0	Reserved1 Reserved
22:16	RW	0x37	RDDQ2OFFSET_DS1 It controls the initial DLL code for Read DQ2 at DS1.
15	RW	0x0	Reserved2 Reserved
14:8	RW	0x37	RDDQ1OFFSET_DS1 It controls the initial DLL code for Read DQ1 at DS1.

Bit	Attr	Reset Value	Description
7	RW	0x0	Reserved3 Reserved
6:0	RW	0x37	RDDQ0OFFSET_DS1 It controls the initial DLL code for Read DQ0 at DS1.

DDRPHY_READ_DQ_OFFSET_CTRL4
Address: Operational Base + offset (0x0988)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:24	RW	0x37	RDDQ7OFFSET_DS1 It controls the initial DLL code for Read DQ7 at DS1.
23	RW	0x0	Reserved1 Reserved
22:16	RW	0x37	RDDQ6OFFSET_DS1 It controls the initial DLL code for Read DQ6 at DS1.
15	RW	0x0	Reserved2 Reserved
14:8	RW	0x37	RDDQ5OFFSET_DS1 It controls the initial DLL code for Read DQ5 at DS1.
7	RW	0x0	Reserved3 Reserved
6:0	RW	0x37	RDDQ4OFFSET_DS1 It controls the initial DLL code for Read DQ4 at DS1.

DDRPHY_READ_DQ_OFFSET_CTRL5
Address: Operational Base + offset (0x098C)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved0 Reserved
6:0	RW	0x37	RDDM8OFFSET_DS1 It controls the initial DLL code for Read DM at DS1.

DDRPHY_READ_DQ_OFFSET_CTRL0_CS1
Address: Operational Base + offset (0x0990)

Bit	Attr	Reset Value	Description
31:0	RW	0x37373737	Reserved0 Reserved

DDRPHY_READ_DQ_OFFSET_CTRL1_CS1
Address: Operational Base + offset (0x0994)

Bit	Attr	Reset Value	Description
31:0	RW	0x37373737	Reserved0 Reserved

DDRPHY_READ_DQ_OFFSET_CTRL2_CS1
Address: Operational Base + offset (0x0998)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000037	Reserved0 Reserved

DDRPHY_READ_DQ_OFFSET_CTRL3_CS1
Address: Operational Base + offset (0x099C)

Bit	Attr	Reset Value	Description
31:0	RW	0x37373737	Reserved0 Reserved

DDRPHY_READ_DQ_OFFSET_CTRL4_CS1
Address: Operational Base + offset (0x09A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x37373737	Reserved0 Reserved

DDRPHY_READ_DQ_OFFSET_CTRL5_CS1
Address: Operational Base + offset (0x09A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000037	Reserved0 Reserved

DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL0
Address: Operational Base + offset (0x09A8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved
17:9	RW	0x000	par_duty_wr_p_ds1 This register control duty of write DQs of data_slice 1. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_wr_p_ds0 This register control duty of write DQs of data_slice 0. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.

DDRPHY_WRITE_DQ_DLINE_DUTY_CTRL1
Address: Operational Base + offset (0x09AC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
17:9	RW	0x000	par_duty_wr_n_ds1 This register control duty of write DQs of data_slice 1. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_wr_n_ds0 This register control duty of write DQs of data_slice 0. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 0: Default par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_ds1[#] = 0 & par_duty_wr_n_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_ds1[#] = 1 & par_duty_wr_n_ds1[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL0

Address: Operational Base + offset (0x09B0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved
17:9	RW	0x000	par_duty_rd0_p_ds1 This register control duty of rank0 read DQs of data_slice 1. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 0: Default par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 0: Increase HI duration. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 1: Decrease HI duration. par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_rd0_p_ds0 This register control duty of rank0 read DQs of data_slice 0. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 0: Default par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 0: Increase HI duration. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 1: Decrease HI duration. par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL1

Address: Operational Base + offset (0x09B4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved
17:9	RW	0x000	par_duty_rd0_n_ds1 This register control duty of rank0 read DQs of data_slice 1. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 0: Default par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 0: Increase HI duration. par_duty_rd0_p_ds1[#] = 0 & par_duty_rd0_n_ds1[#] = 1: Decrease HI duration. par_duty_rd0_p_ds1[#] = 1 & par_duty_rd0_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_rd0_n_ds0 This register control duty of rank0 read DQs of data_slice 0. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 0: Default par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 0: Increase HI duration. par_duty_rd0_p_ds0[#] = 0 & par_duty_rd0_n_ds0[#] = 1: Decrease HI duration. par_duty_rd0_p_ds0[#] = 1 & par_duty_rd0_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL2
Address: Operational Base + offset (0x09B8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved
17:9	RW	0x000	par_duty_rd1_p_ds1 This register control duty of rank1 read DQs of data_slice 1. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 0: Default par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 0: Increase HI duration. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 1: Decrease HI duration. par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_rd1_p_ds0 This register control duty of rank1 read DQs of data_slice 0. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 0: Default par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 0: Increase HI duration. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 1: Decrease HI duration. par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_READ_DQ_DLINE_DUTY_CTRL3
Address: Operational Base + offset (0x09BC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved
17:9	RW	0x000	par_duty_rd1_n_ds1 This register control duty of rank1 read DQs of data_slice 1. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 0: Default par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 0: Increase HI duration. par_duty_rd1_p_ds1[#] = 0 & par_duty_rd1_n_ds1[#] = 1: Decrease HI duration. par_duty_rd1_p_ds1[#] = 1 & par_duty_rd1_n_ds1[#] = 1: Increase 1 fine step delay.
8:0	RW	0x000	par_duty_rd1_n_ds0 This register control duty of rank1 read DQs of data_slice 0. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 0: Default par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 0: Increase HI duration. par_duty_rd1_p_ds0[#] = 0 & par_duty_rd1_n_ds0[#] = 1: Decrease HI duration. par_duty_rd1_p_ds0[#] = 1 & par_duty_rd1_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_WRITE_DQS_DLINE_DUTY_CTRL0

Address: Operational Base + offset (0x09C0)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25	RW	0x0	par_duty_wr_dqs_p_ds1 This register control duty of write DQS of data_slice 1. Example for controling duty. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 0: Default par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_wr_p_dqs_ds1[#] = 0 & par_duty_wr_n_dqs_ds1[#] = 1: Decrease HI duration. par_duty_wr_p_dqs_ds1[#] = 1 & par_duty_wr_n_dqs_ds1[#] = 1: Increase 1 fine step delay.
24	RW	0x0	par_duty_wr_dqs_p_ds0 This register control duty of write DQS of data_slice 0. Example for controling duty. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 0: Default par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 1: Decrease HI duration par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 1: Increase 1 fine step delay
23:18	RW	0x00	Reserved1 Reserved

Bit	Attr	Reset Value	Description
17	RW	0x0	par_duty_wr_dqs_n_ds1 This register control duty of write DQS of data_slice 1. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 0: Default par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_wr_dqs_p_ds1[#] = 0 & par_duty_wr_dqs_n_ds1[#] = 1: Decrease HI duration par_duty_wr_dqs_p_ds1[#] = 1 & par_duty_wr_dqs_n_ds1[#] = 1: Increase 1 fine step delay
16	RW	0x0	par_duty_wr_dqs_n_ds0 This register control duty of write DQS of data_slice 0. Each 1bit is able to control 1bit DQ. Example for controling duty. par_duty_wr_dqs_p_ds0[#] = 0 & par_duty_wr_dqs_n_ds0[#] = 0: Default par_duty_wr_dqs_p_ds0[#] = 1 & par_duty_wr_dqs_n_ds0[#] = 0: Increase HI duration. par_duty_wr_dqs_p_ds0[#] = 0 & par_duty_wr_dqs_n_ds0[#] = 1: Decrease HI duration par_duty_wr_dqs_p_ds0[#] = 1 & par_duty_wr_dqs_n_ds0[#] = 1: Increase 1 fine step delay
15:12	RW	0x0	Reserved2 Reserved
11:10	RW	0x0	par_duty_rd_dqs_p_ds1 This register control duty of read DQS of data_slice 1. Example for controling duty. MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 0: Default par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 1: Decrease HI duration par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 1: Increase 1 fine step delay
9:8	RW	0x0	par_duty_rd_dqs_p_ds0 This register control duty of read DQS of data_slice 0. Example for controling duty. MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] = 0: Default par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] = 1: Decrease HI duration. par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 1: Increase 1 fine step delay.
7:4	RW	0x0	Reserved3 Reserved

Bit	Attr	Reset Value	Description
3:2	RW	0x0	par_duty_rd_dqs_n_ds1 This register control duty of read DQS of data_slice 0. Example for controling duty.MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 0: Default par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds1[#] = 0 & par_duty_rd_dqs_n_ds1[#] = 1: Decrease HI duration. par_duty_rd_dqs_p_ds1[#] = 1 & par_duty_rd_dqs_n_ds1[#] = 1: Increase 1 fine step delay.
1:0	RW	0x0	par_duty_rd_dqs_n_ds0 This register control duty of read DQS of data_slice 0. Example for controling duty. MSB is able to control rank1 and LSB is able to control rank0. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] = 0: Default par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 0: Increase HI duration. par_duty_rd_dqs_p_ds0[#] = 0 & par_duty_rd_dqs_n_ds0[#] = 1: Decrease HI duration. par_duty_rd_dqs_p_ds0[#] = 1 & par_duty_rd_dqs_n_ds0[#] = 1: Increase 1 fine step delay.

DDRPHY_DQ_SEL_CTRL0

Address: Operational Base + offset (0x09C4)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x2	par_sel0_dm8_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DM at read dqs rising edge in data_slice0. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.
23:21	RW	0x2	par_sel0_dq7_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ7 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay

Bit	Attr	Reset Value	Description
20:18	RW	0x2	par_sel0_dq6_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ6 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ5 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.
14:12	RW	0x2	par_sel0_dq4_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ4 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ3 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ2 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ1 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.

Bit	Attr	Reset Value	Description
2:0	RW	0x2	par_sel0_dq0_l_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ0 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.

DDRPHY_DQ_SEL_CTRL1

Address: Operational Base + offset (0x09C8)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x2	par_sel0_dm8_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DM at read dqs rising edge in data_slice1. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ7 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ6 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ5 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay

Bit	Attr	Reset Value	Description
14:12	RW	0x2	par_sel0_dq4_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ4 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ3 at read dqs rising edge in data_slice3. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.
8:6	RW	0x2	par_sel0_dq2_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ2 at read dqs rising edge in data_slice2. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ1 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
2:0	RW	0x2	par_sel0_dq0_l_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ0 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay

DDRPHY_DQ_SEL_CTRL2

Address: Operational Base + offset (0x09CC)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x2	par_sel0_dm8_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DM at read dqs falling edge in data_slice0. The selection is able to control the delay of DM rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ7 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ7 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.
20:18	RW	0x2	par_sel0_dq6_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ6 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ6 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ5 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ5 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.
14:12	RW	0x2	par_sel0_dq4_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ4 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ4 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ3 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ3 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.

Bit	Attr	Reset Value	Description
8:6	RW	0x2	par_sel0_dq2_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ2 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ2 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.
5:3	RW	0x2	par_sel0_dq1_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ1 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ1 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.
2:0	RW	0x2	par_sel0_dq0_h_rank0_ds0 This register select delayed output among 5 different delayed signal of rank0 DQ0 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ0 rising edge. 3'd0: Default delay - 2 coarse delay. 3'd1: Default delay - 1 coarse delay. 3'd2: Default delay 3'd3: Default delay + 1 coarse delay. 3'd4: Default delay + 2 coarse delay.

DDRPHY_DQ_SEL_CTRL3

Address: Operational Base + offset (0x09D0)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x2	par_sel0_dm8_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DM at read dqs falling edge in data_slice1. The selection is able to control the delay of DM rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ7 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ7 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.

Bit	Attr	Reset Value	Description
20:18	RW	0x2	par_sel0_dq6_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ6 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ6 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ5 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ5 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ4 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ4 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ3 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ3 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ2 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ2 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ1 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ1 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay

Bit	Attr	Reset Value	Description
2:0	RW	0x2	par_sel0_dq0_h_rank0_ds1 This register select delayed output among 5 different delayed signal of rank0 DQ0 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ0 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.

DDRPHY_DQ_SEL_CTRL4

Address: Operational Base + offset (0x09D4)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x2	par_sel0_dm8_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DM at read dqs rising edge in data_slice0. The selection is able to control the delay of DM rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ7 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ7 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
20:18	RW	0x2	par_sel0_dq6_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ6 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ6 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
17:15	RW	0x2	par_sel0_dq5_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ5 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ5 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.

Bit	Attr	Reset Value	Description
14:12	RW	0x2	par_sel0_dq4_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ4 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ4 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
11:9	RW	0x2	par_sel0_dq3_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ3 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ3 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ2 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ2 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ1 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ1 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
2:0	RW	0x2	par_sel0_dq0_l_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ0 at read dqs rising edge in data_slice0. The selection is able to control the delay of DQ0 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.

DDRPHY_DQ_SEL_CTRL5

Address: Operational Base + offset (0x09D8)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x2	par_sel0_dm8_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DM at read dqs rising edge in data_slice1. The selection is able to control the delay of DM rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
23:21	RW	0x2	par_sel0_dq7_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ7 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ7 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
20:18	RW	0x2	par_sel0_dq6_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ6 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ6 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
17:15	RW	0x2	par_sel0_dq5_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ5 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ5 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ4 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ4 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ3 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ3 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay

Bit	Attr	Reset Value	Description
8:6	RW	0x2	par_sel0_dq2_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ2 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ2 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
5:3	RW	0x2	par_sel0_dq1_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ1 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ1 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
2:0	RW	0x2	par_sel0_dq0_l_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ0 at read dqs rising edge in data_slice1. The selection is able to control the delay of DQ0 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.

DDRPHY_DQ_SEL_CTRL6

Address: Operational Base + offset (0x09DC)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x2	par_sel0_dm8_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DM at read dqs falling edge in data_slice0. The selection is able to control the delay of DM rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
23:21	RW	0x2	par_sel0_dq7_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ7 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ7 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay

Bit	Attr	Reset Value	Description
20:18	RW	0x2	par_sel0_dq6_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ6 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ6 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
17:15	RW	0x2	par_sel0_dq5_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ5 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ5 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
14:12	RW	0x2	par_sel0_dq4_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ4 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ4 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ3 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ3 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
8:6	RW	0x2	par_sel0_dq2_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ2 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ2 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
5:3	RW	0x2	par_sel0_dq1_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ1 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ1 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay

Bit	Attr	Reset Value	Description
2:0	RW	0x2	par_sel0_dq0_h_rank1_ds0 This register select delayed output among 5 different delayed signal of rank1 DQ0 at read dqs falling edge in data_slice0. The selection is able to control the delay of DQ0 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.

DDRPHY_DQ_SEL_CTRL7

Address: Operational Base + offset (0x09E0)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x2	par_sel0_dm8_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DM at read dqs falling edge in data_slice1. The selection is able to control the delay of DM rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
23:21	RW	0x2	par_sel0_dq7_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ7 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ7 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
20:18	RW	0x2	par_sel0_dq6_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ6 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ6 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
17:15	RW	0x2	par_sel0_dq5_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ5 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ5 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay

Bit	Attr	Reset Value	Description
14:12	RW	0x2	par_sel0_dq4_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ4 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ4 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
11:9	RW	0x2	par_sel0_dq3_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ3 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ3 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay
8:6	RW	0x2	par_sel0_dq2_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ2 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ2 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
5:3	RW	0x2	par_sel0_dq1_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ1 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ1 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.
2:0	RW	0x2	par_sel0_dq0_h_rank1_ds1 This register select delayed output among 5 different delayed signal of rank1 DQ0 at read dqs falling edge in data_slice1. The selection is able to control the delay of DQ0 rising edge. 3'd0 : default delay - 2 coarse delay. 3'd1 : default delay - 1 coarse delay. 3'd2 : default delay 3'd3 : default delay + 1 coarse delay. 3'd4 : default delay + 2 coarse delay.

DDRPHY_CK_DLINE_DUTY_CTRL0

Address: Operational Base + offset (0x09E4)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved
1	RW	0x0	par_duty_ck_n controls par_duty_wr_n of ctrl_slice
0	RW	0x0	par_duty_ck_p controls par_duty_wr_p of ctrl_Sclie

DDRPHY_IO_DUTY_CTRL0
Address: Operational Base + offset (0x09E8)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29:27	RW	0x5	duty_dqs_io_cntp_ds0 It controls io_dqs_duty_ctrlp[2:0] under PHYIO_SLICE
26:24	RW	0x5	duty_dm8_io_cntp_ds0 It controls io_dm0_duty_ctrlp under PHYIO_SLICE
23:21	RW	0x5	duty_dq7_io_cntp_ds0 It controls io_dq7_duty_ctrlp under PHYIO_SLICE
20:18	RW	0x5	duty_dq6_io_cntp_ds0 It controls io_dq6_duty_ctrlp under PHYIO_SLICE
17:15	RW	0x5	duty_dq5_io_cntp_ds0 It controls io_dq5_duty_ctrlp under PHYIO_SLICE
14:12	RW	0x5	duty_dq4_io_cntp_ds0 It controls io_dq4_duty_ctrlp under PHYIO_SLICE
11:9	RW	0x5	duty_dq3_io_cntp_ds0 It controls io_dq3_duty_ctrlp under PHYIO_SLICE
8:6	RW	0x5	duty_dq2_io_cntp_ds0 It controls io_dq2_duty_ctrlp under PHYIO_SLICE
5:3	RW	0x5	duty_dq1_io_cntp_ds0 It controls io_dq1_duty_ctrlp under PHYIO_SLICE
2:0	RW	0x5	duty_dq0_io_cntp_ds0 It controls io_dq0_duty_ctrlp under PHYIO_SLICE

DDRPHY_IO_DUTY_CTRL1
Address: Operational Base + offset (0x09EC)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29:27	RW	0x5	duty_dqs_io_cntp_ds1 It controls io_dqs_duty_ctrlp[5:3] under PHYIO_SLICE
26:24	RW	0x5	duty_dm8_io_cntp_ds1 It controls io_dm1_duty_ctrlp under PHYIO_SLICE
23:21	RW	0x5	duty_dq7_io_cntp_ds1 It controls io_dq15_duty_ctrlp under PHYIO_SLICE
20:18	RW	0x5	duty_dq6_io_cntp_ds1 It controls io_dq14_duty_ctrlp under PHYIO_SLICE
17:15	RW	0x5	duty_dq5_io_cntp_ds1 It controls io_dq13_duty_ctrlp under PHYIO_SLICE
14:12	RW	0x5	duty_dq4_io_cntp_ds1 It controls io_dq12_duty_ctrlp under PHYIO_SLICE
11:9	RW	0x5	duty_dq3_io_cntp_ds1 It controls io_dq11_duty_ctrlp under PHYIO_SLICE
8:6	RW	0x5	duty_dq2_io_cntp_ds1 It controls io_dq10_duty_ctrlp under PHYIO_SLICE
5:3	RW	0x5	duty_dq1_io_cntp_ds1 It controls io_dq9_duty_ctrlp under PHYIO_SLICE
2:0	RW	0x5	duty_dq0_io_cntp_ds1 It controls io_dq8_duty_ctrlp under PHYIO_SLICE

DDRPHY_IO_DUTY_CTRL2
Address: Operational Base + offset (0x09F0)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved
28:27	RW	0x3	duty_dqs_io_cntn_ds0 It controls io_dqs_duty_ctrln[1:0] under PHYIO_SLICE
26:24	RW	0x3	duty_dm8_io_cntn_ds0 It controls io_dm0_duty_ctrln under PHYIO_SLICE
23:21	RW	0x3	duty_dq7_io_cntn_ds0 It controls io_dq7_duty_ctrln under PHYIO_SLICE
20:18	RW	0x3	duty_dq6_io_cntn_ds0 It controls io_dq6_duty_ctrln under PHYIO_SLICE
17:15	RW	0x3	duty_dq5_io_cntn_ds0 It controls io_dq5_duty_ctrln under PHYIO_SLICE
14:12	RW	0x3	duty_dq4_io_cntn_ds0 It controls io_dq4_duty_ctrln under PHYIO_SLICE
11:9	RW	0x3	duty_dq3_io_cntn_ds0 It controls io_dq3_duty_ctrln under PHYIO_SLICE
8:6	RW	0x3	duty_dq2_io_cntn_ds0 It controls io_dq2_duty_ctrln under PHYIO_SLICE
5:3	RW	0x3	duty_dq1_io_cntn_ds0 It controls io_dq1_duty_ctrln under PHYIO_SLICE
2:0	RW	0x3	duty_dq0_io_cntn_ds0 It controls io_dq0_duty_ctrln under PHYIO_SLICE

DDRPHY_IO_DUTY_CTRL3

Address: Operational Base + offset (0x09F4)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved
28:27	RW	0x3	duty_dqs_io_cntn_ds1 It controls io_dqs_duty_ctrln[4:3] under PHYIO_SLICE
26:24	RW	0x3	duty_dm8_io_cntn_ds1 It controls io_dm1_duty_ctrln under PHYIO_SLICE
23:21	RW	0x3	duty_dq7_io_cntn_ds1 It controls io_dq15_duty_ctrln under PHYIO_SLICE
20:18	RW	0x3	duty_dq6_io_cntn_ds1 It controls io_dq14_duty_ctrln under PHYIO_SLICE
17:15	RW	0x3	duty_dq5_io_cntn_ds1 It controls io_dq13_duty_ctrln under PHYIO_SLICE
14:12	RW	0x3	duty_dq4_io_cntn_ds1 It controls io_dq12_duty_ctrln under PHYIO_SLICE
11:9	RW	0x3	duty_dq3_io_cntn_ds1 It controls io_dq11_duty_ctrln under PHYIO_SLICE
8:6	RW	0x3	duty_dq2_io_cntn_ds1 It controls io_dq10_duty_ctrln under PHYIO_SLICE
5:3	RW	0x3	duty_dq1_io_cntn_ds1 It controls io_dq9_duty_ctrln under PHYIO_SLICE
2:0	RW	0x3	duty_dq0_io_cntn_ds1 It controls io_dq8_duty_ctrln under PHYIO_SLICE

DDRPHY_IO_DUTY_CTRL4

Address: Operational Base + offset (0x09F8)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
19	RW	0x0	duty_dqs_io_en_ds1 It controls io_dqs_duty_ctrl_en[1] under PHYIO_SLICE
18	RW	0x0	duty_dm8_io_en_ds1 It controls io_dm_duty_ctrl_en[1] under PHYIO_SLICE
17	RW	0x0	duty_dq7_io_en_ds1 It controls io_dq_duty_ctrl_en[15] under PHYIO_SLICE
16	RW	0x0	duty_dq6_io_en_ds1 It controls io_dq_duty_ctrl_en[14] under PHYIO_SLICE
15	RW	0x0	duty_dq5_io_en_ds1 It controls io_dq_duty_ctrl_en[13] under PHYIO_SLICE
14	RW	0x0	duty_dq4_io_en_ds1 It controls io_dq_duty_ctrl_en[12] under PHYIO_SLICE
13	RW	0x0	duty_dq3_io_en_ds1 It controls io_dq_duty_ctrl_en[11] under PHYIO_SLICE
12	RW	0x0	duty_dq2_io_en_ds1 It controls io_dq_duty_ctrl_en[10] under PHYIO_SLICE
11	RW	0x0	duty_dq1_io_en_ds1 It controls io_dq_duty_ctrl_en[9] under PHYIO_SLICE
10	RW	0x0	duty_dq0_io_en_ds1 It controls io_dq_duty_ctrl_en[8] under PHYIO_SLICE
9	RW	0x0	duty_dqs_io_en_ds0 It controls io_dqs_duty_ctrl_en[0] under PHYIO_SLICE
8	RW	0x0	duty_dm8_io_en_ds0 It controls io_dm_duty_ctrl_en[0] under PHYIO_SLICE
7	RW	0x0	duty_dq7_io_en_ds0 It controls io_dq_duty_ctrl_en[7] under PHYIO_SLICE
6	RW	0x0	duty_dq6_io_en_ds0 It controls io_dq_duty_ctrl_en[6] under PHYIO_SLICE
5	RW	0x0	duty_dq5_io_en_ds0 It controls io_dq_duty_ctrl_en[5] under PHYIO_SLICE
4	RW	0x0	duty_dq4_io_en_ds0 It controls io_dq_duty_ctrl_en[4] under PHYIO_SLICE
3	RW	0x0	duty_dq3_io_en_ds0 It controls io_dq_duty_ctrl_en[3] under PHYIO_SLICE
2	RW	0x0	duty_dq2_io_en_ds0 It controls io_dq_duty_ctrl_en[2] under PHYIO_SLICE
1	RW	0x0	duty_dq1_io_en_ds0 It controls io_dq_duty_ctrl_en[1] under PHYIO_SLICE
0	RW	0x0	duty_dq0_io_en_ds0 It controls io_dq_duty_ctrl_en[0] under PHYIO_SLICE

DDRPHY_IO_DUTY_CTRL5

Address: Operational Base + offset (0x09FC)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved0 Reserved
20	RW	0x0	duty_wck_io_en_ds1 It controls io_wck_duty_ctrl_en BYTE1 under PHYIO_SLICE
19:17	RW	0x0	duty_wck_io_cntn_ds1 It controls io_wck_duty_ctrln BYTE1 under PHYIO_SLICE
16:14	RW	0x0	duty_wck_io_cntp_ds1 It controls io_wck_duty_ctrlp BYTE1 under PHYIO_SLICE
13	RW	0x0	duty_wck_io_en_ds0 It controls io_wck_duty_ctrl_en BYTE0 under PHYIO_SLICE

Bit	Attr	Reset Value	Description
12:10	RW	0x0	duty_wck_io_cntn_ds0 It controls io_wck_duty_ctrln BYTE0 under PHYIO_SLICE
9:7	RW	0x0	duty_wck_io_cntp_ds0 It controls io_wck_duty_ctrlp BYTE0 under PHYIO_SLICE
6	RW	0x0	duty_ck_io_en It controls io_ck_duty_ctrl_en under PHYIO_SLICE
5	RW	0x0	Reserved1 Reserved
4:3	RW	0x3	duty_ck_io_cntn It controls io_ck_duty_ctrln under PHYIO_SLICE
2:0	RW	0x5	duty_ck_io_cntp It controls io_ck_duty_ctrlp under PHYIO_SLICE

DDRPHY_DVFS0_CON6

Address: Operational Base + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved
21:19	RW	0x7	dvfs0_zq_ck_dds Driver pull-down strength control for CK pad. It controls io_zq_ck_dds in dvfs mode 0. One of the following settings is recommended instead of 3'h0. 3'b100: 48 ohm impedance output driver 3'b101: 40 ohm impedance output driver 3'b110: 34 ohm impedance output driver 3'b111: 30 ohm impedance output driver
18:16	RW	0x7	dvfs0_zq_ck_pdds Driver pull-up strength control for CK pad. It controls io_zq_ck_pdds in dvfs mode 0
15:14	RW	0x0	Reserved1 Reserved
13:12	RW	0x0	dvfs0_zq_ds1_ibias_ctrl impcnt bias current control for DS1. controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 0
11:10	RW	0x0	dvfs0_zq_ds0_ibias_ctrl impcnt bias current control for DS0. controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 0
9:8	RW	0x0	dvfs0_zq_mode_ibias_ctrl impcnt bias current control for CS. controls io_zq_mode_ibias_ctrl under PHYIO_SLICE in dvfs mode 0
7:4	RW	0x0	dvfs0_ds1_testircv controls io_dqs1_testircv under PHYIO_SLICE in dvfs mode 0
3:0	RW	0x0	dvfs0_ds0_testircv controls io_dqs0_testircv under PHYIO_SLICE in dvfs mode 0

DDRPHY_DVFS1_CON6

Address: Operational Base + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
21:19	RW	0x7	dvfs1_zq_ck_dds Driver pull-down strength control for CK pad. It controls io_zq_ck_dds in dvfs mode 1. One of the following settings is recommended instead of 3'h0. 3'b100 : 48 ohm Impedance output driver 3'b101 : 40 ohm Impedance output driver 3'b110 : 34 ohm Impedance output driver 3'b111 : 30 ohm Impedance output driver
18:16	RW	0x7	dvfs1_zq_ck_pdds Driver pull-up strength control for CK pad. It controls io_zq_ck_pdds in dvfs mode 1
15:14	RW	0x0	Reserved1 Reserved
13:12	RW	0x0	dvfs1_zq_ds1_ibias_ctrl impcnt bias current control for DS1. controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 1
11:10	RW	0x0	dvfs1_zq_ds_ibias_ctrl impcnt bias current control for DS0. controls io_zq_ds_ibias_ctrl[3:2] under PHYIO_SLICE in dvfs mode 1
9:8	RW	0x0	dvfs1_zq_mode_ibias_ctrl impcnt bias current control for CS. controls io_zq_mode_ibias_ctrl under PHYIO_SLICE in dvfs mode 1
7:4	RW	0x0	dvfs1_ds1_testircv controls io_dqs1_testircv under PHYIO_SLICE in dvfs mode 1
3:0	RW	0x0	dvfs1_ds0_testircv controls io_dqs0_testircv under PHYIO_SLICE in dvfs mode 1

DDRPHY_DQOENDESKEWCODE0

Address: Operational Base + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x0	dqoendeskewcode_dm_ds0 DM0 OEN offset control. It controls io_dm_en[1] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dm_ds0*1tFS.
23:21	RW	0x0	dqoendeskewcode_dq7_ds0 DQ7 OEN offset control. It controls io_dq_en[7] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq7_ds0*1tFS.
20:18	RW	0x0	dqoendeskewcode_dq6_ds0 DQ6 OEN offset control. It controls io_dq_en[6] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq6_ds0*1tFS.
17:15	RW	0x0	dqoendeskewcode_dq5_ds0 DQ5 OEN offset control. It controls io_dq_en[5] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq5_ds0*1tFS.
14:12	RW	0x0	dqoendeskewcode_dq4_ds0 DQ4 OEN offset control. It controls io_dq_en[4] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq4_ds0*1tFS.

Bit	Attr	Reset Value	Description
11:9	RW	0x0	dqoendeskewcode_dq3_ds0 DQ3 OEN offset control. It controls io_dq_en[3] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq3_ds0*1tFS.
8:6	RW	0x0	dqoendeskewcode_dq2_ds0 DQ2 OEN offset control. It controls io_dq_en[2] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq2_ds0*1tFS.
5:3	RW	0x0	dqoendeskewcode_dq1_ds0 DQ1 OEN offset control. It controls io_dq_en[1] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq1_ds0*1tFS.
2:0	RW	0x0	dqoendeskewcode_dq0_ds0 DQ0 OEN offset control. It controls io_dq_en[0] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq0_ds0*1tFS.

DDRPHY_DQOENDESKEWCODE1

Address: Operational Base + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:24	RW	0x0	dqoendeskewcode_dm_ds1 DM1 OEN offset control. It controls io_dm_en[1] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dm_ds1*1tFS.
23:21	RW	0x0	dqoendeskewcode_dq7_ds1 DQ15 OEN offset control. It controls io_dq_en[15] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq7_ds1*1tFS.
20:18	RW	0x0	dqoendeskewcode_dq6_ds1 DQ14 OEN offset control. It controls io_dq_en[14] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq6_ds1*1tFS.
17:15	RW	0x0	dqoendeskewcode_dq5_ds1 DQ13 OEN offset control. It controls io_dq_en[13] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq5_ds1*1tFS.
14:12	RW	0x0	dqoendeskewcode_dq4_ds1 DQ12 OEN offset control. It controls io_dq_en[12] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq4_ds1*1tFS.
11:9	RW	0x0	dqoendeskewcode_dq3_ds1 DQ11 OEN offset control. It controls io_dq_en[11] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq3_ds1*1tFS.
8:6	RW	0x0	dqoendeskewcode_dq2_ds1 DQ10 OEN offset control. It controls io_dq_en[10] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq2_ds1*1tFS.
5:3	RW	0x0	dqoendeskewcode_dq1_ds1 DQ9 OEN offset control. It controls io_dq_en[9] under PHYIO_SLICE. The amount of delay is dqoendeskewcode_dq1_ds1*1tFS.

Bit	Attr	Reset Value	Description
2:0	RW	0x0	dqoendeskewcode_dq0_ds1 DQ8 OEN offset control. It controls io_dq_en[8] under PHYIO_SLICE under PHYIO_SLICE delay. The amount of delay is dqoendeskewcode_dq0_ds1*1tFS.

DDRPHY_DQSOENDESKEWCODE
Address: Operational Base + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved0 Reserved
5:3	RW	0x0	dqsoendeskewcode_ds1 DQS1 OEN offset control. It controls io_pdqs_en[1] and io_ndqs_en[1] under PHYIO_SLICE. The amount of delay is dqsoendeskewcode_ds1*1tFS.
2:0	RW	0x0	dqsoendeskewcode_ds0 DQS0 OEN offset control. It controls io_pdqs_en[0] and io_ndqs_en[0] under PHYIO_SLICE. The amount of delay is dqsoendeskewcode_ds0*1tFS.

DDRPHY_DTB
Address: Operational Base + offset (0x0A14)

Bit	Attr	Reset Value	Description
31	RW	0x0	DTB_enable DTB enable. If DTB_enable is 1, DDRPHY_DTB will be driven depending on DTB_select. If DTB_enable is 0, DDRPHY_DTB = 4'h0.
30:8	RW	0x000000	Reserved0 Reserved
7:0	RW	0x00	DTB_select DTB select. It determines which signal is driven on DDRPHY_DTB. 8'd0: {2'h0, dfi_init_start, dfi_init_complete} 8'd1: {dfi_phyupd_req, dfi_phyupd_ack, dfi_ctrlupd_req, dfi_ctrlupd_ack} 8'd2: {2'h0, cs_phyupd} 8'd3: {1'h0, cs_phydvfs} 8'd4: rdfifo_rptr (ds1) 8'd5: rdfifo_rptr (ds0) 8'd6: rdfifo_wptr (ds1) 8'd7: rdfifo_wptr (ds0) 8'd8: {3'h0, dfi_reset_n} 8'd10: {3'h0, ctrl_dll_on} 8'd11: {3'h0, ctrl_phy_cg_en} 8'd12: {dfi_cke_p0} 8'd13: {dfi_cke_p1} 8'd14: {dfi_cke_p2} 8'd15: {dfi_cke_p3}

DDRPHY_GTCC_CON0
Address: Operational Base + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	gtcc_offsetc1 Gate center control offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and ctrl_vtc_en is high and dfi_ctrlupd_req becomes HIGH and LOW. It is used to give offset to gate training result (T/2 from DQS rising edge by default) for debug purpose. gtcc_offsetc [9] = 1 : (tFS: fine step delay) Total GATE delay amount - gtcc_offsetc [8:0] x tFS gtcc_offsetc [9] = 0 : Total GATE delay amount + gtcc_offsetc [8:0] x tFS
15:10	RW	0x00	Reserved1 Reserved
9:0	RW	0x000	gtcc_offsetc0 Gate offset control offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after ctrl_vtc_en is high and dfi_ctrlupd_req becomes HIGH and LOW. It is used to give offset to gate training result (T/2 from DQS rising edge by default) for debug purpose. gtcc_offsetc [9] = 1 : (tFS: fine step delay) Total GATE delay amount - gtcc_offsetc [8:0] x tFS gtcc_offsetc [9] = 0 : Total GATE delay amount + gtcc_offsetc [8:0] x tFS

DDRPHY_RANK1_CON0

Address: Operational Base + offset (0x0A1C)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved
18	RW	0x0	per_rank_rl_enable Enable signal to support assymmetric rank RL. If this field is enabled, RL of rank1(*_rdlat_rank1) should be set.
17:12	RW	0x20	dvfs1_rdlat_rank1 This field will be used instead of ctrl_rdlat_rank1 during DVFS1 mode.
11:6	RW	0x20	dvfs0_rdlat_rank1 This field will be used instead of ctrl_rdlat_rank1 during DVFS0 mode.
5:0	RW	0x20	ctrl_rdlat_rank1 Read latency(RL) for RANK1

DDRPHY_SCHD_CON0

Address: Operational Base + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved1 Reserved
7	RW	0x0	schd_fsm_clear Phy scheduler FSM reset. Please use set and clear for FSM reset
6	RW	0x1	sw_cmd_start If this bit is disabled, the scheduler command will not be generated. When the sw_cmd_start is enabled, the commands in FIFO that you already requested will be generated by the timing parameter.

Bit	Attr	Reset Value	Description
5	RW	0x0	phy_mstr_cnt_en_APB Enable dfi_phymstr counter. dfi_phymstr_req will be disabled 64 DFI cycles, when dfi_phymstr_ack is not asserted.
4	RW	0x0	dvfs_train_force DVFS training force start control for debug purpose. DVFS training will start when this register changes from 0 to 1 even when there is no frequency change handshake.
3	RW	0x0	periodic_train_force Periodic training force can control for debugging pupose and SW initiated training. Periodic training will be initiated one time when this register changes from 0 to 1. HW Periodic training should be disabled by periodic_en = 0, before periodic training is initiated by this register. Please follow procedure below For debug purpose using HW periodic training. PHY initial training --> HW periodic training enable --> HW periodic training disable --> schd_fsm_clear set and clear --> SW periodic training enable --> SW periodic training disable. Also if this field used by SW periodic training, do not use the mix up both HW periodic training and SW periodic training for normal operation.
2	RW	0x0	phy_mstr_bypass Master interface bypass control. If phy_mstr_bypass = 1, the handshake of DFI PHY master mode is skipped when periodic/dvfs training is excuted.
1	RW	0x0	scheduler_cg_en_disable Scheduler clock gating disable.
0	RW	0x0	scheduler_sw_mode SW sheduler mode enable

DDRPHY_SCHD_TRAIN_CON0

Address: Operational Base + offset (0x0A24)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved
23:22	RW	0x0	periodic_wrtrn_en Enable periodic write training mode. bit[0]: CS-0 enable bit[1]: CS-1 enable
21:20	RW	0x0	periodic_gttrn_en Enable periodic gate training mode. bit[0]: CS-0 enable bit[1]: CS-1 enable
19:18	RW	0x0	dvfs_wrtrn_en Enable DVFS write training mode. bit[0]: CS-0 enable bit[1]: CS-1 enable
17:16	RW	0x0	dvfs_gttrn_en Enable DVFS gate traininig mode. bit[0]: CS-0 enable bit[1]: CS-1 enable

Bit	Attr	Reset Value	Description
15:14	RW	0x0	phy_wrtrn_rank_en Per rank write training enable. 2'b01: Enable rank0. 2'b10: Enable rank1.
13:12	RW	0x0	phy_rdtrn_rank_en Per rank read training enable. 2'b01: Enable rank0. 2'b10: Enable rank1.
11:10	RW	0x0	phy_gttrn_rank_en Per rank gate leveling enable. 2'b01: Enable rank0. 2'b10: Enable rank1.
9:8	RW	0x0	phy_wrlvl_rank_en Per rank write leveling enable. 2'b01: Enable Rank0. 2'b10: Enable Rank1.
7	RW	0x0	phy_wlcal_en Enable WL calibration for DDR4 and DDR3. 1'b0: Disable(default) 1'b1: Control cycle of DQS for searching optimal WL.
6	RW	0x0	phy_wrtrn_en Enable PHY write training mode.
5	RW	0x0	phy_rdtrn_en Enable PHY read training mode.
4	RW	0x0	phy_gttrn_en Enable PHY gate leveling mode.
3	RW	0x0	phy_wrlvl_en Enable PHY write leveling mode.
2	RW	0x0	phy_cbt_en Enable PHY CBT mode.
1	RO	0x0	phy_train_done When phy_train_done is high, phy training mode is finished. Please disable phy_training_en.
0	RW	0x0	phy_train_en PHY training mode enable. It should be enabled after setting CAL_CON5[23:1]. Please disable after phy_train_done is high.

DDRPHY_SCHD_TRAIN_CON1

Address: Operational Base + offset (0x0A28)

Bit	Attr	Reset Value	Description
31	RW	0x0	periodic_en Periodic training enable
30:0	RW	0x000403f5	periodic_time Periodic_time is defined interval of periodic training. Total time = periodic_time*(period of clk_osc)

DDRPHY_SCHD_TIME_CON0

Address: Operational Base + offset (0x0A2C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved
23:18	RW	0x16	tMRW MRW-to-MRW delay time based on memory clk. LPDDR4, LPDDR5: Refer to the Jedec spec about tMRW.

Bit	Attr	Reset Value	Description
17:14	RW	0x8	tMRR MRR-to-MRR delay time based on memory clk. LPDDR4, LPDDR5: Refer to the Jedec spec about tMRR.
13:11	RW	0x0	Reserved0 Reserved
10:6	RW	0x07	phy_t_rddata_en dfi_rddata_en latency. It defines latency of generating dfi_rddata_en after RL(read latency from RD CMD). trddata_en is defined as (RL+phy_t_rddata_en)*memory clock. Note that RL+phy_t_rddata_en should be even number to meet dfi_rddata_en phase requirement. If the sum is odd number, increase phy_t_rddata_en by 1.
5:0	RW	0x12	WL Write latency. It decide latency of generating dfi_wrdata_en after WL(Write Latency from WR CMD).

DDRPHY_SCHD_TIME_CON1

Address: Operational Base + offset (0x0A30)

Bit	Attr	Reset Value	Description
31:28	RW	0x6	tNOP WR-to-NOP or NOP-to-WR delay time based on memory clk.
27:22	RW	0x10	tWTR WRITE-to-READ or LP4_MPC_WR-to_LP4_MPC_RD delay time based on memory clk. Refer to the Jedec spec about tWTR. If you set this bit(tWTR), the each delay will be below value. LPDDR4: (Write-to-Read) WL+1+BL/2+tWTR, (LP4_MPC_WR-to-LP4_MPC_RD) WL+BL/2+tWTR+8 LPDDR5: (Write-to-Read) WL+tBL_divn+tWTR (LP5_WFF-to-LP5_WFF) WL+tBL_divn+tWTR
21:14	RW	0x34	tRCD ACT-to-WRITE delay time based on memory clk. LPDDR4, LPDDR5: Refer to the Jedec spec about tRCD.
13:8	RW	0x10	tRTP READ-to-PRE delay time based on memory clk. Refer to the Jedec spec about tRTP. If you set this bit(tRTP), the each delay wil be below value. LPDDR4: tRTP+BL/2-8 LPDDR5: X
7:0	RW	0x08	tCCD LPDDR4: WRITE-to-WRITE or READ-to-READ or LP4_MPC_RD_DQ_CAL-to-LP4_MPC_RD_DQ_CAL delay time based on memory clk. LPDDR5: LP5_RDC-to-LP5_RDC delay time based on memory clk. Refer to the Jedec spec about tCCD range.

DDRPHY_SCHD_TIME_CON2

Address: Operational Base + offset (0x0A34)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved
30:27	RW	0x0	tDES Default latency

Bit	Attr	Reset Value	Description
26:21	RW	0x1e	tURTW User Read-to-Write or LP4_MPC_RD_FIFO-to-LP4_MPC_WR_FIFO delay time based on memory clk. Refer to the Jedec spec about delay of read to write or MPC READ FIFO to MPC WRITE FIFO. If you set this bit(tURTW), the each delay will be below value. LPDDR4: (Read-to-Write) RL+BL/2-WL+tURTW, (LP4_MPC_RD-to-LP4_MPC_WR) RL+BL/2-WL+tURTW LPDDR5: X
20:13	RW	0x3a	tRP PRE-to-ACT delay or PRE-to-MRS delay time based on memory clk. LPDDR4(PRE-to-ACT): Refer to the Jedec spec about tRP.
12:6	RW	0x1e	tMRD LPDDR4: MRW-to-LP4_MPC_RD_CAL or MRS-to-MRS delay time based on memory clk. LPDDR5: MRW-to-CMD_LP5_RDC delay time based on memory clk. If you set this bit(tMRD), the each delay will be below value. Refer to the Jedec spec about tMRD range.
5:0	RW	0x00	Reserved0 Reserved

DDRPHY_SCHD_TIME_CON3

Address: Operational Base + offset (0x0A38)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved1 Reserved
7:4	RW	0x8	tBL_divn LPDDR4: X LPDDR5: BL/n
3:2	RW	0x0	Reserved0 Reserved
1:0	RW	0x0	Additional_WL Additional control of scheduler's write latency. It is for the write training. 2'b00: WL 2'b01: WL+1 2'b10: WL-1 2'b11: Reserved

DDRPHY_DVFS0_SCHD_TIME_CON0

Address: Operational Base + offset (0x0A3C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved
23:18	RW	0x16	dfs0_tMRW MRW-to-MRW delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRW.
17:14	RW	0x8	dfs0_tMRR MRR-to-MRR delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRR.
13:11	RW	0x0	Reserved0 Reserved

Bit	Attr	Reset Value	Description
10:6	RW	0x07	dfs0_phy_t_rddata_en dfi_rddata_en latency. It defines latency of generating dfi_rddata_en after RL(read latency from RD CMD). trddata_en is defined as (RL+phy_t_rddata_en)*memory clock. Note that RL+phy_t_rddata_en should be even number to meet dfi_rddata_en phase requirement. If the sum is odd number, increase phy_t_rddata_en by 1.
5:0	RW	0x12	dfs0_WL Write latency. It decide latency of generating dfi_wrdata_en after WL(Write Latency from WR CMD).

DDRPHY_DVFS0_SCHD_TIME_CON1

Address: Operational Base + offset (0x0A40)

Bit	Attr	Reset Value	Description
31:28	RW	0x6	dfs0_tNOP WR-to-NOP or NOP-to-WR delay time based on memory clk.
27:22	RW	0x10	dfs0_tWTR WRITE-to-READ or LP4_MPC_WR-to_LP4_MPC_RD delay time based on memory clk. Refer to the Jedec spec about tWTR. If you set this bit(tWTR), the each delay will be below value. LPDDR4: (Write-to-Read) WL+1+BL/2+tWTR, (LP4_MPC_WR-to-LP4_MPC_RD) WL+BL/2+tWTR+8 LPDDR5: (Write-to-Read) WL+tBL_divn+tWTR (LP5_WFF-to-LP5_WFF) WL+tBL_divn+tWTR
21:14	RW	0x34	dfs0_tRCD ACT-to-WRITE delay time based on memory clk. LPDDR4, LPDDR5: Refer to the Jedec spec about tRCD.
13:8	RW	0x10	dfs0_tRTP READ-to-PRE delay time based on memory clk. Refer to the Jedec spec about tRTP. If you set this bit(tRTP), the each delay wil be below value. LPDDR4: tRTP+BL/2-8 LPDDR5: X
7:0	RW	0x08	dfs0_tCCD LPDDR4: WRITE-to-WRITE or READ-to-READ or LP4_MPC_RD_DQ_CAL-to-LP4_MPC_RD_DQ_CAL delay time based on memory clk. LPDDR5: LP5_RDC-to-LP5_RDC delay time based on memory clk. Refer to the Jedec spec about tCCD range.

DDRPHY_DVFS0_SCHD_TIME_CON2

Address: Operational Base + offset (0x0A44)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved
30:27	RW	0x0	dfs0_tDES Default latency

Bit	Attr	Reset Value	Description
26:21	RW	0x1e	dfs0_tURTW User Read-to-Write or LP4_MPC_RD_FIFO-to-LP4_MPC_WR_FIFO delay time based on memory clk. Refer to the Jedec spec about delay of read to write or MPC READ FIFO to MPC WRITE FIFO. If you set this bit(tURTW), the each delay will be below value. LPDDR4: (Read-to-Write) RL+BL/2-WL+tURTW, (LP4_MPC_RD-to-LP4_MPC_WR) RL+BL/2-WL+tURTW LPDDR5: X
20:13	RW	0x3a	dfs0_tRP PRE-to-ACT delay or PRE-to-MRS delay time based on memory clk. LPDDR4(PRE-to-ACT): Refer to the Jedec spec about tRP.
12:6	RW	0x1e	dfs0_tMRD LPDDR4: MRW-to-LP4_MPC_RD_CAL or MRS-to-MRS delay time based on memory clk. LPDDR5: MRW-to-CMD_LP5_RDC delay time based on memory clk. If you set this bit(tMRD), the each delay will be below value. Refer to the Jedec spec about tMRD range.
5:0	RW	0x00	Reserved0 Reserved

DDRPHY_DVFS0_SCHD_TIME_CON3

Address: Operational Base + offset (0x0A48)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved
28:27	RW	0x0	dvfs0_Additional_WL Additional control of scheduler's write latency. It is for the write training. 2'b00: WL 2'b01: WL+1 2'b10: WL-1 2'b11: Reserved
26:23	RW	0x8	dvfs0_tBL_divn LPDDR4: X LPDDR5: BL/n
22:18	RW	0x00	Reserved1 Reserved
17	RW	0x0	dvfs0_periodic_en Periodic training enable
16	RW	0x0	dvfs0_periodic_zq_cnt_en Enable periodic ZQ calibration
15:14	RW	0x0	dvfs0_periodic_wrtrn_en Enable periodic write training mode. bit[0]: CS-0 enable bit[1]: CS-1 enable
13:12	RW	0x0	dvfs0_periodic_gttrn_en Enable periodic gate training mode. bit[0] : CS-0 enable bit[1] : CS-1 enable

Bit	Attr	Reset Value	Description
11:10	RW	0x0	dvfs0_dvfs_wrtrn_en Enable DVFS write training mode. bit[0]: CS-0 enable bit[1]: CS-1 enable
9:8	RW	0x0	dvfs0_dvfs_gttrn_en Enable DVFS gate traininig mode. bit[0]: CS-0 enable bit[1]: CS-1 enable
7:1	RW	0x00	Reserved0 Reserved
0	RW	0x1	dvfs0_CAS_EN LP5 WCK2CK SYNC command driven by phy scheduler. It needs to control to LP5 PHY training mode at DVFS0. dvfs0_cas_en should be enabled during wck2ck syns always on disable mode, dvfs0_cas_en should be disabled during wck2ck sync always on mode. 1'b1: Enable 1'b0: Disable

DDRPHY_DVFS1_SCHD_TIME_CON0

Address: Operational Base + offset (0x0A4C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved
23:18	RW	0x16	dfs1_tMRW MRW-to-MRW delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRW.
17:14	RW	0x8	dfs1_tMRR MRR-to-MRR delay time based on memory clk LPDDR4, LPDDR5: Refer to the Jedec spec about tMRR.
13:11	RW	0x0	Reserved0 Reserved
10:6	RW	0x07	dfs1_phy_t_rddata_en dfi_rddata_en latency. It defines latency of generating dfi_rddata_en after RL(read latency from RD CMD). trddata_en is defined as (RL+phy_t_rddata_en)*memory clock. Note that RL+phy_t_rddata_en should be even number to meet dfi_rddata_en phase requirement. If the sum is odd number, increase phy_t_rddata_en by 1.
5:0	RW	0x12	dfs1_WL Write latency. It decide latency of generating dfi_wrdata_en after WL(Write Latency from WR CMD).

DDRPHY_DVFS1_SCHD_TIME_CON1

Address: Operational Base + offset (0x0A50)

Bit	Attr	Reset Value	Description
31:28	RW	0x6	dfs1_tNOP WR-to-NOP or NOP-to-WR delay time based on memory clk.

Bit	Attr	Reset Value	Description
27:22	RW	0x10	dfs1_tWTR WRITE-to-READ or LP4_MPC_WR-to_LP4_MPC_RD delay time based on memory clk. Refer to the Jedec spec about tWTR. If you set this bit(tWTR), the each delay will be below value. LPDDR4 : (Write-to-Read) WL+1+BL/2+tWTR, (LP4_MPC_WR-to-LP4_MPC_RD) WL+BL/2+tWTR+8 LPDDR5 : (Write-to-Read) WL+tBL_divn+tWTR (LP5_WFF-to-LP5_WFF) WL+tBL_divn+tWTR
21:14	RW	0x34	dfs1_tRCD ACT-to-WRITE delay time based on memory clk. LPDDR4, LPDDR5: Refer to the Jedec spec about tRCD.
13:8	RW	0x10	dfs1_tRTP READ-to-PRE delay time based on memory clk. Refer to the Jedec spec about tRTP. If you set this bit(tRTP), the each delay wil be below value. LPDDR4: tRTP+BL/2-8 LPDDR5: X
7:0	RW	0x08	dfs1_tCCD LPDDR4: WRITE-to-WRITE or READ-to-READ or LP4_MPC_RD_DQ_CAL-to-LP4_MPC_RD_DQ_CAL delay time based on memory clk. LPDDR5: LP5_RDC-to-LP5_RDC delay time based on memory clk. Refer to the Jedec spec about tCCD range.

DDRPHY_DVFS1_SCHD_TIME_CON2

Address: Operational Base + offset (0x0A54)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved
30:27	RW	0x0	dfs1_tDES Default latency
26:21	RW	0x1e	dfs1_tURTW User Read-to-Write or LP4_MPC_RD_FIFO-to-LP4_MPC_WR_FIFO delay time based on memory clk. Refer to the Jedec spec about delay of read to write or MPC READ FIFO to MPC WRITE FIFO. If you set this bit(tURTW), the each delay will be below value. LPDDR4: (Read-to-Write) RL+BL/2-WL+tURTW, (LP4_MPC_RD-to-LP4_MPC_WR) RL+BL/2-WL+tURTW LPDDR5: X
20:13	RW	0x3a	dfs1_tRP PRE-to-ACT delay or PRE-to-MRS delay time based on memory clk. LPDDR4(PRE-to-ACT): Refer to the Jedec spec about tRP.
12:6	RW	0x1e	dfs1_tMRD LPDDR4: MRW-to-LP4_MPC_RD_CAL or MRS-to-MRS delay time based on memory clk. LPDDR5: MRW-to-CMD_LP5_RDC delay time based on memory clk. If you set this bit(tMRD), the each delay will be below value. Refer to the Jedec spec. about tMRD range.
5:0	RW	0x00	Reserved0 Reserved

DDRPHY_DVFS1_SCHD_TIME_CON3
Address: Operational Base + offset (0x0A58)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved
28:27	RW	0x0	dvfs1_Additional_WL Additional control of scheduler's write latency. It is for the write-training. 2'b00: WL 2'b01: WL+1 2'b10: WL-1 2'b11: Reserved
26:23	RW	0x8	dvfs1_tBL_divn LPDDR4: X LPDDR5: BL/n
22:18	RW	0x00	Reserved1 Reserved
17	RW	0x0	dvfs1_periodic_en Periodic training enable
16	RW	0x0	dvfs1_periodic_zq_cnt_en Enable periodic ZQ calibration
15:14	RW	0x0	dvfs1_periodic_wrtrn_en Enable periodic write training mode. bit[0] : CS-0 Enable bit[1] : CS-1 Enable
13:12	RW	0x0	dvfs1_periodic_gttrn_en Enable periodic gate training mode. bit[0]: CS-0 Enable bit[1]: CS-1 Enable
11:10	RW	0x0	dvfs1_dvfs_wrtrn_en Enable DVFS write training mode. bit[0]: CS-0 Enable bit[1]: CS-1 Enable
9:8	RW	0x0	dvfs1_dvfs_gttrn_en Enable DVFS gate traininig mode. bit[0]: CS-0 Enable bit[1]: CS-1 Enable
7:1	RW	0x00	Reserved0 Reserved
0	RW	0x1	dvfs1_CAS_EN LP5 WCK2CK SYNC command driven by phy scheduler. It needs to control to LP5 PHY training mode at DVFS1. dvfs1_cas_en should be enabled during wck2ck syns always on disable mode, dvfs1_cas_en should be disabled during wck2ck sync always on mode. 1'b1: Enable 1'b0: Disable

DDRPHY_SCHD_DIRECT_CMD0
Address: Operational Base + offset (0x0A5C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	DIRECT_EN_APB Direct command Enable, when scheduler_sw_mode is enabled. It should be disabled before generate direct comand again.

DDRPHY_SCHD_DIRECT_CMD1

Address: Operational Base + offset (0x0A60)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29:28	RW	0x0	DIRECT_CS_1 Control CS[1:0] for CMD-1 when DIRECT_EN_APB is enabled.
27:0	RW	0x0000000	DIRECT_CMD_1 Control ADD/CMD for CMD-1 when DIRECT_EN_APB is enabled. 1) LPDDR4 bit[5:0]: CMD-1 for CS high. bit[13:8]: CMD-1 for CS low

DDRPHY_SCHD_DIRECT_CMD2

Address: Operational Base + offset (0x0A64)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29:28	RW	0x0	DIRECT_CS_2 Control CS[1:0] for CMD-2 when DIRECT_EN_APB is enabled.
27:0	RW	0x0000000	DIRECT_CMD_2 Control ADD/CMD for CMD-2 when DIRECT_EN_APB is enabled. 1) LPDDR4 bit[5:0]: CMD-2 for CS high bit[13:8]: CMD-2 for CS low

DDRPHY_SCHD_DIRECT_CMD3

Address: Operational Base + offset (0x0A68)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved
23	RW	0x0	CMD_WCK_GEN_req_APB Generate WCK gen request, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
22	RW	0x0	CMD_DQS_GEN_req_APB Generate DQS gen request, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
21	RW	0x0	CMD_PRE_req_APB Generate PRECHARGE CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
20	RW	0x0	CMD_PREA_req_APB Generate PRECHARGE-ALL CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
19	RW	0x0	CMD_REF_req_APB Generate REFRESH CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
18	RW	0x0	CMD_SRE_req_APB Generate SELF REFRESH ENTER CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.

Bit	Attr	Reset Value	Description
17	RW	0x0	CMD_SRX_req_APB Generate SELF REFRESH EXIT CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
16	RW	0x0	CMD_ACT_req_APB Generate ACTIVE CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
15	RW	0x0	CMD_WR_req_APB Generate WRITE CMD, when scheduler_sw_mode is enabled. It also generate dfi_wrdata_en. The CMD/ADDR is defined by SCHEDULER_CON4~6.
14	RW	0x0	CMD_MWR_req_APB Generate Masked WRITE CMD, when scheduler_sw_mode is enabled. It also generate dfi_wrdata_en. The CMD/ADDR is defined by SCHEDULER_CON4~6.
13	RW	0x0	CMD_RD_req_APB Generate READ CMD, when scheduler_sw_mode is enabled. It also generate dfi_rddata_en after t_rddata_en. The CMD/ADDR is defined by SCHEDULER_CON4~6.
12	RW	0x0	CMD_MRW_req_APB Generate MRW CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
11	RW	0x0	CMD_MRR_req_APB Generate MRR CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
10	RW	0x0	LP4_MPC_RD_FIFO_req_APB Generate MPC_RD_FIFO CMD for LPDDR4, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
9	RW	0x0	LP4_MPC_RD_DQ_CAL_req_APB Generate MPC_RD_DQ_CAL CMD for LPDDR4, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
8	RW	0x0	LP4_MPC_WR_FIFO_req_APB Generate MPC_WR_FIFO CMD for LPDDR4, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
7:4	RW	0x0	Reserved2 Reserved
3	RW	0x0	CMD_CKE_LOW_req_APB Control CKE to low, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6. It is for the LPDDR4.
2	RW	0x0	CMD_CKE_HIGH_req_APB Control CKE to high, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6. It is for the LPDDR4.
1	RW	0x0	CMD_NOP_req_APB Generate NOP CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHEDULER_CON4~6.
0	RW	0x0	Reserved1 Reserved

DDRPHY_SCHD_DIRECT_CMD4
Address: Operational Base + offset (0x0A6C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved
11	RW	0x0	CMD_CAS_LP5_req_APB Generages CAS CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
10	RW	0x0	CMD_LP5_PDE_req_APB Generages PDE CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
9	RW	0x0	CMD_LP5_PDX_req_APB Generages PDX CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
8	RW	0x0	CMD_LP5_WFF_req_APB Generages WFF CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
7	RW	0x0	CMD_LP5_RFF_req_APB Generages RFF CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
6	RW	0x0	CMD_LP5_RDC_req_APB Generages RDC CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
5	RW	0x0	CMD_LP5_MPC_START_WCK2DQI_req_APB Generages MPC START WCK2DQI CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
4	RW	0x0	CMD_LP5_MPC_STOP_WCK2DQI_req_APB Generages MPC STOP WCK2DQI CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
3	RW	0x0	CMD_LP5_MPC_START_WCK2DQO_req_APB Generages MPC START WCK2DQO CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
2	RW	0x0	CMD_LP5_MPC_STOP_WCK2DQO_req_APB Generages MPC STOP WCK2DQO CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.
1	RW	0x0	CMD_LP5_MPC_START_ZQ_req_APB Generages MPC START ZQ CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.

Bit	Attr	Reset Value	Description
0	RW	0x0	CMD_LP5_MPC_STOP_ZQ_req_APB Generages MPC STOP ZQ CMD, when scheduler_sw_mode is enabled. The CMD/ADDR is defined by SCHD_CMD_CON0. It is for the LPDDR5.

DDRPHY_SCHD_CMD_CON0

Address: Operational Base + offset (0x0A70)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved1 Reserved
28	RW	0x0	AB_EN_APB Sets MEMORY All Bank for CMD/ADDR
27	RW	0x0	AP_EN_APB Sets MEMORY Auto Precharge for CMD/ADDR
26	RW	0x0	BL_EN_APB Sets MEMORY Burst Length for CMD/ADDR
25:22	RW	0x0	RANK_SEL_APB Sets MEMORY Rank Selection for CMD/ADDR
21:20	RW	0x0	BK_ORG_APB Controls Bank mode selection for LPDDR5 BK_ORG = 2'b10: 16bank BK_ORG = 2'b01: 8bank BK_ORG = 2'b00: 4bank 4BG
19	RW	0x0	PD_EN_APB Sets MEMORY Power Down for SRE
18	RW	0x0	DSM_EN_APB Sets MEMORY Deep Sleep Mode for SRE
17	RW	0x0	Reserved0 Reserved
16	RW	0x0	WRX_APB Sets MEMORY Write X function for CMD/ADDR
15:12	RW	0x0	DC_CODE_APB Sets MEMORY Data Copy function for CMD/ADDR
11	RW	0x0	WS_FAST_APB Sets MEMORY WS_FS for CAS
10	RW	0x0	WS_RD_APB Sets MEMORY WS_RD for CAS
9	RW	0x0	WS_WR_APB Sets MEMORY WS_WR for CAS
8	RW	0x0	EDC_EN_APB Sets MEMORY EDC for CAS
7:3	RW	0x00	B_CODE_APB Sets MEMORY Bank Address for CMD/ADDR
2:1	RW	0x0	BG_CODE_APB Sets MEMORY Bank Group Address for CMD/ADDR
0	RW	0x1	CAS_EN_APB LP5 WCK2CK SYNC command driven by phy scheduler. It needs to control to LP5 PHY training mode. CAS_EN should be enabled during wck2ck syns always on disable mode, CAS_EN should be disabled during wck2ck sync always on mode. 1'b1: Enable 1'b0: Disable

DDRPHY_SCHD_CMD_CON1

Address: Operational Base + offset (0x0A74)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29:18	RW	0x000	COL_CODE_APB Sets MEMORY COL ADDRESS for CMD/ADDR
17:0	RW	0x00000	ROW_CODE_APB Sets MEMORY ROW ADDRESS for CMD/ADDR

DDRPHY_SCHD_CMD_CON2

Address: Operational Base + offset (0x0A78)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29:12	RW	0x00000	OP_CODE_APB Sets MEMORY OPCODE for MRW
11:4	RW	0x00	MA_CODE_APB Sets MEMORY MACODE for MRW and MRR
3:0	RW	0x0	BA_CODE_APB Sets MEMORY BACODE for CMD/ADDR

DDRPHY_OP_CODE_RDC

Address: Operational Base + offset (0x0A7C)

Bit	Attr	Reset Value	Description
31:24	RW	0x55	OP_CODE_PATB This field register set MEMORY OPCODE for read DQ calibration (Pattern B LP4 : MR40 LP5 : MR33)
23:16	RW	0x55	OP_CODE_PATA This field register set MEMORY OPCODE for read DQ calibration (Pattern A LP4 : MR32 LP5 : MR32)
15:8	RW	0xee	OP_CODE_INVB This field register set MEMORY OPCODE for read DQ calibration (Upper byte invert LP4 : MR20 LP5 : MR32)
7:0	RW	0xee	OP_CODE_INVA This field register set MEMORY OPCODE for read DQ calibration (Lowe byte invert LP4 : MR15 LP5 : MR31)

DDRPHY_LP4_MR_OP0

Address: Operational Base + offset (0x0A80)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LP4_MR12_OP It is MR12 register infromation for LPDDR4. It will be used for CBT on PHY initiated training. bit[5:0]= MR12 OP[5:0] (Vref CA) bit[6]= MR12 OP[6] (VR-CA)
23:16	RW	0x00	LP4_MR11_OP It is MR11 register infromation for LPDDR4. It will be used for CBT on PHY initiated training. bit[2:0]= MR11 OP[2:0] (DQ ODT) bit[6:4]= MR11 OP[6:4] (CA ODT)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	LP4_MR2_OP It is MR2 register infromation for LPDDR4. It will be used for write leveling on PHY initiated training. bit[2:0]= MR2 OP[2:0] (RL) bit[5:3]= MR2 OP[5:3] (WL) bit[6]= MR2 OP[6] (WLS) bit[7]= MR2 OP[7] (WR LEV)
7:0	RW	0x00	LP4_MR1_OP It is MR1 register infromation for LPDDR4. It will be used for write leveling on PHY initiated training. [1:0]= MR1 OP[1:0] (BL) [2]= MR1 OP[2] (WR-PRE) [3]= MR1 OP[3] (RD-PRE) [6:4]= MR1 OP[6:4] (nWR) [7]= MR1 OP[7] (RPST)

DDRPHY_LP4_MR_OP1

Address: Operational Base + offset (0x0A84)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	Reserved0 Reserved
7:0	RW	0x00	LP4_MR13_OP It is MR13 register infromation for LPDDR4. It will be used for CBT and gate training on PHY initiated training. bit[0]= MR13 OP[0] (CBT) bit[1]= MR13 OP[1] (RPT) bit[2]= MR13 OP[2] (VRO) bit[3]= MR13 OP[3] (VRCG) bit[4]= MR13 OP[4] (RRO) bit[5]= MR13 OP[5] (DMD) bit[6]= MR13 OP[6] (FSP-WR) bit[7]= MR13 OP[7] (FSP-OP)

DDRPHY_LP5_MR_OP0

Address: Operational Base + offset (0x0A88)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	LP5_MR16_OP It is MR16 register infromation for LPDDR5. It will be used for CBT on PHY initiated training. bit[1:0] = MR16 OP[1:0] (FSP-WR) bit[3:2] = MR16 OP[3:2] (FSP-OP) bit[5:4] = MR16 OP[5:4] (CBT) bit[6] = MR16 OP[6] (VRCG) bit[7] = MR16 OP[7] (CBT-PH)
23:16	RW	0x00	LP5_MR12_OP It is MR12 register infromation for LPDDR5. It will be used for CBT on PHY initiated training. bit[6:0]= MR12 OP[6:0] (Vref CA) bit[7]= MR12 OP[7] (VBS)
15:8	RW	0x00	LP5_MR11_OP It is MR11 register infromation for LPDDR5. It will be used for CBT on PHY initiated training. bit[2:0] = MR11 OP[2:0] (DQ ODT) bit[6:4] = MR11 OP[6:4] (CA ODT)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	LP5_MR10_OP It is MR10 register infromation for LPDDR5. bit[3:2]= MR10 OP[3:2] (WCK PST) bit[5:4]= MR10 OP[5:4] (RDQS PRE) bit[7:6]= MR10 OP[7:6] (RDQS PST)

DDRPHY_LP5_MR_OP1

Address: Operational Base + offset (0x0A8C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved0 Reserved
15:8	RW	0x00	LP5_MR18_OP It is MR18 register infromation for LPDDR5. It will be used for WCK2CK leveling on PHY initiated training. bit[2:0]= MR30 OP[2:0] (WCK Termination) bit[3]= MR30 OP[3] (Reserved) bit[4]= MR30 OP[4] (WCK ON) bit[5]= MR30 OP[5] (WCK SYNC) bit[6]= MR30 OP[6] (WCK2CK Leveling) bit[7]= MR30 OP[7] (CKR)
7:0	RW	0x00	LP5_MR17_OP It is MR17 register infromation for LPDDR5. It will be used for CBT on PHY initiated training. bit[2:0]= MR17 OP[2:0] (SoC ODT) bit[3]= MR17 OP[3] (ODRD-CK) bit[4]= MR17 OP[4] (ODTD-CS) bit[5]= MR17 OP[5] (ODTD-CA) bit[6]= MR17 OP[6] (X8 ODTD Lower) bit[7]= MR17 OP[7] (X8 ODTD Upper)

DDRPHY_SCHD_FSM

Address: Operational Base + offset (0x0A90)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved0 Reserved
21	RO	0x0	dvfs_fail_status FSM monitoring signal. It shows failure of phymstr in dfs training fsm.
20	RO	0x0	periodic_fail_status FSM monitoring signal. It shows failure of phymstr in periodic training fsm.
19:16	RO	0x0	schd_train_fsm FSM monitoring signal. It shows training FSM status in all training.
15:13	RO	0x0	schd_rank_fsm FSM monitoring signal. It shows rank FSM status in per rank training.
12:9	RO	0x0	schd_periodic_fsm FSM monitoring signal. It shows periodic training start FSM status.
8:5	RO	0x0	schd_dvfs_trn_fsm FSM monitoring signal. It shows DFS training FSM status in dfs training.

Bit	Attr	Reset Value	Description
4:0	RO	0x00	schd_periodic_trn_fsm FSM monitoring signal. It shows periodic training FSM status in enabled periodic training.

DDRPHY_CLKMODE_CON

Address: Operational Base + offset (0x0A94)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved
4	RW	0x0	ctrl_phy_dll_2x 1'b1: PHY DLL 2x clock(=WCK) 1'b0: PHY DLL 1x clock(=WCK/2) Use only MODE4 and under 3200Mbps
3	RW	0x1	ctrl_phy_clk_2x 1'b1: PHY 2x clock 1'b0: PHY 1x clock
2:0	RW	0x1	ctrl_phy_mode Clock ratio mode between MC and PHY for LP4/5 combo. 3'b000: LP4 mode DFI clock ratio MC : CK : DQS = 1:4:4(TBD) 3'b001: LP4 mode DFI clock ratio MC : CK : DQS = 1:2:2 3'b010: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 1:1:2 3'b011: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 2:1:4 3'b100: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 1:1:4

DDRPHY_CASWIZZLE_CON

Address: Operational Base + offset (0x0A98)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:28	RW	0x6	ext_dfi_address_p6 Internal dfi_address bit position for external dfi_address[6] This field specifies a connection between the SOC CA[6] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[6] connection in package will be swapped in the following way. SOC CA[6] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
27	RW	0x0	Reserved1 Reserved
26:24	RW	0x5	ext_dfi_address_p5 Internal dfi_address bit position for external dfi_address[5] This field specifies a connection between the SOC CA[5] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[5] connection in package will be swapped in the following way. SOC CA[5] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
23	RW	0x0	Reserved2 Reserved

Bit	Attr	Reset Value	Description
22:20	RW	0x4	ext_dfi_address_p4 Internal dfi_address bit position for external dfi_address[4] This field specifies a connection between the SOC CA[4] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[4] connection in package will be swapped in the following way. SOC CA[4] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
19	RW	0x0	Reserved3 Reserved
18:16	RW	0x3	ext_dfi_address_p3 Internal dfi_address bit position for external dfi_address[3] This field specifies a connection between the SOC CA[3] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[3] connection in package will be swapped in the following way. SOC CA[3] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
15	RW	0x0	Reserved4 Reserved
14:12	RW	0x2	ext_dfi_address_p2 Internal dfi_address bit position for external dfi_address[2] This field specifies a connection between the SOC CA[2] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[2] connection in package will be swapped in the following way. SOC CA[2] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
11	RW	0x0	Reserved5 Reserved
10:8	RW	0x1	ext_dfi_address_p1 Internal dfi_address bit position for external dfi_address[1] This field specifies a connection between the SOC CA[1] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[1] connection in package will be swapped in the following way. SOC CA[1] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
7	RW	0x0	Reserved6 Reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	ext_dfi_addressH_p0 Internal dfi_address bit position for external dfi_addressH[0] for LPDDR5 This field specifies a connection between the SOC CA[0] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[0] connection in package will be swapped in the following way. SOC CA[0] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.
3	RW	0x0	Reserved7 Reserved
2:0	RW	0x0	ext_dfi_address_p0 Internal dfi_address bit position for external dfi_address[0] This field specifies a connection between the SOC CA[0] and a bit of DRAM CA[6:0]. When this field set to 3'd0, CA[0] connection in package will be swapped in the following way. SOC CA[0] - DRAM CA[0] The memory controller must swap dfi_address_pN[6:0] and drive it to PHY in order to cancel out the swapped CA connection in the package. For PHY training interface, PHY will generate and swap dfi_address_pN[6:0] according to this field.

DDRPHY_TDLL_CON0

Address: Operational Base + offset (0x0A9C)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved
18	RW	0x0	wrdqtracken For debug purpose
17	RW	0x0	rdparityen For debug purpose
16	RW	0x0	slidingwindowen For debug purpose
15	RW	0x0	SLWUpEn For debug purpose
14	RW	0x0	sfr_tdll_auto For debug purpose
13	RW	0x0	sfr_tdll_dury For debug purpose
12	RW	0x0	sfr_tdll_acc For debug purpose
11	RW	0x0	sfr_tdll_resync For debug purpose
10	RW	0x0	sfr_tdll_start For debug purpose
9	RW	0x0	sfr_wDLL_en For debug purpose
8:7	RW	0x0	sfr_wDLL_sens For debug purpose
6	RW	0x0	ctrl_average For debug purpose
5	RW	0x0	ctrl_set_ref For debug purpose

Bit	Attr	Reset Value	Description
4	RW	0x0	sfr_dll_fine_track For debug purpose
3:2	RW	0x0	sfr_read_parity_mask For debug purpose
1:0	RW	0x0	sfr_tdll_en For debug purpose

DDRPHY_TDLL_CON1

Address: Operational Base + offset (0x0AA0)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved
24:16	RW	0x000	ctrl_tdll_enc For debug purpose
15:8	RW	0x00	Reserved1 Reserved
7:0	RW	0x00	sfr_tdll_offset For debug purpose

DDRPHY_TDLL_MON0_DS0

Address: Operational Base + offset (0x0AA4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:16	RO	0x0000	SELtCH_DS0 For debug purpose
15:14	RO	0x0	Reserved1 Reserved
13:0	RO	0x0000	SELtCHL_DS0 For debug purpose

DDRPHY_TDLL_MON1_DS0

Address: Operational Base + offset (0x0AA8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved0 Reserved
21:16	RO	0x00	CNTtCH_DS0 For debug purpose
15:6	RO	0x000	Reserved1 Reserved
5:0	RO	0x00	CNTtCHL_DS0 For debug purpose

DDRPHY_TDLL_MON0_DS1

Address: Operational Base + offset (0x0AAC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:16	RO	0x0000	SELtCH_DS1 For debug purpose
15:14	RO	0x0	Reserved1 Reserved
13:0	RO	0x0000	SELtCHL_DS1 For debug purpose

DDRPHY_TDLL_MON1_DS1
Address: Operational Base + offset (0x0AB0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved0 Reserved
21:16	RO	0x00	CNTtCH_DS1 For debug purpose
15:6	RO	0x000	Reserved1 Reserved
5:0	RO	0x00	CNTtCHL_DS1 For debug purpose

DDRPHY_DQRPARITY_LEFT_DS0
Address: Operational Base + offset (0x0AB4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQRPARITY_LEFT_DS0 For debug purpose

DDRPHY_DQRPARITY_RIGHT_DS0
Address: Operational Base + offset (0x0AB8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQRPARITY_RIGHT_DS0 For debug purpose

DDRPHY_DQFPARITY_LEFT_DS0
Address: Operational Base + offset (0x0ABC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQFPARITY_LEFT_DS0 For debug purpose

DDRPHY_DQFPARITY_RIGHT_DS0
Address: Operational Base + offset (0x0AC0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQFPARITY_RIGHT_DS0 For debug purpose

DDRPHY_DQRPARITY_LEFT_DS1
Address: Operational Base + offset (0x0AC4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQRPARITY_LEFT_DS1 For debug purpose

DDRPHY_DQRPARITY_RIGHT_DS1
Address: Operational Base + offset (0x0AC8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQRPARITY_RIGHT_DS1 For debug purpose

DDRPHY_DQFPARITY_LEFT_DS1

Address: Operational Base + offset (0x0ACC)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQFPARITY_LEFT_DS1 For debug purpose

DDRPHY_DQFPARITY_RIGHT_DS1

Address: Operational Base + offset (0x0AD0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	Reserved0 Reserved
26:0	RO	0x0000000	MON_DQFPARITY_RIGHT_DS1 For debug purpose

DDRPHY_READCAL_URG_DS0

Address: Operational Base + offset (0x0AD4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved0 Reserved
24:16	RO	0x000	ctrl_read_cal_urg_DS0 For debug purpose
15:9	RO	0x00	Reserved1 Reserved
8:0	RO	0x000	ctrl_read_cal_req_DS0 For debug purpose

DDRPHY_READCAL_URG_DS1

Address: Operational Base + offset (0x0AD8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved0 Reserved
24:16	RO	0x000	ctrl_read_cal_urg_DS1 For debug purpose
15:9	RO	0x00	Reserved1 Reserved
8:0	RO	0x000	ctrl_read_cal_req_DS1 For debug purpose

DDRPHY_WCK2CKSYNC_CON0

Address: Operational Base + offset (0x0ADC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
3:2	RW	0x0	ctrl_wck_out_enable_APB I/O OEN control for WCK highz or low generation in IDLE. 1'b1: Low 1'b0: Highz [2]: Control for DS1 [1]: Control for DS0
1:0	RW	0x0	ctrl_WCK_MODE_APB WCK driving policy 2'b00: WCK is driven by PHY at PHY Training with scheduler or wck is driven by MC at Normal operation and CAS_EN should be 1 at this mode. 2'b01: WCK always be driven by MC, this mode use only WCK always on mode and CAS_EN should be 0 at this mode. 2'b10: WCK always be driven by PHY, this field is debug purpose. It needs to require MC CAS command related to WCK2CK(not support WS_FS) and CAS_EN should be 1 at this mode. 2'b11: Reserved

DDRPHY_WCK2CKSYNC_CON1

Address: Operational Base + offset (0x0AE0)

Bit	Attr	Reset Value	Description
31:28	RW	0x2	ctrl_wck_adj WCK start point for write opearation If CK:WCK=1:4, set to twckpre_toggle_WR/4 If CK:WCK=1:2, set to twckpre_toggle_WR/2 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
27	RW	0x0	Reserved0 Reserved
26:24	RW	0x3	ctrl_wck2ck_static WCK static preamble If CK:WCK=1:4, set to tWCKPRE_Static If CK:WCK=1:2, set to tWCKPRE_Static Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
23:16	RW	0x34	ctrl_wckdur_adj WCK duration for write opearation If CK:WCK=1:4, set to (WL+4)*4twck If CK:WCK=1:2, set to (WL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
15:13	RW	0x0	Reserved1 Reserved
12:8	RW	0x07	ctrl_rwck_adj WCK start point for read opearation (set to twckpre_toggle_RD/4) Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
7:0	RW	0x58	ctrl_rwckdur_adj WCK duration for read opearation If CK:WCK=1:4, set to (RL+4)*4twck If CK:WCK=1:2, set to (RL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.

DDRPHY_DVFS0_WCK2CKSYNC_CON1

Address: Operational Base + offset (0x0AE4)

Bit	Attr	Reset Value	Description
31:28	RW	0x2	dvfs0_wck_adj WCK start point for write opearation If CK:WCK=1:4, set to twckpre_toggle_WR/4 If CK:WCK=1:2, set to twckpre_toggle_WR/2 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
27	RW	0x0	Reserved0 Reserved
26:24	RW	0x3	dvfs0_wck2ck_static WCK static preamble If CK:WCK=1:4, set to tWCKPRE_Static If CK:WCK=1:2, set to tWCKPRE_Static Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
23:16	RW	0x34	dvfs0_wckdur_adj WCK duration for write opearation If CK:WCK=1:4, set to (WL+4)*4twck If CK:WCK=1:2, set to (WL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
15:13	RW	0x0	Reserved1 Reserved
12:8	RW	0x07	dvfs0_rwck_adj WCK start point for read opearation (set to twckpre_toggle_RD/4) Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
7:0	RW	0x58	dvfs0_rwckdur_adj WCK duration for read opearation If CK:WCK=1:4, set to (RL+4)*4twck If CK:WCK=1:2, set to (RL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.

DDRPHY_DVFS1_WCK2CKSYNC_CON1

Address: Operational Base + offset (0x0AE8)

Bit	Attr	Reset Value	Description
31:28	RW	0x2	dvfs1_wck_adj WCK start point for write opearation If CK:WCK=1:4, set to twckpre_toggle_WR/4 If CK:WCK=1:2, set to twckpre_toggle_WR/2 Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
27	RW	0x0	Reserved0 Reserved
26:24	RW	0x3	dvfs1_wck2ck_static wck static preamble if CK:WCK = 1:4, set to tWCKPRE_Static if CK:WCK = 1:2, set to tWCKPRE_Static Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.

Bit	Attr	Reset Value	Description
23:16	RW	0x34	dvfs1_wckdur_adj WCK duration for write opearation If CK:WCK=1:4, set to (WL+4)*4twck If CK:WCK=1:2, set to (WL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
15:13	RW	0x0	Reserved1 Reserved
12:8	RW	0x07	dvfs1_rwck_adj WCK start point for read opearation (set to twckpre_toggle_RD/4) Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.
7:0	RW	0x58	dvfs1_rwckdur_adj WCK duration for read opearation If CK:WCK=1:4, set to (RL+4)*4twck If CK:WCK=1:2, set to (RL+8)*2twck Please refer to "LPDDR5 WCK2CK sync parameter" reference guide on PHY Datasheet.

DDRPHY_SCHD_CMD_GATING0

Address: Operational Base + offset (0x0AEC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved
23	RW	0x0	gating_CMD_WCK_GEN_req Blocks WCK gen request, when scheduler_sw_mode is enabled.
22	RW	0x0	gating_CMD_DQS_GEN_req Blocks DQS gen request, when scheduler_sw_mode is enabled.
21	RW	0x0	gating_CMD_DIRECT_req Blocks DIRECT request, when scheduler_sw_mode is enabled.
20	RW	0x0	gating_CMD_PRE_req Blocks PRECHARGE CMD, when scheduler_sw_mode is enabled.
19	RW	0x0	gating_CMD_PREA_req Blocks PRECHARGE-ALL CMD, when scheduler_sw_mode is enabled.
18	RW	0x0	gating_CMD_REF_req Blocks REFRESH CMD, when scheduler_sw_mode is enabled.
17	RW	0x0	gating_CMD_SRE_req Blocks SELF REFRESH ENTER CMD, when scheduler_sw_mode is enabled.
16	RW	0x0	gating_CMD_SRX_req Blocks SELF REFRESH EXIT CMD, when scheduler_sw_mode is enabled.
15	RW	0x0	gating_CMD_ACT_req Blocks ACTIVE CMD, when scheduler_sw_mode is enabled.
14	RW	0x0	gating_CMD_WR_req Blocks WRITE CMD, when scheduler_sw_mode is enabled.
13	RW	0x0	gating_CMD_MWR_req Blocks Masked WRITE CMD, when scheduler_sw_mode is enabled.
12	RW	0x0	gating_CMD_RD_req Blocks READ CMD, when scheduler_sw_mode is enabled.
11	RW	0x0	gating_CMD_MRW_req Blocks MRW CMD, when scheduler_sw_mode is enabled.

Bit	Attr	Reset Value	Description
10	RW	0x0	gating_CMD_MRR_req Blocks MRR CMD, when scheduler_sw_mode is enabled.
9	RW	0x0	gating_LP4_MPC_RD_FIFO_req Blocks MPC_RD_FIFO CMD for LPDDR4, when scheduler_sw_mode is enabled.
8	RW	0x0	gating_LP4_MPC_RD_DQ_CAL_req Blocks MPC_RD_DQ_CAL CMD for LPDDR4, when scheduler_sw_mode is enabled.
7	RW	0x0	gating_LP4_MPC_WR_FIFO_req Blocks MPC_WR_FIFO CMD for LPDDR4, when scheduler_sw_mode is enabled.
6	RW	0x0	gating_LP4_MPC_DQS_OSC_START_req Blocks MPC_MPC_DQ_OSC START CMD for LPDDR4, when scheduler_sw_mode is enabled.
5	RW	0x0	gating_LP4_MPC_DQS_OSC_STOP_req Blocks MPC_MPC_DQ_OSC STOP CMD for LPDDR4, when scheduler_sw_mode is enabled.
4	RW	0x0	gating_LP4_MPC_ZQCAL_START_req Blocks MPC_MPC_ZQCAL START CMD for LPDDR4, when scheduler_sw_mode is enabled.
3	RW	0x0	gating_LP4_MPC_ZQCAL_LATCH_req Blocks MPC_MPC_ZQCAL LATCH CMD for LPDDR4, when scheduler_sw_mode is enabled.
2	RW	0x0	gating_CMD_CKE_LOW_req Blocks CKE to low, when scheduler_sw_mode is enabled.
1	RW	0x0	gating_CMD_CKE_HIGH_req Blocks CKE to high, when scheduler_sw_mode is enabled.
0	RW	0x0	gating_CMD_NOP_req Blocks NOP CMD, when scheduler_sw_mode is enabled.

DDRPHY_SCHD_CMD_GATING1

Address: Operational Base + offset (0x0AF0)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved
11	RW	0x0	gating_CMD_CAS_LP5_req Blocks CAS CMD for LPDDR5, when scheduler_sw_mode is enabled.
10	RW	0x0	gating_CMD_LP5_PDE_req Blocks PDE CMD for LPDDR5, when scheduler_sw_mode is enabled.
9	RW	0x0	gating_CMD_LP5_PDX_req_APB Blocks PDX CMD for LPDDR5, when scheduler_sw_mode is enabled.
8	RW	0x0	gating_CMD_LP5_WFF_req_APB Blocks WFF CMD for LPDDR5, when scheduler_sw_mode is enabled.
7	RW	0x0	gating_CMD_LP5_RFF_req_APB Blocks RFF CMD for LPDDR5, when scheduler_sw_mode is enabled.
6	RW	0x0	gating_CMD_LP5_RDC_req_APB Blocks RDC CMD for LPDDR5, when scheduler_sw_mode is enabled.

Bit	Attr	Reset Value	Description
5	RW	0x0	gating_CMD_LP5_MPC_START_WCK2DQI_req_APB Blocks MPC START WCK2DQI CMD for LPDDR5, when scheduler_sw_mode is enabled.
4	RW	0x0	gating_CMD_LP5_MPC_STOP_WCK2DQI_req_APB Blocks MPC STOP WCK2DQI CMD for LPDDR5, when scheduler_sw_mode is enabled.
3	RW	0x0	gating_CMD_LP5_MPC_START_WCK2DQO_req_APB Blocks MPC START WCK2DQO CMD for LPDDR5, when scheduler_sw_mode is enabled.
2	RW	0x0	gating_CMD_LP5_MPC_STOP_WCK2DQO_req_APB Blocks MPC STOP WCK2DQO CMD for LPDDR5, when scheduler_sw_mode is enabled.
1	RW	0x0	gating_CMD_LP5_MPC_START_ZQ_req_APB Blocks MPC START ZQ CMD for LPDDR5, when scheduler_sw_mode is enabled.
0	RW	0x0	gating_CMD_LP5_MPC_STOP_ZQ_req_APB Blocks MPC STOP ZQ CMD for LPDDR5, when scheduler_sw_mode is enabled.

DDRPHY_DVFS0_WCK2CKSYNC_CON0

Address: Operational Base + offset (0x0AF4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved
3:2	RW	0x0	dvfs0_wck_out_enable_APB I/O OEN control for WCK highz or low generation in IDLE at DVFS0. 1'b1: Low 1'b0: Highz [2]: Control for DS1 [1]: Control for DS0
1:0	RW	0x0	dvfs0_WCK_MODE_APB WCK driving policy at DVFS0 2'b00: WCK is driven by PHY at PHY training with scheduler or WCK is driven by MC at normal operation and dvfs0_CAS_EN should be 1 at this mode. 2'b01: WCK always be driven by MC, this mode use only WCK always on mode and dvfs0_CAS_EN should be 0 at this mode. 2'b10: WCK always be driven by PHY, this field is debug purpose. It needs to require MC CAS command related to WCK2CK (not support WS_FS) and dvfs0_CAS_EN should be 1 at this mode. 2'b11: Reserved

DDRPHY_DVFS1_WCK2CKSYNC_CON0

Address: Operational Base + offset (0x0AF8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved
3:2	RW	0x0	dvfs1_wck_out_enable_APB I/O OEN control for WCK highz or low generation in IDLE at DVFS1. 1'b1: Low 1'b0: Highz [2]: Control for DS1 [1]: Control for DS0

Bit	Attr	Reset Value	Description
1:0	RW	0x0	dvfs1_WCK_MODE_APB WCK driving policy at DVFS1 2'b00: WCK is driven by PHY at PHY training with scheduler or WCK is driven by MC at normal operation and dvfs1_CAS_EN should be 1 at this mode. 2'b01: WCK always be driven by MC, this mode use only WCK always on mode and dvfs1_CAS_EN should be 0 at this mode. 2'b10: WCK always be driven by PHY, this field is debug purpose. It needs to require MC CAS command related to WCK2CK (not support WS_FS) and dvfs1_CAS_EN should be 1 at this mode. 2'b11: Reserved

DDRPHY_MDLL_CON2
Address: Operational Base + offset (0x0AFC)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved0 Reserved
10:0	RW	0x001	SW_ctrl_lock_value_init SW ctrl_lock_value cotrolled by lock_override_APB

DDRPHY_TESTILP5_DQ0
Address: Operational Base + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ0 TEST input port for DQ0 I/O

DDRPHY_TESTILP5_DQ1
Address: Operational Base + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ1 TEST input port for DQ1 I/O

DDRPHY_TESTILP5_DQ2
Address: Operational Base + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ2 TEST input port for DQ2 I/O

DDRPHY_TESTILP5_DQ3
Address: Operational Base + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ3 TEST input port for DQ3 I/O

DDRPHY_TESTILP5_DQ4
Address: Operational Base + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ4 TEST input port for DQ4 I/O

DDRPHY_TESTILP5_DQ5

Address: Operational Base + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ5 TEST input port for DQ5 I/O

DDRPHY_TESTILP5_DQ6

Address: Operational Base + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ6 TEST input port for DQ6 I/O

DDRPHY_TESTILP5_DQ7

Address: Operational Base + offset (0x0B1C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ7 TEST input port for DQ7 I/O

DDRPHY_TESTILP5_DQ8

Address: Operational Base + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ8 TEST input port for DQ8 I/O

DDRPHY_TESTILP5_DQ9

Address: Operational Base + offset (0x0B24)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ9 TEST input port for DQ9 I/O

DDRPHY_TESTILP5_DQ10

Address: Operational Base + offset (0x0B28)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ10 TEST input port for DQ10 I/O

DDRPHY_TESTILP5_DQ11

Address: Operational Base + offset (0x0B2C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ11 TEST input port for DQ11 I/O

DDRPHY_TESTILP5_DQ12

Address: Operational Base + offset (0x0B30)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ12 TEST input port for DQ12 I/O

DDRPHY_TESTILP5_DQ13

Address: Operational Base + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ13 TEST input port for DQ13 I/O

DDRPHY_TESTILP5_DQ14

Address: Operational Base + offset (0x0B38)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ14 TEST input port for DQ14 I/O

DDRPHY_TESTILP5_DQ15

Address: Operational Base + offset (0x0B3C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQ15 TEST input port for DQ15 I/O

DDRPHY_TESTILP5_DM0

Address: Operational Base + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DM0 TEST input port for DM0 I/O

DDRPHY_TESTILP5_DM1

Address: Operational Base + offset (0x0B44)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DM1 TEST input port for DM1 I/O

DDRPHY_TESTILP5_DQS0
Address: Operational Base + offset (0x0B48)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQS0 TEST input port for DQS0 I/O

DDRPHY_TESTILP5_DQS1
Address: Operational Base + offset (0x0B4C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_DQS1 TEST input port for DQS1 I/O

DDRPHY_TESTILP5_CK
Address: Operational Base + offset (0x0B50)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CK TEST input port for CK I/O

DDRPHY_TESTILP5_CA0
Address: Operational Base + offset (0x0B54)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CA0 TEST input port for CA0 I/O

DDRPHY_TESTILP5_CA1
Address: Operational Base + offset (0x0B58)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CA1 TEST input port for CA1 I/O

DDRPHY_TESTILP5_CA2
Address: Operational Base + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CA2 TEST input port for CA2 I/O

DDRPHY_TESTILP5_CA3
Address: Operational Base + offset (0x0B60)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CA3 TEST input port for CA3 I/O

DDRPHY_TESTILP5_CA4
Address: Operational Base + offset (0x0B64)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CA4 TEST input port for CA4 I/O

DDRPHY_TESTILP5_CA5
Address: Operational Base + offset (0x0B68)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CA5 TEST input port for CA5 I/O

DDRPHY_TESTILP5_CA6
Address: Operational Base + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CA6 TEST input port for CA6 I/O

DDRPHY_TESTILP5_CS0
Address: Operational Base + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CS0 TEST input port for CS0 I/O

DDRPHY_TESTILP5_CS1
Address: Operational Base + offset (0x0B74)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_CS1 TEST input port for CS1 I/O

DDRPHY_TESTILP5_WCK0
Address: Operational Base + offset (0x0B78)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved
19:0	RW	0x199e0	TESTILP5_WCK0 TEST input port for WCK0 I/O

DDRPHY_TESTILP5_WCK1
Address: Operational Base + offset (0x0B7C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x199e0	TESTILP5_WCK1 TEST input port for WCK1 I/O

DDRPHY_DQSDUTY_CON0
Address: Operational Base + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSRiseDuty_rank0_DS0 For debug purpose

DDRPHY_DQSDUTY_CON1
Address: Operational Base + offset (0x0B84)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSFallDuty_rank0_DS0 For debug purpose

DDRPHY_DQSDUTY_CON2
Address: Operational Base + offset (0x0B88)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSRiseDuty_rank1_DS0 For debug purpose

DDRPHY_DQSDUTY_CON3
Address: Operational Base + offset (0x0B8C)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSFallDuty_rank1_DS0 For debug purpose

DDRPHY_DQSDUTY_CON4
Address: Operational Base + offset (0x0B90)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSRiseDuty_rank0_DS1 For debug purpose

DDRPHY_DQSDUTY_CON5
Address: Operational Base + offset (0x0B94)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSFallDuty_rank0_DS1 For debug purpose

DDRPHY_DQSDUTY_CON6
Address: Operational Base + offset (0x0B98)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSRiseDuty_rank1_DS1 For debug purpose

DDRPHY_DQSDUTY_CON7

Address: Operational Base + offset (0x0B9C)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved0 Reserved
26:0	RW	0x0000000	DQSFallDuty_rank1_DS1 For debug purpose

DDRPHY_MON_RCNT0

Address: Operational Base + offset (0x0BA0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:0	RO	0x00000000	MON_RCNT_DS0 For debug purpose

DDRPHY_MON_RCNT1

Address: Operational Base + offset (0x0BA4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	Reserved0 Reserved
14:0	RO	0x0000	MON_RCNT_DS0 For debug purpose

DDRPHY_MON_RCNT2

Address: Operational Base + offset (0x0BA8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:0	RO	0x00000000	MON_RCNT_DS1 For debug purpose

DDRPHY_MON_RCNT3

Address: Operational Base + offset (0x0BAC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	Reserved0 Reserved
14:0	RO	0x0000	MON_RCNT_DS1 For debug purpose

DDRPHY_CMD_DESKEWC_CODE0

Address: Operational Base + offset (0x0BB0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca1DeSkewCode CA1 De-skew center code
15:10	RO	0x00	Reserved0 Reserved

Bit	Attr	Reset Value	Description
9:0	RO	0x000	Ca0DeSkewCode CA0 De-skew center code

DDRPHY_CMD_DESKEWC_CODE1
Address: Operational Base + offset (0x0BB4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca3DeSkewCode CA3 De-skew center code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca2DeSkewCode CA2 De-skew center code

DDRPHY_CMD_DESKEWC_CODE2
Address: Operational Base + offset (0x0BB8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca5DeSkewCode CA5 De-skew center code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca4DeSkewCode CA4 De-skew center code

DDRPHY_CMD_DESKEWC_CODE3
Address: Operational Base + offset (0x0BBC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	Reserved0 Reserved
9:0	RO	0x000	Ca6DeSkewCode CA6 De-skew center code

DDRPHY_CMD_DESKEWC_CODE4
Address: Operational Base + offset (0x0BC0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	CsFineDeSkewCode CS Fine training De-skew center code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	CsCoarseDeSkewCode CS Coarse training De-skew center code

DDRPHY_CBT_CAL_STAT0
Address: Operational Base + offset (0x0BC4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25	RO	0x0	cbt_hw_cal_done LPDDR4 HW calibration done signal

Bit	Attr	Reset Value	Description
24:17	RO	0x00	cbt_vwm_max_flag Command bus training searching max flag cbt_fail_status[6:1]: CA0~CA5 cbt_fail_status[7]: CS Coarse cbt_fail_status[8]: CS Fine
16:9	RO	0x00	cbt_fail_status Command bus training fail status cbt_fail_status[6:1]: CA0~CA5 cbt_fail_status[7]: CS Coarse cbt_fail_status[8]: CS Fine
8:1	RO	0x00	cbt_pass_status Command bus training pass status cbt_pass_status[6:1]: CA0~CA5 cbt_pass_status[7]: CS Coarse cbt_pass_status[8]: CS Fine
0	RO	0x0	cbt_ck_offset_fail CS0 De-skew center code

DDRPHY_CMD_LEFT_CODE0
Address: Operational Base + offset (0x0BC8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca1VWMLCode Command bus training CA1 Left code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca0VWMLCode Command bus training CA0 Left code

DDRPHY_CMD_LEFT_CODE1
Address: Operational Base + offset (0x0BCC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca3VWMLCode Command bus training CA3 Left code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca2VWMLCode Command bus training CA2 Left code

DDRPHY_CMD_LEFT_CODE2
Address: Operational Base + offset (0x0BD0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca5VWMLCode Command bus training CA5 Left code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca4VWMLCode Command bus training CA4 Left code

DDRPHY_CMD_LEFT_CODE4

Address: Operational Base + offset (0x0BD8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	CsVWMLFineCode CS Fine training CS Left code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	CsVWMLCoarseCode CS Coarse training CS Left code

DDRPHY_CMD_RIGHT_CODE0
Address: Operational Base + offset (0x0BDC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca1VWMRCode Command bus training CA1 Right code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca0VWMRCode Command bus training CA0 Right code

DDRPHY_CMD_RIGHT_CODE1
Address: Operational Base + offset (0x0BE0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca3VWMRCode Command bus training CA3 Right code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca2VWMRCode Command bus training CA2 Right code

DDRPHY_CMD_RIGHT_CODE2
Address: Operational Base + offset (0x0BE4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	Ca5VWMRCode Command bus training CA5 Right code
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	Ca4VWMRCode Command bus training CA4 Right code

DDRPHY_CMD_RIGHT_CODE4
Address: Operational Base + offset (0x0BEC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved1 Reserved
25:16	RO	0x000	CsVWMRFineCode CS Fine training CS Right code

Bit	Attr	Reset Value	Description
15:10	RO	0x00	Reserved0 Reserved
9:0	RO	0x000	CsVWMRCoarseCode CS Coarse training CS Right code

DDRPHY_DVFS0_CLKMODE_CON

Address: Operational Base + offset (0x0BF0)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved
4	RW	0x0	dvfs0_phy_dll_2x 1'b1: PHY DLL 2x clock(=WCK) 1'b0: PHY DLL 1x clock(=WCK/2) Use only MODE4 and Under 3200Mbps
3	RW	0x1	dvfs0_phy_clk_2x 1'b1: PHY 2x clock 1'b0: PHY 1x clock for DVFS0
2:0	RW	0x1	dvfs0_phy_mode Clock ratio mode between MC and PHY for LP4/5 combo for DVFS0. 3'd0: LP4 mode DFI clock ratio MC : CK : DQS = 1:4:4(TBD) 3'd1: LP4 mode DFI clock ratio MC : CK : DQS = 1:2:2 3'd2: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 1:1:2 3'd3: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 2:1:4 3'd4: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 1:1:4

DDRPHY_DVFS1_CLKMODE_CON

Address: Operational Base + offset (0x0BF4)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved
4	RW	0x0	dvfs1_phy_dll_2x 1'b1: PHY DLL 2x clock(=WCK) 1'b0: PHY DLL 1x clock(=WCK/2) Use only MODE4 and Under 3200Mbps
3	RW	0x1	dvfs1_phy_clk_2x 1'b1: PHY 2x clock 1'b0: PHY 1x clock for DVFS1
2:0	RW	0x1	dvfs1_phy_mode Clock ratio mode between MC and PHY for LP4/5 combo for DVFS1. 3'd0: LP4 mode DFI clock ratio MC : CK : DQS = 1:4:4(TBD) 3'd1: LP4 mode DFI clock ratio MC : CK : DQS = 1:2:2 3'd2: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 1:1:2 3'd3: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 2:1:4 3'd4: LP5 mode DFI clock ratio MC : CK : WCK/RDQS = 1:1:4

DDRPHY_DVFS0_DCC_CON0

Address: Operational Base + offset (0x0BF8)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	Reserved0 Reserved
10	RW	0x0	dvfs0_duty_manual For debug purpose

Bit	Attr	Reset Value	Description
9:5	RW	0x00	dvfs0_DUTY_NCODE For debug purpose
4:0	RW	0x00	dvfs0_DUTY_PCODE For debug purpose

DDRPHY_DVFS1_DCC_CON0
Address: Operational Base + offset (0x0BFC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	Reserved0 Reserved
10	RW	0x0	dvfs1_duty_manual For debug purpose
9:5	RW	0x00	dvfs1_DUTY_NCODE For debug purpose
4:0	RW	0x00	dvfs1_DUTY_PCODE For debug purpose

DDRPHY_PTC_CON0
Address: Operational Base + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved
29:24	RW	0x26	ptc_ext_zq_mode_vref For debug purpose
23	RW	0x0	Reserved1 Reserved
22:20	RW	0x7	ptc_ext_zq_mode_dds For debug purpose
19	RW	0x0	Reserved2 Reserved
18:16	RW	0x7	ptc_ext_zq_mode_pdds For debug purpose
15	RW	0x0	Reserved3 Reserved
14:12	RW	0x0	ptc_ext_zq_force_impp For debug purpose
11	RW	0x0	Reserved4 Reserved
10:8	RW	0x0	ptc_ext_zq_force_impn For debug purpose
7	RO	0x0	Reserved5 Reserved
6:4	RO	0x0	ptc_ext_zq_pmon For debug purpose
3	RO	0x0	Reserved6 Reserved
2:0	RO	0x0	ptc_ext_zq_nmon For debug purpose

DDRPHY_PTC_CON1
Address: Operational Base + offset (0x0C04)

Bit	Attr	Reset Value	Description
31	RW	0x0	ptc_ext_zq_force For debug purpose

Bit	Attr	Reset Value	Description
30	RO	0x0	Reserved0 Reserved
29	RO	0x0	ptc_ext_zq_end For debug purpose
28:13	RW	0x0000	Reserved1 Reserved
12:8	RW	0x00	ptc_ext_ref For debug purpose
7:5	RW	0x0	Reserved2 Reserved
4	RW	0x1	ptc_ext_dfdqs For debug purpose
3	RW	0x0	ptc_ext_cmosrcv For debug purpose
2	RW	0x0	ptc_ext_en For debug purpose
1	RW	0x0	ptc_ext_out For debug purpose
0	RW	0x1	ptc_ext_read For debug purpose

DDRPHY_PTC_CON2

Address: Operational Base + offset (0x0C08)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved0 Reserved
30:20	RO	0x100	ptc_ext_lock_value For debug purpose
19	RW	0x0	Reserved1 Reserved
18:12	RW	0x08	ptc_ext_start_point For debug purpose
11	RW	0x0	Reserved2 Reserved
10:4	RW	0x08	ptc_ext_inc For debug purpose
3	RW	0x0	ptc_ext_half For debug purpose
2	RO	0x0	ptc_ext_clock For debug purpose
1	RO	0x0	ptc_ext_flock For debug purpose
0	RO	0x0	ptc_ext_locked For debug purpose

DDRPHY_PTC_CON3

Address: Operational Base + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:16	RW	0x000	ptc_ext_offsetr For debug purpose
15:10	RW	0x00	Reserved1 Reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	ptc_ext_offsetw For debug purpose

DDRPHY_PTC_CON4

Address: Operational Base + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	ptc_ext_mode For debug purpose
27	RW	0x0	Reserved0 Reserved
26:24	RW	0x0	ptc_ext_shiftc For debug purpose
23:20	RW	0x0	ptc_ext_debug For debug purpose
19:17	RO	0x0	Reserved1 Reserved
16	RO	0x0	ptc_ext_init_complete For debug purpose
15:4	RW	0x000	Reserved2 Reserved
3	RW	0x0	ptc_ext_rdlvl_en For debug purpose
2	RW	0x0	ptc_ext_rdlvl_wr_en For debug purpose
1	RW	0x0	ptc_ext_gatelvl_en For debug purpose
0	RW	0x0	ptc_ext_write_lvl_en For debug purpose

DDRPHY_PTC_CON5

Address: Operational Base + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved0 Feedback write latency
13	RW	0x0	test_compare Test compare
12	RW	0x0	test_end Test end
11:9	RW	0x0	Reserved1 Feedback write latency
8	RW	0x0	test_start Test start
7:6	RO	0x0	reserved
5	RO	0x0	test_err_ds1 For dpc1
4	RO	0x0	test_err_ds0 For dpc0
3:2	RO	0x0	reserved
1	RO	0x0	test_oky_ds1 For dpc1
0	RO	0x0	test_oky_ds0 For dpc0

DDRPHY_PTC_CON6

Address: Operational Base + offset (0x0C18)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 feedback write latency
28:24	RW	0x02	wrlatadj feedback write latency
23:21	RW	0x0	Reserved1 Feedback write latency
20:16	RW	0x02	rdlatadj Feedback read latency
15:8	RW	0x11	wrincradj Feedback write to read latency
7	RW	0x0	ptc_ext_pulld_dq For debug purpose
6	RW	0x0	ptc_ext_pulld_dqs For debug purpose
5	RW	0x0	burst16_mode For debug purpose
4	RW	0x0	PAT_INIT For debug purpose
3	RW	0x0	Reserved2 Reserved
2	RW	0x0	infinite_loop_en For debug purpose
1	RW	0x0	PTC_MODE_DS1 Set initial pattern control
0	RW	0x0	PTC_MODE_DS0 PHY test control mode for DPC0

DDRPHY_PTC_CON7

Address: Operational Base + offset (0x0C1C)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_wrdata_p3 Data pattern for wrdata p3
15:0	RW	0x00ff	ptc_wrdata_p2 Data pattern for wrdata p2

DDRPHY_PTC_CON8

Address: Operational Base + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_wrdata_p1 Data pattern for wrdata p1
15:0	RW	0x00ff	ptc_wrdata_p0 Data pattern for wrdata p0

DDRPHY_PTC_CON9

Address: Operational Base + offset (0x0C24)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_exp_wrdata_p3 Expected data pattern for wrdata p3
15:0	RW	0x00ff	ptc_exp_wrdata_p2 Expected data pattern for wrdata p2

DDRPHY_PTC_CON10

Address: Operational Base + offset (0x0C28)

Bit	Attr	Reset Value	Description
31:16	RW	0x00ff	ptc_exp_wrdata_p1 Expected data pattern for wrdata p1
15:0	RW	0x00ff	ptc_exp_wrdata_p0 Expected data pattern for wrdata p0

DDRPHY_PTC_CON11

Address: Operational Base + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31	RW	0x1	mode_phy For debug purpose
30	RW	0x0	mode_scan For debug purpose
29	RW	0x0	mode_nand For debug purpose
28	RW	0x0	mode_highz For debug purpose
27	RW	0x0	mode_mux For debug purpose
26:24	RW	0x0	mode_run For debug purpose
23:16	RW	0x00	Reserved0 Reserved
15:14	RW	0x0	ptc_wrdata_mask_p3 Data mask pattern for wrdata mask p3
13:12	RW	0x0	ptc_wrdata_mask_p2 Data mask pattern for wrdata mask p2
11:10	RW	0x0	ptc_wrdata_mask_p1 Data mask pattern for wrdata mask p1
9:8	RW	0x0	ptc_wrdata_mask_p0 Data mask pattern for wrdata mask p0
7:6	RW	0x0	ptc_exp_wrdata_mask_p3 Expected data mask pattern for wrdata mask p3
5:4	RW	0x0	ptc_exp_wrdata_mask_p2 Expected data mask pattern for wrdata mask p2
3:2	RW	0x0	ptc_exp_wrdata_mask_p1 Expected data mask pattern for wrdata mask p1
1:0	RW	0x0	ptc_exp_wrdata_mask_p0 Expected data mask pattern for wrdata mask p0

DDRPHY_PTC_CON12

Address: Operational Base + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w3_q1_ds0 w3 read data for DPC0
15:0	RO	0x0000	rddata_w2_q1_ds0 w2 read data for DPC0

DDRPHY_PTC_CON13

Address: Operational Base + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w1_q1_ds0 w1 read data for DPC0
15:0	RO	0x0000	rddata_w0_q1_ds0 w0 read data for DPC0

DDRPHY_PTC_CON14

Address: Operational Base + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w3_q1_ds1 w3 read data for DPC1
15:0	RO	0x0000	rddata_w2_q1_ds1 w2 read data for DPC1

DDRPHY_PTC_CON15

Address: Operational Base + offset (0x0C3C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	rddata_w1_q1_ds1 w1 read data for DPC1
15:0	RO	0x0000	rddata_w0_q1_ds1 w0 read data for DPC1

DDRPHY_PTC_CON16

Address: Operational Base + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:24	RO	0x00	dvfs_wrtrn_monitoring_ds1_cs1 For debug purpose
23:22	RO	0x0	Reserved1 Reserved
21:16	RO	0x00	dvfs_wrtrn_monitoring_ds0_cs1 For debug purpose
15:14	RO	0x0	Reserved2 Reserved
13:8	RO	0x00	dvfs_wrtrn_monitoring_ds1_cs0 For debug purpose
7:6	RO	0x0	Reserved3 Reserved
5:0	RO	0x00	dvfs_wrtrn_monitoring_ds0_cs0 For debug purpose

DDRPHY_PTC_CON17

Address: Operational Base + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Reserved0 Reserved

DDRPHY_PTC_CON18

Address: Operational Base + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Reserved0 Reserved

DDRPHY_PTC_CON19

Address: Operational Base + offset (0x0C4C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Reserved0 Reserved

DDRPHY_PTC_CON20
Address: Operational Base + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved0 Reserved
15:0	RO	0x0000	test_oky_dq test_oky_dq

DDRPHY_PTC_CON21
Address: Operational Base + offset (0x0C54)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved0 Reserved
15:0	RO	0x0000	test_err_dq test_err_dq

DDRPHY_PTC_CON22
Address: Operational Base + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	Reserved0 Reserved
9:8	RO	0x0	test_oky_dm test_oky_dm
7:2	RO	0x00	Reserved1 Reserved
1:0	RO	0x0	test_err_dm test_err_dm

DDRPHY_Periodic_ZQ_CON
Address: Operational Base + offset (0x0C70)

Bit	Attr	Reset Value	Description
31	RW	0x0	periodic_zq_cnt_en Periodic zq counter enable (Enable periodic ZQ calibration)
30:0	RW	0x000403f5	periodic_zq_time periodic_zq_time is defined interval of periodic zq calibrationn Total time = periodic_time*(period of clk_osc)

DDRPHY_PRBS_LEFT_MARGIN_DQ0
Address: Operational Base + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq0 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq0 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ0
Address: Operational Base + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq0 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq0 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ1

Address: Operational Base + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq1 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq1 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ1

Address: Operational Base + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq1 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq1 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ2

Address: Operational Base + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq2 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq2 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ2

Address: Operational Base + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq2 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq2 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ3

Address: Operational Base + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq3 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq3 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ3

Address: Operational Base + offset (0x0D1C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq3 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq3 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ4

Address: Operational Base + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq4 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq4 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ4

Address: Operational Base + offset (0x0D24)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq4 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq4 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ5
Address: Operational Base + offset (0x0D28)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq5 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq5 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ5
Address: Operational Base + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq5 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq5 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ6
Address: Operational Base + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq6 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq6 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ6
Address: Operational Base + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq6 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq6 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ7
Address: Operational Base + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq7 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq7 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ7
Address: Operational Base + offset (0x0D3C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq7 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq7 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ8
Address: Operational Base + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq8 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq8 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ8
Address: Operational Base + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq8 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq8 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ9
Address: Operational Base + offset (0x0D48)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq9 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq9 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ9
Address: Operational Base + offset (0x0D4C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq9 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq9 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ10
Address: Operational Base + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq10 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq10 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ10
Address: Operational Base + offset (0x0D54)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq10 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq10 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ11
Address: Operational Base + offset (0x0D58)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq11 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq11 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ11
Address: Operational Base + offset (0x0D5C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq11 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq11 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ12
Address: Operational Base + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq12 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq12 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ12
Address: Operational Base + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq12 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq12 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ13
Address: Operational Base + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq13 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq13 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ13
Address: Operational Base + offset (0x0D6C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq13 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq13 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ14
Address: Operational Base + offset (0x0D70)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq14 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq14 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ14
Address: Operational Base + offset (0x0D74)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq14 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq14 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DQ15
Address: Operational Base + offset (0x0D78)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dq15 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dq15 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DQ15
Address: Operational Base + offset (0x0D7C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dq15 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dq15 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DM0
Address: Operational Base + offset (0x0D80)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dm0 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dm0 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DM0
Address: Operational Base + offset (0x0D84)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dm0 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dm0 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_LEFT_MARGIN_DM1

Address: Operational Base + offset (0x0D88)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_left_l_dm1 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_left_h_dm1 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_PRBS_RIGHT_MARGIN_DM1

Address: Operational Base + offset (0x0D8C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved0 Reserved
25:16	RO	0x000	prbs_offset_right_l_dm1 prbs offset left margin captured by WDQS rising edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.
15:10	RO	0x00	Reserved1 Reserved
9:0	RO	0x000	prbs_offset_right_h_dm1 prbs offset left margin captured by WDQS falling edge. Should be used by prbs_per_bit_mode[PRBS_CON0[3]] = 1.

DDRPHY_WR_BYTE0_CYC_CS0_CODE

Address: Operational Base + offset (0x0DC0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RO	0x0	ctrl_shift_ecc_ds0_cs0 Write ECC Cycle Code for Data Slice0. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
26:24	RO	0x0	ctrl_shift_dm_ds0_cs0 Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

Bit	Attr	Reset Value	Description
23:21	RO	0x0	ctrl_shift_dq7_ds0_cs0 Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds0_cs0 Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RO	0x0	ctrl_shift_dq5_ds0_cs0 Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds0_cs0 Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RO	0x0	ctrl_shift_dq3_ds0_cs0 Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RO	0x0	ctrl_shift_dq2_ds0_cs0 Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RO	0x0	ctrl_shift_dq1_ds0_cs0 Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds0_cs0 Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WR_BYTE1_CYC_CS0_CODE
Address: Operational Base + offset (0x0DC4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RO	0x0	ctrl_shift_ecc_ds1_cs0 Write ECC Cycle Code for Data Slice1. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
26:24	RO	0x0	ctrl_shift_dm_ds1_cs0 Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RO	0x0	ctrl_shift_dq7_ds1_cs0 Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds1_cs0 Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

Bit	Attr	Reset Value	Description
17:15	RO	0x0	ctrl_shift_dq5_ds1_cs0 Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds1_cs0 Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RO	0x0	ctrl_shift_dq3_ds1_cs0 Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RO	0x0	ctrl_shift_dq2_ds1_cs0 Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RO	0x0	ctrl_shift_dq1_ds1_cs0 Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds1_cs0 Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WR_BYTE0_CYC_CS1_CODE

Address: Operational Base + offset (0x0DC8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RO	0x0	ctrl_shift_ecc_ds0_cs1 Write ECC Cycle Code for Data Slice0. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
26:24	RO	0x0	ctrl_shift_dm_ds0_cs1 Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RO	0x0	ctrl_shift_dq7_ds0_cs1 Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds0_cs1 Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RO	0x0	ctrl_shift_dq5_ds0_cs1 Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds0_cs1 Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

Bit	Attr	Reset Value	Description
11:9	RO	0x0	ctrl_shift_dq3_ds0_cs1 Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RO	0x0	ctrl_shift_dq2_ds0_cs1 Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RO	0x0	ctrl_shift_dq1_ds0_cs1 Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds0_cs1 Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WR_BYTE1_CYC_CS1_CODE

Address: Operational Base + offset (0x0DCC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RO	0x0	ctrl_shift_ecc_ds1_cs1 Write ECC Cycle Code for Data Slice1. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
26:24	RO	0x0	ctrl_shift_dm_ds1_cs1 Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RO	0x0	ctrl_shift_dq7_ds1_cs1 Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RO	0x0	ctrl_shift_dq6_ds1_cs1 Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RO	0x0	ctrl_shift_dq5_ds1_cs1 Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RO	0x0	ctrl_shift_dq4_ds1_cs1 Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RO	0x0	ctrl_shift_dq3_ds1_cs1 Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RO	0x0	ctrl_shift_dq2_ds1_cs1 Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

Bit	Attr	Reset Value	Description
5:3	RO	0x0	ctrl_shift_dq1_ds1_cs1 Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RO	0x0	ctrl_shift_dq0_ds1_cs1 Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE0_CYC_CS0_CODE

Address: Operational Base + offset (0x0DD0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RW	0x0	sw_shift_ecc_ds0_cs0 SW control for Write ECC Cycle Code for Data Slice0. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
26:24	RW	0x0	sw_shift_dm_ds0_cs0 SW control for Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds0_cs0 SW control for Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RW	0x0	sw_shift_dq6_ds0_cs0 SW control for Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RW	0x0	sw_shift_dq5_ds0_cs0 SW control for Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds0_cs0 SW control for Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds0_cs0 SW control for Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RW	0x0	sw_shift_dq2_ds0_cs0 SW control for Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds0_cs0 SW control for Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds0_cs0 SW control for Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE1_CYC_CS0_CODE

Address: Operational Base + offset (0x0DD4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RW	0x0	sw_shift_ecc_ds1_cs0 SW control for Write ECC Cycle Code for Data Slice1. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
26:24	RW	0x0	sw_shift_dm_ds1_cs0 SW control for Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds1_cs0 SW control for Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RW	0x0	sw_shift_dq6_ds1_cs0 SW control for Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RW	0x0	sw_shift_dq5_ds1_cs0 SW control for Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds1_cs0 SW control for Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds1_cs0 SW control for Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RW	0x0	sw_shift_dq2_ds1_cs0 SW control for Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds1_cs0 SW control for Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds1_cs0 SW control for Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE0_CYC_CS1_CODE

Address: Operational Base + offset (0x0DD8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RW	0x0	sw_shift_ecc_ds0_cs1 SW control for Write ECC Cycle Code for Data Slice0. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

Bit	Attr	Reset Value	Description
26:24	RW	0x0	sw_shift_dm_ds0_cs1 SW control for Write DM Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds0_cs1 SW control for Write DQ7 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
20:18	RW	0x0	sw_shift_dq6_ds0_cs1 SW control for Write DQ6 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RW	0x0	sw_shift_dq5_ds0_cs1 SW control for Write DQ5 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds0_cs1 SW control for Write DQ4 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds0_cs1 SW control for Write DQ3 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RW	0x0	sw_shift_dq2_ds0_cs1 SW control for Write DQ2 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds0_cs1 SW control for Write DQ1 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds0_cs1 SW control for Write DQ0 Cycle Code for Data Slice0. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_SW_WR_BYTE1_CYC_CS1_CODE

Address: Operational Base + offset (0x0DDC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved0 Reserved
29:27	RW	0x0	sw_shift_ecc_ds1_cs1 SW control for Write ECC Cycle Code for Data Slice1. Additional delay on ECC is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
26:24	RW	0x0	sw_shift_dm_ds1_cs1 SW control for Write DM Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
23:21	RW	0x0	sw_shift_dq7_ds1_cs1 SW control for Write DQ7 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

Bit	Attr	Reset Value	Description
20:18	RW	0x0	sw_shift_dq6_ds1_cs1 SW control for Write DQ6 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
17:15	RW	0x0	sw_shift_dq5_ds1_cs1 SW control for Write DQ5 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
14:12	RW	0x0	sw_shift_dq4_ds1_cs1 SW control for Write DQ4 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
11:9	RW	0x0	sw_shift_dq3_ds1_cs1 SW control for Write DQ3 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
8:6	RW	0x0	sw_shift_dq2_ds1_cs1 SW control for Write DQ2 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
5:3	RW	0x0	sw_shift_dq1_ds1_cs1 SW control for Write DQ1 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)
2:0	RW	0x0	sw_shift_dq0_ds1_cs1 SW control for Write DQ0 Cycle Code for Data Slice1. Additional delay on DQ/DM is ctrl_shift_d*[2:1] + 0.5* ctrl_shift_d*[0] cycle. (tWCK for LPDDR5, tCK for LPDDR4)

DDRPHY_WCKOSC_CON0

Address: Operational Base + offset (0x0DE0)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:16	RW	0x0437	ctrl_osc_counter Controls oscillator counter
15:8	RW	0x3f	ctrl_osc_runtime Controls oscillator runtime
7:1	RW	0x00	Reserved1 Reserved
0	RW	0x0	ctrl_wck_osc_en Controls wck oscillator enable

DDRPHY_WCKOSC_CON1

Address: Operational Base + offset (0x0DE4)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved
14:8	RW	0x01	wck_osc_upd_range_APB Sets wck oscillator update range
7:6	RW	0x2	wck_osc_avg_window_size_APB Sets wck oscillator average window size
5	RW	0x0	wck_osc_en_APB Sets wck oscillator enable

Bit	Attr	Reset Value	Description
4:3	RW	0x0	wck_osc_dq_swizzle_APB 2'b00: No SWAP 2'b01: BYTE SWAP + BIT SWAP 2'b10: BYTE SWAP 2'b11: BIT SWAP
2:0	RW	0x2	wck_osc_multiplier_APB Sets wck oscillator multiplier

DDRPHY_WCKOSC_CON2

Address: Operational Base + offset (0x0DE8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	wck_osc_cnt_new_cs1 Read wck oscillator counter for cs1
15:0	RO	0x0001	wck_osc_cnt_new_cs0 Read wck oscillator counter for cs0

DDRPHY_WCKOSC_CON3

Address: Operational Base + offset (0x0DEC)

Bit	Attr	Reset Value	Description
31	RO	0x1	wck_osc_cnt_applied Read wck oscillator applied counter
30:27	RO	0x0	Reserved0 Reserved
26	RO	0x0	wck_osc_overflow_cs1 Read wck oscillator overflow cs1
25:16	RO	0x000	offsetw_osc_cs1 Read offsetw oscillator cs1
15:11	RO	0x00	Reserved1 Reserved
10	RO	0x0	wck_osc_overflow_cs0 Read wck oscillator overflow cs0
9:0	RO	0x000	offsetw_osc_cs0 Read offsetw oscillator cs0

DDRPHY_DVFS0_WCKOSC_CON0

Address: Operational Base + offset (0x0DF0)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved
30:16	RW	0x0437	dvfs0_osc_counter Controls dvfs0 oscillator counter
15:8	RW	0x3f	dvfs0_osc_runtime Controls dvfs0 oscillator runtime
7:1	RW	0x00	Reserved1 Reserved
0	RW	0x0	dvfs0_wck_osc_en Controls dvfs0 wck oscillator enable

DDRPHY_DVFS1_WCKOSC_CON0

Address: Operational Base + offset (0x0DF4)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved0 Reserved

Bit	Attr	Reset Value	Description
30:16	RW	0x0437	dvfs1_osc_counter Controls dvfs1 oscillator counter
15:8	RW	0x3f	dvfs1_osc_runtime Controls dvfs1 oscillator runtime
7:1	RW	0x00	Reserved1 Reserved
0	RW	0x0	dvfs1_wck_osc_en Controls dvfs1 wck oscillator enable

DDRPHY_WRTRN_PARA_CON0

Address: Operational Base + offset (0x0DF8)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:20	RW	0x12	RDLAT_LP5_RFF_DMI_ON RFU(Reserved for future use) This field control PHY read latency on write training when LP5_RFF_DMI_ON is High. Read latency on write training can be different from Normal operation because of DRAM DMI buffer is on with LP5_RFF_DMI_ON. So if LP5_RFF_DMI_ON is High, User should be set to PHY read latency with READ DBI ON additionally as per PHY and Jedec specification.
19	RW	0x0	Reserved1 Reserved
18	RW	0x0	LP5_RFF_DMI_ON RFU(Reserved for future use) This field control RFF DMI buffer on MODE for PHY write training. 1'b1: RFF DMI buffer is on when Read dbi, Read link ecc and Read data copy MR settings are off during write training. 1'b0: Followed by user specific condition during write training.
17	RW	0x0	ctrl_RFF_CAS_IGNORE CAS command with RFF ignore during write training. 1'b1: Ignore 1'b0: No ignore
16	RW	0x0	WFF_RFF_TCCD_USER_MODE This field is MODE for control timing delay from WFF to RFF by User setting. This filed should used above 4266Mbps. 1'b1: Timing delay from WFF to RFF will be WFF_RFF_TCCD. 1'b0: Timing delay from WFF to RFF will be WL+BL_n+tWTR by SFR of phy scheduler.
15:8	RW	0x03	WFF_RFF_TCCD This field control timing delay from WFF to RFF during write training using phy scheduler. And WFF_RFF_TCCD_USER_MODE should be 1 for apply this parameter in normal operation. This filed should used above 4266Mbps. <Training FIFO tWTR setting guide> Dynamic sync mode : WFF_RFF_TCCD = FIFO tWTR +1 WCK always on mode(=free running mode) : WFF_RFF_TCCD = FIFO tWTR
7	RW	0x0	Reserved2 Reserved
6	RW	0x0	wrtrn_extra_resync This field control extra DLL update during write training.

Bit	Attr	Reset Value	Description
5:0	RW	0x16	wrtrn_trden2resp This field control timing delay from t_rddata_en to t_rdlvl_resp during write training using phy scheduler. Please only use 0x3 or 0x16(default value).

DDRPHY_DVFS0_WRTRN_PARA_CON0

Address: Operational Base + offset (0x0DFC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:20	RW	0x12	dvfs0_RDLAT_LP5_RFF_DMI_ON RFU(Reserved for future use) This field control PHY read latency on write training when dvfs0_LP5_RFF_DMI_ON is High. Read latency on write training can be different from Normal operation because of DRAM DMI buffer is on with dvfs0_LP5_RFF_DMI_ON. So if dvfs0_LP5_RFF_DMI_ON is High, User should be set to PHY read latency with READ DBI ON additionally as per PHY and Jedec specification.
19	RW	0x0	Reserved1 Reserved
18	RW	0x0	dvfs0_LP5_RFF_DMI_ON RFU(Reserved for future use) This field control RFF DMI buffer on MODE for PHY write training, 1'b1: RFF DMI buffer is on when Read dbi, Read link ecc and Read data copy MR settings are off during write training. 1'b0: Followed by user specific condition during write training.
17	RW	0x0	dvfs0_RFF_CAS_IGNORE CAS command with RFF ignore during write training. 1'b1: Ignore 1'b0: No ignore
16	RW	0x0	dvfs0_WFF_RFF_TCCD_USER_MODE This field is MODE for control timing delay from WFF to RFF by User setting. This filed should used above 4266Mbps. 1'b1: Timing delay from WFF to RFF will be WFF_RFF_TCCD. 1'b0: Timing delay from WFF to RFF will be WL+BL_n+tWTR by SFR of phy scheduler.
15:8	RW	0x03	dvfs0_WFF_RFF_TCCD This field control timing delay from WFF to RFF during write training using phy scheduler. And WFF_RFF_TCCD_USER_MODE should be 1 for apply this parameter in normal operation. minimum value is 3tck This filed should used above 4266Mbps <Training FIFO tWTR setting guide> Dynamic sync mode : WFF_RFF_TCCD = FIFO tWTR +1 WCK always on mode(=free running mode) : WFF_RFF_TCCD = FIFO tWTR
7	RW	0x0	Reserved2 Reserved
6	RW	0x0	dvfs0_wrtrn_extra_resync This field control extra DLL update during write training.
5:0	RW	0x16	dvfs0_wrtrn_trden2resp This field control timing delay from t_rddata_en to t_rdlvl_resp during write training using phy scheduler. Please only use 0x3 or 0x16(default value).

DDRPHY_DVFS1_WRTRN_PARA_CON0
Address: Operational Base + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved0 Reserved
25:20	RW	0x12	dvfs1_RDLAT_LP5_RFF_DMI_ON RFU(Reserved for future use) This field control PHY read latency on write training when dvfs1_LP5_RFF_DMI_ON is High. Read latency on write training can be different from Normal operation because of DRAM DMI buffer is on with dvfs1_LP5_RFF_DMI_ON. So If dvfs1_LP5_RFF_DMI_ON is High, User should be set to PHY read latency with READ DBI ON additionally as per PHY and Jedec specification.
19	RW	0x0	Reserved1 Reserved
18	RW	0x0	dvfs1_LP5_RFF_DMI_ON RFU(Reserved for future use) This field control RFF DMI buffer on MODE for PHY write training, 1'b1: RFF DMI buffer is on when Read dbi, Read link ecc and Read data copy MR settings are off during write training. 1'b0: Followed by user specific condition during write training.
17	RW	0x0	dvfs1_RFF_CAS_IGNORE CAS command with RFF ignore during write training. 1'b1: Ignore 1'b0: No ignore
16	RW	0x0	dvfs1_WFF_RFF_TCCD_USER_MODE This field is MODE for control timing delay from WFF to RFF by User setting. This filed should used above 4266Mbps. 1'b1: Timing delay from WFF to RFF will be WFF_RFF_TCCD. 1'b0: Timing delay from WFF to RFF will be WL+BL_n+tWTR by SFR of phy scheduler.
15:8	RW	0x03	dvfs1_WFF_RFF_TCCD This field control timing delay from WFF to RFF during write training using phy scheduler. And WFF_RFF_TCCD_USER_MODE should be 1 for apply this parameter in normal operation. Minimum value is 3tck. This filed should used above 4266Mbps <Training FIFO tWTR setting guide> Dynamic sync mode : WFF_RFF_TCCD = FIFO tWTR +1 WCK always on mode(=free running mode) : WFF_RFF_TCCD = FIFO tWTR
7	RW	0x0	Reserved2 Reserved
6	RW	0x0	dvfs1_wrtrn_extra_resync This field control extra DLL update during write training.
5:0	RW	0x16	dvfs1_wrtrn_trden2resp This field control timing delay from t_rddata_en to t_rdlvl_resp during write training using phy scheduler. Please only use 0x3 or 0x16(default value).

DDRPHY_DFI_LP_CON0
Address: Operational Base + offset (0x0E04)

Bit	Attr	Reset Value	Description
31	RW	0x0	DFI_LP_MODE_APB 1'b1: PHY clock gating is controlled by dfi_lp* 1'b0: PHY clock gating is controlled by ctrl_phy_cg_en Caution: If DFI_LP_MODE_APB is HiGH, PHY do not support DDRPHY2XCLKGATE_ENABLE control(=PHY root clock gating)
30:15	RW	0x0000	Reserved0 Reserved
14:12	RW	0x2	tlp_ctrl_resp_APB Actual tlp_ctrl_resp for low power I/F. It controls the latnecy between dfi_lp_ctrl_req assertion and dfi_lp_ctrl_ack assertion when low power mode is initated. 0~1: Don't use.
11	RW	0x0	Reserved1 Reserved
10:8	RW	0x3	tlp_ctrl_wakeup_APB Actual tlp_ctrl_wakeup for low power I/F. It controls the latency between dfi_lp_ctrl_req de-assertion and dfi_lp_ctrl_ack de-assertion when low power mode is terminated. 0~1: Don't use.
7	RW	0x0	Reserved2 Reserved
6:4	RW	0x2	tlp_data_resp_APB Actual tlp_data_resp for low power I/F. It controls the latnecy between dfi_lp_data_req assertion and dfi_lp_data_ack assertion when low power mode is initated. 0~1: Don't use.
3	RW	0x0	Reserved3 Reserved
2:0	RW	0x2	tlp_data_wakeup_APB Actual tlp_data_wakeup for low power I/F. It controls the latency between dfi_lp_data_req de-assertion and dfi_lp_data_ack de-assertion when low power mode is terminated. 0~1: Don't use.

DDRPHY_LOCK_CHECK_CON

Address: Operational Base + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved4 Reserved
24	RW	0x0	lock_check_diff_en Select the basic threshold to control the dfi_init_complete 1'b0: Controlled by lock_ratio_threshold_APB. 1'b1: Controlled by lock_diff_threshold_APB.
23	RW	0x0	Reserved3 Reserved

Bit	Attr	Reset Value	Description
22:12	RW	0x007	lock_diff_threshold When lock_check_diff_en_APB = 1'b1, Set the threshold value of the difference of lock value following below equation. lock_diff_threshold_APB ={ (standard_value_difference * period(ps) * 4 * (get_avg_lock_extend_APB+1) * 2^(lock_value_avg_n_sel_APB+3) } / 1000000 'standard_value_difference' have to be based on 1us. 'period' have to be based on ps. dfi_ init_complete will be controlled by equation. lock_value_avg_delta('N-th lock_value_avg' - '1-st lock_value_avg') > lock_diff_threshold_APB
11	RW	0x0	Reserved2 Reserved
10:6	RW	0x04	lock_ratio_threshold When lock_check_diff_en_APB = 1'b0, Select the threshold ratio of the lock value. 5'd0: 50% of start point lock value of average window 5:d1: 37.5% of start point lock value of average window 5'd2: 25% of start point lock value of average window 5'd3: 18.75% of start point lock value of average window 5'd4: 12.5% of start point lock value of average window 5:d5: 9.375% of start point lock value of average window 5'd6: 6.25% of start point lock value of average window 5'd7: 3.125% of start point lock value of average window 5'd8: 1.5625% of start point lock value of average window 5'd9: 0.78125% of start point lock value of average window dfi_ init_complete will be controlled by equation. lock_value_avg_delta('N-th lock_value_avg' - '1-st lock_value_avg') > 'N-th lock_value_avg' * ratio(%)
5:4	RW	0x0	get_avg_lock_extend Extend average window 2'b00: Average window * 1 2'b01: Average window * 2 2'b10: Average window * 3 2'b11: Average window * 4
3	RW	0x0	Reserved0 Reserved
2:1	RW	0x2	lock_check_avg_n_sel Select size of average window 2'b00: 8*4 DFI cycles * period 2'b01: 16*4 DFI cycles * period 2'b10: 32*4 DFI cycles * period 2'b11: 64*4 DFI cycles * period
0	RW	0x0	lock_check_avg_en Enable lock check with average lock value This bit should be set after set of lock_average_en.

DDRPHY_DFI_RDDATA0

Address: Operational Base + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata0_ds1 dfi_rddata_burst0 DS1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata0_ds0 dfi_rddata_burst0 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA1
Address: Operational Base + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata1_ds1 dfi_rddata_burst1 DS1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata1_ds0 dfi_rddata_burst1 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA2
Address: Operational Base + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata2_ds1 dfi_rddata_burst2 DS1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata2_ds0 dfi_rddata_burst2 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA3
Address: Operational Base + offset (0x0E1C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata3_ds1 dfi_rddata_burst3 DS1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata3_ds0 dfi_rddata_burst3 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA4
Address: Operational Base + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata4_ds1 dfi_rddata_burst4 DS1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata4_ds0 dfi_rddata_burst4 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA5
Address: Operational Base + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata5_ds1 dfi_rddata_burst5 DS1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata5_ds0 dfi_rddata_burst5 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA6
Address: Operational Base + offset (0x0E28)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata6_ds1 dfi_rddata_burst6 DS1 when scheduler_sw_mode is on.
15:0	RO	0x0000	dfi_rddata6_ds0 dfi_rddata_burst6 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA7
Address: Operational Base + offset (0x0E2C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dfi_rddata7_ds1 dfi_rddata_burst7 DS1 when scheduler_sw_mode is on.

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	dfi_rddata7_ds0 dfi_rddata_burst7 DS0 when scheduler_sw_mode is on.

DDRPHY_DFI_RDDATA_DM
Address: Operational Base + offset (0x0E30)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	dfi_rddata_dm7_ds1 dfi_rddata_burst7 DS1 when scheduler_sw_mode is on.
29:28	RO	0x0	dfi_rddata_dm7_ds0 dfi_rddata_burst7 DS0 when scheduler_sw_mode is on.
27:26	RO	0x0	dfi_rddata_dm6_ds1 dfi_rddata_burst6 DS1 when scheduler_sw_mode is on.
25:24	RO	0x0	dfi_rddata_dm6_ds0 dfi_rddata_burst6 DS0 when scheduler_sw_mode is on.
23:22	RO	0x0	dfi_rddata_dm5_ds1 dfi_rddata_burst5 DS1 when scheduler_sw_mode is on.
21:20	RO	0x0	dfi_rddata_dm5_ds0 dfi_rddata_burst5 DS0 when scheduler_sw_mode is on.
19:18	RO	0x0	dfi_rddata_dm4_ds1 dfi_rddata_burst4 DS1 when scheduler_sw_mode is on.
17:16	RO	0x0	dfi_rddata_dm4_ds0 dfi_rddata_burst4 DS0 when scheduler_sw_mode is on.
15:14	RO	0x0	dfi_rddata_dm3_ds1 dfi_rddata_burst3 DS1 when scheduler_sw_mode is on.
13:12	RO	0x0	dfi_rddata_dm3_ds0 dfi_rddata_burst3 DS0 when scheduler_sw_mode is on.
11:10	RO	0x0	dfi_rddata_dm2_ds1 dfi_rddata_burst2 DS1 when scheduler_sw_mode is on.
9:8	RO	0x0	dfi_rddata_dm2_ds0 dfi_rddata_burst2 DS0 when scheduler_sw_mode is on.
7:6	RO	0x0	dfi_rddata_dm1_ds1 dfi_rddata_burst1 DS1 when scheduler_sw_mode is on.
5:4	RO	0x0	dfi_rddata_dm1_ds0 dfi_rddata_burst1 DS0 when scheduler_sw_mode is on.
3:2	RO	0x0	dfi_rddata_dm0_ds1 dfi_rddata_burst0 DS1 when scheduler_sw_mode is on.
1:0	RO	0x0	dfi_rddata_dm0_ds0 dfi_rddata_burst0 DS0 when scheduler_sw_mode is on.

DDRPHY_LP5_MR_OP2
Address: Operational Base + offset (0x0E34)

Bit	Attr	Reset Value	Description
31:24	RW	0xc6	LP5_MR3_PHY RFU(Reserved for future use) LP5 DRAM MR3 setting during write training [31:24] = OP[7:0]
23:16	RW	0xbb	LP5_MR2_PHY RFU(Reserved for future use) LP5 DRAM MR2 setting during write training [23:16] = OP[7:0]
15:8	RW	0xc6	LP5_MR3_DRAM RFU(Reserved for future use) LP5 DRAM MR3 setting during normal operation [15:8] = OP[7:0]

Bit	Attr	Reset Value	Description
7:0	RW	0xbb	LP5_MR2_DRAM RFU(Reserved for future use) LP5 DRAM MR2 setting during normal operation [7:0] = OP[7:0]

DDRPHY_DVFS0_LP5_MR_OP2

Address: Operational Base + offset (0x0E38)

Bit	Attr	Reset Value	Description
31:24	RW	0xc6	dvfs0_LP5_MR3_PHY RFU(Reserved for future use) LP5 DRAM MR3 setting during write training [31:24] = OP[7:0]
23:16	RW	0xbb	dvfs0_LP5_MR2_PHY RFU(Reserved for future use) LP5 DRAM MR2 setting during write training [23:16] = OP[7:0]
15:8	RW	0xc6	dvfs0_LP5_MR3_DRAM RFU(Reserved for future use) LP5 DRAM MR3 setting during normal operation [15:8] = OP[7:0]
7:0	RW	0xbb	dvfs0_LP5_MR2_DRAM RFU(Reserved for future use) LP5 DRAM MR2 setting during normal operation [7:0] = OP[7:0]

DDRPHY_DVFS1_LP5_MR_OP2

Address: Operational Base + offset (0x0E3C)

Bit	Attr	Reset Value	Description
31:24	RW	0xc6	dvfs1_LP5_MR3_PHY RFU(Reserved for future use) LP5 DRAM MR3 setting during write training [31:24] = OP[7:0]
23:16	RW	0xbb	dvfs1_LP5_MR2_PHY RFU(Reserved for future use) LP5 DRAM MR2 setting during write training [23:16] = OP[7:0]
15:8	RW	0xc6	dvfs1_LP5_MR3_DRAM RFU(Reserved for future use) LP5 DRAM MR3 setting during normal operation [15:8] = OP[7:0]
7:0	RW	0xbb	dvfs1_LP5_MR2_DRAM RFU(Reserved for future use) LP5 DRAM MR2 setting during normal operation [7:0] = OP[7:0]

DDRPHY_PHYUPD_PARA_CON0

Address: Operational Base + offset (0x0E40)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved0 Reserved
12	RW	0x1	ctrl_upd_req_timeout_en For debug purpose. If ctrl_upd_req_timeout_en = 1 and dfi_phyupd_ack is not asserted to corresponding dfi_phyupd_req assertion, dfi_phyupd_req will be deasserted after tphyupd_resp is expired.

Bit	Attr	Reset Value	Description
11:9	RW	0x0	Reserved1 Reserved
8:0	RW	0x03f	ctrl_tphyupd_resp ctrl_tphyupd_resp parameter in term of DFI clock cycle Please should use default value during normal operation. But If write leveing need to enable during LPDDR5 WCK free running mode, Please control this register under 300ns as per memory controller specification.

DDRPHY_DVFS0_PHYUPD_PARA_CON0

Address: Operational Base + offset (0x0E44)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved0 Reserved
12	RW	0x1	dvfs0_upd_req_timeout_en For debug purpose. If dvfs0_upd_req_timeout_en = 1 and dfi_phyupd_ack is not asserted to corresponding dfi_phyupd_req assertion, dfi_phyupd_req will be deasserted after tphyupd_resp is expired.
11:9	RW	0x0	Reserved1 Reserved
8:0	RW	0x03f	dvfs0_tphyupd_resp dvfs0_tphyupd_resp parameter in term of DFI clock cycle. Please should use default value during normal operation. But If write leveing need to enable during LPDDR5 WCK free running mode on DVFS0, Please control this reigister under 300ns as per memory controller specification.

DDRPHY_DVFS1_PHYUPD_PARA_CON0

Address: Operational Base + offset (0x0E48)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved0 Reserved
12	RW	0x1	dvfs1_upd_req_timeout_en For debug purpose. If dvfs1_upd_req_timeout_en = 1 and dfi_phyupd_ack is not asserted to corresponding dfi_phyupd_req assertion, dfi_phyupd_req will be deasserted after tphyupd_resp is expired.
11:9	RW	0x0	Reserved1 Reserved
8:0	RW	0x03f	dvfs1_tphyupd_resp dvfs1_tphyupd_resp parameter in term of DFI clock cycle. Please should use default value during normal operation. But If write leveing need to enable during LPDDR5 WCK free running mode on DVFS1, Please control this register under 300ns as per memory controller specification.

2.5 Interface Description

DDR IOs from DDRPHY are listed as following table.

Table 2-1 DDR Channel 0 IO description

Pad Name	Description
DDR_CH0_CK_A	Positive differential clock
DDR_CH0_CKB_A	Negative differential clock
DDR_CH0_RESET_A	When asserted LOW, this signal resets the die.
DDR_CH0_LP4/4X_CKE0/LP5_CS0_A	Active-high clock enable signal for rank0 of

	LPDDR4/4X and acts as chip select signal for rank0 of LPDDR5.
DDR_CH0_LP4/4X_CKE1/LP5_CS1_A	Active-high clock enable signal for rank1 of LPDDR4/4X and acts as chip select signal for rank1 of LPDDR5.
DDR_CH0_LP4/4X_CS0_A	Chip select signal for rank0. Only used for LPDDR4/4X.
DDR_CH0_LP4/4X_CS1_A	Chip select signal for rank1. Only used for LPDDR4/4X.
DDR_CH0_Ai_A(i=0~6)	Command and address signals
DDR_CH0_DQS0P_A	Positive DQS for DQ[7:0]
DDR_CH0_DQS0N_A	Negative DQS for DQ[7:0]
DDR_CH0_DQS1P_A	Positive DQS for DQ[15:8]
DDR_CH0_DQS1N_A	Negative DQS for DQ[15:8]
DDR_CH0_WCK0P_A	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH0_WCK0N_A	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH0_WCK1P_A	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH0_WCK1N_A	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH0_DM0_A	This signal achieves multiple function such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and it is a bi-directional signal and each byte of data has a DMI signal. This signal correspondes to DQ[7:0].
DDR_CH0_DM1_A	This signal correspondes to DQ[15:8].
DDR_CH0_DQi_A(i=0~15)	Bidirectional data bus
DDR_CH0_ZQ_A	Used to calibrate the output drive strength and the termination resistance as calibration reference.

Table 2-2 DDR Channel 1 IO description

Pad Name	Description
DDR_CH0_CK_B	Positive differential clock
DDR_CH0_CKB_B	Negative differential clock
DDR_CH0_RESET_B	When asserted LOW, this signal resets the die.
DDR_CH0_LP4/4X_CKE0/LP5_CS0_B	Active-high clock enable signal for rank0 of LPDDR4/4X and acts as chip select signal for rank0 of LPDDR5.
DDR_CH0_LP4/4X_CKE1/LP5_CS1_B	Active-high clock enable signal for rank1 of LPDDR4/4X and acts as chip select signal for rank1 of LPDDR5.
DDR_CH0_LP4/4X_CS0_B	Chip select signal for rank0. Only used for LPDDR4/4X.
DDR_CH0_LP4/4X_CS1_B	Chip select signal for rank1. Only used for LPDDR4/4X.
DDR_CH0_Ai_B(i=0~6)	Command and address signals
DDR_CH0_DQS0P_B	Positive DQS for DQ[7:0]
DDR_CH0_DQS0N_B	Negative DQS for DQ[7:0]
DDR_CH0_DQS1P_B	Positive DQS for DQ[15:8]
DDR_CH0_DQS1N_B	Negative DQS for DQ[15:8]

Pad Name	Description
DDR_CH0_WCK0P_B	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH0_WCK0N_B	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH0_WCK1P_B	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH0_WCK1N_B	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH0_DM0_B	This signal achieves multiple function such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and it is a bi-directional signal and each byte of data has a DMI signal. This signal correspondes to DQ[7:0].
DDR_CH0_DM1_B	This signal correspondes to DQ[15:8].
DDR_CH0_DQi_B(i=0~15)	Bidirectional data bus
DDR_CH0_ZQ_B	Used to calibrate the output drive strength and the termination resistance as calibration reference.

Table 2-3 DDR Channel 2 IO description

Pad Name	Description
DDR_CH1_CK_C	Positive differential clock
DDR_CH1_CKB_C	Negative differential clock
DDR_CH1_RESET_C	When asserted LOW, this signal resets the die.
DDR_CH1_LP4/4X_CKE0/LP5_CS0_C	Active-high clock enable signal for rank0 of LPDDR4/4X and acts as chip select signal for rank0 of LPDDR5.
DDR_CH1_LP4/4X_CKE1/LP5_CS1_C	Active-high clock enable signal for rank1 of LPDDR4/4X and acts as chip select signal for rank1 of LPDDR5.
DDR_CH1_LP4/4X_CS0_C	Chip select signal for rank0. Only used for LPDDR4/4X.
DDR_CH1_LP4/4X_CS1_C	Chip select signal for rank1. Only used for LPDDR4/4X.
DDR_CH1_Ai_C(i=0~6)	Command and address signals
DDR_CH1_DQS0P_C	Positive DQS for DQ[7:0]
DDR_CH1_DQS0N_C	Negative DQS for DQ[7:0]
DDR_CH1_DQS1P_C	Positive DQS for DQ[15:8]
DDR_CH1_DQS1N_C	Negative DQS for DQ[15:8]
DDR_CH1_WCK0P_C	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH1_WCK0N_C	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH1_WCK1P_C	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH1_WCK1N_C	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH1_DM0_C	This signal achieves multiple function such as Data

	Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and it is a bi-directional signal and each byte of data has a DMI signal. This signal correspondes to DQ[7:0].
DDR_CH1_DM1_C	This signal correspondes to DQ[15:8].
DDR_CH1_DQi_C(i=0~15)	Bidirectional data bus
DDR_CH1_ZQ_C	Used to calibrate the output drive strength and the termination resistance as calibration reference.

Table 2-4 DDR Channel 3 IO description

Pad Name	Description
DDR_CH1_CK_D	Positive differential clock
DDR_CH1_CKB_D	Negative differential clock
DDR_CH1_RESET_D	When asserted LOW, this signal resets the die.
DDR_CH1_LP4/4X_CKE0/LP5_CS0_D	Active-high clock enable signal for rank0 of LPDDR4/4X and acts as chip select signal for rank0 of LPDDR5.
DDR_CH1_LP4/4X_CKE1/LP5_CS1_D	Active-high clock enable signal for rank1 of LPDDR4/4X and acts as chip select signal for rank1 of LPDDR5.
DDR_CH1_LP4/4X_CS0_D	Chip select signal for rank0. Only used for LPDDR4/4X.
DDR_CH1_LP4/4X_CS1_D	Chip select signal for rank1. Only used for LPDDR4/4X.
DDR_CH1_Ai_D(i=0~6)	Command and address signals
DDR_CH1_DQS0P_D	Positive DQS for DQ[7:0]
DDR_CH1_DQS0N_D	Negative DQS for DQ[7:0]
DDR_CH1_DQS1P_D	Positive DQS for DQ[15:8]
DDR_CH1_DQS1N_D	Negative DQS for DQ[15:8]
DDR_CH1_WCK0P_D	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH1_WCK0N_D	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[7:0].
DDR_CH1_WCK1P_D	Positive differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH1_WCK1N_D	Negative differential clock used for WRITE data capture and READ data output for LPDDR5. It correspondes to DQ[15:8].
DDR_CH1_DM0_D	This signal achieves multiple function such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and it is a bi-directional signal and each byte of data has a DMI signal. This signal correspondes to DQ[7:0].
DDR_CH1_DM1_D	This signal correspondes to DQ[15:8].
DDR_CH1_DQi_D(i=0~15)	Bidirectional data bus
DDR_CH1_ZQ_D	Used to calibrate the output drive strength and the termination resistance as calibration reference.

2.6 Application Notes

2.6.1 4-channel Interleaving LPDDR4/4X Initialization

Following steps are for 4-channel interleaving LPDDR4/4X initialization.

1. Power up DDRPHY core supply (DDR_CH0_VDD and DDR_CH1_VDD), power up CKE power (DDR_CH0_VDDQ_CKE and DDR_CH1_VDDQ_CKE) and then power up IO supply

(DDR_CH0_VDDQ_CK, DDR_CH0_VDDQ, DDR_CH1_VDDQ_CK and DDR_CH1_VDDQ).
2. Keep DDRPLL (D0APLL, D1APLL, D2APLL and D3APLL) at default configuration to output 24MHz frequency. Configure DDRPLL (D0BPLL, D1BPLL, D2BPLL and D3BPLL) to lock at target operation frequency. Now defaultly the input clk_phy2x of DDRPHY is 24MHz. Make sure that PCLK frequency of DDRPHY is not higher than clk_dfi which is generated from clk_phy2x.
3. De-assert PRESETn of DDRPHY and present of DDRCTL.
4. De-assert RESETn of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
5. Set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1'b1, set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1'b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY. Wait for at least 10 cycles of clk_phy2x.
6. De-assert div_rst_n of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
7. Assert sbr_resetn, core_ddrc_rstn and aresetn_0 of DDRCTL.
8. De-assert rst_n of DDRPHY. Make sure that rst_n is released at 24MHz low frequency.
9. Set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1'b0, set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1'b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
10. Assert div_rst_n of DDRPHY.
11. Set DDRPHY registers to select memory type and clock mode.
- DDRPHY_GNR_CON0.ctrl_ddr_mode='h0
- DDRPHY_CLKMODE_CON.ctrl_phy_mode='h1
- DDRPHY_CLKMODE_CON.ctrl_phy_clk_2x='h1

12. De-assert div_rst_n of DDRPHY.
13. Excutes step 5 again to enable the output clk_dfi of DDRPHY. Clk_dfi is used as the source clock of DDRCTL. It is connected to the core_ddrc_core_clk, aclk_0, sbr_clk and bsm_clk of DDRCTL.
14. Set DDRCTL registers.
15. De-assert sbr_resetn, core_ddrc_rstn and aresetn_0 of DDRCTL.
16. Disable auto-refreshes, self-refresh, powerdown and assertion of dfi_dram_clk_disable by setting DDRCTL_RFSHCTL0.dis_auto_refresh = 1, DDRCTL_PWRCTL.powerdown_en = 0 and DDRCTL_PWRCTL.selfref_en = 0, DDRCTL_PWRTL.en_dfi_dram_clk_disable = 0.
17. Set DDRCTL_SWCTL.sw_done to 1'b0.
18. Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b0.
19. Set DDRCTL_SWCTL.sw_done to 1'b1.
20. Set DDRCTL_PCTRL.port_en to 1'b1 to enable AXI port of DDRCTL.
21. Begin to set DDRPHY registers. Such as read latency, write latency and burst length and so on.
22. Apply DDRPHY IO settings before ZQ calibration.
23. Start DFI initialization
- Set DDRPHY_MDLL_CON0.ctrl_dll_on=1'b0
- DDRCTL should assert dfi_init_start from low to high
- DDRCTL should wait dfi_init_complete change from low to high

24. Set DDRCTL_SWCTL.sw_done to 1'b0. Set DDRCTL_DFIMISC.dfi_init_start to 1'b0 and DDRCTL_DFIMISC.dfi_init_complete_en to 1'b1. Set DDRCTL_SWCTL.sw_done to 1'b1.
25. Wait for DDRCTL to move to normal operating mode by monitoring DDRCTL_STAT.operating_mode register.
26. DDRPHY vref related registers settings without vref training.
27. DDRPHY ODT related registers settings.
28. Start DDRPHY ZQ calibration.
- Enable DDRPHY_ZQ_CON0.zq_clk_div_en
- Enable DDRPHY_ZQ_CON0.zq_manual_str
- Wait until DDRPHY_ZQ_CON1.zq_done is enabled
- Disable DDRPHY_ZQ_CON0.zq_manual_str
- Disable DDRPHY_ZQ_CON0.zq_clk_div_en

29. Frequency change to the target operation speed. Using frequency change protocol via MC-PHY handshake.
- Set DDRCTL_SWCTL.sw_done to 1'b0.
- Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b0.

- Set DDRCTL_DFIMISC.dfi_init_start to 1'b1. Set DDRCTL_SWCTL.sw_done to 1'b1.
- Poll DDRCTL_DFISTAT.dfi_init_complete=1'b0.
- Programming DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1'b0, programming DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1'b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
- Assert div_rst_n of DDRPHY.
- Change clk_phy2x frequency of DDRPHY by setting DDR0CRU_CLKSEL_CON00[0], DDR1CRU_CLKSEL_CON00[0], DDR2CRU_CLKSEL_CON00[0] and DDR3CRU_CLKSEL_CON00[0] to 1'b1 to select D0BPLL, D1BPLL, D2BPLL and D3BPLL output clock as DDRPHY driving clock.
- De-assert div_rst_n of DDRPHY.
- Set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1'b1, set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1'b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
- Set DDRCTL_SWCTL.sw_done to 1'b0. Set DDRCTL_DFIMISC.dfi_init_start to 1'b0. Set DDRCTL_SWCTL.sw_done to 1'b1.
- Poll DDRCTL_DFISTAT.dfi_init_complete=1'b1.
- Set DDRCTL_SWCTL.sw_done to 1'b0.
- Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b1 to indicate to the controller that the DDRPHY has finished frequency change.
- Set DDRCTL_SWCTL.sw_done to 1'b1.

30. Turn DDRPHY master DLL by setting DDRPHY_MDLL_CON0.ctrl_dll_on=1'b1.
31. Start DDRPHY master DLL locking by enable DDRPHY_MDLL_CON0.ctrl_start
    - Set DDRPHY_MDLL_CON0.ctrl_start to 1'b0.
    - Set DDRPHY_MDLL_CON0.ctrl_start to 1'b1.
    - Wait until DDRPHY_MDLL_CON1.ctrl_locked=1'b1.
32. DDRPHY SFR settings. Set DDRPHY_LP_CON0.ctrl_scheduler_en to 1'b1 and other registers if necessary.
33. Start DDRPHY initial training. Please refer to the following section for LPDDR4/4X training procedure.
34. DDRPHY SFR settings that should be set after training such as following registers and so on.
    - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw to 1'b0.
    - Set DDRPHY_CAL_CON0.cal_vtc_en to 1'b1.
    - Set DDRPHY_CAL_CON5.wrtrn_cycle_mode=0 during normal operation.

2.6.2 4-channel Interleaving LPDDR5 Initialization

Following steps are for 4-channel interleaving LPDDR5 initialization.

1. Power up DDRPHY core supply (DDR_CH0_VDD and DDR_CH1_VDD), power up CKE power (DDR_CH0_VDDQ_CKE and DDR_CH1_VDDQ_CKE) and then power up IO supply (DDR_CH0_VDDQ_CK, DDR_CH0_VDDQ, DDR_CH1_VDDQ_CK and DDR_CH1_VDDQ).
2. Keep DDRPLL (D0APLL, D1APLL, D2APLL and D3APLL) at default configuration to output 24MHz frequency. Configure DDRPLL (D0BPLL, D1BPLL, D2BPLL and D3BPLL) to lock at target operation frequency. Now defaultly the input clk_phy2x of DDRPHY is 24MHz. Make sure that PCLK frequency of DDRPHY is not higher than clk_dfi which is generated from clk_phy2x.
3. De-assert PRESETn of DDRPHY and present of DDRCTL.
4. De-assert RESETn of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
5. Set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1'b1, set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1'b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY. Wait for at least 10 cycles of clk_phy2x.
6. De-assert div_rst_n of DDRPHY. Wait for at least 10 cycles of clk_phy2x.
7. Assert sbr_resetn, core_ddrc_rstn and aresetn_0 of DDRCTL.
8. De-assert rst_n of DDRPHY. Make sure that rst_n is released at 24MHz low frequency.
9. Set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1'b0, set DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1'b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
10. Assert div_rst_n of DDRPHY.
11. Set DDRPHY registers to select memory type and clock mode. Following configuration

are for 1:1:4 mode (CLK_DFI: CK: WCK).
- DDRPHY_GNR_CON0.ctrl_ddr_mode='h2
- DDRPHY_CLKMODE_CON.ctrl_phy_mode='h4
- DDRPHY_CLKMODE_CON.ctrl_phy_clk_2x='h1

If CLK_DFI: CK: WCK is 1:1:2, following configuration should be followed.
- DDRPHY_GNR_CON0.ctrl_ddr_mode='h2
- DDRPHY_CLKMODE_CON.ctrl_phy_mode='h2
- DDRPHY_CLKMODE_CON.ctrl_phy_clk_2x='h1

12. De-assert div_rst_n of DDRPHY.
13. Excutes step 5 again to enable the output clk_dfi of DDRPHY. Clk_dfi is used as the source clock of DDRCTL. It is connected to the core_ddrc_core_clk, aclk_0, sbr_clk and bsm_clk of DDRCTL.
14. Set DDRCTL registers.
15. De-assert sbr_resetn, core_ddrc_rstn and aresetn_0 of DDRCTL.
16. Disable auto-refreshes, self-refresh, powerdown and assertion of dfi_dram_clk_disable by setting DDRCTL_RFSHCTL0.dis_auto_refresh = 1, DDRCTL_PWRCTL.powerdown_en = 0 and DDRCTL_PWRCTL.selfref_en = 0, DDRCTL_PWRTL.en_dfi_dram_clk_disable = 0.
17. Set DDRCTL_SWCTL.sw_done to 1'b0.
18. Set DDRCTL_DFIMISC.dfi_init_complete_en to 1'b0.
19. Set DDRCTL_SWCTL.sw_done to 1'b1.
20. Set DDRCTL_PCTRL.port_en to 1'b1 to enable AXI port of DDRCTL.
21. Begin to set DDRPHY registers. Such as read latency, write latency and burst length and so on.
22. Apply DDRPHY IO settings before ZQ calibration.
23. DDRPHY DLL lock value force and update for low frequency initialization under 100MHz.
    - Set DDRPHY_MDLL_CON0.ctrl_force=11'h2ef.
    - Set DDRPHY_MDLL_CON0.ctrl_dll_on=1'b0.
24. Start DFI initialization
    - DDRCTL should assert dfi_init_start from low to high
    - DDRCTL should wait dfi_init_complete change from low to high
    - Enable and then disable DDRPHY_OFFSETD_CON0.ctrl_resync 10 cycles after de-asserting ctrl_dll_on.
25. Set DDRCTL_SWCTL.sw_done to 1'b0. Set DDRCTL_DFIMISC.dfi_init_start to 1'b0 and DDRCTL_DFIMISC.dfi_init_complete_en to 1'b1. Set DDRCTL_SWCTL.sw_done to 1'b1.
26. Delay an appropriate period of time according to the DDRCTL_INITTMG1.dram_rstn_x1024 to issue power down exit asynchronously by programming following registers.
    - Set DDR_GRF_CHA_CON2[17:0] and DDR_GRF_CHB_CON2[17:0] of DDR01_GRF to 8'hff, set DDR_GRF_CHA_CON2[17:0] and DDR_GRF_CHB_CON2[17:0] of DDR23_GRF to 8'hff to toggle LPDDR5 chip select signal(CS).
    - Set DDR_GRF_CHA_CON2[17:0] and DDR_GRF_CHB_CON2[17:0] of DDR01_GRF to 8'h00, set DDR_GRF_CHA_CON2[17:0] and DDR_GRF_CHB_CON2[17:0] of DDR23_GRF to 8'h00.
27. Start memory initialization by DDRCTL by sending MRW command.
28. Wait for DDRCTL to move to normal operating mode by monitoring DDRCTL_STAT.operating_mode register.
29. DDRPHY vref related registers settings without vref training.
30. DDRPHY ODT related registers settings.
31. Start DDRPHY ZQ calibration.
    - Enable DDRPHY_ZQ_CON0.zq_clk_div_en
    - Enable DDRPHY_ZQ_CON0.zq_manual_str
    - Wait until DDRPHY_ZQ_CON1.zq_done is enabled
    - Disable DDRPHY_ZQ_CON0.zq_manual_str
    - Disable DDRPHY_ZQ_CON0.zq_clk_div_en
32. Frequency change to the target operation speed. Using frequency change protocol via MC-PHY hangshake.
    - Set DDRCTL_SWCTL.sw_done to 1'b0.

- Set DDRCTL_DFIMISC.dfi_init_complete_en to 1’b0.
- Set DDRCTL_DFIMISC.dfi_init_start to 1’b1. Set DDRCTL_SWCTL.sw_done to 1’b1.
- Poll DDRCTL_DFISTAT.dfi_init_complete=1’b0.
- Programming DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1’b0, programming DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1’b0 to disable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
- Assert div_rst_n of DDRPHY.
- Change clk_phy2x frequency of DDRPHY by setting DDR0CRU_CLKSEL_CON00[0], DDR1CRU_CLKSEL_CON00[0], DDR2CRU_CLKSEL_CON00[0] and DDR3CRU_CLKSEL_CON00[0] to 1’b1 to select D0BPLL, D1BPLL, D2BPLL and D3BPLL output clock as DDRPHY driving clock.
- De-assert div_rst_n of DDRPHY.
- Programming DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR01_GRF to 1’b1, programming DDR_GRF_PHY_CON0[3] and DDR_GRF_PHY_CON1[3] of DDR23_GRF to 1’b1 to enable DDRPHY2XCLKGATE_ENABLE of each DDRPHY.
- Set DDRCTL_SWCTL.sw_done to 1’b0. Set DDRCTL_DFIMISC.dfi_init_start to 1’b0. Set DDRCTL_SWCTL.sw_done to 1’b1.
- Poll DDRCTL_DFISTAT.dfi_init_complete=1’b1.
- Set DDRCTL_SWCTL.sw_done to 1’b0.
- Set DDRCTL_DFIMISC.dfi_init_complete_en to 1’b1 to indicate to the controller that the DDRPHY has finished frequency change.
- Set DDRCTL_SWCTL.sw_done to 1’b1.

33. Turn DDRPHY master DLL by setting DDRPHY_MDLL_CON0.ctrl_dll_on=1’b1.
34. Start DDRPHY master DLL locking by enable DDRPHY_MDLL_CON0.ctrl_start
    - Set DDRPHY_MDLL_CON0.ctrl_start to 1’b0.
    - Set DDRPHY_MDLL_CON0.ctrl_start to 1’b1.
    - Wait until DDRPHY_MDLL_CON1.ctrl_locked=1’b1.
35. DDRPHY SFR settings.
    - Set DDRPHY_LP_CON0.wck_enable=1’b1.
    - Set DDRPHY_LP_CON0.ctrl_scheduler_en=1’b1.
    - Set DDRPHY_LP_CON0.ctrl_dqs_drv_off=1’b1 if write link ECC is disabled.
    - Set DDRPHY_GNR_CON0.wdqs_oen_mode=1’b1.
36. Set DDRPHY wck_adj, rwck_adj, wckdur_adj, rwckdur_adj properly. Set gate/read settings properly.
37. Start DDRPHY initial training. Please refer to the following section for LPDDR5 training procedure.
38. Please set WCK_MODE_APB before memory normal operation.

If WCK always on mode is enabled, set DDRPHY_WCK2CKSYNC_CON0.WCK_MODE_APB=2’b1 and DDRPHY_SCHD_CMD_CON0.CAS_EN_APB=1’b0. If WCK always on mode is disabled, set DDRPHY_WCK2CKSYNC_CON0.WCK_MODE_APB=2’b0 and DDRPHY_SCHD_CMD_CON0.CAS_EN_APB=1’b1.

2.6.3 LPDDR4/4X Training Procedure

Please apply the following steps before memory initialization if training are required. Controller should not assert dfi_ctrlupd_req during training.

- Settings before training
    - Set DDRPHY_OFFSETD_CON0.upd_mode=1’b0 for PHY-initiated update mode.
    - Write current frequency to DDRPHY_DVFS_CON.freq_train
    - Initial Vref setting.
    - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=1’b1 to freeze DLL lock value during training for stability.
- Command bus training
- Apply one of the following DQS cleaning options.
    - Auto DQS clean mode
    - IO RCV Single-Ended mode
- Read DQ training
- Write DQ training

- Save the training result to read and save training registers for PHY power in/off scenario.
- Initial training at lower frequency if necessary.
- The PHY should start the periodic training to compensate DRAM voltage/temperature variation followed by periodic training guide.

2.6.4 LPDDR4/4X Command Bus Training

DDRPHY supports 2 command bus training modes for LPDDR4/4X. That is SW command bus training mode and HW command bus training mode.
Following steps are for SW command bus training mode.

- Change to low frequency (under 200MHz).
- Set DDRPHY_LP_CON0.ds_io_pd=1’b0.
- Apply DQS offset.
  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1’b1.
  - DDRPHY_WR_LVL_CON0.ctrl_wrlvl*_code=ck_offset (ck_offset=91ps/tFS, tFS: finedelay).
  - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Disable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1’b0.
- Controller should configure memory (LPDDR4/4X) in comman bus training mode. Issue MRW-1 command followed by MRW-2 command to set MR13 OP[0]=1’b1 (command bus training mode enabled).
- After tMRD, configure DDRPHY in command bus training mode.
  - Set DDRPHY_CAL_CON0.ca_cal_mode=1’b1.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=1’b1.
  - After tDQSCKE, set DDRPHY_CBT_CON3.cbt cke=2’b0.
- After tCKELCK, change CK frequency to the highest operating frequency.
- Configure CA Vref setting.
  - Set DDRPHY_CBT_CON0.cbt_ca_vref=CA Vref setting value(MR12 OP[6: 0]).
  - Set DDRPHY_CAL_CON3.wr_sw_mode=1’b1.
  - Set DDRPHY_WR_LVL_CON2.ctrl_dqs_shift=1’b1.
  - After tCAENT(20ns), set DDRPHY_CBT_CON0.cbt_vref_dq_en=1’b1 to drive CA vref setting value on DQ.
  - Wait until DDRPHY_CBT_CON5.cbt_tDSTRAIN+ DDRPHY_CBT_CON5.cbt_tDHTRAIN+6 DFI clock cycle.
  - Set DDRPHY_CBT_CON0.cbt_vref_dq_ en=1’b0.
  - Set DDRPHY_WR_LVL CON2.ctrl dqs shift=1’b0.
  - Set DDRPHY_CAL_CON3.wr_sw_mode=1’b0.
  - Wait for tVREF_LONG(250ns max).
  - Set DDRPHY_CBT_CON0.cbt_sw_mode=1’b1.
- Run command bus training (CA training/CS fine training) as followings.
  Following are function definition.

```
APB_READ(REG_NAME.field_name)
APB_WRITE(REG_NAME.field_name,VAL)
UPD_CODE{
APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync, 1b1)//Update code
APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync, 1 b0)//Update code
}
WAIT_UPD{
Wait(1us)
}
PATTERN_GEN (REG_NAME.field name){
APB_WRITE(REG_NAME.field_name, 1b1)
APB_WRITE(REG_NAME.field_name, 1b0)
}
PATTERN_CLEAR{
```

```
APB_WRITE(DDRPHY_CBT_CON3.cbt_cmd_clear, 1 b1)
APB_WRITE(DDRPHY_CBT_CON3.cbt_cmd_clear, 1'b0)
}
RD_FEEDBACK{
DQ_IO_RD=APB_READ(DDRPHY_DO_IO_RDATA0.DQ_IO_RD1)
}
Lock_value=APB_READ(DDRPHY_MDLL_CON1.ctrl_lock_value)
1. Apply CK/CS offset(OFFSET=91ps/tFS, tFS: finestep delay)
APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode, OFFSET)
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, OFFSET)
UPD_CODE
2. CA training
1) Searching CA_VWML[K] (k=0, 1.2...5)
for(search=’h0; search<’h2FF; search++){
APB_WRITE(CAkDeSkewCode, search)
UPD CODE
WAIT_UPD
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_ca_vwml)
RD_FEEDBACK
if(DDRPHY_DQ_IO_RD[K])!=1’b1){
CA_VWML[k]=search-1
break
}
}
2) Searching CA_VWMR[k](k=0, 1, 2..5)
for(search=’h0; search<‘h2FF; search++){
APB_WRITE(DDRPHY_CA_DESKEW_CON*.CAkDeSkewCode, search)
UPD_CODE
WAIT_UPD
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_ca_vwmr)
RD_FEEDBACK
if(DQ_IO RD[K]==1’b1){
CA_VWMR[K]= Lock_value-search
break
}
}
3) Calculation & Update(k=0, 1, 2…5)
if(CA_VWML[K]>CA_VWMR[K]){
CA_VWMC[K]=(CA_VWML[k]-CA_VWMR[k])/2
}
else { CA_VWMC[K]=’h0}
APB_WRITE(CAkDeSkewCode, CS_VWMC[k])
UPD_CODE
3. CS Fine training
1) Searching CS_VWML_FINE
for(search=’h0; search<’h2FF; search++){
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, search)
```

```
UPD_CODE
WAIT_UPD
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_cs_vwml_fine)
RD_FEEDBACK
if(DQ_IO_RD!=6'b111111){
CS_VWML_FINE=search-1
break
}
PATTERN CLEAR
}
2) Searching CS_VWMR_FINE
for(search='h0; search<'h2FF; search++){
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, search)
UPD_CODE
WAIT_UPD
PATTERN_GEN(DDRPHY_CBT_CON3.cbt_cmd_cs_vwmr_fine)
RD_FEEDBACK
    If(DQ_IO_RD==6'b111111){
CS_VWMR_FINE=Lock_value-search
break
}
        PATTERN_CLEAR
    }
3) Calculation & Update
if(CS_VWML_FINE>CS_VWMR FINE){
CS_VWMC_FINE=(CS_VWML_FINE-CS_VWMR_FINE)/2
}
else {
CS_VWMC_FINE='h0
}
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode, CS_VWMC_FINE)
UPD_CODE
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS1DeSkewCode, CS_VWMC_FINE)
UPD_CODE
```

If two ranks are used, CS1DeSkewCode should be applied by training result of CS0 (CS0DeSkewCode).

- Exit command bus training.
  - Set DDRPHY_CBT_CON3.cbt_cke= 2'b11
  - Wait for tCKEHDQS.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=1'b0.
  - Set DDRPHY_CAL_CON0.ca_cal_mode=1'b0.
  - Set DDRPHY_CBT_CON0.cbt_sw_mode=1'b0.
  - After tFC(20ns), memory controller should configure memory(LPDDR4/4X)in normal mode.

Following steps are for HW command bus training mode.

- Change to the low frequency (under 200MHz)
- Set DDRPHY_LP_CON0.ds_io_pd=1'b0.
- Set DDRPHY_CAL_CON0.ca_swap_mode_dis=1'b1.
- Apply DQS offset

  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1’b1
  - DDRPHY_WR_LVL_CON0.ctrl_wrlvl*_code =ck_offset(ck_offset=91ps/tFS, tFS: finedelay).
  - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Disable DDRPHY_OFFSETD_CON0.ctrl_ resync.
  - DDRPHY_CAL_CON3.wrlvl_sw_mode=1’b0.
- Controller should configure memory(LPDDR4/4X)in command bus training mode. Controller should issue MRW-1 command followed by MRW-2 command to set MR13 OP[0]=1’b1(command bus training mode enabled).
- After tMRD, configure DDRPHY in command bus training mode.
  - Enable DDRPHY_CAL CON0.ca_cal_mode.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en as 2’b01.
  - After tDQSCKE, set DDRPHY_CBT_CON2.cbt_cke as 2’b00.
- After tCKELCK, change CK frequency to the highest operating frequency.
- Configure CA Vref setting
  - Set CA Vref setting value(MR12 OP[6:0]) in DDRPHY_CBT_CON0.cbt_ca_vref.
  - Enable DDRPHY_CAL_CON3.wr_sw_mode.
  - Set DDRPHY_WR_LVL_CON2.ctrl_dqs_shift=1’b1.
  - After tCAENT(20ns), set DDRPHY_CBT_CON0.cbt_vref_dq_en as 2’b01 to drive CA vref setting value on DQ.
  - Wait until DDRPHY_CBT_CON5.cbt_tDSTRAIN+ DDRPHY_CBT_CON5.cbt_tDHTRAIN+6 DFI clock cycle.
  - Set DDRPHY_CBT_CON0.cbt_vref_dq_en as 2’b00.
  - Set DDRPHY_WR_LVL_CON2.ctrl_dqs_shift=1’b0.
  - Disable DDRPHY_CAL_CON3.wr_sw_mode.
  - Wait for tVREF_LONG(250ns max).
- Start CS/CA calibration.
  - Apply CK/CS offset.
    Enable DDRPHY_CBT_CON0.cbt_sw_mode.
    Set DDRPHY_CA_DESKEW_CON4.CKDeSkewCode=ck_offset(ck_offset=91ps/tFS, tFS: finedelay).
    Set DDRPHY_CA_DESKEW_CON5.CS0DeSkewCode=ck_offset(ck_offset=91ps/tFS, tFS: finedelay).
    Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
    Disable DDRPHY_OFFSETD_CON0.ctrl_resync.
    Disable DDRPHY_CBT_CON0.cbt_sw_mode.
  - Enable DDRPHY_LP_CON0.scheduler_HW_clock_gating_disable.
  - Enable DDRPHY_LP_CON0.ctrl_scheduler_en.
  - Enable DDRPHY_CBT_CON0.cbt_cs_coarse_dis.
  - Enable DDRPHY_CBT_CON3.cbt_hw_cal_start.
  - Wait until DDRPHY_CBT_CAL_STAT0.cbt_hw_cal_done.
  - Disbale DDRPHY_LP_CON0.ctrl_scheduler_en.
  - Disable DDRPHY_LP_CON0.scheduler_HW_clock_gating_disable.
- Exit command bus training.
  - Set DDRPHY_CBT_CON2.cbt_cke as 2’b11.
  - Wait for tCKEHDQS.
  - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en as 2’b00.
  - Set DDRPHY_CAL_CON0.ca_cal_mode to 1’b0.
  - Disable DDRPHY_CBT_CON3.cbt_hw_cal_start.
  - After tFC(20ns), memory controller should configure memory (LPDDR4/4X) in normal mode.

2.6.5 LPDDR4/4X DQS Clean Procedure

1. Auto DQS clean mode

The goal of auto DQS clean mode is to get valid read DQS without the gate training. Auto DQS clean mode can be used if VSSQ termination is enabled.

- Set DDRPHY_TESTIRCV_CON0.dqs0_testircv=4’h3, DDRPHY_TESTIRCV_CON0.dqs1_testircv=4’h3.

- Set DDRPHY_CAL_CON0.gate_cal_mode=1’b0.
- Enable DDRPHY_CAL_CON3.auto_dqs_clean.
- Set DDRPHY_CAL_CON2.ctrl_rodt_disable=1’b0.

2. DQS Clean Using IO RCV Single-Ended(SE) mode on VSSQ Termination(Mandatory under 2133Mbps)

The goal of DQS clean using IO RCV SE mode is to get valid read DQS without the gate training and auto dqs clean on VSSQ termination on. It is allowed under 2133Mbps and IO RCV SE mode and RCV ODT should be enabled.

2.6.6 LPDDR4/4X Read DQ Calibration

Read DQ calibration adjusts DQS and DQ delay to compensate the skew introduced by the package, board and on-chip to maximize the setup and hold timing margin.

- Configure DDRPHY training pattern registers in DDRPHY_CAL_RD_PATTERN_CON0.
  - Set rdtrn_inv_pattern_ds0=0xee, rdtrn_inv_pattern_ds1=0xee, rdtrn_rddata_pattern0=0x55 and rdtrn_rddata_pattern1=0x55.
  - Configure DDRPHY_OP_CODE_RDC registers for MR32, MR40, MR20 and MR15 such that the training pattern output from DRAM is the same as the training pattern defined above.
  - Configure MR32, MR40, MR25 and MR15 for read training pattern. OP_CODE_PATA=0x55(=rdtrn_rddata_pattern0), OP_CODE_PATB =0x55(=rdtrn_rddata_pattern1), OP_CODE_INVA=0xee(=rdtrn_inv_pattern_ds0), OP_CODE_INVB=0xee(=rdtrn_inv_pattern_ds1).
  - Rdtrn_inv_pattern should be the same per BYTE.
  - Based on the DDRPHY_OP_CODE* values, DDRPHY will send MRW for MR31, MR32, MR3 and MR34 to DRAM at the beginning of Read training.
- Configure DDRPHY in read training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_rdtrn_en=1’b1.
  - Set SCHD_TRAIN_CON0.phy_rdtrn_rank_en properly. For example, if phy_rdtrn_rank_en is set to 2’b11, per-rank read training will start from rank-0 to rank-1 sequentially. Any rank can be enabled for read training. For example, it is possible to set phy_rdtrn_rank_en= 2’b10.

Caution: For Read DQ's setup/hold margin maximization, read DQ delay should bigger than read DOS delay.

Caution: Pattern configuration is an example. Training pattern can be changed by user selection.

2.6.7 LPDDR4/4X Write DQ Calibration Initiated by DDRPHY

Write DQ calibration adjusts for the delays introduced by the memory (tDQS2DQ), package, board and on-chip that impact the write cycle.

Normal Initial Training Setting (533MHz or more)

- If data mask and DBI are all disabled at DRAM, set DDRPHY_CAL_CON0.wrtrn_dbi_cal_en=1’b0. Otherwise, set to 1’b1.
- If current frequency is equal or greater than 1066MHz
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtm_cyc_mode=0 (High frequency cycle based training mode).
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_th=0x1f.
- If current frequency is less than 1066MHz and equal to or greater than 533MHz, set DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtm_cyc_mode=1 (Low frequency cycle based training mode).
- Increase DDRPHY_CAL_CON4.num_repeat to make the initial training result stable.
- Set DDRPHY_CAL_CON4.wrtrn_multi_pattern to 1, to use more patterns during the initial training. Additional patterns should be defined in DDRPHY_CAL_WR_PATTERN2_CON0~4, DDRPHY_CAL_WR_PATTERN3_CON0~4, DDRPHY_CAL_WR_PATTERN4_CON0~4.
- DDRPHY_CAL_CON5.wrtm_cyc_mode should be 0 during normal operation.

Low Frequency Initial Training Setting (under 533MHz)-

- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0x1.
- Set DDRPHY_CAL_CON4.dvfs_wr_start_adj=0x0.
- Set DDRPHY_CAL_CON5.wrtm_cyc_en=0.
- After low frequency write training is done, apply the following setting.
  - Store the current lockvalue/4 value.
  - Store write training results from DDRPHY_WR_DESKEWC_CS*_CON*, DDRPHY_DM_DESKEWC_CS*_CON*.
  - Write (stored write training result values+lockvalue*2/4 value) to the following registers.
    - Enable DDRPHY_CAL_CON0.wr_cal_mode.
    - Enable DDRPHY_CAL_CON3.wr_sw_mode.
    - DDRPHY_SW_WR_DESKEWC_CS*_CON, DDRPHY_SW_DM_DESKEWC_CS*_CON*.
    - Disable DDRPHY_CAL_CON3.wr_sw_mode.
    - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
    - Disable DDRPHY_OFFSETD_CON0.ctrf_resync.
- Restore DVFS write training related setting for successful DVFS write training or other initial write training.
  - Set DDRPHY_CAL_CON4.dvfs_wr_slart_adj=0xf.
  - Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0.

Common Setting for Write Training

- Set write training paltem
  - DQ pattern in DDRPHY_CAL_WR_PATTERN1_CON0~ DDRPHY_CAL_WR_PATTERN1_CON3.
- Set wrtrn_rddata_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtm_rddata_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtm_rddata_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtm_rddata_adj_w2_bst9_16 for BL13-BL14 pattern.
- Set wrtrn_rddata_adj_w3_bst9_16 for BL15~BL16 pattern.
- Set write DM pattern in CAL_WR_PATTERN1_CON4.
- Set wrtrn_rddata_dm_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtrn_rddata_dm_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst9_16 for BL13~BL14 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst9_16 for BL15~BL16 pattern.
- Configure DDRPHY in write training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_en=1.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_rank_en properly.
  - For example, if phy_wrtrn_rank_en is set to 0x3, per-rank write training will start from rank0 to rank1 sequentially.

2.6.8 LPDDR4/4X Periodic Training

Periodic training using PHY master interface

Periodic write training compensates write center shift and gate shift caused by VT variation in memory. Initial training should be completed before periodic training. During periodic training, DDRPHY uses the PHY master interface and generates MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. Periodic write training will be excuted in sequence.

- The common parameter is same as initial training.
- Enable periodic gate training properly (refer to SFR description)
  - Set DDRPHY_SCHD_TRAIN_CON0.periodic_gttrn_en and if use DVFS, set

DDRPHY_DVFS0_TRAIN_CON0.dvfs0_periodic gttrn_en and
DDRPHY_DVFS1_TRAIN_CON0.dvfs1_periodic_gttrn_en.

- Enable periodic write training properly. Mandatory up to 2133Mbps.
  - Set DDRPHY_SCHD_TRAIN_CON0.periodic_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_TRAIN_CON0.dvfs0_periodic_wrtrn_en and DDRPHY_DVFS1_TRAIN_CON0.dvfs1_periodic_wrtrn_en.
- Set DDRPHY_SCHD_TRAIN_CON1.periodic_time.
  - Interval of periodic training = periodic_time*tCK_osc (oscillator dock).
- Set DDRPHY_SCHD_TRAIN_CON1.periodic_en =1 and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_periodic_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_periodic_en properly.
- Set DDRPHY_SCHD_TRAIN_CON1.periodic en = 0 for disable periodic training and if use DVFS, set
  DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_periodic_en and
  DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_periodic_en properly.

DVFS training using PHY master interface

DVFS training compensates write center shift and gate shift caused by VT variation in memory. Initial write/gate training should be completed before DVFS training. During DVFS training, DDRPHY uses the PHY master interface and generates MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. DVFS training will be executed in sequence.

- The common parameter is same as initial training.
- Enable DVFS gate training properly
  - Set DDRPHY_SCHD_TRAIN_CON0.dvfs_gttrn_en and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_dvfs_gttrn_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_dvfs_gttrn_en.
- Enable DVFS write training properly.
  Set DDRPHY_SCHD_TRAIN_CON0.dvfs_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_dvfs_wrtrn_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_dvfs_wrtrn_en.
- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=1(DVFS mode).

2.6.9 LPDDR5 Training Procedure

- Settings before training.
  - Set DDRPHY_OFFSETD_CON0.upd_mode=0 for PHY-initiated update mode.
  - Write the current frequency to DDRPHY_DVFS_CON.freq_train.
  - Initial Vref setting.
  - Set DDRPHY_MDLL_CON1.clkm_cg_en_sw=1 to freeze DLL lock value during training for stability.

Before DRAM interface training, training setting should be configured properly.

- LP5 SW CBT (command bus training)
- Auto DQS clean
- Read Calibration
- Write DQ Calibration

To set DDRPHY training under 1600Mbps at MODE4/3, under 1067Mbps at MODE2, DDRPHY training need WCK2CK sync always on mode and DDRPHY_WCK2CKSYNC_CON0.ctrl_WCK_MODE_APB=1. So please follow the DDRPHY training procedure below.

Set MR18 OP[4]=0(always on disable), CAS_EN=1, WCK_MODE=0 ==> CBT/WCK2CK leveling(if needed) ==> set MR18 OP[4]=1(always on), CAS_EN=0,WCK_MODE=1 ==> Send CAS command to memory ==> set dfi_wck_en always 1 ==> DDRPHY training except CBT, WCK2CK leveling (if needed) ==> User choice for WCK2CK sync operation (if use wck2ck sync always on, please keep it or if not, set MR18 OP[4]=0(always on disable), CAS_EN=1,WCK_MODE=0 ==>Do normal transactions.

After training setting is done, apply the following sequence.

- Configure common parameter training properly.

  - Set DDRPHY_SCHD_TIME_CON0.phy_t_rddata_en='d6.
  - Set DDRPHY_SCHD_TIME_CON0.WL to match it with DRAM WL setting.
  - Set DDRPHY_SCHD_TIME_CON1.tCCD=0x8(LPDDR5).
  - Set DDRPHY_SCHD_TIME_CON1.tWTR=0x1f.
  - If WCK always on disable, set DDRPHY_WCK2CKSYNC_CON0.ctrl_WCK_MODE_APB=0x0 and DDRPHY_SCHD_CMD_CON0.CAS_EN_APB=0x1.
  - If WCK always on, set WCK2CKSYNC_CON0.ctrl_WCK_MODE_APB=0x1 and SCHD_CMD_CON0.CAS_EN_APB=0x0.
  - WCK should be driven by memory controller at WCK always on mode.
- Set MR operand code same as setting on memory.
  - For LPDDR5, DDRPHY_LP5_MR_OP.
- Enable DDRPHY training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_train_en=0x1.
- Wait until SCHD_TRAIN_CON0.phy_train_done=0x1.
- Disable DDRPHY training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_train_en=0x0.
- Setting after training.
  - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=0 to enable DLL locking.
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_mode=0 during normal operation.
  - Set DDRPHY_CAL_CON0.cal_vtc_en=1 to compensate voltage, temperature variation on calibration results.
  - Set DDRPHY_CAL_CON0.dvfs_wr_train_en=1 initial write training (Write training with dfi_lvl_periodic=0) will be interpreted as DVFS write training afterwards.
- Update DDRPHY DLL
  - Enable DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Disable DDRPHY_OFFSETD_CON0.ctrl_resync.
- The DDRPHY should start the periodic training to compensate DRAM voltage/temperature variation followed by periodic training guide.
  - Write periodic training.

2.6.10 LPDDR5 Command Bus Training

LPDDR5 only supports SW command bus training mode. LPDDR5 SW command bus training supports CA bit de-skewing function. The overall sequence is CA left edge searching-CA right edge searching-Calculation center code of CA. Because LPDDR5 CA is DDR (CA is captured at CK rising edge and falling edge), the edge should be searched with changing CBT-PH mode. **Setting before Training**

- Before CBT training start, check if MR13 OP[6]=1 for CBT mode2.
- Set DDRPHY_SCHD_CMD_CON0.RANK_SEL=cs.
- Set DDRPHY_CBT_CON2.cbt_dqdm_sel=0x80.
- Set DDRPHY_CBT_CON0.cbt_sw_mode=0x1.
- Set DDRPHY_CBT_CON2.cbt_tWCK2DQ7 satisfying memory timing parameter tWCK2DQ7H.
- Set DDRPHY_CBT_CON2.cbt_tDSTRAIN_LP5 satisfying memory timing parameter tDStrain.

CA Left Edge Searching with CBT-PH[7]=1'b0

- Entering CBT Mode
  - Configure the memory entering CBT mode.
    - Set DDRPHY_SCHD_CON0.scheduler_sw_mode=0x1.
    - Set DDRPHY_CAL_CON0.ca_cal_mode=0x1.
    - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=0x1.
    - Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable=0x1.
    - Set DDRPHY_SCHD_CMD_CON2.MA_CODE=0x10.
    - Set DDRPHY_SCHD_CMD_CON2.OP_CODE=0x10.
    - Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.
  - Configure the PHY entering CBT mode.
    - Set DDRPHY_CBT_CON0.cbt_vref_dq_en=0x1.

- ◆ Set DDRPHY_CBT_CON2.cbt_start=0x1.
- ◆ Wait for tDQ7HWCK+tDQ72DQ (255ns).
- ◆ Set DDRPHY_CBT_CON2.cbt_wck_en=0x1.
- ◆ Toggle DDRPHY_CBT_CON2.cbt_vref_set_en.
- ◆ Set DDRPHY_CBT_CON2.cbt_dq_rcv_en=0x1.
- ◆ Set DDRPHY_CBT_CON3.cbt_en=0x1.
- ◆ Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.

- Searching CA Left edge as followings.

```
APB_READ (REG_NAME[bit])
APB_WRITE (REG_NAME[bit],VAL)
UPD_CODE {
    APB_WRITE (DDRPHY_OFFSETD_CON0.ctrl_resync, 1'b1)
    APB_WRITE (DDRPHY_OFFSETD_CON0.ctrl_resync, 1'b0)
}
WAIT_UPD {
     Wait(1us)
}
PATTERN_GEN_1 {
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_1, cs)
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_2, 0x0)
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CMD_1, {13'h0, ca, 1'h0,
     ~ca})
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD1. DIRECT_CMD_2, {13'h0, ~ca, 1'h0,
     ~ca})
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD0.DIRECT_EN_APB, 1'b1)
     Wait(1ns)
     APB_WRITE (DDRPHY_SCHD_DIRECT_CMD0.DIRECT_EN_APB, 1'b0)
}
RD_FEEDBACK {
    DQ_IO_RD = APB_READ (REG_NAME.field_name)
}
if(DDRPHY_CLKMODE_CON == 2)
offset =APB_READ (DDRPHY_MDLL_CON1.ctrl_lock_value)/2
if (DDRPHY_CLKMODE_CON == 4)
offset = APB_READ (DDRPHY_MDLL_CON1.ctrl_lock_value)
1. Apply CK offset and CS offset
APB_WRITE (DDRPHY_CA_DESKEW_CON4.CKDeSkewCode, offset)
APB_WRITE (DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode, offset)
UPD_CODE
2. Searching CA left edge CA_VWML[k] (k = 0, 1, 2...6)
for(search='h0; search < 'h2FF; search++) {
    APB_WRITE (CAkDeSkewCode, search)
    UPD_CODE
    WAIT_UPD
    PATTERN_GEN
    RD_FEEDBACK
    if (DQ_IO_RD[k]!=1'b1) {
        CA_VWML[k] = search-1
```

```
        break
        }
    }
    3. Rollback the CK offset and CS offset
    APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode,0x0).
    APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode,0x0).
    UPD_CODE
```

- Exiting CBT mode
  - Configure the DDRPHY exiting CBT mode
    - Set DDRPHY_CBT_CON3.cbt_en = 0x0
    - Togole DDRPHY_OFFSETD_CON0.ctrl_resync
    - Set DDRPHY_CBT_CON2.cbt_start =0x0
    - Set DDRPHY_CBT CON2.cbt_dq_rcv_en=0x0
    - WAIT for tDQ7LWCK + 10tCK
    - Set DDRPHY_CBT_CON2.cbt_wck_en=0x0
    - Wait tXCBT
  - Configure the memory exiting CBT mode.
    - Set DDRPHY_SCHD_CMD_CON2.MA_CODE=0x10.
    - Set DDRPHY_SCHD_CMD_CON2.OP_CODE = 0x00.
    - Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.
    - Set DDRPHY_CBT_CON0.cbt_vref_dq_en = 0x0.
    - Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable = 0x0.
    - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en = 0x0.
    - Toggle DDRPHY_CBT_CON2.cbt_vref_pre_en.
    - Set DDRPHY_CAL_CON0.ca_cal_mode =0x0.
    - Set DDRPHY_SCHD_CON0.scheduler_sw_mode =0x0.

CA Right Edge Searching with CBT-PH[7] = 1’b1

- Entering CBT Mode
  - Configure the memory entering CBT mode.
    - Set DDRPHY_SCHD_CON0.scheduler_sw_mode = 0x1.
    - Set DDRPHY_CAL CON0.ca_cal_mode = 0x1.
    - Set DDRPHY_CBT_CON0.cbt_vref_dqs_en = 0x1.
    - Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable = 0x1.
    - Set DDRPHY_SCHD_CMD_CON2.MA_CODE= 0x10.
    - Set DDRPHY_SCHD_CMD_CON2.OP_CODE= 0x90.
    - Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.
  - Configure the DDRPHY entering CBT mode.
    - Set DDRPHY_CBT_CON0.cbt_vref_dq_en=0x1.
    - Set DDRPHY_CBT_CON2.cbt_start =0x1.
    - Wait for tDQ7HWCK +tDQ72DQ(255ns).
    - Set DDRPHY_CBT_CON2.cbt_wck_en =0x1.
    - Toggle DDRPHY_CBT_CON2.cbt_vref_set_en.
    - Set DDRPHY_CBT_CON2.cbt_dq_rcv_en = 0x1.
    - Set DDRPHY_CBT_CON3.cbt_en = 0x1.
    - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.
- Searching CA Right edge as followings.

```
APB_READ(REG_NAME[bit])
APB_WRITE(REG_NAME[bit],VAL)
UPD_CODE {
    APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync,1’b1)
    APB_WRITE(DDRPHY_OFFSETD_CON0.ctrl_resync,1’b0)
}
WAIT_UPD {
    Wait(1us)
```

```
}
PATTERN_GEN_1 {
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_1,cs)
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CS_2,0x0)
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CMD_1,{13'h0, ca, 1'b0, ~ca})
    APB_WRITE(DDRPHY_SCHD_DIRECT_CMD1.DIRECT_CMD_2,{13'h0, ~ca, 1'b0, ca})
}
RD_FEEDBACK {
    DQ_IO_RD=APB_READ(REG_NAME.field_name)
}
if(CLKMODE_CON == 2)
    offset=APB_READ(DDRPHY_MDLL_CON1.ctrl_lock_value)/2
if(CLKMODE_CON == 4)
    offset=APB_READ(DDRPHY_MDLL_CON1.ctrl_lock_value)
1. Apply CK offset and CS offset.
APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode, offset)
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode, offset)
UPD_CODE
2. Searching CA left edge CA_VWMR[k](k=0, 1, 2…6)
for(search='h0;search<'h2ff;search++){
    APB_WRITE(CAkDeSkewCode, search)
    UPD_CODE
    WAIT_UPD
    PATTERN_GEN
    RD_FEEDBACK
    if(DQ_IO_RD[k]==1'b1){
        CA_VWMR[k]=search-1
        break
        }
}
3. Rollback the CK offset and CS offset.
APB_WRITE(DDRPHY_CA_DESKEW_CON4.CKDeSkewCode,0x0)
APB_WRITE(DDRPHY_CA_DESKEW_CON5.CS*DeSkewCode,0x0)
UPD_CODE
```

- Exiting CBT Mode
  - Configure the DDRPHY exiting CBT mode.
    - Set DDRPHY_CBT_CON3.cbt_en=0x0.
    - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.
    - Set DDRPHY_CBT_CON2.cbt_start=0x0.
    - Set DDRPHY_CBT_CON2.cbt_dq_rcv_en=0x0.
    - WAIT for tDQ7LWCK.
    - Set DDRPHY_CBT_CON2.cbt_wck_en=0x0.
    - Wait tXCBT.
  - Configure the memory exiting CBT mode.
    - Set DDRPHY_SCHD_CMD_CON2.MA_CODE=0x10.
    - Set DDRPHY_SCHD_CMD_CON2.OP_CODE=0x00.
    - Toggle DDRPHY_SCHD_DIRECT_CMD3.CMD_MWR_req.
    - Set DDRPHY_CBT_CON0.cbt_vref_dq_en=0x0.
    - Set DDRPHY_WCK2CKSYNC_CON0.wck_out_enable=0x0.

- Set DDRPHY_CBT_CON0.cbt_vref_dqs_en=0x0.
- Toggle DDRPHY_CBT_CON2.cbt_vref_pre_en.
- Set DDRPHY_CAL_CON0.ca_cal_mode=0x0.
- Set DDRPHY_SCHD_CON0.scheduler_sw_mode=0x0.

Calculation of CA Center Code

- MODE2
  - CA_VWMR_TMP[k]=Lock_value – CA_VWMR[k](k=0,1,2…6)
  - If CA_VWML[k]>=CA_VWMR_TMP[k], CA_VWMC[k]=(CA_VWML[k]-CA_VWMR_TMP[k])/2+Lock_value/2
  - Else, CA_VWMC[k]=Lock_value/2-((CA_VWMR_TMP[k]-CA_VWML[k])/2)
- MODE4
  - CA_VWMR_TMP[k]=2*Lock_value-CA_VWMR[k](k=0,1,2…6).
  - If CA_VWML[k]>=CA_VWMR_TMP[k], CA_VWMC[k]=(CA_VWML[k]-CA_VWMR_TMP[k])/2+Lock_value.
  - Else, CA_VWMC[k]=Lock_value-((CA_VWMR_TMP[k]-CA_VWML[k])/2).
- Update CA center code on
  - Write DDRPHY_CA_DESKEW_CON0~2.CAkDeSkewCode as CA_VWMC[k].
  - Set DDRPHY_CBT_CON3.cbt_en=0x1.
  - Toggle DDRPHY_OFFSETD_CON0.ctrl_resync.
  - Set DDRPHY_CBT_CON0.cbt_sw_mode=0x0.

2.6.11 LPDDR5 DQS Clean Procedure

Auto DQS Clean (Mandatory above 3200Mbps)

The goal of auto DQS clean mode is to get valid read DQS without the gate training. Auto DQS clean mode can be used if VSSQ termination is enabled.

- Set DDRPHY_TESTIRCV_CON0.dqs0_testircv=0x3, DDRPHY_TESTIRCV_CON0.dqs1_testircv=0x3.
- Set DDRPHY_CAL_CON0.gate_cal_mode=0x0.
- Enable DDRPHY_CAL_CON3.auto_dqs_clean.
- Set DDRPHY_CAL_CON2.ctrl_rodt_disable=0x0.

If auto DQS clean mode is enabled, RL should be minimum RL of below table or more. The memory post_amble duration should be 4.5tWCK static and preamble duration should be 2tWCK static, 2tWCK toggle or 4tWCK static.

Table 2-5 Minimum Read Latency for LPDDR5 Auto DQS Clean Enable

PHY mode	0	1	2	3	4
Memory Type	LPDDR4/4X		LPDDR5		
Min Read Latency w/Auto DQS Enable	28CK	24CK	14CK (28 WCK)	9CK (36 WCK)	9CK (36 WCK)

DQS Clean Using IO RCV Single-Ended (SE) Mode on VSSQ Termination (Mandatory under 3200Mbps)

The goal of DQS clean using IO RCV SE mode is to get valid read DQS without the gate training and auto dqs clean on VSSQ termination ON. It is allowed under 3200Mbps and IO RCV SE MODE and RCV ODT should be enabled.

2.6.12 LPDDR5 Read DQ Calibration

Read Calibration adjusts DQS and DQ delay to compensate the skew introduced by the package, board and on-chip to maximize the setup and hold timing margin.

- Configure PHY training pattern registers in CAL_RD_PATTERN_CON0
  - Set rdtrn_inv_pattern_ds0=0xee, rdtrn_inv_pattern_ds1=0xee, rdtrn_rddata_pattern0=0x55 and rdtrn_rddata_pattern1=0x55.
  - Configure DDRPHY_OP_CODE_RDC registers for MR31, MR32, MR33 and MR34 such that the training pattern output from DRAM is the same as the training pattern defined above.
  - Configure MR31, MR32, MR33 and MR34 for read training pattern.
    - OP_CODE_PATA=0x55(rdtrn_rddata_pattern0), OP_CODE_PATB=0x55(rdtrn_rddata_pattern1), OP_CODE_INVA=0xee(rdtrn_inv_pattern_ds0), OP_CODE_INVB=0xee(rdtrn_inv_pattern_ds1).

- Rdtrn_inv_pattern should be the same per BYTE.
- Based on the OP_CODE_* values, PHY will send MRW for MR31, MR32, MR33 and MR34 to DRAM at the beginning of read training.

- Configure DDRPHY and memory in link ECC mode, if link ECC is enabled.
  - Configure memory in link ECC mode.
    - Issue MR3 command to set DBI-WR enabled and DBI-RD disabled.
    - Issue MR22 command to enable link ECC mode.
  - Configure DDRPHY in link ECC mode.
    - Set DDRPHY_CAL_CON0.rdtrn_dbi_cal_en =0x1.
    - Set DDRPHY_CAL CON3.ctrl_link_ecc_mode=0x1.
- Configure DDRPHY in read training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_rdtrn_en=1
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_rdtrn_rank_en properly.
    - For example, if phy_rdtrn_rank_en is set to 2’b11, per-rank read training will start from rank0 to rank1 sequentially.
    - Any rank can be enabled for read training. For example, it is possible to set phy_rdtrn_rank_en=2’b10.

2.6.13 LPDDR5 Write DQ Calibration

Normal Initial Training Setting (533MHz or More)

- If data mask and DBI are all disabled at DRAM, set DDRPHY_CAL_CON0.wrtrn_dbi_cal_en=0. Otherwise set to 1.
- Configure DDRPHY and memory in link ECC mode if link ECC is enabled.
  - Configure memory in link ECC mode.
    - Issue MR3 command to set DBI-WR enabled and DBI-RD disabled.
    - Issue MR22 command to enable link ECC mode.
  - Configure DDRPHY in link ECC mode.
    Set DDRPHY_CAL_CON0.wrtrn_dbi_cal_en=0x1.
    Set DDRPHY_CAL_CON3.ctrl_link_ecc_mode=0x1.
- If current frequency is equal to or greater than 1066MHz
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtrn_cyc_mode=0(High frequency cycle based training mode).
  - Set DDRPHY_CAL_CON5.wrtrn_cyc_th=31(LPDDR5).
  - If PRBS write training is to be enabled after write training is done
    - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=1
    - Read DDRPHY_MDLL_CON1.ctrl_lock_value
    - Set DDRPHY_CAL_CON5.wrtrn_cyc_th=ctrl_lock_value/4
    - Set DDRPHY_MDLL_CON0.clkm_cg_en_sw=0
- If current frequency is less than 1066MHz and equal to or greater than 533MHz, set DDRPHY_CAL_CON5.wrtrn_cyc_en=1 and DDRPHY_CAL_CON5.wrtrn_cyc_mode=1(Low frequency cycle based training mode).
- Increase DDRPHY_CAL_CON4.num_repeat to make the initial training result stable.
- Set DDRPHY_CAL_CON4.wrtrn_multi_pattern to 1 to use more patterns during the initial training. Additional patterns should be defined in DDRPHY_CAL_WR_PATTERN2_CON0~4, DDRPHY_CAL_WR_PATTERN3_CON0~4, DDRPHY_CAL_WR_PATTERN4_CON0~4.
- DDRPHY_CAL_CON5.wrtrn_cyc_mode should be 0 during normal operation.

Low Frequency Initial Training Setting (under 533MHz)

- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0x1.
- Set DDRPHY_CAL_CON4.dvfs_wr_start_adj=0x0.
- Set DDRPHY_CAL_CON5.wrtrn_cyc_en=0.
- After low frequency write training is done, apply the following setting.
  - Store the current lockvalue/4 value.
  - Store write training results from DDRPHY_WR_DESKEWC_CS*_CON*, DDRPHY_DM_DESKEWC_CS*_CON*, DDRPHY_ECC_DESKEWC_CS*_CON*.
  - Write (stored write training result values + lockvalue/4) to the following register.
    - Enable DDRPHY_CAL_CON0.wr_cal_mode.
    - Enable DDRPHY_CAL_CON3.wr_sw_mode.

- DDRPHY_SW_WR_DESKEWC_CS*_CON, DDRPHY_SW_DM_DESKEWC_CS*_CON*, DDRPHY_SW_ECC_DESKEWC_CS*_CON*.
- Disable DDRPHY_CAL_CON3.wr_sw_mode.
- Restore DVFS write training related setting for successful DVFS write training or other initial write training.
  - Set DDRPHY_CAL_CON4.dvfs_wr_start_adj=0xf.
  - Set DDRPHY_CAL_CON0.dvfs_wr_train_en=0.

Common Setting for Write Training

- Set write training paltem
  - DQ pattern in DDRPHY_CAL_WR_PATTERN1_CON0~ DDRPHY_CAL_WR_PATTERN1_CON3.
- Set wrtrn_rddata_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtm_rddata_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtm_rddata_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtm_rddata_adj_w2_bst9_16 for BL13-BL14 pattern.
- Set wrtrn_rddata_adj_w3_bst9_16 for BL15~BL16 pattern.
- Set write DM pattern in DDRPHY_CAL_WR_PATTERN1_CON4.
- Set wrtrn_rddata_dm_adj_w0_bst1_8 for BL1~BL2 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst1_8 for BL3~BL4 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst1_8 for BL5~BL6 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst1_8 for BL7~BL8 pattern.
- Set wrtrn_rddata_dm_adj_w0_bst9_16 for BL9~BL10 pattern.
- Set wrtrn_rddata_dm_adj_w1_bst9_16 for BL11~BL12 pattern.
- Set wrtrn_rddata_dm_adj_w2_bst9_16 for BL13~BL14 pattern.
- Set wrtrn_rddata_dm_adj_w3_bst9_16 for BL15~BL16 pattern.
- Configure DDRPHY in write training mode.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_en=1.
  - Set DDRPHY_SCHD_TRAIN_CON0.phy_wrtrn_rank_en properly.
  - For example, if phy_wrtrn_rank_en is set to 0x3, per-rank write training will start from rank0 to rank1 sequentially.

2.6.14 LPDDR5 Periodic Training

Periodic training compensates write center shift and gate shift caused by VT variation in memory. Initial write/gate training should be completed before periodic training. During periodic training, DDRPHY uses the PHY master interface and generates RDC/WFF/RFF/MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. Periodic training will be excuted in sequence.

- The common parameter is same as initial training.
- Enable periodic write training properly (refer to SFR description)
  - Set DDRPHY_SCHD_TRAIN_CON0.periodic_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_TRAIN_CON0.dvfs0_periodic_wrtrn_en and DDRPHY_DVFS1_TRAIN_CON0.dvfs1_periodic_wrtrn_en.
- Set DDRPHY_SCHD_TRAIN_CON1.periodic_time.
  - Interval of periodic training = periodic_time*tCK_osc (oscillator clock).
- Set DDRPHY_SCHD_TRAIN_CON1/ DDRPHY_DVFS*_SCHD_TIME_CON3.periodic_en =1 and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_periodic_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_periodic_en properly.

2.6.15 LPDDR5 DVFS Training

DVFS training compensates write center shift and gate shift caused by VT variation in memory. Initial write/gate training should be completed before DVFS training. During DVFS training, DDRPHY uses the PHY master interface and generates RDC/WFF/RFF/MPC commands without the memory controller. When DDRPHY request PHY master mode, the controller should place the DRAM in self refresh and assert dfi_phymstr_ack. DVFS training will be executed in sequence.

- The common parameter is same as initial training.
- Enable DVFS write training properly.
  - Set DDRPHY_SCHD_TRAIN_CON0.dvfs_wrtrn_en and if use DVFS, set DDRPHY_DVFS0_SCHD_TIME_CON3.dvfs0_dvfs_wrtrn_en and DDRPHY_DVFS1_SCHD_TIME_CON3.dvfs1_dvfs_wrtrn_en.
- Set DDRPHY_CAL_CON0.dvfs_wr_train_en=1(DVFS mode).

Chapter 3 Mobile Storage Host Controller

3.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD-max version 3.01) with 1 bits or 4 bits data width, Multimedia Card(MMC-max version 4.51) with 1 bits or 4 bits or 8 bits data width.
The Host Controller is instantiated for SDMMC, SDIO. The interface difference between these instances is shown in “Interface Description”.
The Host Controller supports following features:

- Bus Interface Features:
  - Support AMBA AHB interface for master and slave
  - Supports internal DMA interface(IDMAC)
    - Supports 16/32-bit data transfers
    - Single engine used for Transmit and Receive, which are mutually exclusive
    - Dual-buffer and chained descriptor linked list
    - Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
    - Programmable burst size for optimal host bus utilization
  - Support combined single FIFO for both transmit and receive operations
  - Support FIFO size of 256x32
  - Support FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
  - Support Secure Digital memory protocol commands
  - Support Secure Digital I/O protocol commands
  - Support Multimedia Card protocol commands
  - Support Command Completion Signal and interrupts to host
  - Support CRC generation and error detection
  - Support programmable baud rate
  - Support power management and power switch
  - Support card detection
  - Support write protection
  - Support hardware reset
  - Support SDIO interrupts in 1-bit and 4-bit modes
  - Support 4-bit mode in SDIO3.0
  - Support SDIO suspend and resume operation
  - Support SDIO read wait
  - Support block size of 1 to 65,535 bytes
  - Support 1-bit, 4-bit modes
- Clock Interface Features:
  - Support 0/90/180/270-degree phase shift operation for sample clock (cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock(cclk_in) respectively
  - Support phase tuning using delay line for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock (cclk_in) respectively. The max number of delay element number is 256

3.2 Block Diagram

The Host Controller consists of the following main functional blocks.

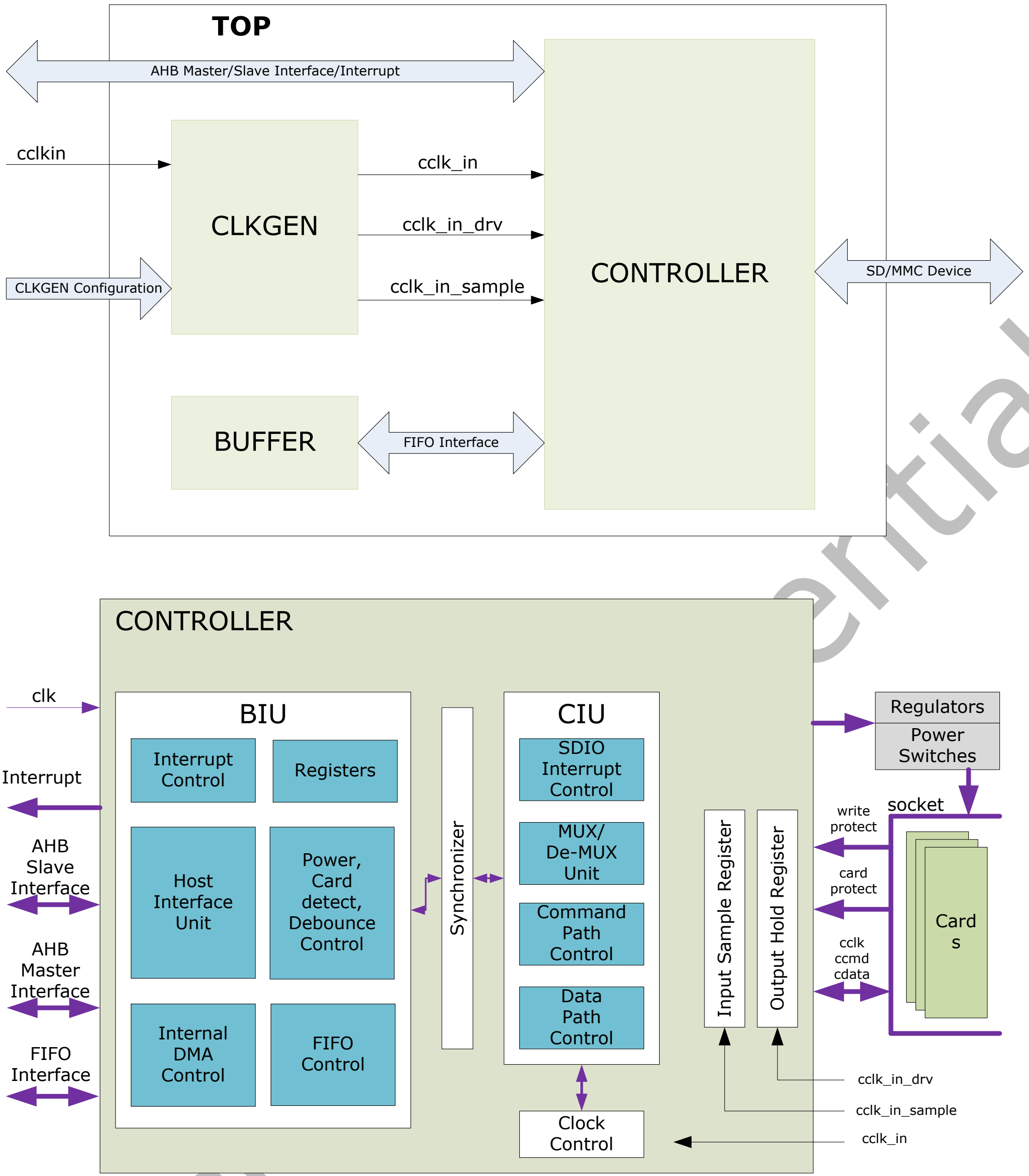


Fig. 3-1 Mobile Storage Host Control Block Diagram

- Clock Generate Unit (CLKGEN): Generates card interface clock cclk_in/ cclk_sample/cclk_drv based on cclkin and configuration information.
  - cclkin: original clock
  - cclk_in: functional clock
  - cclk_sample: sample clock
  - cclk_drv: driver clock
- Asynchronous dual-port memory (BUFFER): Use a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the other port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/write.
- Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

3.3 Function Description

3.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access

- Power control and card detection

3.3.1.1 Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus.

3.3.1.2 Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.
All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the SDMMC_CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.
Once a command start is issued by setting the start_bit of the SDMMC_CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- SDMMC_CMD – Command
- SDMMC_CMDARG – Command Argument
- SDMMC_BYTCNT – Byte Count
- SDMMC_BLKSIZ – Block Size
- SDMMC_CLKDIV – Clock Divider
- SDMMC_CLKENA – Clock Enable
- SDMMC_CLKSRC – Clock Source
- SDMMC_TMOUT – Timeout
- SDMMC_CTYPE – Card Type

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.
When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:
3 (clk) + 3 (cclk_in)
Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

- If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.
- If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the SDMMC_CMD register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.
- If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

3.3.1.3 Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw interrupt status, the interrupt-mask register, and the global interrupt-enable register bit. Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw interrupt status register SDMMC_RINTSTS. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.
The interrupt port is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.
The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32’h0, which masks all the interrupts.
Notes:

Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.
The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 3-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0.
16	Card no-busy	If card exit busy status, the interrupt happened.
15	End Bit Error (read) / Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC received during write operation. For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt. Recommendation: Software typically need not enable this for non CE-ATA accesses; Data Transfer Over (DTO) interrupt that comes after this interrupt determines whether data transfer has correctly competed.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if DAT[0] line indicates start bit-that is, 0-and any of the other data bits do not have start bit, then this error is set. Busy Complete Interrupt when data is written to the card. This interrupt is generated after completion of busy driven by the card after the last data block is written into the card.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically this should not happen, except due to error in software. Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty. If IDMAC is enabled, FIFO under-run/over-run can occur due to a programming error on MSIZE and watermark values in SDMMC_FIFOTH register.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period.

Bits	Interrupt	Description
		Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on command signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	In Normal functioning mode: Data read timeout (DRTO) Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs. In Boot Mode: Boot Data Start (BDS) When set, indicates that Host Controller has started to receive boot data from the card. A write to this register with a value of 1 clears this interrupt.
8	Response Timeout (RTO)	In normal functioning mode: Response timeout (RTO) Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller. In Boot Mode: Boot Ack Received (BAR) When expect_boot_ack is set, on reception of a boot acknowledge pattern—0-1-0—this interrupt is asserted. A write to this register with a value of 1 clears this interrupt.
7	Data CRC Error (DCRC)	Received Data CRC does not match with locally-generated CRC in CIU. Can also occur if the Write CRC status is incorrectly sampled by the Host.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: pop RX_WMark + 1 data from FIFO.

4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level.
		Recommendation:
		In DMA modes, this interrupt should not be enabled.
		In non-DMA mode:
		if (pending_bytes > (FIFO_DEPTH - TX_WMark))
		        push (FIFO_DEPTH - TX_WMark) data into FIFO
		else
		        push pending_bytes data into FIFO

3	Data Transfer Over (DTO)	Indicates Data transfer completed. Though on detection of errors-Start Bit Error, Data CRC error, and so on, DTO may or may not be set; the application must issue CMD12, which ensures that DTO is set. Recommendation:

Bits	Interrupt	Description
		In non-DMA mode, when data is read from card, on seeing interrupt, host should read any pending data from FIFO. In DMA mode, DMA controllers guarantee FIFO is flushed before interrupt. DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.
2	Command Done(CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs.
1	Response Error (RE)	Error in received response set if one of following occurs: ● Transmission bit != 0 ● Command index mismatch ● End-bit != 1
0	Card-Detect (CDT)	When one or more cards inserted or removed, this interrupt occurs. Software should read card-detect register to determine current card status. Recommendation: After power-on and before enabling interrupts, software should read card detect register and store it in memory. When interrupt occurs, it should read card detect register and compare it with value stored in memory to determine which card(s) were removed/inserted. Before exiting ISR, software should update memory with new card-detect value.

3.3.1.4 FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.
The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock(clk), and the second port is connected to the card clock(cclk_in).

Notes: The FIFO controller does not support simultaneous read/write access from the same port. For debugging purposes, the software may try to write into the FIFO and read back the data; results are indeterminate, since the design does not support read/write access from the same port.

3.3.1.5 Card Detection Unit

The register unit has registers that control the power. Power to each card can be selectively turned on or off.
The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounce associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value.

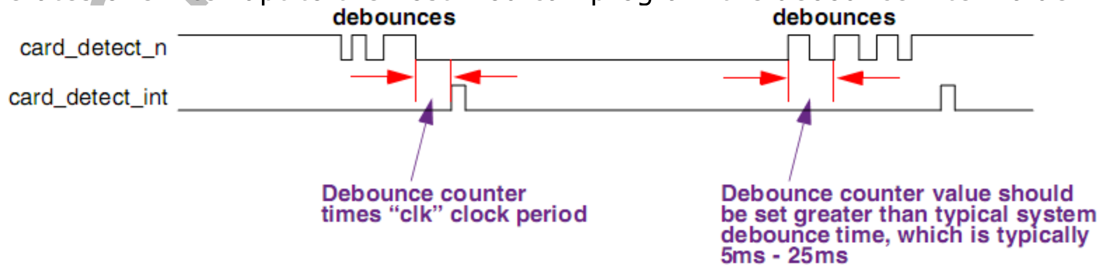


Fig. 3-2 SD/MMC Card-Detect Signal

3.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the external devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.
The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data transfer is in progress, the software must set the stop_abort_cmd bit in the SDMMC_CMD register so that the Host Controller can stop the data transfer after issuing the card reset command.
- When the data end bit error is set in the SDMMC_RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.
- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- Error detection

3.3.2.1 Command Path

The command path performs the following functions:

- Loads clock parameters
- Loads card command parameters
- Sends commands to card bus (ccmd_out line)
- Receives responses from card bus (ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the SDMMC_CMD register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.

Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

One of the following commands or responses is loaded in the command path:

- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the SDMMC_CMD register.
- Internally generated auto-stop command – When the data path ends, the stop command request is loaded.
- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a “send irq response” request is signaled by the BIU, then the send_irq_response bit is set in the SDMMC_CTRL register.

Loading a new command from the BIU in the command path depends on the following SDMMC_CMD register bit settings:

- update_clock_registers_only – If this bit is set in the SDMMC_CMD register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.
- wait_prvdata_complete – If this bit is set, the command path loads the new command under one of the following conditions:
  - Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (byte_count = 0).
  - After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response
Once a new command is loaded in the command path, update_clock_registers_only bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

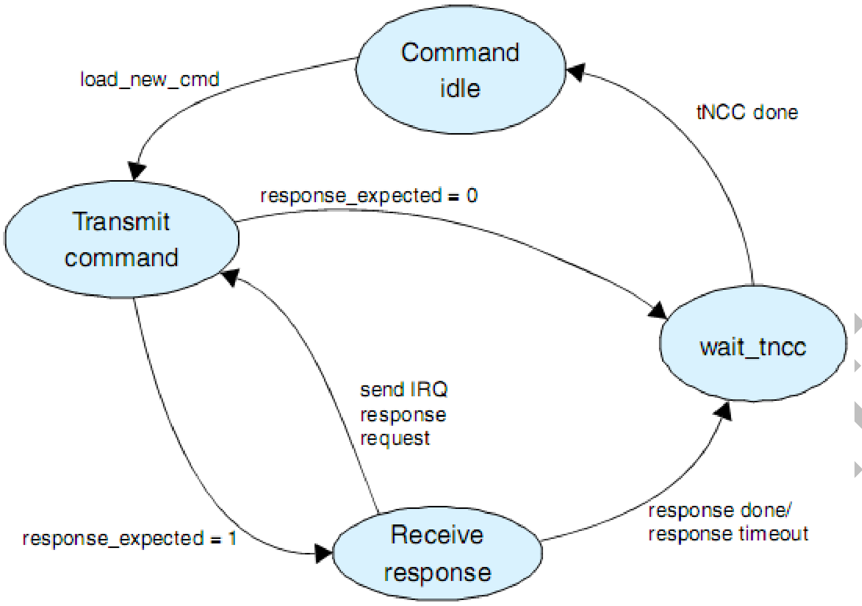


Fig. 3-3 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to SDMMC_CMD register bit values:

- send_initialization – Initialization sequence of 80 clocks is sent before sending the command.
- response_expected – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.
- response_length – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.
- check_response_crc – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in the Raw Interrupt Status register SDMMC_RINTSTS.

Send Response to BIU
If the response_expected bit is set in the SDMMC_CMD register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set.
Additionally, the command path checks for the following:

- Transmission bit = 0
- Command index matches command index of the sent command
- End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved-that is, 111111.
Polling Command Completion Signal
The device generates the Command Completion Signal in order to notify the host controller

of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the SDMMC_CMD register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the SDMMC_RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the SDMMC_CMD register—the command state machine waits for the CCS and remains in a wait_CCSS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the SDMMC_CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in SDMMC_RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

3.3.2.2 Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the SDMMC_CMD register, the new command is a data transfer command and the data path starts one of the following:

- Transmit data if the read/write bit = 1
- Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the value of the transfer_mode bit in the SDMMC_CMD register, the data transmit state machine puts data on the card data bus in a stream or in block(s).

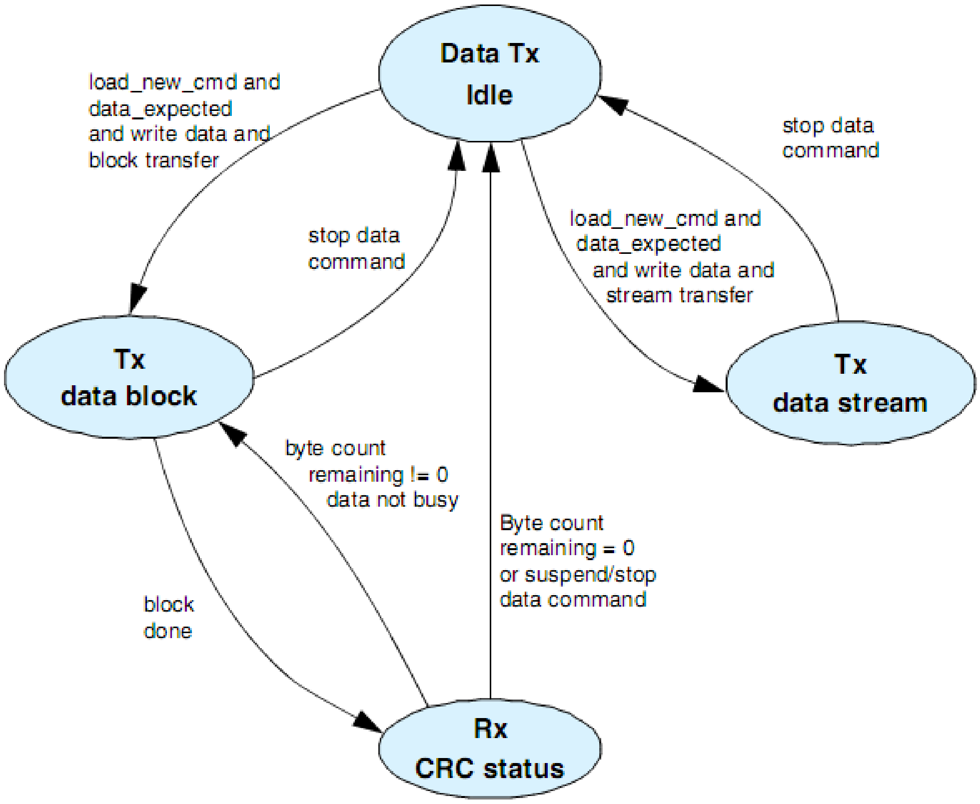


Fig. 3-4 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the SDMMC_CMD register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO.

If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set for a 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register.

Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register.

Multiple Block Data
A multiple-block write-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16.
If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.
After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.
If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.
If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register, and continues further data transmission until all the bytes are transmitted.
Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register; further data transfer is terminated.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.
If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, or 8 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.
If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.
Data Receive
The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.
If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the SDMMC_CMD register, the data-receive state machine gets data from the card data bus in a stream or block(s).

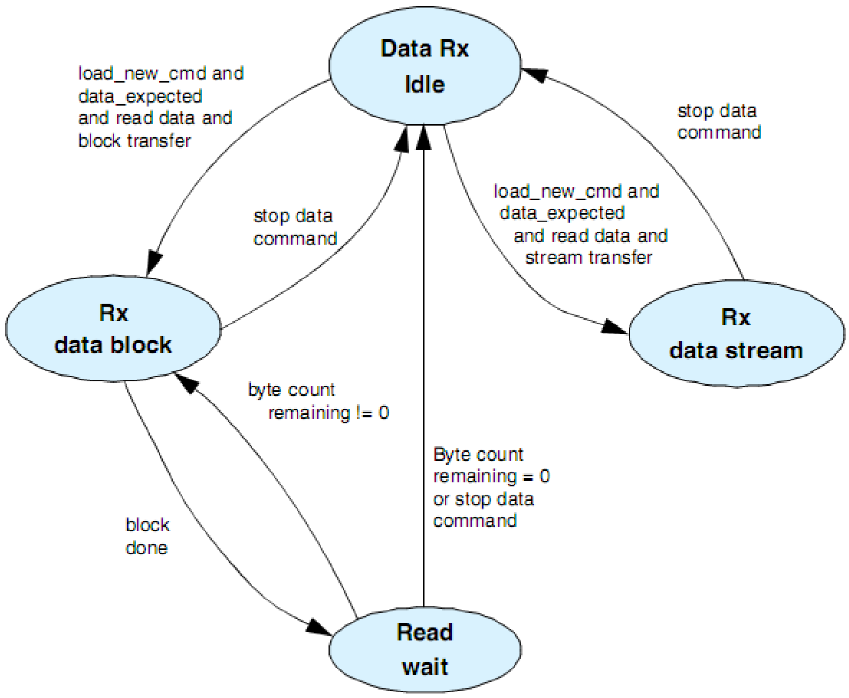


Fig. 3-5 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the SDMMC_CMD register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full.
An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.
If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16.
If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.
If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively.
After a data block is received, if the remaining byte_count becomes 0, the data path signals a data transfer to the BIU.

If the remaining data bytes are greater than 0, the data path state machine causes another data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.
Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.
If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.
If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.

Auto-Stop

The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the SDMMC_CMD register.
The software should set the send_auto_stop bit according to details listed in following table.

Table 3-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes①	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes①	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block write	>0	Yes	Auto-stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block read	0	No	Open-ended multiple block
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block write	0	No	Open-ended multiple block
SDIO	Multiple-block	>0	No	Pre-defined multiple block

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
	write			

*①:The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.*

The following list conditions for the auto-stop command.

- Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.
- Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.
- Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.
- Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.
- Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

3.3.2.3 Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

Table 3-3 Non-data Transfer Commands and Requirements

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
SDMMC_CMD register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1
rResponse_length	0	0	0	0	0	0
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0
transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0
Command Argument register programming						
	stuff bits	32-bit write protect data address	stuff bits	stuff bits	stuff bits	stuff bits
Block Size register programming						
	16	4	Num_bytes①	64	4	8
Byte Count register programming						
	16	4	Num_bytes①	64	4	8

①: Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)

3.3.2.4 SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle
- Non-data transfer command in progress
- Third clock after end bit of data block between two data blocks
- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

- Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.
- Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample SDIO interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

3.3.2.5 Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock (cclk_in >= card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

The clock frequency of a card depends on the following clock control registers:

- Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. A value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2.

- Clock Control register – cclk_out can be enabled or disabled for each card under the following conditions:
  - clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).
  - Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.
Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

- Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).
- If low-power mode is selected and card is idle, or not selected for 8 clocks.
- FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.
- FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

3.3.2.6 Error Detection

- Response
  - Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.
  - Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.
  - Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.
- Data transmit
  - No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:
    - Signals no CRC status error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to the BIU
  - Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.
  - Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.
- Data receive
  - Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:
    - Signals data-timeout error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to BIU
  - Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.
  - Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error

to the BIU and continues further data transfer.
- Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.
- Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in SDMMC_RINTSTS register) and the data path continues to wait for the FIFO to start to empty.

3.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.
The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.
The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.
A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor cannot span multiple data.
A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (SDMMC_DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

3.3.3.1 IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled.
You can enable or disable the IDMAC operation by programming bit[25] in the SDMMC_CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

3.3.3.2 Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:
- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (SDMMC_BMOD @0x80).

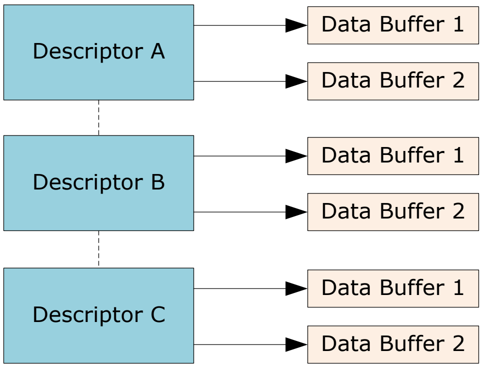


Fig. 3-6 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

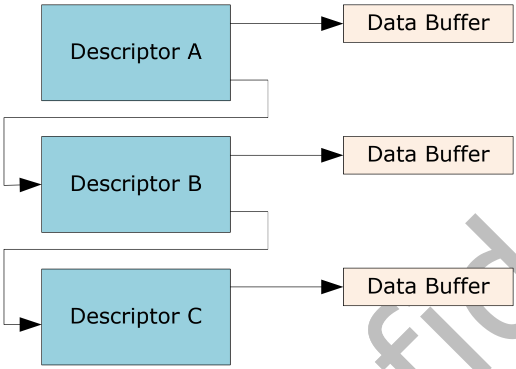


Fig. 3-7 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96] bits.

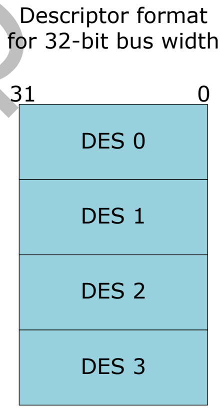


Fig. 3-8 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 3-4 Bits in IDMAC DES0 Element

Bit	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in SDMMC_RINTSTS Indicates the logical OR of the following bits:

Bit	Name	Description
		• EBE: End Bit Error • RTO: Response Time out • RCRC: Response CRC • SBE: Start Bit Error • DRTO: Data Read Timeout • DCRC: Data CRC for Receive • RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on Completion (DIC)	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.
0	Reserved	-

- The DES1 element contains the buffer size.

Table 3-5 Bits in IDMAC DES1 Element

Bit	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES2 element contains the address pointer to the data buffer.

Table 3-6 Bits in IDMAC DES2 Element

Bit	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus

Bit	Name	Description
		widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 3-7 Bits in IDMAC DES3 Element

Bit	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned.

3.3.3.3 Initialization

IDMAC initialization occurs as follows:

1) Write to IDMAC Bus Mode Register—SDMMC_BMOD to set Host bus access parameters.
2) Write to IDMAC Interrupt Enable Register—SDMMC_IDINTEN to mask unnecessary interrupt causes.
3) The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (SDMMC_DBADDR), providing the IDMAC with the starting address of the list.
4) The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- Host Bus Burst Access

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.

The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.

The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- Host Data Buffer Alignment

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

- Buffer Size Calculations

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.

If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- Transmission

IDMAC transmission occurs as follows:

1) The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.
2) The Host programs the write data command in the SDMMC_CMD register in BIU.
3) The Host will also program the required transmit threshold level (TX_WMark field in SDMMC_FIFOTH register).
4) The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can’t be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.
8) The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data transmission is complete, status information is updated in SDMMC_IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

1) The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).
2) The Host programs the read data command in the SDMMC_CMD register in BIU.
3) The Host will program the required receive threshold level (RX_WMark field in FIFOTH register).
4) The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can’t be accessed using a burst, SINGLE transfers are performed on AHB.
8) The IDMAC fetches the data from the FIFO and transfer to Host memory.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data reception is complete, status information is updated in SDMMC_IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. SDMMC_IDSTS register contains all the bits that might cause an interrupt. SDMMC_IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.
There are two groups of summary interrupts-Normal and Abnormal-as outlined in SDMMC_IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.
Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt—SDMMC_IDSTS[1] indicates that one or more data was transferred to the Host buffer.
An interrupt is generated only once for simultaneous, multiple events. The driver must scan SDMMC_IDSTS register for the interrupt cause.

3.3.4 Variable Delay/Clock Generation Unit

Variable delay mechanism for the cclk_in_drv is useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.
The Clock Generation Unit (CLKGEN) includes Phase Shift Unit and Delay Line Unit.
The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in. The Delay Line Unit can shift cclk_in_sample/cclk_in_drv step by step in the unit of delay element. The delay value range is 25ps~56ps for every delay element; the max delay element number is 256.
The architecture is as follows.

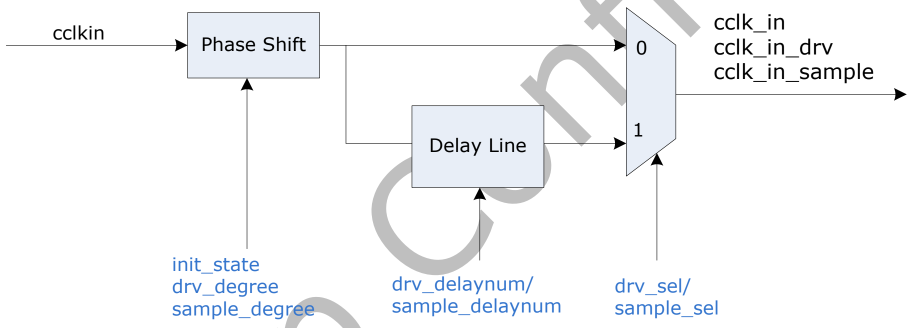


Fig. 3-9 Clock Generation Unit

3.4 Register Description

3.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x00000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock divider register
SDMMC_CLKSRC	0x000c	W	0x00000000	SD clock source register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock enable register
SDMMC_TMOUT	0x0014	W	0xFFFFFF40	Timeout register
SDMMC_CTYPE	0x0018	W	0x00000000	Card type register
SDMMC_BLKSIZ	0x001c	W	0x00000200	Block size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt mask register
SDMMC_CMDARG	0x0028	W	0x00000000	Command argument register
SDMMC_CMD	0x002c	W	0x20000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response register 0
SDMMC_RESP1	0x0034	W	0x00000000	Response register 1
SDMMC_RESP2	0x0038	W	0x00000000	Response register 2
SDMMC_RESP3	0x003c	W	0x00000000	Response register 3
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt status register
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt status register

Name	Offset	Size	Reset Value	Description
SDMMC_STATUS	0x0048	W	0x00000106	Status register
SDMMC_FIFOTH	0x004c	W	0x00FF0000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000001	Card detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write protect register
SDMMC_TCBCNT	0x005c	W	0x00000000	Transferred card byte count register
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host to FIFO byte count register
SDMMC_DEBNCE	0x0064	W	0x00FFFFFF	Debounce count register
SDMMC_USRID	0x0068	W	0x00000000	User ID register
SDMMC_VERID	0x006c	W	0x5342270A	Version ID register
SDMMC_HCON	0x0070	W	0x04C434C1	Hardware configuration register
SDMMC_UHSREG	0x0074	W	0x00000000	UHS-1 control register
SDMMC_RSTN	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus mode register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll demand register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor list base address register
SDMMC_IDSTS	0x008c	W	0x00000000	Internal DMAC status register
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC interrupt enable register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current host descriptor address register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current buffer descriptor address register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card threshold control register
SDMMC_BACKEND_POWER	0x0104	W	0x00000000	Back-end power register
SDMMC_EMMCDDR_REG	0x010c	W	0x00000000	eMMC4.5 DDR start bit detection control register
SDMMC_RDYINT_GEN	0x0120	W	0x00FF0000	Card ready interrupt generation control register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO base address register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.4.2 Detail Register Description

SDMMC_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 1'b0: The host performs data transfers through the slave interface 1'b1: Internal DMAC used for data transfer
24:12	RO	0x0000	reserved
11	RW	0x0	ceata_device_interrupt_status 1'b0: Interrupts not enabled in CE-ATA device 1'b1: Interrupts are enabled in CE-ATA device Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled. If the host enables CE-ATA device interrupt, then software should set this bit.

Bit	Attr	Reset Value	Description
10	RW	0x0	send_auto_stop_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd. When set, the Host Controller automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in SDMMC_RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, the Host Controller automatically clears send_auto_stop_ccsd bit.
9	RW	0x0	send_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, the Host Controller sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, the Host Controller automatically clears send_ccsd bit. It also sets Command Done (CD) bit in SDMMC_RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.
8	RW	0x0	abort_read_data 1'b0: No change 1'b1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.
7	RW	0x0	send_irq_response 1'b0: No change 1'b1: Send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, software issues CMD40, and the Host Controller waits for interrupt response from MMC card. In meantime, if software wants the Controller to exit waiting for interrupt state, it can set this bit, at which time the Host Controller command state-machine sends CMD40 response on bus and returns to idle state.
6	RW	0x0	read_wait 1'b0: Clear read wait 1'b1: Assert read wait For sending read-wait to SDIO cards.

Bit	Attr	Reset Value	Description
5	RW	0x0	dma_enable 1'b0: Disable DMA transfer mode 1'b1: Enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside the controller to prioritize simultaneous host/DMA access.
4	RW	0x0	int_enable Global interrupt enable/disable bit. 1'b0: Disable interrupts 1'b1: Enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
3	RO	0x0	reserved
2	WO	0x0	dma_reset 1'b0: No change 1'b1: Reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.
1	WO	0x0	fifo_reset 1'b0: No change 1'b1: Reset to data FIFO to reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.
0	WO	0x0	controller_reset 1'b0: No change 1'b1: Reset Host Controller To reset Host Controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: a. BIU/CIU interface b. CIU and state machines c. abort_read_data, send_irq_response, and read_wait bits of SDMMC_CTRL register d. start_cmd bit of SDMMC_CMD register Does not affect any registers or DMA interface, or FIFO or controller interrupts.

SDMMC_PWREN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 1'b0: Power off 1'b1: Power on Bit values output to card_power_en port.

SDMMC_CLKDIV

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, and so on. The recommended value is 0 or 1.

SDMMC_CLKSRC

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	clk_source Clock divider source. 2'b00: Clock divider 0 The cclk_out is always from clock divider 0, and this register is not implemented.

SDMMC_CLKENA

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	cclk_low_power Low-power control for SD card clock and MMC card clock supported. 1'b0: Non-low-power mode 1'b1: Low-power mode Stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).
15:1	RO	0x0000	reserved
0	RW	0x0	cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 1'b0: Clock disabled 1'b1: Clock enabled

SDMMC_TMOUT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RW	0xffffff	data_timeout Value for card data read timeout; same value also used for data starvation by host timeout. Value is in number of card output clock. Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.
7:0	RW	0x40	response_timeout Response timeout value. Value is in number of card output clock cclk_out.

SDMMC_CTYPE

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	card_width_8 Indicates if card is 8-bit. 1'b0: Non 8-bit mode 1'b1: 8-bit mode
15:1	RO	0x0000	reserved
0	RW	0x0	card_width Indicates if card is 1-bit or 4-bit. 1'b0: 1-bit mode 1'b1: 4-bit mode

SDMMC_BLKSIZ

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0200	block_size Block size

SDMMC_BYTCNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	byte_count Number of bytes to be transferred; should be integer multiple of block size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.

SDMMC_INTMASK

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sdio_int_mask 1'b0: SDIO interrupt not masked 1'b1: SDIO interrupt masked
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_mask 1'b0: Data no busy interrupt not masked 1'b1: Data no busy interrupt masked

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_CMDARG
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card.

SDMMC_CMD
Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD/MMC cards, Command Done bit is set in raw interrupt register.
30	RO	0x0	reserved
29	RW	0x1	use_hold_reg Use hold register. 1'b0: CMD and DATA sent to card bypassing hold register 1'b1: CMD and DATA sent to card through the hold register
28	RW	0x0	volt_switch Voltage switch bit. 1'b0: No voltage switching 1'b1: Voltage switching enabled; must be set for CMD11 only.
27	RW	0x0	boot_mode Boot mode selection. 1'b0: Mandatory boot operation 1'b1: Alternate boot operation
26	RW	0x0	disable_boot Disable boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do not set disable_boot and enable_boot together.

Bit	Attr	Reset Value	Description
25	RW	0x0	expect_boot_ack Expect boot acknowledge. When software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
24	RW	0x0	enable_boot Enable boot. This bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do not set disable_boot and enable_boot together.
23	RW	0x0	ccs_expected 1'b0: Interrupts are not enabled in CE-ATA device or command does not expect CCS from device 1'b1: Interrupts are enabled in CE-ATA device and RW_BLK command expects command completion signal from CE-ATA device If the command expects command completion signal (CCS) from the CE-ATA device, the software should set this control bit. The Host Controller sets data transfer over (DTO) bit in SDMMC_RINTSTS register and generates interrupt to host if data transfer over interrupt is not masked.
22	RW	0x0	read_ceata_device 1'b0: Host is not performing read access towards CE-ATA device 1'b1: Host is performing read access towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. The Host Controller should not indicate read data timeout while waiting for data from CE-ATA device.
21	RW	0x0	update_clock_regs_only 1'b0: Normal command sequence 1'b1: Do not send commands, just update clock register value into card clock domain. Following register values transferred into card clock domain: SDMMC_CLKDIV, SDMMC_CLRSRC, SDMMC_CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_regs_only = 0, following control registers are transferred from BIU to CIU: SDMMC_CMD, SDMMC_CMDARG, SDMMC_TMOUT, SDMMC_CTYPE, SDMMC_BLKSIZ, SDMMC_BYTCNT. CIU uses new register values for new command sequence to card. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.
20:16	RO	0x00	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	send_initialization 1'b0: Do not send initialization sequence (80 clocks of 1) before sending this command 1'b1: Send initialization sequence before sending this command After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).
14	RW	0x0	stop_abort_cmd 1'b0: Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1'b1: Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with SDMMC_CMD[26]=disable_boot.
13	RW	0x0	wait_prvdata_complete 1'b0: Send command at once, even if previous data transfer has not completed 1'b1: Wait for previous data transfer completion before sending command The wait_prvdata_complete=0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.
12	RW	0x0	send_auto_stop 1'b0: No stop command sent at end of data transfer 1'b1: Send stop command at end of data transfer When set, the Host Controller sends stop command to card at end of data transfer. a. When send_auto_stop bit should be set, since some data transfers do not need explicit stop commands b. Open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume-suspended memory access of SD-Combo card, bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.
11	RW	0x0	transfer_mode 1'b0: Block data transfer command 1'b1: Stream data transfer command Don't care if no data expected.
10	RW	0x0	wr 1'b0: Read from card 1'b1: Write to card Don't care if no data expected from card.
9	RW	0x0	data_expected 1'b0: No data transfer expected (read/write) 1'b1: Data transfer expected (read/write)

Bit	Attr	Reset Value	Description
8	RW	0x0	check_response_crc 1'b0: Do not check response CRC 1'b1: Check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.
7	RW	0x0	response_length 1'b0: Short response expected from card 1'b1: Long response expected from card
6	RW	0x0	response_expect 1'b0: No response expected from card 1'b1: Response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response1 Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them.

SDMMC_RESP2
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response.

SDMMC_RESP3
Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response3 Bit[127:96] of long response.

SDMMC_MINTSTS
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	sdio_interrupt SDIO interrupt status when sdio_int_mask is set.
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status when data_nobusy_int_mask is set

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	int_status Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_RINTSTS
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	WO	0x0	sdio_interrupt Raw SDIO interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
23:17	RO	0x00	reserved
16	WO	0x0	data_nobusy_int_status Raw data no busy interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
15:0	WO	0x0000	int_status Raw interrupt status. Writes to bits clear status bit. Write value of 1 clears status bit, and value of 0 leaves bit intact. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_STATUS
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core.
10	RO	0x0	data_state_mc_busy Data transmit or receive state-machine is busy.
9	RO	0x0	data_busy Inverted version of raw selected card_data[0]. 1'b0: Card data not busy 1'b1: Card data busy
8	RO	0x1	data_3_status Raw selected card_data[3]; checks whether card is present. 1'b0: Card not present 1'b1: Card present
7:4	RO	0x0	command_fsm_states Command FSM states: 4'h0: Idle 4'h1: Send init sequence 4'h2: Tx cmd start bit 4'h3: Tx cmd tx bit 4'h4: Tx cmd index + arg 4'h5: Tx cmd crc7 4'h6: Tx cmd end bit 4'h7: Tx resp start bit 4'h8: Rx resp IRQ response 4'h9: Rx resp tx bit 4'ha: Rx resp cmd idx 4'hb: Rx resp data 4'hc: Rx resp crc7 4'hd: Rx resp end bit 4'he: Cmd path wait NCC 4'hf: Wait; CMD-to-response turnaround The command FSM state is represented using 19 bits. The SDMMC_STATUS register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the SDMMC_STATUS[7:4] register. The three states that are not represented in the SDMMC_STATUS register[7:4] are: Bit 16: Wait for CCS Bit 17: Send CCSD Bit 18: Boot Mode Due to this, while command FSM is in "Wait for CCS state" or "Send CCSD" or "Boot Mode", the SDMMC_STATUS register indicates status as 0 for the bit field [7:4].
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status

Bit	Attr	Reset Value	Description
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer.
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer.

SDMMC_FIFOTH

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	dma_mutiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers The unit for transfer is 32bits.
27:16	RW	0x0ff	rx_wmark FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits-1 bit less than FIFO-count of status register, which is 13 bits. Limitation: rx_wmark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	tx_wmark FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits -1 bit less than FIFO-count of status register, which is 13 bits. Limitation: tx_wmark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)

SDMMC_CDETECT

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	card_detect_n Value on card_detect_n input port. 1'b0: Represents presence of card 1'b1: Represents absence of card

SDMMC_WRTPRT

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection.

SDMMC_TCBCNT

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_card_byte_count Number of bytes transferred by CIU unit to card.

SDMMC_TBBCNT

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_fifo_byte_count Number of bytes transferred between host/DMA memory and BIU FIFO.

SDMMC_DEBNCE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0xffffff	debounce_count Number of host clock used by debounce filter logic; typical debounce time is 5-25 ms.

SDMMC_USRID

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usrid User identification register

SDMMC_VERID

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register

SDMMC_HCON

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x1	area_optimized 1'b0: No area optimization 1'b1: Area optimization
25:24	RO	0x0	num_clk_div divider number-1.
23	RO	0x1	set_clk_false_path 1'b0: No false path 1'b1: False path set
22	RO	0x1	impl_hold_reg 1'b0: No hold register 1'b1: Hold register
21	RO	0x0	fifo_ram_inside 1'b0: Outside 1'b1: Inside
20:18	RO	0x1	ge_dma_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved
17:16	RO	0x0	dma_interface 2'b00: None 2'b01: INT_DMA 2'b10: GENERIC_DMA 2'b11: NON-INT-DMA
15:10	RO	0x1f	h_addr_width 6'h8: 9 bits 6'h9: 10 bits ...... 6'h1f: 32 bits Others: Reserved
9:7	RO	0x1	h_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved

Bit	Attr	Reset Value	Description
6	RO	0x1	h_bus_type 1'b0: APB 1'b1: AHB
5:1	RO	0x00	card_num Card number -1.
0	RO	0x1	card_type Card type. 1'b0: MMC_ONLY 1'b1: SD_MMC

SDMMC_UHSREG

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	ddr_reg DDR mode. These bits indicate DDR mode of operation to the core for the data transfer. 1'b0: Non-DDR mode 1'b1: DDR mode
15:0	RO	0x0000	reserved

SDMMC_RSTN

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	card_reset Hardware reset. 1'b0: Active mode 1'b1: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

SDMMC_BMOD

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
10:8	RO	0x0	pbl Programmable burst length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of SDMMC_FIFOTH register. In order to change this value, write the required value to SDMMC_FIFOTH register. This is an encode value as follows. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers Transfer unit is 32 bits. PBL is a read-only value and is applicable only for data access; it does not apply to descriptor accesses.
7	RW	0x0	de IDMAC enable. When set, the IDMAC is enabled.
6:2	RW	0x00	dsl Descriptor skip length. Specifies the number of word to skip between two unchained descriptors. This is applicable only for dual buffer structure.
1	RW	0x0	fb Fixed burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	RW	0x0	swr Software reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

SDMMC_PLDMND

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	pd Poll demand. If the OWN bit of a descriptor is not set, the FSM goes to the suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation.

SDMMC_DBADDR

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbl Start of descriptor list. Contains the base address of the first descriptor. The LSB bits[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

SDMMC_IDSTS

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:13	RO	0x0	fsm DMAC FSM present state. 4'h0: DMA_IDLE 4'h1: DMA_SUSPEND 4'h2: DESC_RD 4'h3: DESC_CHK 4'h4: DMA_RD_REQ_WAI 4'h5: DMA_WR_REQ_WAI 4'h6: DMA_RD 4'h7: DMA_WR 4'h8: DESC_CLOSE Others: Reserved
12:10	RO	0x0	eb Error bits. Indicates the type of error that caused a bus error. Valid only with fatal bus. 3'h1: Host abort received during transmission 3'h2: Host abort received during reception Others: Reserved
9	RW	0x0	ais Abnormal interrupt summary. Logical OR of the following: SDMMC_IDSTS[2] fatal bus interrupt SDMMC_IDSTS[4] du bit interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes ais to be set is cleared. Writing a 1 clears this bit.
8	RW	0x0	nis Normal interrupt summary. Logical OR of the following: SDMMC_IDSTS[0] transmit interrupt SDMMC_IDSTS[1] receive interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes nis to be set is cleared. Writing a 1 clears this bit.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	ces Card error summary. Indicates the status of the transaction to/from the card; also present in SDMMC_RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot Ack Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a "response error"; however, it will not abort if the CES bit is cleared.
4	RW	0x0	dui Descriptor unavailable interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error interrupt. Indicates that a bus error occurred (SDMMC_IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	RW	0x0	ri Receive interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	RW	0x0	ti Transmit interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit.

SDMMC_IDINTEN

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ai Abnormal interrupt summary enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: SDMMC_IDINTEN[2] fatal bus error interrupt SDMMC_IDINTEN[4] du interrupt
8	RW	0x0	ni Normal interrupt summary enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: SDMMC_IDINTEN[0] transmit interrupt SDMMC_IDINTEN[1] receive interrupt
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	ces Card error summary interrupt enable. When set, it enables the card interrupt summary.
4	RW	0x0	du Descriptor unavailable interrupt. When set along with abnormal interrupt summary enable, the du interrupt is enabled.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error enable. When set with abnormal interrupt summary enable, the fatal bus error interrupt is enabled. When reset, fatal bus error enable interrupt is disabled.
1	RW	0x0	ri Receive interrupt enable. When set with normal interrupt summary enable, receive interrupt is enabled. When reset, receive interrupt is disabled.
0	RW	0x0	ti Transmit interrupt enable. When set with normal interrupt summary enable, transmit interrupt is enabled. When reset, transmit interrupt is disabled.

SDMMC_DSCADDR

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hda Host descriptor address pointer. This register points to the start address of the current descriptor read by the IDMAC. Cleared on reset. Pointer updated by IDMAC during operation.

SDMMC_BUFADDR

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hba Host buffer address pointer. This register points to the current data buffer address being accessed by the IDMAC. Cleared on Reset. Pointer updated by IDMAC during operation.

SDMMC_CARDTHRCTL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	card_rd_thres Card read threshold size
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	busy_clr_int_en Busy clear interrupt. 1'b0: Busy clear interrupt disabled 1'b1: Busy clear interrupt enabled Note: The application can disable this feature if it does not want to wait for a busy clear interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.
0	RW	0x0	card_rd_thres_en Card read threshold enable. 1'b0: Card read threshold disabled 1'b1: Card read threshold enabled. The host initiates read transfer only if zcard_rd_thres amount of space is available in receive FIFO.

SDMMC_BACKEND_POWER

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	back_end_power Back end power. 1'b0: Off; Reset 1'b1: Back-end power supplied to card application

SDMMC_EMMCDDR_REG

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	half_start_bit Control for start bit detection mechanism inside Host Controller based on duration of start bit. For eMMC 4.5, start bit can be: 1'b0: Full cycle (half_start_bit=0) 1'b1: Less than one full cycle (half_start_bit=1) Set half_start_bit=1 for eMMC 4.5 and above; set to 0 for SD applications.

SDMMC_RDYINT_GEN

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	rdyint_cnt_finish Counter finish indication. When high, it indicates that the rdyint counter is finished.
23:16	RO	0xff	rdyint_cnt_status Couner status, reflect internal counter value.
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	rdyint_gen_working Working indication for rdyint generator. When high, Host Controller start to count and generate one rdyint trigger. After the rdyint trigger is generated, this bit will be set to 0 by Host Controller. So software should set it to 1 before detecting next interrupt.
7:0	RW	0x00	rdyint_gen_maxval Max counter value to detect cdata_in0 high value for generating rdyint, based on internal clock frequency.

SDMMC_FIFO_BASE

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr FIFO base address

3.5 Interface Description

3.5.1 SDMMC Interface Description

Table 3-8 SDMMC Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc_cclk	O	SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d	BUS_IOC_GPIO4D_IOMUX_SEL_H[7:4]=4'h1
sdmmc_ccmd	I/O	SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u	BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0]=4'h1
sdmmc_cdata0	I/O	SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u	BUS_IOC_GPIO4D_IOMUX_SEL_L[3:0]=4'h1
sdmmc_cdata1	I/O	SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u	BUS_IOC_GPIO4D_IOMUX_SEL_L[7:4]=4'h1
sdmmc_cdata2	I/O	SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2_u	BUS_IOC_GPIO4D_IOMUX_SEL_L[11:8]=4'h1
sdmmc_cdata3	I/O	SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u	BUS_IOC_GPIO4D_IOMUX_SEL_L[15:12]=4'h1
sdmmc_cdetn	I	SDMMC_DET/GPIO0_A4_u	PMU1_IOC_GPIO0A_IOMUX_SEL_H[3:0]=4'h1
sdmmc_pwr	O	SPI2_CLK_M2/SDMMC_PWREN/PMU_DEBUG/GPIO0_A5_d	PMU1_IOC_GPIO0A_IOMUX_SEL_H[7:4]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

3.5.2 SDIO Interface Description

Table 3-9 SDIO M0 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdio_cclk	O	GMAC0_TXCLK/SDIO_CLK_M0/FSPI_CLK_M1/I2C3_SDA_M3/GPIO2_B3_d	BUS_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'h2
sdio_ccmd	I/O	GMAC0_TXD3/SDIO_CMD_M0/I2C3_SCL_M3/GPIO2_B2_u	BUS_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4'h2
sdio_cdata0	I/O	GMAC0_RXD2/SDIO_D0_M0/FSPI_D0_M1/UART6_RX_M0/GPIO2_A6_u	BUS_IOC_GPIO2A_IOMUX_SEL_H[11:8]=4'h2
sdio_cdata1	I/O	GMAC0_RXD3/SDIO_D1_M0/FSPI_D1_M1/UART6_TX_M0/GPIO2_A7_u	BUS_IOC_GPIO2A_IOMUX_SEL_H[15:12]=4'h2
sdio_cdata2	I/O	GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u	BUS_IOC_GPIO2B_IOMUX_SEL_L[3:0]=4'h2
sdio_cdata3	I/O	GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u	BUS_IOC_GPIO2B_IOMUX_SEL_L[7:4]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 3-10 SDIO M1 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdio_cclk	O	GMAC1_RXCLK/SDIO_CLK_M1/MIPI_CAMERA0_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5_d	BUS_IOC_GPIO3A_IOMUX_SEL_H[7:4]=4'h2
sdio_ccmd	I/O	GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d	BUS_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4'h2
sdio_cdata0	I/O	GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u	BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'h2
sdio_cdata1	I/O	GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_	BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'h2

Module Pin	Dir.	PAD Name	IOMUX Setting
		M1/GPIO3_A1_u	
sdio_cdata2	I/O	GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u	BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'h2
sdio_cdata3	I/O	GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u	BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

3.6 Application Notes

3.6.1 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of SDMMC_STATUS register.
2) Update the Clock Enable register to disable clock. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:
   - start_cmd bit
   - "update clock registers only" bits
   - "wait_previous data complete" bit

   Wait for the CIU to take the command by polling for 0 on the start_cmd bit.
3) Set the start_cmd bit to update the Clock Divider and/or Clock Source register, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.
4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (SDMMC_RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the data is flushed to memory by the DMA interface unit.

While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.

If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DMA is used, the DMA controller channel should also be reset and reprogrammed. If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting the FIFO reset, you should wait until this bit is cleared.

One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only 15 bytes to an SD/MMC card (SDMMC_BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO.

It is recommended that you not change the FIFO threshold register in the middle of data transfers.

3.6.2 Programming Sequence

3.6.2.1 Initialization

Following figure illustrates the initialization flow.

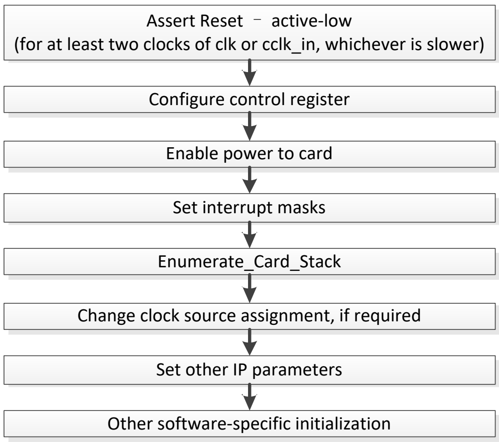


Fig. 3-10 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted(active-low) for at least two cycles of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

1) Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup(bit24) in the SDMMC_CTRL register.
2) Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.
3) Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the SDMMC_CTRL register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts before setting the int_enable bit.
4) Enumerate card stack – Each card is enumerated according to card type; for details, refer to “Enumerated Card Stack”. For enumeration, you should restrict the clock frequency to 400KHz.
5) Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to “Clock Programming”. MMC cards operate at a maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).
6) Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

- ResponseTimeOut = 0x64
- DataTimeOut = highest of one of the following:
- (10*((TAAC*Fop)+(100*NSAC))
- Host FIFO read/write latency from FIFO empty/full
- Set the debounce value to 25ms(default:0x0fffff) in host clock cycle units in the SDMMC_DEBNCE register.
- FIFO threshold value in bytes in the SDMMC_FIFOTH register.

3.6.2.2 Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards
- Reads card-specific information
- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first

identified and the appropriate card enumeration routine is called.
1) Check if the card is connected.
2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
3) Set clock frequency to FOD=400KHz, maximum – Program clock divider0 (bits 0-7 in the SDMMC_CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is 20, 000/(2*400)=25.
4) Identify the card type; that is, SD, MMC, or SDIO.
   a. Send CMD5 first. If a response is received, then the card is SDIO
   b. If not, send CMD8 with the following Argument
      Bit[31:12] = 20'h0 //reserved bits
      Bit[11:8] = 4'b0001 //VHS value
      Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0
   c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b1; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
   d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
   e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b0; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
5) Enumerate the card according to the card type.
6) Use a clock source with a frequency = Fod (that is, 400KHz) and use the following enumeration command sequence:
- SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
- MMC – Send CMD0, CMD1, CMD2, CMD3.

3.6.2.3 Clock Programming

The Host Controller supports one clock source. The clock to an individual card can be enabled or disabled. Registers that support this are:
- SDMMC_CLKDIV – Programs individual clock source frequency. SDMMC_CLKDIV limited to 0 or 1 is recommended.
- SDMMC_CLKSRC – Assign clock source for each card.
- SDMMC_CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the update_clk_regs_only bit in the SDMMC_CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE(Hardware Locked Error). Software should look for the start_cmd and the update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.
The following shows how to program these registers:
1) Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.
2) Stop all clocks by writing 0 to the SDMMC_CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
3) Program the SDMMC_CLKDIV and SDMMC_CLKSRC registers, as required. Set the

start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

4) Re-enable all clocks by programming the SDMMC_CLKENA register. Set the start_cmd, update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

3.6.2.4 No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the SDMMC_CMD register @0x2C and the SDMMC_CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the SDMMC_RINTSTS register.
When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. A short response is copied in Response Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.
For basic commands or non-data commands, follow these steps:

1) Program the Command register @0x28 with the appropriate command argument parameter.
2) Program the Command register @0x2C with the settings in following table.

Table 3-11 Command Settings for No-Data Command

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to “use_hold_reg” on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
data_expected	0	No data command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
wait_prvdata_complete	1	Before sending command on command line, host should wait for completion of any data command in process, if any (recommended to always set this bit, unless the current command is to query status

Parameter	Value	Description
		or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

3) Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:
- Host Controller accepts the command for execution and clears the start_cmd bit in the SDMMC_CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
- If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

4) Check if there is an HLE.
5) Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.
6) Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the SDMMC_RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

3.6.2.5 Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.
Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively.
For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.
The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the SDMMC_RINTSTS register @0x44 as:

1) Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a response timeout error, then the Host Controller does not attempt any data transfer and the "Data Transfer Over" bit is never set.
2) Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.
3) Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.
4) Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.
5) Data read timeout error (bit 9) – Card has not sent data within the timeout period.
6) Data CRC error (bit 7) – CRC error occurred during data reception.
7) Start bit error (bit 13) – Start bit was not received during data reception.
8) End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6), 7), and 8) indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

3.6.2.6 Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size SDMMC_BLKSIZ each.

3) Program the SDMMC_CMDARG register @0x28 with the data address of the beginning of a data read.
4) Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

Table 3-12 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to “use_hold_reg” on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

- Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending a STOP command.
- Software should look for Receive_FIFO_Data_request and/or data starvation by host timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.
- When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

3.6.2.7 Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C; the Host Controller sends data in blocks of size SDMMC_BLKSIZ each.
3) Program SDMMC_CMDARG register @0x28 with the data address to which data should be written.
4) Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.
5) Program the Command register with the parameters listed in following table.

Table 3-13 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to “use_hold_reg” on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

- Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending the STOP command.
- Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.
- When a Data_Transfer_Over interrupt is received, the data command is over. For an

open-ended block transfer, if the byte count is 0, the software must send the STOP command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the SDMMC_RINTSTS register. A response to AUTO_STOP is stored in SDMMC_RESP1 @0x34.

3.6.2.8 Stream Read

A stream read is like the block read mentioned in “Single-Block or Multiple-Block Read”, except for the following bits in the Command register:

transfer_mode = 1; //Stream transfer
cmd_index = CMD20;

A stream transfer is allowed for only a single-bit bus width.

3.6.2.9 Stream Write

A stream write is exactly like the block write mentioned in “Single-Block or Multiple-Block Write”, except for the following bits in the Command register:

transfer_mode = 1;//Stream transfer
cmd_index = CMD11;

In a stream transfer, if the byte count is 0, then the software must send the STOP command. If the byte count is not 0, then when a given number of bytes completes a transfer, the Host Controller sends the STOP command. Completion of this AUTO_STOP command is reflected by the Auto_command_done interrupt. A response to an AUTO_STOP is stored in the SDMMC_RESP1 register@0x34.
A stream transfer is allowed for only a single-bit bus width.

3.6.2.10 Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.

- Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.

- Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

3.6.2.11 Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

1) Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.
2) If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the SDMMC_CTRL register @0x00.
3) Clear the read_wait bit in the SDMMC_CTRL register.

3.6.2.12 Controller/DMA/FIFO Reset Usage

- Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the SDMMC_CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.
- FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the SDMMC_CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is

self-clearing, after issuing the reset, wait until this bit is cleared.
In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO under-run or overrun errors in the SDMMC_RAWINTS register caused by the DMA transfers after the FIFO was reset.

3.6.2.13 Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the SDMMC_CARDTHRCTL register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable (CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the Card Read Threshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

3.6.2.14 Error Handling

The Host Controller implements error checking; errors are reflected in the SDMMC_RAWINTS register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the SDMMC_CTRL register is 0), and all the interrupts are masked (bits 0-31 of the SDMMC_INTMASK register; default is 0).
Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the SDMMC_TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.
- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
- FIFO under-run/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an under-run error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill data in the FIFO in order to start transferring data to the card.
- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data *path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.*

3.6.3 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.
However, whether the IO voltage of 1.8v supported or not is depended on the SoC design.
SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.
If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

- If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the IO voltage selection register based on the soc architecture.
- If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.
Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the SDMMC_DDR_REG register in the CSR space with the appropriate card number.
To choose from any of the SDR or DDR modes, appropriate values should be programmed in the SDMMC_CLKDIV register.

3.6.3.1 Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

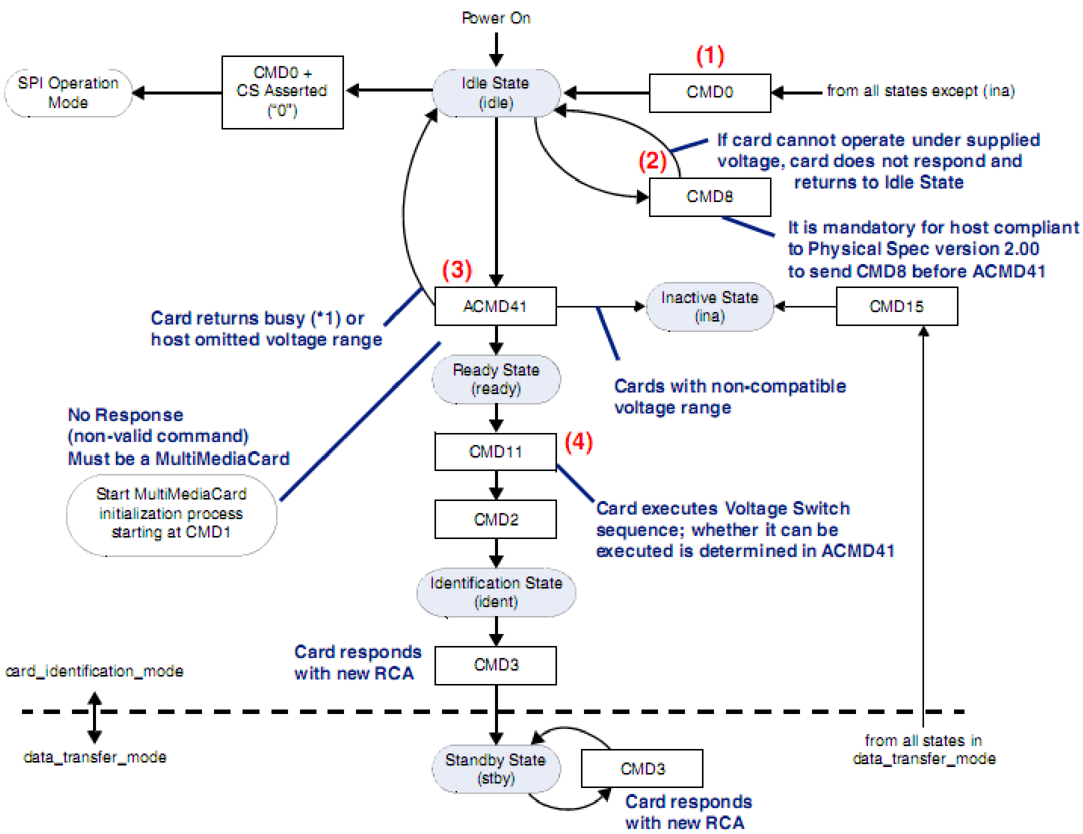


Fig. 3-11 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

1) Software Driver starts CMD0, which selects the bus mode as SD.
2) After the bus is in SD card mode, CMD8 is started in order to verify if the card is compatible with the SD Memory Card Specification, Version 2. 00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.
3) ACMD 41 is started. The response to this command informs the software if the card supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

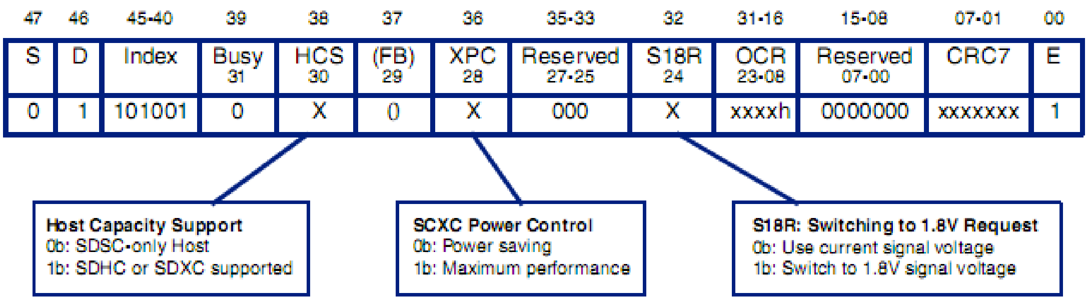


Fig. 3-12 ACMD41 Argument

- Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
- Bit 28 can be either 1 or 0.
- Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to following figure.

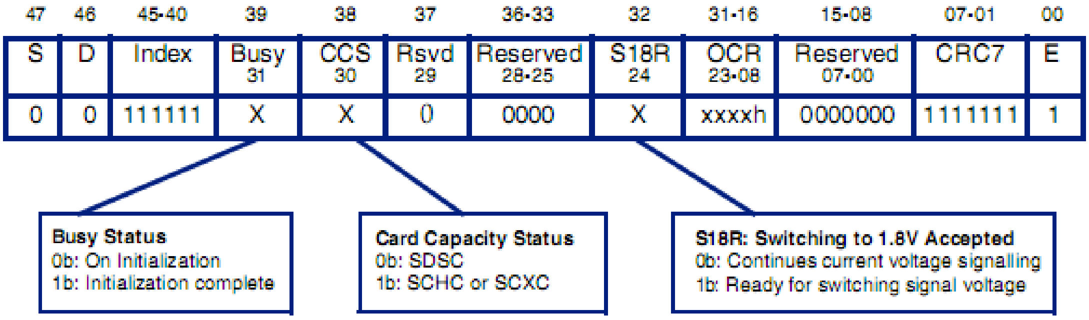


Fig. 3-13 ACMD41 Response(R3)

- Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
- Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
- Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process

4) If the card supports voltage switching, then the software must perform the steps discussed for either the "Voltage Switch Normal Scenario" or the "Voltage Switch Error Scenario".

3.6.3.2 Voltage Switch Normal Scenario

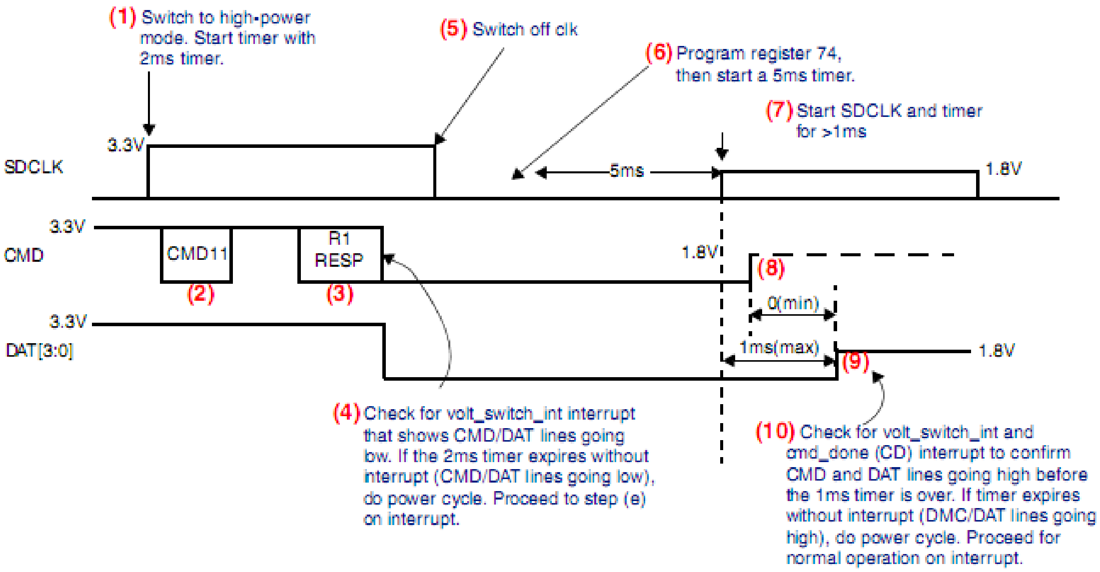


Fig. 3-14 Voltage Switch Normal Scenario

1) The host programs SDMMC_CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2 ms is determined as below: Total cycles required for CMD11 = 48 cycles
   Total cycles required for RESP R1 = 48 cycles
   Maximum clock delay between MCD11 end to start of RESP1 = 60 cycles
   Total = 48+48 + 60 = 160
   Minimum frequency during enumeration is 100 KHz; that is, 10us
   Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms
2) The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to "Boot Operation".
3) The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.
4) The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming SDMMC_CLKENA register

Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be

masked during the voltage switch sequence.
If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle. Proceed to step (5) on interrupt.
1) Program the SDMMC_CLKENA register, with 0 for the corresponding card; the host stops supplying SDCLK.
2) Program Voltage register to the required values for the corresponding card. The application should start a timer > 5ms.
3) After the 5ms timer expires, the host voltage regulator is stable. Program SDMMC_CLKENA register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after Voltage register has been programmed. When the SDMMC_CLKENA register is programmed, the application should start another timer > 1ms.
4) By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).
5) If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms from the start of SDCLK.
6) The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the SDMMC_CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt. After the sequence is completed, the host and the card start communication in SDR12 timing.

3.6.3.3 Voltage Switch Error Scenario

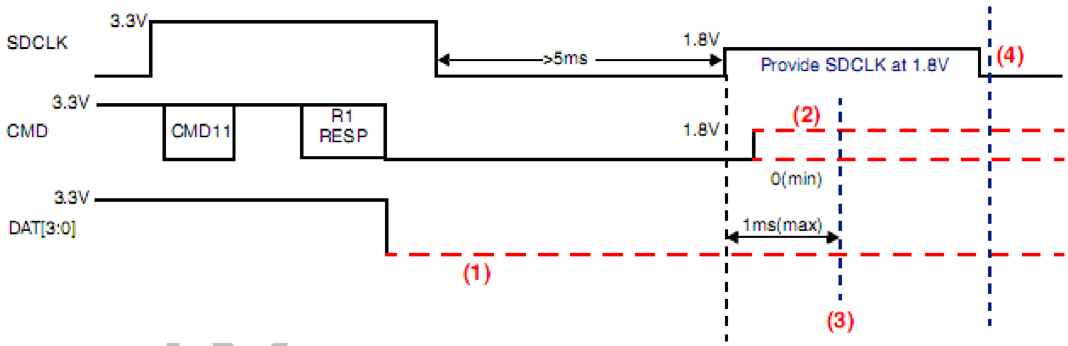


Fig. 3-15 Voltage Switch Error Scenario

1) If the interrupt (VOLT_SWITCH_INT) does not come, then the 2 ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming SDMMC_CLKENA register; no cmd_done (CD) interrupt is generated.

Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in the card keeps driving DAT[3:0] to low until card power off.
2) CMD can be low or tri-state.
3) The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the SDMMC_CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on interrupt.
4) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

- If voltage switching is accepted by the card, the default speed is SDR12.
- Command Done is given:
  - If voltage switching is properly done, CMD and DAT line goes high.
  - If switching is not complete, the 1ms timer expires, and the card clock is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

- The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

3.6.4 DDR Operation

3.6.4.1 4-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

1) Once the voltage switch operation is complete, the user must program voltage selection register to the required values for the corresponding card.
- To start a card to work in DDR mode, the application must program a bit of the newly defined SDMMC_UHSREG[16] register with a value of 1'b1.
- The bit that the user programs depends on which card is to be accessed in DDR mode.
2) To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should SDMMC_UHSREG[16]be set back to 1'b0 for the appropriate card.

3.6.4.2 8-bit DDR Programming Sequence

The following outlines the steps for the 8-bit DDR programming sequence:

1) The cclk_in signal should be twice the speed of the required cclk_out. Thus, if the cclk_out signal is required to be 50 MHz, the cclk_in signal should be 100 MHz.
2) The SDMMC_CLKDIV register should always be programmed with a value higher than zero (0); that is, a clock divider should always be used for 8-bit DDR mode.
3) The application must program the SDMMC_UHSREG[16] register (ddr_reg bits) by assigning it with a value of 1 for the bit corresponding to the card number; this causes the selected card to start working in DDR mode.
4) Depending on the card number, the SDMMC_CTYPE [16] bits should be set in order to make the host work in the 8-bit mode.

3.6.4.3 eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

1) Receiver samples the START bit on the rising edge.
2) On the next rising edge after sampling the START bit, the receiver must sample the data.
3) Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

3.6.4.4 Reset Command/Moving From DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

1) Issue CMD0.
2) When CMD0 is received, the card changes from DDR50 to SDR12.
3) Program the SDMMC_CLKDIV register with an appropriate value.
4) Set ddr_reg to 0.

Note: The Voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

3.6.5 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

The following outlines the steps for the H/W reset programming sequence:
1) Program CMD12 to end any transfer in process.
2) Wait for DTO, even if no response is sent back by the card.
3) Set the following resets:
- DMA reset–SDMMC_CTRL [2] bit
- FIFO reset–SDMMC_CTRL [1] bit

Note: The above steps are required only if a transfer is in process.

4) Program the SDMMC_RSTN register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.
5) Wait for minimum of 1 μs or cclk_in period, whichever is greater
6) After a minimum of 1 μs, the application should program a value of 0 into the SDMMC_RSTN register. This de-asserts the RST_n signal and takes the card out of reset.
7) The application can program a new CMD only after a minimum of 200 μs after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

3.6.6 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:
- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the SDMMC_CTRL[0] bit

3.6.6.1 FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.
- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the SDMMC_BYTCNT=13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

3.6.6.2 Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 3-14 PBL and Watermark Levels

PBL (Number of transfers)	Tx/Rx Watermark Value
1	Greater than or equal to 1
4	Greater than or equal to 4
8	Greater than or equal to 8
16	Greater than or equal to 16
32	Greater than or equal to 32
64	Greater than or equal to 64
128	Greater than or equal to 128
256	Greater than or equal to 256

3.6.7 Variable Delay Usage

The delay time of every element is in the range of 36ps~68ps, varying with different voltage and temperature.

The control signals for variable delay element usage are shown as follows.

3.6.7.1 SDMMC Variable Delay Usage

Table 3-15 Configuration for SDMMC Variable Delay Usage

Signal Name	Source	Default	Description
init_state	CRU_SDMMC_CON0[0]	0	Enable initialization for clock source. 1’b0: Disable 1’b1: Enable When init_state=1, the host clocks including drive clock and sample clock are inactive.
drv_degree[1:0]	CRU_SDMMC_CON0[2:1]	2	Phase selection for drive clock. 2’h0: 0-degree 2’h1: 90-degree 2’h2: 180-degree 2’h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
drv_delaynum[7:0]	CRU_SDMMC_CON0[10:3]	0	Delay element number configuration for drive clock. It can be modified when init_state=1 and should be stable when init_state=0.
drv_sel	CRU_SDMMC_CON0[11]	0	Selection for drive clock: 1’b0: Select clock delayed by phase shift 1’b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
sample_degree[1:0]	CRU_SDMMC_CON1[2:1]	0	Phase selection for sample clock. 2’h0: 0-degree 2’h1: 90-degree 2’h2: 180-degree 2’h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
sample_delaynum[7:0]	CRU_SDMMC_CON1[10:3]	0	Delay element number configuration for sample clock. It can be modified when init_state=1 and should be stable when init_state=0.
sample_sel	CRU_SDMMC_CON1[11]	0	Selection for sample clock: 1’b0: Select clock delayed by phase shift 1’b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.

3.6.7.2 SDIO Variable Delay Usage

Table 3-16 Configuration for SDIO Variable Delay Usage

Signal Name	Source	Default	Description
init_state	CRU_SDIO_CON0[0]	0	Enable initialization for clock

Signal Name	Source	Default	Description
			source. 1'b0: Disable 1'b1: Enable When init_state=1, the host clocks including drive clock and sample clock are inactive.
drv_degree[1:0]	CRU_SDIO_CON0[2:1]	2	Phase selection for drive clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
drv_delaynum [7:0]	CRU_SDIO_CON0[10:3]	0	Delay element number configuration for drive clock. It can be modified when init_state=1 and should be stable when init_state=0.
drv_sel	CRU_SDIO_CON0[11]	0	Selection for drive clock: 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
sample_degree [1:0]	CRU_SDIO_CON1[2:1]	0	Phase selection for sample clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
sample_delaynum[7:0]	CRU_SDIO_CON1[10:3]	0	Delay element number configuration for sample clock. It can be modified when init_state=1 and should be stable when init_state=0.
sample_sel	CRU_SDIO_CON1[11]	0	Selection for sample clock: 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.

The following outlines the steps for clock generation sequence:

1) Assert init_state to soft reset the CLKGEN.
2) Configure drv_degree/sample_degree.
3) If fine adjustment required, delay line can be used by configuring drv_delaynum/sample_delaynum and drv_sel/sample_sel.
4) Dis-assert init_state to start CLKGEN.

3.6.8 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for

the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes-such as DDR50-even though the output delay from the card is less than one cycle.
Command for tuning is different for different cards.

- SD Memory Card:
  - CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.
  - CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.
- Multimedia Card:
  - CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.
  - CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

The following is the procedure for variable delay tuning:

1) Set a phase shift of 0-degree on cclk_in_sample.
2) Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.
3) If the host sees any of the errors—start bit error, data crc error, end bit error, data read time-out, response CRC error, response error—then the sampling point is incorrect.
4) Send CMD12 to bring the host controller state machines to idle.
   - The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.
   - The host controller may generate a response time-out interrupt that must be cleared by software.
5) Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.
6) Mark this phase shift value as the starting point of the sampling window.
7) Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.
8) Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is established, no errors should be visible in the tuning block.

3.6.9 Card Detection Method

There are many methods for SDMMC/SDIO device detection.

- Method1: Using SDMMC_CDETECT register, which is value on card_detect_n input port. 0 represents presence of card. This method is available only for SDMMC/SDIO.
- Method2: Using card detection unit in Host Controller, outputting host interrupt. The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounces associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value in SDMMC_DEBNCE [23:0]. Following figure illustrates the timing for card-detect signals. This method is available only for SDMMC/SDIO.

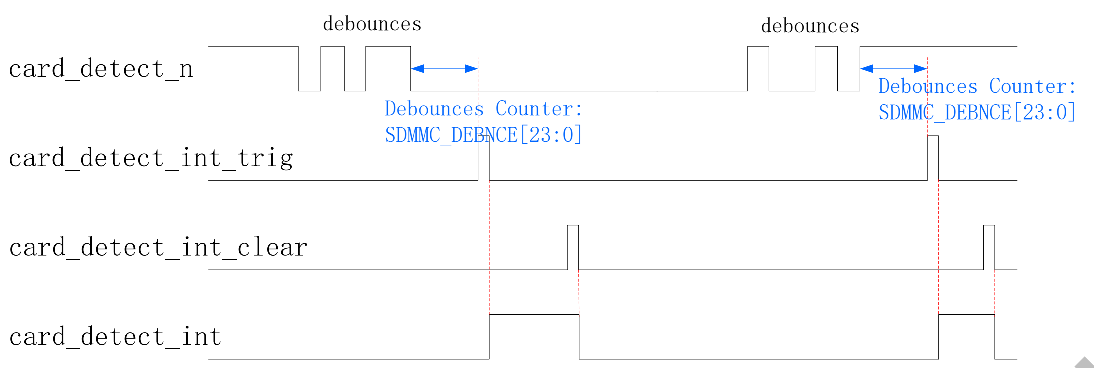


Fig. 3-16 Card Detection Method 2

- Method3: Using general card detection unit, outputting detect_dual_edge_int connecting to IRQ[308]. Similar to Method2, except that the debounce time is configurable by PMU1_GRF_SD_DETECT_CNT; and the insertion/removal detection interrupt can be enabled or cleared respectively.

The detailed register information is:

Table 3-17 Register for SDMMC Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	PMU1_GRF_SD_DETECT_CON[0]	0	Enable SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_fall_edge_detect_en	PMU1_GRF_SD_DETECT_CON[1]	0	Enable SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_rising_edge_dectect_status	PMU1_GRF_SD_DETECT_STS[0]	0	SDMMC detect pin rising edge status. 1'b0: Inactive 1'b1: Active
sd_detect_fall_edge_detect_status	PMU1_GRF_SD_DETECT_STS[1]	0	SDMMC detect pin falling edge status. 1'b0: Inactive 1'b1: Active
sd_detect_rising_edge_dectect_clr	PMU1_GRF_SD_DETECT_CLR[0]	0	Enable clear for SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_fall_edge_detect_clr	PMU1_GRF_SD_DETECT_CLR[1]	0	Enable clear for SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable

3.6.10 SDMMC IOMUX With JTAG

The GPIO4d2/GPIO4d3 for sdmmc_cdata2/sdmmc_cdata3 is shared with jtag_tck/jtag_tms. The condition of usage for SDMMC or JTAG usage is as follows.

- If SYS_GRF_SOC_CON6[14] is equal to 1 and SD/MMC card is not detected within detection time(defined in SYS_GRF_SOC_CON11, in the unit of XIN24M clock), the GPIOs are used for JTAG.
- Otherwise, the GPIOs' usage is defined by IOMUX configuration.

Chapter 4 eMMC Host Controller

4.1 Overview

The eMMC Host Controller is highly programmable, and provides high performance with AXI as the bus interface for data transfer (master interface) and AHB as its slave interface.
It supports following features:

- Supports SD-HCI Host version 4 mode or less
  - Supports same SD-HCI register set for eMMC transfers
  - Supports Command Queuing Engine (CQE) and compliant with eMMC CQ HCI
  - Supports the following data transfer types: CPU, SDMA, AMDM2, ADMA3
- Supports eMMC protocols including eMMC 5.1
  - Supports Auto-tuning
  - Supports 4-bit/8-bit interface
  - Supports legacy, High Speed SDR, High Speed DDR, HS200, and HS400 speed modes
  - Supports boot operation and alternative boot operation
- AHB Slave Interface:
  - Supports 32-bit data width and address width
- AXI Master Interface:
  - Supports 32-bit address width and 64-bit data width
- Phase adjustment:
  - Supports phase auto adjustment for transmit clock, sample clock and data strobe, command output.

4.2 Block Diagram

The Host Controller consists of the following main functional blocks.

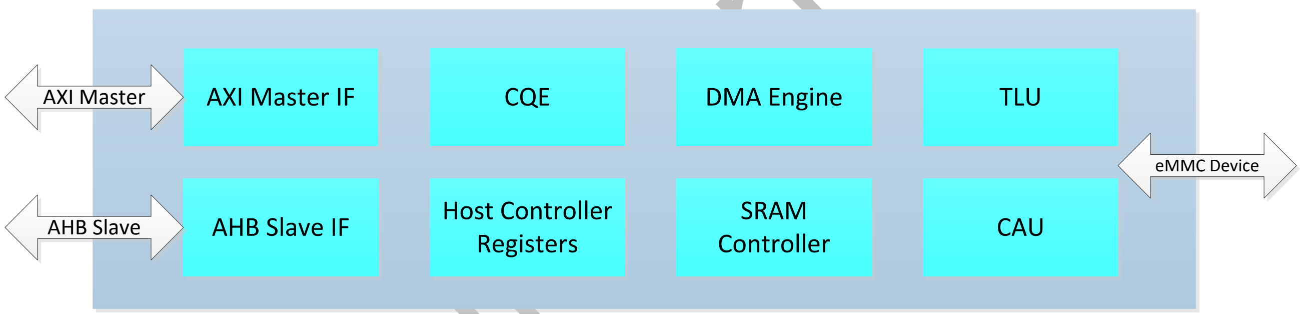


Fig. 4-1 EMMC Host Control Block Diagram

4.3 Function Description

4.3.1 The AXI Master Bus Interface Unit

This Master Bus Interface Unit implements the logic to transfer data on the AMBA Extensible Interface Bus (AXI) bus. The AXI interface transfers data to and from the system memory through the AXI master bus interface, respectively.

4.3.2 The AHB Slave Bus Interface Unit

The AHB slave bus interface module implements the logic to primarily access the host registers by using an external AMBA high-performance (AHB) bus.

4.3.3 Host Controller Registers

The host controller register unit comprises of the standard SD host controller registers as specified in the SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20a. It also includes Command Queuing registers compliance to JEDEC eMMC 5.1 HCI specification.

4.3.4 DMA Engine

The DMA Engine unit handles data transfer between the host and system memory.

- Support SDMA/ADMA2/ADMA3 modes
- Fetch the descriptor and data
- The same DMA engine is used to interleave data transfer and descriptor fetch. This enables new task descriptor fetches (for CMD44 and CMD45) while DMA is moving data during task execution (for CMD46 and CMD47).

- The AXI transaction ID 0 is used for moving data and AXI transaction ID 1 is used to fetch task descriptors.
- Pre-fetch data for back-to-back eMMC write commands
- Write back the received data packets to the system memory

4.3.5 SRAM Controller

The SRAM controller interfaces the packet buffer of the host and the transaction controller units. The SRAM is a single clock single-port RAM synchronous to the core base clock. The width is 64-bit, the depth is 288-location.

4.3.6 Command Queuing Engine

This module implements command queuing and includes the following:

- Task scheduler with the ability to prioritize execution of tasks
- Control logic for descriptor fetch
- Control and sequence task submission and execution
- Status polling
- Timers and counter dedicated for CQE operation
- Interrupt coalescing logic

4.3.7 Transfer Level Unit

The TLU manages the command/response and data flow for communication with memory cards.

4.3.8 Clock Adjustment Unit

The clock adjustment unit (CAU) will detect the clock period and get the delay precision, adjust the clock phase base on the dedicate delay element. Also, you can program the register to set the delay precision. The flowing signals supports adjustment: transmit clock, sample clock and data strobe, command output.

4.4 Register Description

4.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EMMC_SDMASA	0x0000	W	0x00000000	SDMA System Address Register
EMMC_BLOCKSIZE	0x0004	HW	0x00000000	Block Size Register
EMMC_BLOCKCOUNT	0x0006	HW	0x00000000	Block Count Register
EMMC_ARGUMENT	0x0008	W	0x00000000	Argument Register
EMMC_XFER_MODE	0x000C	HW	0x00000000	Transfer Mode Register
EMMC_CMD	0x000E	HW	0x00000000	Command Register
EMMC_RESP01	0x0010	W	0x00000000	Response Register 0/1
EMMC_RESP23	0x0014	W	0x00000000	Response Register 2/3
EMMC_RESP45	0x0018	W	0x00000000	Response Register 4/5
EMMC_RESP67	0x001C	W	0x00000000	Response Register 6/7
EMMC_BUF_DATA	0x0020	W	0x00000000	Buffer Data Port Register
EMMC_PSTATE	0x0024	W	0x19FF0000	Present State Register
EMMC_HOST_CTRL1	0x0028	B	0x00000000	Host Control 1 Register
EMMC_PWR_CTRL	0x0029	B	0x00000000	Power Control Register
EMMC_BGAP_CTRL	0x002A	B	0x00000000	Block Gap Control Register
EMMC_CLK_CTRL	0x002C	HW	0x00000000	Clock Control Register
EMMC_TOUT_CTRL	0x002E	B	0x00000000	Timeout Control Register
EMMC_SW_RST	0x002F	B	0x00000000	Software Reset Register
EMMC_NORMAL_INT_STAT	0x0030	HW	0x00000000	Normal Interrupt Status Register
EMMC_ERROR_INT_STAT	0x0032	HW	0x00000000	Error Interrupt Status Register
EMMC_NORMAL_INT_STAT_EN	0x0034	HW	0x00000000	Normal Interrupt Status Enable Register
EMMC_ERROR_INT_STAT_EN	0x0036	HW	0x00000000	Error Interrupt Status Enable Register
EMMC_NORMAL_INT_SIGNAL_EN	0x0038	HW	0x00000000	Normal Interrupt Signal Enable Register

Name	Offset	Size	Reset Value	Description
EMMC_ERROR_INT_SIGNAL_EN	0x003A	HW	0x00000000	Error Interrupt Signal Enable Register
EMMC_AUTO_CMD_STAT	0x003C	HW	0x00000000	Auto CMD Error Status Register
EMMC_HOST_CTRL2	0x003E	HW	0x00000000	Host Control 2 Register
EMMC_CAPABILITIES1	0x0040	W	0x40EDC880	Capabilities Register 1
EMMC_CAPABILITIES2	0x0044	W	0x000A2077	Capabilities Register 2
EMMC_FORCE_AUTO_CMD_STAT	0x0050	HW	0x00000000	Force Event Register for Auto CMD Error Status Register
EMMC_FORC_ERR_INT_STAT	0x0052	HW	0x00000000	Force Event Register for Error Interrupt Status Register
EMMC_ADMA_ERR_STAT	0x0054	B	0x00000000	ADMA Error Status Register
EMMC_ADMA_SA	0x0058	W	0x00000000	ADMA System Address Register
EMMC_PRESET_INIT	0x0060	HW	0x00000000	Preset Value for Initialization Register
EMMC_PRESET_DS	0x0062	HW	0x00000000	Preset Value for Default Speed Register
EMMC_PRESET_HS	0x0064	HW	0x00000000	Preset Value for High Speed Register
EMMC_PRESET_SDR12	0x0066	HW	0x00000000	Preset Value for SDR12 Register
EMMC_PRESET_SDR25	0x0068	HW	0x00000000	Preset Value for SDR25 Register
EMMC_PRESET_SDR50	0x006A	HW	0x00000000	Preset Value for SDR50 Register
EMMC_PRESET_SDR104	0x006C	HW	0x00000000	Preset Value for SDR104 Register
EMMC_PRESET_DDR50	0x006E	HW	0x00000000	Preset Value for DDR50 Register
EMMC_ADMA_ID	0x0078	W	0x00000000	ADMA3 Integrated Descriptor Address Register
EMMC_SLOT_INTR_STATUS	0x00FC	HW	0x00000000	Slot Interrupt Status Register
EMMC_HOST_CNTRL_VERS	0x00FE	HW	0x00001005	Host Controller Version Register
EMMC_CQVER	0x0180	W	0x00000510	Command Queuing Version Register
EMMC_CQCAP	0x0184	W	0x00000000	Command Queuing Capabilities Register
EMMC_CQCFG	0x0188	W	0x00000000	Command Queuing Configuration Register
EMMC_CQCTRL	0x018C	W	0x00000000	Command Queuing Control Register
EMMC_CQIS	0x0190	W	0x00000000	Command Queuing Interrupt Status Register
EMMC_CQISE	0x0194	W	0x00000000	Command Queuing Interrupt Status Enable Register
EMMC_CQISGE	0x0198	W	0x00000000	Command Queuing Interrupt Signal Enable Register
EMMC_CQIC	0x019C	W	0x00000000	Command Queuing Interrupt Coalescing Register
EMMC_CQTDLBA	0x01A0	W	0x00000000	Command Queuing Task Descriptor List Base Address Register
EMMC_CQTDBR	0x01A8	W	0x00000000	Command Queuing Door Bell Register
EMMC_CQTCN	0x01AC	W	0x00000000	Command Queuing Task Clear Notification Register

Name	Offset	Size	Reset Value	Description
EMMC_CQDQS	0x01B0	W	0x00000000	Command Queuing Device Queue Status Register
EMMC_CQDPT	0x01B4	W	0x00000000	Command Queuing Device Pending Tasks Register
EMMC_CQTCLR	0x01B8	W	0x00000000	Command Queuing Task Clear Register
EMMC_CQSSC1	0x01C0	W	0x00011000	Command Queuing Send Status Configuration 1 Register
EMMC_CQSSC2	0x01C4	W	0x00000000	Command Queuing Send Status Configuration 2 Register
EMMC_CQCRDCT	0x01C8	W	0x00000000	Command Queuing Command Response For Direct Command Register
EMMC_CQRMEM	0x01D0	W	0xFDF9A080	Command Queuing Command Response Mode Error Mask Register
EMMC_CQTERRI	0x01D4	W	0x00000000	Command Queuing Task Error Information Register
EMMC_CQCRI	0x01D8	W	0x00000000	Command Queuing Command Response Index Register
EMMC_CQCRA	0x01DC	W	0x00000000	Command Queuing Command Response Argument Register
EMMC_VER_ID	0x0500	W	0x00000000	Host Version ID Register
EMMC_VER_TYPE	0x0504	W	0x00000000	Host Version Type Register
EMMC_HOST_CTRL3	0x0508	B	0x00000000	Host Control 3 Register
EMMC_EMMC_CTRL	0x052C	HW	0x00000004	EMMC Control Register
EMMC_BOOT_CTRL	0x052E	HW	0x00000000	Boot Control Register
EMMC_AT_CTRL	0x0540	W	0x00000000	Tuning Control Register
EMMC_AT_STAT	0x0544	W	0x00000000	Tuning Status Register
EMMC_DLL_CTRL	0x0800	W	0x00000000	DLL Global Control Register
EMMC_DLL_RXCLK	0x0804	W	0x00000000	DLL Control Register For Receive Clock
EMMC_DLL_TXCLK	0x0808	W	0x00000000	DLL Control Register For Transmit Clock
EMMC_DLL_STRBIN	0x080C	W	0x00000000	DLL Control Register For Strobe Input
EMMC_DLL_CMDOUT	0x0810	W	0x00000000	DLL Control Register For Command Output
EMMC_DLL_STATUS0	0x0840	W	0x00000000	DLL Status Register 0
EMMC_DLL_STATUS1	0x0844	W	0x00000000	DLL Status Register 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.4.2 Detail Register Description

EMMC_SDMASA

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BLOCKCNT_SDMASA 32-bit Block Count (SDMA System Address). 1. SDMA System Address (Host Version 4 Enable = 0): This register contains the system memory address for an SDMA transfer in the 32-bit addressing mode. When the Host Controller stops an SDMA transfer, this register points to the system address of the next contiguous data position. It can be accessed only if no transaction is executing. Reading this register during data transfers may return an invalid value. 2. 32-bit Block Count (Host Version 4 Enable = 1): From the Host Controller Version 4.10 specification, this register is redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block transfer and the data transfer stops when the count reaches zero. This register must be accessed when no transaction is executing. Reading this register during data transfers may return invalid value. Values: 32'hFFFFFFFF: 1 Block ...... 32'h00000002: 2 Blocks 32'h00000001: 1 Block 32'h00000000: Stop Count Note: a. For Host Version 4 Enable = 0, the Host driver does not program the system address in this register while operating in ADMA mode. The system address must be programmed in the ADMA System Address register. b. For Host Version 4 Enable = 0, the Host driver programs a non-zero 32-bit block count value in this register when Auto CMD23 is enabled for non-DMA and ADMA modes. Auto CMD23 cannot be used with SDMA. c. This register must be programmed with a non-zero value for data transfer if the 32-bit Block count register is used instead of the 16-bit Block count register.

EMMC_BLOCKSIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x0	SDMA_BUF_BDARY SDMA Buffer Boundary. These bits specify the size of contiguous buffer in system memory. The SDMA transfer waits at every boundary specified by these fields and the Host Controller generates the DMA interrupt to request the Host Driver to update the SDMA System Address register. Values: 3'h0: 4K bytes SDMA Buffer Boundary 3'h1: 8K bytes SDMA Buffer Boundary 3'h2: 16K bytes SDMA Buffer Boundary 3'h3: 32K bytes SDMA Buffer Boundary 3'h4: 64K bytes SDMA Buffer Boundary 3'h5: 128K bytes SDMA Buffer Boundary 3'h6: 256K bytes SDMA Buffer Boundary 3'h7: 512K bytes SDMA Buffer Boundary

Bit	Attr	Reset Value	Description
11:0	RW	0x000	XFER_BLOCK_SIZE Transfer Block Size. These bits specify the block size of data transfers. In case of memory, it is set to 512 bytes. It can be accessed only if no transaction is executing. Read operations during transfers may return an invalid value, and write operations are ignored. Values: 12'h1: 1 byte 12'h2: 2 bytes 12'h3: 3 bytes ...... 12'h1FF: 511 byte 12'h200: 512 bytes ...... 12'h800: 2048 bytes Note: This register must be programmed with a non-zero value for data transfer.

EMMC_BLOCKCOUNT

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	BLOCK_CNT 16-bit Block Count. If the Host Version 4 Enable bit is set 0 or the 16-bit Block Count register is set to non-zero, the 16-bit Block Count register is selected. If the Host Version 4 Enable bit is set 1 and the 16-bit Block Count register is set to zero, the 32-bit Block Count register is selected. Values: 16'h0: Stop Count 16'h1: 1 Block 16'h2: 2 Blocks ...... 16'hFFFF: 65535 Blocks Note: For Host Version 4 Enable = 0, this register must be set to 0 before programming the 32-bit block count register when Auto CMD23 is enabled for non-DMA and ADMA modes.

EMMC_ARGUMENT

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARGUMENT Command Argument. These bits specify the SD/eMMC command argument that is specified in bits 39-8 of the Command format.

EMMC_XFER_MODE

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	RESP_INT_DISABLE Response Interrupt Disable. The Host Controller supports response check function to avoid overhead of response error check by the Host driver. Response types of only R1 and R5 can be checked by the Controller. If Host Driver checks the response error, set this bit to 0 and wait for Command Complete Interrupt and then check the response register. If the Host Controller checks the response error, set this bit to 1 and set the Response Error Check Enable bit to 1. The Command Complete Interrupt is disabled by this bit regardless of the Command Complete Signal Enable. Note: During tuning (when the Execute Tuning bit in the Host Control2 register is set), the Command Complete Interrupt is not generated irrespective of the Response Interrupt Disable setting. Values: 1'b0: Response Interrupt is enabled 1'b1: Response Interrupt is disabled
7	RW	0x0	RESP_ERR_CHK_ENABLE Response Error Check Enable. The Host Controller supports response check function to avoid overhead of response error check by Host driver. Response types of only R1 and R5 can be checked by the Controller. If the Host Controller checks the response error, set this bit to 1 and set Response Interrupt Disable to 1. If an error is detected, the Response Error interrupt is generated in the Error Interrupt Status register. Note: a. Response error check must not be enabled for any response type other than R1 and R5. b. Response check must not be enabled for the tuning command. Values: 1'b0: Response Error Check is disabled 1'b1: Response Error Check is enabled
6	RW	0x0	RESP_TYPE Response Type R1/R5. This bit selects either R1 or R5 as a response type when the Response Error Check is selected. Values: 1'b0: R1 1'b1: R5
5	RW	0x0	MULTI_BLK_SEL Multi/Single Block Select. This bit is set when issuing multiple-block transfer commands using the DAT line. If this bit is set to 0, it is not necessary to set the Block Count register. Values: 1'b0: Single Block 1'b1: Multiple Block

Bit	Attr	Reset Value	Description
4	RW	0x0	DATA_XFER_DIR Data Transfer Direction Select. This bit defines the direction of DAT line data transfers. This bit is set to 1 by the Host Driver to transfer data from the SD/eMMC card to the Host Controller and it is set to 0 for all other commands. Values: 1'b0: Write (Host to Card) 1'b1: Read (Card to Host)
3:2	RW	0x0	AUTO_CMD_ENABLE Auto Command Enable. This field determines use of Auto Command functions. Values: 2'h0: Auto Command Disabled 2'h1: Auto CMD12 Enable 2'h2: Auto CMD23 Enable 2'h3: Auto CMD Auto Select
1	RW	0x0	BLOCK_COUNT_ENABLE Block Count Enable. This bit is used to enable the Block Count register, which is relevant for multiple block transfers. If this bit is set to 0, the Block Count register is disabled, which is useful in executing an infinite transfer. The Host Driver must set this bit to 0 when ADMA is used. Values: 1'b0: Disable 1'b1: Enable
0	RW	0x0	DMA_ENABLE DMA Enable. This bit enables the DMA functionality. If this bit is set to 1, a DMA operation begins when the Host Driver writes to the Command register. You can select one of the DMA modes by using DMA Select in the Host Control 1 register. Values: 1'b0: No data transfer or Non-DMA data transfer 1'b1: DMA Data transfer

EMMC_CMD

Address: Operational Base + offset (0x000E)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:8	RW	0x00	CMD_INDEX Command Index. These bits are set to the command number that is specified in bits 45-40 of the command format.

Bit	Attr	Reset Value	Description
7:6	RW	0x0	CMD_TYPE Command Type. These bits indicate the command type. Note: While issuing Abort CMD using CMD12/CMD52 or reset CMD using CMD0/CMD52, CMD_TYPE field shall be set to 0x3. Values: 2'h0: Normal 2'h1: Suspend 2'h2: Resume 2'h3: Abort
5	RW	0x0	DATA_PRESENT_SEL Data Present Select. This bit is set to 1 to indicate that data is present and that the data is transferred using the DAT line. This bit is set to 0 in the following instances: a. Command using the CMD line b. Command with no data transfer but using busy signal on the DAT[0] line c. Resume Command Values: 1'b0: No Data Present 1'b1: Data Present
4	RW	0x0	CMD_IDX_CHK_ENABLE Command Index Check Enable. This bit enables the Host Controller to check the index field in the response to verify if it has the same value as the command index. If the value is not the same, it is reported as a Command Index error. Note: a. Index check enable must be set to 0 for the command with no response, R2 response, R3 response and R4 response. b. For the tuning command, this bit must always be set to enable the index check. Values: 1'b0: Disable 1'b1: Enable
3	RW	0x0	CMD_CRC_CHK_ENABLE Command CRC Check Enable. This bit enables the Host Controller to check the CRC field in the response. If an error is detected, it is reported as a Command CRC error. Note: a. CRC check enable must be set to 0 for the command with no response, R3 response, and R4 response. b. For the tuning command, this bit must always be set to 1 to enable the CRC check. Values: 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	SUB_CMD_FLAG Sub Command Flag. This bit distinguishes between a main command and a sub command. Values: 1'b0: Main Command 1'b1: Sub Command
1:0	RW	0x0	RESP_TYPE_SELECT Response Type Select. This bit indicates the type of response expected from the card. Values: 2'h0: No Response 2'h1: Response length 136 2'h2: Response length 48 2'h3: Response length 48, check Busy after response.

EMMC_RESP01

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP01 Command Response. These bits reflect 39-8 bits of SD/eMMC Response Field. Note: For Auto CMD, the 32-bit response (bits 39-8 of the Response Field) is updated in the RESP67 register.

EMMC_RESP23

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP23 Command Response. These bits reflect 71-40 bits of the SD/eMMC Response Field.

EMMC_RESP45

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	RESP45 Command Response. These bits reflect 103-72 bits of the Response Field.

EMMC_RESP67

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP67 Command Response These bits reflect bits 135-104 of SD/EMMC Response Field. For Auto CMD, this register also reflects the 32-bit response (bits 39-8 of the Response Field).

EMMC_BUF_DATA

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BUF_DATA Buffer Data. These bits enable access to the Host Controller packet buffer.

EMMC_PSTATE

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x1	SUB_CMD_STAT Sub Command Status. This bit is used to distinguish between a main command and a sub command status. Values: 1'b0: Main Command Status 1'b1: Sub Command Status
27	RO	0x1	CMD_ISSUE_ERR Command Not Issued by Error. This bit is set if a command cannot be issued after setting the command register due to an error except the Auto CMD12 error. Values: 1'b0: No error for issuing a command 1'b1: Command cannot be issued
26:25	RO	0x0	reserved
24	RO	0x1	CMD_LINE_LVL Command-Line Signal Level. This bit is used to check the CMD line level to recover from errors and for debugging.
23:20	RO	0xf	DAT_3_0 DAT[3:0] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging.
19	RO	0x1	WR_PROTECT_SW_LVL Write Protect Switch Pin Level. This bit is supported only for memory and combo cards. Values: 1'b0: Write protected 1'b1: Write enabled
18	RO	0x1	CARD_DETECT_PIN_LEVEL Card Detect Pin Level. Values: 1'b0: No card present 1'b1: Card Present
17	RO	0x1	CARD_STABLE Card Stable. This bit indicates the stability of the Card Detect Pin Level. A card is not detected if this bit is set to 1 and the value of the CARD_INSERTED bit is 0. Values: 1'b0: Reset or Debouncing 1'b1: No Card or Inserted
16	RO	0x1	CARD_INSERTED Card Inserted. This bit indicates whether a card has been inserted. The Host Controller debounces this signal so that Host Driver need not wait for it to stabilize. Values: 1'b0: Reset, Debouncing, or No card 1'b1: Card Inserted
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RO	0x0	BUF_RD_ENABLE Buffer Read Enable. This bit is used for non-DMA transfers. This bit is set if valid data exists in the Host buffer. Values: 1'b0: Read disable 1'b1: Read enable
10	RO	0x0	BUF_WR_ENABLE Buffer Write Enable. This bit is used for non-DMA transfers. This bit is set if space is available for writing data. Values: 1'b0: Write disable 1'b1: Write enable
9	RW	0x0	RD_XFER_ACTIVE Read Transfer Active. This bit indicates whether a read transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
8	RO	0x0	WR_XFER_ACTIVE Write Transfer Active. This status indicates whether a write transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
7:4	RO	0x0	DAT_7_4 DAT[7:4] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging.
3	RO	0x0	RE_TUNE_REQ Re-Tuning Request. Host Controller does not generate retuning request. The software must maintain the Retuning timer.
2	RO	0x0	DAT_LINE_ACTIVE DAT Line Active (SD/eMMC Mode only). This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use. In the case of read transactions, this bit indicates whether a read transfer is executing on the SD/eMMC bus. In the case of write transactions, this bit indicates whether a write transfer is executing on the SD/eMMC bus. For a command with busy, this status indicates whether the command executing busy is executing on an SD/eMMC bus. Values: 1'b0: DAT Line Inactive 1'b1: DAT Line Active

Bit	Attr	Reset Value	Description
1	RO	0x0	CMD_INHIBIT_DAT Command Inhibit (DAT). This bit is applicable for SD/eMMC mode and is generated if either DAT line active or Read transfer active is set to 1. If this bit is set to 0, it indicates that the Host Controller can issue subsequent SD/eMMC commands. Values: 1'b0: Can issue command which used DAT line 1'b1: Cannot issue command which used DAT line
0	RO	0x0	CMD_INHIBIT Command Inhibit (CMD). If this bit is set to 0, it indicates that the CMD line is not in use and the Host controller can issue an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command. Values: 1'b0: Host Controller is ready to issue a command 1'b1: Host Controller is not ready to issue a command

EMMC_HOST_CTRL1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
7	RW	0x0	CARD_DETECT_SIG_SEL Card Detect Signal Selection. This bit selects a source for card detection. When the source for the card detection is switched, the interrupt must be disabled during the switching period. Values: 1'b0: Card Detect Signal is selected (for normal use) 1'b1: Card Detect Test Level is selected (for test purpose)
6	RW	0x0	CARD_DETECT_TEST_LVL Card Detect Test Level. This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates whether a card inserted or not. Values: 1'b0: No Card 1'b1: Card Inserted
5	RW	0x0	EXT_DAT_XFER Extended Data Transfer Width. This bit controls 8-bit bus width mode of embedded device. Values: 1'b0: Bus Width is selected by the Data Transfer Width 1'b1: 8-bit Bus Width

Bit	Attr	Reset Value	Description
4:3	RW	0x0	DMA_SEL DMA Select. This field is used to select the DMA type. When Host Version 4 Enable is 1 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected When Host Version 4 Enable is 0 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: 32-bit Address ADMA2 is selected 2'h3: Reserved Values: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected
2	RW	0x0	HIGH_SPEED_EN High Speed Enable. In SD/eMMC mode, this bit is used to determine the selection of pre-set value for High Speed mode. Before setting this bit, the Host Driver checks the High Speed Support in the Capabilities register. Values: 1'b0: Normal Speed mode 1'b1: High Speed mode
1	RW	0x0	DAT_XFER_WIDTH Data Transfer Width. For SD/eMMC mode, this bit selects the data transfer width of the Host Controller. The Host Driver sets it to match the data width of the SD/eMMC card. Values: 1'b0: 1-bit mode 1'b1: 4-bit mode
0	RO	0x0	reserved

EMMC_PWR_CTRL

Address: Operational Base + offset (0x0029)

Bit	Attr	Reset Value	Description
7:1	RO	0x00	reserved
0	RW	0x0	SD_BUS_PWR If this bit is cleared, the Host Controller stops the SD Clock by clearing the SD_CLK_IN bit in the EMMC_CLK_CTRL register. Values: 1'b0: Power off 1'b1: Power on

EMMC_BGAP_CTRL

Address: Operational Base + offset (0x002A)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	INT_AT_BGAP Interrupt At Block Gap. This bit is valid only in the 4-bit mode of an SDIO card and is used to select a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer.
2	RW	0x0	RD_WAIT_CTRL Read Wait Control. This bit is used to enable the read wait protocol to stop read data using DAT[2] line if the card supports read wait. Otherwise, the Host Controller has to stop the card clock to hold the read data. Values: 1'b0: Disable Read Wait Control 1'b1: Enable Read Wait Control
1	RW	0x0	CONTINUE_REQ Continue Request. This bit is used to restart the transaction, which was stopped using the Stop At Block Gap Request. The Host Controller automatically clears this bit when the transaction restarts. If stop at block gap request is set to 1, any write to this bit is ignored. Values: 1'b0: No Affect 1'b1: Restart
0	RW	0x0	STOP_BG_REQ Stop At Block Gap Request. This bit is used to stop executing read and write transactions at the next block gap for non-DMA, SDMA, and ADMA transfers. Values: 1'b0: Transfer 1'b1: Stop

EMMC_CLK_CTRL

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	FREQ_SEL SDCLK Frequency Select. These bits specify the lower 8 bits of 10-bit SDCLK Frequency Select control. These bits are used to select the frequency of the SDCLK signal. These bits depend on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, these bits are set by the Host Driver. If Preset Value Enable = 1, these bits are automatically set to a value specified in one of the Preset Value register. 1. 10-bit Divided Clock Mode: 10'h000: Base clock (10MHz - 255 MHz) 10'h001: 1/2 Divided Clock 10'h002: 1/4 Divided Clock ...... 10'h3ff: 1/2046 Divided clock 2. Programmable Clock Mode: 10'h000: Base clock * M 10'h001: Base clock * M /2 10'h002: Base clock * M /3 ...... 10'h3ff: Base clock * M /1024

Bit	Attr	Reset Value	Description
7:6	RW	0x0	UPPER_FREQ_SEL These bits specify the upper 2 bits of 10-bit SDCLK Frequency Select control.
5	RW	0x0	CLK_GEN_SELECT Clock Generator Select. This bit is used to select the clock generator mode in SDCLK Frequency Select. If Preset Value Enable = 0, this bit is set by the Host Driver. If Preset Value Enable = 1, this bit is automatically set to a value specified in one of the Preset Value registers. Values: 1'b0: Divided Clock Mode 1'b1: Programmable Clock Mode
4:3	RO	0x0	reserved
2	RW	0x0	SD_CLK_EN SD/eMMC Clock Enable. This bit stops the SDCLK when set to 0. The SDCLK Frequency Select bit can be changed when this bit is set to 0. Values: 1'b0: Disable providing SDCLK 1'b1: Enable providing SDCLK
1	RO	0x0	INTERNAL_CLK_STABLE Internal Clock Stable. Values: 1'b0: Not Ready 1'b1: Ready
0	RW	0x0	INTERNAL_CLK_EN Internal Clock Enable. This bit is set to 0 when the Host Driver is not using the Host Controller. The Host Controller must stop its internal clock to enter a very low power state. However, registers can still be read and written to. Note: If this bit is not used to control the internal clock (base clock and master clock), it is recommended to set this bit to 1. Values: 1'b0: Stop 1'b1: Oscillate

EMMC_TOUT_CTRL

Address: Operational Base + offset (0x002E)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	TOUT_CNT Data Timeout Counter Value. This value determines the interval by which DAT line timeouts are detected. Timeout clock frequency will be generated by dividing the base clock TMCLK by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). Values: 4'h0: TMCLK * 2^13 4'h1: TMCLK * 2^14 ...... 4'he: TMCLK * 2^27 4'hf: Reserved

EMMC_SW_RST

Address: Operational Base + offset (0x002F)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved
2	RW	0x0	SW_RST_DAT Software Reset For DAT line. This bit is used in SD/eMMC mode and it resets only a part of the data circuit and the DMA circuit is also reset. The following registers and bits are cleared by this bit: a. Buffer Data Port register: Buffer is cleared and initialized. b. Present state register: Buffer Read Enable Buffer Write Enable Read Transfer Active Write Transfer Active DAT Line Active Command Inhibit (DAT) c. Block Gap Control register: Continue Request Stop At Block Gap Request d. Normal Interrupt status register: Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete Values: 1'b0: Work 1'b1: Reset

Bit	Attr	Reset Value	Description
1	RW	0x0	SW_RST_CMD Software Reset For CMD line. This bit resets only a part of the command circuit to be able to issue a command. This reset is effective only for a command issuing circuit (including response error statuses related to Command Inhibit (CMD) control) and does not affect the data transfer circuit. Host Controller can continue data transfer even after this reset is executed while handling subcommand-response errors. The following registers and bits are cleared by this bit: a. Present State register - Command Inhibit (CMD) bit b. Normal Interrupt Status register - Command Complete bit c. Error Interrupt Status - Response error statuses related to Command Inhibit (CMD) bit Values: 1'b0: Work 1'b1: Reset
0	RW	0x0	SW_RST_ALL Software Reset For All. This reset affects the entire Host Controller except for the card detection circuit. During its initialization, the Host Driver sets this bit to 1 to reset the Host Controller. All registers are reset except the capabilities register. If this bit is set to 1, the Host Driver must issue reset command and reinitialize the card. Values: 1'b0: Work 1'b1: Reset

EMMC_NORMAL_INT_STAT

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
15	RO	0x0	ERROR_INT_STAT Error Interrupt. If any of the bits in the Error Interrupt Status register are set, then this bit is set. Values: 1'b0: No Error 1'b1: Error
14	RC/W1C	0x0	CQE_EVENT Command Queuing Event. This status is set if Command Queuing/Crypto related event has occurred in eMMC/SD mode. Read CQHCI's CQIS/CRNQIS register for more details. Values: 1'b0: No Event 1'b1: Command Queuing Event is detected Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
13	RO	0x0	FX_EVENT FX Event. This status is set when R[14] of response register is set to 1 and Response Type R1/R5 is set to 0 in Transfer Mode register. This interrupt is used with response check function. Values: 1'b0: No Event 1'b1: FX Event is detected

Bit	Attr	Reset Value	Description
12	RO	0x0	RE_TUNE_EVENT Re-tuning Event. This bit is set if the Re-Tuning Request changes from 0 to 1. Re-Tuning request is not supported.
11:9	RO	0x0	reserved
8	RO	0x0	CARD_INTERRUPT Card Interrupt. This bit reflects the synchronized value of DAT[1] Interrupt Input for SD Mode. Values: 1'b0: No Card Interrupt 1'b1: Generate Card Interrupt
7	RC/W1C	0x0	CARD_REMOVAL Card Removal. This bit is set if the Card Inserted in the Present State register changes from 1 to 0. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Removed Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
6	RC/W1C	0x0	CARD_INSERTION Card Insertion. This bit is set if the Card Inserted in the Present State register changes from 0 to 1. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Inserted Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
5	RC/W1C	0x0	BUF_RD_READY Buffer Read Ready. This bit is set if the Buffer Read Enable changes from 0 to 1. Values: 1'b0: Not ready to read buffer 1'b1: Ready to read buffer Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
4	RC/W1C	0x0	BUF_WR_READY Buffer Write Ready. This bit is set if the Buffer Write Enable changes from 0 to 1. Values: 1'b0: Not ready to write buffer 1'b1: Ready to write buffer Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.

Bit	Attr	Reset Value	Description
3	RC/W1C	0x0	DMA_INTERRUPT DMA Interrupt. This bit is set if the Host Controller detects the SDMA Buffer Boundary during transfer. In case of ADMA, by setting the Int field in the descriptor table, the Host controller generates this interrupt. This interrupt is not generated after a Transfer Complete. Values: 1'b0: No DMA Interrupt 1'b1: DMA Interrupt is generated Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
2	RC/W1C	0x0	BGAP_EVENT Block Gap Event. This bit is set when both read/write transaction is stopped at block gap due to a Stop at Block Gap Request. Values: 1'b0: No Block Gap Event 1'b1: Transaction stopped at block gap Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
1	RC/W1C	0x0	XFER_COMPLETE Transfer Complete. This bit is set when a read/write transfer and a command with status busy is completed. Values: 1'b0: Not complete 1'b1: Command execution is completed Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
0	RC/W1C	0x0	CMD_COMPLETE Command Complete. In an SD/eMMC Mode, this bit is set when the end bit of a response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt Disable in Transfer Mode Register is set to 1. Values: 1'b0: No Command Complete 1'b1: Command Complete Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.

EMMC_ERROR_INT_STAT

Address: Operational Base + offset (0x0032)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RC/W1C	0x0	BOOT_ACK_ERR Boot Acknowledgement Error. This bit is set when there is a timeout for boot acknowledgement or when detecting boot acknowledgement status having a value other than 3'b010. This is applicable only when boot acknowledgement is expected in eMMC mode. Values: 1'b0: No Error 1'b1: Error

Bit	Attr	Reset Value	Description
11	RC/W1C	0x0	RESP_ERR Response Error Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1. Values: 1'b0: No Error 1'b1: Error
10	RC/W1C	0x0	TUNING_ERR Tuning Error. This bit is set when an unrecoverable error is detected in a tuning circuit except during the tuning procedure (occurrence of an error during tuning procedure is indicated by Sampling Clock Select in the Host Control 2 register). By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock Select is set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver must discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from the tuning circuit error. Values: 1'b0: No Error 1'b1: Error
9	RC/W1C	0x0	ADMA_ERR ADMA Error. This bit is set when the Host Controller detects error during ADMA-based data transfer. The error could be due to following reasons: a. Error response received from System bus b. ADMA3,ADMA2 Descriptors invalid c. CQE Task or Transfer descriptors invalid When the error occurs, the state of the ADMA is saved in the ADMA Error Status register. In eMMC CQE mode: The Host Controller generates this Interrupt when it detects an invalid descriptor data at the Fetch Descriptor state. ADMA Error State in the ADMA Error Status indicates that an error has occurred in Fetch Descriptor state. The Host Driver may find that Valid bit is not set at the error descriptor. Values: 1'b0: No Error 1'b1: Error

Bit	Attr	Reset Value	Description
8	RC/W1C	0x0	AUTO_CMD_ERR Auto CMD Error. This error status is used by Auto CMD12 and Auto CMD23 in SD/eMMC mode. This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared by clearing of this bit. Values: 1'b0: No Error 1'b0: Error
7	RO	0x0	reserved
6	RC/W1C	0x0	DATA_END_BIT_ERR Data End Bit Error. This error occurs in SD/eMMC mode either when detecting 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status. Values: 1'b0: No Error 1'b1: Error
5	RC/W1C	0x0	DATA_CRC_ERR Data CRC Error. This error occurs in SD/eMMC mode when detecting CRC error when transferring read data which uses the DAT line, when detecting the Write CRC status having a value of other than 010 or when write CRC status timeout. Values: 1'b0: No Error 1'b1: Error
4	RC/W1C	0x0	DATA_TOUT_ERR Data Timeout Error. This bit is set in SD/eMMC mode when detecting one of the following timeout conditions: a. Busy timeout for R1b, R5b type b. Busy timeout after Write CRC status c. Write CRC Status timeout d. Read Data timeout Values: 1'b0: No Error 1'b1: Time out
3	RC/W1C	0x0	CMD_IDX_ERR Command Index Error. This bit is set if a Command Index error occurs in the command response in SD/eMMC mode. Values: 1'b0: No Error 1'b1: Error
2	RC/W1C	0x0	CMD_END_BIT_ERR Command End Bit Error. This bit is set when detecting that the end bit of a command response is 0 in SD/eMMC mode. Values: 1'b0: No Error 1'b1: End Bit Error generated

Bit	Attr	Reset Value	Description
1	RC/W1C	0x0	CMD_CRC_ERR Command CRC Error. Command CRC Error is generated in SD/eMMC mode for following two cases. a. If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. b. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller aborts the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error is also set to 1 to distinguish a CMD line conflict. Values: 1'b0: No Error 1'b1: CRC Error generated
0	RC/W1C	0x0	CMD_TOUT_ERR Command Timeout Error. In SD/eMMC Mode, this bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to 1, without waiting for 64 SD/eMMC card clock cycles. Values: 1'b0: No Error 1'b1: Time out

EMMC_NORMAL_INT_STAT_EN
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_STAT_EN CQE Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
13:9	RO	0x00	reserved
8	RW	0x0	CARD_INTERRUPT_STAT_EN Card Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_STAT_EN Card Removal Status Enable. Values: 1'b0: Masked 1'b1: Enabled
6	RW	0x0	CARD_INSERTION_STAT_EN Card Insertion Status Enable. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
5	RW	0x0	BUF_RD_READY_STAT_EN Buffer Read Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_STAT_EN Buffer Write Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_STAT_EN DMA Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_STAT_EN Block Gap Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	XFER_COMPLETE_STAT_EN Transfer Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_STAT_EN Command Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_STAT_EN

Address: Operational Base + offset (0x0036)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_STAT_EN Boot Acknowledgment Error Status Enable.. Values: 1'b0: Masked 1'b1: Enabled
11	RW	0x0	RESP_ERR_STAT_EN Response Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_STAT_EN Tuning Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
9	RW	0x0	ADMA_ERR_STAT_EN ADMA Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
8	RW	0x0	AUTO_CMD_ERR_STAT_EN Auto CMD Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_STAT_EN Data End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_STAT_EN Data CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_STAT_EN Data Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	CMD_IDX_ERR_STAT_EN Command Index Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_STAT_EN Command End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	CMD_CRC_ERR_STAT_EN Command CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_TOUT_ERR_STAT_EN Command Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_NORMAL_INT_SIGNAL_EN

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_SIGNAL_EN CQE Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
13:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	CARD_INTERRUPT_SIGNAL_EN Card Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_SIGNAL_EN Card Removal Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
6	RW	0x0	CARD_INSERTION_SIGNAL_EN Card Insertion Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	BUF_RD_READY_SIGNAL_EN Buffer Read Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_SIGNAL_EN Buffer Write Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_SIGNAL_EN DMA Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_SIGNAL_EN Block Gap Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	XFER_COMPLETE_SIGNAL_EN Transfer Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_SIGNAL_EN Command Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_SIGNAL_EN

Address: Operational Base + offset (0x003A)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_SIGNAL_EN Boot Acknowledgment Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
11	RW	0x0	RESP_ERR_SIGNAL_EN Response Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_SIGNAL_EN Tuning Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
9	RW	0x0	ADMA_ERR_SIGNAL_EN ADMA Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
8	RW	0x0	AUTO_CMD_ERR_SIGNAL_EN Auto CMD Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_SIGNAL_EN Data End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_SIGNAL_EN Data CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_SIGNAL_EN Data Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	CMD_IDX_ERR_SIGNAL_EN Command Index Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_SIGNAL_EN Command End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	CMD_CRC_ERR_SIGNAL_EN Command CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	CMD_TOUT_ERR_SIGNAL_EN Command Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_AUTO_CMD_STAT

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RO	0x0	CMD_NOT_ISSUED_AUTO_CMD12 Command Not Issued By Auto CMD12 Error. If this bit is set to 1, CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: No Error 1'b1: Not Issued
6	RO	0x0	reserved
5	RO	0x0	AUTO_CMD_RESP_ERR Auto CMD Response Error. This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or CMD13. This status is ignored if any bit between D00 to D04 is set to 1. Values: 1'b0: No Error 1'b1: Error
4	RO	0x0	AUTO_CMD_IDX_ERR Auto CMD Index Error. This bit is set if the command index error occurs in response to a command. Values: 1'b0: No Error 1'b1: Error
3	RO	0x0	AUTO_CMD_EBIT_ERR Auto CMD End Bit Error. This bit is set when detecting that the end bit of command response is 0. Values: 1'b0: No Error 1'b1: End Bit Error Generated
2	RO	0x0	AUTO_CMD_CRC_ERR Auto CMD CRC Error. This bit is set when detecting a CRC error in the command response. Values: 1'b0: No Error 1'b1: CRC Error Generated

Bit	Attr	Reset Value	Description
1	RO	0x0	AUTO_CMD_TOUT_ERR Auto CMD Timeout Error. This bit is set if no response is returned with 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, error status bits (D04-D01) are meaningless. Values: 1'b0: No Error 1'b1: Time out
0	RO	0x0	AUTO_CMD12_NOT_EXEC Auto CMD12 Not Executed. If multiple memory block data transfer is not started due to a command error, this bit is not set because it is not necessary to issue an Auto CMD12. Setting this bit to 1 means that the Host Controller cannot issue Auto CMD12 to stop multiple memory block data transfer, due to some error. If this bit is set to 1, error status bits (D04-D01) is meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: Executed 1'b1: Not Executed

EMMC_HOST_CTRL2

Address: Operational Base + offset (0x003E)

Bit	Attr	Reset Value	Description
15	RW	0x0	PRESET_VAL_ENABLE Preset Value Enable. This bit enables automatic selection of SDCLK frequency and Driver strength Preset Value registers. When Preset Value Enable is set, SDCLK frequency generation (Frequency Select and Clock Generator Select) and the driver strength selection are performed by the controller. These values are selected from set of Preset Value registers based on selected speed mode. Values: 1'b0: SDCLK and Driver Strength are controlled by Host Driver 1'b1: Automatic Selection by Preset Value are Enabled
14	RW	0x0	ASYNC_INT_ENABLE Asynchronous Interrupt Enable. This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Values: 1'b0: Disabled 1'b1: Enabled
13	RW	0x0	ADDRESSING 64-bit Addressing. This bit is effective when Host Version 4 Enable is set to 1. Values: 1'b0: 32 bits addressing 1'b1: 64 bits addressing

Bit	Attr	Reset Value	Description
12	RW	0x0	HOST_VER4_ENABLE Host Version 4 Enable. This bit selects either Version 3.00 compatible mode or Version 4 mode. Values: 1'b0: Version 3.00 compatible mode 1'b1: Version 4 mode
11	RW	0x0	CMD23_ENABLE CMD23 Enable. If the card supports CMD23, this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. Values: 1'b0: Auto CMD23 is disabled 1'b1: Auto CMD23 is enabled
10	RW	0x0	ADMA2_LEN_MODE ADMA2 Length Mode. This bit selects ADMA2 Length mode to be either 16-bit or 26-bit. Values: 1'b0: 16-bit Data Length Mode 1'b1: 26-bit Data Length Mode
9	RO	0x0	reserved
8	RW	0x0	UHS2_IF_ENABLE This bit should be set to 0 for SD/eMMC Interface.
7	RW	0x0	SAMPLE_CLK_SEL Sampling Clock Select. This bit is used by the Host Controller to select the sampling clock in SD/eMMC mode to receive CMD and DAT. This bit is set by the tuning procedure and is valid after the completion of tuning (when Execute Tuning is cleared). Setting this bit to 1 means that tuning is completed successfully and setting this bit to 0 means that tuning has failed. Values: 1'b0: Fixed clock is used to sample data 1'b1: Tuned clock is used to sample data
6	RW	0x0	EXEC_TUNING Execute Tuning. This bit is set to 1 to start the tuning procedure in SD/eMMC speed modes and this bit is automatically cleared when tuning procedure is completed. Values: 1'b0: Not Tuned or Tuning completed 1'b1: Execute Tuning
5:4	RO	0x0	reserved
3	RW	0x0	SIGNALING_EN 1.8V Signalling Enable. Values: 1'b0: 3.3V Signalling 1'b1: 1.8V Signalling

Bit	Attr	Reset Value	Description
2:0	RW	0x0	UHS_MODE_SEL UHS Mode/eMMC Speed Mode Select. These bits are used to select UHS mode in the SD mode of operation. In eMMC mode, these bits are used to select eMMC Speed mode. Values: UHS Mode: 3'h0: SDR12 3'h1: SDR25 3'h2: SDR50 3'h3: SDR104 3'h4: DDR50 Others: Reserved eMMC Mode: 3'h0: Legacy 3'h1: High Speed SDR 3'h3: HS200 3'h4: High Speed DDR 3'h7: HS400 Others: Reserved

EMMC_CAPABILITIES1
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x1	SLOT_TYPE Slot Type. These bits indicate usage of a slot by a specific Host System. 2'h0: Removable Card Slot 2'h1: Embedded Slot for One Device 2'h2: Shared Bus Slot (SD mode) 2'h3: Reserved
29	RO	0x0	ASYNC_INT_SUPPORT Asynchronous Interrupt Support (SD Mode only). Values: 1'b0: Asynchronous Interrupt Not Supported 1'b1: Asynchronous Interrupt Supported
28	RO	0x0	SYS_ADDR_64_V3 64-bit System Address Support for V3. This bit sets the Host controller to support 64-bit System Addressing of V3 mode. SDMA cannot be used in 64-bit Addressing in Version 3 Mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL =11b). Values: 1'b0: 64-bit System Address for V3 is Not Supported 1'b1: 64-bit System Address for V3 is Supported

Bit	Attr	Reset Value	Description
27	RO	0x0	SYS_ADDR_64_V4 64-bit System Address Support for V4. This bit sets the Host Controller to support 64-bit System Addressing of V4 mode. When this bit is set to 1, full or part of 64-bit address must be used to decode the Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller registers is effective regardless of setting to 64-bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Addressing for version 4 is enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor. Values: 1'b0: 64-bit System Address for V4 is Not Supported 1'b1: 64-bit System Address for V4 is Supported
26:24	RO	0x0	reserved
23	RO	0x1	SUS_RES_SUPPORT Suspense/Resume Support. This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver does not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not supported. Values: 1'b0: Not Supported 1'b1: Supported
22	RO	0x1	SDMA_SUPPORT SDMA Support. This bit indicates whether the Host Controller is capable of using SDMA to transfer data between the system memory and the Host Controller directly. Values: 1'b0: SDMA not Supported 1'b1: SDMA Supported
21	RO	0x1	HIGH_SPEED_SUPPORT High Speed Support. This bit indicates whether the Host Controller and the Host System supports High Speed mode and they can supply the SD Clock frequency from 25 MHz to 50 MHz. Values: 1'b0: High Speed not Supported 1'b1: High Speed Supported
20	RO	0x0	reserved
19	RO	0x1	ADMA2_SUPPORT ADMA2 Support. This bit indicates whether the Host Controller is capable of using ADMA2. Values: 1'b0: ADMA2 not Supported 1'b1: ADMA2 Supported

Bit	Attr	Reset Value	Description
18	RO	0x1	EMBEDDED_8_BIT 8-bit Support for Embedded Device. This bit indicates whether the Host Controller is capable of using an 8-bit bus width mode. Values: 1'b0: 8-bit Bus Width not Supported 1'b1: 8-bit Bus Width Supported
17:16	RO	0x1	MAX_BLK_LEN Maximum Block Length. This bit indicates the maximum block size that the Host driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory irrespective of this bit. Values: 2'h0: 512 Byte 2'h1: 1024 Byte 2'h2: 2048 Byte 2'h3: Reserved
15:8	RO	0xc8	BASE_CLK_FREQ Base Clock Frequency for SD clock. These bits indicate the base (maximum) clock frequency for the SD Clock. The definition of these bits depends on the Host Controller Version. (1) 6-Bit Base Clock Frequency: This mode is supported by the Host Controller version 1.00 and 2.00. The upper 2 bits are not effective and are always 0. The unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h1: 2 MHz .... 8'h3f: 63 MHz Others: Reserved (2) 8-Bit Base Clock Frequency: This mode is supported by the Host Controller version 3.00. The unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h0: 2 MHz .... 8'hff: 255 MHz
7	RO	0x1	TOUT_CLK_UNIT Timeout Clock Unit. This bit shows the unit of base clock frequency used to detect Data Timeout Error. Values: 1'b0: KHz 1'b1: MHz
6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RO	0x00	TOUT_CLK_FREQ Timeout Clock Frequency. This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock unit defines the unit of timeout clock frequency. It can be KHz or MHz. 6'h0: Get information through another method 6'h1: 1KHz / 1MHz 6'h2: 2KHz / 2MHz 6'h3: 3KHz / 3MHz .... 6'h3f: 63KHz / 63MHz

EMMC_CAPABILITIES2

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	ADMA3_SUPPORT ADMA3 Support. This bit indicates whether the Host Controller is capable of using ADMA3. Values: 1'b0: ADMA3 not Supported 1'b1: ADMA3 Supported
24	RO	0x0	reserved
23:16	RO	0x0a	CLK_MUL Clock Multiplier. These bits indicate the clock multiplier of the programmable clock generator. Setting these bits to 0 means that the Host Controller does not support a programmable clock generator. Values: 8'h0: Clock Multiplier is not Supported 8'h1: Clock Multiplier M = 2 8'h2: Clock Multiplier M = 3 .... 8'hFF: Clock Multiplier M = 256
15:14	RO	0x0	RE_TUNING_MODES Re-Tuning Modes. Values: These bits select the re-tuning method and limit the maximum data length. Values: 2'h0: Timer 2'h1: Timer and Re-Tuning Request (Not supported) 2'h2: Auto Re-Tuning (for transfer) 2'h3: Reserved
13	RO	0x1	USE_TUNING_SDR50 Use Tuning for SDR50. Values: 1'b0: SDR50 does not require tuning 1'b1: SDR50 requires tuning
12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RO	0x0	RETUNE_CNT Timer Count for Re-Tuning. Values: 4'h0: Re-Tuning Timer disabled 4'h1: 1 seconds 4'h2: 2 seconds 4'h3: 4 seconds .... 4'hB: 1024 seconds 4'hC~4'hE: Reserved 4'hF: Get information from other source
7	RO	0x0	reserved
6	RO	0x1	DRV_TYPED This bit indicates support of Driver Type D for 1.8 Signaling. Values: 1'b0: Driver Type D is Not Supported 1'b1: Driver Type D is Supported
5	RO	0x1	DRV_TYPEC This bit indicates support of Driver Type C for 1.8 Signaling. Values: 1'b0: Driver Type C is Not Supported 1'b1: Driver Type C is Supported
4	RO	0x1	DRV_TYPEA This bit indicates support of Driver Type A for 1.8 Signaling. Values: 1'b0: Driver Type A is Not Supported 1'b1: Driver Type A is Supported
3	RO	0x0	UHS2_SUPPORT UHS-II Support. Values: 1'b0: UHS-II is Not Supported 1'b1: UHS-II is Supported
2	RO	0x1	DDR50_SUPPORT DDR50 Support. Values: 1'b0: DDR50 is Not Supported 1'b1: DDR50 is Supported
1	RO	0x1	SDR104_SUPPORT SDR104 Support. Values: 1'b0: SDR104 is Not Supported 1'b1: SDR104 is Supported
0	RO	0x1	SDR50_SUPPORT SDR50 Support. Values: 1'b0: SDR50 is Not Supported 1'b1: SDR50 is Supported

EMMC_FORCE_AUTO_CMD_STAT

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7	WO	0x0	FORCE_CMD_NOT_ISSUED_AUTO_CMD12 Force Event for Command Not Issued By Auto CMD12 Error. Values: 1'b0: Not Affected 1'b1: Command Not Issued By Auto CMD12 Error Status is set
6	RO	0x0	reserved
5	WO	0x0	FORCE_AUTO_CMD_RESP_ERR Force Event for Auto CMD Response Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Response Error Status is set
4	WO	0x0	FORCE_AUTO_CMD_IDX_ERR Force Event for Auto CMD Index Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Index Error Status is set
3	WO	0x0	FORCE_AUTO_CMD_EBIT_ERR Force Event for Auto CMD End Bit Error. Values: 1'b0: Not Affected 1'b1: Auto CMD End Bit Error Status is set
2	WO	0x0	FORCE_AUTO_CMD_CRC_ERR Force Event for Auto CMD CRC Error. Values: 1'b0: Not Affected 1'b1: Auto CMD CRC Error Status is set
1	WO	0x0	FORCE_AUTO_CMD12_TOUT_ERR Force Event for Auto CMD Timeout Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Timeout Error Status is set
0	WO	0x0	FORCE_AUTO_CMD12_NOT_EXEC Force Event for Auto CMD12 Not Executed. Values: 1'b0: Not Affected 1'b1: Auto CMD12 Not Executed Status is set

EMMC_FORC_ERR_INT_STAT

Address: Operational Base + offset (0x0052)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	WO	0x0	FORCE_BOOT_ACK_ERR Force Event for Boot Acknowledge error. Values: 1'b0: Not Affected 1'b1: Boot Acknowledge Error Status is set
11	WO	0x0	FORCE_RESP_ERR Force Event for Response Error. Values: 1'b0: Not Affected 1'b1: Response Error Status is set

Bit	Attr	Reset Value	Description
10	WO	0x0	FORCE_TUNING_ERR Force Event for Tuning Error Values: 1'b0: Not Affected 1'b1: Tuning Error Status is set
9	WO	0x0	FORCE_ADMA_ERR Force Event for ADMA Error. Values: 1'b0: Not Affected 1'b1: ADMA Error Status is set
8	WO	0x0	FORCE_AUTO_CMD_ERR Force Event for Auto CMD Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Error Status is set
7	RO	0x0	reserved
6	WO	0x0	FORCE_DATA_END_BIT_ERR Force Event for Data End Bit Error. Values: 1'b0: Not Affected 1'b1: Data End Bit Error Status is set
5	WO	0x0	FORCE_DATA_CRC_ERR Force Event for Data CRC Error. Values: 1'b0: Not Affected 1'b1: Data CRC Error Status is set
4	WO	0x0	FORCE_DATA_TOUT_ERR Force Event for Data Timeout Error. Values: 1'b0: Not Affected 1'b1: Data Timeout Error Status is set
3	WO	0x0	FORCE_CMD_IDX_ERR Force Event for Command Index Error. Values: 1'b0: Not Affected 1'b1: Command Index Error Status is set
2	WO	0x0	FORCE_CMD_END_BIT_ERR Force Event for Command End Bit Error. Values: 1'b0: Not Affected 1'b1: Command End Bit Error Status is set
1	WO	0x0	FORCE_CMD_CRC_ERR Force Event for Command CRC Error. Values: 1'b0: Not Affected 1'b1: Command CRC Error Status is set
0	WO	0x0	FORCE_CMD_TOUT_ERR Force Event for Command Timeout Error. Values: 1'b0: Not Affected 1'b1: Command Timeout Error Status is set

EMMC_ADMA_ERR_STAT
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved
2	RO	0x0	ADMA_LEN_ERR ADMA Length Mismatch Error States. This error occurs in the following instances: a. While the Block Count Enable is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length; b. When the total data length cannot be divided by the block length Values: 1'b0: No Error 1'b1: Error
1:0	RO	0x0	ADMA_ERR_STATES ADMA Error States. These bits indicate the state of ADMA when an error occurs during ADMA data transfer. Values: 2'h0: Stop DMA - SYS_ADR register points to a location next to the error descriptor 2'h1: Fetch Descriptor - SYS_ADR register points to the error descriptor 2'h2: Never set this state 2'h3: Transfer Data - SYS_ADR register points to a location next to the error descriptor

EMMC_ADMA_SA

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_SA ADMA System Address. These bits indicate the 32 bits of the ADMA system address. a. SDMA: If Host Version 4 Enable is set to 1, this register stores the system address of the data location b. ADMA2: This register stores the byte address of the executing command of the descriptor table c. ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched.

EMMC_PRESET_INIT

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DS

Address: Operational Base + offset (0x0062)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_HS

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR12

Address: Operational Base + offset (0x0066)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR25

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR50

Address: Operational Base + offset (0x006A)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR104

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DDR50

Address: Operational Base + offset (0x006E)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator

Bit	Attr	Reset Value	Description
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_ADMA_ID

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_ID ADMA Integrated Descriptor Address. These bits indicate the 32-bit of the ADMA Integrated Descriptor address. The start address of Integrated Descriptor is set to these register bits. The ADMA3 fetches one Descriptor Address and increments these bits to indicate the next Descriptor address.

EMMC_SLOT_INTR_STATUS

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RO	0x00	INTR_SLOT Interrupt signal for each Slot. Host Controller support single card slot. This register shall always return 0.

EMMC_HOST_CNTRL_VERS

Address: Operational Base + offset (0x00FE)

Bit	Attr	Reset Value	Description
15:8	RO	0x10	VENDOR_VERSION_NUM Vendor Version Number.
7:0	RO	0x05	SPEC_VERSION_NUM Specification Version Number. Values: 8'h0: SD Host Controller Specification Version 1.00 8'h1: SD Host Controller Specification Version 2.00 8'h2: SD Host Controller Specification Version 3.00 8'h3: SD Host Controller Specification Version 4.00 8'h4: SD Host Controller Specification Version 4.10 8'h5: SD Host Controller Specification Version 4.20 Others: Reserved

EMMC_CQVER

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x5	EMMC_VER_MAJOR eMMC Major Version Number (1st digit left of decimal point) in BCD format
7:4	RO	0x1	EMMC_VER_MINOR eMMC Minor Version Number(1st digit right of decimal point) in BCD format
3:0	RO	0x0	EMMC_VER_SUFFIX eMMC Version Suffix (2nd digit right of decimal point) in BCD format

EMMC_CQCAP

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	CRYPTO_SUPPORT Crypto Support. This bit indicates whether the Host Controller supports cryptographic operations. Values: 1'b0: Crypto not Supported 1'b1: Crypto Supported
27:16	RO	0x000	reserved
15:12	RO	0x0	ITCFMUL Internal Timer Clock Frequency Multiplier. This field indicates the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details. 4'h0: 1 KHz clock 4'h1: 10 KHz clock 4'h2: 100 KHz clock 4'h3: 1 MHz clock 4'h4: 10 MHz clock Others: Reserved
11:10	RO	0x0	reserved
9:0	RO	0x000	ITCFVAL Internal Timer Clock Frequency Value. This field scales the frequency of the timer clock provided by ITCFMUL. The Final clock frequency of actual timer clock is calculated as ITCFVAL* ITCFMUL.

EMMC_CQCFG

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	DCMD_EN Direct Command (DCMD) Enable. This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Values: 1'b0: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1'b1: Task descriptor in slot #31 is a DCMD Task Descriptor
11:9	RO	0x0	reserved
8	RW	0x0	TASK_DESC_SIZE This bit indicates the size of task descriptor used in host memory. This bit can only be configured when Command Queueing Enable bit is 0 (command queueing is disabled) Values: 1'b0: Task descriptor size is 64 bits 1'b1: Task descriptor size is 128 bits
7:2	RO	0x00	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	CR_GENERAL_EN Crypto General Enable. Enable/Disable bit for Crypto Engine. If cryptographic operations are not supported, this status bit is reserved. Values: 1'b0: Disable cryptographic operations for all transactions 1'b1: Enable cryptographic operations for transactions where TD.CE=1 or CRNQP.CE=1
0	RW	0x0	CQ_EN Command Queueing Enable. When CQE is disable, the software controls the eMMC bus using the registers between the addresses 0x000 to 0x1FF. Before the software writes to this bit, the software verifies that the eMMC host controller is in idle state and there are no ongoing commands or data transfers. When software wants to exit command queuing mode, it clears all previous tasks (if any) before setting this bit to 0. Values: 1'b0: Disable command queuing 1'b1: Enable command queuing

EMMC_CQCTRL

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	CLR_ALL_TASKS Clear all tasks. This bit can only be written when the controller is halted. This bit does not clear tasks in the device. The software has to use the CMDQ_TASK_MGMT command to clear device's queue. Values: 1'b0: Programming 0 has no effect 1'b1: Clears all the tasks in the controller
7:1	RO	0x00	reserved
0	RW	0x0	HALT Halt request and resume. Values: 1'b0: RESUME_CQE. Software writes 0 to this bit to exit from the halt state and resume CQE activity. 1'b1: HALT_CQE. Software writes 1 to this bit when it wants to acquire software control over the eMMC bus and to disable CQE from issuing command on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When the software writes 1, CQE completes the ongoing task (if any in progress). After the task is completed and the CQE is in idle state, CQE does not issue new commands and indicates to the software by setting this bit to 1. The software can poll on this bit until it is set to 1 and only then send commands on the eMMC bus.

EMMC_CQIS

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RC/W1C	0x0	TCL Task Cleared Interrupt. This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL). Values: 1'b0: TCL Interrupt is not set 1'b1: TCL Interrupt is set
2	RC/W1C	0x0	RED Response Error Detected Interrupt. This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked. Values: 1'b0: RED Interrupt is not set 1'b1: RED Interrupt is set
1	RC/W1C	0x0	TCC Task Complete Interrupt. This status bit is asserted(if CQISTE.TCC=1) when at least one of the following two conditions are met: a. A task is completed and the INT bit is set in its Task Descriptor b. Interrupt caused by Interrupt Coalescing logic Values: 1'b0: TCC Interrupt is not set 1'b1: TCC Interrupt is set
0	RC/W1C	0x0	HAC Halt Complete Interrupt. This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that Hhost Controller has completed its current ongoing task and has entered halt state. Values: 1'b0: HAC Interrupt is not set 1'b1: HAC Interrupt is set

EMMC_CQISE

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_STE Task Cleared Interrupt status enable. Values: 1'b0: CQIS.TCL is disabled 1'b1: CQIS.TCL is set when its interrupt condition is active
2	RW	0x0	RED_STE Response Error Detected Interrupt status enable. Values: 1'b0: CQIS.RED is disabled 1'b1: CQIS.RED is set when its interrupt condition is active

Bit	Attr	Reset Value	Description
1	RW	0x0	TCC_STE Task Complete Interrupt status enable. Values: 1'b0: CQIS.TCC is disabled 1'b1: CQIS.TCC is set when its interrupt condition is active
0	RW	0x0	HAC_STE Halt Complete Interrupt status enable. Values: 1'b0: CQIS.HAC is disabled 1'b1: CQIS.HAC is set when its interrupt condition is active

EMMC_CQISGE

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_SGE Task Cleared Interrupt signal enable. Values: 1'b0: CQIS.TCL interrupt signal generation is disabled 1'b1: CQIS.TCL interrupt signal generation is active
2	RW	0x0	RED_SGE Response Error Detected Interrupt signal enable. Values: 1'b0: CQIS.RED interrupt signal generation is disabled 1'b1: CQIS.RED interrupt signal generation is active
1	RW	0x0	TCC_SGE Task Complete Interrupt signal enable. Values: 1'b0: CQIS.TCC interrupt signal generation is disabled 1'b1: CQIS.TCC interrupt signal generation is active
0	RW	0x0	HAC_SGE Halt Complete Interrupt signal enable. Values: 1'b0: CQIS.HAC interrupt signal generation is disabled 1'b1: CQIS.HAC interrupt signal generation is active

EMMC_CQIC

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RW	0x0	INTC_EN Interrupt Coalescing Enable Bit. Values: 1'b0: Interrupt coalescing mechanism is disabled 1'b1: Interrupt coalescing mechanism is active. Interrupts are counted and timed, and coalesced interrupts are generated
30:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20	RO	0x0	INTC_STAT Interrupt Coalescing Status Bit. This bit indicates to the software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (that is, this is set if and only if INTC counter > 0). Values: 1'b0: INT0 Task completions have not occurred since last counter reset (INTC counter == 0) 1'b1: At least one INT0 task completion has been counted (INTC counter > 0)
19:17	RO	0x0	reserved
16	WO	0x0	INTC_RST Counter and Timer Reset. When host driver writes 1, the interrupt coalescing timer and counter are reset. Values: 1'b0: No Effect 1'b1: Interrupt coalescing timer and counter are reset
15	WO	0x0	INTC_TH_WEN Interrupt Coalescing Counter Threshold Write Enable. When software writes 1 to this bit, the value INTC_TH is updated with the contents written on the same cycle. Values: 1'b0: Clears INTC_TH_WEN 1'b1: Sets INTC_TH_WEN
14:13	RO	0x0	reserved
12:8	WO	0x00	INTC_TH Interrupt Coalescing Counter Threshold filed. Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor), which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in INTC_TH, and generates interrupt. 5'h0: Interrupt coalescing feature disabled 5'h1: Interrupt coalescing interrupt generated after 1 task when INT=0 completes 5'h2: Interrupt coalescing interrupt generated after 2 tasks when INT=0 completes .... 5'h1f: Interrupt coalescing interrupt generated after 31 tasks when INT=0 completes To write to this field, the INTC_TH_WEN bit must be set during the same write operation.
7	WO	0x0	TOUT_VAL_WEN When software writes 1 to this bit, the value TOUT_VAL is updated with the contents written on the same cycle. Values: 1'b0: clears TOUT_VAL_WEN 1'b1: Sets TOUT_VAL_WEN

Bit	Attr	Reset Value	Description
6:0	RW	0x00	TOUT_VAL Interrupt Coalescing Timeout Value. Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. 7'h0: Timer is disabled. Timeout-based interrupt is not generated 7'h1: Timeout on 01x1024 cycles of timer clock frequency 7'h2: Timeout on 02x1024 cycles of timer clock frequency .... 7'h7f: Timeout on 127x1024 cycles of timer clock frequency In order to write to this field, the TOUT_VAL_WEN bit must be set at the same write operation.

EMMC_CQTDLBA

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDLBA Task Descriptor List Base Address. This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KB boundary. The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.

EMMC_CQTDBR

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DBR Command Queueing Task Doorbell. Software shall configure TDLBA, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. Writing 0 by the software does not have any impact on the hardware, and does not change the value of the register bit. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: a. When a task execution is completed (with success or error) b. The task is cleared using CQTCLR register c. All tasks are cleared using CQCTL register d. CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission, CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order.

EMMC_CQTCN

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCN Task Complete Notification. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has completed execution (with success or errors) Bit-N(0): Task-N has not completed, could be pending or not submitted. On task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

EMMC_CQDQS

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DQS Device Queue Status. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Device has marked task N as ready for execution Bit-N(0): Task-N is not ready for execution. This task could be pending in device or not submitted. Host controller updates this register with response of the Device Queue Status command.

EMMC_CQDPT
Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DPT Device Pending Tasks. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has been successfully queued into the device and is awaiting execution. Bit-N(0): Task-N is not yet queued. Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task has not been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software reads this register in the task-discard procedure to determine if the task is queued in the device.

EMMC_CQTCLR
Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCLR Command Queueing Task Clear. Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once the clear operation is complete. Software must poll on the CQTCLR until it is cleared to verify that a clear operation was done.

EMMC_CQSSC1
Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x1	SQSCMD_BLK_CNT Send Status Command Block Counter. This field indicates when SQS CMD is sent while data transfer is in progress. A value of 'n' indicates that CQE sends status command on the CMD line, during the transfer of data block BLOCK_CNT-n, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. 4'h0: SEND_QUEUE_STATUS (CMD13) command is not sent during the transaction. Instead, it is sent only when the data lines are idle. 4'h1: SEND_QUEUE_STATUS command is to be sent during the last block of the transaction. 4'h2: SEND_QUEUE_STATUS command when last 2 blocks are pending. 4'h3: SEND_QUEUE_STATUS command when last 3 blocks are pending. .... 4'hf: SEND_QUEUE_STATUS command when last 15 blocks are pending. Should be programmed only when CQCFG.CQ_EN is '0'.
15:0	RW	0x1000	SQSCMD_IDLE_TMR Send Status Command Idle Timer. This field configures the polling period to be used when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicates that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0x0001 (1 clock period) and the maximum value is 0xFFFF (65535 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 0x1000, the calculated polling period is 4096*52.08 ns= 213.33 ns. Should be programmed only when CQCFG.CQ_EN is '0'.

EMMC_CQSSC2

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	SQSCMD_RCA Send Queue RCA. This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE copies this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

EMMC_CQCRDCT

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DCMD_RESP Direct Command Last Response. This register contains the response of the command generated by the last direct command (DCMD) task that was sent. Contents of this register are valid only after bit 31 of CQTDBR register is cleared by the controller.

EMMC_CQRMEM

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:0	RW	0xfdf9a080	RESP_ERR_MASK Response Mode Error Mask. The bits of this field are bit mapped to the device response. This bit is used as an interrupt mask on the device status filed that is received in R1/R1b responses. The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. 1'b0: When a R1/R1b response is received, bit i in the device status is ignored. 1'b1: When a R1/R1b response is received, with a bit i in the device status set, a RED interrupt is generated. Note: Responses to CMD13 (SQS) encode the QSR so that they are ignored by this logic.

EMMC_CQTERRI

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	TRANS_ERR_FIELDS_VALID Data Transfer Error Field Valid. This bit is updated when an error is detected while a data transfer transaction was in progress. Values: 1'b0: Ignore contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX 1'b1: Data transfer related error detected. Check contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX fields
30:29	RO	0x0	reserved
28:24	RO	0x00	TRANS_ERR_TASKID Data Transfer Error Task ID. This field captures the ID of the task that was executed and whose data transfer has errors.
23:22	RO	0x0	reserved
21:16	RO	0x00	TRANS_ERR_CMD_INDX Data Transfer Error Command Index. This field captures the index of the command that was executed and whose data transfer has errors.
15	RO	0x0	RESP_ERR_FIELDS_VALID Response Mode Error Fields Valid. This bit is updated when an error is detected while a command transaction was in progress. Values: 1'b0: Ignore contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX 1'b1: Response-related error is detected. Check contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX fields

Bit	Attr	Reset Value	Description
14:13	RO	0x0	reserved
12:8	RO	0x00	RESP_ERR_TASKID Response Mode Error Task ID. This field captures the ID of the task which was executed on the command line when the error occurred.
7:6	RO	0x0	reserved
5:0	RO	0x00	RESP_ERR_CMD_INDX Response Mode Error Command Index. This field captures the index of the command that was executed on the command line when the error occurred.

EMMC_CQCRI
Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	CMD_RESP_INDX Last Command Response Index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

EMMC_CQCRA
Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CMD_RESP_ARG Last Command Response Argument. This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

EMMC_VER_ID
Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_ID Current version number.

EMMC_VER_TYPE
Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_TYPE Version type.

EMMC_HOST_CTRL3
Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	SW_CG_DIS Internal clock gating disable control. This bit must be used to disable IP's internal clock gating when required. When disabled clocks are not gated. Clocks to the core (except AHB bus clock) must be stopped when programming this bit. Values: 1'b0: Internal clock gating is disabled, clocks are not gated internally 1'b1: Internal clock gates are active and clock gating is controlled internally
3:1	RO	0x0	reserved
0	RW	0x0	CMD_CONFLICT_CHECK Command conflict check. This bit enables command conflict check. Host Controller monitors the CMD line whenever a command is issued and checks whether the value driven on command output line matches the value on command input line at next subsequent edge of transmit clock to determine command conflict error. This bit is cleared only if the feed back delay (including IO Pad delay) is more than (card clock period - flop setup time). Values: 1'b0: Disable command conflict check 1'b1: Check for command conflict after 1 card clock cycle

EMMC_EMMC_CTRL

Address: Operational Base + offset (0x052C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RW	0x0	CQE_PREFETCH_DISABLE Enable or Disable CQE's PREFETCH feature. This field allows Software to disable CQE's data prefetch feature when set to 1. Values: 1'b0: CQE can prefetch data for successive WRITE transfers and pipeline successive READ transfers 1'b1: Prefetch for WRITE and Pipeline for READ are disabled
9	RW	0x0	CQE_ALGO_SEL Scheduler algorithm selected for execution. This bit selects the Algorithm used for selecting one of the many ready tasks for execution. Values: 1'b0: Priority based reordering with FCFS to resolve equal priority tasks 1'b1: First come First serve, in the order of DBR rings
8	RW	0x0	ENH_STROBE_ENABLE Enhanced Strobe Enable. This bit instructs Host to sample the CMD line using data strobe for HS400 mode. Values: 1'b0: CMD line is sampled using receive clock for HS400 mode 1'b1: CMD line is sampled using data strobe for HS400 mode
7:3	RO	0x00	reserved

Bit	Attr	Reset Value	Description
2	RW	0x1	EMMC_RST_N EMMC Device Reset signal control. Values: 1'b0: Reset to eMMC device asserted 1'b1: Reset to eMMC device is de-asserted
1	RW	0x0	DISABLE_DATA_CRC_CHK Disable Data CRC Check. This bit controls masking of CRC16 error for Card Write in eMMC mode. This is useful in bus testing (CMD19) for an eMMC device. In bus testing, an eMMC card does not send CRC status for a block, which may generate CRC error. This CRC error can be masked using this bit during bus testing. Values: 1'b0: DATA CRC check is enabled 1'b1: DATA CRC check is disabled
0	RW	0x0	CARD_IS_EMMC eMMC Card present. This bit indicates the type of card connected. An application program this bit based on the card connected to Host Controller. Values: 1'b0: Card connected to Host Controller is a non-eMMC card 1'b1: Card connected to Host Controller is an eMMC card

EMMC_BOOT_CTRL

Address: Operational Base + offset (0x052E)

Bit	Attr	Reset Value	Description
15:12	RW	0x0	BOOT_TOUT_CNT Boot Acknowledge Timeout Counter Value. This value determines the interval by which boot acknowledge timeout (50 ms) is detected when boot acknowledge is expected during boot operation. Values: 4'h0: TMCLK x 2^13 4'h1: TMCLK x 2^14 ...... 4'hE: TMCLK x 2^27 4'hF: Reserved
11:9	RO	0x0	reserved
8	RW	0x0	BOOT_ACK_ENABLE Boot Acknowledge Enable. When this bit set, Host checks for boot acknowledge start pattern of 0-1-0 during boot operation. This bit is applicable for both mandatory and alternate boot mode. Values: 1'b1: Boot Acknowledge enable 1'b0: Boot Acknowledge disable
7	RW	0x0	VALIDATE_BOOT Validate Mandatory Boot Enable bit. This bit is used to validate the MAN_BOOT_EN bit. Values: 1'b1: Validate Mandatory boot enable bit 1'b0: Ignore Mandatory boot Enable bit
6:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	MAN_BOOT_EN Mandatory Boot Enable. This bit is used to initiate the mandatory boot operation. The application sets this bit along with VALIDATE_BOOT bit. Writing 0 is ignored. The Host Controller clears this bit after the boot transfer is completed or terminated. Values: 1'b1: Mandatory boot enable 1'b0: Mandatory boot disable

EMMC_AT_CTRL

Address: Operational Base + offset (0x0540)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:19	RW	0x0	POST_CHANGE_DLY Time taken for phase switching and stable clock output. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
18:17	RW	0x0	PRE_CHANGE_DLY Maximum Latency specification between transmit clock and receive clock. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
16	RW	0x0	TUNE_CLK_STOP_EN Clock stopping control for Tuning and auto-tuning circuit. When enabled, clock gate control output is pulled low before changing phase select codes. This effectively stops the receive clock. Changing phase code when clocks are stopped ensures glitch free phase switching. Values: 1'b0: Clocks not stopped 1'b1: Clocks stopped during phase code change
15:5	RO	0x000	reserved
4	RW	0x0	SW_TUNE_EN This fields enables software-managed tuning flow. Values: 1'b0: Software-managed tuning disabled 1'b1: Software-managed tuning enabled
3	RW	0x0	RPT_TUNE_ERR Framing errors are not generated when executing tuning. This debug bit allows users to report these errors. Values: 1'b0: Default mode where per host no errors are reported 1'b1: Debug mode for reporting framing errors

Bit	Attr	Reset Value	Description
2	RW	0x0	SWIN_TH_EN Sampling window Threshold enable. Selects the tuning mode. Field should be programmed only when SAMPLE_CLK_SEL is '0'. Values: 1'b0: Tuning engine sweeps all taps and settles at the largest window. 1'b1: Tuning engine selects the first complete sampling window that meets the threshold set by SWIN_TH_VAL field.
1:0	RO	0x0	reserved

EMMC_AT_STAT
Address: Operational Base + offset (0x0544)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	L_EDGE_PH_CODE Left Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Left edge of sampling window.
15:8	RO	0x00	R_EDGE_PH_CODE Right Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Right edge of sampling window.
7:0	RW	0x00	CENTER_PH_CODE Centered Phase code. Setting AT_CTRL.SW_TUNE_EN enables software to write to this field.

EMMC_DLL_CTRL
Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	DLL_BYPASS_MODE DLL bypass mode select. 1'b0: Normal 1'b1: Bypass
23:16	RW	0x00	DLL_START_POINT DLL start point for phase detect.
15:8	RW	0x00	DLL_INCRMENT DLL increment value.
7:2	RO	0x00	reserved
1	RW	0x0	DLL_SRST DLL software reset indication. 1'b0: Normal work 1'b1: Reset
0	RW	0x0	DLL_START DLL working indication. 1'b0: DLL is not working 1'b1: DLL is working

EMMC_DLL_RXCLK
Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31	RW	0x0	RX_CLK_ORI_GATE Receive original clock source gating enable. 1'b0: Receive original clock source is not auto gating, active when card clock is stable and enable. 1'b1: Receive original clock source is auto gating, active when card is working.
30	RO	0x0	reserved
29	RW	0x0	RX_CLK_SRC_SEL Receive clock source selection. 1'b0: Receive clock source is transmit clock output 1'b1: Receive clock source is original clock input
28	RW	0x0	RX_CLK_CHGWIN Receive clock change window configuration. When high, receive clock is gated.
27	RW	0x0	RX_CLK_DLY_ENA Delay enable for receive clock output. 1'b0: Disable delay. Receive clock output comes from receive clock source, determined by RX_CLK_SRC_SEL. 1'b1: Enable delay. Receive clock output comes from delay line output of receive clock source.
26	RW	0x0	RX_DELAY_NUM_SEL Delay element number selection for receive clock. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (RX_DELAY_NUM)
25	RW	0x0	RX_TAP_VALUE_SEL Tap value selection for receive clock. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (RX_TAP_VALUE)
24	RW	0x0	RX_TAP_NUM_SEL Tap number selection for receive clock. 1'b0: Tap number comes from tuning result 1'b1: Tap number comes from software (RX_TAP_NUM)
23:16	RW	0x00	RX_DELAY_NUM Total delay element number of selected tap used for receive clock.
15:8	RW	0x00	RX_TAP_VALUE Tap value for receive clock. It denotes delay element number for receive clock cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	RX_TAP_NUM Tap number for receive clock. Every clock is divided into 32 taps equably. The selected tap number is RX_TAP_NUM+1. Use tap number to select tap used for receive clock.

EMMC_DLL_TXCLK

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	TX_CLK_SRC_SEL Transmit clock source selection. 1'b0: Transmit clock source is invertion of original clock input 1'b1: Transmit clock source is original clock input

Bit	Attr	Reset Value	Description
28	RO	0x0	reserved
27	RW	0x0	TX_CLK_DLY_ENA Delay enable for transmit clock output. 1'b0: Disable delay. Transmit clock output comes from transmit clock source, determined by TX_CLK_SRC_SEL. 1'b1: Enable delay. Transmit clock output comes from delay line output of transmit clock source.
26	RW	0x0	TX_DELAY_NUM_SEL Delay element number selection for transmit clock. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (TX_DELAY_NUM)
25	RW	0x0	TX_TAP_VALUE_SEL Tap value selection for transmit clock. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (TX_TAP_VALUE)
24	RW	0x0	TX_TAP_NUM_SEL Tap number selection for transmit clock. 1'b0: Tap number is 8 1'b1: Tap number comes from software (TX_TAP_NUM)
23:16	RW	0x00	TX_DELAY_NUM Total delay element number of selected tap used for transmit clock.
15:8	RW	0x00	TX_TAP_VALUE Tap value for transmit clock. It denotes delay element number for transmit clock cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	TX_TAP_NUM Tap number for transmit clock. Every clock is divided into 32 taps equably. The selected tap number is TX_TAP_NUM+1. Use tap number to select tap used for transmit clock.

EMMC_DLL_STRBIN

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	STRBIN_DELAY_ENA Delay enable for strobe input. 1'b0: Disable delay. Strobe input comes from original data strobe. 1'b1: Enable delay. Strobe input comes from delay line output of original data strobe.
26	RW	0x0	STRBIN_DELAY_NUM_SEL Delay element number selection for strobe input. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (STRBIN_DELAY_NUM)
25	RW	0x0	STRBIN_TAP_VALUE_SEL Tap value selection for strobe input. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (STRBIN_TAP_VALUE)
24	RW	0x0	STRBIN_TAP_NUM_SEL Tap number selection for strobe input. 1'b0: Tap number is 8 1'b1: Tap number comes from software (TAPNUM_TAP_NUM)

Bit	Attr	Reset Value	Description
23:16	RW	0x00	STRBIN_DELAY_NUM Total delay element number of selected tap used for strobe input.
15:8	RW	0x00	STRBIN_TAP_VALUE Tap value for strobe input. It denotes delay element number for strobe input cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	STRBIN_TAP_NUM Tap number for strobe input. Every clock is divided into 32 taps equably. The selected tap number is STRBIN_TAP_NUM+1. Use tap number to select tap used for strobe input.

EMMC_DLL_CMDOUT

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x0	CMDOEN_SRC_SEL Command output enable selection. 2'b00: Command output enable is from register output triggered by clock rising edge 2'b01: Command output enable is from register output triggered by clock falling edge Others: Command output enable is from both register output triggered by clock rising edge and register output triggered by clock falling edge
28	RW	0x0	CMDOUT_SRC_SEL Command output source selection. 1'b0: Command output source is from register output triggered by clock rising edge 1'b1: Command output source is from register output triggered by clock falling edge
27	RW	0x0	CMDOUT_DELAY_ENA Delay enable for command output. 1'b0: Disable delay. Command output comes from command output source, determined by CMDOUT_SRC_SEL. 1'b1: Enable delay. Command output comes from delay line output of command output source.
26	RW	0x0	CMDOUT_DELAY_NUM_SEL Delay element number selection for command output. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (CMDOUT_DELAY_NUM)
25	RW	0x0	CMDOUT_TAP_VALUE_SEL Tap value selection for command output. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (CMDOUT_TAP_VALUE)
24	RW	0x0	CMDOUT_TAP_NUM_SEL Tap number selection for command output. 1'b0: Tap number is 0 1'b1: Tap number comes from software (CMDOUT_TAP_NUM)
23:16	RW	0x00	CMDOUT_DELAY_NUM Total delay element number of selected tap used for command output.

Bit	Attr	Reset Value	Description
15:8	RW	0x00	CMDOUT_TAP_VALUE Tap value for command output. It denotes delay element number for command output.
7:5	RO	0x0	reserved
4:0	RW	0x00	CMDOUT_TAP_NUM Tap number for command output. Every clock is divided into 32 taps equably. The selected tap number is CMDOUT_TAP_NUM+1. Use tap number to select tap used for command output.

EMMC_DLL_STATUS0
Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	DLL_CMDOUT_DELAY_VALUE Delay element number used for command output
15:10	RO	0x00	reserved
9	RO	0x0	DLL_LOCK_TIMEOUT Delay line phase detection timeout status. 1'b0: Not timeout 1'b1: Timeout
8	RO	0x0	DLL_LOCK Delay line lock indication. 1'b0: Delay line is not locked 1'b1: Delay line is locked
7:0	RO	0x00	DLL_LOCK_VALUE Delay line lock value for half card clock cycle. It denotes the delay element number needed for delay line locked. It is valid when DLL_LOCK is high.

EMMC_DLL_STATUS1
Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	DLL_STRBIN_DELAY_VALUE Delay element number used for strobe input
15:8	RO	0x00	DLL_RXCLK_DELAY_VALUE Delay element number used for receive clock
7:0	RO	0x00	DLL_TXCLK_DELAY_VALUE Delay element number used for transmit clock

4.5 Interface Description

4.5.1 EMMC Interface Description

Table 4-1 EMMC Interface Description

Module Pin	Direction	PAD Name	IOMUX Setting
emmc_cclk	O	EMMC_CLKOUT/GPIO2_A1_d	EMMC_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'h1
emmc_ccmd	I/O	EMMC_CMD/FSPI_CLK_M0/GPIO2_A0_u	EMMC_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h1
emmc_cdata0	I/O	EMMC_D0/FSPI_D0_M0/GPIO2_D0_u	EMMC_IOC_GPIO2D_IOMUX_SEL_L[3:0]=4'h1
emmc_cdata1	I/O	EMMC_D1/FSPI_D1_M0/GPIO2_D1_u	EMMC_IOC_GPIO2D_IOMUX_SEL_L[7:4]=4'h1
emmc_cdata2	I/O	EMMC_D2/FSPI_D2_M0/GPIO2_D2_u	EMMC_IOC_GPIO2D_IOMUX_SEL_L[11:8]=4'h1
emmc_cdata3	I/O	EMMC_D3/FSPI_D3_M0/GPIO2	EMMC_IOC_GPIO2D_IOMUX_SEL_L[

Module Pin	Direction	PAD Name	IOMUX Setting
		_D3_u	15:12]=4’h1
emmc_cdata4	I/O	EMMC_D4/I2C1_SCL_M3/UART5_RX_M2/GPIO2_D4_u	EMMC_IOC_GPIO2D_IOMUX_SEL_H[3:0]=4’h1
emmc_cdata5	I/O	EMMC_D5/I2C1_SDA_M3/UART5_TX_M2/GPIO2_D5_u	EMMC_IOC_GPIO2D_IOMUX_SEL_H[7:4]=4’h1
emmc_cdata6	I/O	EMMC_D6/FSPI_CS0N_M0/GPIO2_D6_u	EMMC_IOC_GPIO2D_IOMUX_SEL_H[11:8]=4’h1
emmc_cdata7	I/O	EMMC_D7/FSPI_CS1N_M0/GPIO2_D7_u	EMMC_IOC_GPIO2D_IOMUX_SEL_H[15:12]=4’h1
emmc_strbin	I	EMMC_DATA_STROBE/I2C2_SDA_M2/UART5_CTSN_M1/GPIO2_A2_d	EMMC_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4’h1
emmc_rstn	O	EMMC_RSTN/I2C2_SCL_M2/UART5_RTSN_M1/GPIO2_A3_d	EMMC_IOC_GPIO2A_IOMUX_SEL_L[15:12]=4’h1

Notes: I=input, O=output, I/O=input/output, bidirectional

4.6 Application Notes

4.6.1 Clock Adjustment

Phase detection is needed if you want to know the card clock’s precision before clock adjustment. The detection flow is as below:

(1) Set EMMC_DLL_CTRL[1]=1 to reset the EMMC DLL; then set EMMC_DLL_CTRL[1]=0 to dis-reset EMMC DLL;
(2) Set DLL_START_POINT in EMMC_DLL_CTRL[23:16]; set DLL_INCREMENT in EMMC_DLL_CTRL[15:8], and set EMMC_DLL_CTRL[0] to start the DLL phase detection.
(3) Wait for DLL lock until EMMC_DLL_STATUS0[8] equals to 1. Get the EMMC_DLL_STATUS0[7:0] as the locked value for the half card clock cycle time.
(4) If EMMC_DLL_STATUS0[9]=1 and EMMC_DLL_STATUS0[8]=0, the detection is timeout, you can adjust the DLL_START_POINT or DLL_INCREMENT to re-detection.; or bypass the detection if the total delay line length is short than half clock cycle. You need to set EMMC_DLL_CTRL[0] to 0 before you restart phase detection as(1)~(3).

After phase detection, the clock’s precision is shown in EMMC_DLL_STATUS0[7:0] (DLL_LOCK_VALUE) based on delay element.

We can calculate the delay element numbers requirement for transmit clock (TXCLK), receive clock (RXCLK), data strobe input (STRBIN), command output (CMDOUT), denoted as “XX” as follows:

(1) Get tap value: if XX_TAP_VALUE_SEL=0, tap value equals to (DLL_LOCK_VALUE*2)%256; else tap value is set by software, XX_TAP_VALUE;
(2) Get tap number: if XX_TAP_NUM_SEL=0, tap number comes from Host Controller; else tap number is set by software, XX_TAP_NUM;
(3) Get required delay element numbers: if XX_DELAY_NUM_SEL=0, delay element number equals to tap value* tap number; else delay element number is set by software, XX_DELAY_NUM.

The adjustment value for every cycle (XX) is equals to required delay element numbers*delay time of every element.

The delay time of every element is in the range of 36ps~68ps, varying with different voltage and temperature.

Chapter 5 Raster Graphic Acceleration 3 (RGA3)

5.1 Overview

RGA3 is a separate 2D graphics accelerator, used to accelerate basic operations, including: image position transformation (rotation, mirroring), size transformation (scale down, scale up), format conversion, FBC encoding and decoding, TILE encoding and decoding, and window overlap.

5.2 Feature

5.2.1 Image input mode and data format

- Raster mode
  - ARGB8888/RGB888/RGB565
  - YUV420(8bit & 10bit)/YUV422(8bit &10bit)/YUYV(8bit)
  - YUV support semi-planer
  - YUV10bit support compacted/uncompacted, little/big endian
- FBCD mode
  - ARGB8888/RGB888/RGB565
  - YUV420(8bit & 10bit)/YUV422(8bit & 10bit)
- Tile8x8 mode
  - YUV420(8bit & 10bit)/YUV422(8bit & 10bit)
  - YUV 10bit support compacted

5.2.2 Image output mode and data format

- Raster mode
  - ARGB8888/RGB888/RGB565
  - YUV420(8bit &10bit)/YUV422(8bit &10bit)/YUYV(8bit)
  - YUV support semi-planer
  - YUV10bit support compacted/uncompacted, little/big endian
- FBCE mode
  - ARGB8888/RGB888/RGB565
  - YUV420(8&10bit)/YUV422(8bit &10bit)
  - FBCE payload support sparse/unsparse mode
- Tile8x8 mode
  - YUV420(8bit &10bit)/YUV422(8bit &10bit)
  - YUV support semi-planer
  - YUV10bit support compacted/uncompacted, little/big endian

5.2.3 Support 9 path

- RASTER -> RASTER
- RASTER -> FBCE
- RASTER -> TILE
- FBCD -> RASTER
- FBCD -> FBCE
- FBCD -> TILE
- TILE -> RASTER
- TILE -> FBCE
- TILE -> TILE

5.2.4 Support 2 layers and CSC

- Y2R: BT601L, BT601R, BT709,BT2020
- R2Y: BT601L, BT601R, BT709, BT2020
- RB swap, UV swap, YC swap(YUV422)

5.2.5 Input/Output resolution

- Min input/output resolution is 128x128
- Max input resolution is (8192-16) x (8192-16)
- Max output resolution is (8192-64) x (8192-64)

- Max virtual width is 8192 word

5.2.6 Resize

- Scale down: Average, max ratio is 8
- Scale up: Bicubic, max ratio is 8

5.2.7 Orient

- Normal
- Ymirror
- Xmirror
- Rot180(xmirror+ymirror)
- Rot90
- Rot90+ymirror(xmirror+rot90)
- Rot90+xmirror(xmirror+rot270)
- Rot270

5.2.8 Overlap

- 2 overlap mode: ABB and ABC
- Support YUV field and RGB field

5.2.9 Config

- Support 32bit AHB configuration setting
- support AXI command configuration setting

5.2.10 Others

- Support level interrupt
- Support 128bit AXI
- Support 128bit MMU, max mapping to 32G DDR
- 4pixel/cycle when resize is bypass, 2pixel/cycle when resize is scale up/ scale down

5.3 Block Diagram

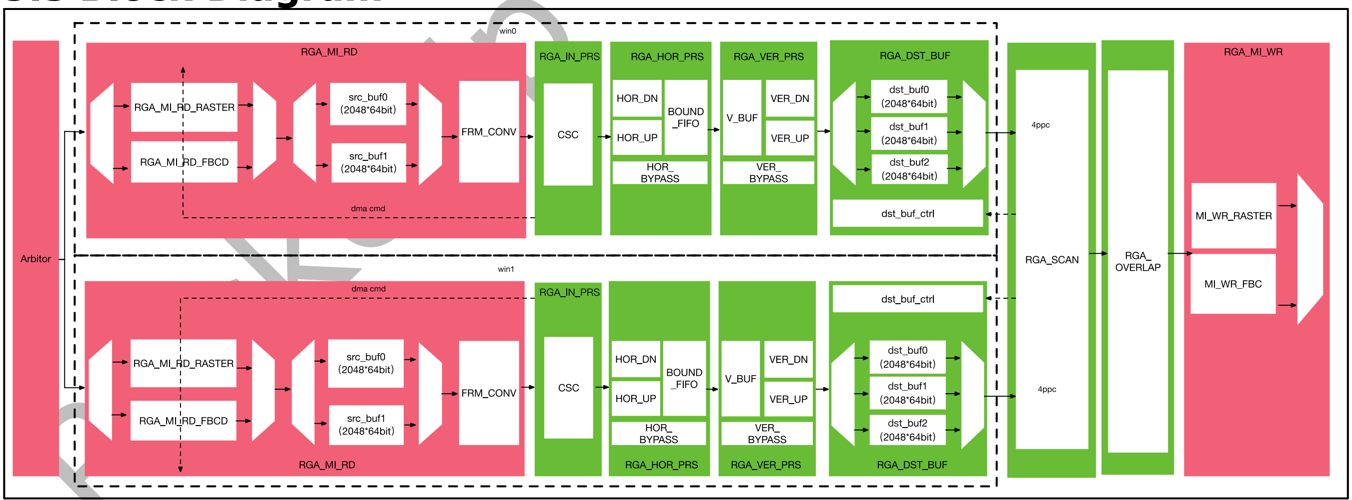


Fig. 5-1 RGA3 Block Diagram

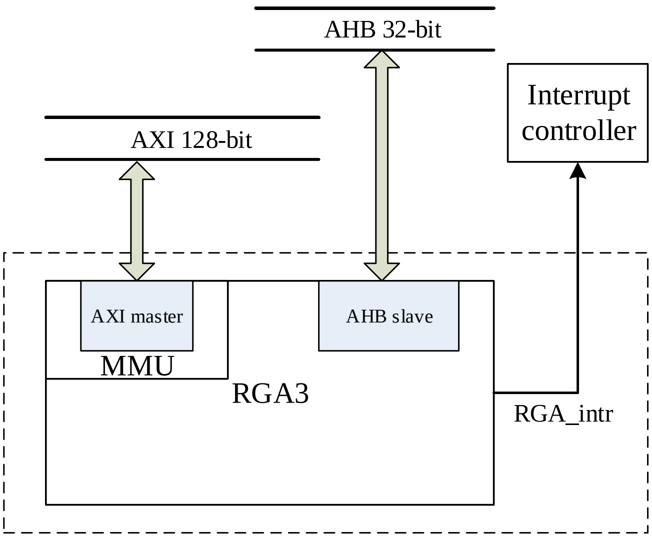


Fig. 5-2 RGA3 in SOC

5.4 Function Description

5.4.1 RGA3 Size

RGA3 common size relationship show as below:

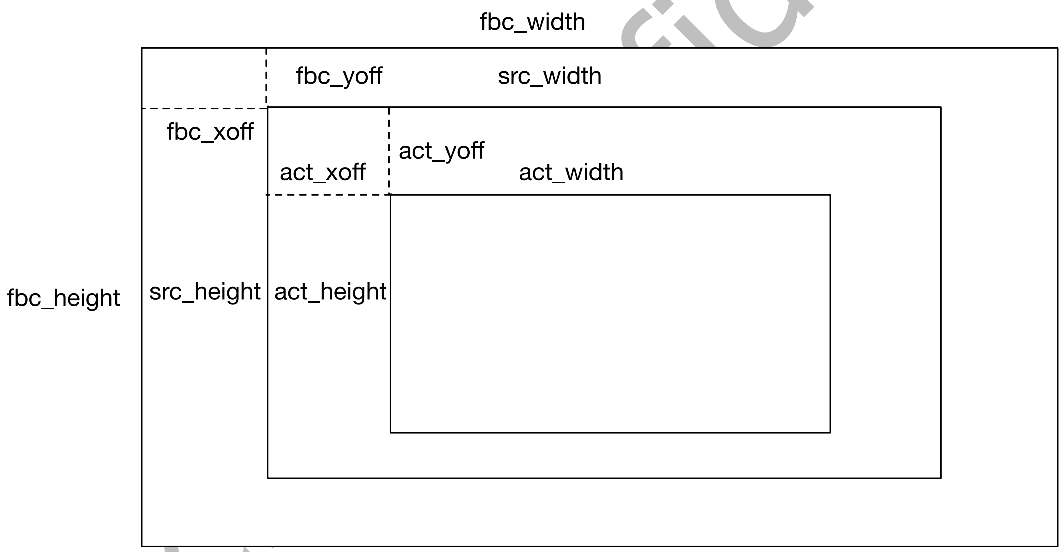


Fig. 5-3 RGA3 Size

5.4.2 Raster mode

- **RGA3 support Raster mode for input and output, which is stored in DDR as below:**

  1) rd_format/wr_format = 1 semi-planer format

YUV semi-planer format, we need two buffers in DDR(Y buffer, C buffer):

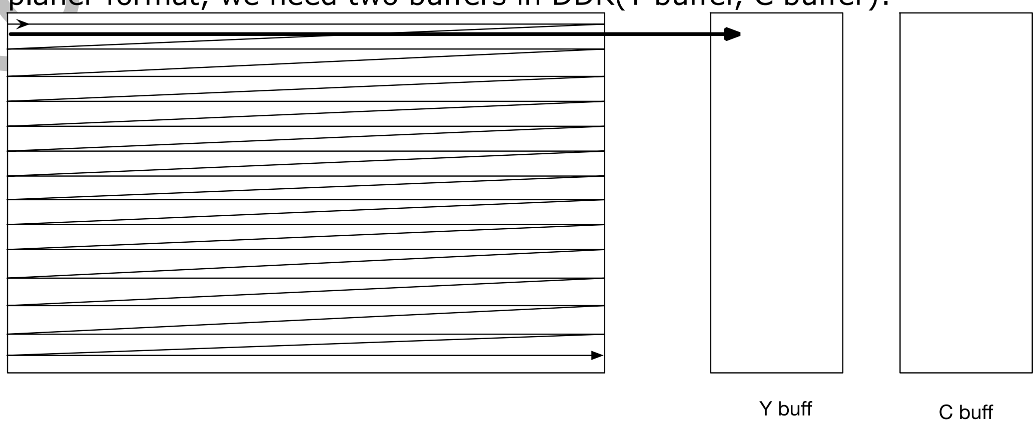


Fig. 5-4 Raster semi-planer buffer in DDR

According to different format, data will be stored in different ways as below:

YUV422sp

31 24 16 8 0

Y03	Y02	Y01	Y00
Y13	Y12	Y11	Y10

V02	U02	V00	U00
V22	U22	V10	U10

YUV420sp

31 24 16 8 0

Y03	Y02	Y01	Y00
Y13	Y12	Y11	Y10

V02	U02	V00	U00

YUV422sp 10bit uncompact

31 26 16 10 0

Y03	Y02	Y01	Y00
Y13	Y12	Y11	Y10

V02	U02	V00	U00
V12	U12	V10	U10

YUV420sp 10bit uncompact

31 26 16 10 0

Y03	Y02	Y01	Y00
Y13	Y12	Y11	Y10

V02	U02	V00	U00

YUV422sp 10bit compact

39 30 20 10 0

Y03	Y02	Y01	Y00
Y13	Y12	Y11	Y10

V02	U02	V00	U00
V12	U12	V10	U10

YUV420sp 10bit compact

39 30 20 10 0

Y03	Y02	Y01	Y00
Y13	Y12	Y11	Y10

V02	U02	V00	U00

Fig. 5-5 Different format in DDR

2) rd_format/wr_format = 2 interleave format
RGB or YVYU format, we need only one buffer in DDR:

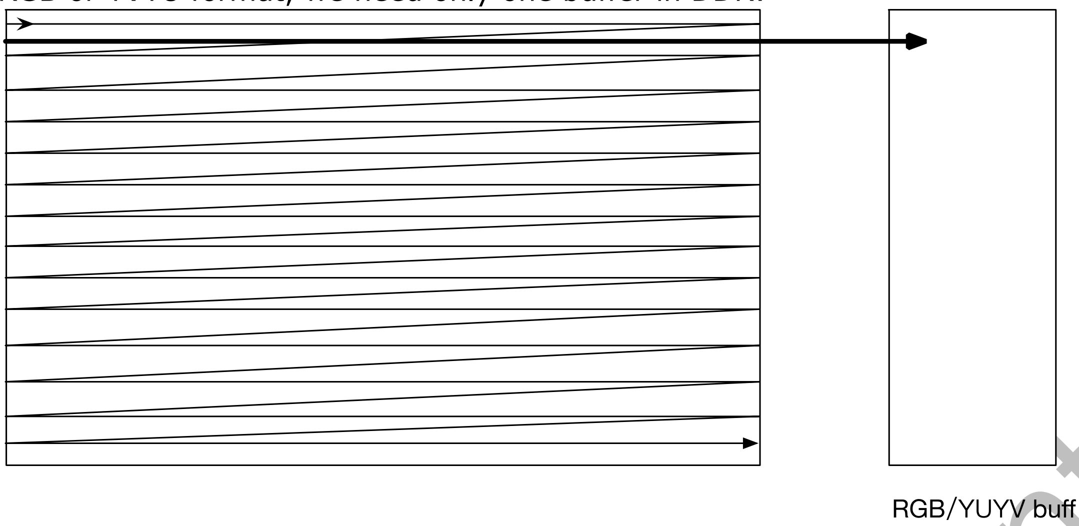


Fig. 5-6 Raster interleave buffer in DDR

According to different format, data will be stored in different ways as below:

RGB565

15	11	5	0
R	G	B	

RGB888packed

31	24	16	8	0
B1	R0	G0	B0	
G2	B2	R1	G1	
R3	G3	B3	R2	

ARGB8888

31	24	16	8	0
A	R	G	B	

ABGR8888

31	24	16	8	0
A	B	G	R	

RGBA8888

31	24	16	8	0
R	G	B	A	

BGRA8888

31	24	16	8	0
B	G	R	A	

YVYU（YUV422I)

31	24	16	8	0
Y00	V00	Y01	U00	
Y10	V10	Y11	U10	

Fig. 5-7 Different format in DDR

5.4.3 FBCD mode

This compression format is designed to be used for textures and frame buffers. It has been optimized to decrease external bandwidth as well as being random access and decodable at line speed for the texture cache.

Random access is available to individual 16x16 blocks, which in turn index individual 4x4 blocks. This is done using a structure where a header block is stored for each 16x16 block at a predictable memory address in what is referred to as the header buffer. If the horizontal size is given by "width" and A is the start address of the head buff, the address of the header for the 16x16 block containing a given pixel at position x, y is given by A+16*(x/16+((y/16)*(width/16))). A consequence of the 16x16 block structure is that only multiples of 16 are allowed as width and height as shown below.

The data that is used to store the individual 4x4 blocks in a 16x16 block is referred to as the payload data for that block. It is stored continuously in body buff from the offset that is supplied in the header. Each section in the body buffer contains payload data which is used to decode a 16x16 block. The header contains an offset to the payload that resides inside of the body buffer, which is typically allocated after allocated after the header buffer in the memory. The offset to the payload data is relative to the start of the header buffer. In some cases it may sense to store payload data inside the header buffer, such as when encoding blocks that are less than 16x16 in size and not all sub block sizes are used in a header.

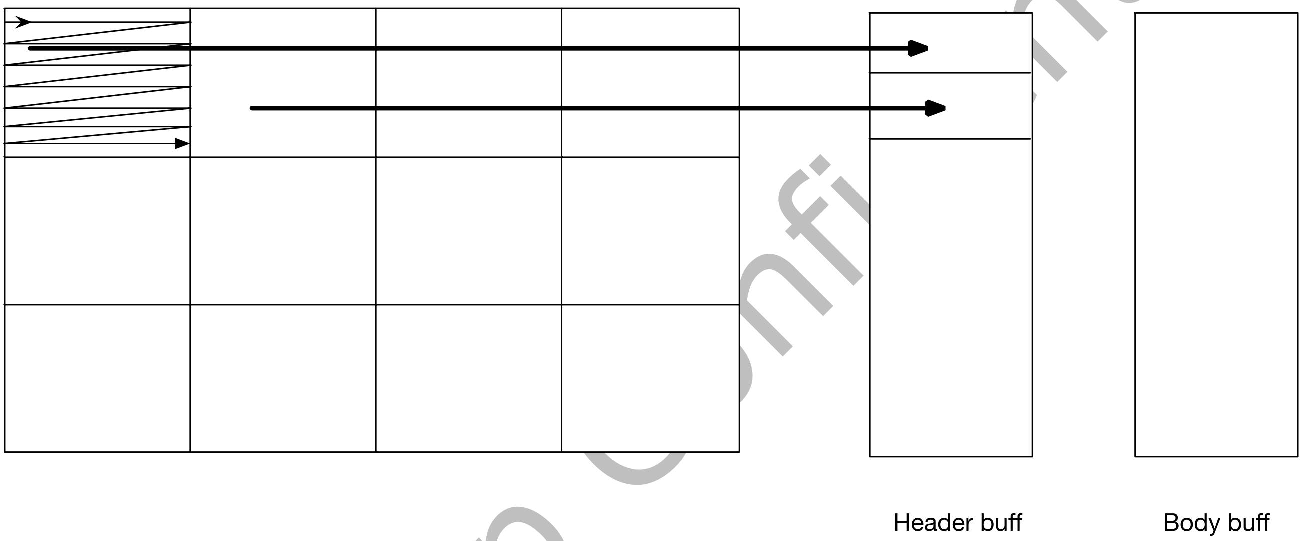


Fig. 5-8 FBC buffer in DDR

5.4.4 Tile8x8 mode

RGA3 support Tile8x8 mode for input and output(only support YUV420SP/YUV422SP/ YUV420SP 10bit/YUV422SP 10bit), we need two buffers in DDR as below:

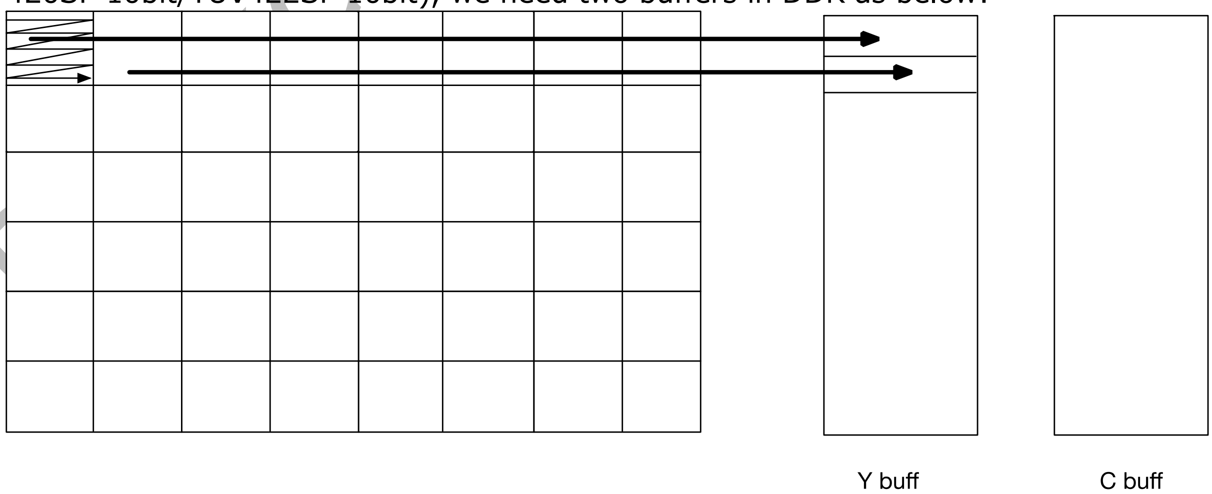


Fig. 5-9 Tile buffer in DDR

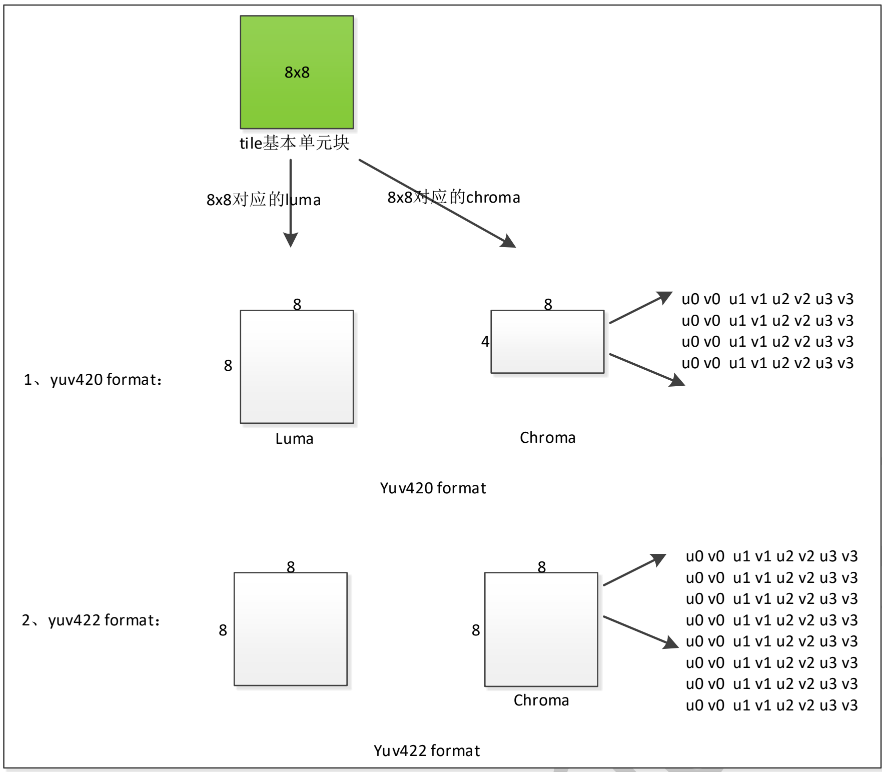


Fig. 5-10 Tile8x8 in DDR

According to different format, data will be stored in different ways as below:

YUV422sp

63 56 48 16 8 0

Y07	Y06	…	Y01	Y00
Y13	Y16	…	Y11	Y10
…	…	…	…	…
Y67	Y66	…	Y61	Y60
Y77	Y76	…	Y71	Y70

V06	U06	…	V00	U00
V26	U26	…	V10	U10
…	…	…	…	…
V66	U66	…	V60	U60
V76	U76	…	V70	U70

YUV420sp

63 56 48 16 8 0

Y07	Y06	…	Y01	Y00
Y13	Y16	…	Y11	Y10
…	…	…	…	…
Y67	Y66	…	Y61	Y60
Y77	Y76	…	Y71	Y70

V06	U06	…	V00	U00
…	…	…	…	…
V66	U66	…	V60	U60

YUV422sp 10bit uncompact
read not support

127 112 96 32 16 0

Y07	dummy	Y06	dummy	…	dummy	Y01	dummy	Y00
Y13	dummy	Y16	dummy	…	dummy	Y11	dummy	Y10
…	…	…	…	…	…	…	…	…
Y67	dummy	Y66	dummy	…	dummy	Y61	dummy	Y60
Y77	dummy	Y76	dummy	…	dummy	Y71	dummy	Y70

V06	dummy	U06	dummy	…	dummy	V00	dummy	U00
V26	dummy	U26	dummy	…	dummy	V10	dummy	U10
…	…	…	…	…	…	…	…	…
V66	dummy	U66	dummy	…	dummy	V60	dummy	U60
V76	dummy	U76	dummy	…	dummy	V70	dummy	U70

YUV420sp 10bit uncompact
read not support

127 112 96 32 16 0

Y07	dummy	Y06	dummy	…	dummy	Y01	dummy	Y00
Y13	dummy	Y16	dummy	…	dummy	Y11	dummy	Y10
…	…	…	…	…	…	…	…	…
Y67	dummy	Y66	dummy	…	dummy	Y61	dummy	Y60
Y77	dummy	Y76	dummy	…	dummy	Y71	dummy	Y70

V06	dummy	U06	dummy	…	dummy	V00	dummy	U00
…	…	…	…	…	…	…	…	…
V66	dummy	U66	dummy	…	dummy	V60	dummy	U60

YUV422sp 10bit compact

79 60 50 20 10 0

Y07	Y06	…	Y01	Y00
Y13	Y16	…	Y11	Y10
…	…	…	…	…
Y67	Y66	…	Y61	Y60
Y77	Y76	…	Y71	Y70

V06	U06	…	V00	U00
V26	U26	…	V10	U10
…	…	…	…	…
V66	U66	…	V60	U60
V76	U76	…	V70	U70

YUV420sp 10bit compact

79 60 50 20 10 0

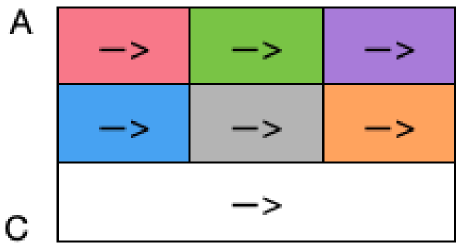
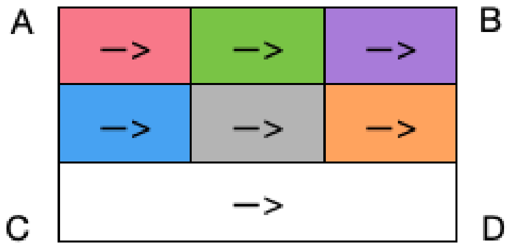
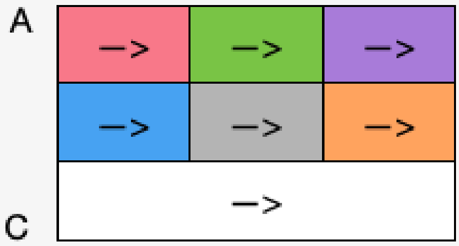
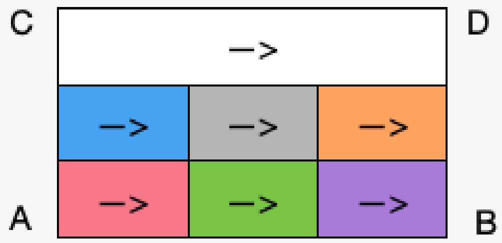
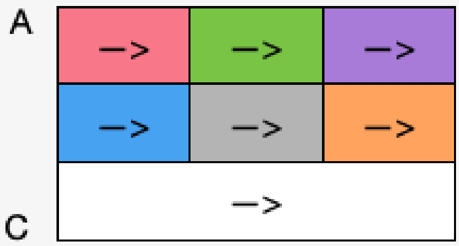
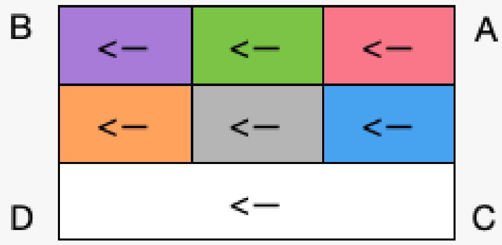
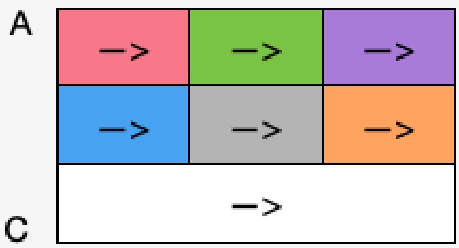
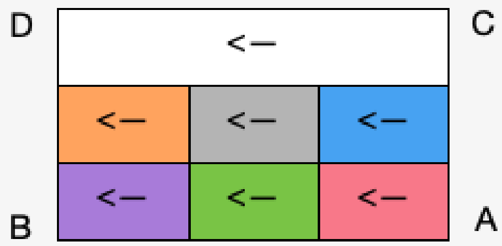
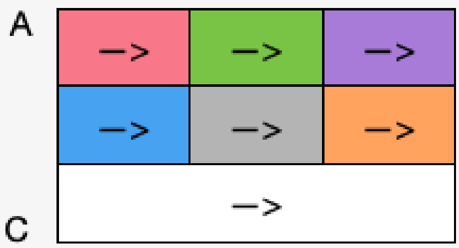
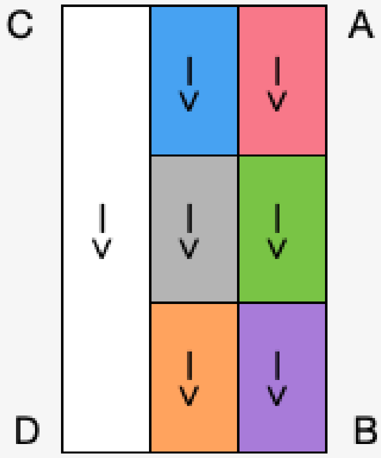
Y07	Y06	…	Y01	Y00
Y13	Y16	…	Y11	Y10
…	…	…	…	…
Y67	Y66	…	Y61	Y60
Y77	Y76	…	Y71	Y70

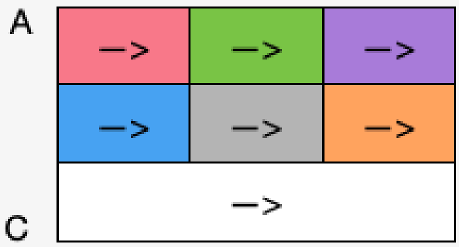
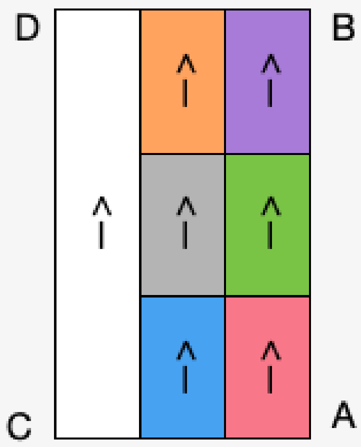
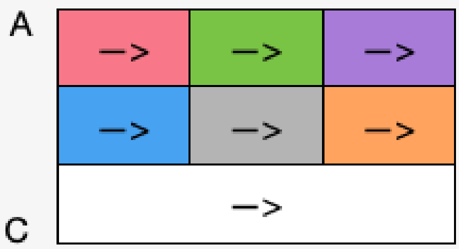
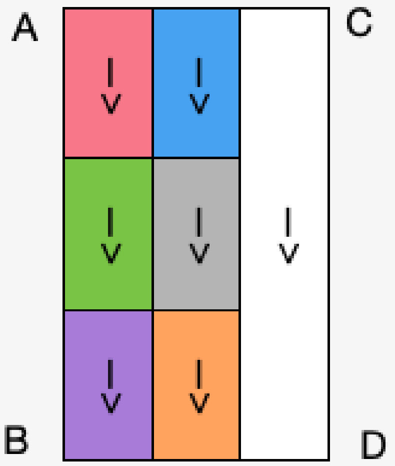
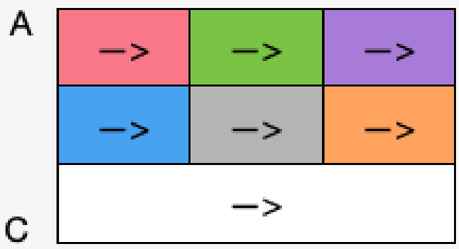
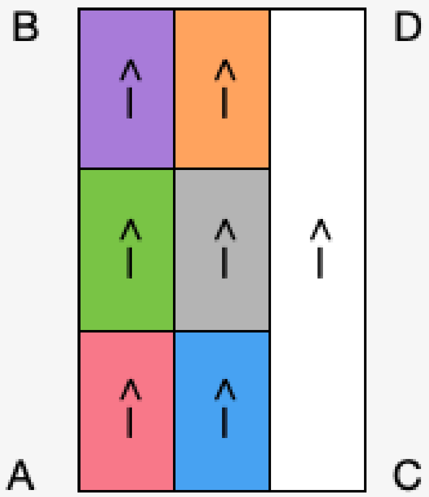
V06	U06	…	V00	U00
…	…	…	…	…
V66	U66	…	V60	U60

Fig. 5-11 Different format in DDR

5.4.5 Orient

RGA3 support rot/xmirror/ymirror, which can show as below:

rot, xmirror,ymirror	original	Orient
0, 0, 0 normal		
0, 0, 1 ymirror		
0, 1, 0 xmirror		
0, 1, 1 rot180		
1, 0, 0 rot90		

rot, xmirror,ymirror	original	Orient
1, 0, 1 rot90+ymirror		
1, 1, 0 rot90+xmirror		
1, 1, 1 rot-90		

5.4.6 CSC

The red, green, and blue(RGB) color space is widely used for computer graphics and displays. Red, green and blue are three primary additive colors. The YCbCr color space is used by the PAL and NTSC composite color video standards. The black-and-white system used only luma(Y) information. Color information(Cb and Cr) was added in such a way that a black-and-white

receiver would still display a normal black-and-white picture. Color receivers decoded the additional color information to display a color picture.
There are four equations used to convert between RGB and YCbCr space.

YUV2RGB:
1) YUV to RGB (BT601L)

R = 1.164(Y-16) + 1.596(V-128)
G = 1.164(Y-16) - 0.391(U-128) - 0.813(V-128)
B = 1.164(Y-16) + 2.018(U-128)

2) YUV to RGB (BT601F)

R = (Y-16) + 1.402(V-128)
G = (Y-16) - 0.344(U-128) - 0.714(V-128)
B = (Y-16) + 1.772(U-128)

3) YUV to RGB (BT709L)

R = 1.164(Y-16) + 1.793(V-128)
G = 1.164(Y-16) - 0.213(U-128) - 0.534(V-128)
B = 1.164(Y-16) + 2.115(U-128)

4) YUV to RGB (BT2020)

R = 1.1636(Y-64) + 1.6778(V-512)
G = 1.1636(Y-64) - 0.1872(U-512) - 0.6501(V-512)
B = 1.1636(Y-64) + 2.1406(U-512)

RGB2YUV:
1) RGB to YUV (BT601L)

Y = 0.257R + 0.504G + 0.098B + 16
Cb =-0.148R - 0.291G + 0.439B + 128
Cr = 0.439R - 0.368G - 0.071B + 128

2) RGB to YUV (BT601F)

Y = 0.299R + 0.5870G + 0.1140B + 0
Cb = -0.1687R - 0.3313G + 0.5000B + 512
Cr = 0.500R - 0.4187G - 0.0813B + 512

3) RGB to YUV (BT709L)

Y = 0.183R + 0.614G + 0.062B + 16
Cb =-0.101R - 0.338G + 0.439B + 128
Cr = 0.439R - 0.399G - 0.040B + 128

4) RGB to YUV (BT2020)

Y = 0.2250R + 0.5807G + 0.0508B + 64
Cb = -0.1223R - 0.3157G + 0.4380B + 512
Cr = 0.4380R - 0.4028G - 0.0352B + 512

5.4.7 Resize

Horizontal can be scale up, scale down, bypass, vertical can be scale up, scale down, bypass, max ratio is 1/8 ~ 8:

```
Scale down:
    factor = int(65536*(dst-1)/(src-1)) + 1
Scale up:
if((dst-1) % (src-1) == 0)
    factor = int(65536*(dst-1)/(src-1)) - 1
else
    factor = int(65536*(dst-1)/(src-1));
```

Scale down: s0~s11 is source pixel, d0~d3 is destination pixel, factor = 0.3, factor = 0.4, factor = 0.9:

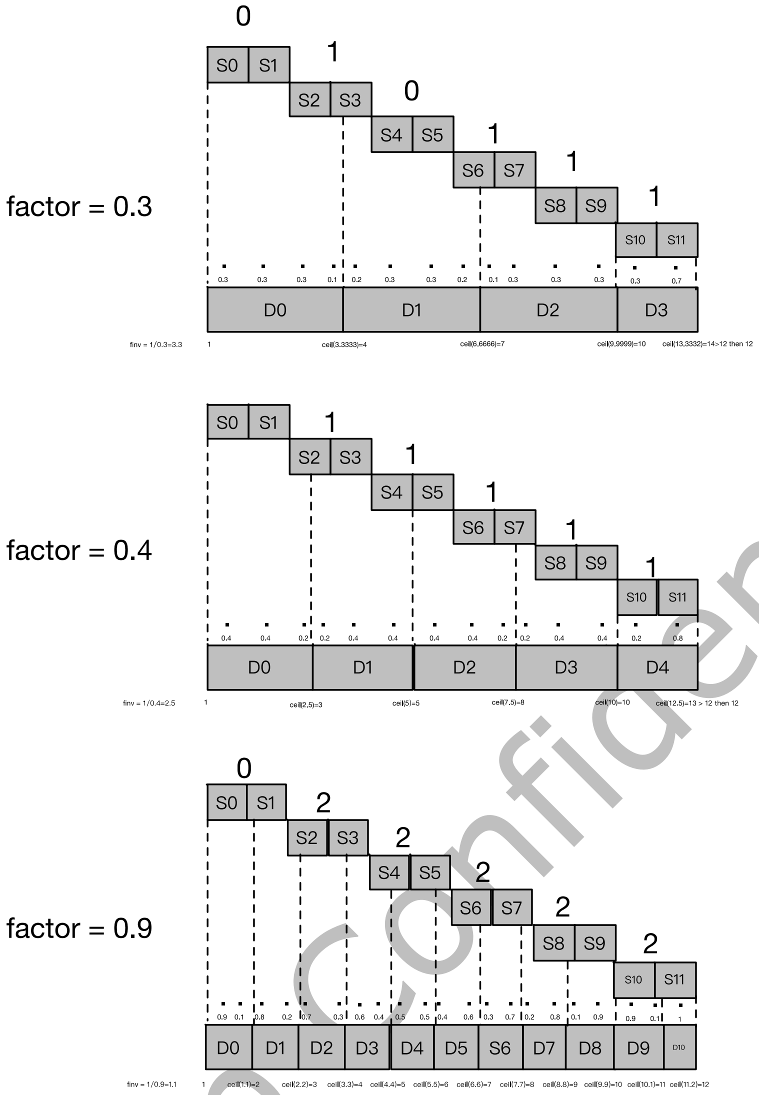


Fig. 5-12 factor = 0.3/0.4/0.9 scale down

Scale up: s0~s11 is source pixel, d0~d3 is destination pixel, factor = 0.3, factor = 0.4, factor = 0.9:

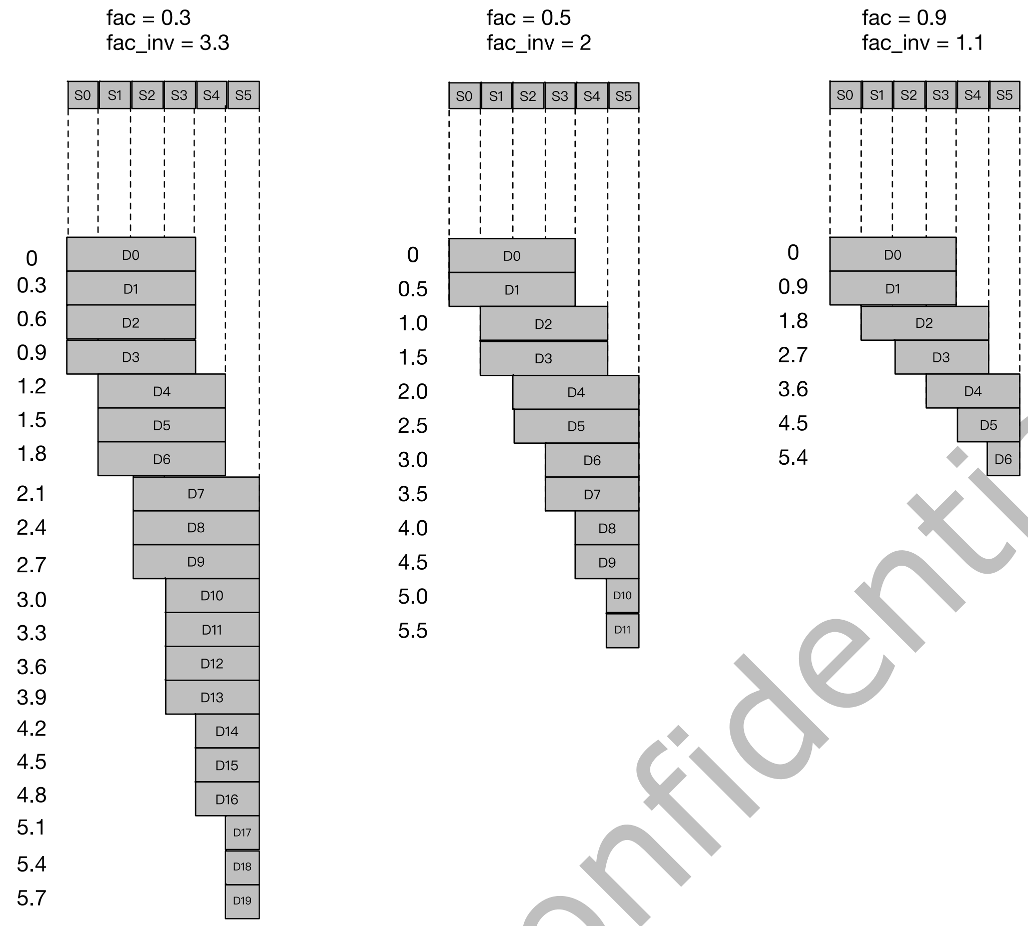


Fig. 5-13 factor = 0.3/0.5/0.9 scale up

5.4.8 Scan/Overlap

5.4.8.1 Overlap mode

RGA3 support win0/win1 layers overlap, after then can write to original DDR address or new DDR address. So RGA3 is ABB/ABC two overlap mode:

1) ABB: A+B->B
2) ABC: A+B->C

ABC mode:

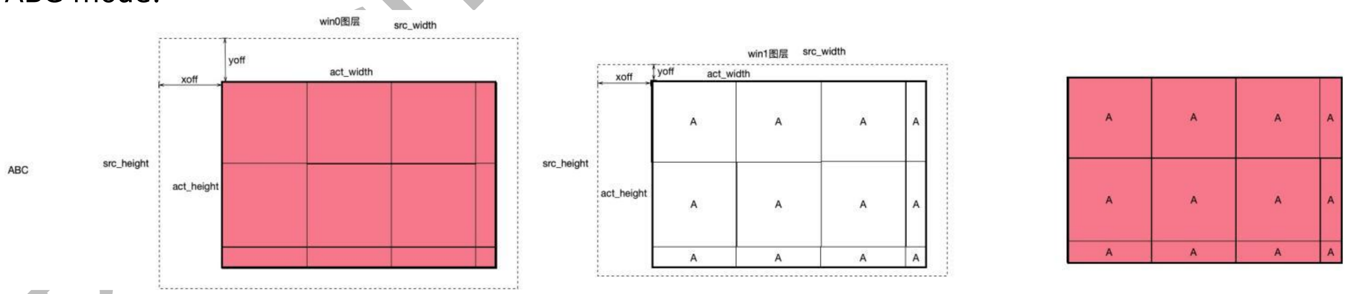


Fig. 5-14 ABC mode

ABB mode:

1) WIN0 = RASTER: win0 act_xoff, act_yoff must aligned to 4pixel by software setting when input format is 10bit, otherwise no limit is required
2) WIN0 = TILE: win0 act_xoff, act_yoff must aligned to 8pixel by software setting
3) WIN0 = FBCE: only support sparse mode, win0 act_xoff, act_yoff must aligned to 16pixel by software setting

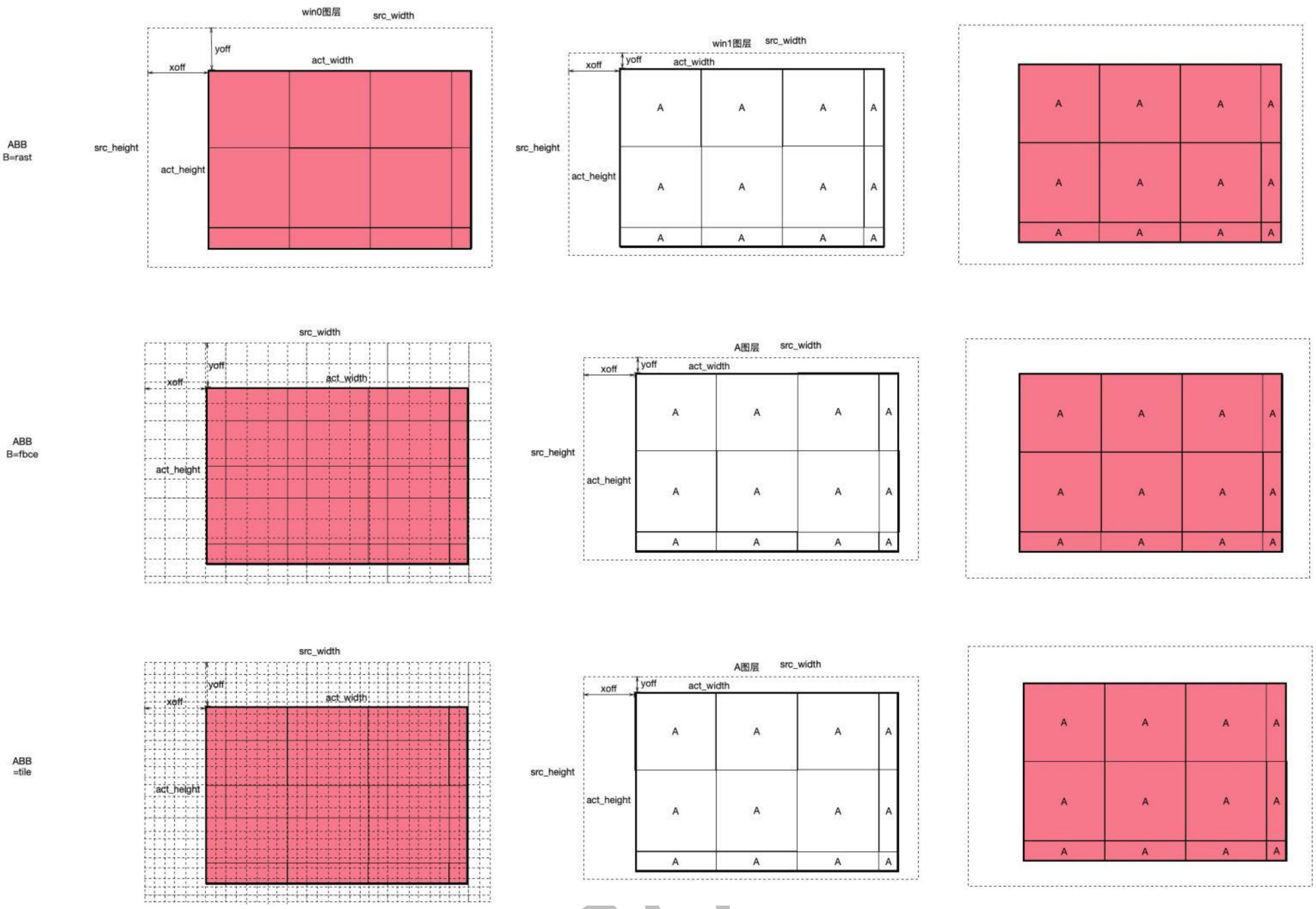


Fig. 5-15 ABB mode

5.4.8.2 Scan

Split and expand destination image using 64x32 block, as show below：
1) mi_wr_mode is fbce mode, horizontal must be aligned to 16pixel
2) mi_wr_mode is tile mode, horizontal and vertical must be aligned to 8pixel

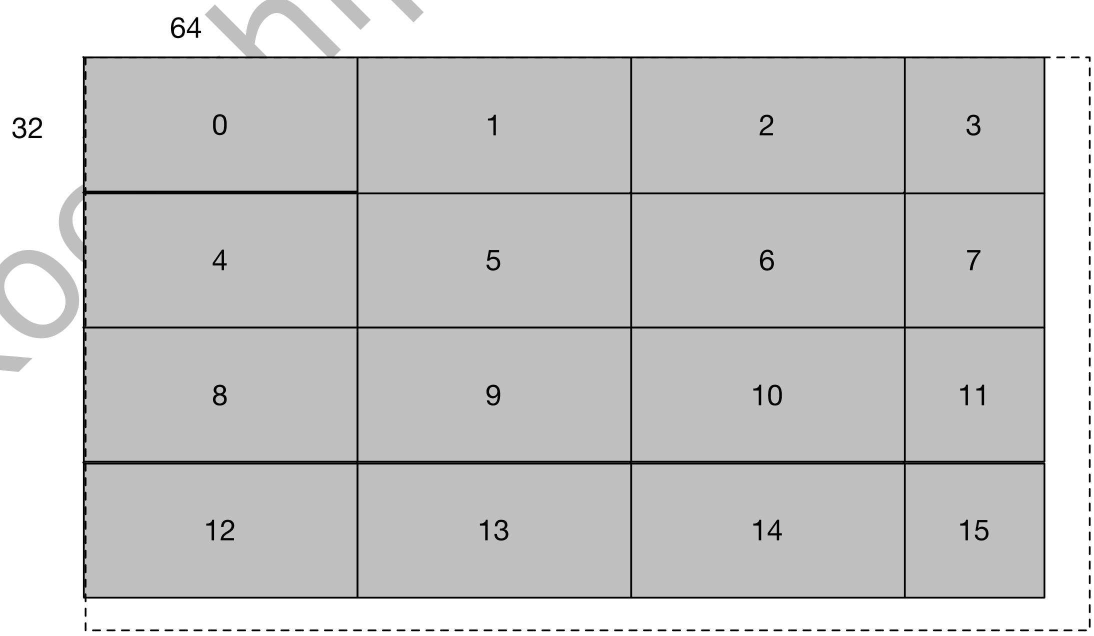


Fig. 5-16 Scan mode with 64x32

According to mi_wr_mode, will generate different scan timing, as below:

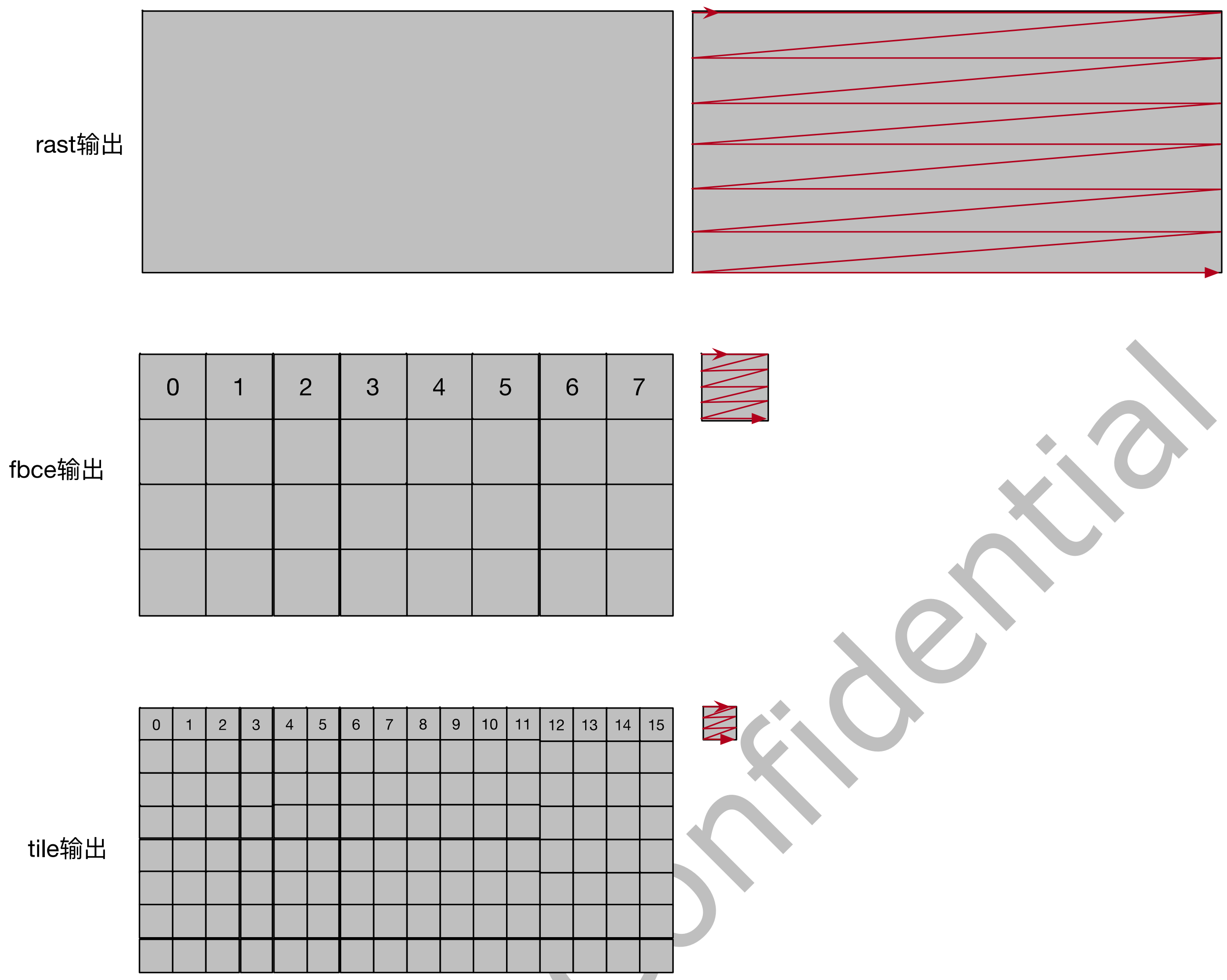
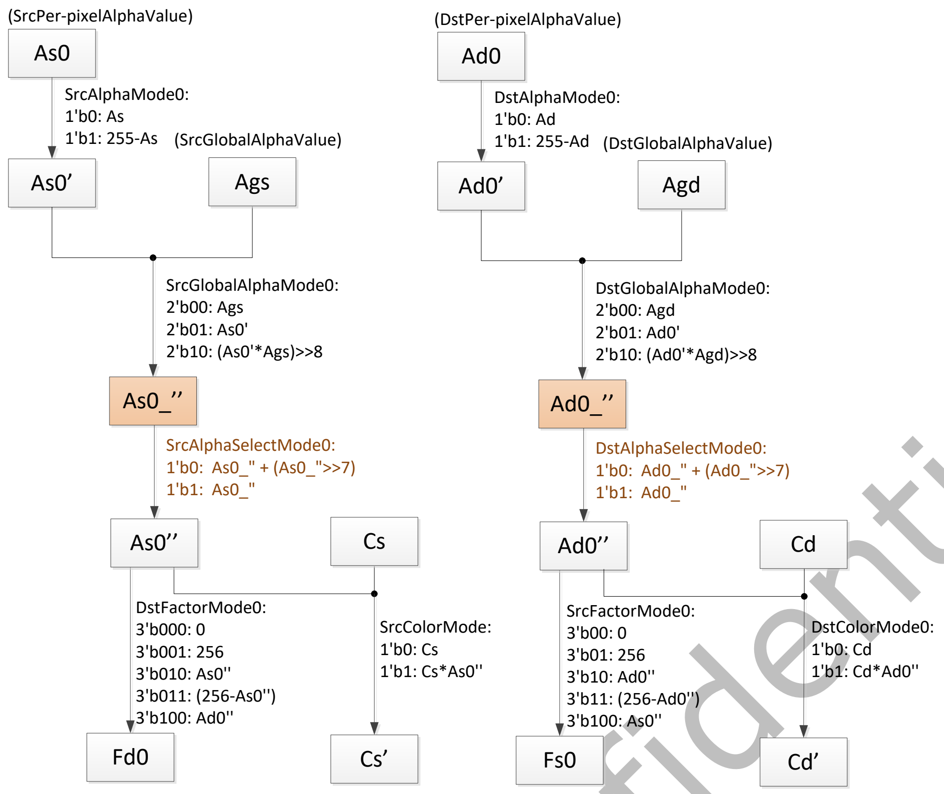


Fig. 5-17 Scan timing for raster/fbce/tile

5.4.8.3 Alpha blending

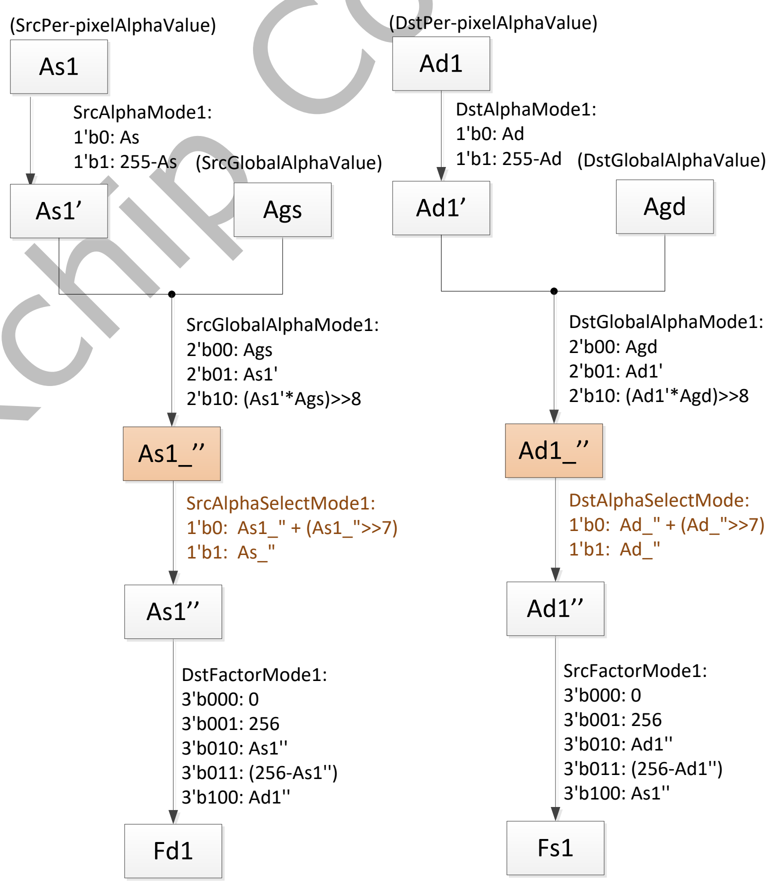
Alpha calculation flow as below:



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')

Fig. 5-18 layer0 alpha blending calculate flow



$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

Fig. 5-19 layer1 alpha blending calculate flow

5.5 Register Description

5.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
RGA3_SYS_CTRL	0x0000	W	0x00000000	System control
RGA3_CMD_CTRL	0x0004	W	0x00000000	Command control
RGA3_CMD_ADDR	0x0008	W	0x00000000	Command address
RGA3_MI_GROUP_CTRL	0x000C	W	0x00000000	DMA read group control
RGA3_ARQOS_CTRL	0x0010	W	0x00000331	DMA read qos control
RGA3_VERSION_NUM	0x0018	W	0x00000000	RGA3 version number
RGA3_VERSION_TIM	0x001C	W	0x00000000	RGA3 version time
RGA3_INT_EN	0x0020	W	0x00000000	Interrupt enable
RGA3_INT_RAW	0x0024	W	0x00000000	Interrupt raw status
RGA3_INT_MSK	0x0028	W	0x00000000	Interrupt mask
RGA3_INT_CLR	0x002C	W	0x00000000	Interrupt clear
RGA3_RO_SRST	0x0030	W	0x00000000	RGA soft reset done
RGA3_STATUS0	0x0034	W	0x00000000	RGA3 status
RGA3_CMD_STATE	0x0040	W	0x00000000	Command state
RGA3_WIN0_CTRL	0x0100	W	0x00000000	Win0 control
RGA3_WIN0_Y_BASE	0x0110	W	0x00000000	Base address of input picture y or RGB or header(FBCD mode) component ring buffer
RGA3_WIN0_C_BASE	0x0114	W	0x00000000	Base address of input picture c or payload (FBCD mode) component ring buffer
RGA3_WIN0_VIR_STRIDE	0x011C	W	0x00000000	Virtual stride of input picture y or RGB or header (FBCD mode) component ring buffer
RGA3_WIN0_FBC_OFF	0x0120	W	0x00000000	Win0 FBCD offset
RGA3_WIN0_SRC_SIZE	0x0124	W	0x00000000	Win0 source size
RGA3_WIN0_ACT_OFF	0x0128	W	0x00000000	Win0 actual offset
RGA3_WIN0_ACT_SIZE	0x012C	W	0x00000000	Win0 actual size
RGA3_WIN0_DST_SIZE	0x0130	W	0x00000000	Win0 destination size
RGA3_WIN0_SCL_FAC	0x0134	W	0x00000000	Win0 scale factor
RGA3_WIN0_C_VIR_STRIDE	0x0138	W	0x00000000	Win0 uv virtual stride
RGA3_WIN1_CTRL	0x0140	W	0x00000000	Win1 control
RGA3_WIN1_Y_BASE	0x0150	W	0x00000000	Base address of input picture y or RGB or header (FBCD mode) component ring buffer
RGA3_WIN1_C_BASE	0x0154	W	0x00000000	Base address of input picture c or payload (FBCD mode) component ring buffer

Name	Offset	Size	Reset Value	Description
RGA3_WIN1_VIR_STRIDE	0x015C	W	0x00000000	Virtual stride of input picture y or RGB or header (FBCD mode) component ring buffer
RGA3_WIN1_FBC_OFF	0x0160	W	0x00000000	Win1 FBCD offset
RGA3_WIN1_SRC_SIZE	0x0164	W	0x00000000	Win1 source size
RGA3_WIN1_ACT_OFF	0x0168	W	0x00000000	Win1 actual offset
RGA3_WIN1_ACT_SIZE	0x016C	W	0x00000000	Win1 actual size
RGA3_WIN1_DST_SIZE	0x0170	W	0x00000000	Win1 destination size
RGA3_WIN1_SCL_FAC	0x0174	W	0x00000000	Win1 scale factor
RGA3_WIN1_C_VIR_STRIDE	0x0178	W	0x00000000	Win1 uv virtual stride
RGA3_OVLP_CTRL	0x0180	W	0x00000000	Overlap control
RGA3_OVLP_OFF	0x0184	W	0x00000000	Overlap offset
RGA3_OVLP_TOP_KEY_MIN	0x0188	W	0x00000000	Overlap top key min value
RGA3_OVLP_TOP_KEY_MAX	0x018C	W	0x00000000	Overlap top key max value
RGA3_OVLP_TOP_COLOR_CTRL	0x0190	W	0x00000000	Overlap top color control
RGA3_OVLP_BOT_COLOR_CTRL	0x0194	W	0x00000000	Overlap bottom color control
RGA3_OVLP_TOP_ALPHA_CTRL	0x0198	W	0x00000000	Overlap top alpha control
RGA3_OVLP_BOT_ALPHA_CTRL	0x019C	W	0x00000000	Overlap bottom alpha control
RGA3_WR_CTRL	0x01A0	W	0x00000000	DMA write control
RGA3_WR_FBCE_CTRL	0x01A4	W	0x00000000	DMA FBCE write control
RGA3_WR_VIR_STRIDE	0x01A8	W	0x00000000	Write virtual stride
RGA3_WR_PL_VIR_STRIDE	0x01AC	W	0x00000000	Write payload virtual stride
RGA3_WR_Y_BASE	0x01B0	W	0x00000000	Write y base address
RGA3_WR_C_BASE	0x01B4	W	0x00000000	Write c base address
RGA3_MMU_DTE_ADDR	0x0F00	W	0x00000000	MMU current page Table address
RGA3_MMU_STATUS	0x0F04	W	0x00000018	MMU status
RGA3_MMU_COMMAND	0x0F08	W	0x00000000	MMU command
RGA3_MMU_PAGE_FAULT_ADDR	0x0F0C	W	0x00000000	MMU address of last page fault
RGA3_MMU_ZAP_ONE_LINE	0x0F10	W	0x00000000	MMU address to be invalidated from the page table cache
RGA3_MMU_INT_RAWSTAT	0x0F14	W	0x00000000	MMU interrupt raw
RGA3_MMU_INT_CLEAR	0x0F18	W	0x00000000	MMU interrupt clear
RGA3_MMU_INT_MASK	0x0F1C	W	0x00000000	MMU interrupt mask

Name	Offset	Size	Reset Value	Description
RGA3_MMU_INT_STATUS	0x0F20	W	0x00000000	MMU interrupt status
RGA3_MMU_AUTO_GATING	0x0F24	W	0x00000002	MMU auto gating
RGA3_MMU_REG_LOAD_EN	0x0F28	W	0x00000001	MMU register load enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.5.2 Detail Register Description

RGA3_SYS_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	sw_frmend_auto_rstn_en Auto reset after frame done
10:9	RW	0x0	sw_rga_bic_mode Bicubic mode: 2'b00: Precise 2'b01: Spline 2'b10: Catrom 2'b11: Mitchell
8	RW	0x0	sw_rga_ram_clk_on RGA ram clock always on
7:5	RO	0x0	reserved
4	RW	0x0	sw_cclk_sreset Core clock soft reset
3	RW	0x0	sw_aclk_sreset Aclk soft reset
2	RW	0x0	sw_rga_lgc_clk_on RGA logic clock always on
1	RW	0x0	sw_cmd_mode Configuration mode 1'b0: Slave mode use AHB write 1'b1: Master mode use AXI read
0	W1C	0x0	rga_start RGA start

RGA3_CMD_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:3	RW	0x000	sw_cmd_incr_num Command increase start max number

Bit	Attr	Reset Value	Description
2	RW	0x0	sw_cmd_stop_mode Command stop mode: 1'b0: Disable 1'b1: Enable
1	RW	0x0	cmd_incr_valid_p Command increase start pulse
0	RW	0x0	cmd_line_st_p Command line start pulse, clear itself 1'b0: Master mode no start 1'b1: Master mode start

RGA3_CMD_ADDR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cmd_base Command address when using master configuration mode, 16B aligned

RGA3_MI_GROUP_CTRL

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mi_rd_group_dis AXI read command group disable 1'b0: Disable 1'b1: Enable
30:3	RO	0x0000000	reserved
2:0	RW	0x0	sw_mi_rd_group_num AXI read command group number 3'b000: fill internal fifo to full 3'b001: Burst*2 3'b010: Burst*3 3'b011: Burst*4 3'b100: Burst*5 3'b101: Burst*6 3'b110: Burst*7 3'b111: Burst*8

RGA3_ARQOS_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x3	sw_noc_hurry_value NOC hurry value 3'b000: The Low priority to NOC 3'b111: The first High priority to NOC

Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:4	RW	0x3	sw_ar_mmu_qos Read qos, configure 0 to 7, default 3
3:1	RO	0x0	reserved
0	RW	0x1	sw_ar_qos_en All bus channel AXI read qos enable 1'b0: Disable 1'b1: Enable

RGA3_VERSION_NUM

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	major RGA3 major number
27:20	RW	0x00	minor RGA3 minor number
19:0	RW	0x00000	svnbulid RGA3 svn build number

RGA3_VERSION_TIM

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	year RGA3 year
15:8	RW	0x00	month RGA3 month
7:0	RW	0x00	date RGA3 date

RGA3_INT_EN

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	int_en_win1_ver_fifo_ren_err RGA3 win1 vertical FIFO read error enable 1'b0: Disable 1'b1: Enable
28	RW	0x0	int_en_win1_ver_fifo_wen_err RGA3 win1 vertical FIFO write error enable 1'b0: Disable 1'b1: Enable
27	RW	0x0	int_en_win1_hor_fifo_ren_err RGA3 win1 horizontal FIFO read error enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
26	RW	0x0	int_en_win1_hor_fifo_wen_err RGA3 win1 horizontal FIFO write error enable 1'b0: Disable 1'b1: Enable
25	RW	0x0	int_en_win1_in_fifo_ren_err RGA3 win1 in FIFO read error enable 1'b0: Disable 1'b1: Enable
24	RW	0x0	int_en_win1_in_fifo_wen_err RGA3 win1 in FIFO write error enable 1'b0: Disable 1'b1: Enable
23:22	RO	0x0	reserved
21	RW	0x0	int_en_win0_ver_fifo_ren_err RGA3 win0 vertical FIFO read error enable 1'b0: Disable 1'b1: Enable
20	RW	0x0	int_en_win0_ver_fifo_wen_err RGA3 win0 vertical FIFO write error enable 1'b0: Disable 1'b1: Enable
19	RW	0x0	int_en_win0_hor_fifo_ren_err RGA3 win0 horizontal FIFO read error enable 1'b0: Disable 1'b1: Enable
18	RW	0x0	int_en_win0_hor_fifo_wen_err RGA3 win0 horizontal FIFO write error enable 1'b0: Disable 1'b1: Enable
17	RW	0x0	int_en_win0_in_fifo_ren_err RGA3 win0 in FIFO read error enable 1'b0: Disable 1'b1: Enable
16	RW	0x0	int_en_win0_in_fifo_wen_err RGA3 win0 in FIFO write error enable 1'b0: Disable 1'b1: Enable
15	RW	0x0	int_en_rga_mi_wr_bus_err RGA3 mi_wr bus error enable 1'b0: Disable 1'b1: Enable
14	RW	0x0	int_en_rga_mi_wr_in_herr RGA3 mi_wr horizontal error enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
13	RW	0x0	int_en_rga_mi_wr_in_verr RGA3 mi_wr vertical error enable 1'b0: Disable 1'b1: Enable
12	RO	0x0	reserved
11	RW	0x0	int_en_win1_v_err RGA3 win1 vertical error enable 1'b0: Disable 1'b1: Enable
10	RW	0x0	int_en_win1_h_err RGA3 win1 horizontal error enable 1'b0: Disable 1'b1: Enable
9	RW	0x0	int_en_win1_fbcd_dec_err RGA3 win1 FBCD decoder error enable 1'b0: Disable 1'b1: Enable
8	RW	0x0	int_en_win1_rd_frm_end RGA3 win1 read frame end enable 1'b0: Disable 1'b1: Enable
7	RW	0x0	int_en_win0_v_err RGA3 win0 vertical error enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	int_en_win0_h_err RGA3 win0 horizontal error enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	int_en_win0_fbcd_dec_err RGA3 win0 FBCD decoder error enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_en_win0_rd_frm_end RGA3 win0 read frame end enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en_cmd_line_finish RGA3 command line finish enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	int_en_rga_mi_rd_bus_err RGA3 DMA read bus error enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1	RW	0x0	int_en_rga_mmu_intr RGA3 MMU interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	int_en_frm_done RGA3 frame done enable 1'b0: Disable 1'b1: Enable

RGA3_INT_RAW

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	int_raw_win1_ver_fifo_ren_err RGA3 win1 vertical FIFO read error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
28	RO	0x0	int_raw_win1_ver_fifo_wen_err RGA3 win1 vertical FIFO write error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
27	RO	0x0	int_raw_win1_hor_fifo_ren_err RGA3 win1 horizontal FIFO read error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
26	RO	0x0	int_raw_win1_hor_fifo_wen_err RGA3 win1 horizontal FIFO write error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
25	RO	0x0	int_raw_win1_in_fifo_ren_err RGA3 win1 in FIFO read error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
24	RO	0x0	int_raw_win1_in_fifo_wen_err RGA3 win1 in FIFO write error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
23:22	RO	0x0	reserved
21	RW	0x0	int_raw_win0_ver_fifo_ren_err RGA3 win0 vertical FIFO read error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid

Bit	Attr	Reset Value	Description
20	RO	0x0	int_raw_win0_ver_fifo_wen_err RGA3 win0 vertical FIFO write error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
19	RO	0x0	int_raw_win0_hor_fifo_ren_err RGA3 win0 horizontal FIFO read error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
18	RO	0x0	int_raw_win0_hor_fifo_wen_err RGA3 win0 horizontal FIFO write error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
17	RO	0x0	int_raw_win0_in_fifo_ren_err RGA3 win0 in FIFO read error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
16	RO	0x0	int_raw_win0_in_fifo_wen_err RGA3 win0 in FIFO write error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
15	RO	0x0	int_raw_rga_mi_wr_bus_err RGA3 mi_wr bus error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
14	RO	0x0	int_raw_rga_mi_wr_in_herr RGA3 mi_wr horizontal error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
13	RW	0x0	int_raw_rga_mi_wr_in_verr RGA3 mi_wr vertical error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
12	RO	0x0	reserved
11	RO	0x0	int_raw_win1_v_err RGA3 win1 vertical error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
10	RO	0x0	int_raw_win1_h_err RGA3 win1 horizontal error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
9	RO	0x0	int_raw_win1_fbcd_dec_err RGA3 win1 FBCD decoder error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid

Bit	Attr	Reset Value	Description
8	RO	0x0	int_raw_win1_rd_frm_end RGA3 win1 read frame end interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
7	RO	0x0	int_raw_win0_v_err RGA3 win0 vertical error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
6	RO	0x0	int_raw_win0_h_err RGA3 win0 horizontal error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
5	RW	0x0	int_raw_win0_fbcd_dec_err RGA3 win0 FBCD decoder error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
4	RO	0x0	int_raw_win0_rd_frm_end RGA3 win0 read frame end interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
3	RO	0x0	int_raw_cmd_line_finish RGA3 command line finish interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
2	RO	0x0	int_raw_rga_mi_rd_bus_err RGA3 DMA read bus error interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
1	RO	0x0	int_raw_rga_mmu_intr RGA3 MMU interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid
0	RO	0x0	int_raw_frm_done RGA3 frame done interrupt raw status 1'b0: Interrupt invalid 1'b1: Interrupt valid

RGA3_INT_MSK

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	int_msk_win1_ver_fifo_ren_err RGA3 win1 vertical FIFO read error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid

Bit	Attr	Reset Value	Description
28	RW	0x0	int_msk_win1_ver_fifo_wen_err RGA3 win1 vertical FIFO write error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
27	RW	0x0	int_msk_win1_hor_fifo_ren_err RGA3 win1 horizontal FIFO read error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
26	RW	0x0	int_msk_win1_hor_fifo_wen_err RGA3 win1 horizontal FIFO write error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
25	RW	0x0	int_msk_win1_in_fifo_ren_err RGA3 win1 in FIFO read error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
24	RW	0x0	int_msk_win1_in_fifo_wen_err RGA3 win1 in FIFO write error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
23:22	RO	0x0	reserved
21	RW	0x0	int_msk_win0_ver_fifo_ren_err RGA3 win0 vertical FIFO read error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
20	RW	0x0	int_msk_win0_ver_fifo_wen_err RGA3 win0 vertical FIFO write error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
19	RW	0x0	int_msk_win0_hor_fifo_ren_err RGA3 win0 horizontal FIFO read error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
18	RW	0x0	int_msk_win0_hor_fifo_wen_err RGA3 win0 horizontal FIFO write error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
17	RW	0x0	int_msk_win0_in_fifo_ren_err RGA3 win0 in FIFO read error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
16	RW	0x0	int_msk_win0_in_fifo_wen_err RGA3 win0 in FIFO write error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid

Bit	Attr	Reset Value	Description
15	RW	0x0	int_msk_rga_mi_wr_bus_err RGA3 mi_wr bus error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
14	RW	0x0	int_msk_rga_mi_wr_in_herr RGA3 mi_wr horizontal error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
13	RW	0x0	int_msk_rga_mi_wr_in_verr RGA3 mi_wr vertical error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
12	RO	0x0	reserved
11	RW	0x0	int_msk_win1_v_err RGA3 win1 vertical error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
10	RW	0x0	int_msk_win1_h_err RGA3 win1 horizontal error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
9	RW	0x0	int_msk_win1_fbcd_dec_err RGA3 win1 FBCD decoder error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
8	RW	0x0	int_msk_win1_rd_frm_end RGA3 win1 read frame end interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
7	RW	0x0	int_msk_win0_v_err RGA3 win0 vertical error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
6	RW	0x0	int_msk_win0_h_err RGA3 win0 horizontal error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
5	RW	0x0	int_msk_win0_fbcd_dec_err RGA3 win0 FBCD decoder error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
4	RW	0x0	int_msk_win0_rd_frm_end RGA3 win0 read frame end interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid

Bit	Attr	Reset Value	Description
3	RW	0x0	int_msk_cmd_line_finish RGA3 command line finish interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
2	RW	0x0	int_msk_rga_mi_rd_bus_err RGA3 DMA read bus error interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
1	RW	0x0	int_msk_rga_mmu_intr RGA3 MMU interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid
0	RW	0x0	int_msk_frm_done RGA3 frame done interrupt mask 1'b0: Interrupt invalid 1'b1: Interrupt valid

RGA3_INT_CLR

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	int_clr_win1_ver_fifo_ren_err RGA3 win1 vertical FIFO read error interrupt clear 1'b0: Disable 1'b1: Enable
28	R/W SC	0x0	int_clr_win1_ver_fifo_wen_err RGA3 win1 vertical FIFO write error interrupt clear 1'b0: Disable 1'b1: Enable
27	R/W SC	0x0	int_clr_win1_hor_fifo_ren_err RGA3 win1 horizontal FIFO read error interrupt clear 1'b0: Disable 1'b1: Enable
26	R/W SC	0x0	int_clr_win1_hor_fifo_wen_err RGA3 win1 horizontal FIFO write error interrupt clear 1'b0: Disable 1'b1: Enable
25	RW	0x0	int_clr_win1_in_fifo_ren_err RGA3 win1 in FIFO read error interrupt clear 1'b0: Disable 1'b1: Enable
24	R/W SC	0x0	int_clr_win1_in_fifo_wen_err RGA3 win1 in FIFO write error interrupt clear 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
23:22	RO	0x0	reserved
21	RW	0x0	int_clr_win0_ver_fifo_ren_err RGA3 win0 vertical FIFO read error interrupt clear 1'b0: Disable 1'b1: Enable
20	RW	0x0	int_clr_win0_ver_fifo_wen_err RGA3 win0 vertical FIFO write error interrupt clear 1'b0: Disable 1'b1: Enable
19	R/W SC	0x0	int_clr_win0_hor_fifo_ren_err RGA3 win0 horizontal FIFO read error interrupt clear 1'b0: Disable 1'b1: Enable
18	RW	0x0	int_clr_win0_hor_fifo_wen_err RGA3 win0 hor horizontal FIFO write error interrupt clear 1'b0: Disable 1'b1: Enable
17	R/W SC	0x0	int_clr_win0_in_fifo_ren_err RGA3 win0 in FIFO read error interrupt clear 1'b0: Disable 1'b1: Enable
16	RW	0x0	int_clr_win0_in_fifo_wen_err RGA3 win0 in FIFO write error interrupt clear 1'b0: Disable 1'b1: Enable
15	R/W SC	0x0	int_clr_rga_mi_wr_bus_err RGA3 mi_wr bus error interrupt clear 1'b0: Disable 1'b1: Enable
14	R/W SC	0x0	int_clr_rga_mi_wr_in_herr RGA3 mi_wr horizontal error interrupt clear 1'b0: Disable 1'b1: Enable
13	R/W SC	0x0	int_clr_rga_mi_wr_in_verr RGA3 mi_wr vertical error interrupt clear 1'b0: Disable 1'b1: Enable
12	RO	0x0	reserved
11	RW	0x0	int_clr_win1_v_err RGA3 win1 vertical error interrupt clear 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
10	R/W SC	0x0	int_clr_win1_h_err RGA3 win1 horizontal error interrupt clear 1'b0: Disable 1'b1: Enable
9	R/W SC	0x0	int_clr_win1_fbcd_dec_err RGA3 win1 FBCD decoder error interrupt clear 1'b0: Disable 1'b1: Enable
8	R/W SC	0x0	int_clr_win1_rd_frm_end RGA3 win1 read frame end interrupt clear 1'b0: Disable 1'b1: Enable
7	R/W SC	0x0	int_clr_win0_v_err RGA3 win0 vertical error interrupt clear 1'b0: Disable 1'b1: Enable
6	R/W SC	0x0	int_clr_win0_h_err RGA3 win0 horizontal error interrupt clear 1'b0: Disable 1'b1: Enable
5	R/W SC	0x0	int_clr_win0_fbcd_dec_err RGA3 win0 FBCD decoder error interrupt clear 1'b0: Disable 1'b1: Enable
4	R/W SC	0x0	int_clr_win0_rd_frm_end RGA3 win0 read frame end interrupt clear 1'b0: Disable 1'b1: Enable
3	R/W SC	0x0	int_clr_cmd_line_finish RGA3 command line finish interrupt clear 1'b0: Disable 1'b1: Enable
2	R/W SC	0x0	int_clr_rga_mi_rd_bus_err RGA3 DMA read bus error interrupt clear 1'b0: Disable 1'b1: Enable
1	R/W SC	0x0	int_clr_rga_mmu_intr RGA3 MMU interrupt clear 1'b0: Disable 1'b1: Enable
0	R/W SC	0x0	int_clr_frm_done RGA3 frame done interrupt clear 1'b0: Disable 1'b1: Enable

RGA3_RO_SRST

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	ro_srst_done RGA soft reset done

RGA3_STATUS0

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	ovlp_ack Ovlp_ack 1'b0: Signal is low 1'b1: Signal is high
18	RO	0x0	ovlp_val Ovlp_val 1'b0: Signal is low 1'b1: Signal is high
17	RO	0x0	scan_ack Scan_ack 1'b0: Signal is low 1'b1: Signal is high
16	RW	0x0	scan_val Scan_val 1'b0: Signal is low 1'b1: Signal is high
15	RO	0x0	win1_ver_ack Win1_ver_ack 1'b0: Signal is low 1'b1: Signal is high
14	RO	0x0	win1_ver_val Win1_ver_val 1'b0: Signal is low 1'b1: Signal is high
13	RO	0x0	win1_hor_ack Win1_hor_ack 1'b0: Signal is low 1'b1: Signal is high
12	RO	0x0	win1_hor_val Win1_hor_val 1'b0: Signal is low 1'b1: Signal is high

Bit	Attr	Reset Value	Description
11	RO	0x0	win1_src_ack Win1_src_ack 1'b0: Signal is low 1'b1: Signal is high
10	RO	0x0	win1_src_val Win1_src_val 1'b0: Signal is low 1'b1: Signal is high
9	RO	0x0	win1_in_ack Win1_in_ack 1'b0: Signal is low 1'b1: Signal is high
8	RO	0x0	win1_in_val Win1_in_val 1'b0: Signal is low 1'b1: Signal is high
7	RO	0x0	win0_ver_ack Win0_ver_ack 1'b0: Signal is low 1'b1: Signal is high
6	RO	0x0	win0_ver_val Win0_ver_val 1'b0: Signal is low 1'b1: Signal is high
5	RO	0x0	win0_hor_ack Win0_hor_ack 1'b0: Signal is low 1'b1: Signal is high
4	RO	0x0	win0_hor_val Win0_hor_val 1'b0: Signal is low 1'b1: Signal is high
3	RO	0x0	win0_src_ack Win0_src_ack 1'b0: Signal is low 1'b1: Signal is high
2	RO	0x0	win0_src_val Win0_src_val 1'b0: Signal is low 1'b1: Signal is high
1	RO	0x0	win0_in_ack Win0_in_ack 1'b0: Signal is low 1'b1: Signal is high

Bit	Attr	Reset Value	Description
0	RO	0x0	win0_in_val Win0_in_val 1'b0: Signal is low 1'b1: Signal is high

RGA3_CMD_STATE

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	cmd_cnt_cur Command current frame counter
15:1	RO	0x0000	reserved
0	RO	0x0	cmd_working Command working status 1'b0: RGA is idle 1'b1: RGA is working

RGA3_WIN0_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_win0_rd_align_dis Raster read mode align disable 1'b0: Enable 1'b1: Disable
29	RW	0x0	sw_win0_perf_opt_dis AXI read performance optimization disable 1'b0: Enable 1'b1: Disable
28	RO	0x0	reserved
27:26	RW	0x0	sw_win0_csc_mode Color space conversion 2'b00: BT601_L 2'b01: BT709 2'b10: BT601_F 2'b11: BT2020
25	RW	0x0	sw_win0_r2y_en Win RGB to YUV transfer, if input is RGB, overlap field is YUV 1'b0: Disable 1'b1: Enable
24	RW	0x0	sw_win0_y2r_en Win YUV to RGB transfer, if input is YUV, overlap field is RGB 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
23	RW	0x0	sw_win_ver_up Win vertical up scale 1'b0: No scale up 1'b1: Scale up
22	RW	0x0	sw_win0_ver_by Win vertical bypass 1'b0: No bypass 1'b1: Bypass
21	RW	0x0	sw_win0_hor_up Win horizontal up scale 1'b0: No scale up 1'b1: Scale up
20	RW	0x0	sw_win0_hor_by Win horizontal bypass 1'b0: No bypass 1'b1: Bypass
19	RO	0x0	reserved
18	RW	0x0	sw_win0_ymirror Input picture y-mirror enable 1'b0: No y-mirror 1'b1: Y-mirror
17	RW	0x0	sw_win0_xmirror Input picture x-mirror enable 1'b0: No x-mirror 1'b1: X-mirror
16	RW	0x0	sw_win0_rot Input picture rotation enable 1'b0: No rotation 1'b1: Rotation Note: YUV422 (or YUYV) does not support rotation
15:14	RO	0x0	reserved
13	RW	0x0	sw_win0_yc_swap YC swap, used by YUYV
12	RW	0x0	sw_win0_pix_swap Input data pixel swap. If RGB mode, do RB swap, else do UV swap
11	RW	0x0	sw_win0_endian_mode Input YUV10bit incompact data endian mode in DDR for raster mode 1'b0: Little-endian 1'b1: Big-endian
10	RW	0x0	sw_win0_yuv10b_compact Input YUV10bit data is compact in DDR for raster mode 1'b0: Incompact 1'b1: Compact

Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_win0_rd_format Defines how YUV picture data is read from DDR 2'b00: Reserved 2'b01: Semi planar, for YUV 4:2:x 2'b10: Interleaved, RGB or YUYV(YUV422 8bti) 2'b11: Reserved
7:4	RW	0x0	sw_win0_pic_format Input picture format 4'b0000: YUV420 8bit 4'b0001: YUV422 8bit 4'b0010: YUV420 10bit 4'b0011: YUV422 10bit 4'b0100: RGB565 4'b0101: RGB888 4'b0110: ARGB8888 4'b0111: RGBA8888 4'b1000: ABGR8888 4'b1001: BGRA8888 4'b1010~4'b1111: Reserved
3	RO	0x0	reserved
2:1	RW	0x0	sw_win0_rd_mode Win0 read mode 2'b00: Raster mode 2'b01: FBCD mode 2'b10: Tile8x8 mode 2'b11: Reserved
0	RW	0x0	sw_win0_enable Win0 enable 1'b0: Win0 disable 1'b1: Win0 enable

RGA3_WIN0_Y_BASE

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_win0_y_base Base address of input picture Y or RGB or header (FBCD mode) component ring buffer Note: 16byte aligned
3:0	RO	0x0	reserved

RGA3_WIN0_C_BASE

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_win0_c_base Base address of input picture C or payload (FBCD mode) component ring buffer Note: 16byte aligned
3:0	RO	0x0	reserved

RGA3_WIN0_VIR_STRIDE

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_win0_vir_stride Virtual stride of input picture y or RGB or header (FBCD mode) component ring buffer Note: Word unit, 16byte align. If header, the recommended configuration is 0.

RGA3_WIN0_FBC_OFF

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win0_fbc_yoff Source picture FBCD up y-offset for src_height + fbc_yoff is 16pixel align.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win0_fbc_xoff Source picture FBCD left x-offset for src_width + fbc_xoff is 16pixel align.

RGA3_WIN0_SRC_SIZE

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win0_src_height Input source picture height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win0_src_width Input source picture width

RGA3_WIN0_ACT_OFF

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win0_act_yoff Actual input picture y-offset

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win0_act_xoff Actual input picture x-offset

RGA3_WIN0_ACT_SIZE

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win0_act_height Actual picture height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win0_act_width Actual picture width

RGA3_WIN0_DST_SIZE

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win0_dst_height Destination picture height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win0_dst_width Destination picture width

RGA3_WIN0_SCL_FAC

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description

31:16	RW	0x0000	sw_win0_ver_fac
			Scale down
			int(65536*(dst-1)/(src-1)) + 1
			scale up
			if((dst-1) % (src-1) == 0)
			    int(65536*(dst-1)/(src-1)) - 1
			else
			    int(65536*(dst-1)/(src-1));

15:0	RW	0x0000	sw_win0_hor_fac
			Scale down
			int(65536*(dst-1)/(src-1)) + 1
			scale up
			if((dst-1) % (src-1) == 0)
			    int(65536*(dst-1)/(src-1)) - 1
			else
			    int(65536*(dst-1)/(src-1));

RGA3_WIN0_C_VIR_STRIDE

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_win0_uv_vir_stride Virtual stride of input picture uv component ring buffer Note: Word unit, 16byte align

RGA3_WIN1_CTRL

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_win1_rd_align_dis Raster read mode align disable 1'b0: Enable 1'b1: Disable
29	RW	0x0	sw_win1_perf_opt_dis AXI read performance optimization disable 1'b0: Enable 1'b1: Disable
28	RO	0x0	reserved
27:26	RW	0x0	sw_win1_csc_mode Color space conversion 2'b00: BT601_L 2'b01: BT709 2'b10: BT601_F 2'b11: BT2020
25	RW	0x0	sw_win1_r2y_en Win RGB to YUV transfer, if input is RGB, overlap field is YUV 1'b0: Disable 1'b1: Enable
24	RW	0x0	sw_win1_y2r_en Win YUV to RGB transfer, if input is YUV, overlap field is RGB 1'b0: Disable 1'b1: Enable
23	RW	0x0	sw_win1_ver_up Win vertical up scale 1'b0: No scale up 1'b1: Scale up
22	RW	0x0	sw_win1_ver_by Win vertical bypass 1'b0: No bypass 1'b1: Bypass
21	RW	0x0	sw_win1_hor_up Win horizontal up scale 1'b0: No scale up 1'b1: Scale up

Bit	Attr	Reset Value	Description
20	RW	0x0	sw_win1_hor_by Win horizontal bypass 1'b0: No bypass 1'b1: Bypass
19	RO	0x0	reserved
18	RW	0x0	sw_win1_ymirror Input picture y-mirror enable 1'b0: No y-mirror 1'b1: Y-mirror
17	RW	0x0	sw_win1_xmirror Input picture x-mirror enable 1'b0: No x-mirror 1'b1: X-mirror
16	RW	0x0	sw_win1_rot Input picture rotation enable 1'b0: No rotation 1'b1: Rotation Note: YUV422 (or YUYV) does not support rotation
15:14	RO	0x0	reserved
13	RW	0x0	sw_win1_yc_swap YC swap, used by YUYV
12	RW	0x0	sw_win1_pix_swap Input data pixel swap. If RGB mode, do RB swap, else do UV swap
11	RW	0x0	sw_win1_endian_mode Input YUV10bit incompact data endian mode in DDR for raster mode 1'b0: Little-endian 1'b1: Big-endian
10	RW	0x0	sw_win1_yuv10b_compact Input YUV10bit data is compact in DDR for raster mode 1'b0: Incompact 1'b1: Compact
9:8	RW	0x0	sw_win1_rd_format Defines how YUV picture data is read from DDR 2'b00: Reserved 2'b01: Semi planar, for YUV 4:2:x 2'b10: Interleaved, RGB or YUYV(YUV422 8bit) 2'b11: Reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_win1_pic_format Input picture format 4'b0000: YUV420 8bit 4'b0001: YUV422 8bit 4'b0010: YUV420 10bit 4'b0011: YUV422 10bit 4'b0100: RGB565 4'b0101: RGB888 4'b0110: ARGB8888 4'b0111: RGBA8888 4'b1000: ABGR8888 4'b1001: BGRA8888 4'b1010~4'b1111: reserved
3	RO	0x0	reserved
2:1	RW	0x0	sw_win1_rd_mode Win1 read mode 2'b00: Raster mode 2'b01: FBCD mode 2'b10: Tile8x8 mode 2'b11: Reserved
0	RW	0x0	sw_win1_enable Win1 enable 1'b0: Win1 disable 1'b1: Win1 enable

RGA3_WIN1_Y_BASE

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_win1_y_base Base address of input picture Y or RGB or header (FBCD mode) component ring buffer Note: 16byte aligned
3:0	RO	0x0	reserved

RGA3_WIN1_C_BASE

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_win1_u_base Base address of input picture uv or payload (FBCD mode) component ring buffer Note: 16byte aligned
3:0	RO	0x0	reserved

RGA3_WIN1_VIR_STRIDE

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_win1_vir_stride Virtual stride of input picture Y or RGB or header (FBCD mode) component ring buffer Note: Word unit, 16byte align. If header, the recommended configuration is 0.

RGA3_WIN1_FBC_OFF

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win1_fbc_yoff Source picture fbcd up y-offset for src_height + fbc_yoff is16pixel align
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win1_fbc_xoff Source picture fbcd left x-offset for src_width + fbc_xoff is16pixel align

RGA3_WIN1_SRC_SIZE

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win1_src_height Input source picture height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win1_src_width Input source picture width

RGA3_WIN1_ACT_OFF

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win1_act_yoff Actual input picture y-offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win1_act_xoff Actual input picture x-offset

RGA3_WIN1_ACT_SIZE

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_win1_act_height Actual picture height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win1_act_width Actual picture width

RGA3_WIN1_DST_SIZE

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_win1_dst_height Destination picture height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_win1_dst_width Destination picture width

RGA3_WIN1_SCL_FAC

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description

31:16	RW	0x0000	sw_win1_ver_fac
			Scale down
			int(65536*(dst-1)/(src-1)) + 1
			scale up
			if((dst-1) % (src-1) == 0)
			    int(65536*(dst-1)/(src-1)) - 1
			else
			    int(65536*(dst-1)/(src-1));

15:0	RW	0x0000	sw_win1_hor_fac
			Scale down
			int(65536*(dst-1)/(src-1)) + 1
			scale up
			if((dst-1) % (src-1) == 0)
			    int(65536*(dst-1)/(src-1)) - 1
			else
			    int(65536*(dst-1)/(src-1));

RGA3_WIN1_C_VIR_STRIDE

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_win1_uv_vir_stride Virtual stride of input picture uv component ring buffer Note: Word unit, 16byte aligned

RGA3_OVLP_CTRL

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:5	RW	0x0000	sw_top_key_en Top key enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_top_alpha_en Top alpha enable 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2	RW	0x0	sw_ovlp_field Overlap field 1'b0: RGB field 1'b1: YUV field
1:0	RW	0x0	sw_ovlp_mode Overlap mode 1'b0: ABC mode 1'b1: ABB mode

RGA3_OVLP_OFF

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_ovlp_yoff Overlap y-offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_ovlp_xoff Overlap x-offset

RGA3_OVLP_TOP_KEY_MIN

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_top_key_vr_min Color key vr min value, if RGB or YUV 8bit, then shift left 2bits
19:10	RW	0x000	sw_top_key_ub_min Color key ub min value, if RGB or YUV 8bit, then shift left 2bits
9:0	RW	0x000	sw_top_key_yg_min Color key yg min value, if RGB or YUV 8bit, then shift left 2bits

RGA3_OVLP_TOP_KEY_MAX

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_top_key_vr_max Color key vr max value, if RGB or YUV 8bit, then shift left 2bits
19:10	RW	0x000	sw_top_key_ub_max Color key ub max value, if RGB or YUV 8bit, then shift left 2bits
9:0	RW	0x000	sw_top_key_yg_max Color key yg max value, if RGB or YUV 8bit, then shift left 2bits

RGA3_OVLP_TOP_COLOR_CTRL

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_top_global_alpha Source global alpha value(Ags)
15:8	RO	0x00	reserved
7:5	RW	0x0	sw_top_factor_m0 Source factor of color channel 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	sw_top_alpha_cal_m0 Source alpha select mode of color channel 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	sw_top_blend_m0 Source alpha blending mode of color channel 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	sw_top_alpha_m0 Source alpha mode of color channel 1'b0: As 1'b1: 255-As
0	RW	0x0	sw_top_color_m0 Source color mode 1'b0: Cs 1'b1: Cs*As0"

RGA3_OVLP_BOT_COLOR_CTRL

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	sw_bot_global_alpha Destination global alpha value(Agd)
15:8	RO	0x00	reserved
7:5	RW	0x0	sw_bot_factor_m0 Destination factor of color channel 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0 3'b101: Ads
4	RW	0x0	sw_bot_alpha_cal_m0 Destination alpha select mode of color channel 1'b0: Ad0_"+Ad0_">> 7 1'b1: Ad0_"
3:2	RW	0x0	sw_bot_blend_m0 Destination alpha blending mode of color channel 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	sw_bot_alpha_m0 Destination alpha mode of color channel 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	sw_bot_color_m0 Destination color mode 1'b0: Cd 1'b1: Cd*Ad0"

RGA3_OVLP_TOP_ALPHA_CTRL

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	sw_top_factor_m1 Source factor of alpha channel 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	sw_top_alpha_cal_m1 Source alpha select mode of alpha channel 1'b0: As0_"+As0_">>7 1'b1: As0_"

Bit	Attr	Reset Value	Description
3:2	RW	0x0	sw_top_blend_m1 Source alpha blending mode of alpha channel 2'b00: Ag 2'b01: As0 2'b10: (As0'*Ags)>>8
1	RW	0x0	sw_top_alpha_m1 Source alpha mode of alpha channel 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

RGA3_OVLP_BOT_ALPHA_CTRL

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	sw_bot_factor_m1 Destination factor of alpha channel 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	sw_bot_alpha_cal_m1 Destination alpha select mode of alpha channel 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	sw_bot_blend_m1 Destination alpha blending mode of alpha channel 2'b00: Ag 2'b01: Ad0" 2'b10: (Ad0"*Agd)>>8
1	RW	0x0	sw_bot_alpha_m1 Destination alpha mode of alpha channel 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

RGA3_WR_CTRL

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	sw_wr_yc_swap YC swap, used by YUYV
19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:13	RW	0x00	sw_outstanding_max MI write ddr outstanding: 6'd0~6'd63
12	RW	0x0	sw_wr_pix_swap Output data pixel swap. If RGB mode, do RB swap, else do UV swap
11	RW	0x0	sw_wr_endian_mode Output YUV10bit incompact data endian mode in DDR 1'b0: Little-endiab 1'b1: Big-endian
10	RW	0x0	sw_wr_yuv10b_compact Output YUV10bit data is compact in DDR 1'b0: Incompact 1'b1: Compact
9:8	RW	0x0	sw_wr_format Defines how YUV picture data is written to DDR 2'b00: Reserved 2'b01: Semi planar, for YUV 4:2:x 2'b10: Interleaved, for RGB or YUYV(YUV422 8bit) 2'b11: Reserved
7:4	RW	0x0	sw_wr_pic_format Output picture format 4'b0000: YUV420 8bit 4'b0001: YUV422 8bit 4'b0010: YUV420 10bit 4'b0011: YUV422 10bit 4'b0100: RGB565 4'b0101: RGB888 4'b0110: ARGB8888 others: Reserved
3	RO	0x0	reserved
2	RW	0x0	sw_wr_fbce_sparse_en Write fbce payload sparse mode enable 1'b0: Non-sparse mode 1'b1: Sparse mode
1:0	RW	0x0	sw_wr_mode Write mode 2'b00: Raster mode 2'b01: FBCE mode 2'b10: Tile8x8 mode 2'b11: Reserved

RGA3_WR_FBCE_CTRL

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_wr_fbce_size_align_dis FBCE output payload size align 1'b0: FBCE 16x16 block payload aligned to 16B 1'b1: FBCE 16x16 block payload not aligned to 16B Note: only valid when YUV420 10bit output
30:14	RO	0x00000	reserved
13:8	RW	0x00	sw_wr_fbce_pl_fifo1_watermark FBCE payload fifo0 watermark, default is 6
7:2	RW	0x00	sw_wr_fbce_pl_fifo0_watermark FBCE payload fifo0 watermark, default is 6
1	RW	0x0	sw_wr_fbce_head_off_dis Write FBCE payload sparse mode enable 1'b0: Payload offset in head 1'b1: Payload no offset in head
0	RW	0x0	sw_wr_fbce_blk_opt_dis FBCE block optimize for DDR 1'b0: Disable 1'b1: Enable

RGA3_WR_VIR_STRIDE

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	sw_wr_vir_stride Virtual stride of output picture Y or RGB or header (FBCE mode) component ring buffer Note: Word unit, 16byte align. If header, the recommended configuration is 0.

RGA3_WR_PL_VIR_STRIDE

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	sw_wr_pl_vir_stride Virtual stride of input picture uv or payload (FBCE compact mode) component ring buffer Note: Word unit, 16byte align

RGA3_WR_Y_BASE

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_wr_y_base Base address of output picture Y or RGB or header (FBCE mode) component ring buffer Note: 16byte align

RGA3_WR_C_BASE

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_wr_u_base Base address of output picture UV or payload (FBCE mode) component ring buffer Note: 16byte align

RGA3_MMU_DTE_ADDR

Address: Operational Base + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	MMU_DTE_ADDR MMU current page Table address
3:0	RW	0x0	reserved Reserved

RGA3_MMU_STATUS

Address: Operational Base + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault
5	RW	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty.
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled.

RGA3_MMU_COMMAND

Address: Operational Base + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGIN 3'b001: MMU_DISABLE_PAGIN 3'b010: MMU_ENABLE_STAL 3'b011: MMU_DISABLE_STAL 3'b100: MMU_ZAP_CACH 3'b101: MMU_PAGE_FAULT_DON 3'b110: MMU_FORCE_RESET

RGA3_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR MMU address of last page fault

RGA3_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE MMU address to be invalidated from the page table cache

RGA3_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	READ_BUS_ERROR Read bus error
0	RO	0x0	PAGE_FAULT Page fault

RGA3_MMU_INT_CLEAR

Address: Operational Base + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	READ_BUS_ERROR Read bus error
0	WO	0x0	PAGE_FAULT Page fault

RGA3_MMU_INT_MASK

Address: Operational Base + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

RGA3_MMU_INT_STATUS
Address: Operational Base + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

RGA3_MMU_AUTO_GATING
Address: Operational Base + offset (0x0F24)

Bit	Attr	Reset Value	Description
31	RW	0x0	mmu_bug_fixed_disable MMU bug fixed disable, must be 1
30:2	RO	0x00000000	reserved
1	RO	0x1	mmu_cfg_mode MMU configuration mode
0	RW	0x0	mmu_auto_gating When it is 1'b1, the MMU will auto gate itself.

RGA3_MMU_REG_LOAD_EN
Address: Operational Base + offset (0x0F28)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	reg_load_mmu_en Register load enable

5.6 Application Notes

5.6.1 Register Partition

RGA3 contains two types of command modes: slave mode, master mode. The registers at the end of the address space (0x0-0xFC) are system registers, including command mode, command parameters, RGA3 status, interrupts and other related registers. Other registers (starting from 0x100) are the parameter configuration registers of the function.

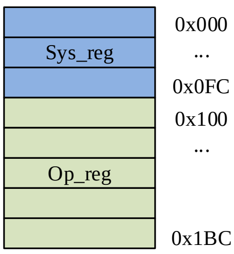


Fig. 5-20 RGA3 software main register-region

5.6.2 Command Modes

1) slave mode(using AHB Bus)
   setting RGA3_SYS_CTRL[1] = 1’b0
   setting RGA3_SYS_CTRL[0] = 1’b1 (frame start) when all configuration is set done
2) master mode(using AXI Bus)
   setting RGA3_SYS_CTRL[1] = 1’b1
   setting RGA3_CMD_ADDR
   setting AXI INCR burst number RGA3_CMD_CTRL[12:3]
   setting RGA3_CMD_CTRL[1]=1’b1 to fetch configuration from DDR:

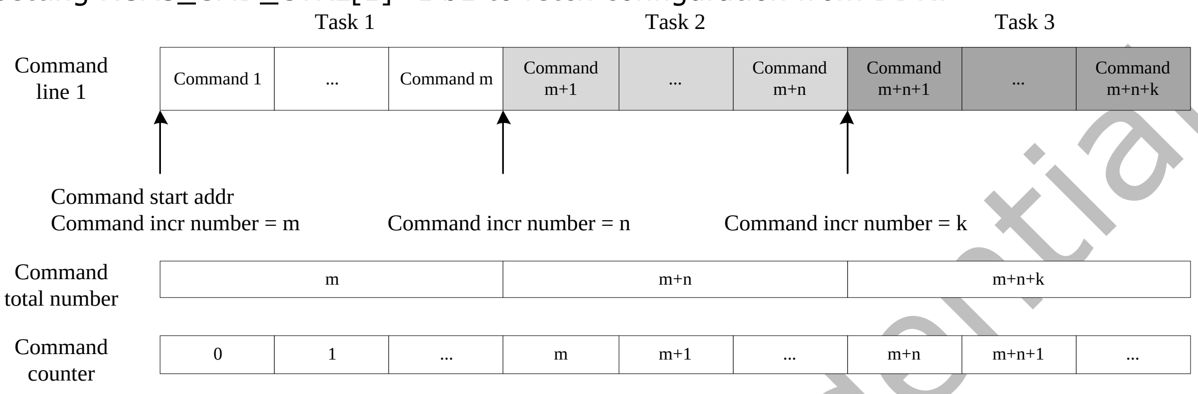


Fig. 5-21 RGA3 command line and command counter

5.6.3 Some special application constraint

1) When input format is YUV422 or YUYV, only xmirror/ymirror is supported, rotation must not be set
2) sw_win_fbc_xoff, sw_win_fbc_yoff only using when rd_mode is FBCD, and then
   sw_win_fbc_xoff + sw_win_src_width must be aligned to 16pixel
   sw_win_fbc_yoff + sw_win_src_height must be aligned to 16pixel
3) act_xoff/act_yoff/act_width/act_height constrain
   input format = YUV420 8 bit: act_xoff/act_yoff/act_width/act_height must be aligned to 2pixel
   input format = YUV420 10bit: act_xoff/act_width must be aligned to 4pixel, act_yoff /act_height must be aligned to 2pixel;
   input format = YUV422 8bit: act_xoff/act_width must be aligned to 2pixel
   input format = YUV422 10bit: act_xoff/act_width must be aligned to 4pixel
4) Overlap constrain
   sw_win0_dst_width >= sw_win1_dst_width
   sw_win0_dst_height >= sw_win1_dst_height
5) Other ABB constrains:
   a) B must not be set orient or resize
   b) B is fbcd layers(16x16), only support spared FBCD, and act_xoffset must be aligned to 16pixel, act_yoffset must be aligned to 16pixel, act_width must be aligned to 16pixel, act_height must be aligned to 16pixel
   c) B is tile layer(8x8), act_xoffset must be aligned to 8pixel, act_yoffset must be aligned to 8pixel, act_width must aligned to 8pixel, act_height must be aligned to 8pixel

Chapter 6 Raster Graphic Acceleration(RGA2)

6.1 Overview

RGA2 is a separate 2D raster graphic accelerator, use to accelerate basic 2D graphics operations, including: image scaling, rotation, BitBLT, alpha blending.

6.1.1 Features

- **Data format**
  - Input data:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551
    - YUV420/YUV422/YVYU422/YVYU420/YUV422SP10bit/YUV420SP10bit
  - Output data:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551
    - YUV420/YUV422/YUV400/Y4/YVYU422/YVYU420
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror & rotation operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT
  - A+B=B only BitBLT, A support rotate & scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - Comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- **Others**
  - Support NN quantize (CLIP((source + offset) * scale) for RGB channel)
- **MMU**
  - 4k/64k page size
  - Four channel: SRC/SRC1/DST/CMD, individual base address and enable control bit
  - TLB pre-fetch

6.1.2 The Constraints

- YUV420/422-8bit virtual stride need 8byte align, xoff/yoff need 2byte align
- YUV420/422-10bit virtual stride need 16byte align, not support xoff/yoff
- Vertical scale down or bypass && Horizontal bi-cubic scale up src0 width<=2048
- Vertical scale up && Horizontal bi-cubic scale up src0 width<=1928
- Vertical scale down or bypass Horizontal BI-linear scale up src0 width<=4096
- Vertical scale up && Horizontal BI-linear scale up src0 width<=3856

6.2 Block Diagram

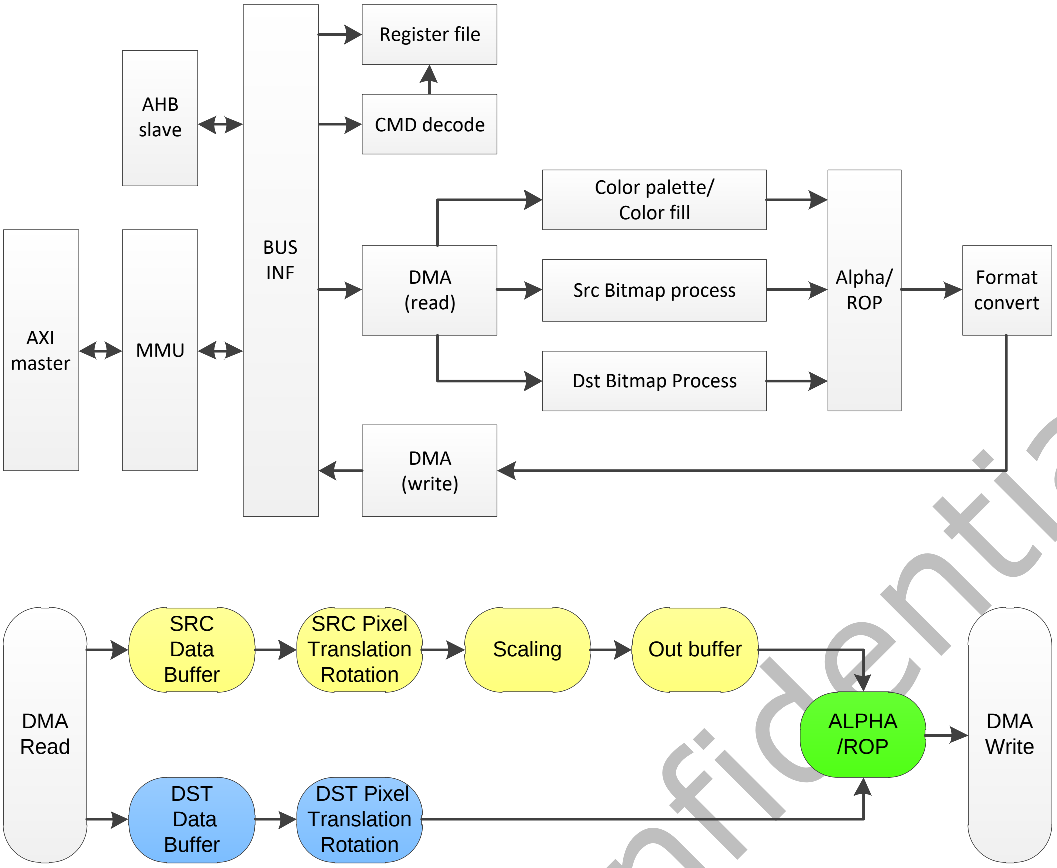


Fig. 6-1 RGA2 Block Diagram

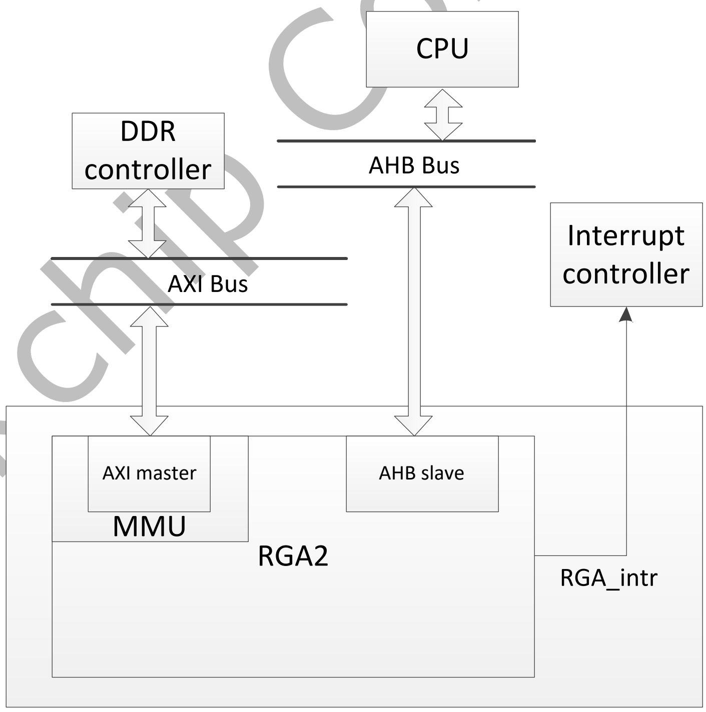


Fig. 6-2 RGA2 in SOC

6.3 Function Description

6.3.1 Data Format

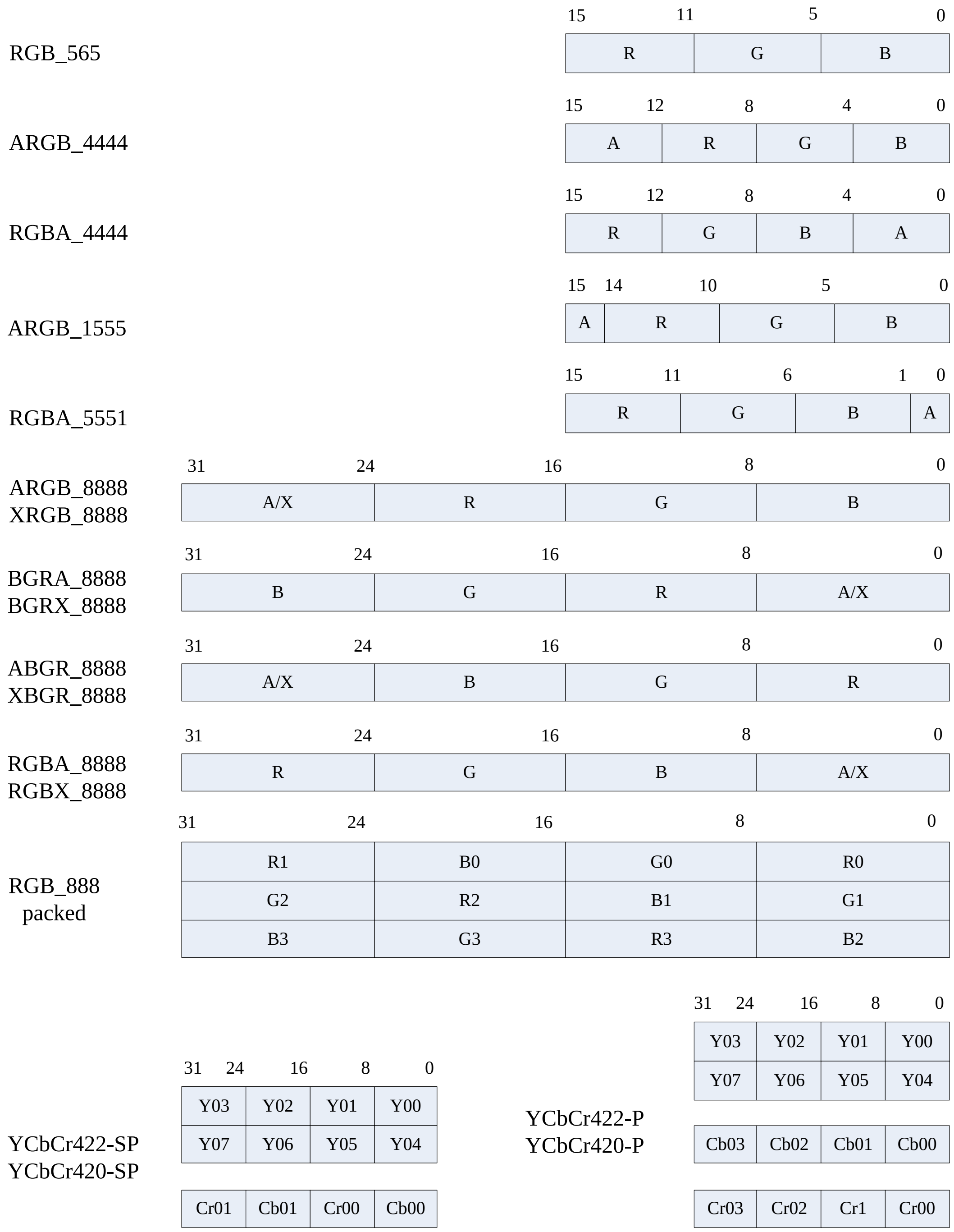


Fig. 6-3 RGA Input Data Format

All input data (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888/AUYV8888. The results are converted to the output data format (defined by DST_OUT_FMT).

6.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.
The down-dithering is done using Dither Allegro.

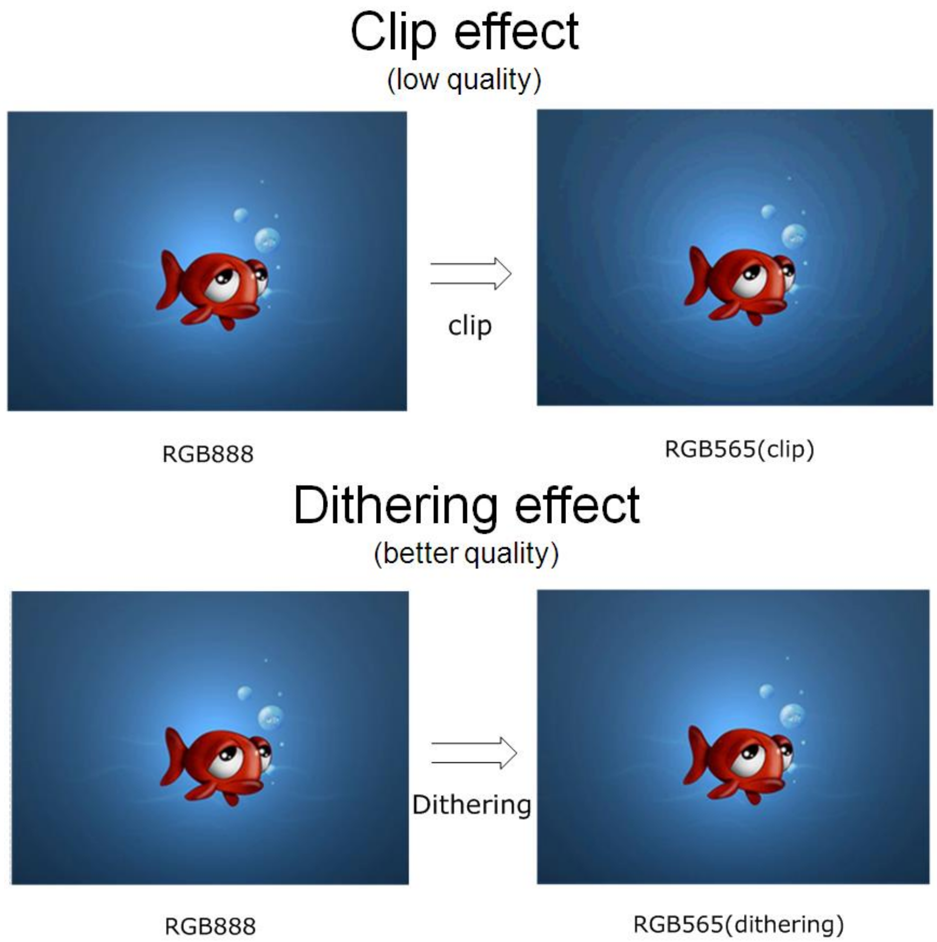
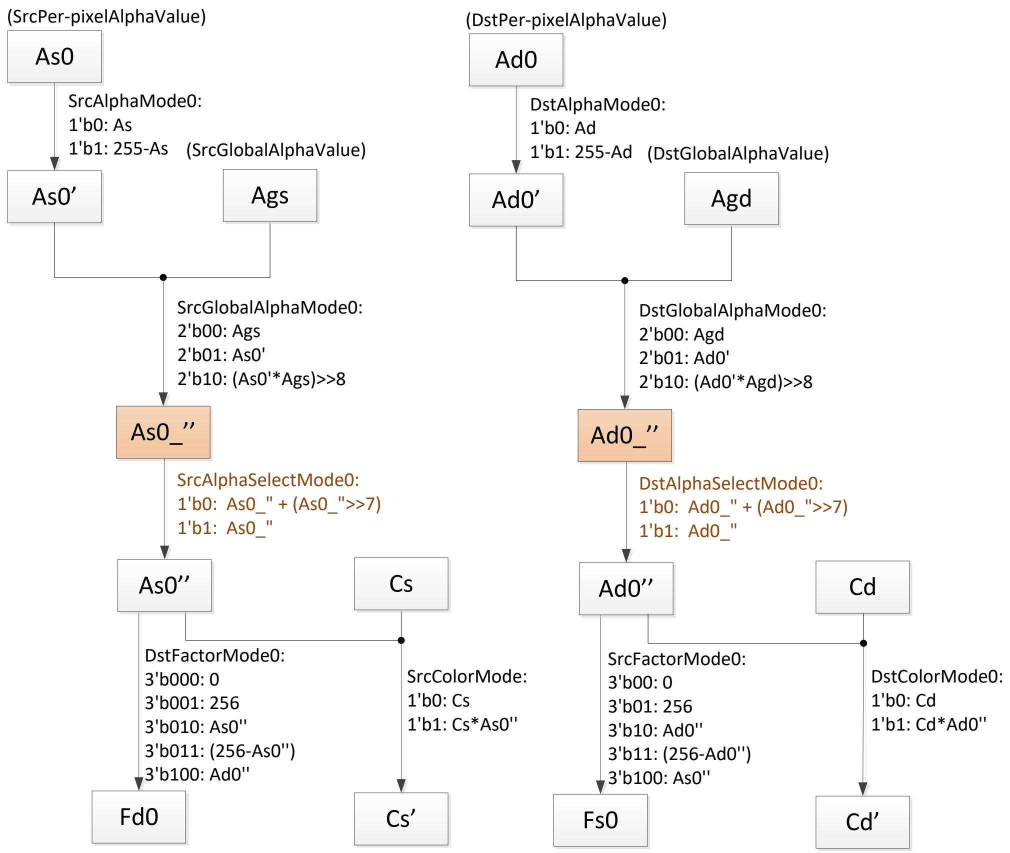


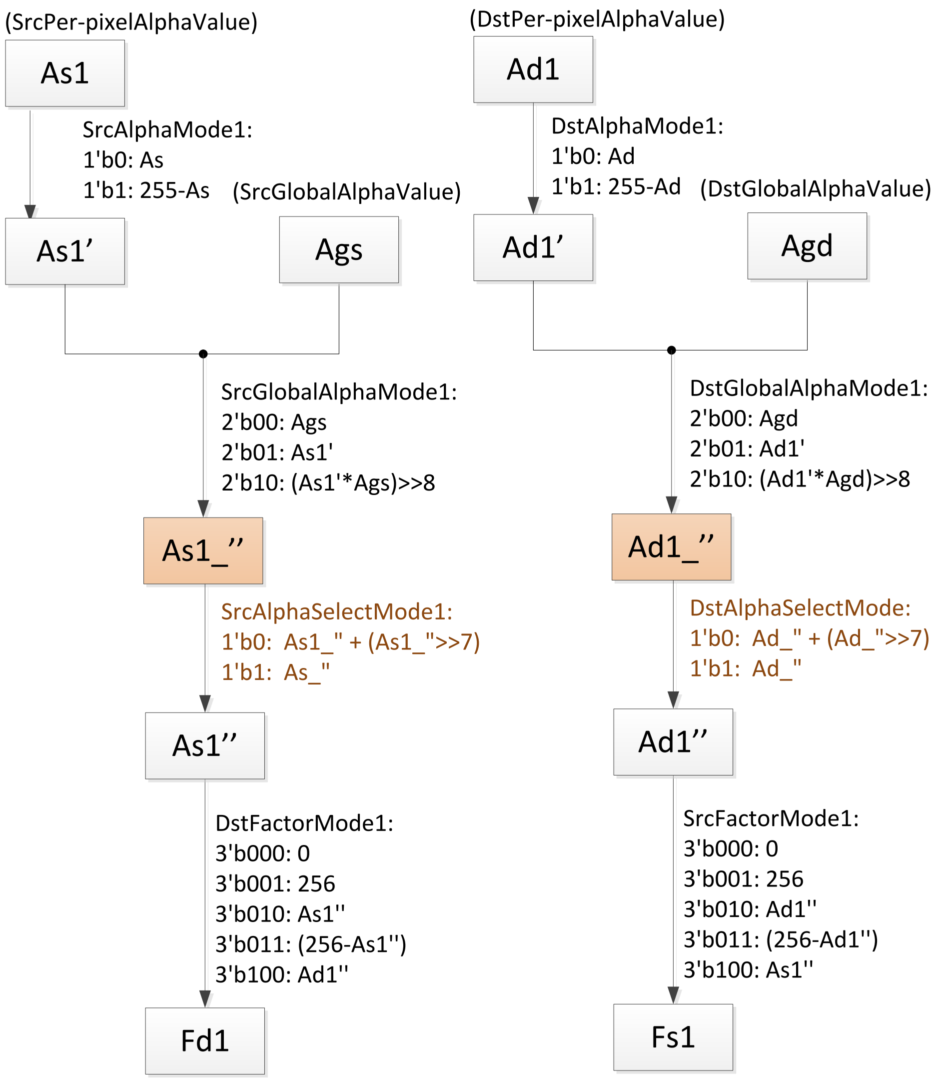
Fig. 6-4 RGA Dither effect

6.3.3 Alpha Mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')



$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \qquad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

Fig. 6-5 alpha mode configure description

6.3.4 Color Fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

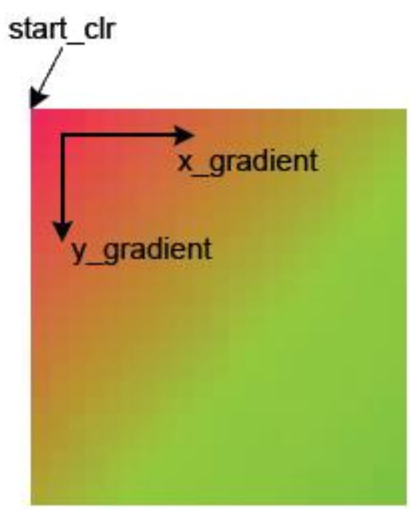


Fig. 6-6 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different

coordinate.
A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;

A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

6.3.5 Scaling

The scaling operation is the image reshaping processing of source image. Scaling is done base on ARGB8888 format.
There are three sampling modes: scale down (Average); scale up(Bi-cubic).

6.3.6 NN Quantize

The NN quantize is for NN pre_process using. The function is CLIP((source + offset) * scale) for R G B channel. When use this function, the signal sw_dst_nn_quantize_en and reg NN_QUANTIZE_SCALE, NN_QUANTIZE_OFFSET need be configured.

6.4 Register description

6.4.1 Register Summary

Slave address can be divided into different length for different usage, which is shown as follows.

Name	Offset	Size	Reset Value	Description
RGA2_SYS_CTRL	0x0000	W	0x00000044	RGA system control register
RGA2_CMD_CTRL	0x0004	W	0x00000000	RGA command control register
RGA2_CMD_BASE	0x0008	W	0x00000000	RGA command codes base address register
RGA2_STATUS1	0x000C	W	0x00000000	RGA status register
RGA2_INT	0x0010	W	0x00000000	RGA interrupt register
RGA2_MMU_CTRL0	0x0014	W	0x00000000	RGA MMU control 0 register
RGA2_MMU_CMD_BASE	0x0018	W	0x00000000	MMU CMD channel base address
RGA2_STATUS2	0x001C	W	0x00000000	RGA status register
RGA2_WORK_CNT	0x0020	W	0x00000000	RGA work counter
RGA2_VERSION_INFO	0x0028	W	0x00000000	RTL version and FPGA version information
RGA2_PERF_LATENCY_CTRL0	0x0040	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_LATENCY_CTRL1	0x0044	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_RD_MAX_LATENCY_NUM	0x0048	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_RD_LATENCY_SAMP_NUM	0x004C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_RD_LATENCY_ACC_SUM	0x0050	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_RD_AXI_TOTAL_BYTE	0x0054	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_WR_AXI_TOTAL_BYTE	0x0058	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_WORKING_CNT	0x005C	W	0x00000000	Only exist when this IP has axi_performance monitor feature

Name	Offset	Size	Reset Value	Description
RGA2_DST_CSC_00	0x0060	W	0x000000BC	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_01	0x0064	W	0x00000274	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_02	0x0068	W	0x00000040	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF0	0x006C	W	0x00004200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_10	0x0070	W	0x00000798	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_11	0x0074	W	0x000006A4	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_12	0x0078	W	0x000001C0	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF1	0x007C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_20	0x0080	W	0x000001C0	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_21	0x0084	W	0x00000668	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_22	0x0088	W	0x000007D8	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF2	0x008C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA2_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA2_SRC_BASE0	0x0108	W	0x00000000	RGA source image Y/RGB base address register
RGA2_SRC_BASE1	0x010C	W	0x00000000	RGA source image Cb/Cbr base address register
RGA2_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register
RGA2_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA2_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number register
RGA2_SRC_ACT_INFO	0x011C	W	0x00000000	RGA source image active width/height register
RGA2_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA2_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA2_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA2_SRC_FG_COLOR	0x012C	W	0x00000000	RGA source image foreground color
RGA2_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_CP_GR_A	0x0130	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_SRC_TR_COLOR1	0x0134	W	0x00000000	RGA source image transparency color max value

Name	Offset	Size	Reset Value	Description
RGA2_CP_GR_B	0x0134	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_DST_INFO	0x0138	W	0x00000000	RGA destination format register
RGA2_DST_BASE0	0x013C	W	0x00000000	RGA destination image base address 0 register
RGA2_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA2_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register
RGA2_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register
RGA2_DST_ACT_INFO	0x014C	W	0x00000000	RGA destination image active width/height register
RGA2_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA2_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Description
RGA2_FADING_CTRL	0x0158	W	0x00000000	Fading control register
RGA2_PAT_CON	0x015C	W	0x00000000	Pattern size/offset register
RGA2_ROP_CON0	0x0160	W	0x00000000	ROP code 0 control register
RGA2_CP_GR_G	0x0160	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_DST_Y4MAP_LUT0	0x0160	W	0x76543210	Y4MAP LUT REGS from lut0 to lut7
RGA2_NN_QUANTIZE_SCALE	0x0160	W	0x00000000	Quantize scale of RGB (2bit integer+8bit fraction, 0~3.99)
RGA2_NN_QUANTIZE_OFFSET	0x0164	W	0x00000000	Quantize offset of RGB (1bit signed + 8bit integer)
RGA2_CP_GR_R	0x0164	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_DST_Y4MAP_LUT1	0x0164	W	0xFEDCBA98	Y4MAP LUT REGS from lut8 to lut15
RGA2_ROP_CON1	0x0164	W	0x00000000	ROP code 1 control register
RGA2_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA2_MMU_CTRL1	0x016C	W	0x00000000	RGA MMU control register 1
RGA2_MMU_SRC_BASE	0x0170	W	0x00000000	RGA source MMU TLB base address
RGA2_MMU_SRC1_BASE	0x0174	W	0x00000000	RGA source1 MMU TLB base address
RGA2_MMU_DST_BASE	0x0178	W	0x00000000	RGA destination MMU TLB base address
RGA2_MMU_ELS_BASE	0x017C	W	0x00000000	RGA else channel MMU TLB base address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

6.4.2 Detail Registers Description

RGA2_SYS_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	sw_rst_handsave_p It would save protect-rstn into initial status if long time dead in protect-rstn status(auto clear into '0').

Bit	Attr	Reset Value	Description
6	RW	0x1	sw_rst_protect_e Protect-rstn mode enable. It would be ensure all AXI write/read operation into completion status when sw_cclk_sreset_p or sw_aclk_sreset_p valid.
5	RW	0x0	sw_auto_rst It would auto-resetn after one frame finish. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except configure registers.
3	WO	0x0	sw_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except configure registers.
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 1'b0: Disable 1'b1: Enable
1	WO	0x0	sw_cmd_mode RGA command mode 1'b0: Slave mode 1'b1: Master mode
0	W1C	0x0	sw_cmd_op_st_p Only used in passive (slave) control mode

RGA2_CMD_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop RGA command stop mode. Command execution would stop after the current graphic operation finish if set this bit to 1.
1	WO	0x0	sw_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total command number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sw_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total command number would reset to RGA_INCR_CMD_NUM.

RGA2_CMD_BASE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cmd_base RGA command codes base address

RGA2_STATUS1

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RO	0x00	reserved
0	RO	0x0	sw_rga_sta RGA engine status 1'b0: Idle 1'b1: Working

RGA2_INT
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_mmu_e MMU interrupt enable
8	RW	0x0	sw_intr_err_e Error interrupt enable
7	WO	0x0	sw_intr_cf_clr Current command finished interrupt clear
6	WO	0x0	sw_intr_af_clr All command finished interrupt clear
5	WO	0x0	sw_intr_mmu_clr MMU interrupt clear
4	WO	0x0	sw_intr_err_clr Error interrupt clear
3	RO	0x0	sw_intr_cf Current command finished interrupt flag
2	RO	0x0	sw_intr_af All command finished interrupt flag
1	RO	0x0	sw_intr_mmu MMU interrupt
0	RO	0x0	sw_intr_err Error interrupt flag

RGA2_MMU_CTRL0
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:9	RW	0x0	sw_els_ch_priority The priority of this channel
8:7	RW	0x0	sw_dst_ch_priority The priority of this channel
6:5	RW	0x0	sw_src1_ch_priority The priority of this channel
4:3	RW	0x0	sw_src_ch_priority The priority of this channel
2	RW	0x0	sw_cmd_mmu_flush RGA CMD channel MMU TLB flush. Set 1 to this bit to flush MMU TLB, and auto clear.

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_cmd_mmu_en RGA CMD channel MMU enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_mmu_page_size RGA MMU Page table size 1'b0: 4KB page 1'b1: 64KB page

RGA2_MMU_CMD_BASE

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_cmd_base RGA command MMU TLB base address (word)

RGA2_STATUS2

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:11	RO	0x0	rpp_mkram_rready Rpp mkram rready
10:6	RO	0x00	dstrpp_outbuf_rready Dstrpp outbuf rready
5:2	RO	0x0	srcrpp_outbuf_rready Srcrpp outbuf rready
1	RO	0x0	bus_error Bus error status
0	RO	0x0	rpp_error RPP error status

RGA2_WORK_CNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	sw_work_cnt RGA total working counter

RGA2_VERSION_INFO

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major Used for IP structure version information
23:16	RW	0x00	minor Big feature change under same structure
15:0	RW	0x0000	svnbuild RTL current SVN number

RGA2_PERF_LATENCY_CTRL0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr AXI Read latency threshold

Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_rd_latency_id AXI read channel id for latency AXI_PERF test
3	RW	0x0	sw_axi_cnt_type 1'b0: AXI transfer test 1'b1: DDR align transfer test
2	RW	0x0	sw_axi_perf_frm_type 1'b0: Clear by software configuration 1'b1: Clear by frame end or by software configuration
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enable note: user need write 1 to this bit and then write 0 to generate a clear pulse
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

RGA2_PERF_LATENCY_CTRL1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type 1'b0: Count all write channels 1'b1: Count sw_aw_count_id write channel only
2	RW	0x0	sw_ar_cnt_id_type 1'b0: Count all read channels 1'b1: Count sw_ar_count_id read channel only
1:0	RW	0x0	sw_addr_align_type 2'b00: 16-Byte align 2'b01: 32-Byte align 2'b10: 64-Byte align 2'b11: 128-Byte align

RGA2_PERF_RD_MAX_LATENCY_NUM

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rd_max_latency_num AXI max read latency(unit: cycles)

RGA2_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num AXI read latency total sample number

RGA2_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum AXI read latency (>sw_rd_latency_thr) total number

RGA2_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_rd_axi_total_byte AXI active total read bytes/DDR align read bytes

RGA2_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_wr_axi_total_byte AXI active total write bytes/DDR align write bytes

RGA2_PERF_WORKING_CNT
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_working_cnt RKIP working counter

RGA2_DST_CSC_00
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x0bc	sw_dst_coe_00 1bit signed+10bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_01
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x274	sw_dst_coe_01 1bit signed+10bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_02
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x040	sw_dst_coe_02 1bit signed+10bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_OFF0
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
18:0	RW	0x04200	sw_dst_coe_off0 1bit signed+8bit integer+10bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_10
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x798	sw_dst_coe_10 1bit signed+10bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_11
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x6a4	sw_dst_coe_11 1bit signed+10bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_12
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x1c0	sw_dst_coe_12 1bit signed+10bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_OFF1
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x20200	sw_dst_coe_off1 1bit signed+8bit integer+10bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_20
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x1c0	sw_dst_coe_20 1bit signed+10bit factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_21
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
10:0	RW	0x668	sw_dst_coe_21 1bit signed+10bit factorr V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_22
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x7d8	sw_dst_coe_22 1bit signed+10bit factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_OFF2
Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x20200	sw_dst_coe_off2 1bit signed+8bit integer+10bit factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_MODE_CTRL
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 1'b0:Clip 1'b1:Not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 1'b0: Solid color 1'b1: Pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 1'b0: SRC + DST => DST 1'b1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 3'b000: Bitblt 3'b001: Color palette 3'b010: Rectangle fill 3'b011: Update palette LUT/pattern ram

RGA2_SRC_INFO

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_src_yuv10_round_e This bit valid when RGA2E/2L support YUV 10bit picture input 1'b0: YUV 10bit to 8bit round disable 1'b1: YUV 10bit to 8bit round enable
27	RW	0x0	sw_src_yuv10_e This bit valid when RGA2E/2L support YUV 10bit picture input. 1'b0: YUV 10bit disable 1'b1: YUV 10bit enable
26	RW	0x0	sw_vsp_mode 1'b0:By-cubic 1'b1:Bi-linear
25:24	RW	0x0	sw_bic_coe_sel SRC BI-cubic scaling coefficient select 2'b00: CATROM 2'b01: MITCHELL 2'b10: HERMITE 2'b11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 1'b0: Disable 1'b1: Enable
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
18	RW	0x0	sw_src_trans_mode Source transparency mode 1'b0: Normal stencil test (color key) 1'b1: Inverted stencil test
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 2'b00No scaling 2'b01: Down-scaling 2'b10: Up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 2'b00No scaling 2'b01: Down-scaling 2'b10: Up-scaling
13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 2'b00: No mirror 2'b01: X mirror 2'b10: Y mirror 2'b11: X mirror + y mirror

Bit	Attr	Reset Value	Description
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 2'b00: 0 degree 2'b01: 90 degree 2'b10: 180 degree 2'b11: 270 degree
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 2'b00: Bypass 2'b01: BT.601-range0(limit range) 2'b10: BT.601-range1(full range) 2'b11: BT.709-range0(limit range)
7	RW	0x0	sw_cp_endian Source Color palette endian swap 1'b0: Big endian 1'b1: Little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 1'b0: CrCb 1'b1: CbCr For YVYU422 mode, UV swap 1'b0: YVYU422(U LSB) 1'b1: YUYV422(V LSB)
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 1'b0: BGR 1'b1: RGB For YVYU422 mode, YC swap 1'b0: YVYU422(U LSB) 1'b1: VYUY422(Y LSB)
3:0	RW	0x0	sw_src_fmt Source bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 4'b0111: YVYU422(U LSB) 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P 4'b1100: 1BPP (color palette) 4'b1101: 2BPP (color palette) 4'b1110: 4BPP (color palette) 4'b1111: 8BPP (color palette)

RGA2_SRC_BASE0
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 Source image Y/RGB base address

RGA2_SRC_BASE1
Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 Source image Cb base address (YUV422/420-P) Source image Cb/Cr base address (YU,V422/420-SP)

RGA2_SRC_BASE2
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base2 Source image Cr base address (YUV422/420-P)

RGA2_SRC_BASE3
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base3 Source image 1 RGB base address(source bitblt mode1)

RGA2_SRC_VIR_INFO
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_mask_vir_stride Mask image virtual stride (words)
15	RO	0x0	reserved
14:0	RW	0x0000	sw_src_vir_stride SRC image virtual stride (words)

RGA2_SRC_ACT_INFO
Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_src_act_height Source image active height
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_src_act_width Source image active width

RGA2_SRC_X_FACTOR
Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor =((SRC_ACT_WIDTH-1)/(DST_ACT_WIDTH-1)) * 65536
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor =(DST_ACT_WIDTH/(SRC_ACT_WIDTH) * 65536 + 1

RGA2_SRC_Y_FACTOR
Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor =((SRC_ACT_ HEIGHT -1)/(DST_ACT_ HEIGHT -1)) * 65536
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor =(DST_ACT_ HEIGHT /(SRC_ACT_ HEIGHT) * 65536 + 1

RGA2_SRC_BG_COLOR
Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA2_SRC_FG_COLOR
Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA2_SRC_TR_COLOR0
Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin Source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin Source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin Source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin Source image transparency color R min value

RGA2_CP_GR_A
Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA2_SRC_TR_COLOR1
Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax Source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax Source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax Source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax Source image transparency color R max value

RGA2_CP_GR_B

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA2_DST_INFO

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	sw_dst_nn_quantize_en Destination output RGB quantize calculate 1'b0: Quantize calculate disable 1'b1: Quantize calculate enable
25	RW	0x0	sw_dst_fmt_y4_en Destination output Y channel 4bit and UV 0bit 1'b0: Y4 out disable 1'b1: Y4 out enable
24	RW	0x0	sw_dst_fmt_yuv400_en Destination Cb-Cr output disable (valid for YUV420/2 P/SP format) 1'b0: CbCr output normal 1'b1: CbCr output disable
23	RO	0x0	reserved
22	RW	0x0	sw_src1_csc_clip Src1 read BGR2YUV Clip mode(RGB from 0~255 clip to 36~235) 1'b0: Clip disable 1'b1: Clip enable
21:20	RW	0x0	sw_src1_csc_mode SRC1 read bitmap RGB2YUV conversion mode 2'b00: Bypass 2'b01: BT.601-range0,BT601_l, Y{00,255}, UV{00,255} 2'b10: BT.601-range1,BT601_f, Y{16,235}, UV{19,237} 2'b11: BT.709-range0,BT709_l, Y{16,255}, UV{16,237}
19	RW	0x0	sw_dst_csc_mode_2 sw_dst_csc_mode[2]+sw_dst_csc_mode[1:0]; DST read bitmap CSC(r2y/y2y) conversion mode under sw_dst_csc_mode[2]=1'b0: 3'b10x: Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0 U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1 V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2 without clip 3'b110: BT.709-range1,BT601_f,Y{16,235},UV{16,240} clip 3'b111: BT.709-range1,BT601_f,Y{16,235},UV{16,237} clip
18	RW	0x0	sw_dst_csc_clip Dst write RGB2YUV Clip mode(RGB from 0~255 clip to 16~235) 1'b1: Clip enable 1'b0: Clip disable

Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_dst_csc_mode_01 sw_dst_csc_mode[1:0] under sw_dst_csc_mode[2]=1'b0: DST read bitmap RGB2YUV conversion mode 3'b000: Bypass 3'b001: BT.601-range0,BT601_l,Y{00,255},UV{00,255} 3'b010: BT.601-range1,BT601_f,Y{16,235},UV{19,237} 3'b011: BT.709-range0,BT709_l,Y{16,255},UV{16,237}
15:14	RW	0x0	sw_dither_mode DST dither down bit mode 2'b00: 888 to 666 2'b01: 888 to 565 2'b10: 888 to 555 2'b11: 888 to 444 DST YUV dither down bit mode 2'b00: Y8 to Y4 others:Y8 to Y1
13	RW	0x0	sw_dither_down DST dither down enable 1'b0: Disable 1'b1: Enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 1'b0: BGR 1'b1: RGB
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 3'b000: ABGR888 3'b001: XBGR888 3'b010: BGR packed 3'b100: RGB565 3'b101: ARGB1555 3'b110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 1'b0: CrCb 1'b1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 1'b0: BGR 1'b1: RGB

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 when sw_dst_fmt_yuv400_en=1, YUV420/2 P/SP format will change to YUV400: 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P only RGA2E has yuyv output format feature: 4'b1100: YVYU422(U, LSB) 4'b1101: YVYU420(U, LSB) 4'b1110: VYUY422(Y, LSB) 4'b1111: VYUY420(Y, LSB)

RGA2_DST_BASE0
Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 Destination image Y/RGB base address

RGA2_DST_BASE1
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 Destination image Cb/CbCr base address

RGA2_DST_BASE2
Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 Destination image Cr base address

RGA2_DST_VIR_INFO
Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_src1_vir_stride Source image 1 virtual stride (words)
15	RO	0x0	reserved
14:0	RW	0x0000	sw_dst_vir_stride Destination image virtual stride(words)

RGA2_DST_ACT_INFO
Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA2_ALPHA_CTRL0

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved Reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 1'b0: Big endian 1'b1: Little endian
19:12	RW	0x00	sw_dst_global_alpha Global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha Global alpha value of SRC(Ags) Fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 2'b00: ROP 2 2'b01: ROP 3 2'b10: ROP 4
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 1'b0: Alpha 1'b1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 1'b0: Disable 1'b1: Enable

RGA2_ALPHA_CTRL1

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 SRC Transparent/opaque of alpha channel (As1) 1'b0: As 1'b1: 255-As
28	RW	0x0	sw_dst_alpha_m1 DST Transparent/opaque of alpha channel (Ad1) 1'b0: Ad 1'b1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha SRC blend mode select of alpha channel (As1_) 2'b00: Ags 2'b01: As1 2'b10: (As1*Ags)>>8 2'b11: reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	sw_dst_blend_m1 Alpha DST blend mode select of alpha channel(Ad1_) 2'b00: Agd 2'b01: Ad1 2'b10: (Ad1*Agd)>>8 2'b11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha SRC calculate mode of alpha channel(As1) 1'b0: As1= As1_ + (As1_ >>7) 1'b1: As1= As1 _
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha DST calculate mode of alpha channel(Ad1) 1'b0: Ad1= Ad1_ + (Ad1_ >>7) 1'b1: Ad1= Ad1_
21:19	RW	0x0	w_src_factor_m1 SRC factormode of alpha channel(Fs1) 3'b000: 0 3'b001: 256 3'b010: Ad1 3'b011: 256-Ad1 3'b100: As1
18:16	RW	0x0	sw_dst_factor_m1 DST factormode of alpha channel(Fd1) 3'b000: 0 3'b001: 256 3'b010: As1 3'b011: 256-As1 3'b100: Ad1
15	RW	0x0	sw_src_alpha_m0 SRC Transparent/opaque of color channel (As0) 1'b0: As 1'b1: 255-As
14	RW	0x0	sw_dst_alpha_m0 DST Transparent/opaque of color channel (Ad0) 1'b0: Ad 1'b1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha SRC blend mode select of color channel (As0_) 2'b00: Ags 2'b01: As0 2'b10: (As0*Ags)>>8 2'b11: Reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha DST blend mode select of color channel(Ad0_) 2'b00: Agd 2'b01: Ad0 2'b10: (Ad0*Agd)>>8 2'b11: Reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha src calculate mode of color channel(As0) 1'b0: As0= As0_ + (As0_ >>7) 1'b1: As0= As0 _

Bit	Attr	Reset Value	Description
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha dst calculate mode of color channel(Ad0) 1'b0: Ad0= Ad0_ + (Ad0_ >>7) 1'b1: Ad0= Ad0_
7:5	RW	0x0	sw_src_factor_m0 Src factormode of color channel(Fs0) 3'b000: 0 3'b001: 256 3'b010: Ad0 3'b011: 256-Ad0 3'b100: As0
4:2	RW	0x0	sw_dst_factor_m0 Dst factor mode of color channel(Fd0) 3'b000: 0 3'b001: 256 3'b010: As0 3'b011: 256-As0 3'b100: Ad0
1	RW	0x0	sw_src_color_m0 SRC color select(Cs) 1'b0: Cs 1'b1: Cs * As0
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd) 1'b0: Cd 1'b1: Cd * Ad0

RGA2_FADING_CTRL
Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA2_PAT_CON
Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA2_ROP_CON0

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x0000000	sw_rop3_code0 Rop3 code 0 control bits

RGA2_CP_GR_G
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA2_DST_Y4MAP_LUT0
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x76543210	sw_dst_y4map_lut0 Y4 lut from lut0 to lut7

RGA2_NN_QUANTIZE_SCALE
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_nn_quantize_scale_b Quantize scale of Blue (2bit integer+8bit fraction, 0--3.99)
19:10	RW	0x000	sw_nn_quantize_scale_g Quantize scale of Green (2bit integer+8bit fraction, 0--3.99)
9:0	RW	0x000	sw_nn_quantize_scale_r Quantize scale of Red (2bit integer+8bit fraction, 0--3.99)

RGA2_NN_QUANTIZE_OFFSET
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	sw_nn_quantize_offset_b Quantize offset of Blue(1bit signed + 8bit integer)
19	RO	0x0	reserved
18:10	RW	0x000	sw_nn_quantize_offset_g Quantize offset of Green (1bit signed + 8bit integer)
9	RO	0x0	reserved
8:0	RW	0x000	sw_nn_quantize_offset_r Quantize offset of Red(1bit signed + 8bit integer)

RGA2_CP_GR_R
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0x0000	sw_gradient_x_r X gradient value of Red(signed 8.8)

RGA2_DST_Y4MAP_LUT1
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0xfedcba98	sw_dst_y4map_lut1 Y4 lut from lut8 to lut15

RGA2_ROP_CON1

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x0000000	sw_rop3_code1 Rop3 code 1 control bits

RGA2_MASK_BASE

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base Mask base address in ROP4 mode. LUT/ pattern load base address

RGA2_MMU_CTRL1

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_els_mmu_flush RGA ELSE channel MMU TLB flush. Set 1 to this bit to flush MMU TLB, and auto clear.
12	RW	0x0	sw_els_mmu_en RGA ELSE channel MMU enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	sw_dst_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
10	RW	0x0	sw_dst_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	sw_dst_mmu_flush RGA DST channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
8	RW	0x0	sw_dst_mmu_en RGA DST channel MMU enable 1'b0: Disable 1'b1: Enable
7	RW	0x0	sw_src1_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
6	RW	0x0	sw_src1_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	sw_src1_mmu_flush RGA SRC1 channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
4	RW	0x0	sw_src1_mmu_en RGA SRC1 channel MMU enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
3	RW	0x0	sw_src_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
2	RW	0x0	sw_src_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	sw_src_mmu_flush RGA SRC channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
0	RW	0x0	sw_src_mmu_en RGA SRC channel MMU enable 1'b0: Disable 1'b1: Enable

RGA2_MMU_SRC_BASE
Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src_base RGA source MMU TLB base address

RGA2_MMU_SRC1_BASE
Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src1_base RGA source1 MMU TLB base address

RGA2_MMU_DST_BASE
Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_dst_base RGA destination MMU TLB base address

RGA2_MMU_ELS_BASE
Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_els_base RGA destination MMU TLB base address

6.5 Application Notes

6.5.1 Register Partition

There are two types of register in RGA. The first part registers (0x0 - 0xFC) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

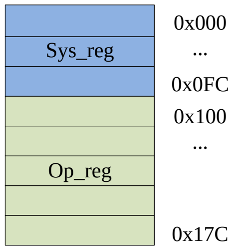


Fig. 6-7 RGA software main register-region

6.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[1] = 1’b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[0] to 1. In master mode (RGA_SYS_CTRL[1] = 1’b1), 2D graphic commands could be run sequentially. After setting command’s number to RGA_CMD_CTRL[12:3], writing 1 to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write 1 to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1’b1).

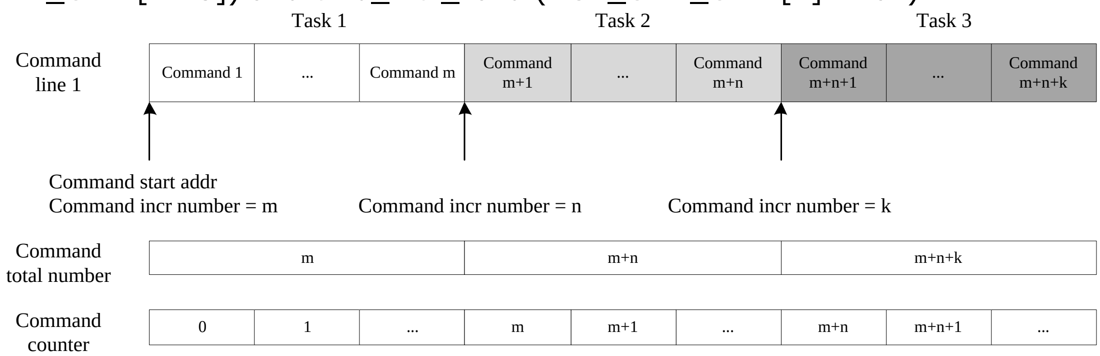


Fig. 6-8 RGA command line and command counter

6.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.
In master command mode, user can enable the current_cmd_int (sw_intr_cf), command by command to generate a interrupt at the end point of target command operation.

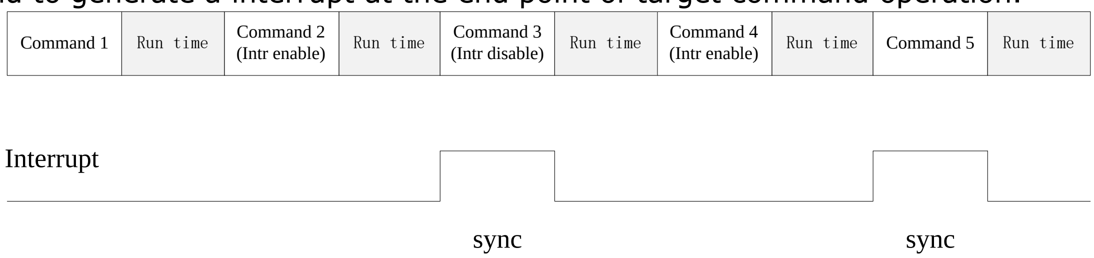


Fig. 6-9 RGA command sync generation

6.5.4 Color Palette Application Notes

1. Palette/LUT Load into special RAM in ELS_BUF_CTRL.
2. Color Palette/Pattern interval operations no need to initial LUT/pattern ram if LUT/pattern content no update.

6.5.5 Some Special Application Constraints

1. The algorithm of vertical scale up: must select BI-cubic algorithm when source picture is smaller or equal to 2k and must select BI-linear when bigger than 2k.

2. The effects that The output’s definition is near 2k or 4k may not very well when at the scenario that the vertical side is scale up and the horizontal is scale down within range of

2%(such as:2048x32→2008x64).

3. At the scenario A+B->C(A means SRC0, B means DST, C means SRC1), the size among the A B C has some constraints:
A’s size after scale must be equal to C. C’s size must equal to B when A+C is no rotation. C’s rotation (90degree)size must equal to B1 when A+C is rotation 90 degree.

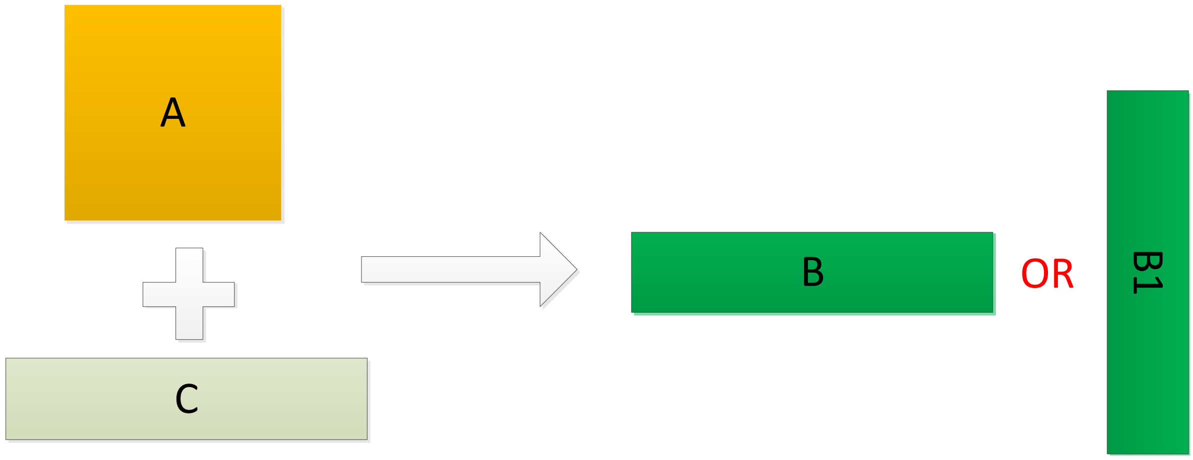


Fig. 6-10 The size constraint among A B C

Chapter 7 Video Output Processor (VOP)

7.1 Overview

The VOP (video output process) module is a display output processor. It reads video data and UI data from the frame buffer of the system memory, performs corresponding processing such as cropping, color gamut space conversion, scaling, and superposition, and outputs to each high-speed via video port display interface.

VOP2 supports the following features:

- Display Output Interface
  - Two DP Interface
    - Max support 7680x4320@30Hz
    - Support RGB/YUV444/YUV422/YUV420 (up to 10bit) format
    - Support Display Split
  - Two HDMI / eDP Combo Interface
    - HDMI
      - Max resolution support 7680x4320@60Hz
      - Support RGB/YUV444/YUV420 (up to 10bit) format
      - VESA DSC 1.2a
      - Support Display Split
    - eDP
      - Max resolution support 4096x2304@60Hz
      - Support RGB/YUV422 (up to 10bit) format
      - Support Display Split
  - Two MIPI DSI2 Interface
    - Max resolution support 4096x2304@60Hz
    - Support RGB (up to 10bit) format
    - Support Dual Channel: Left-Right display mode.
    - VESA DSC 1.1/1.2a
  - Parallel Interface
    - BT656
      - support PAL and NTSC
      - Support RGB (up to 8bit) format
    - BT1120
      - Max resolution support 1920x1080@60Hz
      - Support RGB (up to 8bit) format
- Bus
  - One 32bit AHB Slave to configure registers
  - Two 128bit AXI read bus
  - One 128bit AXI write bus
- Video Ports
  - Video Port0
    - Resolution
      - Max output resolution: 7680x4320@60Hz
      - Bits per component: 10
    - Color bar
      - Horizontal mode
      - Vertical mode
    - BCSH(10bit)
      - Brightness(8bit), Contrast(9bit), Saturation(10bit), Hue adjustment(9bit)
    - 3D_LUT
      - Support 9x9x9(12bit) LUT
    - CSC
      - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
      - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
    - Gamma
    - Dither down

    - Allegro
    - FRC
  - Post LB mode
    - 4096pixels x 4 mode
    - 2048pixels x 8 mode
  - Display mode
    - P2I/Interlace display
    - Blank display
    - Black display
    - Standby mode
- Video Port1
  - Resolution
    - Max output resolution: 4096x4320@60Hz
    - Bits per component: 10
  - Color bar
    - Horizontal mode
    - Vertical mode
  - BCSH(10bit)
    - Brightness(6bit), Contrast(9bit), Saturation(10bit), Hue adjustment(9bit)
  - 3D_LUT
    - Support 9x9x9(12bit) LUT
  - CSC
    - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
    - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
  - Gamma
  - Dither down
    - Allegro
    - FRC
  - Post LB mode
    - 2048pixel x 4 mode
    - 1024pixel x 8 mode
  - Display mode
    - P2I/Interlace display
    - X-mirror
    - Blank display
    - Black display
    - Standby mode
- Video Port2
  - Resolution
    - Max output resolution: 4096x4320@60Hz
    - Bits per component: 10
  - Color bar
    - Horizontal mode
    - Vertical mode
  - BCSH(10bit)
    - Brightness(6bit), Contrast(9bit), Saturation(10bit), Hue adjustment(9bit)
  - 3D_LUT
    - Support 17x17x17(12bit) LUT
  - CSC
    - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
    - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
  - Gamma
  - Dither down
    - Allegro
    - FRC
  - Post LB mode
    - 2048pixelx4 mode

- 1024pixelx8 mode
- Display mode
  - P2I/Interlace display
  - Blank display
  - Black display
  - Standby mode
- Video Port3
  - Resolution
    - Max output resolution: 2048x1080@60Hz
    - Bits per component: 8
  - Color bar
    - Horizontal mode
    - Vertical mode
  - BCSH(8bit)
    - Brightness(6bit), Contrast(9bit), Saturation(10bit), Hue adjustment(9bit)
  - CSC
    - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
    - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
  - Gamma
  - Dither down
    - Allegro
    - FRC
  - Post LB mode
    - 1024pixel x 4 mode
    - 512pixel x 8 mode
  - Display mode
    - P2I/Interlace display
    - Blank display
    - Black display
    - Standby mode
- Cluster 0/1/2/3
  - Resolution
    - Max resolution:
      - Two Cluster Merge :7680x4320
      - Single Cluster: 4096x4320
  - Data format
    - AFBCD: RGBA8888/RGB888/RGB565/RGBA1010102/
      YUV420 (8,10bit)/YUV422 (8,10bit)
    - Line: RGBA8888/RGB888/RGB565
    - Tile8x8：YUV420 (8,10bit)/YUV422 (8,10bit)/YUV444 (8,10bit)
  - Image
    - Support virtual width (max 8K word)
    - Support active offset
    - Support display offset
    - Support Y-mirror/X-mirror/rotation-90/rotation-270
      - If rotation-90 or rotation-270 is enable, the maximum height of the source image is 2048
    - Swap: alpha/RB/UV swap
    - Support YUV clip
  - Cluster Line Buff Mode
    - Mode0: 1 x 4096 width layer mode
    - Mode1: 2 x 2048 width layer mode
    - Mode2: 1 x 2048 width AFBCD rotation layer mode
  - Support Gauss filter
  - Scale
    - Scale down
      - Support scale rate 1/4~1

- Scale mode: bilinear
- Scale up
  - Support scale rate 1~4
  - Scale mode: bilinear
- CSC
  - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
  - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
- Esmart 0/1/2/3
  - Resolution
    - Two Esmart merge :7680x4320
    - Single Esmart: 4096x4320
  - Data format
    - RGB: ARGB8888/RGB888/RGB565
    - YUV: YUV420/YUV422/YUV444 8bit/10bit
    - YUYV: YUYV422/420; UYVY420/422
    - BPP: 8BPP
  - Image
    - Support virtual width (max 8k word)
    - Support active offset
    - Support display offset
    - Support Y-mirror
    - Swap: alpha/RB/UV swap
    - Support YUV clip
  - Multi-region
    - Only one region at one line
    - All regions are RGB or YUV format
    - Up to 4 regions
  - Scale
    - Scale down
      - Support scale rate 1/8~1
      - Scale mode: nearest/bilinear/average
    - Scale up
      - Support scale rate 1~8
      - Scale mode: nearest/bilinear/bicubic
  - CSC
    - YUV2RGB: bt601-f/bt709-l/bt601-l/bt2020
    - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
- Overlay
  - Support MAX 8 layers overlay: 4 Cluster / 4 Esmart
  - Support RGB/YUV domain overlay
  - Support layers mux
  - Support per-pixel/global alpha
  - Support HDR10
    - Support HDR2SDR
    - Support SDR2HDR
- Write Back
  Format: ARGB8888/RGB888/RGB565/YUV420
  Max resolution: 1920x1080
- Interrupt
  - Vop_intr
    - System interrupt
      - AXI0 bus error
      - AXI0 dma finish
      - Write back YRGB FIFO overflow
      - Write back dma finish
      - MMU0 interrupt
      - System1 interrupt

- AXI1 bus error
- AXI1 dma finish
- MMU1 interrupt

◆ Video port0/1/2 interrupt

- Frame start interrupt
- Line flag0 interrupt
- Line flag1 interrupt
- Post empty interrupt
- Field start interrupt
- Display hold interrupt
- Video front porch interrupt
- Post almost full interrupt

◆ AFBCD interrupt

- Cluster0 decode error interrupt
- Cluster0 AXI response error interrupt
- Cluster1 decode error interrupt
- Cluster1 AXI response error interrupt
- Cluster2 decode error interrupt
- Cluster2 AXI response error interrupt
- Cluster3 decode error interrupt
- Cluster3 AXI response error interrupt

■ Vop_intr_ddr

◆ Vop_dma_finish

■ Vop_intr_lb

◆ Video port0 post almost full
◆ Video port1 post almost full
◆ Video port2 post almost full
◆ Video port3 post almost full

- Power gating: Independent power domains for cluster layer 0/1/2/3, esmart layer 1/2/3, DSC 8K/4K encoder

7.2 Block Diagram

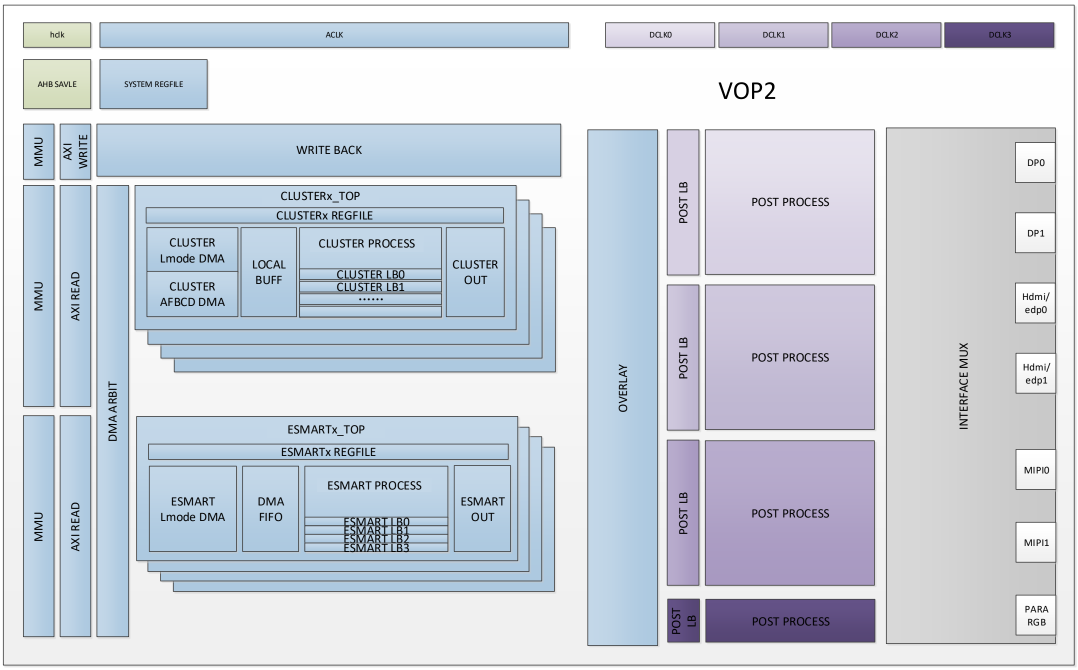


Fig. 7-1 VOP Block Diagram

VOP comprises with:

- AHB SLAVE

The VOP configuration bus is used to read and write all register configurations of the VOP. Some of the address segments are secure SLAVE address segments, which can only be accessed by a secure CPU when the security is enabled. For details, please refer to the security program description chapter.

- SYSTEM REGFILE

The register arrays, including system control, layer, overlay, and post process registers, are all in the ACLK domain, and read and write from HCLK to the ACLK domain through synchronization logic.

- MMU

The Memory Management Unit maps the configured virtual address to the physical address through the page table. Since there are two buses in the system, there are two MMU addresses. In the security mode, the address of the security layer is configured as a physical address from the MMU according to the configuration. The module is bypassed, so as to avoid the address being rewritten when the MMU is mapped.

- AXI READ/WRITE

There are AXI0 and AXI1 bus in VOP interface. The AXI0 supports both write and read channel, while AXI1 only supports read channel.

- DMA ARBITER

Each layer in the system will initiate a different read request, and DMA arbiter will perform a global arbitration for internal requests based on priority settings and FIFO status.

- CLUSTERx

Cluster layer, which supports AFBCD、line mode and tile mode.

- ESMARTx

Esmart layer only supports line mode and support display up to 4 regions where the regions can’t overlap horizontally.

- OVERLAY

Perform the synthesis operation between layers according to the configuration and send it to the corresponding post process modules.

- POST PROCESS

Including gamma, BCSH, 3D-LUT and other post-processing modules, the data is processed by the post-processing module and then store them into the POST line buffer.

- POST LINE BUFFER

The Post Process line buffer is used to store the data processed by the post process modules and output to corresponding display interface.

- INTERFACE MUX

The VOP supports variety of output interface including HDMI, eDP, DP, MIPI DSI2, BT.1120, BT 656. By setting the interface mux module, the corresponding PORT can be selected and output to the corresponding interface.

7.3 Operating Mode

7.3.1 Clock and Reset Description

- **HCLK**

The maximum operating frequency: 200MHz

- **ACLK**

The maximum operating frequency: 800MHz

- **DCLK0/1/2/3**

The maximum operating frequency of DCLK0/1/2: 600MHz
The maximum operating frequency of DCLK3: 200MHz

- **Hardware Reset**

System hardware reset, that is, the hardware reset of the entire VOP through the system, all the logic inside the VOP will enter the initial state, if the current screen is being displayed, there will be abnormal phenomena such as a black screen.

- **Software Frame Reset**

The frame reset of each layer is supported, that is, when the vsync signal of each frame arrives, the layer's internal logic will be reset exclude register logic.

- **MMU Frame Reset**

Support the MMU soft reset, when the MMU is abnormal, the entire MMU logic can be reset without causing the MMU to hang up.

7.3.2 Bus Description

- **AHB Bus**

Configuration bus for register/LUT

- **AXI 0 Bus**

The AXI0 bus is readable and writable, which supports write back function. In the system design, the bus performance of AXI0 is better than the AXI1, so AXI0 is used first in the bus allocation, and AXI1 is configured when the total VOP loading is heavy. In order to maintain synchronization between layers, allocating the layers used by the one port on the AXI0 and AXI1 buses respectively is not allowed.

- **AXI 1 Bus**

Read-only data bus

- **RID Default Configuration**

There are 15 IDs available for each bus. For YUV and AFBCD, two IDs are required for each layer. The driver allocates the rid according to the data of the layer on the bus. If it exceeds 15, another bus is required to be enabled.

- **Hurry/QoS**

VOP2 hurry has an enable bit and hurry value. Initiating a hurry request depends on whether the memory of the layer initiates a hurry request. When the layer's esmart_dma_rreq_hurry_en is enabled and the number of empty memory is greater than the set waterline, a hurry request is initiated.
VOP2 QoS has an enable bit in SYS_CTRL_SYS_AXI_HURRY_CTRL0_IMD. When QoS is enabled and rid is greater than or equal to 0xa, QoS signal is asserted.

- **MMU Frame Valid Mechanism**

MMU supports the bypass function in register mmu_bypass_en and mmu_bypass_id. When rid>=mmu_bypass_id, the AXI request and the returned data will bypass MMU. Noted that mmu_bypass_en and mmu_bypass_id is enabled immediately. At that time, rid is effective frame for the layer, so it can realize whether the layer data access is mmu_bypass.

- **Protection Mechanism**

In the protection mode, the port number of the protected layer can be set and sent to the designated protected port, otherwise the layer will be forcibly closed.

7.3.3 Display Output Interface Description

The following figure shows the interface connection diagram of VOP2. There are 4 ports in the VOP to distribute video data to different high-speed interfaces through the software setting interface MUX.

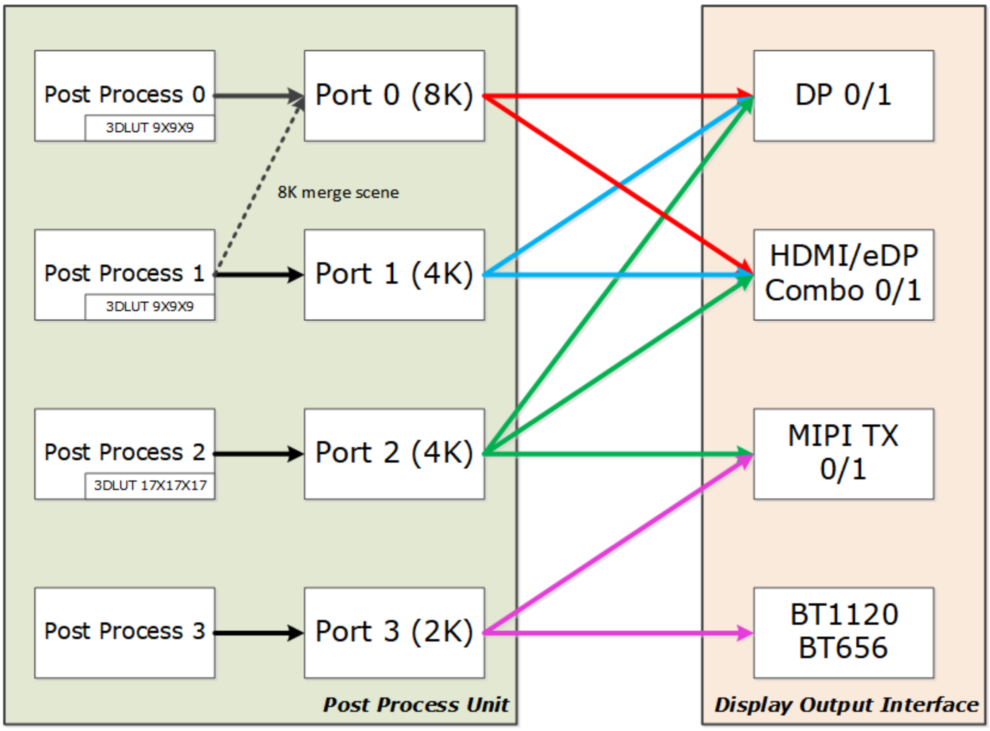


Fig. 7-2 Schematic Diagram of Display Output Interface

- HDMI/eDP Combo Interface 0/1
  - The data source of the HDMI/eDP Combo interface can come from port 0 or port 1 or port 2.
  - Maximum resolution support:
    - HDMI: 7680x4320@60 (VIC 199 using YUV420 format) supported by merged function of PORT0 and PORT1
    - eDP: 4096x2304@60 supported by single port
  - In system, HDMI TX interface and eDP interface share the one Combo PHY, which means VOP can only work in HDMI or eDP mode. There are two HDMI/eDP Combo PHYs in SoC, so application has the four scenes:
    (1) HDMI0 + HDMI1
    (2) HDMI0 + eDP1
    (3) eDP0 + HDMI1
    (4) eDP0 + eDP1.
  - Split mode: The one frame is split to left-right part which send to HDMI/eDP TX 0/1 respectively.

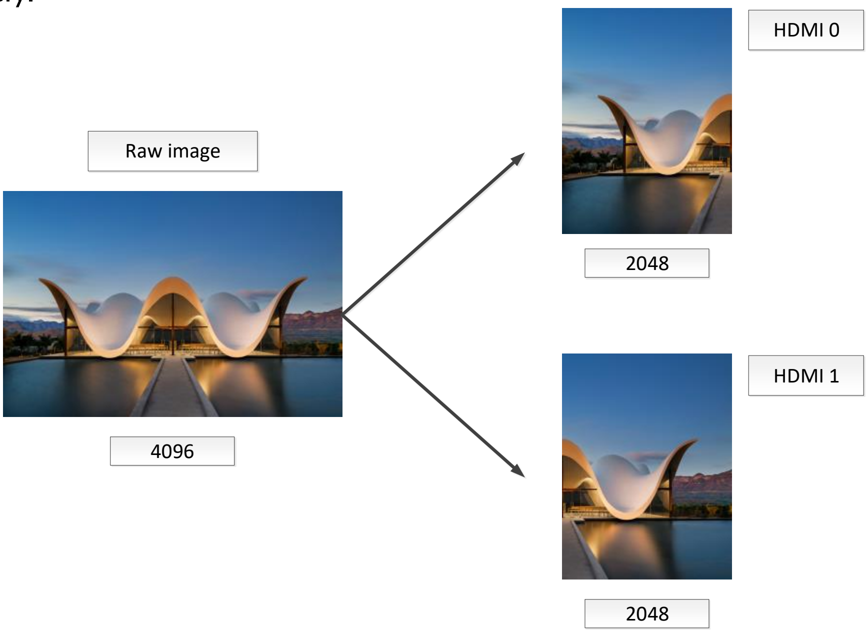


Fig. 7-3 Split (Left-Right) Display Mode

- DP Interface 0/1
  - The data source of the DP interface can come from port 0 or port 1 or port 2
  - The maximum supported resolution (limited by the DP TX PHY's maximum available bandwidth-25.92Gbps):
    7680x4320@30: supported by merged function of port 0 and port 1
    4096x2304@60: supported by port 0 or port 1 or port 2
  - Split mode: The one frame is split to left-right part which send to DP TX 0/1 respectively.
  - The DSC function is not supported.

- MIPI TX DSI2 Interface 0/1
  - The maximum resolution supports 4096x2304@60
  - The data source of the MIPI TX interface can come from port 2 (up 4096 pixel's image width) or port 3 (up 2048 pixel's image width).
  - Support operation mode:
    Copy: The MIPI TX 0 and MIPI TX 1 are driven from the same output port.
    Dual channel: The one frame is split to left-right part which send to MIPI TX 0/1 respectively.

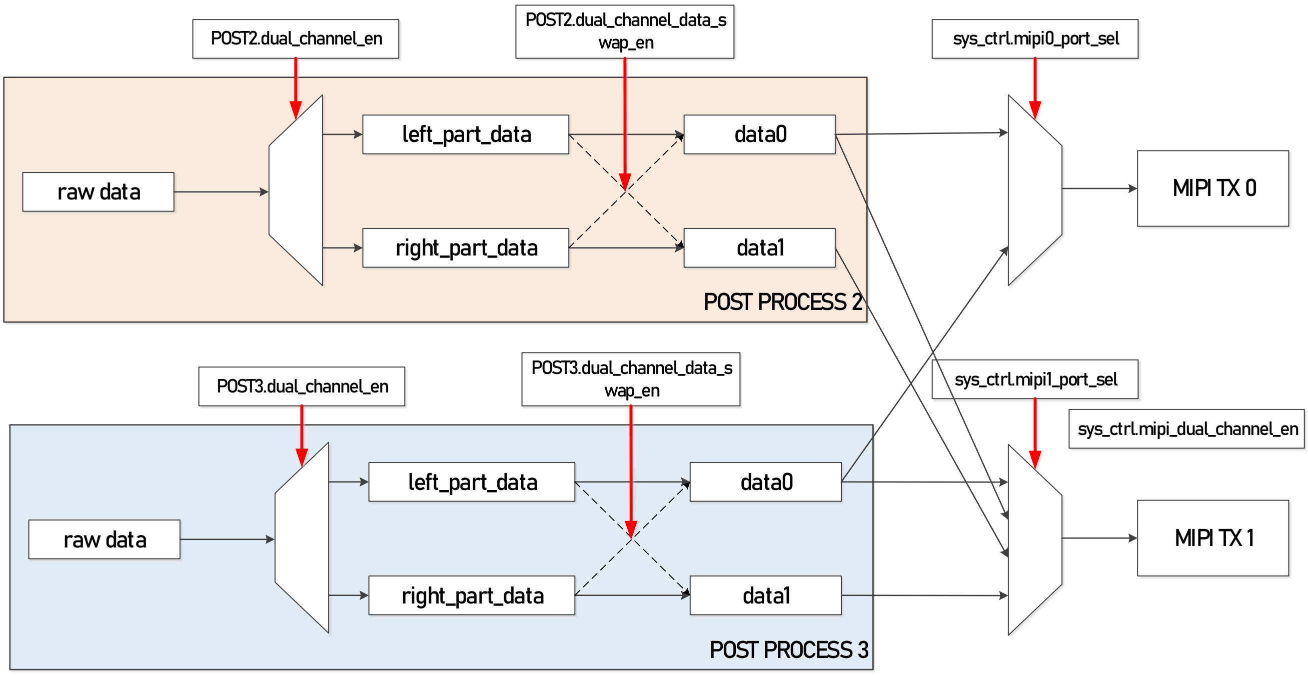


Fig. 7-4 MIPI dual channel display mode

- Support DSC:
  MIPI TX 0 is bound to DSC 8K encoder which supports up to 8 slices, which data source is bound to port 2.
  MIPI TX 1 is bound to DSC 4K encoder which supports up to 2 slices, , which data source is bound to port 1 or port3.
  The port mux of dsc function reference Fig.1-5

- BT656 / BT1120 / RGB (for debug)
  - Maximum resolution support: 1080p60, pixel rate 150M/s
  - The data source of the para interface is directly connected to port 3 (up 2048 pixel's image width).
  - The three modes share one I/O group, which contains 1-bit clock signal and 16-bit data signals.
  - The bit mapping relationship corresponding to each interface is as shown in the figure Below.

interface	RGB454(RGB)	BT656(8bit)	BT1120 (16bit)
display mode			
dsp_out_mode			
dclk	dclk	dclk	
data	data	data[7:0]	data[15:0]
d15	R7		√(D15)
d14	R6		√(D14)
d13	R5		√(D13)
d12	R4		√(D12)
d11	G7		√(D11)
d10	G6		√(D10)
d09	G5		√(D9)
d08	G4		√(D8)
d07	G3	√ (D7_m0)	√(D7)
d06	B7	√ (D6_m0)	√(D6)
d05	B6	√ (D5_m0)	√(D5)
d04	B5	√ (D4_m0)	√(D4)
d03	B4	√ (D3_m0)	√(D3)
d02	den	√ (D2_m0)	√(D2)
d01	hsync	√ (D1_m0)	√(D1)
d00	vsync	√ (D0_m0)	√(D0)

Fig. 7-5 Map of parallel port I/O output

  - The output pixel clock supports Delay-Line function which maximum adjustable range is 3~5ns.
  - support output pixel clock polarity inversion function.
  - Due to the I/O number limitation, there is only 13bit valid data output in the case of RGB mode only supports the data format of RGB454, which can be connected to the most significant 4 and most significant 5 bits to the RGB interface display panel.

Note: Though RGB454 format causes a certain color information loss, it does not affect the judgment of the image content correctness for debug purpose.

7.3.4 DSC Encoder Description

- DSC 8K encoder for HDMI TX0 / MIPI TX DSI2 Host0 interface
  - Maximum 1,2,4,8 slices per line
  - up to 8K (7680×4320) resolution
- DSC 4K encoder for HDMI TX1 / MIPI TX DSI2 Host1 interface
  - Maximum 1,2 slices per line
  - up to 4K (4096×2160) resolution
- Conformance Standard
  - VESA Display Stream Compression (DSC) Standard Version 1.2a
  - VESA Display Stream Compression (DSC) Standard Version 1.1
- Output formats
  - RGB
  - YCbCr
  - Not supported YCbCr Simple 4:2:2, Native 4:2:2, Native 4:2:0
- Coding Method
  - Constant bit rate (CBR) mode only
  - Variable bit rate mode (VBR) is not supported
- Coding Schemes
  - Modified MAP (MMAP)
  - Mid-Point Prediction (MP)
  - Block Prediction (BP)
  - Index Coloring History (ICH)
- Data Precision (maximum number of bits per component)
  - 8, 10

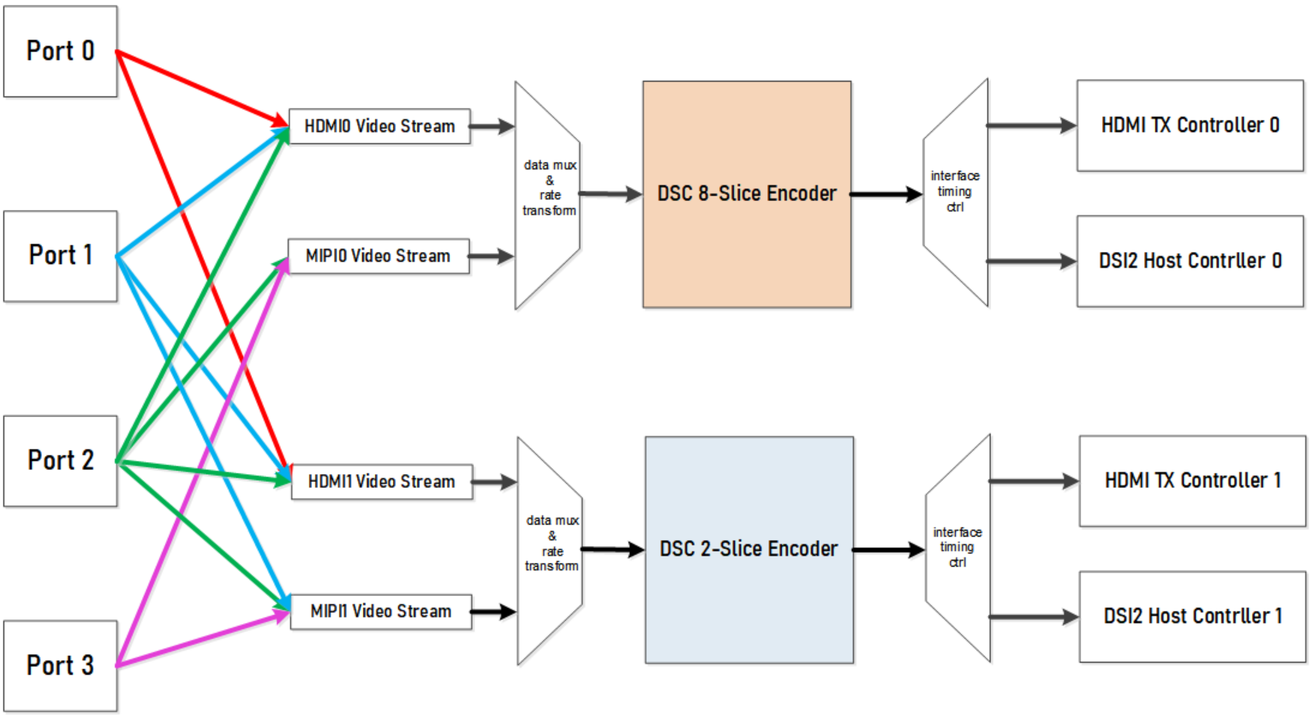


Fig. 7-6 Two DSC Encoder Architecture in VOP

The below figure shows the block diagram of a single display being split into multiple slices of equal dimensions (of equal height and width) and each slice being handled by dedicated and independent data path in DSC encoder. The pixel demultiplexer (pixel demux) separates input pixel stream based on slice dimensions. Pixel demultiplexed data are handled by different slices independently. When the input pixels are in RGB format, they are converted to YCoCg format. These pixels are reconstructed using either predicted version of the pixels or from a History lookup. Variable Length coder/Entropy Code block determines whether Prediction or Look up based reconstruction is to be used based on a cost function. Entropy code block creates separate syntax element for each sub stream corresponding to Y, Co, Cg such that syntax element contains residue values for prediction based reconstruction and look up index for History Look Up based reconstruction. Syntax element data from individual streams are written to respective balance FIFOs and size of the corresponding syntax elements are written to syntax element size FIFOs. After a specified amount of group delay time units, the sub stream multiplexer multiplexes the mux words from the sub streams based on the mux word requests from an idealized decoder model. The sub stream multiplexer outputs are written to the rate buffer. The slice multiplexer (slice mux) reads data from each of the rate buffers in units of chunk size and sends out the compressed stream.

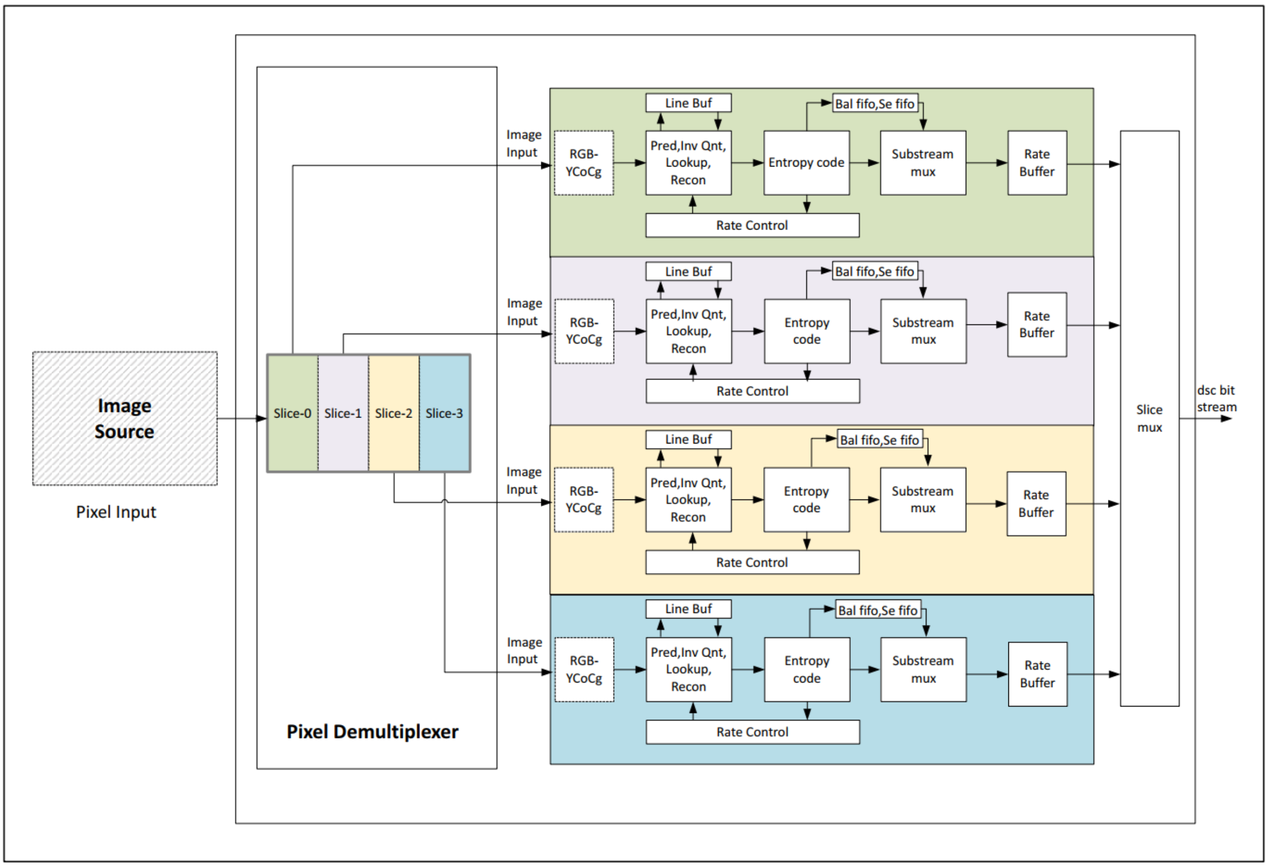


Fig. 7-7 Structure of DSC Encoder

7.3.5 Interrupt Description

There are three interrupt signals.

VOP_intr: Including the following groups of interrupt sources

- VOP_intr_sys
- VOP_intr_sys1
- VOP_intr_post
- VOP_intr_fbcd
- DSC_8K_err
- DSC_4K_err

VOP_intr_DDR: Conditional interrupt source dma_finish from DDR frequency conversion, refer to frequency conversion description for details.

VOP_intr_lb: Including the following groups of interrupt sources, which can set the buffer waterline to notify the CPU that the predetermined waterline has been reached.

- int_status_post_full0
- int_status_post_full1

- int_status_post_full2
- int_status_post_full3

7.3.6 Maximum Performance and Functional Attributes of each PORT

- PORT0
  - The maximum supported resolution in single PORT mode is 4K.
  - To support more than 4096 pixel's width, combination of PORT0 and PORT1 should be used, which the merged data stream output from PORT0.
  - Dual gamma
  - 9x9x9 3DLUT
- PORT1
  - The maximum supported resolution of single PORT mode is 4K; when it exceeds 4K, the data of the previous two channels is spliced and multiplexed to PORT0.
  - Dual gamma
  - 9x9x9 3DLUT
- PORT2
  - Only supports single PORT mode, the maximum supported resolution is 4K.
  - 600M pixel rate
  - Dual gamma
  - 17x17x17 3DLUT
- PORT3
  - Only supports single PORT mode, the maximum resolution is 2048.
  - 200M pixel rate
  - Dual gamma

7.3.7 Multi-port Configuration Instructions

The connection relationship between PORT0 and the interface is as follows.

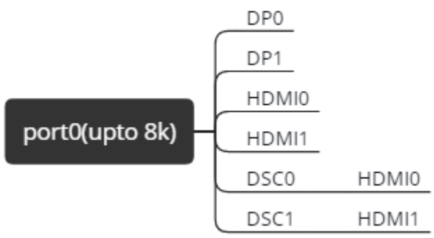


Fig. 7-8 Map of PORT0 interface

The connection relationship between PORT1 and the interface is as follows.

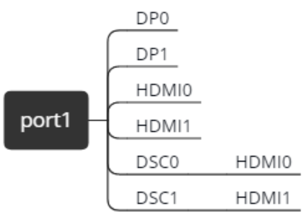


Fig. 7-9 Map of PORT1 interface

The connection relationship between PORT2 and the interface is as follows.

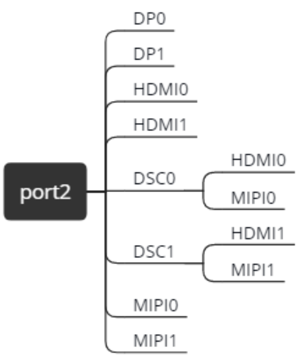


Fig. 7-10 Map of PORT2 interface

The connection relationship between PORT3 and the interface is as follows.

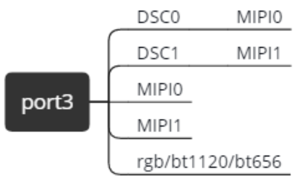


Fig. 7-11 Map of PORT3 interface

7.3.8 Power Domain Power Up/Down Description

There are seven power domains inside VOP, show as the below figures where the green border is the boundary of each power domain.

- Cluster Power Domain: Four power domains for cluster 0/1/2/3 respectively
- Esmart Power Domain: One power domain for esmart1, esmart2 and esmart3
- DSC Power Domain: Two power domains for DSC 8K encoder and DSC 4K encoder respectively

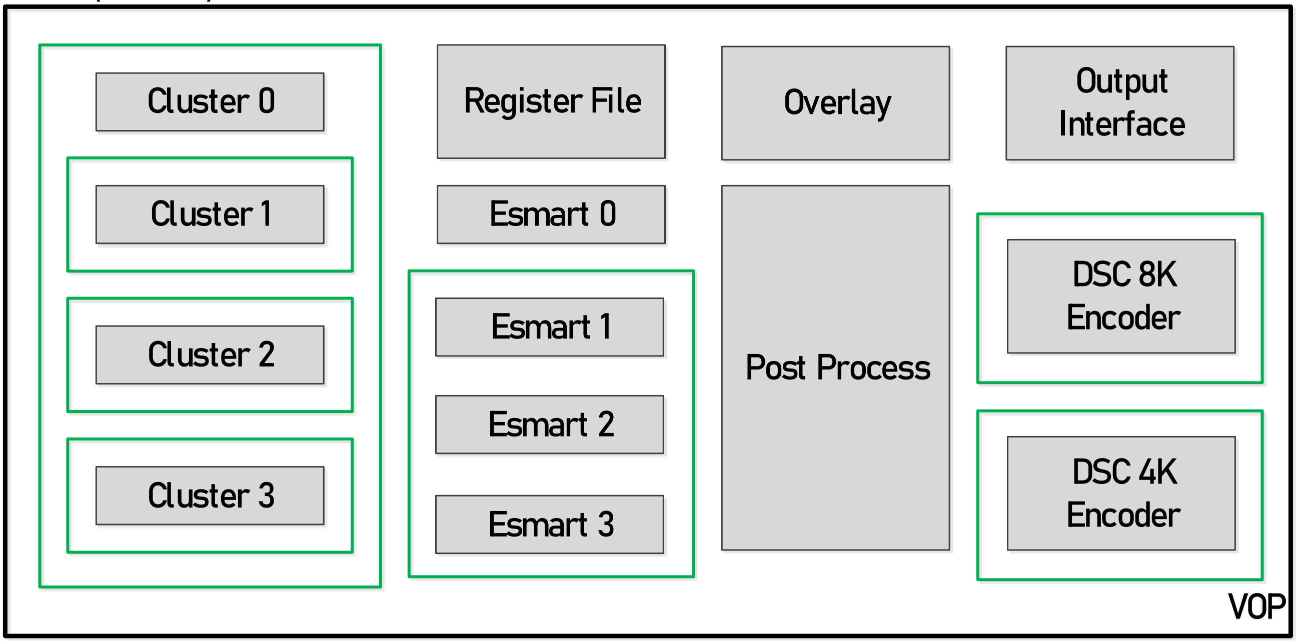


Fig. 7-12 Power Domains Structure Diagram of VOP

The cluster has 4 PDs where cluster0 PD operates as master power switch shall be powered on firstly and powered off lastly. The two DSC encoders have independent power domain. The esmart layer 1/2/3 share one power domain. It is recommended that only static switches are used according to the application scenario.

The power switching process is as follows:

- Normal display sequence:

The VOP configuration register adopts the Ping-Pong register configuration mode. The power switch configuration before the Vsync signal is completed will take effect in the next frame.

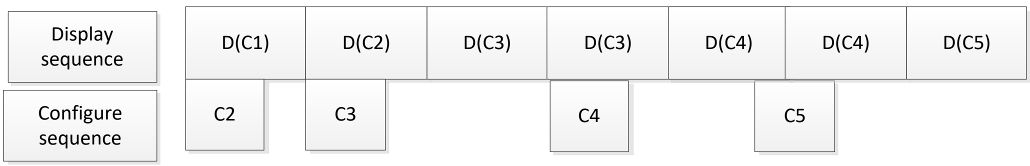


Fig. 7-13 Diagram of power domain switch configuration

Note: D(n) represents display frame; C(n) represents configure frame after the configure, it will appear after the next vsync comes.

The power status switch from power on to power off, the following steps occur inside VOP:

1. Turn off the clock

2. Enable isolation cell, clamp cell is enabled
3. Send a power off request
4. According to the feedback ack signal, the corresponding power status will be asserted

The power status switch from power off to power on, the following steps occur inside VOP:
1. Send a power on request
2. Cancel the power off request
3. After received the valid ack signal, the reset output
4. After 32 cycles, deassert clock reset
5. Recover the clock
6. Disable isolation cell
7. After a sufficient period of time, reset is released

7.3.9 Function Memory Chain Switch Description

Since the power domain cannot achieve the functional level power switch, in some application scenarios, when a memory function does not need to be dynamically turned on, the power supply of the memory chain can be turned off, which can reduce the power consumption as much as possible. It is divided into eight memory chains of WB, Post Process Module 0/1/2/3.

The register address is as follows:
- PMU_SUBMEM_PWR_GATE_SFTCON1
- PMU_SUBMEM_PWR_GATE_SFTCON2

The bit allocation of memory chain is as follows:
- #define MID_VOPPOST0 (1<<15)
- #define MID_VOPPOST1 (1<<16)
- #define MID_VOPPOST2 (1<<17)
- #define MID_VOPPOST3 (1<<18)
- #define MID_VOPWB (1<<22)

7.3.10 Security Program Description

7.3.10.1 SoC Connection Diagram

(1) The switch of the security layer and the selection of the security port controlled by register vop_sec_ctrl from the system's SGRF.

(2) Support a certain address segment (security layer address segment) of the AHB slave can be designated as a secure address on the interconnect;

(3) The bus supports MMU bypass logic according to the layer's ID.

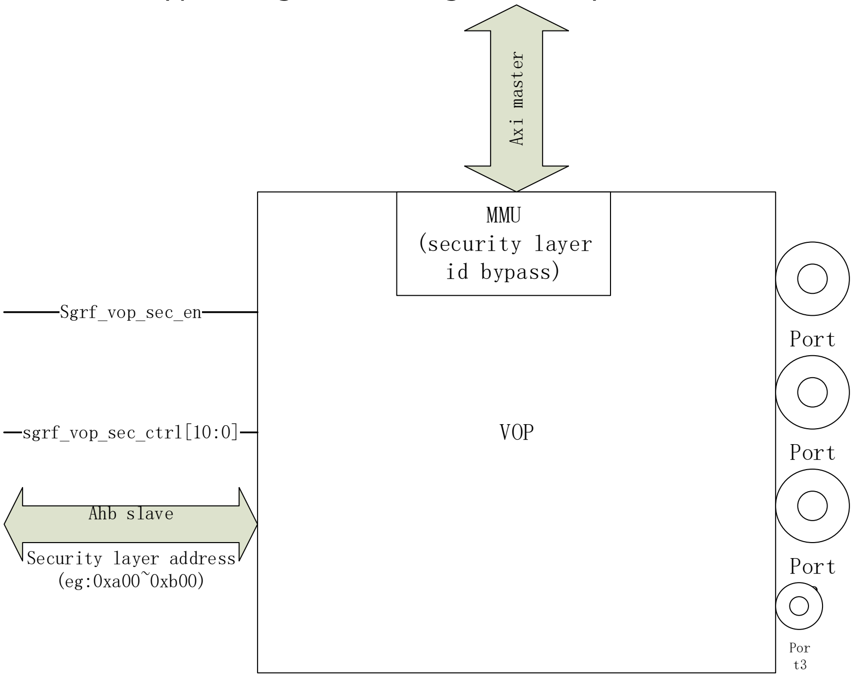


Fig. 7-14 Security schematic block diagram

7.3.10.2 Hardware Security Implementation

(1) The following points shall be guaranteed:
1) The secure layer shall only be selected to the corresponding secure PORT;
2) The secure layer shall be at the top;
3) The secure layer shall not use alpha, and directly covers the underlying layers;
4) The secure mode write back function shall be disabled;

(2) The layer address segment will not be accessed by non-secure CPU;
The address space corresponding to esmart0 is defined as a secure address, and the specific address is as follows:

0xFDD91800 ~ 0xFDD918ff

(3) MMU bypass logic ensures that the MMU page table will not be tampered with and accessed to other addresses;
vop_sec_ctrl[10:0] is added to the VOP interface, the specific description is as follows.

Table 7-1 Description of security-related registers

SGRF	bits	description
vop_sec_en	1	1'b0: non-secure mode 1'b1: secure mode
vop_sec_port	2	2'b00: video PORT0 2'b01: video PORT1 2'b10: video PORT2 2'b11: video PORT3
vop_wb_dis	1	1'b0: normal 1'b1: disable WB function
vop_post_dis	1	1'b0: normal 1'b1: disable Post process
vop_nonsec_black	1	1'b0: normal 1'b1: non-sec PORT display black
vop_sec_cfg_en	1	1'b0: disable 1'b1: enable
vop_sec_cfg	3	3'b000: Except for the secure layer, all configurations are not configurable. 3'b001: Except for layers, all configurations are not configurable 3'b010: Except for layers and overlay, all configurations are not configurable. 3'b011: Except for layer, overlay and system, all configurations are not configurable. 3'b100: Except for layer, overlay, system and post, all configurations are not configurable.
vop_drm_en	1	1. The security layer esmart0 is forced to vop_sec_port (check) 2. When secure PORT_mux=4'h8 (no layer), it is forced to be equal to 4'h1, and other PORTs are forced to have no layer, which means the value is 4'h8 3. When the non-secure PORT conflicts with the PORT_mux of the secure PORT, force the non-secure PORT mux=4'h8 (check) 4. Force the security layer to be at the top of the security PORT (check) 5. When a secure layer is selected for non-secure PORT, the layer is forcibly closed (check) 6. Alpha operation after turning off the security layer (check) 7. sys_dsp_inface_en is not configurable

7.3.10.3 Security Scene

1. Secure payment:

- esmart0 is a secure payment layer and support to specify a secure PORT. With vop_sec_en enable.
- vop_sec_port selects secure PORT;
- vop_wb_dis can disable the write-back function.
- vop_post_dis can turn off non-secure PORT.
- vop_nonsec_black can make non-secure PORT black screen.
- vop_drm_en is forcibly sent to secure layer security payment enable. The layer is placed on top of the secure PORT.
- the alpha operation of the secure layer is turned off.

2. Drm

VOP uses 0x100~0x1ff as the secure slave address segment, which is used to configure drm related operations.

- Content to layer security

support to set whether the layer is secure, and set whether to initiate secure access according to the rid.

- Content to PORT security

PORT(X) with a secure layer can be set, the secure layer can only be sent to the designated secure PORT(X), otherwise the layer will be forcibly closed.

7.3.10.4 Secure Mode Entry and Exit Process

It is recommended that driver performs the layer transfer in secure mode and normal mode.

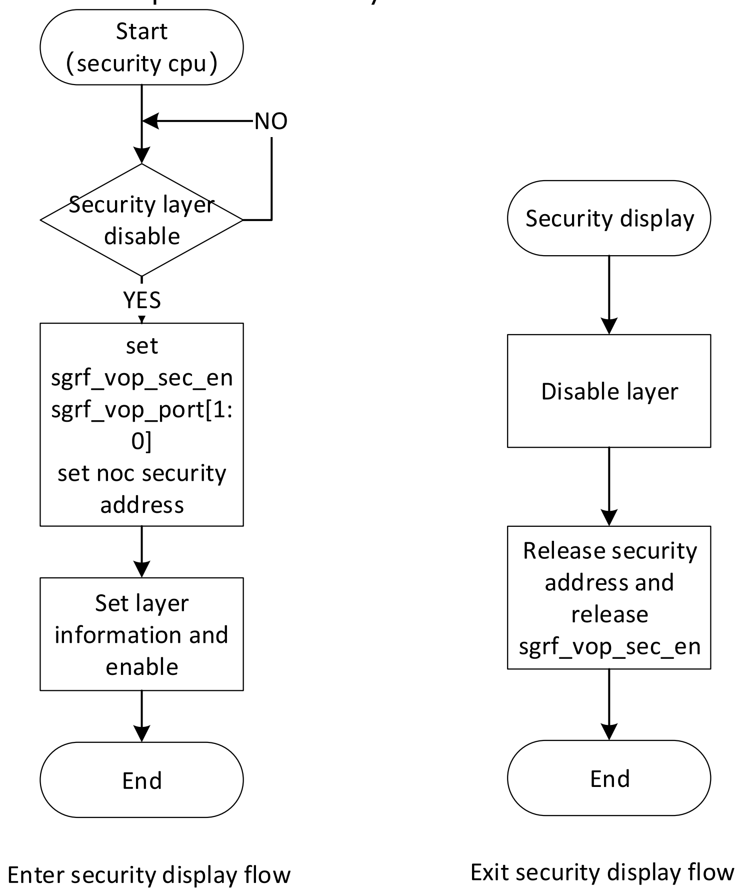


Fig. 7-15 Secure mode entry and exit diagram

7.3.11 Power Consumption Description and Recommendations

The smart layer does not have AFBCD, the logic power consumption of the layer is relatively lower, and the layer current is about 4.3MA. Because the cluster layer adds AFBCD related logic, the current of the layer is 2.2MA larger than that of smart. However, due to the addition of AFBCD, the total data volume is much smaller, and the access behavior is more friendly to DDR, and the overall power consumption of the system will be much lower. See the table below for detailed power consumption data.

Table 7-2 Data sheet for layer power consumption

Scenes	Without auto gating, current at 400MHz (mA)
Single-layer compressed data, ctrl + interconnect+ bus data toggle power consumption	12.4
Single layer uncompressed data, ctrl+ interconnect +bus data toggle power consumption	41
Total VOP cluster logic power consumption	56.1
Total VOP smart logic power consumption	54

In SoC, cluster pd, smart pd, and DSC pd are added inside the VOP. At the same time, post0/1/2/3, and wb related memorys have separate power chains.
The application recommendations are as follows:
(1) By default, all PDs are power off. Power on the cluster or smart PDs before opening the layer.
(2) Use cluster0 and smart0 firstly.
(3) In case of there are few enabled overlay layers, it is recommended that disable the useless alpha module and take the priority to subsequent pipe stage.
(4) The POST/wb blocks have the switch function of memory power chain. When it is not enabled, turn off the memory power.
(5) For simple scenes such as static desktops, it is recommended that synthesize one AFBCD layer and use cluster0 to refresh the screen.
It is not recommended to switch pd frequently, because the switch pd needs to charge and discharge the MOSFET, which can cause considerable power consumption.

7.3.12 DDR Frequency Conversion Instructions

1. dma_finish interrupt source
This interrupt is connected to DCF and DCF can handle frequency conversion.

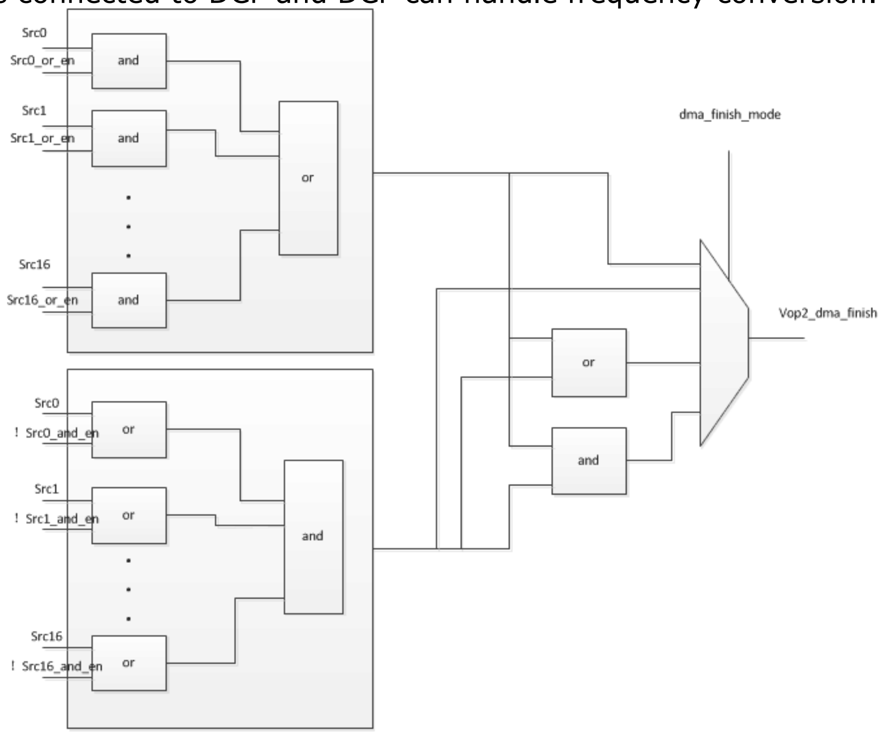


Fig. 7-16 dma finish interrupt structure diagram

The source of dma_finish is as follows, and the logic from win almost full, vp line flag, dsp hold and almost full is combined and output.

Table 7-3 dma finish interrupt source description

source list	name	remark
dma_finish	src0	AXI0_dma_finish & AXI1_dma_finish
wb_dma_finish	src1	WB DMA finish detected
vp0_line_flag	src2	When port0 line count equals the configured line flag number
vp1_line_flag	src3	When port1 line count equals the configured line flag number
vp2_line_flag	src4	When port2 line count equals the configured line flag number
vp3_line_flag	src5	When port3 line count equals the configured line flag number
vp0_dsp_hold	src6	Port0 hold status detected
vp1_dsp_hold	src7	Port1 hold status detected
vp2_dsp_hold	src8	Port2 hold status detected
vp3_dsp_hold	src9	Port3 hold status detected
vp0_almost_full	src10	When port0 post line buffer number equals dsp_almost_full_thold
vp1_almost_full	src11	When port1 post line buffer number equals dsp_almost_full_thold
vp2_almost_full	src12	When port2 post line buffer number equals dsp_almost_full_thold
vp3_almost_full	src13	When port3 post line buffer number equals dsp_almost_full_thold

2. VOP_intr_DDR
The VOP_intr_DDR signal comes from dma_finish, which is connected to the system interrupt controller through an interrupt signal, and the frequency can be converted through the interrupt, which is consistent with the DCF function.

3. VOP_intr_lb
Set the waterline of the post line buffer, and realize real-time frequency conversion through the status of line buffer, which can provide about 20us for frequency conversion.

7.4 Function Description

7.4.1 Cluster Layer

1. Basic Feature

- Support AFBCD compression mode
- Support raster line/tile mode
- Support color gamut space conversion
- Support double Gauss filter
- Support 1/4~4 times scale
- Support mirror/rotation
- Support image virtual width/cropping

7.4.1.1 Support line buffer mode description

Cluster line buffer supports the following three modes:
(1)Single window mode (mode0): In this mode, he maximum resolution supports single 4096 pixels width layer output.

(2)Two windows mode (mode1): In this mode, the cluster allows up to 2x2048 pixels width layers to be enabled and the two windows would be mixed firstly before send into overlay.

(3) AFBCD Full Mode(mode2): In this line buff mode, the cluster supports single layer rotation of 90° and 270° with AFBCD operating in full mode.

7.4.1.2 Support format description

AFBCD format:
The format needs to be written into the format register configuration related to AFBCD. There is no one-to-one correspondence between the format and the format of the layer, and the driver needs to do a mapping.
Parameter AFBCD_RGB565 =4’h0;//0000
Parameter AFBCD_RGBA1010102 =4’h2;//0010
Parameter AFBCD_RGB888 =4’h4;//0100
Parameter AFBCD_RGBA8888 =4’h5;//0101
Parameter AFBCD_YUV420_8b =4’h9;//1001
Parameter AFBCD_YUV420_10b =4’h3;//0011
Parameter AFBCD_YUV422_8b =4’hb; //1011
Parameter AFBCD_YUV422_10b =4’he;//1110

Line/tile mode format: The format is configured in the layer format register
parameter FMT_ARGB8888 = 5'b00000;
parameter FMT_RGB888 = 5'b00001;
parameter FMT_RGB565 = 5'b00010;
parameter FMT_YUV420_TILE = 5'b01100;
parameter FMT_YUV422_TILE = 5'b01101;
parameter FMT_YUV444_TILE = 5'b01110;
parameter FMT_YUV400_TILE = 5'b01111;
parameter FMT_YUV420_10B_TILE = 5'b11100;
parameter FMT_YUV422_10B_TILE = 5'b11101;
parameter FMT_YUV444_10B_TILE = 5'b11110;
parameter FMT_YUV400_10B_TILE = 5'b11111;
The following table shows the default swap configuration in various formats:

Table 7-4 The swap configuration table in the default format of the cluster

cluster					
Format		AFBCD_uv_swap	AFBCD_rb_swap	rb_swap	uv_swap
AFBCD	ARGB	0	0	0	0
	RGB888	0	0	0	0
	RGB565	0	1	0	0
	YUV444	0	1	0	0
	YUV422	1	0	0	0
	YUV420	1	0	0	0
	YUV444_10b	0	1	0	0
	YUV422_10b	1	0	0	0
	YUV420_10b	1	0	0	0
LINE	ARGB888	0	0	1	0
	RGB888	0	0	1	0
	RGB565	0	1	0	0
TILE	YUV444_TILE	0	0	0	1
	YUV422_TILE	0	0	0	1
	YUV420_TILE	0	0	0	1
	YUV400_TILE	0	0	0	0
	YUV444_TILE_10B	0	0	0	1
	YUV422_TILE_10B	0	0	0	1
	YUV420_TILE_10B	0	0	0	1
	YUV400_TILE_10B	0	0	0	0

7.4.1.3 AFBCD mode

The combinations of AFBCD define supported by VOP are as follows, divided into RGB and

YUV:
RGB format:
AFBC_SIZE_16X16
AFBC_SIZE_16X16| AFBC_CBR
AFBC_SIZE_16X16| AFBC_SPARSE
AFBC_SIZE_16X16| AFBC_CBR| AFBC_SPARSE

AFBC_SIZE_16X16| AFBC_YTR|
AFBC_SIZE_16X16| AFBC_YTR| AFBC_CBR
AFBC_SIZE_16X16| AFBC_YTR| AFBC_SPARSE
AFBC_SIZE_16X16| AFBC_YTR| AFBC_CBR| AFBC_SPARSE

YUV format:
AFBC_SIZE_16X16| AFBC_CBR AFBC_CBR
AFBC_SIZE_16X16| AFBC_CBR| AFBC_SPARSE

The various define of the kernel are described as follows:

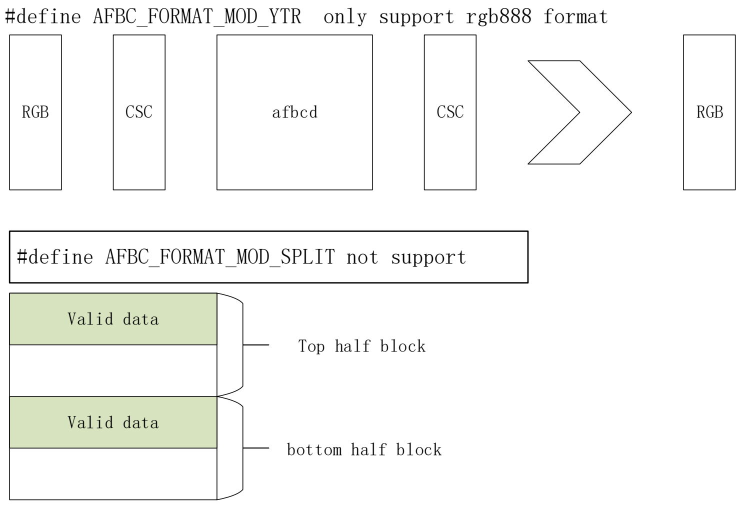


Fig. 7-17 Diagram 1 of AFBCD define

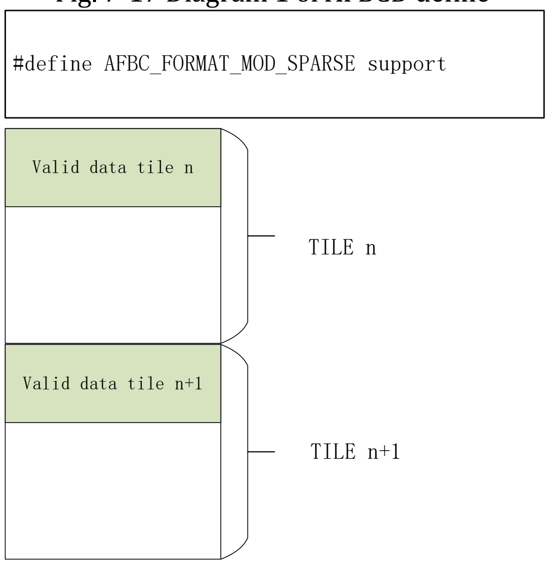


Fig. 7-18 Diagram 2 of AFBCD define

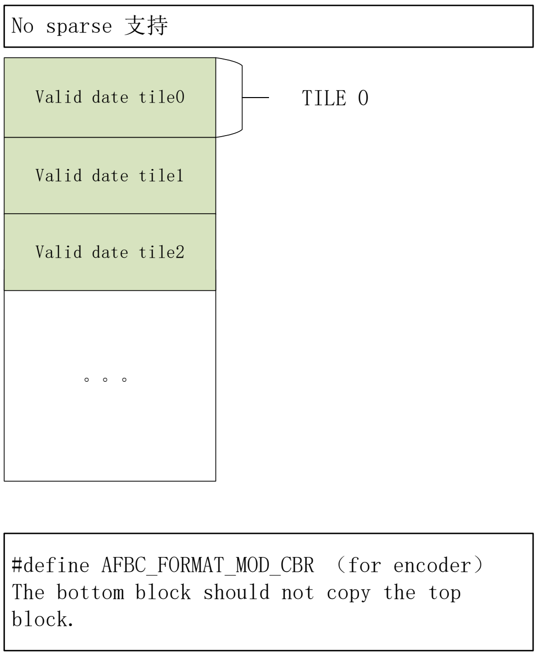


Fig. 7-19 Diagram 3 of AFBCD define

7.4.1.4 line/tile mode

When using raster sequence line/tile mode
Line mode:

- RGBA8888
- RGB888
- RGB565

Tile8x8 mode :

- YUV420 8bit/10bit
- YUV422 8bit/10bit
- YUV444 8bit/10bit

7.4.1.5 CSC module description

Support yuv2rgb, rgb2yuv color gamut space conversion, you can select the corresponding csc according to the input image format and the spatial gamut of the overlay.

RGB2YUV supports the following modes:
Parameter BT_601_L = 2’b00;
Parameter BT_709 = 2’b01;
Parameter BT_601_F = 2’b10;
Parameter BT_2020 = 2’b11;

YUV2RGB supports the following modes:
Parameter BT_601_L = 2’b00;
Parameter BT_709 = 2’b01;
Parameter BT_601_F = 2’b10;
Parameter BT_2020 = 2’b11;

In BT2020 mode, it defaults to limit range, and there is no full range option.

7.4.1.6 Gauss filter

As shown in the figure, the two-scale Gauss filter weighted sum mainly includes two steps: the first step is to calculate the edge detection and the strong and weak Gauss filter respectively; the second step is to obtain the weighting coefficient and the result of the two Gauss filter based on the edge detection result Perform a weighted sum.
In principle, denoising intensity and detail preservation are two mutually exclusive effects, so edge detection and weighting are used to balance the effects of both sides as much as possible, and the filtering effect should be strengthened in the flat area as much as possible, and filtering should be done as little as possible in the rich detail area to avoid affecting the

sharpness and detail.

Through edge detection, confirm whether the calculation point is an edge or a flat area. If it is an edge, use weak Gauss filter to preserve details. If it is a flat area, use a stronger gauss to enhance the filtering effect.

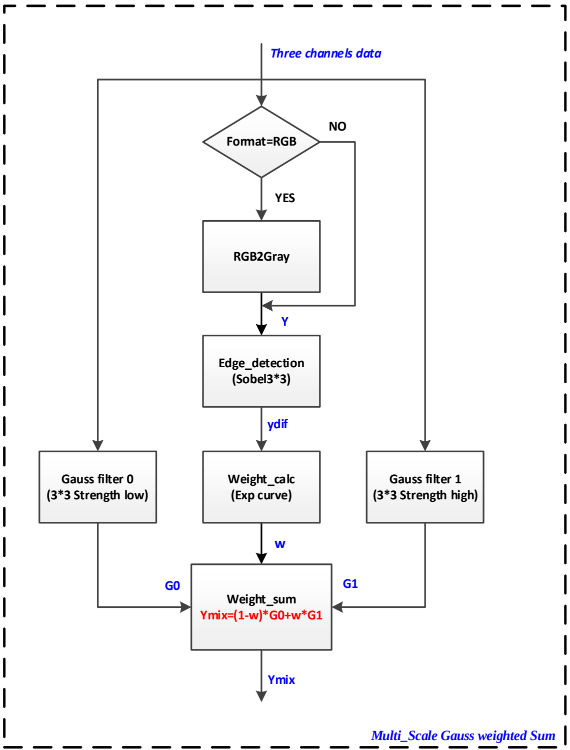


Fig. 7-20 Flow chart of dual gauss filter

In terms of configuration, filter coefficients of high and low intensities are respectively configured. If they are configured to be consistent, it can be considered as a unified Gauss filter.

7.4.1.7 Scale

In the horizontal direction: bilinear and bicubic
In the vertical direction: bilinear

7.4.1.8 Mirror/rotation

In AFBCD full mode, cluster supports X-mirror, Y-mirror, X-mirror plus Y-mirror (equivalent to rotation180°), and rotation 90° and rotation270°.

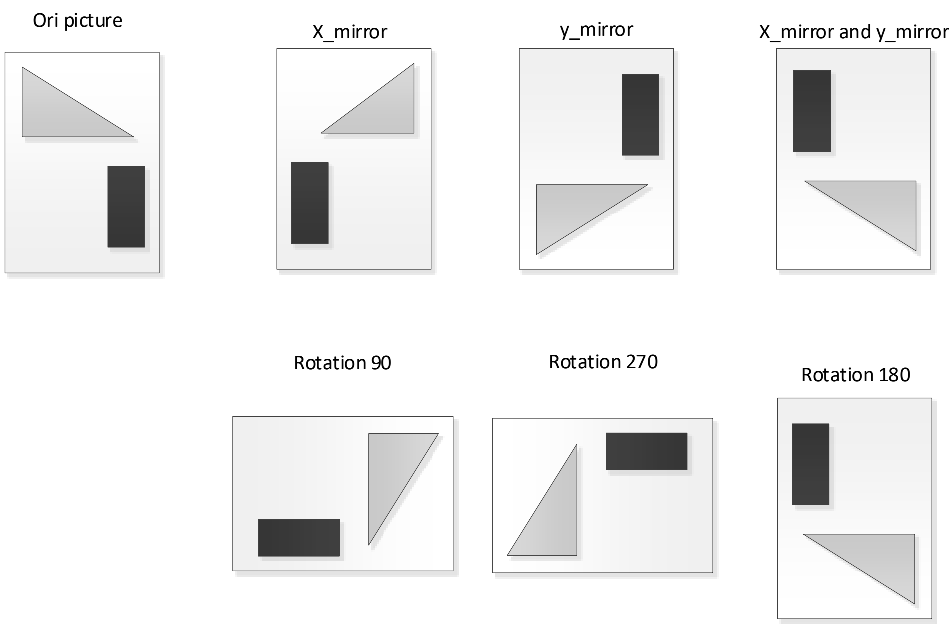


Fig. 7-21 Schematic diagram of mirror and rotation

7.4.1.9 Crop

Due to the characteristics of Android, the UI stored in the DDR is often an image larger than the actual display, so it is necessary to cut out a small image from the original image to display.

For VOP, only the following key parameters are required:
(1) pic base_DDR
(2) Vir_stride
(3) Act_width/act_height
(4) Act_x_offset/act_y_offset

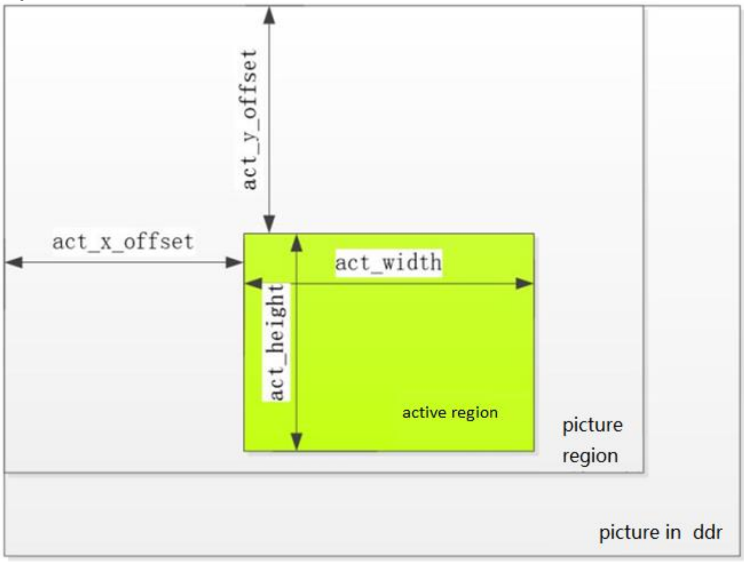


Fig. 7-22 Image storage and activation diagram

The characteristics of the Cluster layer, that is, for the AFBCD-encoded layer, the original width and height are all aligned with 16 pixels.

7.4.1.10 Cluster Usage Constraints

1. The virtual width and height need to be aligned to 16 pixels and the act_width shall not exceed 4096 or 2048 after alignment.
2. In the case of AFBCD rotation enable, virtual width need to be aligned to 64 pixels. The source picture's height cannot exceed 2048 pixels. Rotation and x-mirror can be enabled at the same time, but rotation and y-mirror are not supported at the same time. Rot90 and rot270 cannot be enabled at the same time.
3. Line/Tile mode unsupported: Guass Filter / Rotation / Mirror.
4. Line/Tile mode, the half mode bit should be set to 1.
5. Scaling ratio: (1/4~4)
6. In the case of LB two window mode, (act_width+act_xoffset%16) <= 2048 pixels.
7. In the case of LB two window mode, the parity of the two windows's dsp_xoffset、dsp_yoffset and dsp_width value shoule be same.
8. When AFBCD_mode is half mode, crop can be 0 or 1; when AFBCD_mode is full mode, crop can be 0/1/2.
9. When enable the win*_yrgb_vsd_gt4, the win*_act_yoffset should be multiple of 4.
10. When enable the win*_yrgb_vsd_gt2, the win*_act_yoffset should be multiple of 2.
11. When the data format is YUV420, the win*_act_xoffset and win*_act_yoffset should be multiple of 2.
12. When the data format is YUV422, the win*_act_xoffset should be multiple of 2.

7.4.2 Esmart layer

1. Feature
- Support line mode
- Support color gamut space conversion

- Support 4 area display
- Support 1/8~8 times infinite scale
- Support image virtual width/cropping

2. Basic bus
The bus behavior of the Smart layer is to take one row of buffers when one row is free. It cannot be taken in two rows at a time like the 8 rows of the cluster layer. Basically, each row has a part of time for bus access. The power consumption of DDR is also not very friendly.

3. Power consumption description
The logical power consumption of the smart layer is smaller than that of the cluster layer, but because the cluster has AFBCD modules, plus the power consumption of the DDR controller and phy, the overall power consumption of the smart layer is much larger than the overall power consumption of the cluster layer.

It is recommended to use AFBCD as much as possible for those AFBCD application, and smart layer may be used in multi-region features.

7.4.2.1 Format

Table 7-5 Swap configuration table in esmart default format

esmart		
Format	**rb_swap**	**uv_swap**
ARGB	1	0
RGB888	1	0
RGB565	0	0
YUV420	0	1
YUV422	0	1
YUV444	0	1
YVYU422	0	1
YVYU420	0	1
VYUY422	0	1
VYUY420	0	1
YUV420_10b	0	1
YUV422_10b	0	1
YUV444_10b	0	1

7.4.2.2 CSC

Smart's csc and cluster are the same, please refer to the cluster chapter.

7.4.2.3 Scale

Horizontal direction algorithm:
Scl up: best-neigh/bilinear/bicubic
Scl dn: best-neigh/bilinear/average

Vertical direction algorithm:
Scl up: best-neigh/bilinear/bicubic
Scl dn: best-neigh/bilinear/average

7.4.2.4 Crop

The cutting function of Smart is basically the same as that of cluster, and the film source does not have the limitation of 16align.

7.4.2.5 Usage Constraints

(1) YUV422/420_10b act_offset in smart must be an integral multiple of 8.
(2) vrev_en is not supported under YUYV420.
(3) Under the YUYV/VYUY420 format, the uv component does not support the bic/average algorithm in the Y direction.

(4) In YUYV/VYUY420 format, the Y direction cannot exceed 2 times when scaling (bil/nei algorithm).

7.4.3 8K Senario

7.4.3.1 Layer stitching

Since 8K(7680x4320) is 4 times the performance of 4K, the performance of a single layer 2pixel rate*750M cannot meet the requirements of 8K (4pixel rate*600M). So two layers are needed to stitch together to get 4pixel rate * 750M computing performance to meet actual needs.

Fig. 7-23 Description of 8K layer left and right stitching

7.4.3.2 8K Scaling

7.4.3.2.1 No scale

For the scene without scaling, a picture size between 4K and 8K is displayed on the screen of 7680x4320 as follows. It is recommended that the left 4K part is handed over to a cluster or esmart layer to process, and the remaining right part is handed over to the other layer.

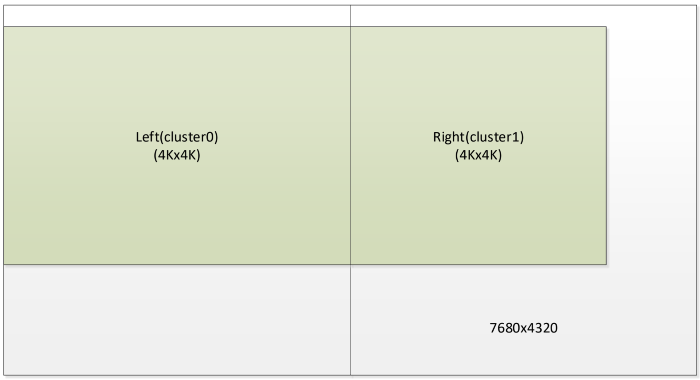


Fig. 7-24 8K Diagram without Scaling

7.4.3.2.2 Scale up

As shown in the figure below, if a 4K picture needs to be placed in 6.5K and displayed on an 8K interface; the configuration needs to reverse the left and right of dst to src and enlarge them respectively.

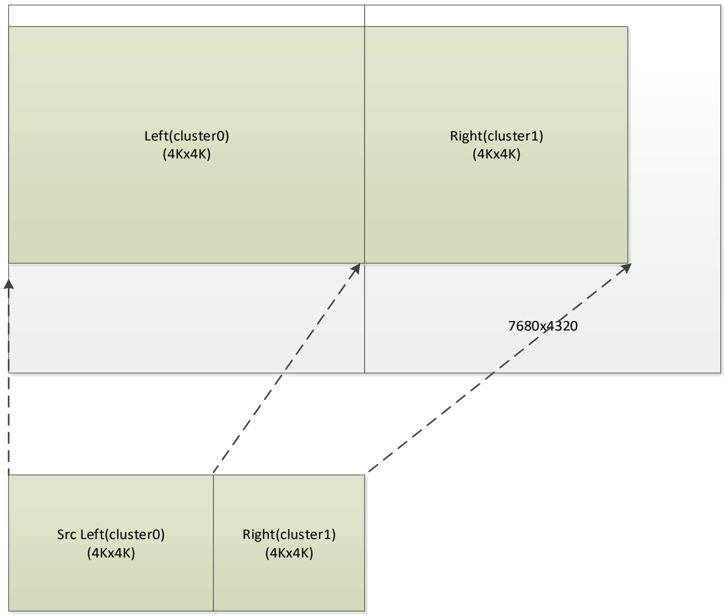


Fig. 7-25 8K scale up schematic diagram

7.4.3.2.3 Scale down

- Cluster:

Due to the performance problems of the previous layer processing under 8K, the cluster performance cannot meet the downscale requirement. At the same time, the structure of the cluster is the data advanced line buffer and then scaled, so try not to use the cluster layer When scaling out, scaling can only scale out in the center of the layer. It can meet 8096->7680. That is, the processing scene is that the source is 8K and the screen is 7680. in addition, it can meet the reduction problem of TV over-scanning.

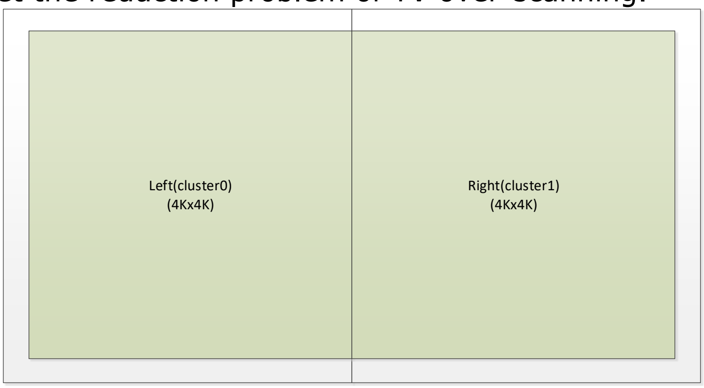


Fig. 7-26 8K centered scaling diagram

- Smart:

Because the structure of smart is different from cluster, the scaling process for X direction is finished before writing to the buffer, so for smart, 8K scaling has no effect, as long as destination picture size does not exceed 4K, source picture size could support 8K. As shown in the figure below, a 6.5K source picture needs to be displayed on the left half of the screen, so only one layer needs to be enabled.

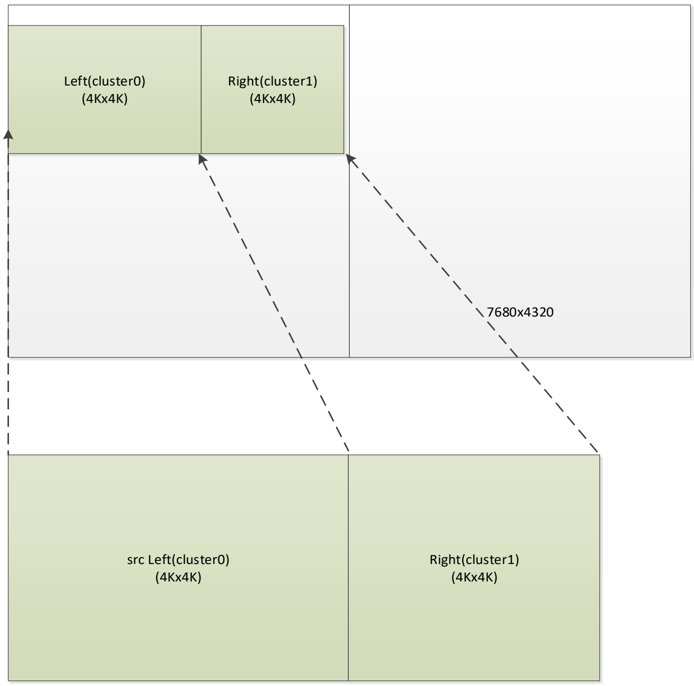


Fig. 7-27 8K smart scaler down schematic diagram

7.4.3.3 PORT splicing and configuration

For the post-processing module, it is also required to support the 8K resolution through the cooperative processing of the two PORTs where enable port0 and port1 at the same time. And the subsequent processing of the two PORTs both are processed in accordance with the 4Kx4K image processing of the left and right half screens, and are written into the post line buffer according to a certain data order relationship. Finally, under the control of the scan timing of port 0, the left half and the right half of the image data are sequentially read from the line buffer 0 and the line buffer 1 to form a complete 8K picture.

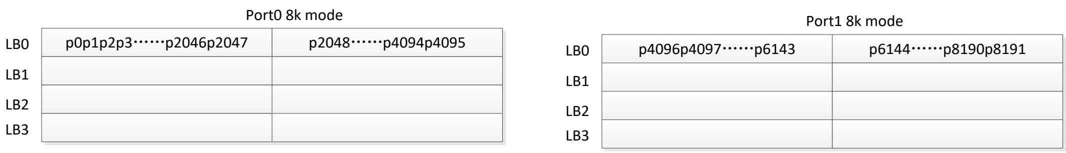


Fig. 7-28 Description of PORT0/1 Post Line Buffer in 8K Mode

7.4.3.4 8K Usage Constraints

(1) It is recommended that the cluster does not enable scaling function.
(2) To support over 4K resolution, the width of picture shall be 8 pixel's alignment.
(3) Unsupport feature: rotation

7.4.4 HDR10

7.4.4.1 Basic process introduction

- **SDR2HDR**

In order to get a better viewing experience, not only the bit depth and the ITU standard have been upgraded to 10bit BT2020, but also HDR has been studied in recent years, with a higher dynamic range to better produce bright and dark scenes.
The conversion process is shown in the figure below:

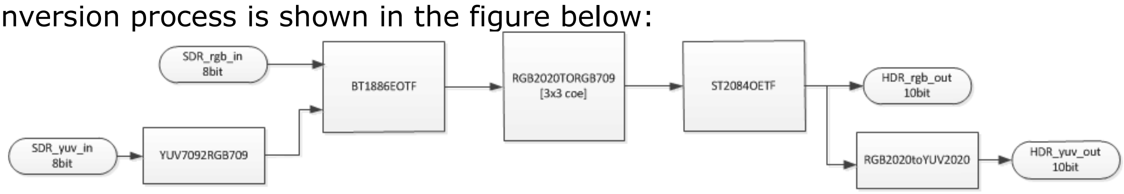


Fig. 7-29 SDR2HDR conversion flowchart

- **HDR2SDR**

The conversion process is shown in the figure below:

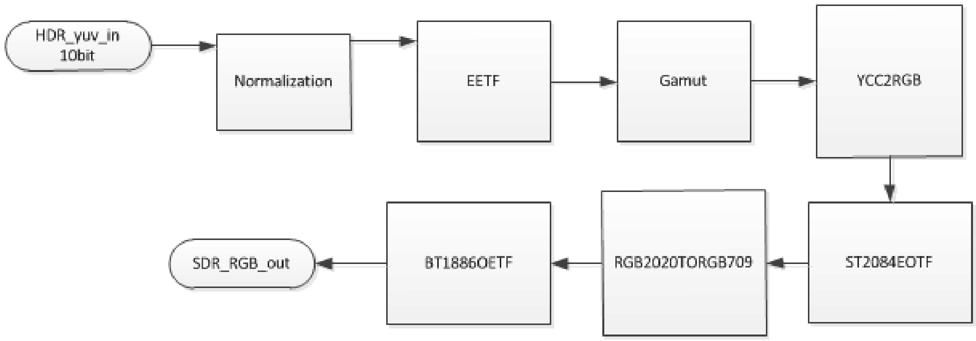


Fig. 7-30 HDR2SDR conversion flowchart

7.4.4.2 LUT configuration instructions

7.4.4.3 Display Effect

If the TV is in HDR mode, then the original SDR source or SDR UI needs to be converted accordingly, otherwise the displayed color will have a great sense of distortion (such as over-saturated, over-brilliant).

If the TV interface is SDR, user need to do the corresponding conversion when playing HDR source, otherwise there will be great distortion in the displayed color (such as loss of saturation and pale color).

7.4.5 Overlay

7.4.5.1 Schematic diagram of layer data path

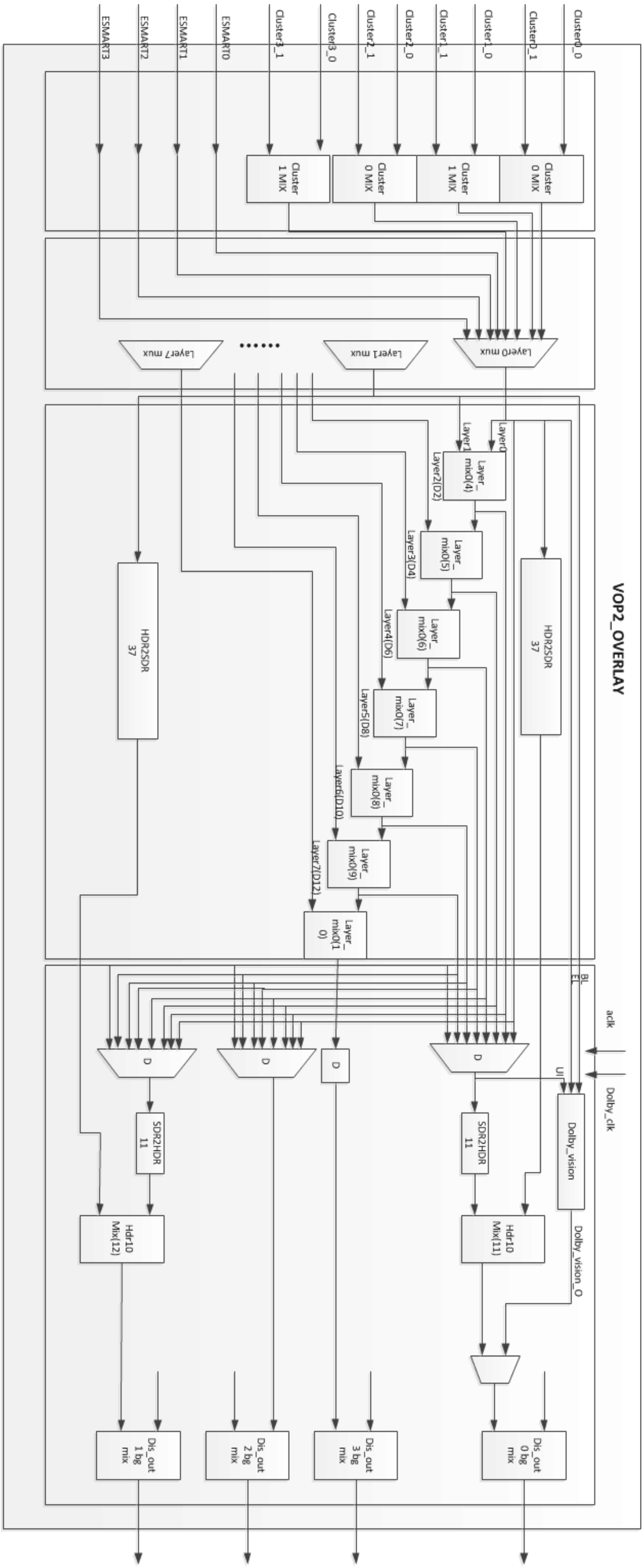


Fig. 7-31 VOP2 overlay block diagram

7.4.5.2 Delay setting of each function

As shown in the figure below, the upper part is the basic delay of each module, the lower

part is the typical delay number setting. Bg is set according to the output of the last level of mux, if the output from the previous level is reduced by 2 on this basis.
The following conditions shall be met:
Cluster default delay+HDR default delay+the delay set by the cluster software =
Smart default delay+HDR default delay+the delay set by the smart software =
Delay set by Bg
Typical settings are as follows:

Table 7-6 Default table of layer delay number

Block		**Delay_num**
HDR2SDR		37
SDR2HDR		11
cluster		33
esmart		14
The delay of the last mux output	ovl_PORT0/1	17
	ovl_PORT2/3	15

Table 7-7 Default table of layer delay number

	cluster	**esmart**	**bg0/1(The delay of the last level mux output)**	**bg2/3(The delay of the last level mux output)**
normal	4	23	54	52
HDR2SDR	26(SDR)	45(SDR)	76	NA
	4(HDR10)	23(HDR10)		
SDR2HDR	4(SDR)	23(SDR)	65	NA
	29(HDR10)	48(HDR10)		

7.4.5.3 Alpha module

If there is no alpha processing, it is a direct coverage effect. Therefore, it is necessary to do an alpha effect on the corresponding layer or the corresponding position to achieve the superposition of the UI and the background or video. Most of them are aimed at the RGB data with alpha output by the GPU, such as RGBA8888; or the global alpha of the layer is configured inside the VOP to realize the special effect of superimposing between the layers. The following picture shows the basic alpha overlay effect:

Fig. 7-32 Schematic diagram of alpha effect

1. Per-pixel Alpha

Per-pixel alpha, as the name implies, is that each point has corresponding alpha information. As shown in the picture above, the alpha value of each point in Jordan's picture increases from 0 to 255 in cycles from left to right, and the effect gradually changes from fully transparent to impermeable.

2. Global Alpha

The global alpha has nothing to do with the original data. You can set the alpha value of the entire layer separately. As shown in the figure above, the little bee layer is a global alpha effect, and the transparency of the entire layer is the same.

3. Pre-mult Alpha

Pre-multiplied alpha means that in the process of GPU operation, the original data and alpha have been multiplied accordingly, and there is no need to multiply alpha by its own RGB value during subsequent superposition.

The modes of Alpha are shown in the figure below:

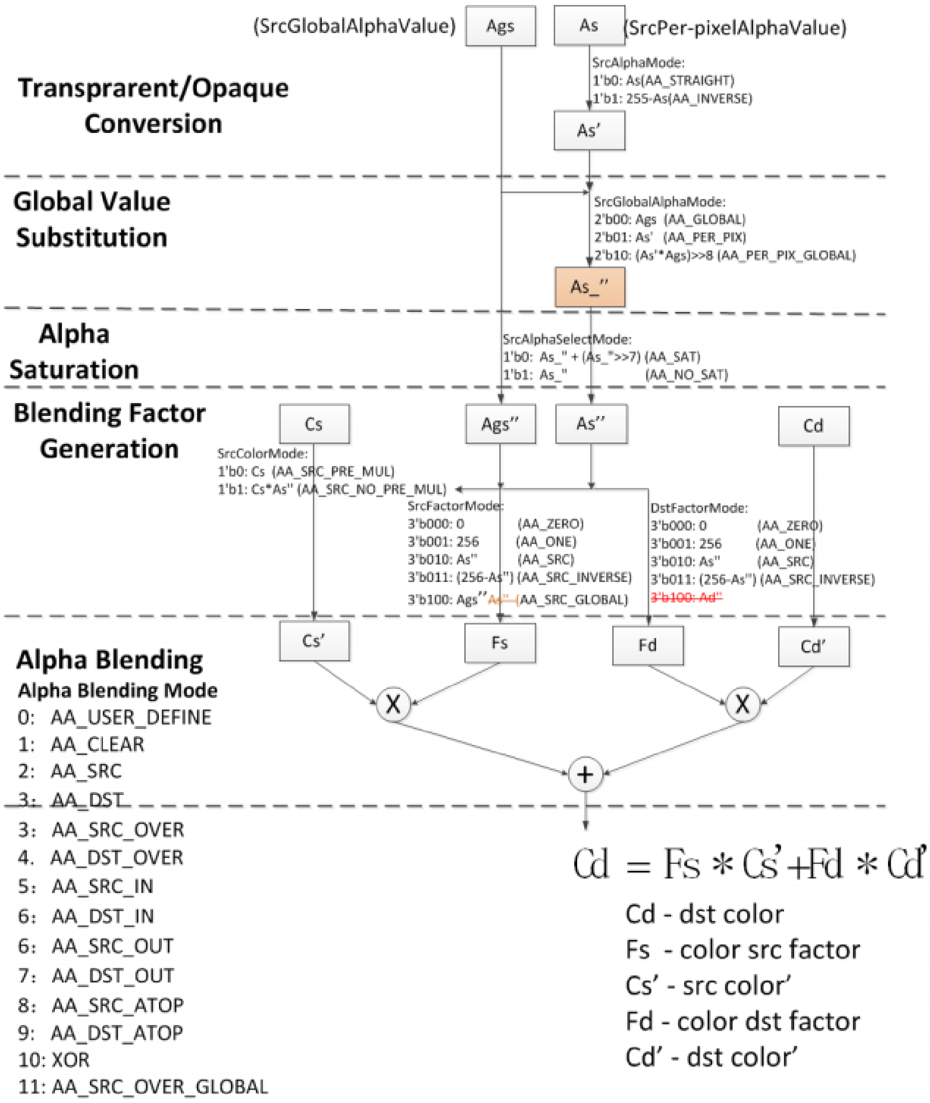


Fig. 7-33 Alpha structure diagram

7.4.5.4 Secure Mode

The secure mode hardware will put the secure layer on the top layer of the selected PORT. For details, please refer to the description of 1.3.9 secure scheme.

7.4.5.5 Usage Constraints

(1) When the layer is switched by bus, the layer shall be disabled.
(2) When the post is switching mix, all the layers involved shall be disabled.

7.4.6 Write Back

7.4.6.1 Support format

1. Support format

- ARGB888
- RGB888
- RGB565

- YUV420

2. Color gamut conversion
Since the main application scenario output is RGB, but there is a need for YUV420 write-back, the write-back module adds RGB2YUV format conversion, which is enabled by configuring wb_rgb2yuv_en register bit.

7.4.6.2 Single frame/multi frame mode

(1) Single frame mode
Operating in single frame mode, enable the oneframe_clr register, and automatically disable wb_en after each frame is written, so that only one frame of content will be written out.

(2) Multi-frame mode
Each frame is configured with a different address, and the wb module will continuously write out the corresponding whole frame content.

(3) Line write mode
After enabling, the pixels accumulated in a row are written back to DDR in a concentrated manner to improve the efficiency of write back.

7.4.6.3 Horizontal scaling

The bilinear scaling algorithm is used in the horizontal direction.

7.4.6.4 Vertical stroke

Due to the limitation of memory, there is not enough linebuffer opened separately, so no scaling is done in the y direction. If more than twice, wb_ythrow_en is configured to control the line-throwing operation to reduce the output bandwidth.

7.4.6.5 Usage Constraints

(1) In the case of YUV domain output, the conversion of YUV2RGB is not supported, that is, RGB format cannot be written back under YUV domain.
(2) Act_width must be an integer multiple of 16 in write-back mode.

7.4.7 Post process

Function of each PORT 0/1/2/3 and the post-processing modules included in each PORT.

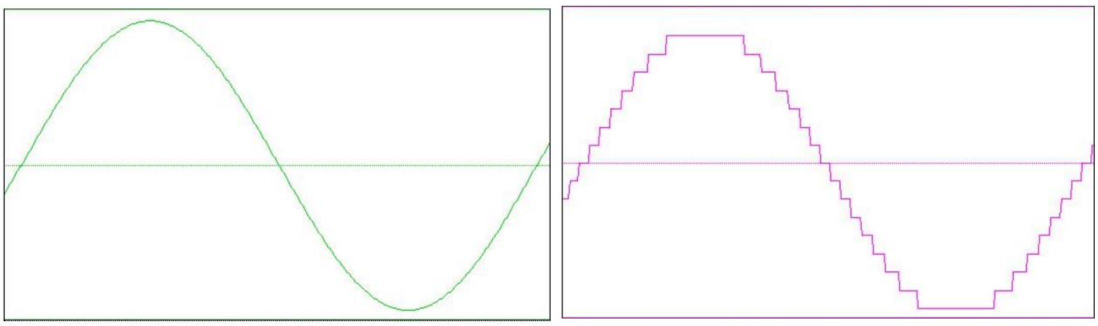
7.4.7.1 Color bar

Each PORT has a corresponding color bar setting, which can be used to debug to eliminate bus and layer problems, and it can also bypass the layer to directly adjust each high-speed output interface.
Control register color_bar_en to enable colorbar of PORT;
Control register color_bar_mode to switch horizontal colorbar or vertical colorbar.

7.4.7.2 Dither

If an 8bit film source needs to be output to the rgb666 screen, if there is no dither, it is directly connected to the screen with a high 6bit. In this case, the color gradation will be caused.

In principle, the smooth curve becomes a ladder after losing the low position. In order to solve this problem, noise is added to the ladder, so that the transition can restore the original smooth curve as much as possible.



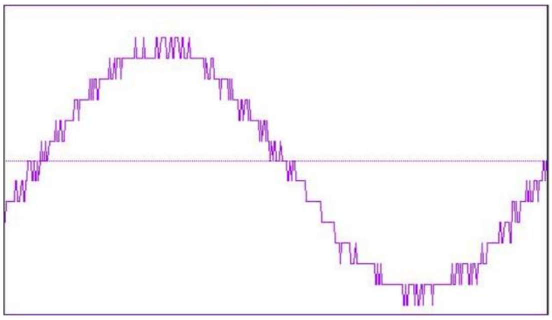


Fig. 7-34 Schematic diagram of dither principle

VOP has ALG in the dither algorithm of 10bit->8bit; there are ALG and FRC in the dither algorithm for 8bit->666/565, which can be selected by dither_down_mode.

ALG algorithm: Add fixed noise, the possible negative effect is that there will be more regular stripes similar to tire tracks;

FRC algorithm: time-domain jitter is added to the space, which works well in high frame rate scenes, and low frame rate scenes may feel a little flickering and jittery.

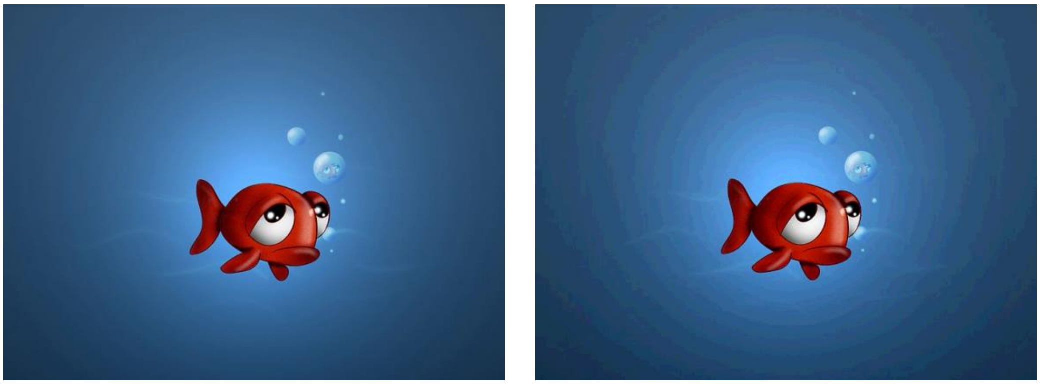


Fig. 7-35 Dither effect diagram

Left: original picture; right: direct clip effect

The above picture shows the color scale effect of the original picture and the direct clip. The figure below is the figure processed by the dither algorithm. The overall effect is obvious to solve the color gradation problem caused by dither, but after partial magnification, the tire-like effect on the right side of the figure below will appear.

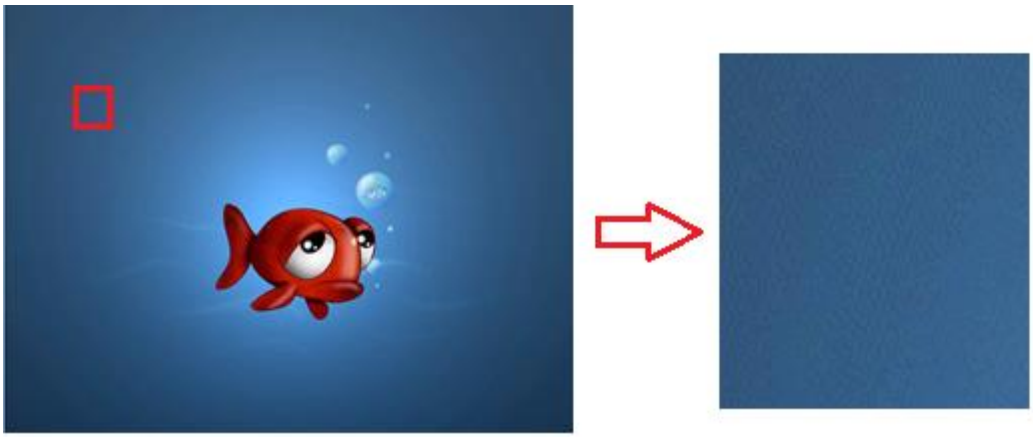


Fig. 7-36 Schematic diagram of dither's tire pattern

7.4.7.3 BCSH

BCSH mainly adjusts the following effects:

(1) CON: Contrast coefficient

(2) BRT: Bright picture adjustment value

(3) HUE: hue adjustment angle

(4) SAT: Saturation coefficient

Y processing calculation formula
Y0=Y_{input}-16;   (0<Y0<239)
Y1=Y0*CON; (0<CON<1.992)   (0<Y1<478)
Y2=Y1+BRT;(-32<BRT<31)   (-32<Y2<509)
Y3=Y2+16;   (-16<Y3<525)
Y_{output}= 4 mux 1

U processing calculation formula
U0=U_{input}-128;   (-128，127)
U1=U0*cosHUE + V0*sinHUE （-30º<HUE<30º）   (-175，174)
U2=U1*CON*SAT; (0<CON<1.992，0<SAT<1.992)   (-695，691)
U3=U2+128;   (-567，819)
U_{output}= 4 mux 1
Cos(HUE)+sin(HUE) = $(1+1/2*\sin(2HUE))^{1/2}$;
So this value increases monotonically with the increase of the value of HUE. The value range of HUE is -30~30.

V processing calculation formula
V0=V_{input}-128;   （-128，127）
V1=V0*cosHUE - U0*sinHUE （-30º<HUE<30º）   （-175，174）
V2=V1*CON*SAT; (0<CON<1.992，0<SAT<1.992)   （-695，691）
V3=V2+128;   （-567，819）
V_{output}= 4 mux 1
cosHUE-sinHUE = $(1+1/2*\sin(-2HUE))^{1/2}$;

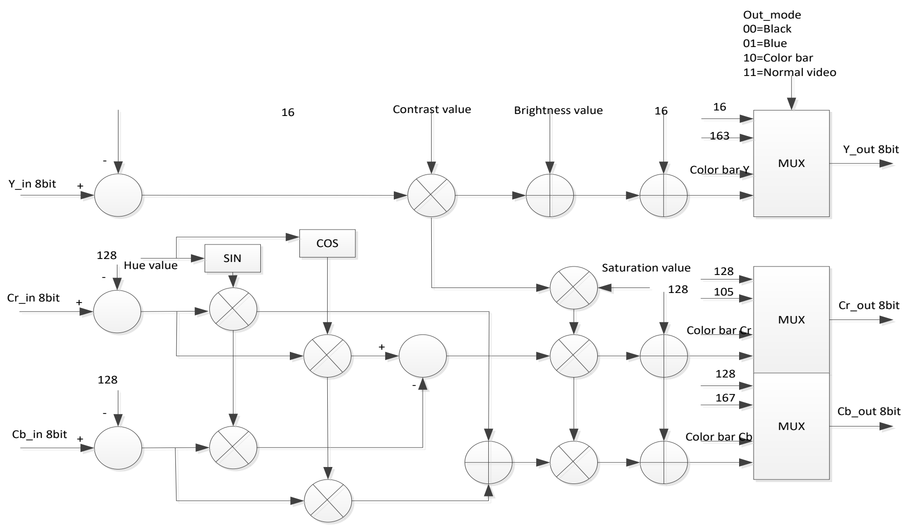


Fig. 7-37 Schematic diagram of BCSH algorithm

7.4.7.4 Gamma

Gamma basic principle:
Gamma can be understood as a 1:1 remapping of the RGB on the display channel. The three RGB curves can be consistent or inconsistent. Therefore, the display color temperature and blue light removal effects can be adjusted through the mapping relationship of the three curves.

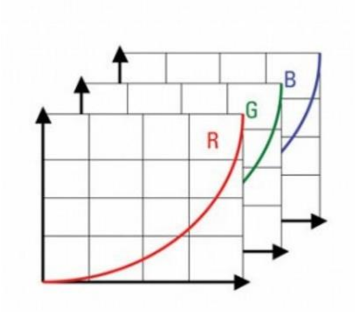


Fig. 7-38 Schematic of gamma

Dual gamma:
Because the application may adjust the gamma curve to achieve dynamic adjustment of some color temperature effects. However, the memory of the gamma table is a single-port memory. When a new table is written, it is necessary to disable gamma, which will cause screen flicker when dynamically adjusting the gamma curve.

In order to solve this flicker phenomenon, VOP adopts the ping-pong dual gamma. By statically switching gamma, one table is displayed and used in real time, and the other table is a new table that can be configured.

7.4.7.5 3D LUT

Gamma can be regarded as a 1D LUT. The RGB data in the 1D LUT are independent of each other, which means that the 1D LUT can only control the gamma value, RGB balance (gray scale) and white point. In order to overcome the limitation of 1D LUT, we can form a 3×3 matrix of three 1D LUTs of RGB to control the color saturation and brightness, and perform linear scaling in the complete color space. The 3D LUT can affect the hue, saturation, brightness, etc. in a full three-dimensional color space control method.

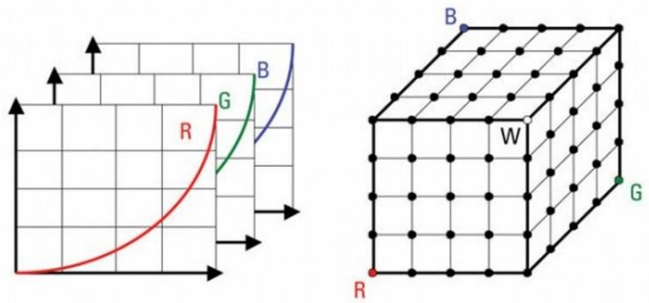


Fig. 7-39 Schematic diagram of 2D/3D-LUT

3D LUT application scenarios:
(1) Calibration (calibration LUT)
It is mainly used for the calibration of hardware and display equipment in color management. The video will be processed by different systems during the shooting, post-processing and final projection, and will appear in different forms. Therefore, the 3D LUT color space mapping can ensure that the video remains visually consistent in different systems.

(2) Technology (Technical LUT)
It is mostly used for conversion under different characteristic curves in different color spaces. Mapping from Log to Rec709 belongs to this type. The color standards of computer monitors, televisions, mobile phones, and Pads that we come into contact with in work and life are very close to Rec.709. However, now a large number of cameras and even SLRs can shoot log (Log) video. If the log video is sent to the Rec.709 standard monitor for monitoring, it cannot be restored normally. The fundamental reason is that the gamma difference between the two is very large, so it needs to be artificially corrected to the display system gamma.

Fig. 7-40 Effect picture before correction

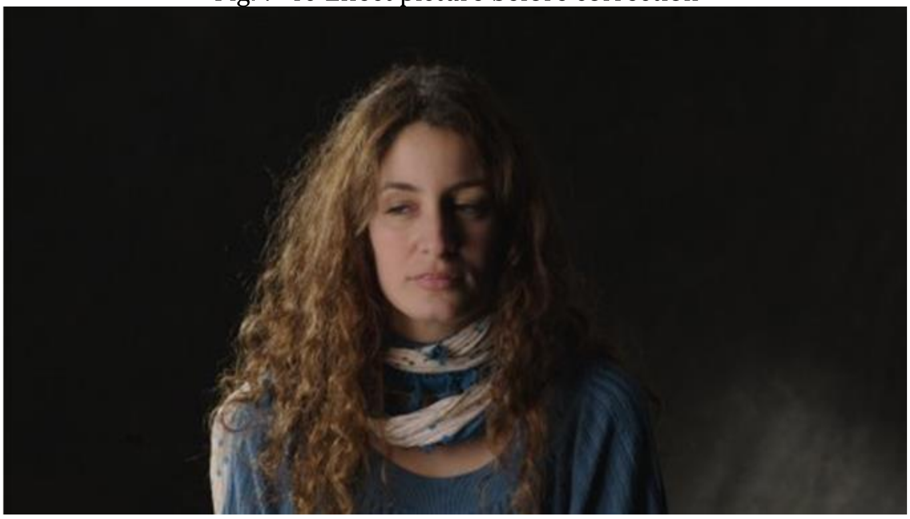


Fig. 7-41 Effect picture after correction

(3) Style (Creative LUT/Looks LUT)

In order to realize a certain style of LUT, the LUT produced by the director of photography during the pre-shooting and can be previewed on-site. Using LUT to calibrate the color of the monitor does not creatively process the video. Another type of use of LUT is to color, that is, creatively process the video.

Fig. 7-42 Effect picture before and after toning

Comparison of 3D LUT before (left) and after (right) toning

Accuracy description

Most 3D LUTs use stereo in the range of 9^3 to 65^3. A 9^3 LUT means that each axis has 9 points from input to output, and between these points Interpolation is required for the value between. Different systems will achieve this with varying degrees of accuracy.

In the evaluation of accuracy, the linear table adds a random value of 0 to 0.1 to make a non-linear 3DLUT table. Then use 9x9x9, 17x17x17, 33x33x33 table item evaluation respectively, it can be seen that the more table items, the closer the polyline effect can be. Some scenes need to use 33x33x33 3d LUT.

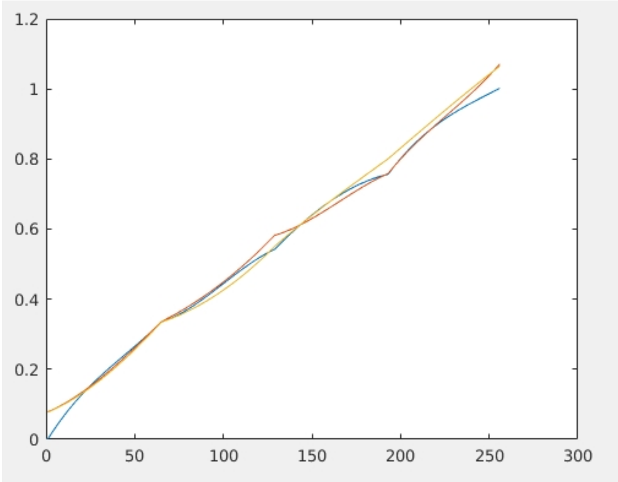


Fig. 7-43 9x9x9 table renderings

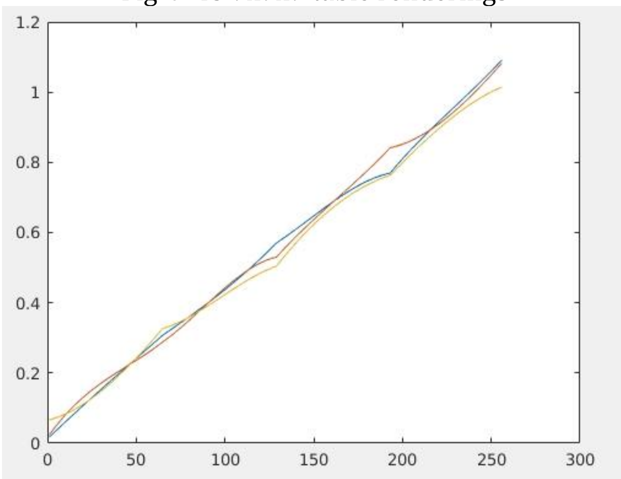


Fig. 7-44 17x17x17 table renderings

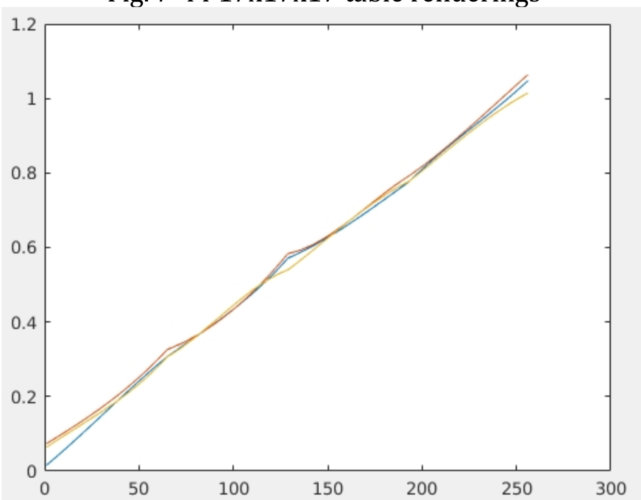


Fig. 7-45 33x33x33 table renderings

But from an implementation point of view, the memory area occupied by 33x33x33 is too large.
7*7*7 memory area 0.0638*2 = 0.1276 mm2
17*17*17 memory area 0.1742*2 = 0.3484 mm2
33*33*33 memory area 0.4683*2 = 0.9366 mm2

According to the compromise between application scenarios and area in VOP, the accuracy of 3D LUT is allocated as follows:
PORT0 and PORT1: 9x9x9;
PORT2: 17x17x17;
PORT3: 3DLUT is not supported.

Application and configuration

In the application, user can adjust the required scene effects through the 3D LUT Creator software and save the 3D LUT table configuration corresponding to 9x9x9 or 17x17x17 to the address corresponding to the VOP.

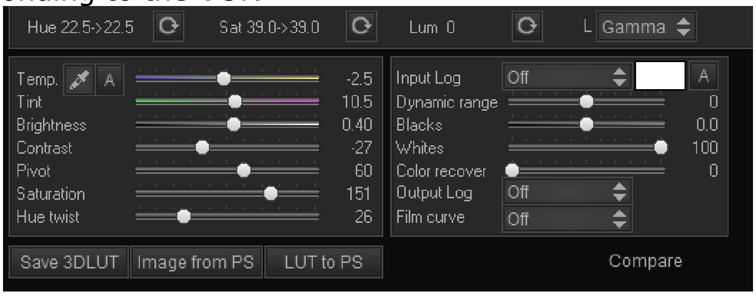


Fig. 7-46 Basic operation interface of 3D LUT Creator

For example, for a 9x9x9 LUT table, a 729-point constant needs to be written to the corresponding memory, which can be written through AXI or AHB. The arrangement is as follows:

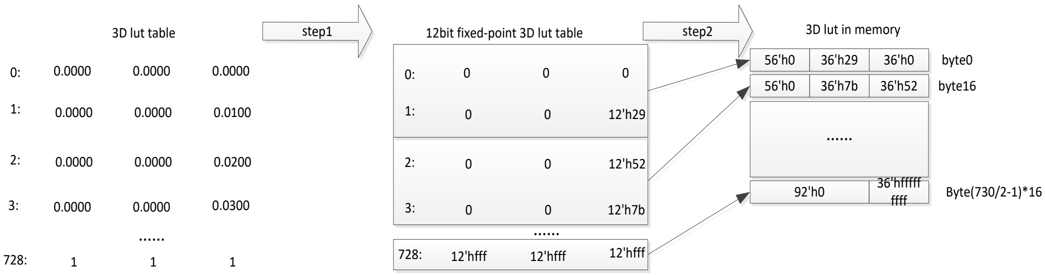


Fig. 7-47 3D LUT table sorting diagram

7.4.7.6 Split

Port0/1/2

7.4.7.7 Timing description

A. Progressive timing configuration

The POST*_PROC registers need to configure:

- VOP_DSP_HTOTAL_HS_END
- VOP_DSP_HACT_ST_END
- VOP_DSP_VTOTAL_VS_END
- VOP_DSP_VACT_ST_END

B. p timing chart example

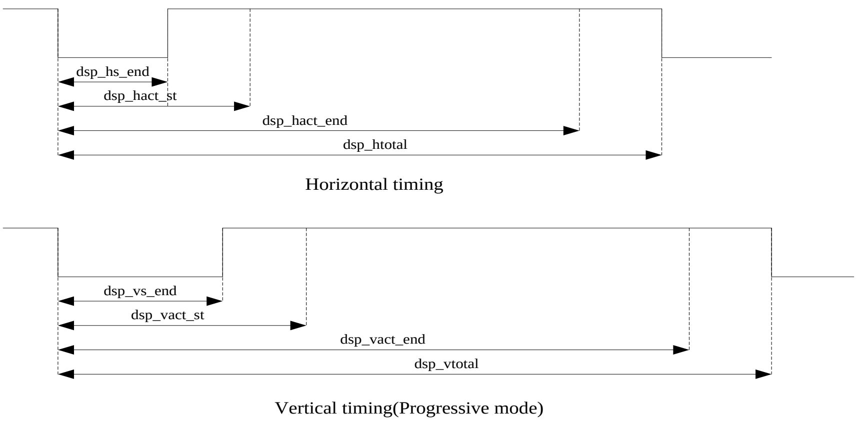


Fig. 7-48 VOP RGB interface timing diagram (progressive mode)

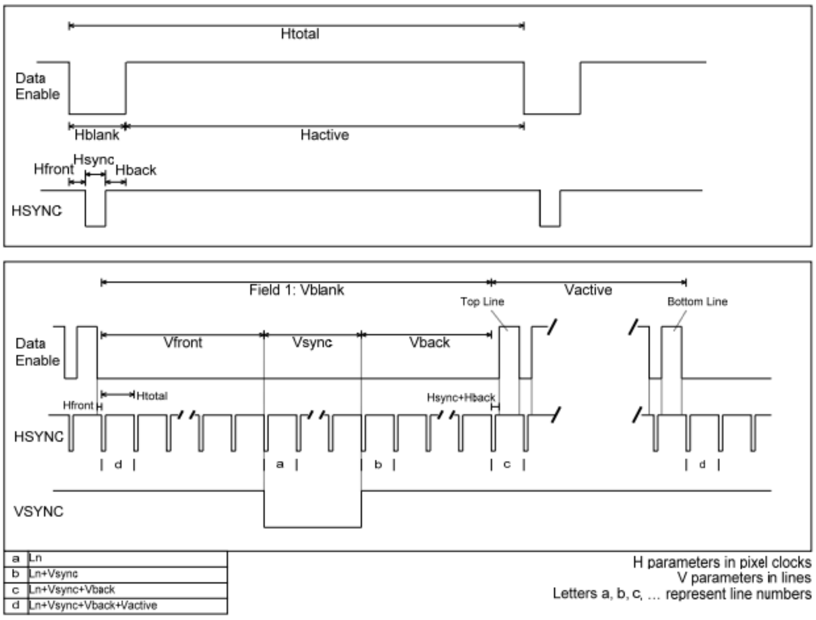


Fig. 7-49 CTA-861 standard timing diagram (progressive mode)

C. Interlace timing configuration

Need to configure the following timing registers:

- VOP_DSP_HTOTAL_HS_END
- VOP_DSP_HACT_ST_END
- VOP_DSP_VTOTAL_VS_END
- VOP_DSP_VACT_ST_END
- VOP_DSP_VS_ST_END_F1
- VOP_DSP_VACT_ST_END_F1

D. i timing chart example

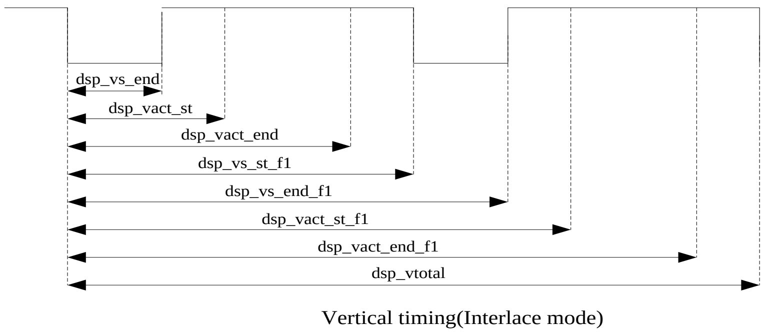


Fig. 7-50 VOP RGB interface timing diagram (interlace mode)

Points to note, the starting point of the second field is at 1/2 of htotal.

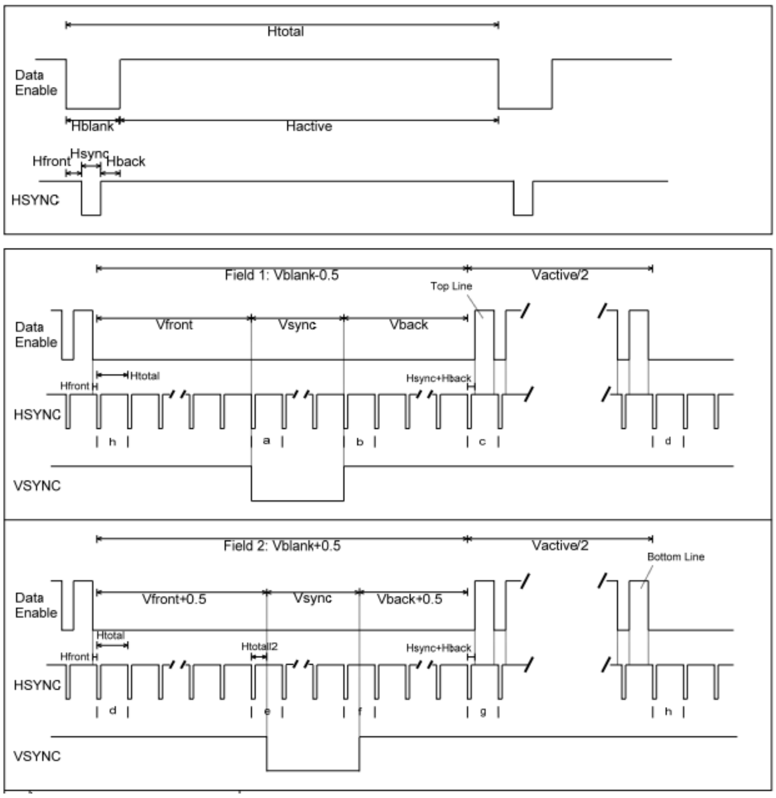


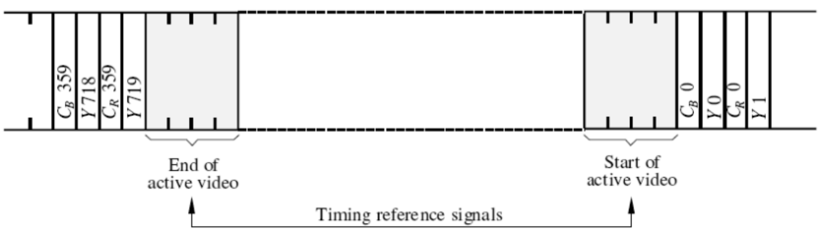
Fig. 7-51 CTA-861 standard timing diagram (interlace mode)

E. BT.656 encoder

VOP extracts the BT656 encoder module separately, the input interface is RGB parallel timing input, and the output is the standard bt656 interface output.

BT656 embeds the line and field synchronization information into the data stream in the form of encoding, which is the so-called Video timing reference codes. Each line includes four parts: SAV, EAV, blanking and video data:

每一行包括SAV、EAV、blanking和video data四个部分：



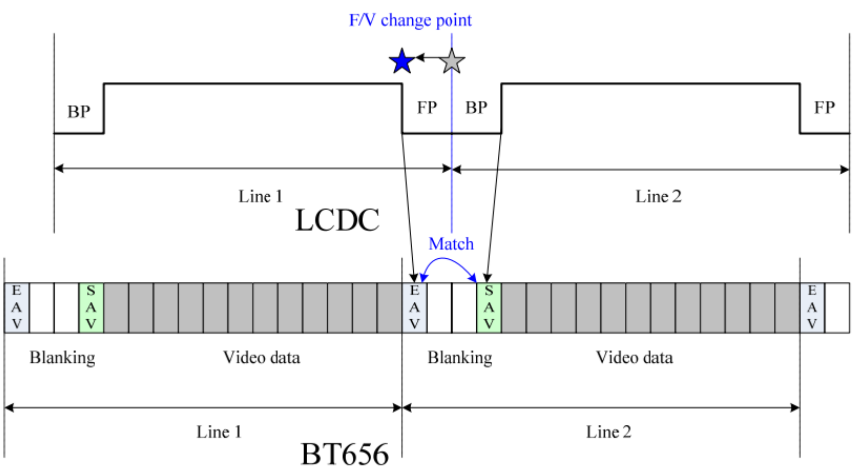
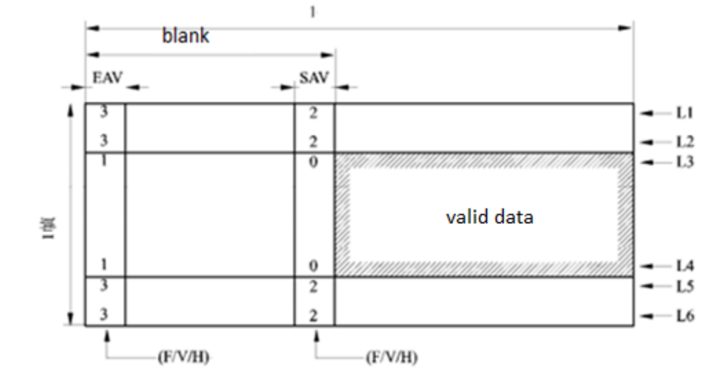


Fig. 7-52 Timing description of BT656

F. BT.1120 encoder

The encoding method is almost the same as BT656, except that the number of data bits increases and the frequency becomes larger to support the transmission of HD data. Maximum support for data transmission up to 1080p, DCLK to 150M. Supports both interlace and progressive transmission at the same time. The specific timing diagram is as follows.



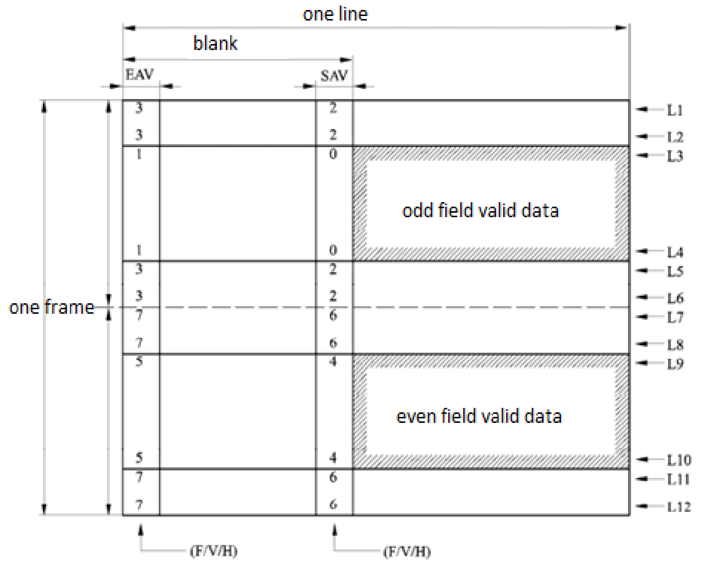


Fig. 7-53 Timing description of BT1120

7.5 Register Description

7.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 7-8 VOP2 Address Mapping

Base Address[15:8]	Module	Address Length	Offset Address Range
0x00	SYS_CTRL	256 BYTE	0X0000 ~ 0X00FF
0x02	DSC_SYS_CTRL	256 BYTE	0X0200 ~ 0X02FF
0x06	OVERLAY	256 BYTE	0X0600 ~ 0X06FF
0x0c	POST0	256 BYTE	0X0C00 ~ 0X0CFF
0x0d	POST1	256 BYTE	0X0D00 ~ 0X0DFF
0x0e	POST2	256 BYTE	0X0E00 ~ 0X0EFF
0x0f	POST3	256 BYTE	0X0F00 ~ 0X0FFF
0x10	CLUSTER0	512 BYTE	0X1000 ~ 0X11FF
0x12	CLUSTER1	512 BYTE	0X1200 ~ 0X13FF

Base Address[15:8]	Module	Address Length	Offset Address Range
0x14	CLUSTER2	512 BYTE	0X1400 ~ 0X15FF
0x16	CLUSTER3	512 BYTE	0X1600 ~ 0X17FF
0x18	ESMART0	512 BYTE	0X1800 ~ 0X19FF
0x1a	ESMART1	512 BYTE	0X1A00 ~ 0X1BFF
0x1c	ESMART2	512 BYTE	0X1C00 ~ 0X1DFF
0x1e	ESMART3	512 BYTE	0X1E00 ~ 0X1FFF
0x40	DSC_8K	256 BYTE	0X4000 ~ 0X40FF
0x41	DSC_4K	256 BYTE	0X4100 ~ 0X41FF
0x50	GAMMA_LUT_ADDR	4096 BYTE	0X5000 ~ 0X5FFF
0x60	BPP_LUT_ADDR	1024 BYTE	0X6000 ~ 0X63FF
0x7e	MMU0	256 BYTE	0X7E00 ~ 0X7EFF
0x7f	MMU1	256 BYTE	0X7F00 ~ 0X7FFF

7.5.2 Registers Summary

7.5.2.1 SYS_CTRL

Name	Offset	Size	Reset Value	Description
SYS_CTRL_REG_CFG_DONE	0x0000	W	0x00008000	Register configure done flag
SYS_CTRL_VERSION_INFO	0x0004	W	0x00000000	RTL version
SYS_CTRL_AUTO_GATING_CTRL_IMD	0x0008	W	0x9FFF7DFF	To control auto-gating
SYS_CTRL_WIN_REG_CFG_DONE	0x000C	W	0x00000000	Win register configure done flag
SYS_CTRL_AXI_CTRL0_IMD	0x0010	W	0x00000000	To control AXI
SYS_CTRL_AXI_HURRY_CTRL0_IMD	0x0014	W	0x00000000	To control AXI0 hurry mode
SYS_CTRL_AXI_HURRY_CTRL1_IMD	0x0018	W	0x00000000	To control AXI1 hurry mode
SYS_CTRL_AXI_OUTSTANDING_CTRL0_IMD	0x001C	W	0x00000000	To control AXI outstanding number
SYS_CTRL_AXI_LUT_CTRL_IMD	0x0024	W	0x00000000	To control the DMA of fetching LUT
SYS_CTRL_DSP_INFACE_EN	0x0028	W	0x00000000	Enable display IF and choose the port
SYS_CTRL_DSP_INFACE_CTRL	0x002C	W	0x00000000	Select Display Interface Pixel Clock Frequency
SYS_CTRL_DSP_INFACE_POL	0x0030	W	0x00000000	To control the polarity of interface
SYS_CTRL_POWER_CTRL	0x0034	W	0x0000000F	To control VOP sub Power Domain
SYS_CTRL_VAR_FERQ_CTRL_IMD	0x0038	W	0x00000000	The address is used to bypass MCU command
SYS_CTRL_MMU_RADDR_RANGE	0x003C	W	0x00000000	To control TVE
SYS_CTRL_WB_CTRL0	0x0040	W	0x70680000	To control WB
SYS_CTRL_WB_XSPD_FACTOR	0x0044	W	0x00000000	To configure the scale factor of WB

Name	Offset	Size	Reset Value	Description
SYS_CTRL_WB_YRGB_MST	0x0048	W	0x00000000	WB YRGB memory starting address
SYS_CTRL_WB_CBR_MST	0x004C	W	0x00000000	WB CbCr memory starting address
SYS_CTRL_OTP_WIN_EN_IMD	0x0050	W	0x00000000	To enable optional function
SYS_CTRL_OTP_MIRR_CTRL_IMD	0x0054	W	0x00000000	To disable optional function
SYS_CTRL_LUT_PORT_SEL	0x0058	W	0x00000000	To select the video output for LUT
SYS_CTRL_POWER_STABLE_CTRL	0x005C	W	0x00000000	control VOP sub power domain stable count value
SYS_CTRL_STATUS0	0x0060	W	0x00000000	The system status of video output0
SYS_CTRL_STATUS1	0x0064	W	0x00000000	The system status of video output1
SYS_CTRL_STATUS2	0x0068	W	0x00000000	The system status of video output2
SYS_CTRL_STATUS3	0x006C	W	0x00000000	The system status of video output2
SYS_CTRL_LINE_FLAG0	0x0070	W	0x00000000	To set the line flag of video output0
SYS_CTRL_LINE_FLAG1	0x0074	W	0x00000000	To set the line flag of video output1
SYS_CTRL_LINE_FLAG2	0x0078	W	0x00000000	To set the line flag of video output2
SYS_CTRL_LINE_FLAG3	0x007C	W	0x00000000	To set the line flag of video output2
SYS_CTRL_INTR_EN0	0x0080	W	0x00000000	To enable system0 interrupt
SYS_CTRL_INTR_CLR0	0x0084	W	0x00000000	To clear system0 interrupt
SYS_CTRL_INTR_STATUS0	0x0088	W	0x00000000	System0 interrupt status
SYS_CTRL_INTR_RAW_STATUS0	0x008C	W	0x00000000	System0 interrupt raw status
SYS_CTRL_INTR_EN1	0x0090	W	0x00000000	To enable system1 interrupt
SYS_CTRL_INTR_CLR_SYS1	0x0094	W	0x00000000	To clear system1 interrupt
SYS_CTRL_INTR_STATUS1	0x0098	W	0x00000000	System1 interrupt status
SYS_CTRL_INTR_RAW_STATUS1	0x009C	W	0x00000000	System1 interrupt raw status
SYS_CTRL_PORT0_INTR_EN	0x00A0	W	0x00000000	To enable video output0 interrupt
SYS_CTRL_PORT0_INTR_CLR	0x00A4	W	0x00000000	To clear video output0 interrupt
SYS_CTRL_PORT0_INTR_STATUS	0x00A8	W	0x00000000	Video output0 interrupt status
SYS_CTRL_PORT0_INTR_RAW_STATUS	0x00AC	W	0x00000000	Video output0 interrupt raw status
SYS_CTRL_PORT1_INTR_EN	0x00B0	W	0x00000000	To enable video output1 interrupt
SYS_CTRL_PORT1_INTR_CLR	0x00B4	W	0x00000000	To clear video output1 interrupt

Name	Offset	Size	Reset Value	Description
SYS_CTRL_PORT1_INTR_STATUS	0x00B8	W	0x00000000	Video output1 interrupt status
SYS_CTRL_PORT1_INTR_RAW_STATUS	0x00BC	W	0x00000000	Video output1 interrupt raw status
SYS_CTRL_PORT2_INTR_EN	0x00C0	W	0x00000000	To enable video output2 interrupt
SYS_CTRL_PORT2_INTR_CLR	0x00C4	W	0x00000000	To clear video output2 interrupt
SYS_CTRL_PORT2_INTR_STATUS	0x00C8	W	0x00000000	Video output2 interrupt status
SYS_CTRL_PORT2_INTR_RAW_STATUS	0x00CC	W	0x00000000	Video output2 interrupt raw status
SYS_CTRL_PORT3_INTR_EN	0x00D0	W	0x00000000	To enable video output2 interrupt
SYS_CTRL_PORT3_INTR_CLR	0x00D4	W	0x00000000	To clear video output2 interrupt
SYS_CTRL_PORT3_INTR_STATUS	0x00D8	W	0x00000000	Video output2 interrupt status
SYS_CTRL_PORT3_INTR_RAW_STATUS	0x00DC	W	0x00000000	Video output2 interrupt raw status
SYS_CTRL_AFBCD_INTR_EN0	0x00E0	W	0x00000000	To enable AFBCD interrupt
SYS_CTRL_AFBCD_INTR_CLR0	0x00E4	W	0x00000000	To clear AFBCD interrupt
SYS_CTRL_AFBCD_INTR_STATUS0	0x00E8	W	0x00000000	AFBCD interrupt status
SYS_CTRL_AFBCD_INTR_RAW_STATUS0	0x00EC	W	0x00000000	AFBCD interrupt raw status
SYS_CTRL_AFBCD_INTR_EN1	0x00F0	W	0x00000000	To enable AFBCD interrupts
SYS_CTRL_AFBCD_INTR_CLR1	0x00F4	W	0x00000000	To clear AFBCD interrupts
SYS_CTRL_AFBCD_INTR_STATUS1	0x00F8	W	0x00000000	AFBCD interrupt status
SYS_CTRL_AFBCD_INTR_RAW_STATUS1	0x00FC	W	0x00000000	AFBCD interrupt raw status
SYS_CTRL_SEC_DRM_CTRL	0x0100	W	0x00000000	Secure control
SYS_CTRL_SEC_DRM_LAYER_SEL	0x0104	W	0x00000000	Secure layer select
SYS_CTRL_SEC_DRM_PORT_MUX	0x0108	W	0x00000000	Secure port mux
SYS_CTRL_SEC_DRM_INFACE_MUX	0x010C	W	0x00000000	Secure interface mux
SYS_CTRL_SEC_AXI_RID_PROT	0x0110	W	0x00000000	Secure rid

7.5.2.2 DSC_SYS_CTRL

Name	Offset	Size	Reset Value	Description
DSC_SYS_CTRL_DSC_8K_SYS_CTRL	0x0000	W	0x00000000	DSC 8K general control

Name	Offset	Size	Reset Value	Description
DSC_SYS_CTRL_DSC_8K_RST	0x0004	W	0x00000000	DSC 8K power on reset
DSC_SYS_CTRL_DSC_8K_CFG_DONE	0x0008	W	0x00000000	DSC 8K configure done flag
DSC_SYS_CTRL_DSC_8K_INIT_DLY_NUM	0x000C	W	0x00000000	DSC 8K initialized delay number
DSC_SYS_CTRL_DSC_8K_HTOTAL_HS_END	0x0010	W	0x00000000	DSC 8K H timing control 0
DSC_SYS_CTRL_DSC_8K_HACT_ST_END	0x0014	W	0x00000000	DSC 8K H timing control 1
DSC_SYS_CTRL_DSC_8K_VTOTAL_VS_END	0x0018	W	0x00000000	DSC 8K V timing control 0
DSC_SYS_CTRL_DSC_8K_VACT_ST_END	0x001C	W	0x00000000	DSC 8K V timing control 1
DSC_SYS_CTRL_DSC_8K_STATUS	0x0020	W	0x00000000	DSC 8K Error Status
DSC_SYS_CTRL_DSC_8K_DEBUG_0	0x0024	W	0x00000000	DSC 8K Debug Status 0
DSC_SYS_CTRL_DSC_8K_DEBUG_1	0x0028	W	0x00000000	DSC 8K Debug Status 1
DSC_SYS_CTRL_DSC_8K_DEBUG_2	0x002C	W	0x00000000	DSC 8K Debug Status 2
DSC_SYS_CTRL_DSC_4K_SYS_CTRL	0x0030	W	0x00000000	DSC 4K general control
DSC_SYS_CTRL_DSC_4K_RST	0x0034	W	0x00000000	DSC 4K power on reset
DSC_SYS_CTRL_DSC_4K_CFG_DONE	0x0038	W	0x00000000	DSC 4K configure done flag
DSC_SYS_CTRL_DSC_4K_INIT_DLY_NUM	0x003C	W	0x00000000	DSC 4K initialized delay number
DSC_SYS_CTRL_DSC_4K_HTOTAL_HS_END	0x0040	W	0x00000000	DSC 4K H timing control 0
DSC_SYS_CTRL_DSC_4K_HACT_ST_END	0x0044	W	0x00000000	DSC 4K H timing control 1
DSC_SYS_CTRL_DSC_4K_VTOTAL_VS_END	0x0048	W	0x00000000	DSC 4K V timing control 0
DSC_SYS_CTRL_DSC_4K_VACT_ST_END	0x004C	W	0x00000000	DSC 4K V timing control 1
DSC_SYS_CTRL_DSC_4K_STATUS	0x0050	W	0x00000000	DSC 4K Error Status
DSC_SYS_CTRL_DSC_4K_DEBUG_0	0x0054	W	0x00000000	DSC 4K Debug Status 0
DSC_SYS_CTRL_DSC_4K_DEBUG_1	0x0058	W	0x00000000	DSC 4K Debug Status 1
DSC_SYS_CTRL_DSC_4K_DEBUG_2	0x005C	W	0x00000000	DSC 4K Debug Status 2

7.5.2.3 OVERLAY

Name	Offset	Size	Reset Value	Description
VOP2_OVERLAY_CTRL	0x0000	W	0x00000000	OVERLAY control register
VOP2_OVERLAY_LAYER_SEL	0x0004	W	0x76543210	OVERLAY layer select

Name	Offset	Size	Reset Value	Description
VOP2_OVERLAY_PORT_SEL	0x0008	W	0xA0507753	OVERLAY port select
VOP2_OVERLAY_RESERVED_LUT_MST	0x000C	W	0x00000000	RESERVED LUT start address
VOP2_OVERLAY_CLUSTER0_MIX_SRC_COLOR_CTRL	0x0010	W	0x00000000	To configure the source color of cluster0 MIX
VOP2_OVERLAY_CLUSTER0_MIX_DST_COLOR_CTRL	0x0014	W	0x00000000	To configure the destination color of cluster0 MIX
VOP2_OVERLAY_CLUSTER0_MIX_SRC_ALPHA_CTRL	0x0018	W	0x00000000	To configure the source alpha of cluster0 MIX
VOP2_OVERLAY_CLUSTER0_MIX_DST_ALPHA_CTRL	0x001C	W	0x00000000	To configure the destination alpha of cluster0 MIX
VOP2_OVERLAY_CLUSTER1_MIX_SRC_COLOR_CTRL	0x0020	W	0x00000000	To configure the source color of cluster1 MIX
VOP2_OVERLAY_CLUSTER1_MIX_DST_COLOR_CTRL	0x0024	W	0x00000000	To configure the destination color of cluster1 MIX
VOP2_OVERLAY_CLUSTER1_MIX_SRC_ALPHA_CTRL	0x0028	W	0x00000000	To configure the source alpha of cluster1 MIX
VOP2_OVERLAY_CLUSTER1_MIX_DST_ALPHA_CTRL	0x002C	W	0x00000000	To configure the destination alpha of cluster1 MIX
VOP2_OVERLAY_CLUSTER2_MIX_SRC_COLOR_CTRL	0x0030	W	0x00000000	To configure the source color of cluster2 MIX
VOP2_OVERLAY_CLUSTER2_MIX_DST_COLOR_CTRL	0x0034	W	0x00000000	To configure the destination color of cluster2 MIX
VOP2_OVERLAY_CLUSTER2_MIX_SRC_ALPHA_CTRL	0x0038	W	0x00000000	To configure the source alpha of cluster2 MIX
VOP2_OVERLAY_CLUSTER2_MIX_DST_ALPHA_CTRL	0x003C	W	0x00000000	To configure the destination alpha of cluster2 MIX
VOP2_OVERLAY_CLUSTER3_MIX_SRC_COLOR_CTRL	0x0040	W	0x00000000	To configure the source color of cluster3 MIX
VOP2_OVERLAY_CLUSTER3_MIX_DST_COLOR_CTRL	0x0044	W	0x00000000	To configure the destination color of cluster3 MIX
VOP2_OVERLAY_CLUSTER3_MIX_SRC_ALPHA_CTRL	0x0048	W	0x00000000	To configure the source alpha of cluster3 MIX
VOP2_OVERLAY_CLUSTER3_MIX_DST_ALPHA_CTRL	0x004C	W	0x00000000	To configure the destination alpha of cluster3 MIX
VOP2_OVERLAY_MIX0_SRC_COLOR_CTRL	0x0050	W	0x00000000	To configure the source color of MIX0
VOP2_OVERLAY_MIX0_DST_COLOR_CTRL	0x0054	W	0x00000000	To configure the destination color of MIX0
VOP2_OVERLAY_MIX0_SRC_ALPHA_CTRL	0x0058	W	0x00000000	To configure the source alpha of MIX0
VOP2_OVERLAY_MIX0_DST_ALPHA_CTRL	0x005C	W	0x00000000	To configure the destination alpha of MIX0
VOP2_OVERLAY_MIX1_SRC_COLOR_CTRL	0x0060	W	0x00000000	To configure the source color of MIX1
VOP2_OVERLAY_MIX1_DST_COLOR_CTRL	0x0064	W	0x00000000	To configure the destination color of MIX1
VOP2_OVERLAY_MIX1_SRC_ALPHA_CTRL	0x0068	W	0x00000000	To configure the source alpha of MIX1
VOP2_OVERLAY_MIX1_DST_ALPHA_CTRL	0x006C	W	0x00000000	To configure the destination alpha of MIX1

Name	Offset	Size	Reset Value	Description
VOP2_OVERLAY_MIX2_SRC_COLOR_CTRL	0x0070	W	0x00000000	To configure the source color of MIX2
VOP2_OVERLAY_MIX2_DST_COLOR_CTRL	0x0074	W	0x00000000	To configure the destination color of MIX2
VOP2_OVERLAY_MIX2_SRC_ALPHA_CTRL	0x0078	W	0x00000000	To configure the source alpha of MIX2
VOP2_OVERLAY_MIX2_DST_ALPHA_CTRL	0x007C	W	0x00000000	To configure the destination alpha of MIX2
VOP2_OVERLAY_MIX3_SRC_COLOR_CTRL	0x0080	W	0x00000000	To configure the source color of MIX3
VOP2_OVERLAY_MIX3_DST_COLOR_CTRL	0x0084	W	0x00000000	To configure the destination color of MIX3
VOP2_OVERLAY_MIX3_SRC_ALPHA_CTRL	0x0088	W	0x00000000	To configure the source alpha of MIX3
VOP2_OVERLAY_MIX3_DST_ALPHA_CTRL	0x008C	W	0x00000000	To configure the destination alpha of MIX3
VOP2_OVERLAY_MIX4_SRC_COLOR_CTRL	0x0090	W	0x00000000	To configure the source color of MIX4
VOP2_OVERLAY_MIX4_DST_COLOR_CTRL	0x0094	W	0x00000000	To configure the destination color of MIX4
VOP2_OVERLAY_MIX4_SRC_ALPHA_CTRL	0x0098	W	0x00000000	To configure the source alpha of MIX4
VOP2_OVERLAY_MIX4_DST_ALPHA_CTRL	0x009C	W	0x00000000	To configure the destination alpha of MIX4
VOP2_OVERLAY_MIX5_SRC_COLOR_CTRL	0x00A0	W	0x00000000	To configure the source color of MIX5
VOP2_OVERLAY_MIX5_DST_COLOR_CTRL	0x00A4	W	0x00000000	To configure the destination color of MIX5
VOP2_OVERLAY_MIX5_SRC_ALPHA_CTRL	0x00A8	W	0x00000000	To configure the source alpha of MIX5
VOP2_OVERLAY_MIX5_DST_ALPHA_CTRL	0x00AC	W	0x00000000	To configure the destination alpha of MIX5
VOP2_OVERLAY_MIX6_SRC_COLOR_CTRL	0x00B0	W	0x00000000	To configure the source color of MIX6
VOP2_OVERLAY_MIX6_DST_COLOR_CTRL	0x00B4	W	0x00000000	To configure the destination color of MIX6
VOP2_OVERLAY_MIX6_SRC_ALPHA_CTRL	0x00B8	W	0x00000000	To configure the source alpha of MIX6
VOP2_OVERLAY_MIX6_DST_ALPHA_CTRL	0x00BC	W	0x00000000	To configure the destination alpha of MIX6
VOP2_OVERLAY_HDR0_MIX_SRC_COLOR_CTRL	0x00C0	W	0x00000000	To configure the source color of HDR0 MIX
VOP2_OVERLAY_HDR0_MIX_DST_COLOR_CTRL	0x00C4	W	0x00000000	To configure the destination color of HDR0 MIX
VOP2_OVERLAY_HDR0_MIX_SRC_ALPHA_CTRL	0x00C8	W	0x00000000	To configure the source alpha of HDR0 MIX
VOP2_OVERLAY_HDR0_MIX_DST_ALPHA_CTRL	0x00CC	W	0x00000000	To configure the destination alpha of HDR0 MIX
VOP2_OVERLAY_HDR1_MIX_SRC_COLOR_CTRL	0x00D0	W	0x00000000	To configure the source color of HDR1 MIX
VOP2_OVERLAY_HDR1_MIX_DST_COLOR_CTRL	0x00D4	W	0x00000000	To configure the destination color of HDR1 MIX

Name	Offset	Size	Reset Value	Description
VOP2_OVERLAY_HDR1_MIX_SRC_ALPHA_CTRL	0x00D8	W	0x00000000	To configure the source alpha of HDR1 MIX
VOP2_OVERLAY_HDR1_MIX_DST_ALPHA_CTRL	0x00DC	W	0x00000000	To configure the destination alpha of HDR1 MIX
VOP2_OVERLAY_DP0_BG_MIX_CTRL	0x00E0	W	0x2D000000	To control the background MIX of video output0
VOP2_OVERLAY_DP1_BG_MIX_CTRL	0x00E4	W	0x31000000	To control the background MIX of video output1
VOP2_OVERLAY_DP2_BG_MIX_CTRL	0x00E8	W	0x33000000	To control the background MIX of video output2
VOP2_OVERLAY_DP3_BG_MIX_CTRL	0x00EC	W	0x33000000	To control the background MIX of video output2
VOP2_OVERLAY_Cluster_DLY_NUM0	0x00F0	W	0x04040404	To configure the delay cycle of cluster
VOP2_OVERLAY_Cluster_DLY_NUM1	0x00F4	W	0x04040404	To configure the delay cycle of cluster
VOP2_OVERLAY_SMART_DLY_NUM	0x00F8	W	0x17171717	To configure the delay cycle of esmart

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.5.2.4 POST0/1/2/3

Name	Offset	Size	Reset Value	Description
VOP2_POST0_DSP_CTRL	0x0000	W	0x8000000F	To control the display mode of video output port
VOP2_POST0_DUAL_DISPLAY_CTRL	0x0004	W	0x00000000	To control dual channel mode
VOP2_POST0_COLOR_CTRL	0x0008	W	0x00000000	To control color bar
VOP2_POST0_CLK_CTRL	0x000C	W	0x00000000	Clock control
VOP2_POST0_3D_LUT_CTRL	0x0010	W	0x00000000	To control 3D LUT
VOP2_POST0_3D_LUT_R	0x0014	W	0x00000000	To configure the red component of 3D LUT
VOP2_POST0_3D_LUT_G	0x0018	W	0x00000000	To configure the green component of 3D LUT
VOP2_POST0_3D_LUT_B	0x001C	W	0x00000000	To configure the blue component of 3D LUT
VOP2_POST0_3DLUT_MST	0x0020	W	0x00000000	To configure the starting address of 3D LUT in memory
VOP2_POST0_DSP_BG	0x002C	W	0x00000000	To configure the background color of video output port
VOP2_POST0_PRE_SCAN_HTIMING0	0x0030	W	0x00000000	To configure the pre-process timing of video output port
VOP2_POST0_PRE_SCAN_TIMING1	0x0034	W	0x00000000	To configure the post-process horizontal timing of video output port
VOP2_POST0_PRE_SCAN_TIMING2	0x0038	W	0x00000000	To configure the post-process vertical timing of video output port
VOP2_POST0_PRE_SCAN_TIMING3	0x003C	W	0x00000000	To configure the post-process vertical timing of video output port

Name	Offset	Size	Reset Value	Description
VOP2_POST0_DSP_VACT_INFO_F1	0x0044	W	0x00000000	To configure the interlace vertical timing of video output port
VOP2_POST0_DSP_HTOTAL_HS_END	0x0048	W	0x00000000	To configure the horizontal timing of video output port
VOP2_POST0_DSP_HACT_ST_END	0x004C	W	0x00000000	To configure the horizontal timing of video output port
VOP2_POST0_DSP_VTOTAL_VS_END	0x0050	W	0x00000000	To configure the vertical timing of video output port
VOP2_POST0_DSP_VACT_ST_END	0x0054	W	0x00000000	To configure the vertical timing of video output port
VOP2_POST0_DSP_VS_ST_END_F1	0x0058	W	0x00000000	To configure the interlace vertical timing of video output port
VOP2_POST0_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	To configure the interlace vertical timing of video output port
VOP2_POST0_BCSH_CTRL	0x0060	W	0x00000000	To control BCSH
VOP2_POST0_BCSH_BCS	0x0064	W	0x00000000	To configure the brightness, contrast, sat and output mode of BCSH
VOP2_POST0_BCSH_H	0x0068	W	0x00000000	To configure the hue of BCSH
VOP2_POST0_BCSH_COLOR_BAR	0x006C	W	0x00000000	To enable BCSH
VOP2_POST0_FRC_LOWER01_0	0x00A0	W	0x12844821	To configure the filter coefficients of FRC
VOP2_POST0_FRC_LOWER01_1	0x00A4	W	0x21488412	To configure the filter coefficients of FRC
VOP2_POST0_FRC_LOWER10_0	0x00A8	W	0xA55A9696	To configure the filter coefficients of FRC
VOP2_POST0_FRC_LOWER10_1	0x00AC	W	0x5AA56969	To configure the filter coefficients of FRC
VOP2_POST0_FRC_LOWER11_0	0x00B0	W	0xDEB77BED	To configure the filter coefficients of FRC
VOP2_POST0_FRC_LOWER11_1	0x00B4	W	0xED7BB7DE	To configure the filter coefficients of FRC

7.5.2.5 CLUSTER0/1/2/3

Name	Offset	Size	Reset Value	Description
VOP2_CLUSTER0_WIN0_CTRL0	0x0000	W	0x00000000	WIN0 control register0
VOP2_CLUSTER0_WIN0_CTRL1	0x0004	W	0x00000000	WIN0 control register1
VOP2_CLUSTER0_WIN0_CTRL2	0x0008	W	0x00000000	WIN0 control register2
VOP2_CLUSTER0_WIN0_YRGB_MST	0x0010	W	0x00000000	WIN0 YRGB memory starting
VOP2_CLUSTER0_WIN0_CBCR_MST	0x0014	W	0x00000000	WIN0 YRGB memory starting
VOP2_CLUSTER0_WIN0_VIR	0x0018	W	0x00000000	WIN0 virtual width
VOP2_CLUSTER0_WIN0_ACT_INFO	0x0020	W	0x00000000	WIN0 actual information
VOP2_CLUSTER0_WIN0_DSP_INFO	0x0024	W	0x00000000	WIN0 display information

Name	Offset	Size	Reset Value	Description
VOP2_CLUSTER0_WIN0_DSP_ST	0x0028	W	0x00000000	WIN0 display start
VOP2_CLUSTER0_WIN0_DSP_BG	0x002C	W	0x00000000	WIN0 display background
VOP2_CLUSTER0_WIN0_SCL_FACTOR_YRGB	0x0030	W	0x00000000	WIN0 yrgb scale factor
VOP2_CLUSTER0_WIN0_SCL_OFFSET	0x0038	W	0x00000000	WIN0 scale offset
VOP2_CLUSTER0_WIN0_TRANSFORMED_OFFSET	0x003C	W	0x00000000	WIN0 transform offset
VOP2_CLUSTER0_WIN0_AFBCD_OUTPUT_CTRL	0x0050	W	0x00000000	WIN0 AFBCD control register
VOP2_CLUSTER0_WIN0_AFBCD_MODE	0x0054	W	0x00000000	WIN0 AFBCD mode
VOP2_CLUSTER0_WIN0_AFBCD_HDR_PTR	0x0058	W	0x00000000	WIN0 AFBCD HDR pointer
VOP2_CLUSTER0_WIN0_AFBCD_VIR_WIDTH	0x005C	W	0x00000000	WIN0 AFBCD virtual width
VOP2_CLUSTER0_WIN0_AFBCD_SIZE	0x0060	W	0x00000000	WIN0 AFBCD size
VOP2_CLUSTER0_WIN0_AFBCD_PIC_OFFSET	0x0064	W	0x00000000	WIN0 AFBCD picture offset
VOP2_CLUSTER0_WIN0_AFBCD_DIS_OFFSET	0x0068	W	0x00000000	WIN0 AFBCD display offset
VOP2_CLUSTER0_WIN0_AFBCD_CTRL	0x006C	W	0x00000000	WIN0 AFBCD control
VOP2_CLUSTER0_WIN1_CTRL0	0x0080	W	0x00000000	WIN1 control register0
VOP2_CLUSTER0_WIN1_CTRL1	0x0084	W	0x00000000	WIN1 control register1
VOP2_CLUSTER0_WIN1_CTRL2	0x0088	W	0x00000000	WIN1 control register2
VOP2_CLUSTER0_WIN1_YRGB_MST	0x0090	W	0x00000000	WIN1 YRGB memory starting
VOP2_CLUSTER0_WIN1_CBCR_MST	0x0094	W	0x00000000	WIN1 YRGB memory starting
VOP2_CLUSTER0_WIN1_VIR	0x0098	W	0x00000000	WIN1 virtual width
VOP2_CLUSTER0_WIN1_ACT_INFO	0x00A0	W	0x00000000	WIN1 actual information
VOP2_CLUSTER0_WIN1_DSP_INFO	0x00A4	W	0x00000000	WIN1 display information
VOP2_CLUSTER0_WIN1_DSP_ST	0x00A8	W	0x00000000	WIN1 display start
VOP2_CLUSTER0_WIN1_DSP_BG	0x00AC	W	0x00000000	WIN1 display background
VOP2_CLUSTER0_WIN1_SCL_FACTOR_YRGB	0x00B0	W	0x00000000	WIN1 yrgb scale factor
VOP2_CLUSTER0_WIN1_SCL_OFFSET	0x00B8	W	0x00000000	WIN1 scale offset
VOP2_CLUSTER0_WIN1_TRANSFORMED_OFFSET	0x00BC	W	0x00000000	WIN1 transform offset

Name	Offset	Size	Reset Value	Description
VOP2_CLUSTER0_WIN1_AFBCD_OUTPUT_CTRL	0x00D0	W	0x00000000	WIN0 AFBCD control register
VOP2_CLUSTER0_WIN1_AFBCD_MODE	0x00D4	W	0x00000000	WIN0 AFBCD mode
VOP2_CLUSTER0_WIN1_AFBCD_HDR_PTR	0x00D8	W	0x00000000	WIN0 AFBCD HDR pointer
VOP2_CLUSTER0_WIN1_AFBCD_VIR_WIDTH	0x00DC	W	0x00000000	WIN0 AFBCD virtual width
VOP2_CLUSTER0_WIN1_AFBCD_SIZE	0x00E0	W	0x00000000	WIN0 AFBCD size
VOP2_CLUSTER0_WIN1_AFBCD_PIC_OFFSET	0x00E4	W	0x00000000	WIN0 AFBCD picture offset
VOP2_CLUSTER0_WIN1_AFBCD_DIS_OFFSET	0x00E8	W	0x00000000	WIN0 AFBCD display offset
VOP2_CLUSTER0_WIN1_AFBCD_CTRL	0x00EC	W	0x00000000	WIN0 AFBCD control
VOP2_CLUSTER0_CTRL	0x0100	W	0x00000000	CLUSTER control register
VOP2_CLUSTER0_LG_COE0	0x0110	W	0x00000000	CLUSTER low gauss coefficient
VOP2_CLUSTER0_LG_COE1	0x0114	W	0x00000000	CLUSTER low gauss coefficient
VOP2_CLUSTER0_LG_COE2	0x0118	W	0x00000000	CLUSTER low gauss coefficient
VOP2_CLUSTER0_HG_COE0	0x0120	W	0x00000000	CLUSTER high gauss coefficient
VOP2_CLUSTER0_HG_COE1	0x0124	W	0x00000000	CLUSTER high gauss coefficient
VOP2_CLUSTER0_HG_COE2	0x0128	W	0x00000000	CLUSTER high gauss coefficient

7.5.2.6 ESMART0/1/2/3

Name	Offset	Size	Reset Value	Description
VOP2_ESMART0_CTRL0	0x0000	W	0x00000000	To enable the color space conversion of esmart
VOP2_ESMART0_CTRL1	0x0004	W	0x0330B0AC	To control the DMA of esmart
VOP2_ESMART0_AXI_CTRL	0x0008	W	0x00000000	To Control AXI parameter
VOP2_ESMART0_REGION0_MST_CTL	0x0010	W	0x00000000	To enable the region0 of esmart
VOP2_ESMART0_REGION0_MST_YRGB	0x0014	W	0x00000000	To configure the starting address of YRGB in memory
VOP2_ESMART0_REGION0_MST_CBCR	0x0018	W	0x00000000	To configure the starting address of CBCR in memory
VOP2_ESMART0_REGION0_VIR	0x001C	W	0x00000000	To configure the virtual width of data in memory
VOP2_ESMART0_REGION0_ACT_INFO	0x0020	W	0x00000000	To configure the active size of data
VOP2_ESMART0_REGION0_DSP_INFO	0x0024	W	0x00000000	To configure the display size of data
VOP2_ESMART0_REGION0_DSP_OFFSET	0x0028	W	0x00000000	To configure the display offset of data

Name	Offset	Size	Reset Value	Description
VOP2_ESMART0_REGION0_SCL_CTRL	0x0030	W	0x00000000	To enable the scaling of esmart
VOP2_ESMART0_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	To configure the scaling factor of YRGB
VOP2_ESMART0_REGION0_SCL_FACTOR_CBCR	0x0038	W	0x10001000	To configure the scaling factor of CBCR
VOP2_ESMART0_REGION0_SCL_OFFSET	0x003C	W	0x00000000	To configure the scaling offset of esmart
VOP2_ESMART0_REGION1_MST_CTL	0x0040	W	0x00000000	To enable the region1 of esmart
VOP2_ESMART0_REGION1_MST_YRGB	0x0044	W	0x00000000	To configure the starting address of YRGB in memory
VOP2_ESMART0_REGION1_MST_CBCR	0x0048	W	0x00000000	To configure the starting address of CBCR in memory
VOP2_ESMART0_REGION1_VIR	0x004C	W	0x00000000	To configure the virtual width of data in memory
VOP2_ESMART0_REGION1_ACT_INFO	0x0050	W	0x00000000	To configure the active size of data
VOP2_ESMART0_REGION1_DSP_INFO	0x0054	W	0x00000000	To configure the display size of data
VOP2_ESMART0_REGION1_DSP_OFFSET	0x0058	W	0x00000000	To configure the display offset of data
VOP2_ESMART0_REGION1_SCL_CTRL	0x0060	W	0x00000000	To enable the scaling of esmart
VOP2_ESMART0_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	To configure the scaling factor of YRGB
VOP2_ESMART0_REGION1_SCL_FACTOR_CBCR	0x0068	W	0x10001000	To configure the scaling factor of CBCR
VOP2_ESMART0_REGION1_SCL_OFFSET	0x006C	W	0x00000000	To configure the scaling offset of esmart
VOP2_ESMART0_REGION2_MST_CTL	0x0070	W	0x00000000	To enable the region2 of esmart
VOP2_ESMART0_REGION2_MST_YRGB	0x0074	W	0x00000000	To configure the starting address of YRGB in memory
VOP2_ESMART0_REGION2_MST_CBCR	0x0078	W	0x00000000	To configure the starting address of CBCR in memory
VOP2_ESMART0_REGION2_VIR	0x007C	W	0x00000000	To configure the virtual width of data in memory
VOP2_ESMART0_REGION2_ACT_INFO	0x0080	W	0x00000000	To configure the active size of data
VOP2_ESMART0_REGION2_DSP_INFO	0x0084	W	0x00000000	To configure the display size of data
VOP2_ESMART0_REGION2_DSP_OFFSET	0x0088	W	0x00000000	To configure the display offset of data
VOP2_ESMART0_REGION2_SCL_CTRL	0x0090	W	0x00000000	To enable the scaling of esmart
VOP2_ESMART0_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	To configure the scaling factor of YRGB
VOP2_ESMART0_REGION2_SCL_FACTOR_CBCR	0x0098	W	0x10001000	To configure the scaling factor of CBCR
VOP2_ESMART0_REGION2_SCL_OFFSET	0x009C	W	0x00000000	To configure the scaling offset of esmart

Name	Offset	Size	Reset Value	Description
VOP2_ESMART0_REGION3_MST_CTL	0x00A0	W	0x00000000	To enable the region3 of esmart
VOP2_ESMART0_REGION3_MST_YRGB	0x00A4	W	0x00000000	To configure the starting address of YRGB in memory
VOP2_ESMART0_REGION3_MST_CBCR	0x00A8	W	0x00000000	To configure the starting address of CBCR in memory
VOP2_ESMART0_REGION3_VIR	0x00AC	W	0x00000000	To configure the virtual width of data in memory
VOP2_ESMART0_REGION3_ACT_INFO	0x00B0	W	0x00000000	To configure the active size of data
VOP2_ESMART0_REGION3_DSP_INFO	0x00B4	W	0x00000000	To configure the display size of data
VOP2_ESMART0_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	To configure the display offset of data
VOP2_ESMART0_REGION3_SCL_CTRL	0x00C0	W	0x00000000	To enable the scaling of esmart
VOP2_ESMART0_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	To configure the scaling factor of YRGB
VOP2_ESMART0_REGION3_SCL_FACTOR_CBCR	0x00C8	W	0x10001000	To configure the scaling factor of CBCR
VOP2_ESMART0_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	To configure the scaling offset of esmart
VOP2_ESMART0_KEY_CTRL	0x00D0	W	0x00000000	To configure the color key of esmart
VOP2_ESMART0_BG_EN	0x00D4	W	0x00000000	To enable the background of esmart

7.5.2.7 HDR10

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_HDR10_LUT_CTRL	0x0000	W	0x00000000	To control the fetching of HDR10 LUT.
VOP2_HDR10_HDR10_LUT_MST	0x0004	W	0x00000000	To control the fetching of HDR10 LUT.
VOP2_HDR10_SDR2HDR_CTRL	0x0010	W	0x00000000	To enable the SDR2HDR of HDR10.
VOP2_HDR10_SDR2HDR_CTRL1	0x0018	W	0x00000000	To enable the SDR2HDR of HDR10.
VOP2_HDR10_HDR2SDR_CTRL1	0x001C	W	0x00000000	To enable the HDR2SDR of HDR10.
VOP2_HDR10_HDR2SDR_CTRL	0x0020	W	0x00000000	To enable the HDR2SDR of HDR10.
VOP2_HDR10_HDR2SDR_SRC_RANGE	0x0024	W	0x00000000	To configure the source luminance of HDR10.
VOP2_HDR10_HDR2SDR_NORFACEETF	0x0028	W	0x00000000	To configure the normalized factor of EETF.
VOP2_HDR10_HDR2SDR_DST_RANGE	0x002C	W	0x00000000	To configure the destination luminance of HDR10.
VOP2_HDR10_HDR2SDR_NORMFACCGAMMA	0x0030	W	0x00000000	To configure the normalized factor of GAMMA.
VOP2_HDR10_EETF_OETF_0	0x003C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_EETF_OETF 1	0x0040	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 2	0x0044	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 3	0x0048	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 4	0x004C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 5	0x0050	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 6	0x0054	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 7	0x0058	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 8	0x005C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 9	0x0060	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 10	0x0064	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 11	0x0068	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 12	0x006C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 13	0x0070	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 14	0x0074	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 15	0x0078	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 16	0x007C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 17	0x0080	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 18	0x0084	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 19	0x0088	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 20	0x008C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 21	0x0090	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 22	0x0094	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 23	0x0098	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 24	0x009C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 25	0x00A0	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF 26	0x00A4	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_EETF_OETF27	0x00A8	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF28	0x00AC	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF29	0x00B0	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF30	0x00B4	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF31	0x00B8	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_EETF_OETF32	0x00BC	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_HDR10_SAT_Y0	0x00C0	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y1	0x00C4	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y2	0x00C8	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y3	0x00CC	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y4	0x00D0	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y5	0x00D4	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y6	0x00D8	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y7	0x00DC	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_SAT_Y8	0x00E0	W	0x00000000	To configure the Y value of square root curve.
VOP2_HDR10_EOTF_OETF_Y0	0x00F0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y1	0x00F4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y2	0x00F8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y3	0x00FC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y4	0x0100	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y5	0x0104	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y6	0x0108	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y7	0x010C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_EOTF_OETF_Y8	0x0110	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y9	0x0114	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y10	0x0118	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y11	0x011C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y12	0x0120	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y13	0x0124	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y14	0x0128	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y15	0x012C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y16	0x0130	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y17	0x0134	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y18	0x0138	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y19	0x013C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y20	0x0140	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y21	0x0144	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y22	0x0148	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y23	0x014C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y24	0x0150	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y25	0x0154	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_EOTF_OETF_Y26	0x0158	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y27	0x015C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y28	0x0160	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y29	0x0164	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y30	0x0168	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y31	0x016C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y32	0x0170	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y33	0x0174	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y34	0x0178	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y35	0x017C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y36	0x0180	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y37	0x0184	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y38	0x0188	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y39	0x018C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y40	0x0190	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y41	0x0194	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y42	0x0198	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y43	0x019C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_EOTF_OETF_Y44	0x01A0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y45	0x01A4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y46	0x01A8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y47	0x01AC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y48	0x01B0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y49	0x01B4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y50	0x01B8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y51	0x01BC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y52	0x01C0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y53	0x01C4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y54	0x01C8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y55	0x01CC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y56	0x01D0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y57	0x01D4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y58	0x01D8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y59	0x01DC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y60	0x01E0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y61	0x01E4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_EOTF_OETF_Y62	0x01E8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y63	0x01EC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_EOTF_OETF_Y64	0x01F0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW1	0x0200	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW2	0x0204	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW3	0x0208	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW4	0x020C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW5	0x0210	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW6	0x0214	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW7	0x0218	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW8	0x021C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW9	0x0220	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW10	0x0224	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW11	0x0228	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW12	0x022C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW13	0x0230	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW14	0x0234	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW15	0x0238	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW16	0x023C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW17	0x0240	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW18	0x0244	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW19	0x0248	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW20	0x024C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW21	0x0250	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW22	0x0254	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_OETF_DX_DXPOW23	0x0258	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW24	0x025C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW25	0x0260	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW26	0x0264	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW27	0x0268	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW28	0x026C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW29	0x0270	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW30	0x0274	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW31	0x0278	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW32	0x027C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW33	0x0280	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW34	0x0284	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW35	0x0288	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW36	0x028C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW37	0x0290	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW38	0x0294	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW39	0x0298	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW40	0x029C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW41	0x02A0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW42	0x02A4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW43	0x02A8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW44	0x02AC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW45	0x02B0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW46	0x02B4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW47	0x02B8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW48	0x02BC	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_OETF_DX_DXPOW49	0x02C0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW50	0x02C4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW51	0x02C8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW52	0x02CC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW53	0x02D0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW54	0x02D4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW55	0x02D8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW56	0x02DC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW57	0x02E0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW58	0x02E4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW59	0x02E8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW60	0x02EC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW61	0x02F0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW62	0x02F4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW63	0x02F8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_DX_DXPOW64	0x02FC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN1	0x0300	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN2	0x0304	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN3	0x0308	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN4	0x030C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN5	0x0310	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN6	0x0314	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN7	0x0318	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN8	0x031C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN9	0x0320	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN10	0x0324	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_OETF_XN11	0x0328	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN12	0x032C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN13	0x0330	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN14	0x0334	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN15	0x0338	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN16	0x033C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN17	0x0340	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN18	0x0344	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN19	0x0348	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN20	0x034C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN21	0x0350	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN22	0x0354	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN23	0x0358	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN24	0x035C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN25	0x0360	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN26	0x0364	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN27	0x0368	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN28	0x036C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN29	0x0370	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN30	0x0374	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN31	0x0378	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN32	0x037C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN33	0x0380	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN34	0x0384	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN35	0x0388	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN36	0x038C	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_OETF_XN37	0x0390	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN38	0x0394	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN39	0x0398	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN40	0x039C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN41	0x03A0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN42	0x03A4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN43	0x03A8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN44	0x03AC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN45	0x03B0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN46	0x03B4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN47	0x03B8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN48	0x03BC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN49	0x03C0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN50	0x03C4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN51	0x03C8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN52	0x03CC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN53	0x03D0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN54	0x03D4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN55	0x03D8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN56	0x03DC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN57	0x03E0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN58	0x03E4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN59	0x03E8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN60	0x03EC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN61	0x03F0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_HDR10_OETF_XN62	0x03F4	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_OETF_XN63	0x03F8	W	0x00000000	To configure the X value of ST2048_OETF curve.

7.5.2.8 DSC_8K

Name	Offset	Size	Reset Value	Description
DSC_8K_PPS0_3	0x0000	W	0xAB000012	PPS0_3
DSC_8K_PPS4_7	0x0004	W	0xE0106030	PPS4_7
DSC_8K_PPS8_11	0x0008	W	0xE010001E	PPS8_11
DSC_8K_PPS12_15	0x000C	W	0x8016001E	PPS12_15
DSC_8K_PPS16_19	0x0010	W	0x00B4AA02	PPS16_19
DSC_8K_PPS20_23	0x0014	W	0x20012000	PPS20_23
DSC_8K_PPS24_27	0x0018	W	0x0F000100	PPS24_27
DSC_8K_PPS28_31	0x001C	W	0x140DE701	PPS28_31
DSC_8K_PPS32_35	0x0020	W	0xFE100018	PPS32_35
DSC_8K_PPS36_39	0x0024	W	0x00200C03	PPS36_39
DSC_8K_PPS40_43	0x0028	W	0x330B0B06	PPS40_43
DSC_8K_PPS44_47	0x002C	W	0x382A1C0E	PPS44_47
DSC_8K_PPS48_51	0x0030	W	0x69625446	PPS48_51
DSC_8K_PPS52_55	0x0034	W	0x7B797770	PPS52_55
DSC_8K_PPS56_59	0x0038	W	0x00007E7D	PPS56_59
DSC_8K_PPS60_63	0x003C	W	0x00000000	PPS60_63
DSC_8K_PPS64_67	0x0040	W	0x00000000	PPS60_63
DSC_8K_PPS68_71	0x0044	W	0x00000000	PPS60_63
DSC_8K_PPS72_75	0x0048	W	0x00000000	PPS60_63
DSC_8K_PPS76_79	0x004C	W	0x00000000	PPS60_63
DSC_8K_PPS80_83	0x0050	W	0x00000000	PPS60_63
DSC_8K_PPS84_87	0x0054	W	0x00000000	PPS60_63
DSC_8K_PPS88_91	0x0058	W	0x00000000	PPS88_91
DSC_8K_PPS92_95	0x005C	W	0x00000000	PPS92_95
DSC_8K_VERSION	0x0080	W	0x10000110	VERSION
DSC_8K_CFG_REG0	0x0084	W	0x58120BA1	Configuration 0
DSC_8K_CFG_REG1	0x0088	W	0x1E0010E0	Configuration 1
DSC_8K_CFG_REG2	0x008C	W	0x000010E0	Configuration 2
DSC_8K_CFG_REG3	0x0090	W	0x1E0010E0	Configuration 3
DSC_8K_CTRL0	0x00A0	W	0x20000010	Control 0
DSC_8K_CTRL1	0x00A4	W	0x00100000	Control 1
DSC_8K_STS0	0x00A8	W	0x000000FF	Status 0
DSC_8K_STS1	0x00AC	W	0x000000FF	Status 1
DSC_8K_STS2	0x00B0	W	0x000000FF	Status 2
DSC_8K_STS3	0x00B4	W	0x000000FF	Status 3
DSC_8K_STS4	0x00B8	W	0x000000FF	Status 4
DSC_8K_STS5	0x00BC	W	0x000000FF	Status 5
DSC_8K_ERS	0x00C4	W	0xFFFFFFFF	Error status

7.5.2.9 DSC_4K

Name	Offset	Size	Reset Value	Description
DSC_4K_PPS0_3	0x0000	W	0xAB000012	PPS0_3
DSC_4K_PPS4_7	0x0004	W	0x70086030	PPS4_7
DSC_4K_PPS8_11	0x0008	W	0x70080010	PPS8_11
DSC_4K_PPS12_15	0x000C	W	0x000C0010	PPS12_15

Name	Offset	Size	Reset Value	Description
DSC_4K_PPS16_19	0x0010	W	0x0060AA02	PPS16_19
DSC_4K_PPS20_23	0x0014	W	0x20012000	PPS20_23
DSC_4K_PPS24_27	0x0018	W	0x0F000100	PPS24_27
DSC_4K_PPS28_31	0x001C	W	0x140DE701	PPS28_31
DSC_4K_PPS32_35	0x0020	W	0xFE100018	PPS32_35
DSC_4K_PPS36_39	0x0024	W	0x00200C03	PPS36_39
DSC_4K_PPS40_43	0x0028	W	0x330B0B06	PPS40_43
DSC_4K_PPS44_47	0x002C	W	0x382A1C0E	PPS44_47
DSC_4K_PPS48_51	0x0030	W	0x69625446	PPS48_51
DSC_4K_PPS52_55	0x0034	W	0x7B797770	PPS52_55
DSC_4K_PPS56_59	0x0038	W	0x00007E7D	PPS56_59
DSC_4K_PPS60_63	0x003C	W	0x00000000	PPS60_63
DSC_4K_PPS64_67	0x0040	W	0x00000000	PPS60_63
DSC_4K_PPS68_71	0x0044	W	0x00000000	PPS60_63
DSC_4K_PPS72_75	0x0048	W	0x00000000	PPS60_63
DSC_4K_PPS76_79	0x004C	W	0x00000000	PPS60_63
DSC_4K_PPS80_83	0x0050	W	0x00000000	PPS60_63
DSC_4K_PPS84_87	0x0054	W	0x00000000	PPS60_63
DSC_4K_PPS88_91	0x0058	W	0x00000000	PPS88_91
DSC_4K_PPS92_95	0x005C	W	0x00000000	PPS92_95
DSC_4K_VERSION	0x0080	W	0x10000110	VERSION
DSC_4K_CFG_REG0	0x0084	W	0x48120BA1	Configuration 0
DSC_4K_CFG_REG1	0x0088	W	0x10000870	Configuration 1
DSC_4K_CFG_REG2	0x008C	W	0x00002400	Configuration 2
DSC_4K_CFG_REG3	0x0090	W	0x10000870	Configuration 3
DSC_4K_CTRL0	0x00A0	W	0x20000010	Control 0
DSC_4K_CTRL1	0x00A4	W	0x00100000	Control 1
DSC_4K_STS0	0x00A8	W	0x00000003	Status 0
DSC_4K_STS1	0x00AC	W	0x00000003	Status 1
DSC_4K_STS2	0x00B0	W	0x00000003	Status 2
DSC_4K_STS3	0x00B4	W	0x00000003	Status 3
DSC_4K_STS4	0x00B8	W	0x00000003	Status 4
DSC_4K_STS5	0x00BC	W	0x00000003	Status 5
DSC_4K_ERS	0x00C4	W	0xFFFFFFFF	Error status

7.5.2.10 MMU0/1

Name	Offset	Size	Reset Value	Description
VOP2_MMU0_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address.
VOP2_MMU0_STATUS	0x0004	W	0x00000000	MMU status register.
VOP2_MMU0_COMMAND	0x0008	W	0x00000000	MMU command register.
VOP2_MMU0_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault.
VOP2_MMU0_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register.
VOP2_MMU0_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register.
VOP2_MMU0_INT_CLEAR	0x0018	W	0x00000000	MMU interrupt clear register.
VOP2_MMU0_INT_MASK	0x001C	W	0x00000000	MMU interrupt mask register.
VOP2_MMU0_INT_STATUS	0x0020	W	0x00000000	MMU interrupt status register.
VOP2_MMU0_AUTO_GATING	0x0024	W	0x00000000	MMU auto gating.

7.5.3 Detail Register Description

7.5.3.1 SYS_CTRL

SYS_CTRL_REG_CFG_DONE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15	RW	0x1	sw_global_regdone_en Global regdone enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	reg_load_wb_en In the first setting of the register, the new value was saved into the mirror register. When all the wb register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
13:8	RO	0x00	reserved
7	RW	0x0	reg_load_sys3_en In the first setting of the register, the new value was saved into the mirror register. When all the system3 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
6	RW	0x0	reg_load_sys2_en In the first setting of the register, the new value was saved into the mirror register. When all the system2 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
5	RW	0x0	reg_load_sys1_en In the first setting of the register, the new value was saved into the mirror register. When all the system1 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_sys0_en In the first setting of the register, the new value was saved into the mirror register. When all the system0 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3	RW	0x0	reg_load_global3_en In the first setting of the register, the new value was saved into the mirror register. When all the register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
2	RW	0x0	reg_load_global2_en In the first setting of the register, the new value was saved into the mirror register. When all the register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

Bit	Attr	Reset Value	Description
1	RW	0x0	reg_load_global1_en In the first setting of the register, the new value was saved into the mirror register. When all the register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	RW	0x0	reg_load_global0_en In the first setting of the register, the new value was saved into the mirror register. When all the register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

SYS_CTRL_VERSION_INFO
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major Used for IP structure.
23:16	RW	0x00	minor Big feature change under same structure.
15:0	RW	0x0000	svnbuild RTL current SVN number.

SYS_CTRL_AUTO_GATING_CTRL_IMD
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x1	auto_gating_en 1'b0: Disable auto gating 1'b1: Enable auto gating default auto gating enable
30:29	RO	0x0	reserved
28	RW	0x1	port3_aclk_enable Configure 1 to enable clock
27	RW	0x1	port2_aclk_enable Configure 1 to enable clock
26	RW	0x1	port1_aclk_enable Configure 1 to enable clock
25	RW	0x1	port0_aclk_enable Configure 1 to enable clock
24	RW	0x1	rgb_clk_enable Configure 1 to enable clock
23	RW	0x1	dsc4k_clk_enable Configure 1 to enable clock
22	RW	0x1	dsc8k_clk_enable Configure 1 to enable clock
21	RW	0x1	mipi1_pixclk_enable Configure 1 to enable clock
20	RW	0x1	mipi0_pixclk_enable Configure 1 to enable clock
19	RW	0x1	hdmiedp1_pixclk_enable Configure 1 to enable clock
18	RW	0x1	hdmiedp0_pixclk_enable Configure 1 to enable clock
17	RW	0x1	dp1_pixclk_enable Configure 1 to enable clock

Bit	Attr	Reset Value	Description
16	RW	0x1	dp0_pixclk_enable Configure 1 to enable clock
15	RO	0x0	reserved
14	RW	0x1	port_dclk_gating_en 1'b0: Disable 1'b1: Enable
13	RW	0x1	prescan_aclk_gating_en 1'b0: Disable 1'b1: Enable
12	RW	0x1	pwm_pwmclk_gating_en 1'b0: Disable 1'b1: Enable
11	RW	0x1	wb_aclk_gating_en 1'b0: Disable 1'b1: Enable
10	RW	0x1	cabc_dclk_gating_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	gamma_dclk_gating_en 1'b0: Disable 1'b1: Enable
8	RW	0x1	overlay_aclk_gating_en 1'b0: Disable 1'b1: Enable
7	RW	0x1	smart1_aclk_gating_en 1'b0: Disable 1'b1: Enable
6	RW	0x1	smart0_aclk_gating_en 1'b0: Disable 1'b1: Enable
5	RW	0x1	esmart1_aclk_gating_en 1'b0: Disable 1'b1: Enable
4	RW	0x1	esmart0_aclk_gating_en 1'b0: Disable 1'b1: Enable
3	RW	0x1	cluster3_aclk_gating_en 1'b0: Disable 1'b1: Enable
2	RW	0x1	cluster2_aclk_gating_en 1'b0: Disable 1'b1: Enable
1	RW	0x1	cluster1_aclk_gating_en 1'b0: Disable 1'b1: Enable
0	RW	0x1	cluster0_aclk_gating_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_WIN_REG_CFG_DONE

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x0	reg_load_esmart3_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart3 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
6	RW	0x0	reg_load_esmart2_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart2 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
5	RW	0x0	reg_load_esmart1_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart1 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_esmart0_en In the first setting of the register, the new value was saved into the mirror register. When all the esmart0 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3	RW	0x0	reg_load_cluster3_en In the first setting of the register, the new value was saved into the mirror register. When all the cluster3 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
2	RW	0x0	reg_load_cluster2_en In the first setting of the register, the new value was saved into the mirror register. When all the cluster2 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
1	RW	0x0	reg_load_cluster1_en In the first setting of the register, the new value was saved into the mirror register. When all the Cluster 1 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	RW	0x0	reg_load_cluster0_en In the first setting of the register, the new value was saved into the mirror register. When all the cluster0 register configuration finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

SYS_CTRL_AXI_CTRL0_IMD

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	lut_use_axi1 Select AXI1. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	axi1_dma_stop Stop AXI1 DMA. 1'b0: Disable 1'b1: Enable
0	RW	0x0	axi0_dma_stop Stop AXI0 DMA. 1'b0: Disable 1'b1: Enable

SYS_CTRL_AXI_HURRY_CTRL0_IMD

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	axi0_qos_value Interconnect qos value
12	RW	0x0	axi0_qos_en Interconnect qos enable.
11	RW	0x0	axi0_hurry_threshold Interconnect hurry threshold value.
10:9	RW	0x0	axi0_hurry_value Interconnect hurry value.
8	RW	0x0	axi0_hurry_en Interconnect hurry enable.
7:5	RO	0x0	reserved
4:3	RW	0x0	axi0_hurry_w_mode 2'b00: Interconnect_hurry_w disable 2'b01: Left 1/4 FIFO empty 2'b10: Left 1/2 FIFO empty 2'b11: Left 3/4 FIFO empty
2:1	RW	0x0	axi0_hurry_w_value Interconnect hurry value. 2'b00: Low priority 2'b11: High priority
0	RW	0x0	axi0_hurry_w_en Interconnect hurry enable.

SYS_CTRL_AXI_HURRY_CTRL1_IMD

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	axi1_qos_value Interconnect qos value.
12	RW	0x0	axi1_qos_en Interconnect qos enable.
11	RW	0x0	axi1_hurry_threshold Interconnect hurry threshold value.
10:9	RW	0x0	axi1_hurry_value Interconnect hurry value.
8	RW	0x0	axi1_hurry_en Interconnect hurry enable.

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4:3	RW	0x0	axi1_hurry_w_mode 2'b00: Interconnect_hurry_w disable. 2'b01: Left 1/4 FIFO empty 2'b10: Left 1/2 FIFO empty 2'b11: Left 3/4 FIFO empty
2:1	RW	0x0	axi1_hurry_w_value Interconnect hurry value. 2'b00: Low priority 2'b11: High priority
0	RW	0x0	axi1_hurry_w_en Interconnect hurry enable.

SYS_CTRL_AXI_OUTSTANDING_CTRL0_IMD

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:11	RW	0x0	axi1_outstanding_num AXI0 bus max outstanding number.
10:9	RO	0x0	reserved
8	RW	0x0	axi1_outstanding_en AXI1 bus max outstanding enable. 1'b0: Disable 1'b1: Enable
7:3	RW	0x00	axi0_outstanding_num AXI0 bus max outstanding number.
2:1	RO	0x0	reserved
0	RW	0x0	axi0_outstanding_en AXI0 bus max outstanding enable. 1'b0: Disable 1'b1: Enable

SYS_CTRL_AXI_LUT_CTRL_IMD

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x0	mmu_bypass_en If AXI rid > mmu_bypass_id, bypass mmu. 1'b0: Disable 1'b1: Enable
30:26	RW	0x00	mmu_bypass_id If AXI rid > mmu_bypass_id, bypass mmu.
25:24	RW	0x0	mmu_resetn_mode 2'b00: mmu_page_fault && AXI_idle 2'b01: mmu_page_fault others: Reserved
23:22	RW	0x0	mmu1_regdone_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
21	RO	0x0	reserved
20	RW	0x0	mmu_resetn_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
19:18	RW	0x0	mmu0_regdone_sel 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
17:16	RO	0x0	reserved
15	RW	0x0	vp3_interlace_frm_reg_done Video output3 reg done frame valid. 1'b0: Reg done every field for interlace. 1'b1: Reg done every frame for interlace.
14	RW	0x0	vp2_interlace_frm_reg_done Video output2 reg done frame valid. 1'b0: Reg done every field for interlace. 1'b1: Reg done every frame for interlace.
13	RW	0x0	vp1_interlace_frm_reg_done Video output1 reg done frame valid. 1'b0: Reg done every field for interlace. 1'b1: Reg done every frame for interlace.
12	RW	0x0	vp0_interlace_frm_reg_done Video output0 reg done frame valid. 1'b0: Reg done every field for interlace. 1'b1: Reg done every frame for interlace.
11:8	RO	0x0	reserved
7:4	RW	0x0	lut_dma_rid LUT AXI read id. VP0 LUT AXI id = LUT_DMA_rid. VP1 LUT AXI id = LUT_DMA_rid + 1. VP2 LUT AXI id = LUT_DMA_rid + 2.
3:2	RW	0x0	lut_dma_rlen LUT AXI read burst. 2'b00: Burst16 2'b01: Burst8 2'b1x: Burst4
1	RW	0x0	lut_dma_stop Stop LUT DMA. 1'b0: Disable 1'b1: Enable
0	RW	0x0	lut_dma_en Enable LUT DMA. 1'b0: Disable 1'b1: Enable

SYS_CTRL_DSP_INFACE_EN

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:21	RW	0x0	mipi1_port_sel Select MIPI1 interface video source: 2'h0: Video output2 2'h1: Video output3 2'h3: Video output1 (Only Supported In DSC Mode)
20	RW	0x0	mipi0_port_sel Select MIPI0 interface video source: 1'b0: Video output2 1'b1: Video output3

Bit	Attr	Reset Value	Description
19:18	RW	0x0	hdmiedp1_port_sel Select HDMI/eDP Combo 1 interface video source: 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
17:16	RW	0x0	hdmiedp0_port_sel Select HDMI/eDP Combo 0 interface video source: 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
15:14	RW	0x0	dp1_port_sel Select DP1 interface video source: 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
13:12	RW	0x0	dp0_port_sel Select DP0 interface video source: 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
11	RO	0x0	reserved
10:8	RW	0x0	rgb_mode Enable parallel display interface. 3'b000: Disable 3'b010: BT656 3'b011: BT1120 3'b100: Debug mode(RGB454)
7	RW	0x0	mipi1_mode_en Enable MIPI1 display interface. 1'b0: Disable 1'b1: Enable
6	RW	0x0	mipi0_mode_en Enable MIPI0 display interface. 1'b0: Disable 1'b1: Enable
5:4	RW	0x0	hdmiedp1_mode Enable HDMI/eDP Combo 1 display interface. 2'b00: Disable 2'b01: EDP mode Others: HDMI mode
3:2	RW	0x0	hdmiedp0_mode Enable HDMI/eDP Combo 0 display interface. 2'b00: Disable 2'b01: EDP mode Others: HDMI mode
1	RW	0x0	dp1_mode_en Enable DP1 display interface. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dp0_mode_en Enable DP0 display interface. 1'b0: Disable 1'b1: Enable

SYS_CTRL_DSP_INFACE_CTRL

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x0	mipi1_pix_clk_sel Division factor for MIPI1 pixel clock to generated from dclk out source. 2'b00: dclk out N 2'b01: dclk out N / 2 2'b10: dclk out N / 4 N is determined by SYS_DSP_INFACE_EN.mipi10_port_sel.
25:24	RW	0x0	mipi0_pix_clk_sel Division factor for MIPI0 pixel clock to generated from dclk out source. 2'b00: dclk out N 2'b01: dclk out N / 2 2'b10: dclk out N / 4 N is determined by SYS_DSP_INFACE_EN.mipi0_port_sel.
23	RO	0x0	reserved
22	RW	0x0	hdmiedp1_pix_clk_sel Division factor for HDMI/eDP 1 interface pixel clock to generated from dclk source. 2'b00: dclk N 2'b01: dclk N / 2 N is determined by SYS_DSP_INFACE_EN.hdmiedp1_port_sel.
21:20	RW	0x0	hdmiedp1_dclk_sel Division factor for HDMI/eDP 1 internal process clock to generated from dclk source. 2'b00: dclk N 2'b01: dclk N / 2 2'b10: dclk N / 4 N is determined by SYS_DSP_INFACE_EN.hdmiedp1_port_sel.
19	RO	0x0	reserved
18	RW	0x0	hdmiedp0_pix_clk_sel Division factor for HDMI/eDP 0 interface pixel clock to generated from dclk source. 2'b00: dclk N 2'b01: dclk N / 2 N is determined by SYS_DSP_INFACE_EN.hdmiedp0_port_sel.
17:16	RW	0x0	hdmiedp0_dclk_sel Division factor for HDMI/eDP 0 internal process clock to generated from dclk source. 2'b00: dclk N 2'b01: dclk N / 2 2'b10: dclk N / 4 N is determined by SYS_DSP_INFACE_EN.hdmiedp0_port_sel.
15:13	RO	0x0	reserved
12	RW	0x0	mipi1_dsi_mode MIPI1 display interface operating mode in uncompressed mode. 1'h0: Video Mode 1'h1: Command(DataStream) Mode
11	RW	0x0	mipi0_dsi_mode MIPI0 display interface operating mode in uncompressed mode. 1'h0: Video Mode 1'h1: Command(DataStream) Mode

Bit	Attr	Reset Value	Description
10	RW	0x0	mipi_dual_channel_en MIPI DSI Double Channel Display Mode. 1'b0: Disable 1'b1: Enable
9	RW	0x0	dp_split_en DP Display Split Mode. 1'b0: Disable 1'b1: Enable
8	RW	0x0	hdmiedp_split_en HDMI/eDP Display Split Mode. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	bt1120_yc_swap Swap gray and color component. 1'b0: Disable 1'b1: Enable
4	RW	0x0	bt1120_uv_swap Swap U and V component. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	bt656_yc_swap Swap GRAY and COLOR component of BT656.
0	RW	0x0	bt656_uv_swap Swap U and V component of BT656.

SYS_CTRL_DSP_INFACE_POL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	regdone_sel Select interface control register regdone sync port: 2'b00: Video output 0 2'b01: Video output 1 2'b10: Video output 2 2'b11: Video output 3
29	RO	0x0	reserved
28	RW	0x0	regdone_imd_en Enable interface control register (SYS_DSP_INFACE_EN / SYS_DSP_INFACE_CTRL / SYS_DSP_INFACE_POL) update immediately.
27:15	RO	0x0000	reserved
14	RW	0x0	dp1_den_pol Active polarity: 1'b0: Positive 1'b1: Negative
13	RW	0x0	dp1_vsync_pol Active polarity: 1'b0: Negative 1'b1: Positive
12	RW	0x0	dp1_hsync_pol Active polarity: 1'b0: Negative 1'b1: Positive
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	dp0_den_pol Active polarity: 1'b0: Positive 1'b1: Negative
9	RW	0x0	dp0_vsync_pol Active polarity: 1'b0: Negative 1'b1: Positive
8	RW	0x0	dp0_hsync_pol Active polarity: 1'b0: Negative 1'b1: Positive
7:4	RO	0x0	reserved
3	RW	0x0	rgb_clk_pol 1'b0: Normal 1'b1: Invert
2	RW	0x0	rgb_den_pol Active polarity: 1'b0: Positive 1'b1: Negative
1	RW	0x0	rgb_vsync_pol Active polarity: 1'b0: Negative 1'b1: Positive
0	RW	0x0	rgb_hsync_pol Active polarity: 1'b0: Negative 1'b1: Positive

SYS_CTRL_POWER_CTRL

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	esmart_pu_stable_en Enable stable counter between power chains for esmart power up flow. 1'b0: Disable 1'b1: Enable
22	RW	0x0	dsc_4k_pu_stable_en Enable stable counter between power chains for DSC_4K power up flow. 1'b0: Disable 1'b1: Enable
21	RW	0x0	dsc_8k_pu_stable_en Enable stable counter between power chains for DSC_8K power up flow. 1'b0: Disable 1'b1: Enable
20	RO	0x0	reserved
19	RW	0x0	cluster3_pu_stable_en Enable stable counter between power chains for Cluster 3 power up flow. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
18	RW	0x0	cluster2_pu_stable_en Enable stable counter between power chains for Cluster 2 power up flow. 1'b0: Disable 1'b1: Enable
17	RW	0x0	cluster1_pu_stable_en Enable stable counter between power chains for Cluster 1 power up flow. 1'b0: Disable 1'b1: Enable
16	RW	0x0	cluster0_pu_stable_en Enable stable counter between power chains for Cluster 0 power up flow. 1'b0: Disable 1'b1: Enable
15	RW	0x0	esmart_pd_stable_en Enable stable counter between power chains for esmart power down flow. 1'b0: Disable 1'b1: Enable
14	RW	0x0	dsc_4k_pd_stable_en Enable stable counter between power chains for DSC_4K power down flow. 1'b0: Disable 1'b1: Enable
13	RW	0x0	dsc_8k_pd_stable_en Enable stable counter between power chains for DSC_8K power down flow. 1'b0: Disable 1'b1: Enable
12	RO	0x0	reserved
11	RW	0x0	cluster3_pd_stable_en Enable stable counter between power chains for Cluster 3 power down flow. 1'b0: Disable 1'b1: Enable
10	RW	0x0	cluster2_pd_stable_en Enable stable counter between power chains for Cluster 2 power down flow. 1'b0: Disable 1'b1: Enable
9	RW	0x0	cluster1_pd_stable_en Enable stable counter between power chains for Cluster 1 power down flow. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cluster0_pd_stable_en Enable stable counter between power chains for Cluster 0 power down flow. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
7	RW	0x0	esmart_pd_en Power Control to Esmart1/2/3 Power Domain 1'b0: Power on (immediate effect) 1'b1: Power down (set corresponding regdone bit and it will be effective on the next frame start)
6	RW	0x0	dsc_4k_pd_en Power Control to DSC 4K Power Domain 1'b0: Power on (immediate effect) 1'b1: Power down (immediate effect)
5	RW	0x0	dsc_8k_pd_en Power Control to DSC 8K Power Domain 1'b0: Power on (immediate effect) 1'b1: Power down (immediate effect)
4	RO	0x0	reserved
3	RW	0x1	cluster3_pd_en Power Control to Cluster 3 Power Domain 1'b0: Power on (immediate effect) 1'b1: Power down (set corresponding regdone bit and it will be effective on the next frame start)
2	RW	0x1	cluster2_pd_en Power Control to Cluster 2 Power Domain 1'b0: Power on (immediate effect) 1'b1: Power down (set corresponding regdone bit and it will be vaild on the next frame start)
1	RW	0x1	cluster1_pd_en Power Control to Cluster 1 Power Domain 1'b0: Power on (immediate effect) 1'b1: Power down (set corresponding regdone bit and it will be vaild on the next frame start)
0	RW	0x1	cluster0_pd_en Power Control to whole Cluster Power Domain, include the cluster0/1/2/3. 1'b0: Power on (immediate effect) 1'b1: Power down (set corresponding regdone bit and it will be vaild on the next frame start)

SYS_CTRL_VAR_FERQ_CTRL_IMD

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RW	0x0	vp3_almost_full_or_en 1'b0: Disable 1'b1: Enable
30	RW	0x0	vp2_almost_full_or_en 1'b0: Disable 1'b1: Enable
29	RW	0x0	vp1_almost_full_or_en 1'b0: Disable 1'b1: Enable
28	RW	0x0	vp0_almost_full_or_en 1'b0: Disable 1'b1: Enable
27	RW	0x0	vp3_dsp_hold_or_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
26	RW	0x0	vp2_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
25	RW	0x0	vp1_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
24	RW	0x0	vp0_dsp_hold_or_en 1'b0: Disable 1'b1: Enable
23	RW	0x0	vp3_line_flag_or_en 1'b0: Disable 1'b1: Enable
22	RW	0x0	vp2_line_flag_or_en 1'b0: Disable 1'b1: Enable
21	RW	0x0	vp1_line_flag_or_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	vp0_line_flag_or_en 1'b0: Disable 1'b1: Enable
19	RW	0x0	wb_dma_finish_or_en 1'b0: Disable 1'b1: Enable
18	RW	0x0	axi_dma_finish_or_en 1'b0: Disable 1'b1: Enable
17:16	RO	0x0	reserved
15	RW	0x0	vp3_almost_full_and_en 1'b0: Disable 1'b1: Enable
14	RW	0x0	vp2_almost_full_and_en 1'b0: Disable 1'b1: Enable
13	RW	0x0	vp1_almost_full_and_en 1'b0: Disable 1'b1: Enable
12	RW	0x0	vp0_almost_full_and_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	vp3_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
10	RW	0x0	vp2_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	vp1_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	vp0_dsp_hold_and_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	vp3_line_flag_and_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x0	vp2_line_flag_and_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	vp1_line_flag_and_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	vp0_line_flag_and_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	wb_dma_finish_and_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	axi_dma_finish_and_en 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	dma_finish_mode 2'b00: Src_or 2'b01: Src_and 2'b10: Src_or && src_and 2'b11: Src_or || src_and

SYS_CTRL_MMU_RADDR_RANGE

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mmu_raddr_range1 Min mmu raddress = {mmu_raddr_range1.16'h0}
15:0	RW	0x0000	mmu_raddr_range0 Min mmu raddress = {mmu_raddr_range0.16'h0}

SYS_CTRL_WB_CTRL0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0xe	wb_uv_id Use default 0xe.
26:23	RO	0x0	reserved
22:19	RW	0xd	wb_yrgb_id Use default 0xd.
18:13	RO	0x00	reserved
12	RW	0x0	wb_oneframe_mode 1'b0: Disable 1'b1: Enable
11	RW	0x0	wb_handshake_mode 1'b0: Full handshake 1'b1: Half handshake
10	RO	0x0	reserved
9	RW	0x0	wb_ythrow_mode 1'b0: Throw odd line 1'b1: Throw even line
8	RW	0x0	wb_ythrow_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	wb_xpsd_bil_en 1'b0: Enable scale 1'b1: Disable scale

Bit	Attr	Reset Value	Description
6	RW	0x0	wb_rgb2yuv_mode 1'b0: BT601 1'b1: BT709
5	RW	0x0	wb_rgb2yuv_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	wb_dither_en When wb_fmt is RGB565. 1'b0: Without dither, RGB888 clip to RGB565 1'b1: With dither, RGB888 dither to RGB565
3:1	RW	0x0	wb_fmt 3'b000: ARGB888 3'b001: RGB888 3'b010: RGB565 3'b100: YcbCr420 other: Reserved
0	RW	0x0	wb_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_WB_XSPD_FACTOR

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	wb_xpsd_bil_factor Factor=((src_width[11:0])/(dst_width[11:0]))*2^12.
15:10	RO	0x00	reserved
9:0	RW	0x000	fifo_thold When wb_FIFO_wcnt < FIFO_thold, hold the pre_scan timing. FIFO_thold = wb_width * fmt_byte / 16 3'b000: ARGB888, fmt_byte = 4 3'b001: RGB888, fmt_byte = 3 3'b010: RGB565, fmt_byte = 2 3'b100: YcbCr420, fmt_byte = 1

SYS_CTRL_WB_YRGB_MST

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_yrgb_mst YRGB mst address.

SYS_CTRL_WB_CBR_MST

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_cbr_mst CBR mst adress.

SYS_CTRL_OTP_WIN_EN_IMD

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	otp_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_OTP_MIRR_CTRL_IMD

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dis_otp_function Disable otp function step by step. step one: Write 32'h20151223 step two: Write 32'h20180224

SYS_CTRL_LUT_PORT_SEL

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RW	0x0	port2_dclk_source_sel Select the port 2 dclk source, valid at next frame start after set port 2 reg_done. 1'h0: Select dclk2 1'h1: Select dclk1
30	RW	0x0	port0_dclk_source_sel Select the port 0 dclk source, valid at next frame start after set port 0 reg_done. 1'h0: Select dclk0 1'h1: Select dclk1
29:17	RO	0x0000	reserved
16	RW	0x0	port01_merge_en Enable port0 and port1 pixel stream merge to support the video timing Hactive exceed the 4096 pixels. (immediate effect)
15:14	RO	0x0	reserved
13:12	RW	0x0	gamma_ahb_write_sel 2'b00: Vp0 gamma 2'b01: Vp1 gamma 2'b10: Vp2 gamma 2'b11: Vp3 gamma
11:10	RO	0x0	reserved
9:8	RW	0x0	wb_port_sel Select WB display output. 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
7:5	RW	0x0	bpp_win_sel Select 8BPP LUT esmart num. 2'b00: Esmart0 2'b01: Esmart1 2'b10: Esmart2 2'b11: Esmart3
4	RW	0x0	bpp_lut_en Enable 8BPP LUT. 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

SYS_CTRL_POWER_STABLE_CTRL

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	vop_powerdown_stable_cnt_thresh VOP power up stable count thresh. Number of clk_pmu used by counter logic.
7:4	RO	0x0	reserved
3:0	RW	0x0	vop_powerup_stable_cnt_thresh VOP power down stable count thresh. Number of clk_pmu used by counter logic.

SYS_CTRL_STATUS0

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	dsp_vcnt0 Read the video output0 vertical counter.
15	RO	0x0	esmart_power_domain_status Indicates esmart1/2/3 power domain status 1'b1: Power down 1'b0: Power up
14	RO	0x0	dsc4k_power_domain_status Indicates DSC 4K encoder power domain status 1'b1: Power down 1'b0: Power up
13	RO	0x0	dsc8k_power_domain_status Indicates DSC 8K encoder power domain status 1'b1: Power down 1'b0: Power up
12	RO	0x0	reserved
11	RO	0x0	cluster3_power_domain_status Indicates cluster 3 power domain status 1'b1: Power down 1'b0: Power up
10	RO	0x0	cluster2_power_domain_status Indicates cluster 2 power domain status 1'b1: Power down 1'b0: Power up
9	RO	0x0	cluster1_power_domain_status Indicates cluster 1 power domain status 1'b1: Power down 1'b0: Power up
8	RO	0x0	cluster0_power_domain_status Indicates cluster 0 power domain status 1'b1: Power down 1'b0: Power up
7:2	RO	0x00	reserved
1	RW	0x0	mmu0_idle MMU0 idle status.
0	RW	0x0	dma_stop_valid0 AXI0 DMA stop status.

SYS_CTRL_STATUS1

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt1 Read the video output1 vertical counter.

Bit	Attr	Reset Value	Description
15:2	RO	0x0000	reserved
1	RW	0x0	mmu1_idle MMU1 idle status.
0	RW	0x0	dma_stop_valid1 AXI1 DMA stop status.

SYS_CTRL_STATUS2

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt2 Read the video output2 vertical counter.
15:0	RO	0x0000	reserved

SYS_CTRL_STATUS3

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt3 Read the video output2 vertical counter.
15:0	RO	0x0000	reserved

SYS_CTRL_LINE_FLAG0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1, intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_LINE_FLAG1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1, intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_LINE_FLAG2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1, intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_LINE_FLAG3

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1, intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

SYS_CTRL_INTR_EN0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_en_mmu0 1'b0: Disable 1'b1: Enable
6	RO	0x0	reserved
5	RW	0x0	int_en_wb0_finish 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_en_wb0_yrgb_fifo_full 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en_wb0_uv_fifo_full 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_dma0_finish 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_bus0_error 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

SYS_CTRL_INTR_CLR0

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_clr_mmu0 Interrupt clear (Auto clear).
6	RO	0x0	reserved
5	RW	0x0	intr_clr_wb_dma_finish WB_DMA finish interrupt clear (Auto clear).
4	RW	0x0	intr_clr_wb_yrgb_fifo_full Interrupt clear (Auto clear).
3	RW	0x0	intr_clr_wb_uv_fifo_full Interrupt clear (Auto clear).
2	RW	0x0	intr_clr_dma_finish DMA finish interrupt clear (Auto clear).
1	RW	0x0	intr_clr_bus_error Bus error Interrupt clear (Auto clear).
0	RO	0x0	reserved

SYS_CTRL_INTR_STATUS0

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_status_mmu0 Interrupt status of MMU0.
6	RO	0x0	reserved
5	RW	0x0	intr_status_wb_dma_finish Interrupt status.
4	RW	0x0	intr_status_wb_yrgb_fifo_full Interrupt status.
3	RW	0x0	intr_status_wb_uv_fifo_full Interrupt status.
2	RW	0x0	intr_status_dma_finish DMA finish interrupt status.
1	RW	0x0	intr_status_bus_error Bus error Interrupt clear status.
0	RO	0x0	reserved

SYS_CTRL_INTR_RAW_STATUS0

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_raw_status_mmu0 Interrupt of MMU0 raw status.
6	RO	0x0	reserved
5	RW	0x0	intr_raw_status_wb_dma_finish Interrupt raw status.
4	RW	0x0	intr_raw_status_wb_yrgb_fifo_full Interrupt raw status.
3	RW	0x0	intr_raw_status_wb_uv_fifo_full Interrupt raw status.
2	RW	0x0	intr_raw_status_dma_finish DMA finish interrupt raw status.
1	RW	0x0	intr_raw_status_bus_error Bus error Interrupt raw status.

Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

SYS_CTRL_INTR_EN1
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_en_mmu1 1'b0: Disable 1'b1: Enable
6:3	RO	0x0	reserved
2	RW	0x0	intr_en_dma1_finish 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_bus1_error 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

SYS_CTRL_INTR_CLR_SYS1
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_clr_mmu1 Interrupt clear (Auto clear).
6:3	RO	0x0	reserved
2	RW	0x0	intr_clr_dma_finish DMA finish interrupt clear (Auto clear).
1	RW	0x0	intr_clr_bus_error Bus error Interrupt clear (Auto clear).
0	RO	0x0	reserved

SYS_CTRL_INTR_STATUS1
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_status_mmu1 Interrupt status.
6:3	RO	0x0	reserved
2	RW	0x0	intr_status_dma_finish DMA finish interrupt status.
1	RW	0x0	intr_status_bus_error Bus error Interrupt status.
0	RO	0x0	reserved

SYS_CTRL_INTR_RAW_STATUS1
Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_raw_status_mmu1 Interrupt raw_status.

Bit	Attr	Reset Value	Description
6:3	RO	0x0	reserved
2	RW	0x0	intr_raw_status_dma_finish DMA finish interrupt raw_status.
1	RW	0x0	intr_raw_status_bus_error Bus error Interrupt raw_status.
0	RO	0x0	reserved

SYS_CTRL_PORT0_INTR_EN

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15	RO	0x0	reserved
14	RW	0x0	intr_en_reserved_core3 1'b0: Disable 1'b1: Enable
13	RW	0x0	intr_en_ reserved _core2 1'b0: Disable 1'b1: Enable
12	RW	0x0	intr_en_ reserved _core1 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT0_INTR_CLR

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15	RO	0x0	reserved
14	RW	0x0	intr_clr_reserved_core3 Reserved core3 interrupt clear (Auto clear).
13	RW	0x0	intr_clr_reserved_core2 Reserved core2 interrupt clear (Auto clear).
12	RW	0x0	intr_clr_reserved_core1 Reserved core1 interrupt clear (Auto clear).
11:10	RO	0x0	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear (Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display VFP interrupt clear (Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear (Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear (Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear (Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear (Auto clear).
1	RW	0x0	intr_clr_fs_new Frame new start interrupt clear (Auto clear).
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear).

SYS_CTRL_PORT0_INTR_STATUS

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	intr_status_reserved_core3 Reserved core3 interrupt status.
13	RW	0x0	intr_status_reserved_core2 Reserved core2 interrupt status.
12	RW	0x0	intr_status_reserved_core1 Reserved core1 interrupt status.
11:10	RO	0x0	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display VFP interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.

Bit	Attr	Reset Value	Description
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT0_INTR_RAW_STATUS

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	intr_raw_reserved_core3 Reserved core3 interrupt raw status.
13	RW	0x0	intr_raw_reserved_core2 Reserved core2 interrupt raw status.
12	RW	0x0	intr_raw_reserved_core1 Reserved core1 interrupt raw status.
11:10	RO	0x0	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display VFP interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

SYS_CTRL_PORT1_INTR_EN

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT1_INTR_CLR
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear (Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display VFP interrupt clear (Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear (Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear (Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear (Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear (Auto clear).
1	RO	0x0	reserved
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear).

SYS_CTRL_PORT1_INTR_STATUS
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display VFP interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.

Bit	Attr	Reset Value	Description
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT1_INTR_RAW_STATUS

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display VFP interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

SYS_CTRL_PORT2_INTR_EN

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT2_INTR_CLR

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear (Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display VFP interrupt clear (Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear (Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear (Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear (Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear (Auto clear).
1	RO	0x0	reserved
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear).

SYS_CTRL_PORT2_INTR_STATUS

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display VFP interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.

Bit	Attr	Reset Value	Description
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT2_INTR_RAW_STATUS
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display VFP interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

SYS_CTRL_PORT3_INTR_EN
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

SYS_CTRL_PORT3_INTR_CLR

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear (Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display VFP interrupt clear (Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear (Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear (Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear (Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear (Auto clear).
1	RO	0x0	reserved
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear).

SYS_CTRL_PORT3_INTR_STATUS

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display VFP interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.

Bit	Attr	Reset Value	Description
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

SYS_CTRL_PORT3_INTR_RAW_STATUS

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display VFP interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

SYS_CTRL_AFBCD_INTR_EN0

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	intr_en_afbcd3_cfg_done 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_afbcd2_cfg_done 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_afbcd1_cfg_done 1'b0: Disable 1'b1: Enable
0	RW	0x0	intr_en_afbcd0_cfg_done 1'b0: Disable 1'b1: Enable

SYS_CTRL_AFBCD_INTR_CLR0

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	intr_clr_afbcd3_cfg_done Interrupt clear (Auto clear).
2	RW	0x0	intr_clr_afbcd2_cfg_done Interrupt clear (Auto clear).

Bit	Attr	Reset Value	Description
1	RW	0x0	intr_clr_afbcd1_cfg_done Interrupt clear (Auto clear).
0	RW	0x0	intr_clr_afbcd0_cfg_done Interrupt clear (Auto clear).

SYS_CTRL_AFBCD_INTR_STATUS0

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	int_status_afbcd3_cfg_done Interrupt status.
2	RW	0x0	int_status_afbcd2_cfg_done Interrupt status.
1	RW	0x0	int_status_afbcd1_cfg_done Interrupt status.
0	RW	0x0	int_status_afbcd0_cfg_done Interrupt status.

SYS_CTRL_AFBCD_INTR_RAW_STATUS0

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	int_raw_status_afbcd3_cfg_done Interrupt raw status.
2	RW	0x0	int_raw_status_afbcd2_cfg_done Interrupt raw status.
1	RW	0x0	int_raw_status_afbcd1_cfg_done Interrupt raw status.
0	RW	0x0	int_raw_status_afbcd0_cfg_done Interrupt raw status.

SYS_CTRL_AFBCD_INTR_EN1

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	int_en_afbcd3_hreg_axi_rresp 1'b0: Disable 1'b1: Enable
6	RW	0x0	int_en_afbcd3_hreg_dec_resp 1'b0: Disable 1'b1: Enable
5	RW	0x0	int_en_afbcd2_hreg_axi_rresp 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_en_afbcd2_hreg_dec_resp 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en_afbcd1_hreg_axi_rresp 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	int_en_afbcd1_hreg_dec_resp 1'b0: Disable 1'b1: Enable
1	RW	0x0	int_en_afbcd0_hreg_axi_rresp 1'b0: Disable 1'b1: Enable
0	RW	0x0	int_en_afbcd0_hreg_dec_resp 1'b0: Disable 1'b1: Enable

SYS_CTRL_AFBCD_INTR_CLR1

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	int_clr_afbcd3_hreg_axi_rresp Interrupt clear (Auto clear).
6	RW	0x0	int_clr_afbcd3_hreg_dec_resp Interrupt clear (Auto clear).
5	RW	0x0	int_clr_afbcd2_hreg_axi_rresp Interrupt clear (Auto clear).
4	RW	0x0	int_clr_afbcd2_hreg_dec_resp Interrupt clear (Auto clear).
3	RW	0x0	int_clr_afbcd1_hreg_axi_rresp Interrupt clear (Auto clear).
2	RW	0x0	int_clr_afbcd1_hreg_dec_resp Interrupt clear (Auto clear).
1	RW	0x0	int_clr_afbcd0_hreg_axi_rresp Interrupt clear (Auto clear).
0	RW	0x0	int_clr_afbcd0_hreg_dec_resp Interrupt clear (Auto clear).

SYS_CTRL_AFBCD_INTR_STATUS1

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	int_status_afbcd3_hreg_axi_rresp Interrupt status.
6	RW	0x0	int_status_afbcd3_hreg_dec_resp Interrupt status.
5	RW	0x0	int_status_afbcd2_hreg_axi_rresp Interrupt status.
4	RW	0x0	int_status_afbcd2_hreg_dec_resp Interrupt status.
3	RW	0x0	int_status_afbcd1_hreg_axi_rresp Interrupt status.
2	RW	0x0	int_status_afbcd1_hreg_dec_resp Interrupt status.
1	RW	0x0	int_status_afbcd0_hreg_axi_rresp Interrupt status.
0	RW	0x0	int_status_afbcd0_hreg_dec_resp Interrupt status.

SYS_CTRL_AFBCD_INTR_RAW_STATUS1
Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	int_raw_status_afbcd3_hreg_axi_rresp Interrupt raw status.
6	RW	0x0	int_raw_status_afbcd3_hreg_dec_resp Interrupt raw status.
5	RW	0x0	int_raw_status_afbcd2_hreg_axi_rresp Interrupt raw status.
4	RW	0x0	int_raw_status_afbcd2_hreg_dec_resp Interrupt raw status.
3	RW	0x0	int_raw_status_afbcd1_hreg_axi_rresp Interrupt raw status.
2	RW	0x0	int_raw_status_afbcd1_hreg_dec_resp Interrupt raw status.
1	RW	0x0	int_raw_status_afbcd0_hreg_axi_rresp Interrupt raw status.
0	RW	0x0	int_raw_status_afbcd0_hreg_dec_resp Interrupt raw status.

SYS_CTRL_SEC_DRM_CTRL
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	sec_axi1_rid3_prot_en 1'b0: Disable 1'b1: Enable
22	RW	0x0	sec_axi1_rid2_prot_en 1'b0: Disable 1'b1: Enable
21	RW	0x0	sec_axi1_rid1_prot_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	sec_axi1_rid0_prot_en 1'b0: Disable 1'b1: Enable
19	RW	0x0	sec_axi0_rid3_prot_en 1'b0: Disable 1'b1: Enable
18	RW	0x0	sec_axi0_rid2_prot_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	sec_axi0_rid1_prot_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	sec_axi0_rid0_prot_en 1'b0: Disable 1'b1: Enable
15	RW	0x0	sec_esmart3_en 1'b0: Disable 1'b1: Enable
14	RW	0x0	sec_esmart2_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
13	RW	0x0	sec_esmart1_en 1'b0: Disable 1'b1: Enable
12	RW	0x0	sec_esmart0_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	sec_cluster3_en 1'b0: Disable 1'b1: Enable
10	RW	0x0	sec_cluster2_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	sec_cluster1_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	sec_cluster0_en 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	sec_rid_lock_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	sec_wb_dis 1'b0: Disable 1'b1: Enable
3	RW	0x0	sec_inface_mux_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	sec_port_mux_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	sec_layer_sel_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	sec_drm_en 1'b0: Disable 1'b1: Enable

SYS_CTRL_SEC_DRM_LAYER_SEL

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	sec_layer7_sel layer7 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
27	RO	0x0	reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x0	sec_layer6_sel layer6 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
23	RO	0x0	reserved
22:20	RW	0x0	sec_layer5_sel layer5 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
19	RO	0x0	reserved
18:16	RW	0x0	sec_layer4_sel layer4 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
15	RO	0x0	reserved
14:12	RW	0x0	sec_layer3_sel layer3 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
11	RO	0x0	reserved
10:8	RW	0x0	sec_layer2_sel layer2 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	sec_layer1_sel layer1 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
3	RO	0x0	reserved
2:0	RW	0x0	sec_layer0_sel layer0 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3

SYS_CTRL_SEC_DRM_PORT_MUX

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sec_esmart3_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
29:28	RW	0x0	sec_esmart2_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
27:26	RW	0x0	sec_esmart1_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
25:24	RW	0x0	sec_esmart0_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
23:22	RW	0x0	sec_cluster3_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
21:20	RW	0x0	sec_cluster2_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3

Bit	Attr	Reset Value	Description
19:18	RW	0x0	sec_cluster1_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
17:16	RW	0x0	sec_cluster0_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
15:12	RW	0x0	sec_port3_mux port3 output mux is selected according to the layer number. Note that port3_mux >= port2_mux. 4'b0000: 1 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0001: 2 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0010: 3 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0011: 4 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0100: 5 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0101: 6 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0110: 7 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0111: 8 - port0_layer_number - port1_layer_number-port2_layer_number
11:8	RW	0x0	sec_port2_mux port2 output mux is selected according to the layer number. Note that port2_mux >= port1_mux. 4'b0000: 1 - port0_layer_number - port1_layer_number 4'b0001: 2 - port0_layer_number - port1_layer_number 4'b0010: 3 - port0_layer_number - port1_layer_number 4'b0011: 4 - port0_layer_number - port1_layer_number 4'b0100: 5 - port0_layer_number - port1_layer_number 4'b0101: 6 - port0_layer_number - port1_layer_number 4'b0110: 7 - port0_layer_number - port1_layer_number 4'b0111: 8 - port0_layer_number - port1_layer_number 4'b1xxx: 0
7:4	RW	0x0	sec_port1_mux port1 output mux is selected according to the layer number. Note that port1_mux >= port0_mux. 4'b0000: 1 - port0_layer_number 4'b0001: 2 - port0_layer_number 4'b0010: 3 - port0_layer_number 4'b0011: 4 - port0_layer_number 4'b0100: 5 - port0_layer_number 4'b0101: 6 - port0_layer_number 4'b0110: 7 - port0_layer_number 4'b0111: 8 - port0_layer_number 4'b1xxx: 0

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sec_port0_mux port0 output mux is selected according to the layer number. 4'b0000: 1 layer 4'b0001: 2 layers 4'b0010: 3 layers 4'b0011: 4 layers 4'b0100: 5 layers 4'b0101: 6 layers 4'b0110: 7 layers 4'b0111: 8 layers 4'b1000: 0 layers

SYS_CTRL_SEC_DRM_INFACE_MUX

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	sec_mipi1_port_sel Select MIPI1 interface video source: 1'b0: Video output2 1'b1: Video output3
20	RW	0x0	sec_mipi0_port_sel Select MIPI0 interface video source: 1'b0: Video output2 1'b1: Video output3
19:18	RW	0x0	sec_hdmiedpi1_port_sel Enable HDMI/eDP Combo 1 display interface. 2'b00: Disable 2'b01: EDP mode Others: HDMI mode
17:16	RW	0x0	sec_hdmiedpi0_port_sel Enable HDMI/eDP Combo 0 display interface. 2'b00: Disable 2'b01: EDP mode Others: HDMI mode
15:14	RW	0x0	sec_dp1_port_sel Select DP1 interface video source: 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
13:12	RW	0x0	sec_dp0_port_sel Select DP0 interface video source: 2'b00: Video output0 2'b01: Video output1 2'b1x: Video output2
11	RO	0x0	reserved
10:8	RW	0x0	sec_rgb_mode Enable parallel display interface. 3'b000: Disable 3'b010: BT656 3'b011: BT1120 3'b100: Debug mode(RGB454)
7	RW	0x0	sec_mipi1_mode_en Enable MIPI1 display interface. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x0	sec_mipi0_mode_en Enable MIPI0 display interface. 1'b0: Disable 1'b1: Enable
5:4	RW	0x0	sec_hdmiedp1_mode Enable HDMI/eDP Combo 1 display interface. 2'b00: Disable 2'b01: EDP mode Others: HDMI mode
3:2	RW	0x0	sec_hdmiedp0_mode Enable HDMI/eDP Combo 0 display interface. 2'b00: Disable 2'b01: EDP mode Others: HDMI mode
1	RW	0x0	sec_dp1_mode_en Enable DP1 display interface. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sec_dp0_mode_en Enable DP0 display interface. 1'b0: Disable 1'b1: Enable

SYS_CTRL_SEC_AXI_RID_PROT
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sec_axi1_rid3_prot secure axi read id.
27:24	RW	0x0	sec_axi1_rid2_prot secure axi read id.
23:20	RW	0x0	sec_axi1_rid1_prot secure axi read id.
19:16	RW	0x0	sec_axi1_rid0_prot secure axi read id.
15:12	RW	0x0	sec_axi0_rid3_prot secure axi read id.
11:8	RW	0x0	sec_axi0_rid2_prot secure axi read id.
7:4	RW	0x0	sec_axi0_rid1_prot secure axi read id.
3:0	RW	0x0	sec_axi0_rid0_prot secure axi read id.

7.5.3.2 DSC_SYS_CTRL

DSC_SYS_CTRL_DSC_8K_SYS_CTRL
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	dsc_halt_en Enable DSC output timing operating in bypass mode. Only used for MIPI DSI command mode.

Bit	Attr	Reset Value	Description
17	RW	0x0	dsc_scan_en Enable DSC output timing operating in scan timing mode, which controlled by DSC_8K_HTOTAL_HS_END/DSC_8K_HACT_ST_END/DSC_8K_VTOTAL_HS_END/DSC_8K_VACT_ST_END/ registers.
16	RW	0x0	dsc_init_dly_mode Configures DSC output delay mode: 1'b0: Delay number manual mode 1'b1: Delay number auto mode
15:14	RW	0x0	dsc_txp_clk_div Configures DSC txp_clk clock divider. The txp_clk drives DSC input pixel interface. 2'b00: txp_clk = dclk N 2'b01: txp_clk = dclk N / 2 2'b10: txp_clk = dclk N / 4 N is determined by dsc_port_sel.
13:12	RW	0x0	dsc_cds_clk_div Configures DSC cds_clk clock divider. The cds_clk drives DSC output compressed data stream interface. 2'b00: cds_clk = txp_clk 2'b01: cds_clk = txp_clk / 2 2'b10: cds_clk = txp_clk / 4
11:9	RO	0x0	reserved
8	RW	0x0	dsc_pxl_clk_div Configures DSC pxl_clk clock divider. The pxl_clk drives DSC slice's data path operations. 1'b0: pxl_clk = txp_clk 1'b1: pxl_clk = txp_clk / 2
7:6	RW	0x0	dsc_pixel_num Configures DSC input pixel number per cycle. The number of slices per lines must be more than or equal to the number of pixels per clock fed at the DSC encoder pixel input interface. 2'b00: 1 Pixels/cycle 2'b01: 2 Pixels/cycle Others: 4 Pixels/cycle
5:4	RW	0x0	dsc_inface_mode Configures DSC output compressed data stream interface mode 2'b00: Disable 2'b01: HDMI0 2'b10: MIPI0 Command(DataStream) Mode 2'b11: MIPI0 Video Mode
3	RO	0x0	reserved
2	RW	0x0	dsc_man_mode Enable DSC pixel source selection manual mode. The default pixel source come from MIPI interface 0 or HDMI interface 0.
1:0	RW	0x0	dsc_port_sel Configures the DSC pixel stream and pixel clock source. 2'b00: Port0 2'b01: Port1 2'b10: Port2 2'b11: Port3

DSC_SYS_CTRL_DSC_8K_RST

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	dsc_flush DSC datapath flush control. Flush control input is to be asserted to recover from an error condition and subsequently to bring DSC encoder to its initial state. Active level of this input is dependent on the state of Flush Active Level control bit (FLAL - bit 4 in DSC encoder register DSC_CTRL0).
15:1	RO	0x0000	reserved
0	RW	0x0	dsc_soft_rst DSC power on reset. Active Low.

DSC_SYS_CTRL_DSC_8K_CFG_DONE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	cfg_done When all the register of DSC encoder has been done, writing this bit 1 to unmask input to encoder which will be valid at the next frame start. When received the frame start, the hardware will clear this bit.

DSC_SYS_CTRL_DSC_8K_INIT_DLY_NUM

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	scan_timing_para_imd_en Configure this field to 1 to enable scan timing parameters with immediate effect.
15:0	RW	0x0000	dsc_init_dly_num Configures the initial delay number of compressed clock cycles. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_8K_HTOTAL_HS_END

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_htotal DSC output compressed interface scanning horizontal period. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_hs_end DSC output compressed interface scanning hsync pulse width. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_8K_HACT_ST_END

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_hact_end DSC output compressed interface scanning horizontal active end point. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_hact_st DSC output compressed interface scanning horizontal active start point. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_8K_VTOTAL_VS_END

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_vtotal DSC output compressed interface scanning vertical period. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_vs_end DSC output compressed interface scanning vsync pulse width. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_8K_VACT_ST_END
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_vact_end DSC output compressed interface scanning vertical active end point. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_vact_st DSC output compressed interface scanning vertical active start point. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_8K_STATUS
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dsc error status This bit equal 1 indicates an error condition detected in DSC encoder. This bit will be clear when host has read the Error Code Word Register in DSC encoder.

DSC_SYS_CTRL_DSC_8K_DEBUG_0
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	compressed_if_n_ready_err This bit assert when compressed data interface ready signal is valid but DSC encoder is not ready to output valid data content. Only used in scan mode.
1	RC	0x0	pixel_if_n_ready_err This bit assert when pixel stream fed in DSC encoder pixel data interface is valid but DSC encoder is not ready to accept data.
0	RO	0x0	reserved

DSC_SYS_CTRL_DSC_8K_DEBUG_1
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	cds_frame_cnt Current DSC output compressed data frame count for debug observation.
15:0	RO	0x0000	cds_line_cnt Current DSC output compressed data line count for debug observation.

DSC_SYS_CTRL_DSC_8K_DEBUG_2
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cds_frame_num_err Record the frame number when error status detected.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	cds_line_num_err Record the line number when error status detected.

DSC_SYS_CTRL_DSC_4K_SYS_CTRL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	dsc_halt_en Enable DSC output timing operating in bypass mode. Only used for MIPI DSI command mode.
17	RW	0x0	dsc_scan_en Enable DSC output timing operating in scan timing mode, which controlled by DSC_4K_HTOTAL_HS_END/DSC_4K_HACT_ST_END/DSC_4K_VTOTAL_HS_END/DSC_4K_VACT_ST_END/ registers.
16	RW	0x0	dsc_init_dly_mode Configures DSC output delay mode: 1'b0: Delay number manual mode 1'b1: Delay number auto mode
15:14	RW	0x0	dsc_txp_clk_div Configures DSC txp_clk clock divider. The txp_clk drives DSC input pixel interface. 2'b00: txp_clk = dclk N 2'b01: txp_clk = dclk N / 2 2'b10: txp_clk = dclk N / 4 N is determined by dsc_port_sel.
13:12	RW	0x0	dsc_cds_clk_div Configures DSC cds_clk clock divider. The cds_clk drives DSC output compressed data stream interface. 2'b00: cds_clk = txp_clk 2'b01: cds_clk = txp_clk / 2 2'b10: cds_clk = txp_clk / 4
11:9	RO	0x0	reserved
8	RW	0x0	dsc_pxl_clk_div Configures DSC pxl_clk clock divider. The pxl_clk drives DSC slice's data path operations. 1'b0: pxl_clk = txp_clk 1'b1: pxl_clk = txp_clk / 2
7	RO	0x0	reserved
6	RW	0x0	dsc_pixel_num Configures DSC input pixel number per cycle. The number of slices per lines must be more than or equal to the number of pixels per clock fed at the DSC encoder pixel input interface. 2'b00: 1 Pixels/cycle 2'b01: 2 Pixels/cycle
5:4	RW	0x0	dsc_inface_mode Configures DSC output compressed data stream interface mode 2'b00: Disable 2'b01: HDMI1 2'b10: MIPI1 Command(DataStream) Mode 2'b11: MIPI1 Video Mode
3	RO	0x0	reserved
2	RW	0x0	dsc_man_mode Enable DSC source selection manual mode. The default pixel source come from MIPI interface 1 or HDMI interface 1.

Bit	Attr	Reset Value	Description
1:0	RW	0x0	dsc_port_sel Configures the DSC pixel stream and pixel clock source. 2'b00: Port0 2'b01: Port1 2'b10: Port2 2'b11: Port3

DSC_SYS_CTRL_DSC_4K_RST
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	dsc_flush DSC datapath flush control. Flush control input is to be asserted to recover from an error condition and subsequently to bring DSC encoder to its initial state. Active level of this input is dependent on the state of Flush Active Level control bit (FLAL - bit 4 in DSC encoder register DSC_CTRL0).
15:1	RO	0x0000	reserved
0	RW	0x0	dsc_soft_rst DSC power on reset. Active Low.

DSC_SYS_CTRL_DSC_4K_CFG_DONE
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	cfg_done When all the register of DSC encoder has been done, writing this bit 1 to unmask input to encoder which will be valid at the next frame start. When received the frame start, the hardware will clear this bit.

DSC_SYS_CTRL_DSC_4K_INIT_DLY_NUM
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	scan_timing_para_imd_en Configure this field to 1 to enable scan timing parameters with immediate effect.
15:0	RW	0x0000	dsc_init_dly_num Configures the initial delay number of compressed clock cycles. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_4K_HTOTAL_HS_END
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_htotal DSC output compressed interface scanning horizontal period. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_hs_end DSC output compressed interface scanning hsync pulse width. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_4K_HACT_ST_END
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_hact_end DSC output compressed interface scanning horizontal active end point. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_hact_st DSC output compressed interface scanning horizontal active start point. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_4K_VTOTAL_VS_END

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_vtotal DSC output compressed interface scanning vertical period. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_vs_end DSC output compressed interface scanning vsync pulse width. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_4K_VACT_ST_END

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsc_vact_end DSC output compressed interface scanning vertical active end point. Valid at the next frame start after set cfg_done = 1.
15:0	RW	0x0000	dsc_vact_st DSC output compressed interface scanning vertical active start point. Valid at the next frame start after set cfg_done = 1.

DSC_SYS_CTRL_DSC_4K_STATUS

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dsc error status This bit equal 1 indicates an error condition detected in DSC encoder. This bit will be clear when host has read the Error Code Word Register in DSC encoder.

DSC_SYS_CTRL_DSC_4K_DEBUG_0

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	compressed_if_n_ready_err This bit assert when compressed data interface ready signal is valid but DSC encoder is not ready to output valid data content. Only used in scan mode.
1	RC	0x0	pixel_if_n_ready_err This bit assert when pixel stream fed in DSC encoder pixel data interface is valid but DSC encoder is not ready to accept data.
0	RO	0x0	reserved

DSC_SYS_CTRL_DSC_4K_DEBUG_1

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	cds_frame_cnt Current DSC output compressed data frame count for debug observation.

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	cds_line_cnt Current DSC output compressed data line count for debug observation.

DSC_SYS_CTRL_DSC_4K_DEBUG_2
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cds_frame_num_err Record the frame number when error status detected.
15:0	RW	0x0000	cds_line_num_err Record the line number when error status detected.

7.5.3.3 OVERLAY

VOP2_OVERLAY_CTRL
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	layer_sel_regdone_sel_imd Select overlay_layer_sel and overlay_port_sel regdone. 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
29	RO	0x0	reserved
28	RW	0x0	layer_sel_regdone_imd Enable interface control register regdone immediately.
27:26	RO	0x0	reserved
25	RW	0x0	sdr2hdr_path_en1 1'b0: Disable 1'b1: Enable
24	RW	0x0	hdr10_path_en1 1'b0: Disable 1'b1: Enable
23:6	RO	0x000	reserved
5	RW	0x0	sdr2hdr_path_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	hdr10_path_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	vp3_overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay
2	RW	0x0	vp2_overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay
1	RW	0x0	vp1_overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay
0	RW	0x0	vp0_overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay

VOP2_OVERLAY_LAYER_SEL
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x7	layer7_sel layer7 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
27	RO	0x0	reserved
26:24	RW	0x6	layer6_sel layer6 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
23	RO	0x0	reserved
22:20	RW	0x5	layer5_sel layer5 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
19	RO	0x0	reserved
18:16	RW	0x4	layer4_sel layer4 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
15	RO	0x0	reserved
14:12	RW	0x3	layer3_sel layer3 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3

Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10:8	RW	0x2	layer2_sel layer2 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
7	RO	0x0	reserved
6:4	RW	0x1	layer1_sel layer1 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3
3	RO	0x0	reserved
2:0	RW	0x0	layer0_sel layer0 select port. 3'b000: Cluster0 3'b001: Cluster1 3'b010: Esmart0 3'b011: Esmart1 3'b100: Cluster2 3'b101: Cluster3 3'b110: Esmart2 3'b111: Esmart3

VOP2_OVERLAY_PORT_SEL
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RW	0x2	esmart3_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
29:28	RW	0x2	esmart2_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
27:26	RW	0x0	esmart1_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3

Bit	Attr	Reset Value	Description
25:24	RW	0x0	esmart0_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
23:22	RW	0x1	cluster3_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
21:20	RW	0x1	cluster2_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
19:18	RW	0x0	cluster1_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
17:16	RW	0x0	cluster0_sel_port 2'b00: Video output0 2'b01: Video output1 2'b10: Video output2 2'b11: Video output3
15	RO	0x0	reserved
14:12	RW	0x7	port3_mux port3 output mux is selected according to the layer number. Note that port3_mux >= port2_mux. 4'b0000: 1 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0001: 2 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0010: 3 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0011: 4 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0100: 5 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0101: 6 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0110: 7 - port0_layer_number - port1_layer_number-port2_layer_number 4'b0111: 8 - port0_layer_number - port1_layer_number-port2_layer_number
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x7	port2_mux port2 output mux is selected according to the layer number. Note that port2_mux >= port1_mux. 4'b0000: 1 - port0_layer_number - port1_layer_number 4'b0001: 2 - port0_layer_number - port1_layer_number 4'b0010: 3 - port0_layer_number - port1_layer_number 4'b0011: 4 - port0_layer_number - port1_layer_number 4'b0100: 5 - port0_layer_number - port1_layer_number 4'b0101: 6 - port0_layer_number - port1_layer_number 4'b0110: 7 - port0_layer_number - port1_layer_number 4'b0111: 8 - port0_layer_number - port1_layer_number 4'b1xxx: 0
7	RO	0x0	reserved
6:4	RW	0x5	port1_mux port1 output mux is selected according to the layer number. Note that port1_mux >= port0_mux. 4'b0000: 1 - port0_layer_number 4'b0001: 2 - port0_layer_number 4'b0010: 3 - port0_layer_number 4'b0011: 4 - port0_layer_number 4'b0100: 5 - port0_layer_number 4'b0101: 6 - port0_layer_number 4'b0110: 7 - port0_layer_number 4'b0111: 8 - port0_layer_number 4'b1xxx: 0
3:0	RW	0x3	port0_mux port0 output mux is selected according to the layer number. 4'b0000: 1 layer 4'b0001: 2 layers 4'b0010: 3 layers 4'b0011: 4 layers 4'b0100: 5 layers 4'b0101: 6 layers 4'b0110: 7 layers 4'b0111: 8 layers 4'b1000: 0 layers

VOP2_OVERLAY_RESERVED_LUT_MST

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved_lut_mst Reserved LUT start address

VOP2_OVERLAY_CLUSTER0_MIX_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster0_mix_src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	cluster0_mix_src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	cluster0_mix_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	cluster0_mix_src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster0_mix_src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster0_mix_src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster0_mix_src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	cluster0_mix_src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_CLUSTER0_MIX_DST_COLOR_CTRL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster0_mix_dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	cluster0_mix_dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster0_mix_dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster0_mix_dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	cluster0_mix_dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	cluster0_mix_dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_CLUSTER0_MIX_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster0_mix_src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster0_mix_src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster0_mix_src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster0_mix_src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_CLUSTER0_MIX_DST_ALPHA_CTRL
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster0_mix_dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster0_mix_dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"

Bit	Attr	Reset Value	Description
3:2	RW	0x0	cluster0_mix_dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster0_mix_dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_CLUSTER1_MIX_SRC_COLOR_CTRL
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster1_mix_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	cluster1_mix_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cluster1_mix_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	cluster1_mix_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster1_mix_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster1_mix_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster1_mix_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	cluster1_mix_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_CLUSTER1_MIX_DST_COLOR_CTRL
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster1_mix_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	cluster1_mix_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster1_mix_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster1_mix_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster1_mix_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	cluster1_mix_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_CLUSTER1_MIX_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster1_mix_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster1_mix_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster1_mix_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster1_mix_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As

Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

VOP2_OVERLAY_CLUSTER1_MIX_DST_ALPHA_CTRL
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster1_mix_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster1_mix_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster1_mix_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster1_mix_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_CLUSTER2_MIX_SRC_COLOR_CTRL
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster2_mix_src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	cluster2_mix_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cluster2_mix_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	cluster2_mix_src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	cluster2_mix_src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster2_mix_src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster2_mix_src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	cluster2_mix_src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_CLUSTER2_MIX_DST_COLOR_CTRL
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster2_mix_dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	cluster2_mix_dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster2_mix_dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster2_mix_dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster2_mix_dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	cluster2_mix_dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_CLUSTER2_MIX_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	cluster2_mix_src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster2_mix_src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster2_mix_src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster2_mix_src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_CLUSTER2_MIX_DST_ALPHA_CTRL

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster2_mix_dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster2_mix_dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster2_mix_dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster2_mix_dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_CLUSTER3_MIX_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	cluster3_mix_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	cluster3_mix_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cluster3_mix_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	cluster3_mix_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster3_mix_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster3_mix_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster3_mix_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	cluster3_mix_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_CLUSTER3_MIX_DST_COLOR_CTRL
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster3_mix_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	cluster3_mix_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads

Bit	Attr	Reset Value	Description
4	RW	0x0	cluster3_mix_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster3_mix_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster3_mix_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	cluster3_mix_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_CLUSTER3_MIX_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster3_mix_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster3_mix_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster3_mix_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster3_mix_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_CLUSTER3_MIX_DST_ALPHA_CTRL

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	cluster3_mix_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster3_mix_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster3_mix_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster3_mix_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_MIX0_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix0_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix0_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix0_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix0_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix0_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix0_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	mix0_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix0_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_MIX0_DST_COLOR_CTRL

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix0_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix0_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix0_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix0_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix0_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix0_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_MIX0_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix0_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	mix0_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix0_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix0_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_MIX0_DST_ALPHA_CTRL
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix0_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix0_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix0_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix0_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_MIX1_SRC_COLOR_CTRL
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix1_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix1_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	mix1_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix1_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix1_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix1_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix1_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix1_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_MIX1_DST_COLOR_CTRL

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix1_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix1_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix1_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix1_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	mix1_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix1_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_MIX1_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix1_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix1_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix1_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix1_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_MIX1_DST_ALPHA_CTRL

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix1_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix1_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"

Bit	Attr	Reset Value	Description
3:2	RW	0x0	mix1_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix1_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_MIX2_SRC_COLOR_CTRL
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix2_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix2_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix2_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix2_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix2_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix2_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix2_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix2_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_MIX2_DST_COLOR_CTRL
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix2_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix2_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix2_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix2_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix2_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix2_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_MIX2_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix2_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix2_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix2_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix2_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As

Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

VOP2_OVERLAY_MIX2_DST_ALPHA_CTRL
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix2_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix2_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix2_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix2_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_MIX3_SRC_COLOR_CTRL
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix3_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix3_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix3_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix3_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	mix3_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix3_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix3_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix3_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_MIX3_DST_COLOR_CTRL
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix3_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix3_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix3_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix3_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix3_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix3_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_MIX3_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	mix3_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix3_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix3_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix3_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_MIX3_DST_ALPHA_CTRL

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix3_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix3_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix3_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix3_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_MIX4_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	mix4_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix4_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix4_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix4_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix4_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix4_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix4_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix4_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_MIX4_DST_COLOR_CTRL
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix4_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix4_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads

Bit	Attr	Reset Value	Description
4	RW	0x0	mix4_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix4_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix4_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix4_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_MIX4_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix4_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix4_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix4_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix4_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_MIX4_DST_ALPHA_CTRL

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	mix4_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix4_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix4_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix4_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_MIX5_SRC_COLOR_CTRL

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix5_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix5_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix5_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix5_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix5_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix5_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	mix5_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix5_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_MIX5_DST_COLOR_CTRL
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix5_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix5_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix5_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix5_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix5_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix5_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_MIX5_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix5_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	mix5_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix5_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix5_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_MIX5_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix5_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix5_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix5_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix5_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_MIX6_SRC_COLOR_CTRL

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix6_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix6_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	mix6_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix6_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix6_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix6_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix6_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix6_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_MIX6_DST_COLOR_CTRL
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix6_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix6_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix6_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix6_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	mix6_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix6_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_MIX6_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix6_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix6_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix6_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix6_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_MIX6_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix6_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix6_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"

Bit	Attr	Reset Value	Description
3:2	RW	0x0	mix6_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix6_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_HDR0_MIX_SRC_COLOR_CTRL

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hdr0_mix_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	hdr0_mix_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	hdr0_mix_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	hdr0_mix_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	hdr0_mix_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	hdr0_mix_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	hdr0_mix_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	hdr0_mix_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_HDR0_MIX_DST_COLOR_CTRL

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hdr0_mix_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	hdr0_mix_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	hdr0_mix_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	hdr0_mix_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	hdr0_mix_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	hdr0_mix_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_HDR0_MIX_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	hdr0_mix_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	hdr0_mix_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	hdr0_mix_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	hdr0_mix_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As

Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

VOP2_OVERLAY_HDR0_MIX_DST_ALPHA_CTRL
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	hdr0_mix_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	hdr0_mix_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	hdr0_mix_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	hdr0_mix_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_HDR1_MIX_SRC_COLOR_CTRL
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hdr1_mix_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	hdr1_mix_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	hdr1_mix_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	hdr1_mix_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	hdr1_mix_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	hdr1_mix_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	hdr1_mix_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	hdr1_mix_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_OVERLAY_HDR1_MIX_DST_COLOR_CTRL
Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hdr1_mix_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	hdr1_mix_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	hdr1_mix_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	hdr1_mix_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	hdr1_mix_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	hdr1_mix_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_OVERLAY_HDR1_MIX_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	hdr1_mix_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	hdr1_mix_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	hdr1_mix_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	hdr1_mix_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_OVERLAY_HDR1_MIX_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	hdr1_mix_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	hdr1_mix_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	hdr1_mix_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	hdr1_mix_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_OVERLAY_DP0_BG_MIX_CTRL

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:24	RW	0x2d	dp_bg_dly_num BG delay cycle number.

Bit	Attr	Reset Value	Description
23:16	RO	0x00	reserved
15:8	RW	0x00	dp_bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	dp_bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
2	RW	0x0	dp_bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	dp_bg_alpha_mode Select source alpha. 1'b0: per_pixel alpha 1'b1: global alpha
0	RW	0x0	dp_bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

VOP2_OVERLAY_DP1_BG_MIX_CTRL
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x31	dp_bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	dp_bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	dp_bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
2	RW	0x0	dp_bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	dp_bg_alpha_mode Select source alpha. 1'b0: per_pixel alpha 1'b1: global alpha
0	RW	0x0	dp_bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

VOP2_OVERLAY_DP2_BG_MIX_CTRL
Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x33	dp_bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	dp_bg_global_alpha Source global alpha value(Ags).

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3	RW	0x0	dp_bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
2	RW	0x0	dp_bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	dp_bg_alpha_mode Select source alpha. 1'b0: per_pixel alpha 1'b1: global alpha
0	RW	0x0	dp_bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

VOP2_OVERLAY_DP3_BG_MIX_CTRL
Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:24	RW	0x33	dp_bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	dp_bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	dp_bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
2	RW	0x0	dp_bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	dp_bg_alpha_mode Select source alpha. 1'b0: per_pixel alpha 1'b1: global alpha
0	RW	0x0	dp_bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

VOP2_OVERLAY_Cluster_DLY_NUM0
Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:24	RW	0x04	cluster1_1_dly_num Cluster1_1 delay cycle number.
23:16	RW	0x04	cluster1_0_dly_num Cluster1_0 delay cycle number.
15:8	RW	0x04	cluster0_1_dly_num Cluster0_1 delay cycle number.
7:0	RW	0x04	cluster0_0_dly_num Cluster0_0 delay cycle number.

VOP2_OVERLAY_Cluster_DLY_NUM1
Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RW	0x04	cluster3_1_dly_num Cluster2_1 delay cycle number.
23:16	RW	0x04	cluster3_0_dly_num Cluster3_0 delay cycle number.
15:8	RW	0x04	cluster2_1_dly_num Cluster2_1 delay cycle number.
7:0	RW	0x04	cluster2_0_dly_num Cluster2_0 delay cycle number.

VOP2_OVERLAY_SMART_DLY_NUM
Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:24	RW	0x17	smart1_dly_num Smart0 delay cycle number.
23:16	RW	0x17	smart0_dly_num Smart0 delay cycle number.
15:8	RW	0x17	esmart1_dly_num Esmart1 delay cycle number.
7:0	RW	0x17	esmart0_dly_num Esmart0 delay cycle number.

7.5.3.4 POST0/1/2/3

VOP2_POST0_DSP_CTRL
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x1	vop_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.

Bit	Attr	Reset Value	Description
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000).
26	RW	0x0	dsp_out_zero 1'b0: Normal output 1'b1: All output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the VSYNC/HSYNC/DATAEN output is blank.
23	RW	0x0	post_lb_mode 1'b0: 4x4096 (for post_act_width > 2048 pixels) 1'b1: 8x2048
22	RW	0x0	gamma_update_en 1'b0: Disable 1'b1: Enable
21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: Allegro 2'b1: FRC
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro).
15	RO	0x0	reserved
14	RW	0x0	dsp_y_mir_en 1'b0: Disable Y mirror 1'b1: Enable Y mirror
13	RW	0x0	dsp_x_mir_en 1'b0: Disable X mirror 1'b1: Enable X mirror
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: Dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: Normal 1'b1: Invert

Bit	Attr	Reset Value	Description
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3:0	RW	0xf	dsp_out_mode Ouput data format: 4'b0000: RGB888 4'b0001: RGB666 4'b0010: RGB565 4'b0011: YUV422 for eDP Interface 4'b1100: YUV422 for DP Interface 4'b1101: YUV420 for DP Interface 4'b1110: YUV420 for HDMI Interface 4'b1111: RGB101010 Others: Reserved

VOP2_POST0_DUAL_DISPLAY_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	edpi_wms_fs Frame start in hold mode. 1'b0: Disable 1'b1: Enable
30	RW	0x0	edpi_wms_hold_en Enable hold mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	edpi_te_mode 1'b0: New frame is started by TE. 1'b1: New frame is started by TE and wms_fs.
28	RW	0x0	edpi_te_en Enable MIPI TE. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	dual_channle_overlap_num 4'h0: overlap num 0 pixels 4'h1: overlap num 2 pixels 4'h2: overlap num 4 pixels 4'h3: overlap num 6 pixels 4'h4: overlap num 8 pixels 4'h5: overlap num 10 pixels 4'h6: overlap num 12 pixels 4'h7: overlap num 14 pixels 4'h8: overlap num 16 pixels
23:22	RO	0x0	reserved
21	RW	0x0	dual_channle_data_swap Swap two channel data. 1'b0: Disable 1'b1: Enable
20	RW	0x0	dual_channle_en Enable dual channel display. 1'b0: Disable 1'b1: Enable
19:0	RO	0x00000	reserved

VOP2_POST0_COLOR_CTRL
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: Horizontal mode 1'b1: Vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

VOP2_POST0_CLK_CTRL
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	dclk_out_sel Configures the divider factor to dclk output clock which used as VOP internal post output clock. (immediate effect) 2'b00: Dclk_out = dclk 2'b01: Dclk_out = dclk / 2 2'b10: Dclk_out = dclk / 4
1:0	RW	0x0	dclk_core_sel Configures the divider factor to dclk core clock which used as VOP internal post scan timing clock. (immediate effect) 2'b00: Dclk_core = dclk 2'b01: Dclk_core = dclk / 2 2'b10: Dclk_core = dclk / 4

VOP2_POST0_3D_LUT_CTRL
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_3dlut_addr AHB write or read LUT address of 3d_LUT.
15:4	RO	0x000	reserved
3	RW	0x0	dsp_3dlut_mode 1'b0: LUT is fetched by AXI 1'b1: LUT is fetched by AHB
2	RW	0x0	dsp_3dlut_update_en Update the LUT of 3d_LUT. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dsp_3dlut_bypass_en Bypass 3d_LUT function. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dsp_3dlut_en 1'b0: Disable 1'b1: Enable

VOP2_POST0_3D_LUT_R
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	lut_3d_r_comp 3D_LUT red component.

VOP2_POST0_3D_LUT_G
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_g_comp 3D_LUT green component.

VOP2_POST0_3D_LUT_B
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_b_comp 3D_LUT blue component.

VOP2_POST0_3DLUT_MST
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	post_3dlut_mst 3D_LUT memory start address.

VOP2_POST0_DSP_BG
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bg_display_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

VOP2_POST0_PRE_SCAN_HTIMING0
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:15	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
14:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

VOP2_POST0_DSP_VACT_INFO_F1
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

VOP2_POST0_DSP_HTOTAL_HS_END
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hs_end Panel display scanning hsync pulse width.

VOP2_POST0_DSP_HACT_ST_END
Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st Panel display scanning horizontal active end point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end Panel display scanning horizontal active end point.

VOP2_POST0_DSP_VTOTAL_VS_END
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end Panel display scanning vsync pulse width.

VOP2_POST0_DSP_VACT_ST_END
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st Panel display scanning vertical active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end Panel display scanning vertical active end point.

VOP2_POST0_DSP_VS_ST_END_F1
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

VOP2_POST0_DSP_VACT_ST_END_F1
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

VOP2_POST0_BCSH_CTRL
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Bypass 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0: Bypass 1'b1: Enable

VOP2_POST0_BCSH_BCS
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	brightness Brightness: {-32,31}.

VOP2_POST0_BCSH_H
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

VOP2_POST0_BCSH_COLOR_BAR
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: BCSH bypass 1'b1: BCSH enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

VOP2_POST0_FRC_LOWER01_0
Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 FRC parameter lower bit = 2'b01, frm1.
15:0	RW	0x4821	lower01_frm0 FRC parameter lower bit = 2'b01, frm0.

VOP2_POST0_FRC_LOWER01_1
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 FRC parameter lower bit = 2'b01, frm3.
15:0	RW	0x8412	lower01_frm2 FRC parameter lower bit = 2'b01, frm2.

VOP2_POST0_FRC_LOWER10_0
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 FRC parameter lower bit = 2'b10, frm1.
15:0	RW	0x9696	lower10_frm0 FRC parameter lower bit = 2'b10, frm0.

VOP2_POST0_FRC_LOWER10_1
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 FRC parameter lower bit = 2'b10, frm3.
15:0	RW	0x6969	lower10_frm2 FRC parameter lower bit = 2'b10, frm2.

VOP2_POST0_FRC_LOWER11_0
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 FRC parameter lower bit = 2'b11, frm1.
15:0	RW	0x7bed	lower11_frm0 FRC parameter lower bit = 2'b11, frm0.

VOP2_POST0_FRC_LOWER11_1
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 FRC parameter lower bit = 2'b11, frm3.
15:0	RW	0xb7de	lower11_frm2 FRC parameter lower bit = 2'b11, frm2.

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VOP2_CLUSTER0_WIN0_CTRL0
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	win0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win0_dither_up_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	win0_uv_swap Only used in line mode. 1'b0: Disable 1'b1: Enable
16	RO	0x0	reserved
15	RW	0x0	win0_alpha_swap Only used in line mode. 1'b0: Disable 1'b1: Enable
14	RW	0x0	win0_rb_swap 1'b0: RGB 1'b1: BGR
13:12	RO	0x0	reserved
11:10	RW	0x0	win0_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020

Bit	Attr	Reset Value	Description
9	RW	0x0	win0_csc_r2y_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	win0_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_no_outstanding 1'b0: Disable 1'b1: Enable
6	RW	0x0	win0_hw_pre_mul_en 1'b0: No hardware pre multiply mode 1'b1: Hardware pre multiply mode
5:1	RW	0x00	win0_data_fmt 5'b00000: ARGB888 5'b00001: RGB888 5'b00010: RGB565 5'b00011: RGB101010 5'b00100: YCbCr420 5'b00101: YCbCr422 5'b00110: YCbCr444 5'b10000: YCbCr420_101010 5'b10001: YCbCr422_101010 5'b10010: YCbCr444_101010 5'b01100: Tile_YCbCr420 5'b01101: Tile_YCbCr422 5'b01110: Tile_YCbCr444 5'b01111: Tile_YCbCr400 5'b11100: Tile_YCbCr420_101010 5'b11101: Tile_YCbCr422_101010 5'b11110: Tile_YCbCr444_101010 5'b11111: Tile_YCbCr400_101010
0	RW	0x0	win0_en 1'b0: Disable 1'b1: Enable

VOP2_CLUSTER0_WIN0_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	win0_yrgb_vsd_gt4 If win0 yrgb_act_height/yrgb_dsp_height > 4, win0_yrgb_vsd_gt4 must be enable.
28	RW	0x0	win0_yrgb_vsd_gt2 If win0 yrgb_act_height/yrgb_dsp_height > 2, win0_yrgb_vsd_gt2 must be enable.
27:20	RO	0x00	reserved
19	RW	0x0	win0_yrgb_vsd_mode 1'b0: Bilinear2
18	RW	0x0	win0_yrgb_vsu_mode 1'b0: Bilinear2
17	RO	0x0	reserved
16	RW	0x0	win0_yrgb_hsd_mode 1'b0: Bilinear2

Bit	Attr	Reset Value	Description
15:14	RW	0x0	win0_yrgb_ver_scl_mode 2'b00: No scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
13:12	RW	0x0	win0_yrgb_hor_scl_mode 2'b00: No scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
11:4	RO	0x00	reserved
3:2	RW	0x0	win0_bic_coe_sel 2'b00: PRECISE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHELL
1	RO	0x0	reserved
0	RW	0x0	win0_yrgb_axi_gather_en Win0 AXI bus yrgb data gather transfer enable.

VOP2_CLUSTER0_WIN0_CTRL2
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:5	RW	0x0	win0_rid_cbr AXI read id of win0 cbr channel
4	RO	0x0	reserved
3:0	RW	0x0	win0_rid_yrgb AXI read id of win0 yrgb channel

VOP2_CLUSTER0_WIN0_YRGB_MST
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb_mst Win0 YRGB frame buffer memory start address.

VOP2_CLUSTER0_WIN0_CBCR_MST
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbcr_mst Win0 CBCR frame buffer memory start address.

VOP2_CLUSTER0_WIN0_VIR
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_uv_vir_stride Number of words of Win0 CbCr virtual width.
15:0	RW	0x0000	win0_vir_stride Number of words of Win0 yrgb virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_CLUSTER0_WIN0_ACT_INFO
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_act_height win_act_height = (win0 vertical size -1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	win0_act_width win_act_width = (win0 horizontal size -1).

VOP2_CLUSTER0_WIN0_DSP_INFO
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_dsp_height win0_dsp_height = (win0 vertical size -1).
15:12	RO	0x0	reserved
11:0	RW	0x000	win0_dsp_width win0_dsp_width = (win0 horizontal size -1).

VOP2_CLUSTER0_WIN0_DSP_ST
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_dsp_yst Win0 vertical start point(y) of the display region.
15:13	RO	0x0	reserved
12:0	RW	0x0000	win0_dsp_xst Win0 horizontal start point(x) of the display region.

VOP2_CLUSTER0_WIN0_DSP_BG
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win0_dsp_bg_red Win0 layer Background Red color.
19:10	RW	0x000	win0_dsp_bg_green Win0 layer Background Green color.
9:0	RW	0x000	win0_dsp_bg_blue Win0 layer Background Blue color.

VOP2_CLUSTER0_WIN0_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_vs_factor_yrgb factor=((LCDC_WIN0_ACT_INFO[31:16]) / (LCDC_WIN0_DSP_INFO[31:16]))*2^12.
15:0	RW	0x0000	win0_hs_factor_yrgb factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_CLUSTER0_WIN0_SCL_OFFSET
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	win0_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved
7:0	RW	0x00	win0_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

VOP2_CLUSTER0_WIN0_TRANSFORMED_OFFSET
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first active pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first active pixel and the first pixel of line.

VOP2_CLUSTER0_WIN0_AFBCD_OUTPUT_CTRL
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	win0_afbcd_gating_en AFBCD gating enable 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

VOP2_CLUSTER0_WIN0_AFBCD_MODE
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	win0_ymir_en 1'b0: Y-mirror disable 1'b1: Y-mirror when AFBCD output
2	RW	0x0	win0_xmir_en 1'b0: X-mirror disable 1'b1: X-mirror when AFBCD output
1	RW	0x0	win0_rot270_en 1'b0: Rotation 270 disable 1'b1: Rotation 270 angle, when AFBCD output
0	RW	0x0	win0_rot90_en 1'b0: Rotation 90 disable 1'b1: Enable, rotation 90 angle when AFBCD output

VOP2_CLUSTER0_WIN0_AFBCD_HDR_PTR
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_afbcd_hdr_ptr AFBC encode stream starting address in DDR.

VOP2_CLUSTER0_WIN0_AFBCD_VIR_WIDTH
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_tail_num Header/payload arbiter tail number.
15:0	RW	0x0000	win0_afbcd_pic_vir_width When AFBCD mode is x_mirror/rot90/rot270, it must be aligned to 64 pixels, else it must be aligned to 16 pixels.

VOP2_CLUSTER0_WIN0_AFBCD_SIZE
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_pic_height This value should equal to (picture height - 1) and aligned to 16 pixels.
15:0	RW	0x0000	win0_afbcd_pic_width This value should equal to (picture width - 1) and aligned to 16 pixels.

VOP2_CLUSTER0_WIN0_AFBCD_PIC_OFFSET
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_pic_yoffset Display image vertical offset in DDR. it must be aligned to 16 pixels.
15:0	RW	0x0000	win0_afbcd_pic_xoffset Display image horizon offset in DDR. it must be aligned to 16 pixels.

VOP2_CLUSTER0_WIN0_AFBCD_DIS_OFFSET
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win0_afbcd_dis_xoffset Display image horizon offset in panel. it can be random.

VOP2_CLUSTER0_WIN0_AFBCD_CTRL
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	win0_afbcd_uv_swap_en win0 AFBCD mode uv swap enable
9	RW	0x0	win0_afbcd_rb_swap_en win0 AFBCD mode rb swap enable
8	RW	0x0	win0_afbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_afbcd_half_block 1'b0: AFBCD full mode, 16 line one tail line 1'b1: AFBCD half mode, 8 line one tail line

Bit	Attr	Reset Value	Description
6:2	RW	0x00	win0_afbcd_pixel_packing_fmt AFBCD data format. 4'h0: RGB565 4'h2: RGBA1010102 4'h3: YUV420_101010 4'h4: RGB888 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: color transform 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	win0_afbcd_video_top_crop video top crop. 2'b00: 0 2'b01: 4 2'b10: 8 others: Reserved

VOP2_CLUSTER0_WIN1_CTRL0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	win1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win1_dither_up_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	win1_uv_swap Only used in line mode. 1'b0: Disable 1'b1: Enable
16	RO	0x0	reserved
15	RW	0x0	win1_alpha_swap Only used in line mode. 1'b0: Disable 1'b1: Enable
14	RW	0x0	win1_rb_swap 1'b0: RGB 1'b1: BGR
13:12	RO	0x0	reserved
11:10	RW	0x0	win1_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
9	RW	0x0	win1_csc_r2y_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	win1_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	win1_no_outstanding 1'b0: Disable 1'b1: Enable
6	RW	0x0	win1_hw_pre_mul_en 1'b0: No hardware pre multiply mode 1'b1: Hardware pre multiply mode
5:1	RW	0x00	win1_data_fmt 5'b00000: ARGB888 5'b00001: RGB888 5'b00010: RGB565 5'b00011: RGB101010 5'b00100: YCbCr420 5'b00101: YCbCr422 5'b00110: YCbCr444 5'b10000: YCbCr420_101010 5'b10001: YCbCr422_101010 5'b10010: YCbCr444_101010
0	RW	0x0	win1_en 1'b0: Disable 1'b1: Enable

VOP2_CLUSTER0_WIN1_CTRL1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	win1_yrgb_vsd_gt4 If win1 yrgb_act_height/yrgb_dsp_height > 4, win1_yrgb_vsd_gt4 must be enable.
28	RW	0x0	win1_yrgb_vsd_gt2 If win1 yrgb_act_height/yrgb_dsp_height > 2, win1_yrgb_vsd_gt2 must be enable.
27:20	RO	0x00	reserved
19	RW	0x0	win1_yrgb_vsd_mode 1'b0: Bilinear2
18	RW	0x0	win1_yrgb_vsu_mode 1'b0: Bilinear2
17	RO	0x0	reserved
16	RW	0x0	win1_yrgb_hsd_mode 1'b0: Bilinear2
15:14	RW	0x0	win1_yrgb_ver_scl_mode 2'b00: No scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
13:12	RW	0x0	win1_yrgb_hor_scl_mode 2'b00: No scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
11:4	RO	0x00	reserved

Bit	Attr	Reset Value	Description
3:2	RW	0x0	win1_bic_coe_sel 2'b00: PRECISE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHELL
1	RO	0x0	reserved
0	RW	0x0	win1_yrgb_axi_gather_en win1 AXI bus yrgb data gather transfer enable.

VOP2_CLUSTER0_WIN1_CTRL2
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:5	RW	0x0	win1_rid_cbr AXI read id of win1 cbr channel
4	RO	0x0	reserved
3:0	RW	0x0	win1_rid_yrgb AXI read id of win1 yrgb channel

VOP2_CLUSTER0_WIN1_YRGB_MST
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_yrgb_mst win1 YRGB frame buffer memory start address.

VOP2_CLUSTER0_WIN1_CBCR_MST
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_cbcr_mst win1 CBCR frame buffer memory start address.

VOP2_CLUSTER0_WIN1_VIR
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_uv_vir_stride Number of words of win1 CbCr virtual width.
15:0	RW	0x0000	win1_vir_stride Number of words of win1 yrgb virtual width. ARGB888: win1_vir_width RGB888: (win1_vir_width*3/4) + (win1_vir_width%3) RGB565: ceil(win1_vir_width/2) YUV: ceil(win1_vir_width/4) YUV tile: ceil(win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win1_vir_width/4)

VOP2_CLUSTER0_WIN1_ACT_INFO
Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_act_height win_act_height = (win1 vertical size -1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	win1_act_width win_act_width = (win1 horizontal size -1).

VOP2_CLUSTER0_WIN1_DSP_INFO
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_dsp_height win1_dsp_height = (win1 vertical size -1).
15:12	RO	0x0	reserved
11:0	RW	0x000	win1_dsp_width win1_dsp_width = (win1 horizontal size -1).

VOP2_CLUSTER0_WIN1_DSP_ST
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_dsp_yst win1 vertical start point(y) of the display region.
15:13	RO	0x0	reserved
12:0	RW	0x0000	win1_dsp_xst win1 horizontal start point(x) of the display region.

VOP2_CLUSTER0_WIN1_DSP_BG
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win1_dsp_bg_red win1 layer Background Red color.
19:10	RW	0x000	win1_dsp_bg_green win1 layer Background Green color.
9:0	RW	0x000	win1_dsp_bg_blue win1 layer Background Blue color.

VOP2_CLUSTER0_WIN1_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_vs_factor_yrgb factor=((LCDC_win1_ACT_INFO[31:16]) / (LCDC_win1_DSP_INFO[31:16]))*2^12.
15:0	RW	0x0000	win1_hs_factor_yrgb factor=((LCDC_win1_ACT_INFO[15:0]) / (LCDC_win1_DSP_INFO[15:0]))*2^12.

VOP2_CLUSTER0_WIN1_SCL_OFFSET
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	win1_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved
7:0	RW	0x00	win1_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

VOP2_CLUSTER0_WIN1_TRANSFORMED_OFFSET
Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first active pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first active pixel and the first pixel of line.

VOP2_CLUSTER0_WIN1_AFBCD_OUTPUT_CTRL
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	win0_afbcd_gating_en AFBCD gating enable 1'b0: Disable 1'b1: Enable
3:0	RO	0x0	reserved

VOP2_CLUSTER0_WIN1_AFBCD_MODE
Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	win0_ymir_en 1'b0: Y-mirror disable 1'b1: Y-mirror when AFBCD output
2	RW	0x0	win0_xmir_en 1'b0: X-mirror disable 1'b1: X-mirror when AFBCD output
1	RW	0x0	win0_rot270_en 1'b0: Rotation 270 disable 1'b1: Rotation 270 angle, when AFBCD output
0	RW	0x0	win0_rot90_en 1'b0: Rotation 90 disable 1'b1: Enable, rotation 90 angle when AFBCD output

VOP2_CLUSTER0_WIN1_AFBCD_HDR_PTR
Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_afbcd_hdr_ptr AFBC encode stream starting address in DDR.

VOP2_CLUSTER0_WIN1_AFBCD_VIR_WIDTH
Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_tail_num Header/payload arbiter tail number.
15:0	RW	0x0000	win0_afbcd_pic_vir_width When AFBCD mode is x_mirror/rot90/rot270, it must be aligned to 64 pixels, else it must be aligned to 16 pixels.

VOP2_CLUSTER0_WIN1_AFBCD_SIZE
Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_pic_height This value should equal to (picture height - 1) and aligned to 16 pixels.
15:0	RW	0x0000	win0_afbcd_pic_width This value should equal to (picture width - 1) and aligned to 16 pixels.

VOP2_CLUSTER0_WIN1_AFBCD_PIC_OFFSET

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_pic_yoffset Display image vertical offset in DDR. it must be aligned to 16 pixels.
15:0	RW	0x0000	win0_afbcd_pic_xoffset Display image horizon offset in DDR. it must be aligned to 16 pixels.

VOP2_CLUSTER0_WIN1_AFBCD_DIS_OFFSET

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win0_afbcd_dis_xoffset Display image horizon offset in panel. it can be random.

VOP2_CLUSTER0_WIN1_AFBCD_CTRL

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	win0_afbcd_uv_swap_en win0 AFBCD mode uv swap enable
9	RW	0x0	win0_afbcd_rb_swap_en win0 AFBCD mode rb swap enable
8	RW	0x0	win0_afbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_afbcd_half_block 1'b0: AFBCD full mode, 16 line one tail line 1'b1: AFBCD half mode, 8 line one tail line
6:2	RW	0x00	win0_afbcd_pixel_packing_fmt AFBCD data format. 4'h0: RGB565 4'h2: RGBA1010102 4'h3: YUV420_101010 4'h4: RGB888 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: color transform 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1:0	RW	0x0	win0_afbcd_video_top_crop video top crop. 2'b00: 0 2'b01: 4 2'b10: 8 others: Reserved

VOP2_CLUSTER0_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	cluster_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:21	RO	0x000	reserved
20	RW	0x0	cluster_wrap_en 1'b0: Disable 1'b1: Enable
19:15	RO	0x00	reserved
14	RW	0x0	cluster_mmu_bypass 1'b0: Disable 1'b1: Enable
13	RW	0x0	cluster_axi_sel 1'b0: Select AXI0 1'b1: Select AXI1
12	RW	0x0	cluster_dma_stop Stop cluster DMA. 1'b0: Disable 1'b1: Enable
11:9	RO	0x0	reserved
8	RW	0x0	cluster_filter_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	cluster_lb_mode CLUSTER line buffer mode, calculated by driver. 2'b00: One window, max width is 4096, AFBCD is half_block mode 2'b01: Two window, max width is 2048, AFBCD is half_block mode 2'b10: One window, max width is 2048, AFBCD is full mode
3	RW	0x0	win1_en_status win1 enable status.
2	RW	0x0	win0_en_status win0 enable status.
1	RW	0x0	cluster_afbcd_en 1'b0: Win0 and win1 AFBCD disable 1'b1: Win0 and win1 AFBCD enable
0	RW	0x0	cluster_en 1'b0: Disable 1'b1: Enable

VOP2_CLUSTER0_LG_COE0

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_lg_coe0 Coefficient of 3x3 matrix.

VOP2_CLUSTER0_LG_COE1
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_lg_coe1 Coefficient of 3x3 matrix.

VOP2_CLUSTER0_LG_COE2
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_lg_coe2 Coefficient of 3x3 matrix.

VOP2_CLUSTER0_HG_COE0
Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_hg_coe0 Coefficient of 3x3 matrix.

VOP2_CLUSTER0_HG_COE1
Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_hg_coe1 Coefficient of 3x3 matrix.

VOP2_CLUSTER0_HG_COE2
Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_hg_coe2 Coefficient of 3x3 matrix.

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VOP2_ESMART0_CTRL0
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_frm_resetn_en 1'b0: Disable 1'b1: Enable
30:5	RO	0x0000000	reserved
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_CTRL1
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: AXI addr add vstep 1'b1: AXI addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart DMA hurry read request thold. If esmart empty lb number >= esmart_DMA_rreq_thold, DMA_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart DMA hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x3	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x3	esmart_yrgb_gather_num The gather number of YRGB.
19:17	RO	0x0	reserved
16:12	RW	0x0b	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:9	RO	0x0	reserved
8:4	RW	0x0a	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x1	esmart_cbcr_gather_en To enable CBCR gather transfer.
2	RW	0x1	esmart_yrgb_gather_en To enable YRGB gather transfer.
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

VOP2_ESMART0_AXI_CTRL
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	esmart_auto_gating_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	esmart_outstanding_num esmart outstanding number.
3	RW	0x0	esmart_outstanding_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	esmart_mmu_bypass 1'b0: Disable 1'b1: Enable
1	RW	0x0	esmart_axi_sel 1'b0: Select AXI0 1'b1: Select AXI1
0	RW	0x0	esmart_dma_sop 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION0_MST_CTL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enabled.
10	RW	0x0	region0_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enabled.
9	RW	0x0	region0_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enabled.
8	RW	0x0	region0_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enabled.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP62 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION0_MST_YRGB

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

VOP2_ESMART0_REGION0_MST_CBCR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART0_REGION0_VIR

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART0_REGION0_ACT_INFO

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region0_act_width win_act_width = (win0 horizontal size -1).

VOP2_ESMART0_REGION0_DSP_INFO
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width dsp_width = horizontal size -1.

VOP2_ESMART0_REGION0_DSP_OFFSET
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART0_REGION0_SCL_CTRL
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region0_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:14	RW	0x0	region0_cbcr_yscl_mode When cbcr_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when cbcr_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
13	RW	0x0	region0_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
12	RW	0x0	region0_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region0_cbcr_xscl_mode When cbcr_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when cbcr_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
9	RW	0x0	region0_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region0_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	region0_yrgb_yscl_mode When yrgb_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when yrgb_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region0_yrgb_xscl_mode When yrgb_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when yrgb_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale

Bit	Attr	Reset Value	Description
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION0_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region0_yrgb_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION0_SCL_FACTOR_CBCR
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_cbcr_yfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_cbcr_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION0_SCL_OFFSET
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region0_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region0_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region0_yrgb_yscl_offset Esmart yrgb vertical scale offset.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART0_REGION1_MST_CTL
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enabled.
10	RW	0x0	region1_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enabled.
9	RW	0x0	region1_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enabled.
8	RW	0x0	region1_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enabled.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION1_MST_YRGB
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

VOP2_ESMART0_REGION1_MST_CBCR
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART0_REGION1_VIR
Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART0_REGION1_ACT_INFO
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region1_act_width win_act_width = (win0 horizontal size -1).

VOP2_ESMART0_REGION1_DSP_INFO
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width dsp_width = horizontal size -1.

VOP2_ESMART0_REGION1_DSP_OFFSET
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART0_REGION1_SCL_CTRL
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region1_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:14	RW	0x0	region1_cbcr_yscl_mode When cbcr_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale When cbcr_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
13	RW	0x0	region1_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
12	RW	0x0	region1_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region1_cbcr_xscl_mode When cbcr_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale When cbcr_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
9	RW	0x0	region1_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region1_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	region1_yrgb_yscl_mode When yrgb_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale When yrgb_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region1_yrgb_xscl_mode When yrgb_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale When yrgb_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale

Bit	Attr	Reset Value	Description
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION1_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region1_yrgb_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION1_SCL_FACTOR_CBCR
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_cbcr_yfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region1_cbcr_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION1_SCL_OFFSET
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region1_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region1_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region1_yrgb_yscl_offset Esmart yrgb vertical scale offset.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART0_REGION2_MST_CTL

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enabled.
10	RW	0x0	region2_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enabled.
9	RW	0x0	region2_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enabled.
8	RW	0x0	region2_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enabled.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION2_MST_YRGB
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

VOP2_ESMART0_REGION2_MST_CBCR
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART0_REGION2_VIR
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART0_REGION2_ACT_INFO
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region2_act_width win_act_width = (win0 horizontal size -1).

VOP2_ESMART0_REGION2_DSP_INFO
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width dsp_width = horizontal size -1.

VOP2_ESMART0_REGION2_DSP_OFFSET
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART0_REGION2_SCL_CTRL
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region2_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:14	RW	0x0	region2_cbcr_yscl_mode When cbcr_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale When cbcr_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
13	RW	0x0	region2_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
12	RW	0x0	region2_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region2_cbcr_xscl_mode When cbcr_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale When cbcr_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
9	RW	0x0	region2_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region2_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	region2_yrgb_yscl_mode When yrgb_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale When yrgb_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region2_yrgb_xscl_mode When yrgb_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale When yrgb_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale

Bit	Attr	Reset Value	Description
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION2_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region2_yrgb_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION2_SCL_FACTOR_CBCR

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_cbcr_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_cbcr_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION2_SCL_OFFSET

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region2_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region2_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region2_yrgb_yscl_offset Esmart yrgb vertical scale offset.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	region2_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART0_REGION3_MST_CTL

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_4gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_4gt must be enabled.
10	RW	0x0	region3_cbcr_2gt If esmart_cbcr_ysd_enc, bilinear is enabled and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_2gt must be enabled.
9	RW	0x0	region3_yrgb_4gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_4gt must be enabled.
8	RW	0x0	region3_yrgb_2gt If esmart_yrgb_ysd_enc, bilinear is enabled and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_2gt must be enabled.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION3_MST_YRGB
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

VOP2_ESMART0_REGION3_MST_CBCR
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART0_REGION3_VIR
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART0_REGION3_ACT_INFO
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region3_act_width win_act_width = (win0 horizontal size -1).

VOP2_ESMART0_REGION3_DSP_INFO
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height esmart0_dsp_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width dsp_width = horizontal size -1.

VOP2_ESMART0_REGION3_DSP_OFFSET
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART0_REGION3_SCL_CTRL
Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region3_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:14	RW	0x0	region3_cbcr_yscl_mode When cbcr_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale When cbcr_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
13	RW	0x0	region3_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
12	RW	0x0	region3_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region3_cbcr_xscl_mode When cbcr_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale When cbcr_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
9	RW	0x0	region3_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region3_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	region3_yrgb_yscl_mode When yrgb_ysu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale When yrgb_ysd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region3_yrgb_xscl_mode When yrgb_xsu_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale When yrgb_xsd_en is enabled. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale

Bit	Attr	Reset Value	Description
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART0_REGION3_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region3_yrgb_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION3_SCL_FACTOR_CBCR
Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_cbcr_yfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_cbcr_xfactor When yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. When yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART0_REGION3_SCL_OFFSET
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region3_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region3_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region3_yrgb_yscl_offset Esmart yrgb vertical scale offset.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	region3_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART0_KEY_CTRL

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

VOP2_ESMART0_BG_EN

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

7.5.3.7 HDR10

VOP2_HDR10_HDR10_LUT_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	hdr10_lut_mode Configure HDR10 register mode. 1'b0: AXI 1'b1: AHB
0	RW	0x0	hdr10_lut_update_en Update HDR10 configure. 1'b0: Disable 1'b1: Enable

VOP2_HDR10_HDR10_LUT_MST

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hdr10_lut_mst HDR10 configure's start address in memory.

VOP2_HDR10_SDR2HDR_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	sdr2hdr_gating_en Enable SDR2HDR auto-gating. 1'b0: Disable 1'b1: Enable
8	RW	0x0	sdr2hdr_bypass_en Bypass SDR2HDR function. 1'b0: Disable 1'b1: Enable
7:4	RO	0x0	reserved
3	RW	0x0	sdr2hdr_oetf_en Enable OETF curve. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sdr2hdr_r2r_mode Select R2R mode. 1'b0: RGB709TORGB2020 1'b1: RGB2020TORGB709
1	RW	0x0	sdr2hdr_r2r_en Enable R2R convert. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sdr2hdr_eotf_en Enable EOTF curve. 1'b0: Disable 1'b1: Enable

VOP2_HDR10_SDR2HDR_CTRL1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	sdr2hdr_gating_en Enable SDR2HDR auto-gating. 1'b0: Disable 1'b1: Enable
8	RW	0x0	sdr2hdr_bypass_en Bypass SDR2HDR function. 1'b0: Disable 1'b1: Enable
7:4	RO	0x0	reserved
3	RW	0x0	sdr2hdr_oetf_en Enable OETF curve. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sdr2hdr_r2r_mode Select R2R mode. 1'b0: RGB709TORGB2020 1'b1: RGB2020TORGB709
1	RW	0x0	sdr2hdr_r2r_en Enable R2R convert. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	sdr2hdr_eotf_en Enable EOTF curve. 1'b0: Disable 1'b1: Enable

VOP2_HDR10_HDR2SDR_CTRL1

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	hdr2sdr_en 1'b0: Disable 1'b1: Enable

VOP2_HDR10_HDR2SDR_CTRL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	hdr2sdr_gating_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	hdr2sdr_bypass_en 1'b0: Disable 1'b1: Enable
7:1	RO	0x00	reserved
0	RW	0x0	hdr2sdr_en 1'b0: Disable 1'b1: Enable

VOP2_HDR10_HDR2SDR_SRC_RANGE

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	src_max Source max luminance.
15:14	RO	0x0	reserved
13:0	RW	0x0000	src_min Source min luminance.

VOP2_HDR10_HDR2SDR_NORFACEETF

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	normfaceetf Normalization eetf factor.

VOP2_HDR10_HDR2SDR_DST_RANGE

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dst_max Destination max luminance.
15:0	RW	0x0000	dst_min Destination min luminance.

VOP2_HDR10_HDR2SDR_NORMFACCGAMMA

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	normfaccgamma Normalization gamma factor.

VOP2_HDR10_EETF_OETF0

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF1

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF2

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF3

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF4

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF5

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF6

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF7

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF8

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF9

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF10

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF11
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF12
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF13
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF14
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF15
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF16
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF17
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF18
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF19
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF20
Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF21

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF22

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF23

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF24

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF25

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF26

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF27
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF28
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF29
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF30
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF31
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_EETF_OETF32
Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_HDR10_SAT_Y0
Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y1
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y2
Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y3
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y4
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y5
Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y6
Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y7
Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_SAT_Y8
Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_HDR10_EOTF_OETF_Y0
Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y1
Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y2
Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y3
Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y4
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st2084oetf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y5

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st2084oetf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y6

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st2084oetf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y7

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st2084oetf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y8

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st2084oetf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y9

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st2084oetf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y10

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st2084oetf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y11

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y12

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y13

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y14

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y15

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y16

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y17

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y18
Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y19
Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y20
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y21
Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y22
Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y23
Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y24
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y25
Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y26
Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y27
Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y28
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y29
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y30
Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y31
Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.

Bit	Attr	Reset Value	Description
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y32
Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y33
Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y34
Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y35
Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y36
Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y37
Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf_y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf_y.

VOP2_HDR10_EOTF_OETF_Y38
Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y39
Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y40
Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y41
Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y42
Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y43
Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y44
Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y45

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y46

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y47

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y48

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y49

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y50

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y51

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y52
Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y53
Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y54
Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y55
Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y56
Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y57
Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y58
Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y59
Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y60
Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y61
Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y62
Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y63
Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_EOTF_OETF_Y64
Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_HDR10_OETF_DX_DXPOW1
Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW2
Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW3
Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW4
Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW5
Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW6
Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW7
Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW8
Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW9
Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW10
Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW11
Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW12
Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW13
Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW14
Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW15
Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW16
Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW17
Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW18
Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW19
Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW20
Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW21
Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW22
Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW23
Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW24
Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW25
Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW26
Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW27
Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW28
Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW29
Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW30
Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW31
Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW32
Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW33
Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW34
Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW35
Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW36
Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW37
Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW38
Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW39
Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW40
Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW41
Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW42
Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW43
Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW44
Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW45
Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW46
Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW47
Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW48
Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW49
Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW50
Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW51
Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW52
Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW53
Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW54
Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW55
Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW56
Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW57
Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW58
Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW59
Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW60
Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW61
Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW62
Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW63
Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_DX_DXPOW64
Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_HDR10_OETF_XN1
Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN2
Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN3
Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN4
Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN5
Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN6
Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN7
Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN8
Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN9
Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN10
Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN11
Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN12

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN13

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN14

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN15

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN16

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN17

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN18

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN19

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN20
Address: Operational Base + offset (0x034C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN21
Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN22
Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN23
Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN24
Address: Operational Base + offset (0x035C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN25
Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN26
Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN27
Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN28
Address: Operational Base + offset (0x036C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN29
Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN30
Address: Operational Base + offset (0x0374)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN31
Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN32
Address: Operational Base + offset (0x037C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN33
Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN34
Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN35
Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN36
Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN37
Address: Operational Base + offset (0x0390)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN38
Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN39
Address: Operational Base + offset (0x0398)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN40
Address: Operational Base + offset (0x039C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN41
Address: Operational Base + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN42
Address: Operational Base + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN43
Address: Operational Base + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN44
Address: Operational Base + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN45
Address: Operational Base + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN46
Address: Operational Base + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN47
Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN48
Address: Operational Base + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN49
Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN50
Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN51

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN52
Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN53
Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN54
Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN55
Address: Operational Base + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN56
Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN57
Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN58
Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN59
Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN60
Address: Operational Base + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN61
Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN62
Address: Operational Base + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_HDR10_OETF_XN63
Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

7.5.3.8 DSC_8K

DSC_8K_PPS0_3
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:28	RW	0xa	BPC This field indicates the number of bits per component for the original pixels of the encoded picture. 4'b1000: BPC8 4'b1010: BPC10 4'b1100: BPC12 4'b1110: BPC14 4'b0000: BPC16

Bit	Attr	Reset Value	Description
27:24	RW	0xb	LBD This field contains the line buffer bit depth used for Line buffer memories. If the bit depth (after color space conversion) of a component is greater than this value, the line storage rounds the reconstructed values to this number of bits. 4'b1000: Line buffer bit depth is 8. 4'b1001: Line buffer bit depth is 9. 4'b1010: Line buffer bit depth is 10. 4'b1011: Line buffer bit depth is 11. 4'b1100: Line buffer bit depth is 12. 4'b1101: Line buffer bit depth is 13. 4'b1110: Line buffer bit depth is 14. 4'b1111: Line buffer bit depth is 15. 4'b0000: Line buffer bit depth is 16.
23:16	RO	0x00	reserved
15:8	RW	0x00	PPSID This field represents PPS identifier. Program PPS table-0 registers.
7:4	RW	0x1	MJV This field contains major version of DSC.
3:0	RW	0x2	MNV This field contains minor version of DSC. 4'b0001: DSC1.1 4'b0010: DSC1.2

DSC_8K_PPS4_7

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0xe0	PCHL Picture height, lower bits. This field specifies the lower 8 bits of picture height, in units of pixel rows. Picture height {PCHH [7:0], PCHL [7:0]} is the number of pixel rows within the raster. Although not required, it is recommended that picture height be close to integer multiples of slice height. Minimum Slice height is 4.
23:16	RW	0x10	PCHH Picture height, higher bits.
15:8	RW	0x60	BPPL Bits per pixel lower bits. This field specifies the lower 8bits of target per pixel for the compressed bit stream. The resolution per bit 1/16 of a bit per pixel; Minimum value of BPP={BPPH[1:0], BPPL[7:0]} >= 0x60,corresponds to 6.0;
7:6	RO	0x0	reserved
5	RW	0x1	BPE Block prediction enable. 1'b0: Block prediction is not used. 1'b1: Block prediction is used.
4	RW	0x1	CRGB The field indicates whether the color space is RGB/YCbCr. In color space RGB mode, conversion from RGB to YCoCg-R and vice versa is supported. 1'b0: YCbCr 1'b1: RGB

Bit	Attr	Reset Value	Description
3	RW	0x0	S422 Simple 422 mode of operation. S422 bit must be 0 when operation in native modes. 1'b0: Not operating in simple 422 mode. 1'b1: Operating in simple 422 mode.
2	RW	0x0	VBR Variable bit rate mode (VBR) is not supported. This field indicates variable bit rate mode of operation. 1'b0: Variable bit rate disabled. 1'b1: Variable bit rate enabled.
1:0	RW	0x0	BPPH This field specifies the upper 2 bits of target bits per pixel for the compressed bit stream. The resolution per bit 1/16 of a bit per pixel; Minimum value of BPP={BPPH[1:0], BPPL[7:0]} >= 0x60,corresponds to 6.0;

DSC_8K_PPS8_11
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0xe0	SLHL Slice height, lower bits. This field specifies the lower 8 bits of Slice height, in units of pixel lines. Slice height SLH = {SLHH [7:0], SLHL [7:0]} is the number of pixel rows within the raster for the given slice. Although not required, it is recommended that picture height be close to integer multiples of slice height. Minimum slice height is 4.
23:16	RW	0x10	SLHH Slice height, higher bits.
15:8	RW	0x00	PCWL Picture width, lower bits.
7:0	RW	0x1e	PCWH Picture width, higher bits.

DSC_8K_PPS12_15
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	CHSL Chunk size, lower bits.
23:16	RW	0x16	CHSH Chunk size, higher bits.
15:8	RW	0x00	SLWL Slice width, lower bits. This field specifies the lower 8 bits of Slice Width, in units of pixels. Slice Width {SLWH [7:0], SLWL [7:0]} is the number of pixel columns within the raster for the given slice. Although not required, it is recommended that picture width be close to integer multiples of slice width.
7:0	RW	0x1e	SLWH Slice width, higher bits.

DSC_8K_PPS16_19
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	IDDL This field specifies the lower 8 bits of initial decoding delay.
23:16	RW	0xb4	IDDH This field specifies the higher 8 bits of initial decoding delay.
15:8	RW	0xaa	IXDL This field specifies the lower 8 bits of initial transmit delay of the encoder.
7:2	RO	0x00	reserved
1:0	RW	0x2	IXDH This field specifies the higher 2 bits of initial transmit delay of the encoder.

DSC_8K_PPS20_23
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	SIIL Scale increment interval, lower bits.
23:16	RW	0x01	SIIH Scale increment interval, higher bits.
15:14	RO	0x0	reserved
13:8	RW	0x20	ISV Initial scale value.
7:0	RO	0x00	reserved

DSC_8K_PPS24_27
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0f	FBO First line BPG offset. SLH >=8: FBO=12+(int)(0.09*MIN(34,SLH-8)) SLH<8: FBO=2*(SLH-1)
23:16	RO	0x00	reserved
15:8	RW	0x01	SDIL Scale decrement interval, lower bits.
7:4	RO	0x0	reserved
3:0	RW	0x0	SDIH Scale decrement interval, higher bits.

DSC_8K_PPS28_31
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RW	0x14	SBOL Slice BPG offset, lower bits.
23:16	RW	0x0d	SBOH Slice BPG offset, higher bits.
15:8	RW	0xe7	NFBOL Non-first line BPG offset, lower bits.
7:0	RW	0x01	NFBOH Non-first line BPG offset, higher bits.

DSC_8K_PPS32_35
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RW	0xfe	FNOL Final offset, lower bits.
23:16	RW	0x10	FNOH Final offset, higher bits.
15:8	RW	0x00	INOL Initial offset, lower bits.
7:0	RW	0x18	INOH Initial offset, higher bits.

DSC_8K_PPS36_39
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	RCMSL RC model size, lower bits.
23:16	RW	0x20	RCMSH RC model size, higher bits.
15:13	RO	0x0	reserved
12:8	RW	0x0c	FMXQ Flatness max QP.
7:5	RO	0x0	reserved
4:0	RW	0x03	FMNQ Flatness min QP.

DSC_8K_PPS40_43
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RW	0x3	RCTOH RC target offset higher limit.
27:24	RW	0x3	RCTOL RC target offset lower limit.
23:21	RO	0x0	reserved
20:16	RW	0x0b	RCQIL1 RC quantization increment limit 1.
15:13	RO	0x0	reserved
12:8	RW	0x0b	RCQIL0 RC quantization increment limit 0.
7:4	RO	0x0	reserved
3:0	RW	0x6	RCEF RC edge factor

DSC_8K_PPS44_47
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x38	RCBT3 RC buffer threshold-3.
23:16	RW	0x2a	RCBT2 RC buffer threshold-2.
15:8	RW	0x1c	RCBT1 RC buffer threshold-1.
7:0	RW	0x0e	RCBT0 RC buffer threshold-0.

DSC_8K_PPS48_51
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RW	0x69	RCBT7 RC buffer threshold-7.
23:16	RW	0x62	RCBT6 RC buffer threshold-6.
15:8	RW	0x54	RCBT5 RC buffer threshold-5.
7:0	RW	0x46	RCBT4 RC buffer threshold-4.

DSC_8K_PPS52_55
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x7b	RCBT11 RC buffer threshold-11.
23:16	RW	0x79	RCBT10 RC buffer threshold-10.
15:8	RW	0x77	RCBT9 RC buffer threshold-9.
7:0	RW	0x70	RCBT8 RC buffer threshold-8.

DSC_8K_PPS56_59
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:8	RW	0x7e	RCBT13 RC buffer threshold-13.
7:0	RW	0x7d	RCBT12 RC buffer threshold-12.

DSC_8K_PPS60_63
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_8K_PPS64_67
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].

Bit	Attr	Reset Value	Description
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_8K_PPS68_71

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

Bit	Attr	Reset Value	Description
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_8K_PPS72_75

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].

Bit	Attr	Reset Value	Description
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_8K_PPS76_79

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_8K_PPS80_83

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_8K_PPS84_87

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

Bit	Attr	Reset Value	Description
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_8K_PPS88_91
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	NSLBOL Non-second line BPG offset lower bits.
23:16	RW	0x00	NSLBOH Non-second line BPG offset higher bits.
15:13	RO	0x0	reserved
12:8	RW	0x00	SLBO Second line BPG offset bits.
7:2	RO	0x00	reserved
1	RW	0x0	N420 Native420 mode. 1'b0: Disable 1'b1: Enable
0	RW	0x0	N422 Native422 mode. 1'b0: Disable 1'b1: Enable

DSC_8K_PPS92_95

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SLOAL Second line offset adjust lower bits.
7:0	RW	0x00	SLOAH Second line offset adjust higher bits.

DSC_8K_VERSION

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x10000110	VERSION DSC Encoder IP release version information.

DSC_8K_CFG_REG0

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x1	PPSREG 0x1 (PPS_REG): PPS Registers Interface is present
29:27	RO	0x3	MNSLC 0x3 (NSLC8): 8 slice per line
26	RO	0x0	reserved
25:24	RO	0x0	FYYP 0x0 (ENCODER): Encoder Function when Encoder feature is selected. Otherwise, Reserved.
23:20	RO	0x1	MJV_ABL This field indicates the number of bits of precision within the line buffer. This field contains the line buffer bit depth used to generate the bit-stream. If a component's bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits. 0xb (LBD11): Line buffer bit depth is 11
19:16	RO	0x2	MNV_ABL DSC Minor Version Support This field indicates the Minor version supported in the configuration. Values: 0x1 (DSC_v11): Supports VESA DSC v1.1 0x2 (DSC_v12): Supports both VESA DSC 1.2a and DSC1.1
15:14	RO	0x0	reserved
13	RO	0x0	N422_ABL 0x0 (NOT_SUPPORTED): Native 422 mode is not supported.
12	RO	0x0	N420_ABL 0x0 (NOT_SUPPORTED): Native 420 mode is not supported.
11:8	RO	0xb	LBFD This field indicates the number of bits of precision within the line buffer. This field contains the line buffer bit depth used to generate the bit-stream. If a component's bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits. 0xb (LBD11): Line buffer bit depth is 11

Bit	Attr	Reset Value	Description
7:4	RO	0xa	NBPC This field indicates the Native Bits per Component of the Display (Maximum Bits per Component set during configuration of DSC encoder) 0xa (BPC10): Bits per component is 10
3:2	RO	0x0	reserved
1	RO	0x0	VBA This field indicates the availability of Variable Bit Rate (VBR) in the configuration. 0x0 (NOT_SUPPORTED): Variable Bit Rate is not supported
0	RO	0x1	BPA This field indicates the availability of Block Prediction (BP) feature in the configuration. 0x1 (SUPPORTED): Block Prediction is supported

DSC_8K_CFG_REG1
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x1e00	MPCW Maximum Picture Width This field represents the maximum picture width (maximum number of pixels per raster/line) supported by the configuration.
15:0	RO	0x10e0	MPCH Maximum Picture Height This field represents the maximum picture height (Maximum number of pixel rows within the raster) supported by the configuration.

DSC_8K_CFG_REG2
Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x10e0	RES Rate Buffer Size (in bytes)

DSC_8K_CFG_REG3
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RO	0x1e00	MSLW Maximum Slice Width
15:0	RO	0x10e0	MSLH Maximum Slice Height

DSC_8K_CTRL0
Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31	RW	0x0	PPS_UPD PPS update. This field provides a control to indicate to DSC encoder that a PPS update has been done. The host can intimate PPS update by setting this bit. DSC encoder clears this bit after the PPS update is accepted. Note: This bit must be written only after all the necessary PPS registers are programmed with desired values. Otherwise, behavior of DSC encoder is undefined.

Bit	Attr	Reset Value	Description
30	RO	0x0	reserved
29	RW	0x1	IFEP ICH full error precision. Note: The IFEP bit is available only in VESA DSC 1.2a Encoder configuration. Its programmed value is considered when operating in VESA DSC ENC v1.2a mode only. 1'b0: ICH error is truncated in accordance with the bits per component programmed in the PPS. 1'b1: Full precision of ICH error is retained.
28	RW	0x0	SBO Single burst output. 1'b0: DSC output data can be discontinuous for a data line. 1'b1: DSC outputs data in a single burst for a data line.
27:19	RO	0x000	reserved
18:16	RW	0x0	NSLC Number of slices per line. This field provides control to enable required number of data path units (equivalently number of slices per line) in a configuration. 3'b000: 1 slice per line 3'b001: 2 slice per line 3'b010: 4 slice per line 3'b100: 8 slice per line
15:9	RO	0x00	reserved
8	RW	0x0	INIT Datapath initialization control. 1'b0: Init control is not asserted 1'b1: Init control is asserted
7	RW	0x0	EPL Enable partial bytes at every line end on CDS interface. 1'b0: Disable 1'b1: Enable
6	RW	0x0	EPB Enable partial bytes at chunk ends on CDS interface. 1'b0: Disable 1'b1: Enable
5	RW	0x0	MER This field provides a way to mask the error reporting through the dsc_err_o port. An error detected in DSC encoder results in assertion of dsc_err_o port and the corresponding Error Status is captured in the Error Status Register. 0x0: Error reporting on dsc_err_o is not masked. So, when an error is detected, dsc_err_o is asserted and the corresponding error code word is captured in the Error Status Register. 0x1: Error reporting on dsc_err_o is masked and only the Error status is captured in the Error Status register.
4	RW	0x1	FLAL This field provides a way to specify the active level of the flush control input, dsc_flush_i. By default, dsc_flush_i is considered as active high signal. 0x0: Dsc_flush_i is treated as active low signal and a falling edge of dsc_flush_i triggers an initialization cycle in DSC encoder. 0x1: Dsc_flush_i is treated as active high signal and a rising edge of dsc_flush_i triggers an initialization cycle in DSC encoder.

Bit	Attr	Reset Value	Description
3	RW	0x0	RBYT Reverse data bytes. This field controls the order of packing of data bytes on the compressed data interface. This field provides a control to reverse byte positions of data bytes on CDS interface. 1'b0: Disable 1'b1: Enable
2	RW	0x0	RBIT This field controls the order of packing of data bits on the compressed data interface. This field provides a control to reverse bits' organization in each byte of the data bytes on Compressed Data Interface. 1'b0: Disable 1'b1: Enable
1	RO	0x0	FSEL 1'b0: Encoder function
0	RW	0x0	EN This field is used to control the operation of DSC encoder. Host has to write to this bit to enable the operation of DSC encoder. Failing to follow the recommended initialization sequence might lead to undefined behavior.

DSC_8K_CTRL1
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:8	RW	0x1000	RBFTH Rate buffer threshold for overflow(bits). Rate buffer threshold value to trigger buffer fullness. A non-zero initial_xmit_delay allows a final maximum buffer fullness of up to initial_xmit_delay* bits_per_pixel. initial_xmit_delay * bits_per_pixel ~= rc_model_size * 0.5.
7:0	RW	0x00	PPS_SEL PPS table select. If only one PPS table is supported, the value must be 0.

DSC_8K_STS0
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RBOF Rate buffer overflow status. RBUF[i] = 0: No overflow detected in rate buffer of slice-i. RBUF[i] = 1: Overflow detected in rate buffer of slice-i.
15:0	RC	0x00ff	RBUF Rate buffer underflow status. RBUF[i] = 0: No underflow detected in rate buffer of slice-i. RBUF[i] = 1: Underflow detected in rate buffer of slice-i.

DSC_8K_STS1
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LBOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in line buffer of slice-i. LBUF[i] = 1: Overflow detected in line buffer of slice-i.

Bit	Attr	Reset Value	Description
15:0	RW	0x00ff	LBUF Line buffer underflow status. LBUF[i] = 0: No underflow detected in line buffer of slice-i. LBUF[i] = 1: Underflow detected in line buffer of slice-i.

DSC_8K_STS2
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	FSOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in line buffer of slice-i. LBUF[i] = 1: Overflow detected in line buffer of slice-i.
15:0	RW	0x00ff	FSUF Funnel shift underflow status. FBUF[i] = 0: No underflow detected in funnel shifts of slice-i. FBUF[i] = 1: Underflow detected in funnel shifts of slice-i.

DSC_8K_STS3
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	SEOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in line buffer of slice-i. LBUF[i] = 1: Overflow detected in line buffer of slice-i.
15:0	RW	0x00ff	SEUF Syntax element size FIFO underflow status. SEUF[i] = 0: No underflow detected in syntax element size FIFOs of slice-i. SEUF[i] = 1: Underflow detected in syntax element size FIFOs of slice-i.

DSC_8K_STS4
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	BLOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in balance FIFOs of slice-i. LBUF[i] = 1: Overflow detected in balance FIFOs of slice-i.
15:0	RW	0x00ff	BLUF Balance FIFO underflow status. BLUF[i] = 0: No underflow detected in balance FIFOs of slice-i. BLUF[i] = 1: Underflow detected in balance FIFOs of slice-i.

DSC_8K_STS5
Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PBOF Pixel buffer overflow status. PBUF[i] = 0: No overflow detected in pixel buffer of slice-i. PBUF[i] = 1: Overflow detected in pixel buffer of slice-i.
15:0	RW	0x00ff	PBUF Pixel buffer underflow status. PBUF[i] = 0: No underflow detected in pixel buffer of slice-i. PBUF[i] = 1: Underflow detected in pixel buffer of slice-i.

DSC_8K_ERS
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RC	0xffffffff	ECW This field reports any error detected in either in PPS, frame processing or in reset sequence. Any error reported through the ECW register needs re-initialization of DSC encoder by asserting INIT through CTRL0 register. Without the re-initialization, the behavior of encoder is undefined.

7.5.3.9 DSC_4K

DSC_4K_PPS0_3
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:28	RW	0xa	BPC 4'b1000: BPC8 4'b1010: BPC10 4'b1100: BPC12 4'b1110: BPC14 4'b0000: BPC16
27:24	RW	0xb	LBD 4'b1000: Line buffer bit depth is 8. 4'b1001: Line buffer bit depth is 9. 4'b1010: Line buffer bit depth is 10. 4'b1011: Line buffer bit depth is 11. 4'b1100: Line buffer bit depth is 12. 4'b1101: Line buffer bit depth is 13. 4'b1110: Line buffer bit depth is 14. 4'b1111: Line buffer bit depth is 15. 4'b0000: Line buffer bit depth is 16.
23:16	RO	0x00	reserved
15:8	RW	0x00	PPSID This field represents PPS identifier. Program PPS table-0 registers.
7:4	RW	0x1	MJV This field contains major version of DSC.
3:0	RW	0x2	MNV This field contains minor version of DSC. 4'b0001: DSC1.1 4'b0010: DSC1.2

DSC_4K_PPS4_7
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x70	PCHL Picture height, lower bits.
23:16	RW	0x08	PCHH Picture height, higher bits.

Bit	Attr	Reset Value	Description
15:8	RW	0x60	BPPL Bits per pixel lower bits. This field specifies the lower 8bits of target per pixel for the compressed bit stream. The resolution per bit 1/16 of a bit per pixel; Minimum value of BPP={BPPH[1:0], BPPL[7:0]} >= 0x60,corresponds to 6.0; For native 420/422 modes must be programmed with a value which is twice the target bits per pixel rate.
7:6	RO	0x0	reserved
5	RW	0x1	BPE Block prediction enable. 1'b0: Block prediction is not used. 1'b1: Block prediction is used.
4	RW	0x1	CRGB The field indicates whether the color space is RGB/YCbCr. In color space RGB mode, conversion from RGB to YCoCg-R and vice versa is supported. 1'b0: YCbCr 1'b1: RGB
3	RW	0x0	S422 Simple 422 mode of operation. S422 bit must be 0 when operation in native modes. 1'b0: Not operating in simple 422 mode. 1'b1: Operating in simple 422 mode.
2	RW	0x0	VBR This field indicates variable bit rate mode of operation. 1'b0: Variable bit rate disabled. 1'b0: Variable bit rate enabled.
1:0	RW	0x0	BPPH This field specifies the upper 2 bits of target bits per pixel for the compressed bit stream. The resolution per bit 1/16 of a bit per pixel; Minimum value of BPP={BPPH[1:0], BPPL[7:0]} >= 0x60,corresponds to 6.0; For native 420/422 modes must be programmed with a value which is twice the target bits per pixel rate.

DSC_4K_PPS8_11
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x70	SLHL Slice height, lower bits.
23:16	RW	0x08	SLHH Slice height, higher bits.
15:8	RW	0x00	PCWL Picture width, lower bits.
7:0	RW	0x10	PCWH Picture width, higher bits.

DSC_4K_PPS12_15
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CHSL Chunk size, lower bits. This field specifies the lower 8bits of chunk size in bytes. If VBR bit is set to 1, this {CHSH[7:0],CHSL[7:0]} represents the maximum size of the chunks. N422 = 0 && N420=0: ceil(BPP * SLW/8) bytes.
23:16	RW	0x0c	CHSH Chunk size, higher bits. This field specifies the higher 2bits of chunk size in bytes. If VBR bit is set to 1, this {CHSH[7:0],CHSL[7:0]} represents the maximum size of the chunks. N422 = 0 && N420=0: ceil(BPP * SLW/8) bytes.
15:8	RW	0x00	SLWL Slice width, lower bits.
7:0	RW	0x10	SLWH Slice width, higher bits.

DSC_4K_PPS16_19

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	IDDL This field specifies the lower 8 bits of initial decoding delay.
23:16	RW	0x60	IDDH This field specifies the higher 8 bits of initial decoding delay.
15:8	RW	0xaa	IXDL This field specifies the lower 8 bits of initial transmit delay of the encoder.
7:2	RO	0x00	reserved
1:0	RW	0x2	IXDH This field specifies the higher 2 bits of initial transmit delay of the encoder.

DSC_4K_PPS20_23

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	SIIL Scale increment interval, lower bits.
23:16	RW	0x01	SIIH Scale increment interval, higher bits.
15:14	RO	0x0	reserved
13:8	RW	0x20	ISV Initial scale value.
7:0	RO	0x00	reserved

DSC_4K_PPS24_27

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0f	FBO First line BPG offset. SLH >=8: FBO=12+(int)(0.09*MIN(34,SLH-8)) SLH<8: FBO=2*(SLH-1)
23:16	RO	0x00	reserved
15:8	RW	0x01	SDIL Scale decrement interval, lower bits.

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3:0	RW	0x0	SDIH Scale decrement interval, higher bits.

DSC_4K_PPS28_31
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RW	0x14	SBOL Slice BPG offset, lower bits.
23:16	RW	0x0d	SBOH Slice BPG offset, higher bits.
15:8	RW	0xe7	NFBOL Non-first line BPG offset, lower bits.
7:0	RW	0x01	NFBOH Non-first line BPG offset, higher bits.

DSC_4K_PPS32_35
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RW	0xfe	FNOL Final offset, lower bits.
23:16	RW	0x10	FNOH Final offset, higher bits.
15:8	RW	0x00	INOL Initial offset, lower bits.
7:0	RW	0x18	INOH Initial offset, higher bits.

DSC_4K_PPS36_39
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	RCMSL RC model size, lower bits.
23:16	RW	0x20	RCMSH RC model size, higher bits.
15:13	RO	0x0	reserved
12:8	RW	0x0c	FMXQ Flatness max QP.
7:5	RO	0x0	reserved
4:0	RW	0x03	FMNQ Flatness min QP.

DSC_4K_PPS40_43
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RW	0x3	RCTOH RC target offset higher limit.
27:24	RW	0x3	RCTOL RC target offset lower limit.
23:21	RO	0x0	reserved
20:16	RW	0x0b	RCQIL1 RC quantization increment limit 1.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x0b	RCQIL0 RC quantization increment limit 0.
7:4	RO	0x0	reserved
3:0	RW	0x6	RCEF RC edge factor

DSC_4K_PPS44_47
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x38	RCBT3 RC buffer threshold-3.
23:16	RW	0x2a	RCBT2 RC buffer threshold-2.
15:8	RW	0x1c	RCBT1 RC buffer threshold-1.
7:0	RW	0x0e	RCBT0 RC buffer threshold-0.

DSC_4K_PPS48_51
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RW	0x69	RCBT7 RC buffer threshold-7.
23:16	RW	0x62	RCBT6 RC buffer threshold-6.
15:8	RW	0x54	RCBT5 RC buffer threshold-5.
7:0	RW	0x46	RCBT4 RC buffer threshold-4.

DSC_4K_PPS52_55
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x7b	RCBT11 RC buffer threshold-11.
23:16	RW	0x79	RCBT10 RC buffer threshold-10.
15:8	RW	0x77	RCBT9 RC buffer threshold-9.
7:0	RW	0x70	RCBT8 RC buffer threshold-8.

DSC_4K_PPS56_59
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

Bit	Attr	Reset Value	Description
25:23	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:8	RW	0x7e	RCBT13 RC buffer threshold-13.
7:0	RW	0x7d	RCBT12 RC buffer threshold-12.

DSC_4K_PPS60_63
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].

Bit	Attr	Reset Value	Description
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_4K_PPS64_67

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_4K_PPS68_71

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_4K_PPS72_75

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].

Bit	Attr	Reset Value	Description
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_4K_PPS76_79

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

Bit	Attr	Reset Value	Description
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_4K_PPS80_83
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].

Bit	Attr	Reset Value	Description
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_4K_PPS84_87

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	RCRP1_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
27:26	RW	0x0	RCRP1_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
25:23	RW	0x0	RCRP1_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
22:21	RW	0x0	RCRP1_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
20:18	RW	0x0	RCRP1_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
17:16	RW	0x0	RCRP1_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
15:12	RW	0x0	RCRP0_RGBPO_L For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[3:0].
11:10	RW	0x0	RCRP0_MXQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].
9:7	RW	0x0	RCRP0_MNQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
6:5	RW	0x0	RCRP0_RGBPO_H For range-0, this field specifiers the target bits per group adjustment that is performed if the RC model has tracked to the current range[5:4].
4:2	RW	0x0	RCRP0_MXQRG_L For range-0, this field specifiers the maximum QP that is allowed if the RC model has tracked to the current range[2:0].
1:0	RW	0x0	RCRP0_MNQRG_H For range-0, this field specifiers the minimum QP that is allowed if the RC model has tracked to the current range[4:3].

DSC_4K_PPS88_91
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	NSLBOL Non-second line BPG offset lower bits.
23:16	RW	0x00	NSLBOH Non-second line BPG offset higher bits.
15:13	RO	0x0	reserved
12:8	RW	0x00	SLBO Second line BPG offset bits.
7:2	RO	0x00	reserved
1	RW	0x0	N420 Native420 mode. 1'b0: Disable 1'b1: Enable
0	RW	0x0	N422 Native422 mode. 1'b0: Disable 1'b1: Enable

DSC_4K_PPS92_95
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SLOAL Second line offset adjust lower bits.
7:0	RW	0x00	SLOAH Second line offset adjust higher bits.

DSC_4K_VERSION
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x10000110	VERSION DSC version.

DSC_4K_CFG_REG0
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x1	PPSREG 0x1 (PPS_REG): PPS Registers Interface is present
29:27	RO	0x1	MNSLC 0x1 (NSLC2): 2 slice per line
26	RO	0x0	reserved
25:24	RO	0x0	FYYP 0x0 (ENCODER): Encoder Function when Encoder feature is selected. Otherwise, Reserved.
23:20	RO	0x1	MJV_ABL This field indicates the number of bits of precision within the line buffer. This field contains the line buffer bit depth used to generate the bit-stream. If a component's bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits. 0xb (LBD11): Line buffer bit depth is 11

Bit	Attr	Reset Value	Description
19:16	RO	0x2	MNV_ABL DSC Minor Version Support This field indicates the Minor version supported in the configuration. Values: 0x1 (DSC_v11): Supports VESA DSC v1.1 0x2 (DSC_v12): Supports both VESA DSC 1.2a and DSC1.1
15:14	RO	0x0	reserved
13	RO	0x0	N422_ABL 0x0 (NOT_SUPPORTED): Native 422 mode is not supported.
12	RO	0x0	N420_ABL 0x0 (NOT_SUPPORTED): Native 420 mode is not supported.
11:8	RO	0xb	LBFD This field indicates the number of bits of precision within the line buffer. This field contains the line buffer bit depth used to generate the bit-stream. If a component's bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits. 0xb (LBD11): Line buffer bit depth is 11
7:4	RO	0xa	NBPC This field indicates the Native Bits per Component of the Display (Maximum Bits per Component set during configuration of DSC encoder) 0xa (BPC10): Bits per component is 10
3:2	RO	0x0	reserved
1	RO	0x0	VBA This field indicates the availability of Variable Bit Rate (VBR) in the configuration. 0x0 (NOT_SUPPORTED): Variable Bit Rate is not supported
0	RO	0x1	BPA This field indicates the availability of Block Prediction (BP) feature in the configuration. 0x1 (SUPPORTED): Block Prediction is supported

DSC_4K_CFG_REG1

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x1000	MPCW Maximum Picture Width This field represents the maximum picture width (maximum number of pixels per raster/line) supported by the configuration.
15:0	RO	0x0870	MPCH Maximum Picture Height This field represents the maximum picture height (Maximum number of pixel rows within the raster) supported by the configuration.

DSC_4K_CFG_REG2

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x2400	RES Rate Buffer Size (in bytes)

DSC_4K_CFG_REG3

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RO	0x1000	MSLW Maximum Slice Width
15:0	RO	0x0870	MSLH Maximum Slice Height

DSC_4K_CTRL0

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31	RW	0x0	PPS_UPD This field provides a control to indicate to DSC encoder that a PPS update has been done. The host can intimate PPS update by setting this bit. DSC encoder clears this bit after the PPS update is accepted. Note: This bit must be written only after all the necessary PPS registers are programmed with desired values. Otherwise, behavior of DSC encoder is undefined.
30	RO	0x0	reserved
29	RW	0x1	IFEP ICH full error precision. Note: The IFEP bit is available only in VESA DSC 1.2a Encoder configuration. Its programmed value is considered when operating in VESA DSC ENC v1.2a mode only. 1'b0: ICH error is truncated in accordance with the bits per component programmed in the PPS. 1'b1: Full precision of ICH error is retained.
28	RW	0x0	SBO Single burst output. 1'b0: DSC output data can be discontinuous for a data line. 1'b1: DSC outputs data in a single burst for a data line.
27:19	RO	0x000	reserved
18:16	RW	0x0	NSLC Number of slices per line. This field provides control to enable required number of data path units (equivalently number of slices per line) in a configuration. 3'b000: 1 slice per line 3'b001: 2 slice per line
15:9	RO	0x00	reserved
8	RW	0x0	INIT Datapath initialization control. 1'b0: Init control is not asserted 1'b1: Init control is asserted
7	RW	0x0	EPL Enable partial bytes at every line end on CDS interface. 1'b0: Disable 1'b1: Enable
6	RW	0x0	EPB Enable partial bytes at chunk ends on CDS interface. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	MER This field provides a way to mask the error reporting through the dsc_err_o port.An error detected in DSC encoder results in assertion of dsc_err_o port and the corresponding Error Status is captured in the Error Status Register. 0x0: Error reporting on dsc_err_o is not masked. So, when an error is detected, dsc_err_o is asserted and the corresponding error code word is captured in the Error Status Register. 0x1: Error reporting on dsc_err_o is masked and only the Error status is captured in the Error Status register.
4	RW	0x1	FLAL This field provides a way to specify the active level of the flush control input, dsc_flush_i. By default, dsc_flush_i is considered as active high signal. 0x0: Dsc_flush_i is treated as active low signal and a falling edge of dsc_flush_i triggers an initialization cycle in DSC encoder. 0x1: Dsc_flush_i is treated as active high signal and a rising edge of dsc_flush_i triggers an initialization cycle in DSC encoder.
3	RW	0x0	RBYT Reverse data bytes. This field controls the order of packing of data bytes on the compressed data interface. This field provides a control to reverse byte positions of data bytes on CDS interface. 1'b0: Disable 1'b1: Enable
2	RW	0x0	RBIT This field controls the order of packing of data bits on the compressed data interface. This field provides a control to reverse bits' organization in each byte of the data bytes on Compressed Data Interface. 1'b0: Disable 1'b1: Enable
1	RO	0x0	FSEL 1'b0: Encoder function
0	RW	0x0	EN This field is used to control the operation of DSC encoder. Host has to write to this bit to enable the operation of DSC encoder. Failing to follow the recommended initialization sequence might lead to undefined behavior.

DSC_4K_CTRL1

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:8	RW	0x1000	RBFTH Rate buffer threshold for overflow(bits). Rate buffer threshold value to trigger buffer fullness. A non-zero initial_xmit_delay allows a final maximum buffer fullness of up to initial_xmit_delay* bits_per_pixel. initial_xmit_delay * bits_per_pixel ~= rc_model_size * 0.5.
7:0	RW	0x00	PPS_SEL PPS table select. If only one PPS table is supported, the value must be 0.

DSC_4K_STS0

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RBOF Rate buffer overflow status. RBUF[i] = 0: No overflow detected in rate buffer of slice-i. RBUF[i] = 1: Overflow detected in rate buffer of slice-i.
15:0	RC	0x0003	RBUF Rate buffer underflow status. RBUF[i] = 0: No underflow detected in rate buffer of slice-i. RBUF[i] = 1: Underflow detected in rate buffer of slice-i.

DSC_4K_STS1

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LBOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in line buffer of slice-i. LBUF[i] = 1: Overflow detected in line buffer of slice-i.
15:0	RW	0x0003	LBUF Line buffer underflow status. LBUF[i] = 0: No underflow detected in line buffer of slice-i. LBUF[i] = 1: Underflow detected in line buffer of slice-i.

DSC_4K_STS2

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	FSOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in line buffer of slice-i. LBUF[i] = 1: Overflow detected in line buffer of slice-i.
15:0	RW	0x0003	FSUF Funnel shift underflow status. FBUF[i] = 0: No underflow detected in funnel shifts of slice-i. FBUF[i] = 1: Underflow detected in funnel shifts of slice-i.

DSC_4K_STS3

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	SEOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in line buffer of slice-i. LBUF[i] = 1: Overflow detected in line buffer of slice-i.
15:0	RW	0x0003	SEUF Syntax element size FIFO underflow status. SEUF[i] = 0: No underflow detected in syntax element size FIFOs of slice-i. SEUF[i] = 1: Underflow detected in syntax element size FIFOs of slice-i.

DSC_4K_STS4

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	BLOF Line buffer overflow status. LBUF[i] = 0: No overflow detected in balance FIFOs of slice-i. LBUF[i] = 1: Overflow detected in balance FIFOs of slice-i.

Bit	Attr	Reset Value	Description
15:0	RW	0x0003	BLUF Balance FIFO underflow status. BLUF[i] = 0: No underflow detected in balance FIFOs of slice-i. BLUF[i] = 1: Underflow detected in balance FIFOs of slice-i.

DSC_4K_STS5
Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PBOF Pixel buffer overflow status. PBUF[i] = 0: No overflow detected in pixel buffer of slice-i. PBUF[i] = 1: Overflow detected in pixel buffer of slice-i.
15:0	RW	0x0003	PBUF Pixel buffer underflow status. PBUF[i] = 0: No underflow detected in pixel buffer of slice-i. PBUF[i] = 1: Underflow detected in pixel buffer of slice-i.

DSC_4K_ERS
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RC	0xffffffff	ECW This field reports any error detected in either in PPS, frame processing or in reset sequence. Any error reported through the ECW register needs re-initialization of DSC encoder by asserting INIT through CTRL0 register. Without the re-initialization, the behavior of encoder is undefined.

7.5.3.10 MMU0/1

VOP2_MMU0_DTE_ADDR
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dte_addr Current page table address.

VOP2_MMU0_STATUS
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	page_fault_bus_id Index of master responsible for last page fault.
5	RW	0x0	page_fault_is_write The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RW	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	stall_active MMU stall mode currently enabled. The mode is enabled by command.

Bit	Attr	Reset Value	Description
1	RW	0x0	page_fault_active MMU page fault mode currently enabled. The mode is enabled by command.
0	RW	0x0	paging_en Paging is enabled. 1'b0: disable 1'b1: enable

VOP2_MMU0_COMMAND
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd This can be: 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET Others: reserved

VOP2_MMU0_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

VOP2_MMU0_ZAP_ONE_LINE
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

VOP2_MMU0_INT_RAWSTAT
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rawst_bus_error Raw interrupt status of read bus error.
0	RW	0x0	rawst_page_fault Raw interrupt status of page fault.

VOP2_MMU0_INT_CLEAR
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	clr_bus_error Clear interrupt of bus error.
0	RW	0x0	clr_page_fault Clear interrupt of page fault.

VOP2_MMU0_INT_MASK
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mask_bus_error Mask interrupt of bus error.
0	RW	0x0	mask_page_fault Mask interrupt of page fault.

VOP2_MMU0_INT_STATUS
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	st_bus_error Interrupt status of bus error.
0	RW	0x0	st_page_fault Interrupt status of page fault.

VOP2_MMU0_AUTO_GATING
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mmu_cfg_mode 1'b0: regdone when frame start 1'b1: regdone immediately
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating itself.

7.6 Application Notes

7.6.1 VOP Pixel Clock Configuration

- **dclk**: The clock source of the post-processing module and interface pixel clock, provided by the CRU module in the pd_VOP subsystem.
- **dclk_core**: The operating clock of the scanning timing of the post-processing module.
- **dclk_out**: Output interface operating clock, used by DP and MIPI interfaces.

7.6.1.1 dclk Frequency Requirements

Because it is necessary to provide clock sources for post-processing modules (dclk_core, dclk_out) and various output display interfaces (mipi_pixel_clock, eDP_pixel_clock, etc.), it is necessary to ensure that dclk is the highest frequency to meet various interface format rate conversion and frequency division requirements.

7.6.1.2 dclk_core Frequency Requirements

Matching with the pixel rate of the post-processing module, the post-processing pixel operating rate of VOP is 4pixel/cycle:

dclk_core = (Video Timing Pixel Rate) / 4

For example, the expected video timing is 4K@60hz format, where pixel rate equals 594Mhz, so the dclk_core frequency shall be configured as 148.5M.

7.6.1.3 dclk_out Frequency Requirements

Match the pixel rate of the output interface, for example, the pixel clock of the DP interface comes from the corresponding dclk_out.

7.6.1.4 RGB Interface Clock Frequency Requirements

The processing rate of the RGB interface is 1pixel/cycle, and the scan timing of the VOP post-processing is 4pixel/cycle, that is, the dclk frequency provided by the SoC to the VOP is required to be equal to the Pixel Rate. For example, the current video timing is 1080p@60hz format, and dclk is 148.5M and dclk_core is 37.125M.

RGB Interface Pixel Rate =dclk = dclk_core × 4

7.6.1.5 DP Interface Clock Frequency Requirements

The pixel clock of the DP interface is derived from the dclk_out clock of the corresponding port.

When transmitting RGB format, the DP interface rate is 4 pixels/cycle:

Video Timing Pixel Rate = 4×dclk_out =4×dclk_core

When transmitting the YUV420 format, the DP interface rate is 8 pixels/cycle:

Video Timing Pixel Rate = 8×dclk_out =4×dclk_core

7.6.1.6 HDMI/eDP Combo Interface Clock Frequency Requirements

The frequency division selection of hdmieDP*_dclk_sel controls the processing clock hdmieDP_dclk of the VOP HDMI/eDP combo interface.

The hdmieDP*_pixclk_sel frequency division selection controls the transmission clock hdmieDP_pixel_clk sent by the HDMI/eDP Combo to the HDMI TX controller or eDP controller.

When configured in eDP interface mode, the processing rate of the eDP interface is 1pixel/cycle, and the scan timing of the VOP post-processing is 4pixel/cycle, so the dclk frequency provided by the SoC to the VOP is required to be equal to the eDP Interface Pixel Rate. For example, the current video timing is 4K@60hz format, and dclk shall be set to 600M and dclk_core to 148.5M.

Video Timing Pixel Rate = (hdmieDP_pixel_clk × K)
= (hdmieDP_dclk × K)
= (dclk_core × 4)

When eDP is configured in SPLIT display mode, K is equal to 2, and in other cases, K is equal to 1.

When configured in HDMI interface mode and operating in uncompressed mode, the processing rate of the HDMI interface is 4pixel/cycle, which is consistent with the VOP post-processing rate. The special treatment is that because there is a rate conversion circuit that reduces the bit width of the data bus by half between the VOP and the HDMI TX controller, the channel transmission clock hdmieDP_pixel_clk needs to be twice the hdmieDP_dclk.

(Video Timing Pixel Rate)/ (4) = ((hdmieDP_pixel_clk)/2×K) = (hdmieDP_dclk×K) = dclk_core

When HDMI transmits YUV420 format or is configured as SPLIT display mode, K is equal to 2, and in other cases, K is equal to 1.

When operating in compressed mode:

((hdmieDP_pixel_clk) / 2) = hdmieDP_dclk = cds_clk

cds_clk: DSC encoder Compressed Data Stream output interface drive clock

7.6.1.7 MIPI Interface Clock Frequency Requirements

When MIPI works in uncompressed mode, the MIPI interface rate is 4Pixel/cycle.

(Video Timing Pixel Rate)/(4) = (MIPI Pixel Clock×K)=(dclk_out×K)=dclk_core

When MIPI works in compressed mode:

MIPI Pixel Clock = cds_clk / 2

Since the MIPI DSI controller's pixel interface is 192bit data width and DSC encoder CDS interface is 96bit data width.

Note that when MIPI is configured as double channel display mode, K=2, otherwise K=1.

7.6.1.8 Example of Typical Video Timing Configuration

Table 7-9 Frequency and select configuration table in typical mode

Video Timing	Pixel Format	dclk Freq	dclk_core (dclk_core_sel)	dclk_out (dclk_out_sel)	DP Pixel Clock
8K@24Hz (VIC 194)	RGB	297	297 (0)	297 (0)	297
4K@60Hz (VIC 97)	RGB	148.5	148.5 (0)	148.5 (0)	148.5
4K@60Hz - Split	RGB	148.5	148.5 (0)	74.25 (1)	74.25
1080p@60Hz (VIC 16)	RGB	37.125	37.125 (0)	37.125 (0)	37.125
720x480i@60Hz(VIC 6)	RGB	27	13.5 (1)	27 (0)	27

The cru picture inside the VOP is shown below, refer to VOP2_cru.pdf for details.

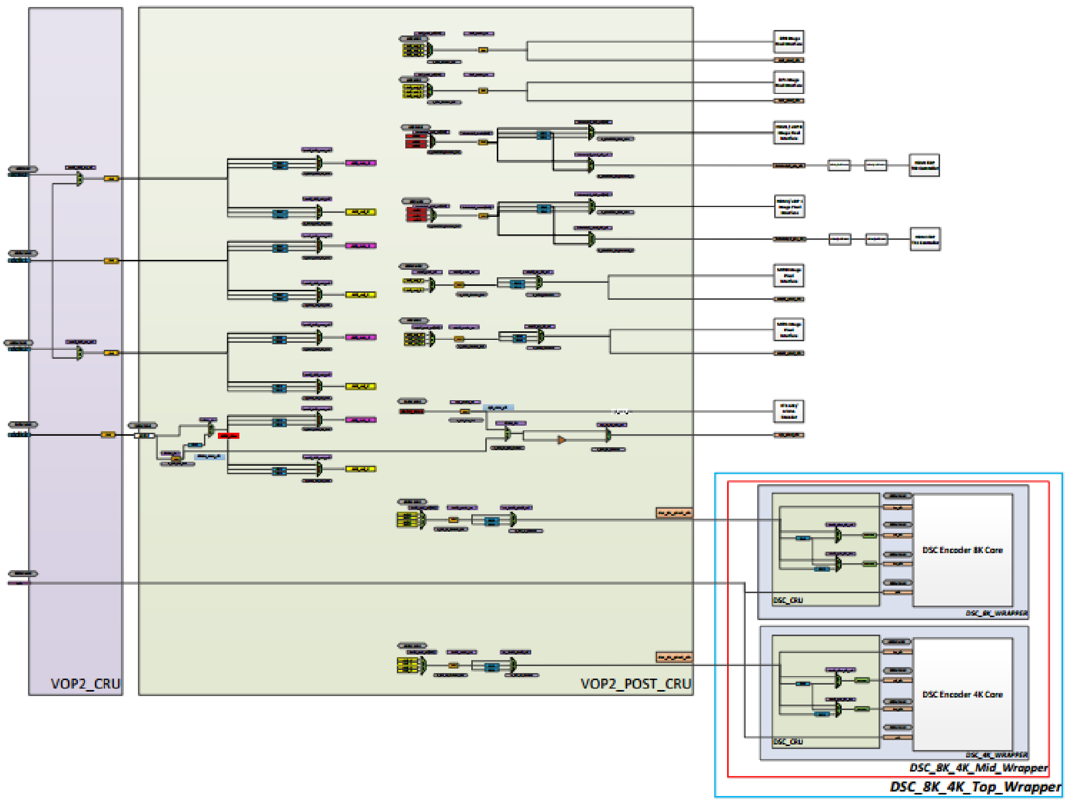

Fig. 7-54 VOP2 internal cru block diagram

The post operating clock mux inside each PORT is shown in the figure below:

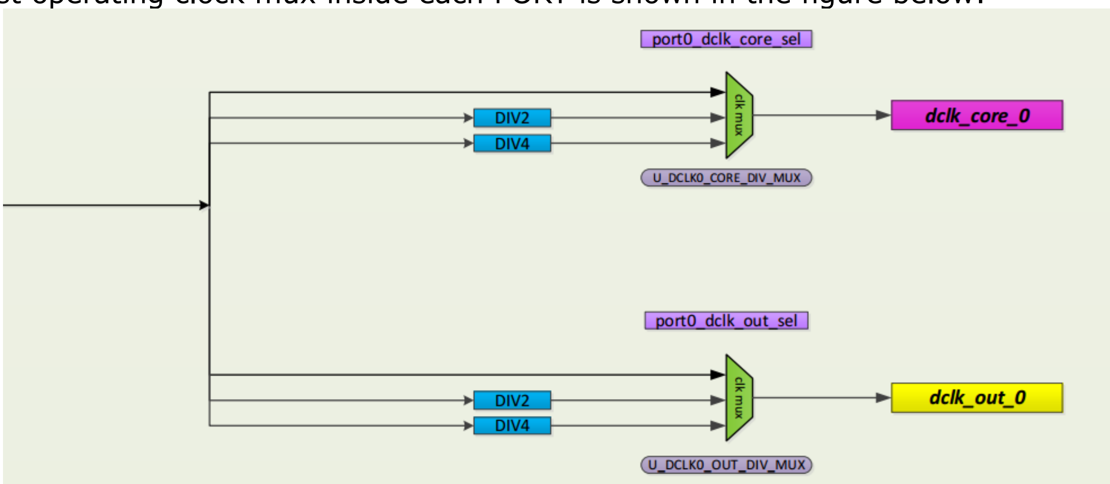

Fig. 7-55 PORT operating clock mux

The clock mux diagram of each high-speed interface is as follows:

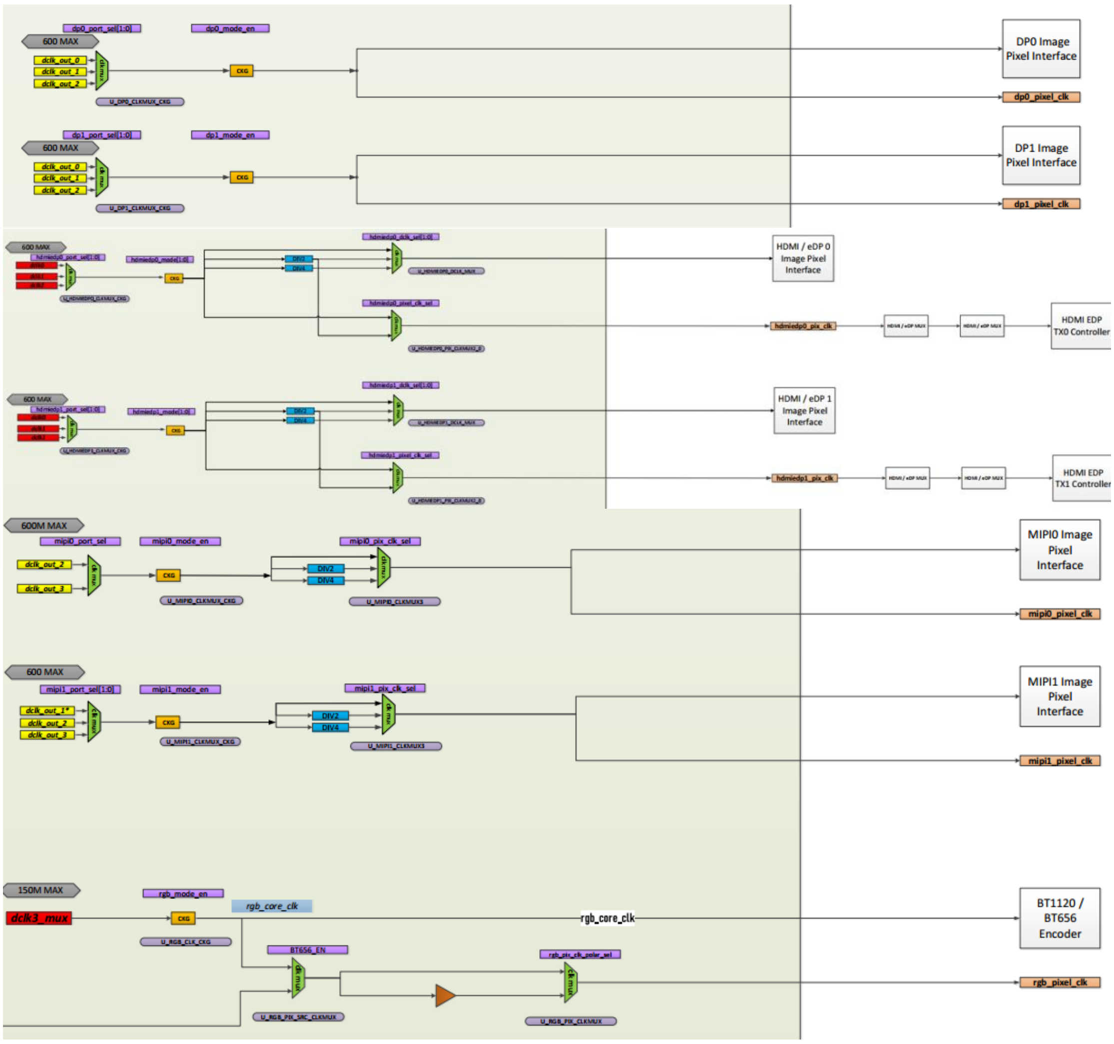

Fig. 7-56 Clock mux of each output interface

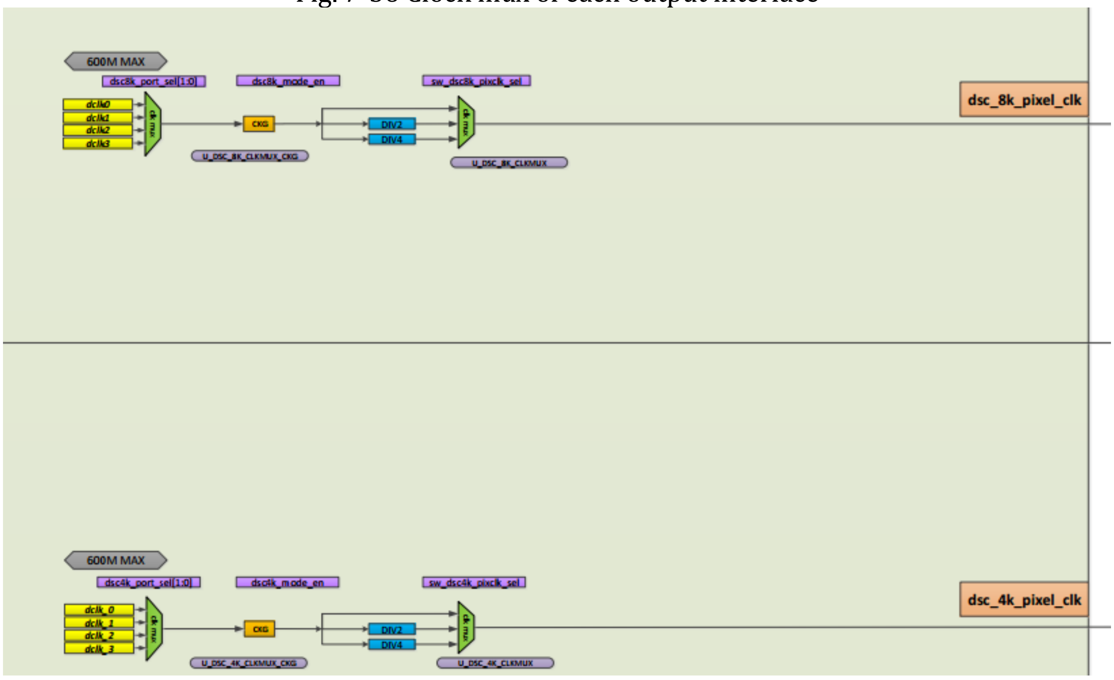

Fig. 7-57 Clock mux structure output to DSC

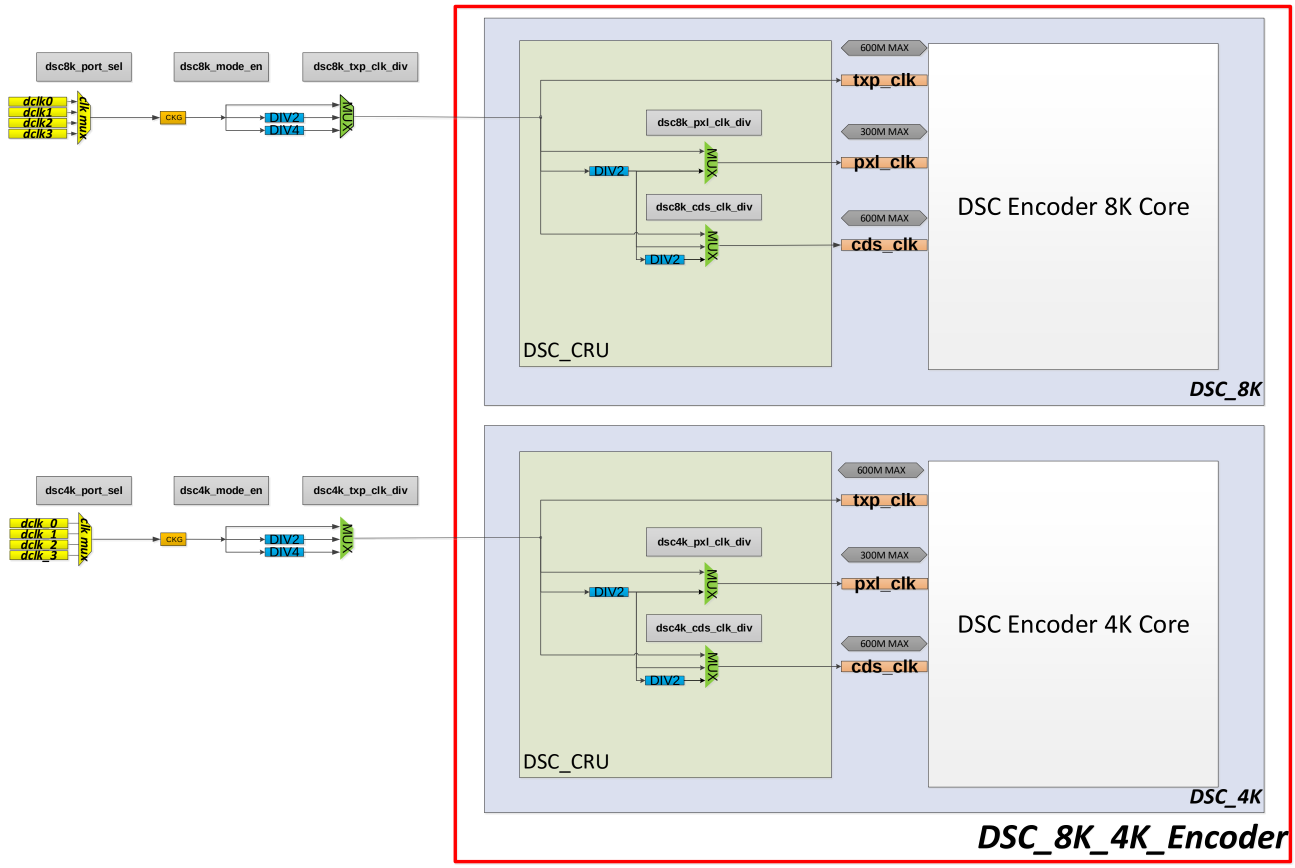

Fig. 7-58 Clock structure inside DSC

7.6.2 DSC Encoder Configuration

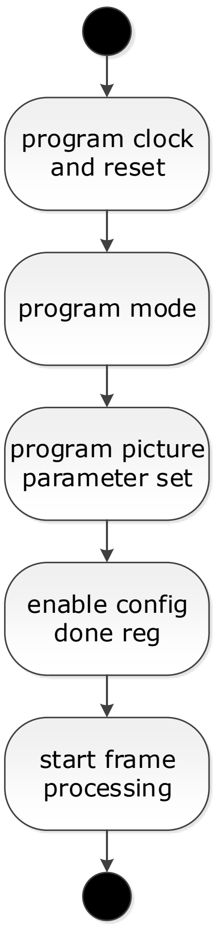

Fig. 7-59 Configuration Sequence of DSC Encoder

7.6.2.1 Clock and Reset

The process path of DSC encoder pixel clock includes, 4 to 1 clock mux, clock gating, clock divider. DSC encoder clock are configurable to select the source from dclk0/dclk1/dclk2/dclk3, which should be matched the video source. for example, if use DSC 8K encoder process MIPI0 video data which comes from the port2 data path, the DSC_8K_SYS_CTRL.dsc_port_sel register field should be set to 0x2 to select dclk2.

- **txp_clk:** the clock feed input pixels to DSC encoder, max frequency 600MHz, divided from dclk programmed by register VOP.DSC_SYS_CTRL.dsc_txp_clk_div. Frequency of txp_clk clock must be more than or equal that of pxl_clk.

$$\text{Frequence of txp\_clk} = \frac{(\text{Vtotal} \times \text{Htotal} \times \text{RefreshRate})}{(\text{Number of pixel feed into DSC encoder per clock} \times \text{K})}$$

- **pxl_clk:** used for slice's data path operations, max frequency 300MHz, divided from txp_clk programmed by register VOP.DSC_SYS_CTRL.dsc_pxl_clk_div.

$$\text{Frequence of pxl\_clk} >= \frac{(\text{Vtotal} \times \text{Htotal} \times \text{RefreshRate})}{(\text{Number of active slices} \times \text{K})}$$

- **cds_clk:** used to drive the output CDS (Compressed Data Stream) interface, max frequency 600MHz, divided from txp_clk programmed by register VOP.DSC_SYS_CTRL.dsc_cds_clk_div.

$$\text{Frequence of cds\_clk} >= \frac{(\text{Vtotal} \times \text{Htotal} \times \text{RefreshRate})}{\left(\left(\text{CDS\_Data\_Width}/\text{Bits per pixel}\right) \times \text{K}\right)}$$

where CDS_Data_Width is DSC encoder output data width which is fixed 96bit.

Note that the number of active slices per lines must be more than or equal to the number of pixels per clock fed at the DSC encoder pixel input interface.
Note that when MIPI is configured as double channel display mode K = 2, otherwise K = 1.

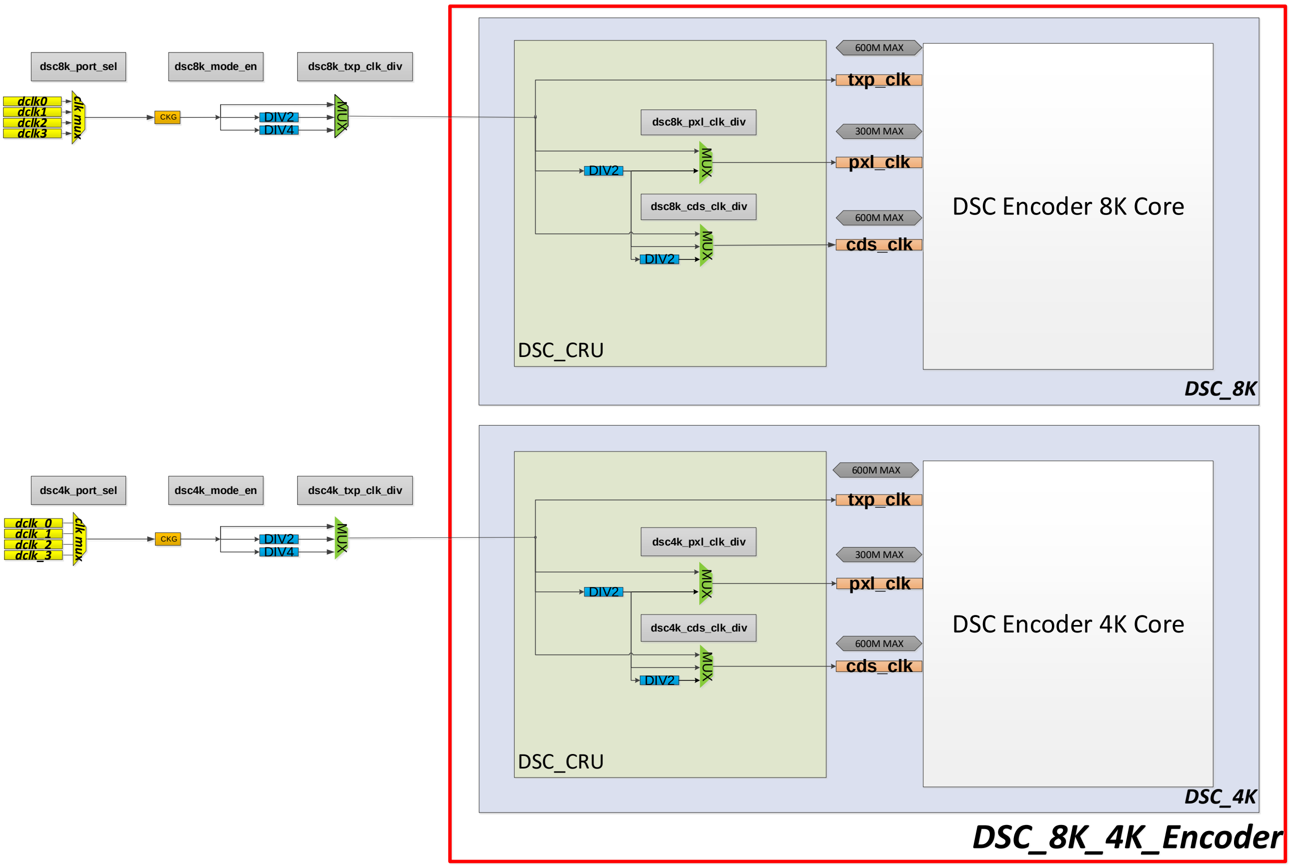

Fig. 7-60 Clock Structure of DSC Encoder

DSC encoder power_on_resetn signal is controlled in register field DSC_SYS_CTRL.DSC_8K_RST.dsc_soft_rst.

7.6.2.2 Programming encoder

7.6.2.2.1 program mode

Based on the configuration settings, use the DSC encoder CTRL0 and DSC encoder CTRL1 control registers to enable or disable the available features.

The SBO field of DSC encoder CTRL0[28] should be set to 1'b1 for output data in a single burst for a data line.

7.6.2.2.2 Program Picture Parameter Set

1. To enable the DSC encoder operation, set the EN field to 1, in the DSC encoder CTRL0 register by writing 1'b1 to bit [0] of DSC encoder CTRL0.
2. Program the PPS register fields.
3. For the new PPS values to take effect, set the PPS_UPD field in the DSC encoder CTRL0 register to 1 by writing 1'b1 to bit [31] of DSC encoder CTRL0 register.
4. Wait for the PPS to be updated
   - PPS_UPD field is cleared by DSC encoder after the PPS update is complete. This marks the completion of PPS update procedure.
   - Read/Poll bit [31] of DSC encoder CTRL0 register

The field definitions of PPS56_59 and registers from PPS60_63 to PPS84_87 needs special attention, as there is a subtle difference between the mapping of fields in DSC encoder and in VESA PPS, as shown in the below figure.

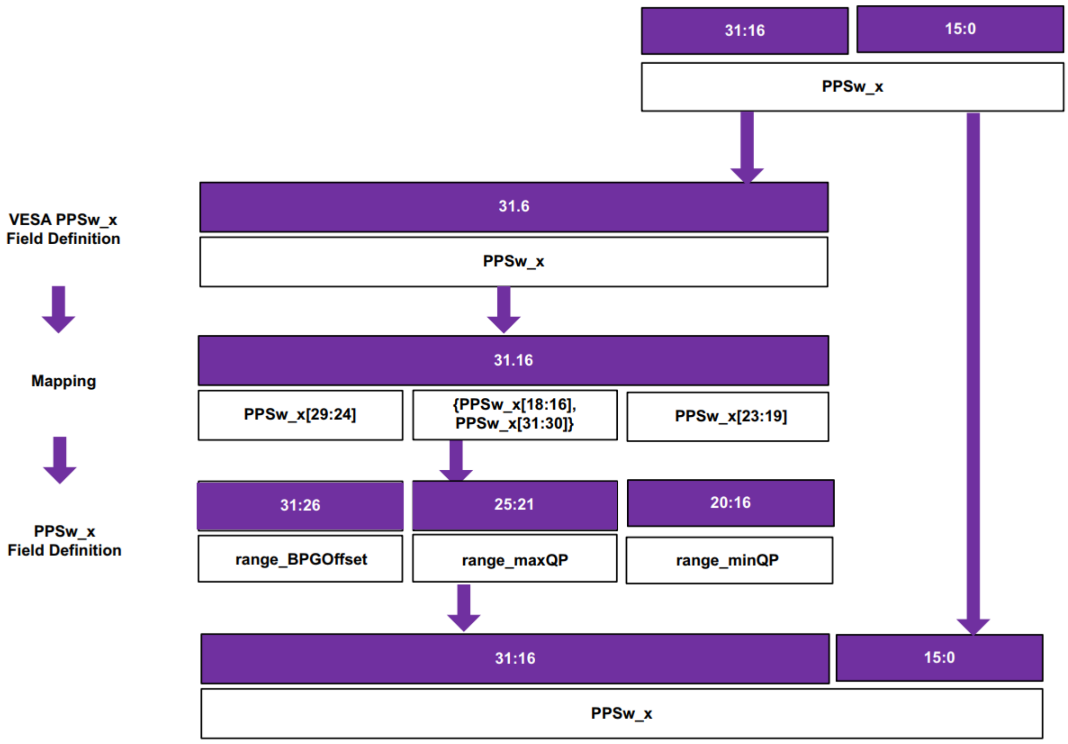

Fig. 7-61 Mapping of DSC encoder Register field to PPS56_59

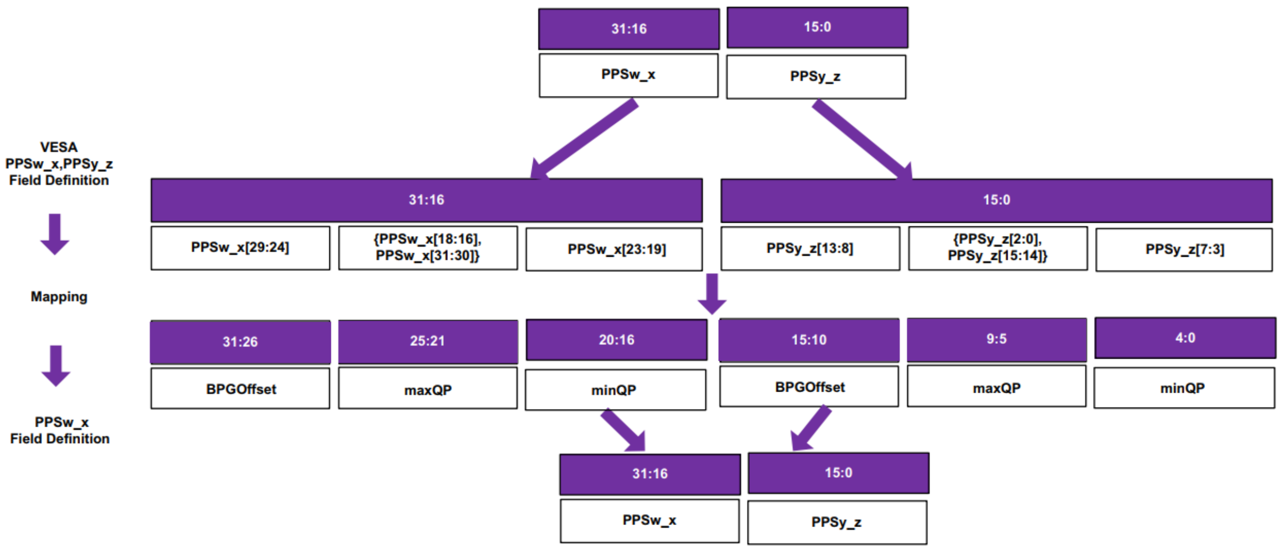

Fig. 7-62 Mapping of DSC encoder Register field PPS60_63 to PPS84_87

7.6.2.3 Set Configuration done signal

When the above register of DSC encoder has been configured, set DSC_8K_CFG_DONE = 1 (DSC_SYS_CTRL.DSC_8K_CFG_DONE) to unmask video data input to encoder which will be valid at the next frame start pulse. When encoder received the valid frame start, the hardware will clear this bit.

7.6.2.4 Error Monitoring

DSC encoder can detect and report error under the following conditions:

1. An inappropriate value programmed for a Picture Parameter Set (PPS) field
   DSC encoder validates programmed PPS fields value against target configuration and reports error if PPS value programmed does not correspond to or is not supported by the target configuration.

2. An overflow condition detected in any of the buffer stages is reported as an error. The buffer overflow error can be due to either rate mismatch or insufficient rate buffer size.
   DSC encoder reports error by asserting dsc_err_o port. The below figure shows how to monitor the reported error through the dsc_err_o signal.

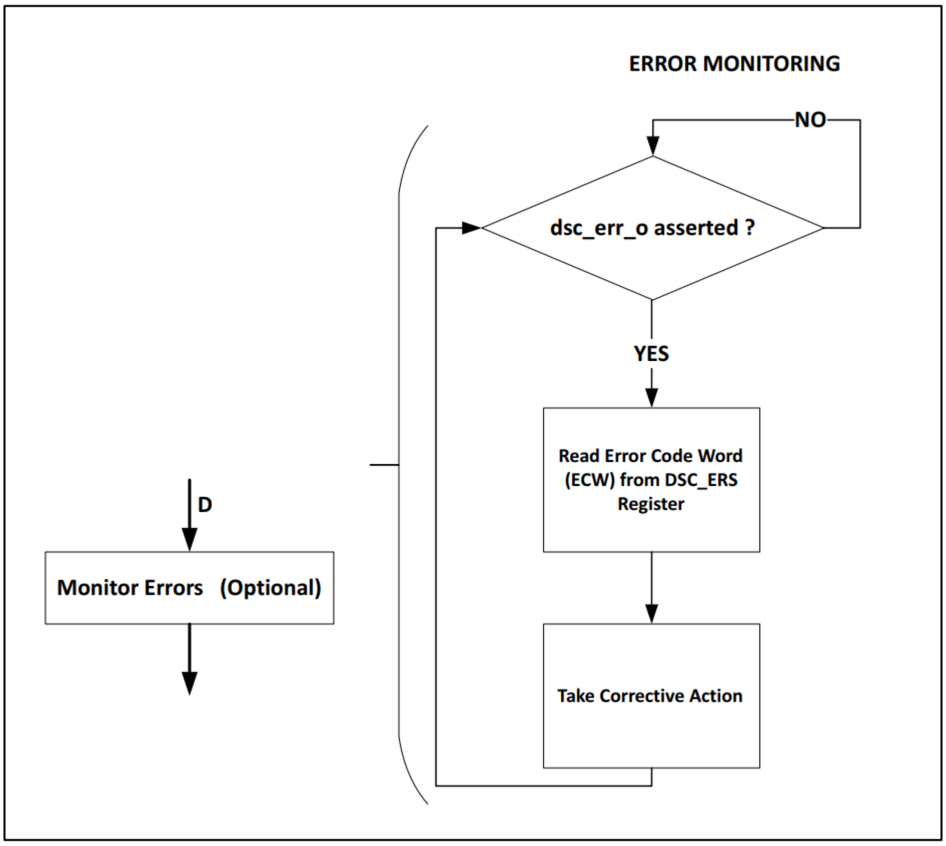

Fig. 7-63 Error Monitoring of DSC Encoder

Following steps are involved in Error Monitoring:
1. Continuously monitor dsc_err_o (through register or interrupt). If DSC encoder encounters an error, dsc_err_o is asserted.
2. Read ECW in DSC_ERS register to determine the source of error, on detecting dsc_err_o assertion.
3. Take corrective action to fix the error.
The dsc_err_o signal is connected to DSC_SYS_CTRL register “dsc_error_status” and VOP interrupt pin which connected to the GIC.

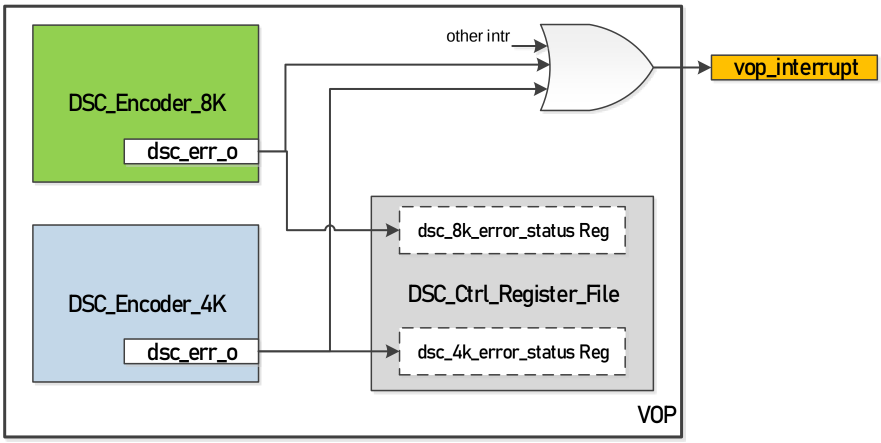

Fig. 7-64 Error Report Structure of DSC Encoder

7.6.2.4.1 Error Conditions and Error Codes

The below table lists the various error conditions and error codes:

Table 7-10 DSC Encoder Error Codes

Error Condition and Description	Error Code Word
No error detected by DSC encoder	0x0

Error Condition and Description	Error Code Word
Bits per component error when the programmed bits per component value is invalid. Also, BPC error is reported if the programmed BPC value is more than the maximum BPC value supported in the configuration.	0x0030ffff
Multiple mode error is reported when more than one mode is enabled in the PPS. for example if the PPS programmed has both Native 420 mode and Native 422 mode enabled, multi-mode error is reported.	0x0040ffff
Line buffer depth Error is reported when the value of Line-buffer Depth field in the PPS is more than the maximum Line-buffer depth (DWCDSC_LBf_DPTH) specified in the configuration	0x0050ffff
Minor version error is reported if the programmed value of Minor version is not supported in the configuration. for example, in a DSC 1.2a configuration, both DSC 1.1 mode and DSC1.2a modes are supported. Accordingly, the minor version field is to be set to either 1 or 2. If the minor version field is set to any other value, minor version Error is reported.	0x0060ffff
Picture height error is reported when the programmed picture height in the PPS is beyond the limits of the picture height supported in the configuration. Minimum and maximum value of picture height are 4 and DWCDSC_MAX_LNS respectively.	0x0070ffff
Picture width error is reported if the programmed picture width is beyond the valid range of picture width supported in the configuration.	0x0080ffff
Number of slices error is reported when the programmed number of slices per line is more than the number of slices per line specified in the configuration.	0x0090ffff
Slice height Error is reported when the programmed slice height is invalid.	0x00c0ffff
Slice width error is reported when the programmed slice width is invalid.	0x00d0ffff
Second Line BPG Offset Error is reported when a non-zero value is programmed for Second Line BPG offset field in modes other than Native 420.	0x00e0ffff
Non Second Line BPG Offset Error is reported when a non- zero value is programmed for Non Second Line BPG offset field in modes other than Native 420 mode.	0x00f0ffff
PPS ID Error, if the programmed PPS ID exceeds the Number of PPS IDs supported in the configuration. for single PPS ID support, a non-zero value of PPS ID results in error.	0x0100ffff
Bits per Pixel (BPP) Error is reported when the programmed Bits per Pixel value is beyond the valid range.	0x0110ffff
Buffer flow error detected in one of the buffers. To determine the buffer that has an overflow, read the overflow status flags from the registers. ● Rate buffer ● Line buffer ● Decoder model ● Pixel buffer	0x0120ffff

Error Condition and Description	Error Code Word
● Balance FIFO buffer ● Syntax Element FIFO buffer	
RC Buffer model overflow Error detected in slice 0	0x01510001
RC Buffer model overflow Error detected in slice 1	0x01510002
RC Buffer model overflow Error detected in slice 2	0x01510004
RC Buffer model overflow Error detected in slice 3	0x01510008
RC Buffer model overflow Error detected in slice 4	0x01510010
RC Buffer model overflow Error detected in slice 5	0x01510020
RC Buffer model overflow Error detected in slice 6	0x01510040
RC Buffer model overflow Error detected in slice 7	0x01510080
RC Buffer underflow condition detected in slice0	0x01610001
RC Buffer underflow condition detected in slice1	0x01610002
RC Buffer underflow condition detected in slice2	0x01610004
RC Buffer underflow condition detected in slice3	0x01610008
RC Buffer underflow condition detected in slice4	0x01610010
RC Buffer underflow condition detected in slice5	0x01610020
RC Buffer underflow condition detected in slice6	0x01610040
RC Buffer underflow condition detected in slice7	0x01610080
Unsuccessful RESET Cycle Status.	0xffffffff
ICH full Error Precision Settings Error This error is reported when IFEP (ICH full Error Precision) field of DSC_CRTL0 register is set to 1'b1 in VESA DSC ENC v1.1 mode. Note: The IfEP field of the DSC_CRTL0 register is available only in VESA DSC 1.2a encoder configuration.	0x00a0ffff
Native mode error is reported when either of Native 420 or Native 422 mode is enabled in DSC v1.1 mode.	0x0020ffff

7.6.2.5 Example Programming Sequences

7.6.2.5.1 Case1 (VOP Port2 → DSC 4K → MIPI 1)

- Esmart0, Port2, DSC 4K Encoder, MIPI 1
- 720 width x 1560 height, 2 Slice, RGB888, 8BPP

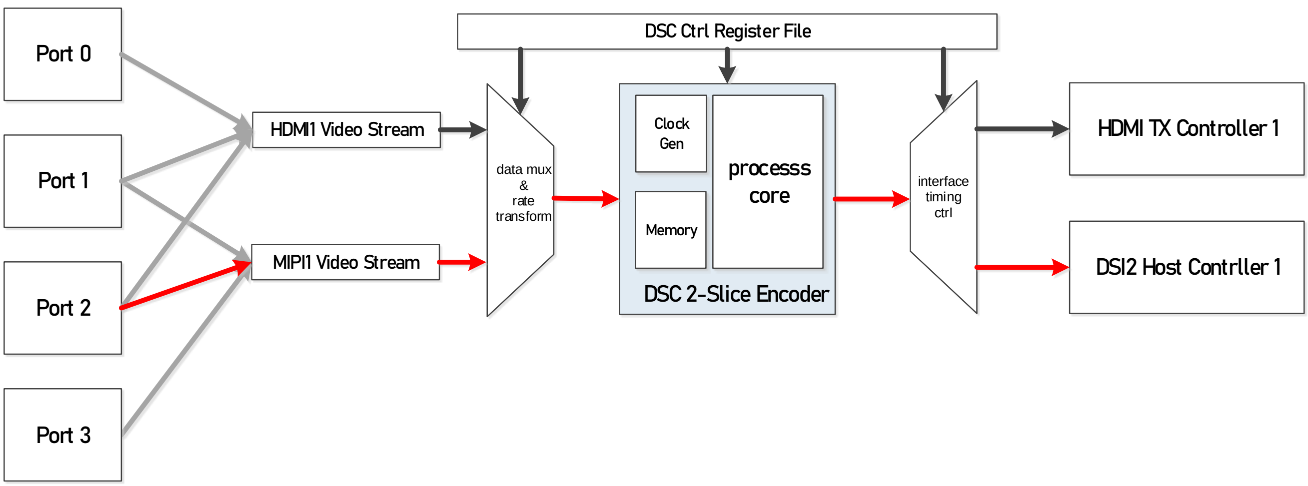

Fig. 7-65 Case1 DSC 4K - MIPI Video Stream

Sequence:

1. Power up DSC_4K encoder through VOP.SYS_CTRL.SYS_POWER_CTRL.dsc_4K_pd_en

2. Wait DSC_4K encoder power up completed by polling dsc4K_power_domain_status = 0
3. Program esmart0, overlay, post process 2.
4. Enable MIPI1 interface in VOP.SYS_CTRL.SYS_DSP_INFACE_EN register mipi1_mode_en bit and select dclk2 in mipi1_port_sel bit.
5. Program VOP.DSC_SYS_CTRL.DSC_4K_SYS_CTRL = 0x00044066 to set DSC operation mode, pixel clock source, data source port.
6. Program VOP.DSC_SYS_CTRL.DSC_4K_RST = 0x1 to release power-up reset of DSC encoder.
7. Program VOP.DSC_4K.CTRL0 = 0x10010095 to specify active slice number, bit order.
8. Program PPS register
   1) PPS0~3 = 0x89000011
   2) PPS4~7 = 0x18068030
   3) PPS8~11 = 0x3400d002
   4) PPS12~15= 0x68016801
   5) PPS16~19= 0xb4010002
   6) PPS20~23= 0x04042000
   7) PPS24~27= 0x0c000500
   8) PPS28~31= 0xef02e201
   9) PPS32~35= 0xf0100018
   10) PPS36~39= 0x00200c03
   11) PPS40~43= 0x330b0b06
   12) PPS44~47= 0x382a1c0e
   13) PPS48~51= 0x69625446
   14) PPS51~55= 0x7b797770
   15) PPS56~59= 0x08807e7d
   16) PPS60~63= 0x00a10080
   17) PPS64~67= 0xf0e3f8c1
   18) PPS68~71= 0xe0e3e8e3
   19) PPS72~75= 0xe123e103
   20) PPS76~79= 0xd965d943
   21) PPS80~83= 0xd1a5d185
   22) PPS84~87= 0xd1edd1a7
9. Program DSC_4K CTRL0 = 0x90010095 to enable PPS update.
10. Poll for the PPS UPDATE acknowledgment (auto clearing of VOP.DSC_4K.CTRL0.PPS_UPD field) by DSC encoder.
11. Power up MIPI Combo PHY and DSI2 Host Controller.
12. Program VOP.DSC_SYS_CTRL.DSC_4K_CFG_DONE.cfg_done = 1
13. Program VOP.SYS_CTRL.SYS_REG_CFG_DONE to start frame processing.

7.6.2.5.2 Case2 (VOP Port0 → DSC 8K → HDMI 0)

- Cluster 0/1, Port0, DSC 8K Encoder, HDMI TX0
- picture size = 7680x4320
- bits_per_component = 0xa (10bit)
- bits_per_pixel = 0xa0 (10.0 bpp)
- slice_width = 960
- slice_height = 2160
- RGB format

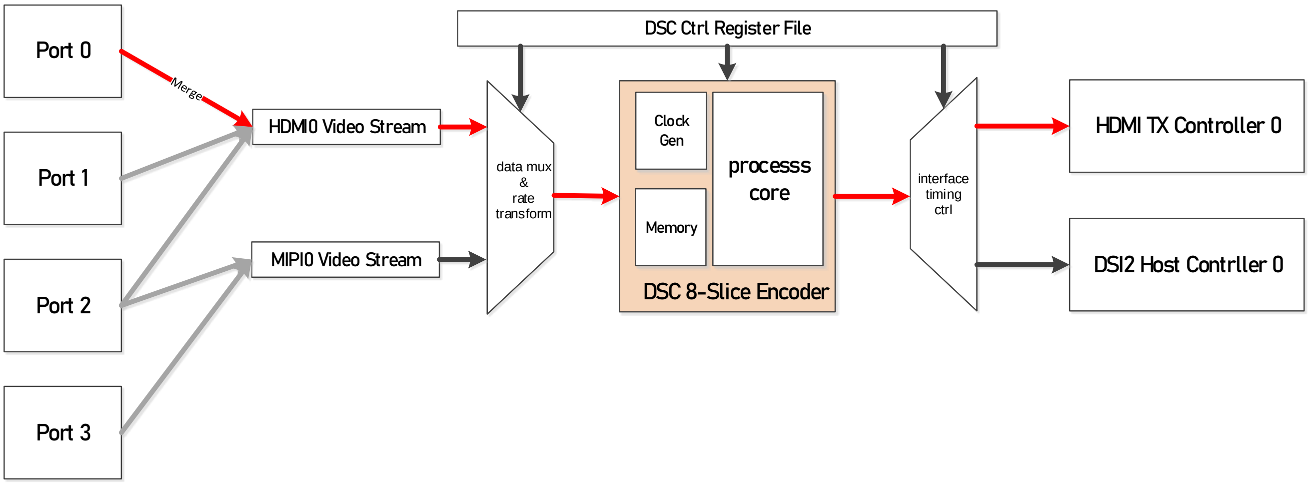

Fig. 7-66 Case2 DSC 8K - HDMI Video Stream

Sequence:

1. Power up cluster 0/1 and DSC_8K encoder through VOP.SYS_CTRL.SYS_POWER_CTRL
2. Wait cluster 0/1 and DSC_8K encoder power up completed by polling cluster 0/1 and DSC_8K power_domain_status = 0
3. Enable HDMI 0 interface in VOP.SYS_CTRL.SYS_DSP_INFACE_EN register hdmieDP0_mode bit and select dclk0 in hdmieDP0_port_sel bit.
4. Enable hdmi0 pixel clock by setting VOP.SYS_CTRL.SYS_AUTO_GATING_CTRL_IMD.hdmieDP0_pixclk_enable = 1
5. Program esmart0/1, overlay, post process 0/1.
6. Program VOP.DSC_SYS_CTRL.DSC_8K_SYS_CTRL = 0x00021190 to set DSC operating as HDMI mode, pixel clock source, data source port.
7. Program VOP.DSC_SYS_CTRL.DSC_8K_RST = 0x1 to release power-up reset of DSC encoder.
8. Program compressed output video timing through DSC_8K_HTOTAL_HS_END / DSC_8K_HACT_ST_END / DSC_8K_VTOTAL_VS_END / DSC_8K_VACT_ST_END
9. Program output timing scan delay number through DSC_8K_INIT_DLY_NUM (2~3 lines delay)
10. Program VOP.DSC_8K.CTRL0 = 0x30030095 to specify active slice number, bit order.
11. Program 128 bytes PPS register
12. Program VOP.DSC_8K.CTRL0 = 0xb0030095 to enable PPS update.
13. Poll for the PPS update acknowledgment (auto clearing of VOP.DSC_8K.CTRL0.PPS_UPD field) by DSC encoder.
14. Program VOP.DSC_SYS_CTRL.DSC_8K_CFG_DONE.CFG_done = 1
15. Power up HDMI TX PHY and HDMI TX Controller.
16. Program VOP.SYS_CTRL.SYS_REG_CFG_DONE to start frame processing.

Chapter 8 Image Enhancement Processor（IEP)

8.1 Overview

The Image Enhancement Processor (IEP) receives data from system main memory and transmits data to system main memory by AXI bus.

The features of IEP are as follows:

- **Image format**
  - Input data: YUV420/YUV422; Semi-planar/planar; UV swap
  - Output data: YUV420/YUV422; Semi-planar; UV swap; Tile mode
  - YUV down sampling conversion from 422 to 420
  - Max resolution for dynamic image up to 1920x1080
- **De-interlace**
  - **I5O2**: Input 5 Fields Output 2 frames mode
  - **I5O1T**: Input 5 Fields Output 1 Top frame mode
  - **I5O1B**: Input 5 Fields Output 1 Bottom frame mode
  - **I2O2**: Input 2 Fields Output 2 frames mode
  - **I1O1T**: Input 1 Field Output 1 Top frame mode
  - **I1O1B**: Input 1 Field Output 1 Bottom frame mode
  - **PULLDOWN_REC**: Pull-down Recovery mode
  - **DETECT_ONLY**: Detect Only mode
  - **MVHIST**: De-interlace MV Histogram
  - **MD**: Motion Detection
  - **ME**: Motion Estimate
  - **MC**: Motion Compensation
  - **EEDI**: Enhanced Edge based Interpolation
  - **OSD DETECT**: On-Screen Display Detection
  - **FF DETECT**: Frame Field Detection
  - **FO DETECT**: Field Order Detection
  - **PD DETECT**: Pull Down Detection
  - **CC**: Combining Check
- **Interface**
  - 32bit AHB bus slave
  - 128bit AXI bus master
  - Combined interrupt output

8.2 Block Diagram

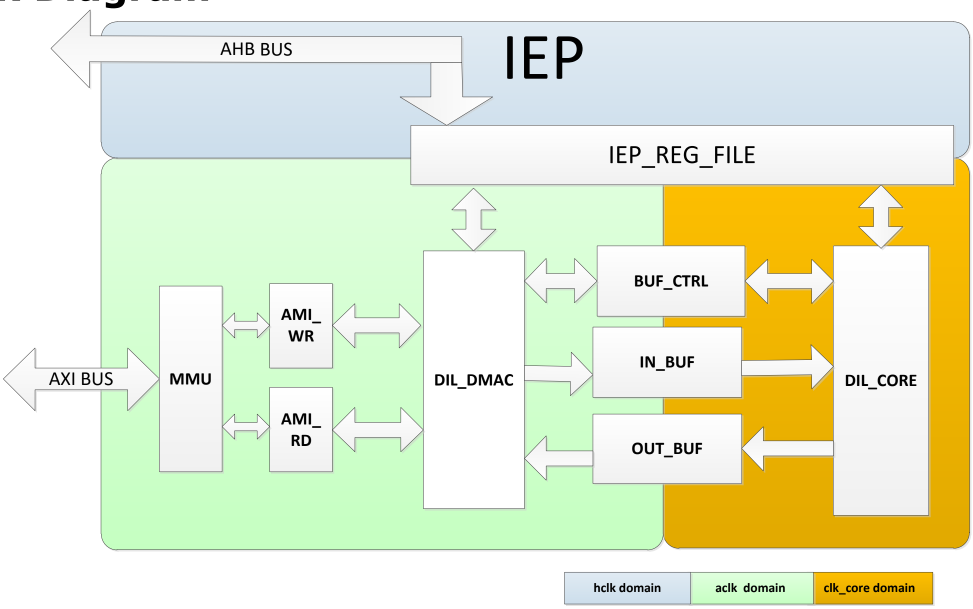

Fig. 8-1 IEP block diagram

The data path in IEP is in the previously diagram. The IEP comprises with:

Deinterlace Core Processing
There are eight de-interlace modes (refer to feature description above) in the DIL_CORE block. Some important functions for deinterlace are in this module such as MD, ME, MC, EEDI.

DMA
DMA block responses for reading interlaced video data from DDR and writing frame data to DDR.

REG FILE
All configurable signals will be configured in this block and send to other function modules for using. Detect data and MVHIST data will be read back to user in this module by AHB bus.

8.3 Function Description

8.3.1 Deinterlace

There are eight deinterlace modes including I5O2, I5O1B, I5O1T, I2O2, I1O1B, I1O1T and detect only mode in the deinterlace block.

I5O2 mode
The I5O2 mode represents for 5 fields of input images and 2 frames of output images. This mode is the most frequently used. The input source images are stored as interlaced mode which means top field and bottom field are stored by the method that one top field line follows one bottom field or conversely. So, current, next and preview input frame address (SRC_ADDR_CURY, SRC_ADDR_NXTY and SRC_ADDR_PREY for Y channel) need to be configured. Top frame and bottom frame address (DST_ADDR_TOPY, DST_ADDR_BOTY for Y channel) need to be configured for output 2 frames.

I5O1B/T mode
The I5O1B and I5O1T mode have the same input images as the I5O2 mode, but only one frame output is generated which means only need configure one output frame address(top frame address for I5O1T mode and bottom frame address for I5O1B mode).

I2O2 mode
The I2O2 mode only need current input source frame, output is the same as I5O2 mode. This mode is the fastest and the most bandwidth saving.

I1O1B/T mode
The I1O1B and I1O1T mode just need read one filed. The output is same as I5O1B and I5O1T mode.

Bypass mode
If bypass mode is selected, there are not any deinterlace operations.

Pulldown Recovery mode
If the pulldown detection block detects the current source is pulldown interlace video. IEP supports pulldown recovery by setting this mode.

Detect Only mode
This mode has no output frames for saving power and bandwidth. All of the detection results will be read back though AHB bus.

8.4 Register Description

8.4.1 Registers Summary

Slave address can be divided into different length for different usage, which is shown as follows.

Name	Offset	Size	Reset Value	Description
IEP2_FRM_START	0x0000	W	0x00000000	Frame start and frame state register
IEP2_IEP_CONFIG0	0x0004	W	0x00000303	IEP configuration register0
IEP2_GATING_CTRL	0x0010	W	0x00000800	IEP auto gating register
IEP2_STATUS	0x0014	W	0x00000000	IEP status
IEP2_INT_EN	0x0020	W	0x00000011	IEP interrupt enable
IEP2_INT_CLR	0x0024	W	0x00000000	IEP interrupt clear
IEP2_INT_STS	0x0028	W	0x00000000	IEP interrupt status
IEP2_INT_RAW_STS	0x002C	W	0x00000000	IEP interrupt raw status
IEP2_VIR_SRC_IMG_WIDTH	0x0030	W	0x00000000	Source image virtual width
IEP2_VIR_DST_IMG_WIDTH	0x0034	W	0x00000000	Destination image virtual width
IEP2_SRC_IMG_SIZE	0x0038	W	0x00000000	Source image size
IEP2_DIL_CONFIG0	0x0040	W	0x00029F01	Deinterlace configuration register0
IEP2_IEP_TIMEOUT_CFG	0x0050	W	0x0065B9AA	Timeout configuration
IEP2_IEP_VERSION_INFO	0x0054	W	0x20000000	IEP version information
IEP2_DBG_FRM_CNT	0x0058	W	0x00000000	Frame counter
IEP2_DBG_TIMEOUT_CNT	0x005C	W	0x00000000	Timeout counter
IEP2_SRC_ADDR_CURY	0x0060	W	0x00000000	Start address of source current image(Y), frame address
IEP2_SRC_ADDR_NXTY	0x0064	W	0x00000000	Start address of source next image(Y), frame address
IEP2_SRC_ADDR_PREY	0x0068	W	0x00000000	Start address of source previous image(Y), frame address
IEP2_SRC_ADDR_CURUV	0x006C	W	0x00000000	Start address of source current image(UV), SP mode UV frame or U P mode frame address
IEP2_SRC_ADDR_CURV	0x0070	W	0x00000000	Start address of source current image(V), P mode V frame address
IEP2_SRC_ADDR_NXTUV	0x0074	W	0x00000000	Start address of source next image(UV), SP mode UV frame or U P mode frame address
IEP2_SRC_ADDR_NXTV	0x0078	W	0x00000000	Start address of source next image(V), P mode V frame address
IEP2_SRC_ADDR_PREUV	0x007C	W	0x00000000	Start address of source previous image(UV), SP mode UV frame address or U P mode frame address
IEP2_SRC_ADDR_PREV	0x0080	W	0x00000000	Start address of source previous image(V), P mode V frame address
IEP2_SRC_ADDR_MD	0x0084	W	0x00000000	MD load address base register0
IEP2_SRC_ADDR_MV	0x0088	W	0x00000000	MV load address base register0
IEP2_ROI_ADDR	0x008C	W	0x00000000	ROI address register

Name	Offset	Size	Reset Value	Description
IEP2_DST_ADDR_TOPY	0x00B0	W	0x00000000	DST top frame luma address register
IEP2_DST_ADDR_BOTY	0x00B4	W	0x00000000	DST bottom frame luma address register
IEP2_DST_ADDR_TOPC	0x00B8	W	0x00000000	DST top frame chroma address register
IEP2_DST_ADDR_BOTC	0x00BC	W	0x00000000	DST bottom frame chroma address register
IEP2_DST_ADDR_MD	0x00C0	W	0x00000000	MD output base address register
IEP2_DST_ADDR_MV	0x00C4	W	0x00000000	MV output base address register
IEP2_MD_CONFIG0	0x00E0	W	0x00000044	Motion Detection configuration
IEP2_DECT_CONFIG0	0x00E4	W	0x3C3C001E	Frame field detection, pulldown detection, OSD detection, combine detection
IEP2_OSD_LIMIT_CONFIG	0x00F0	W	0x00000000	OSD limit area detection configuration
IEP2_OSD_LIMIT_AREA0	0x00F4	W	0x00000000	OSD limit area 0
IEP2_OSD_LIMIT_AREA1	0x00F8	W	0x00000000	OSD limit area 1
IEP2_OSD_CONFIG0	0x00FC	W	0x00020032	OSD detection configuration
IEP2_OSD_AREA_CONF0	0x0100	W	0x00000000	OSD area 0
IEP2_OSD_AREA_CONF1	0x0104	W	0x00000000	OSD area 1
IEP2_OSD_AREA_CONF2	0x0108	W	0x00000000	OSD area 2
IEP2_OSD_AREA_CONF3	0x010C	W	0x00000000	OSD area 3
IEP2_OSD_AREA_CONF4	0x0110	W	0x00000000	OSD area 4
IEP2_OSD_AREA_CONF5	0x0114	W	0x00000000	OSD area 5
IEP2_OSD_AREA_CONF6	0x0118	W	0x00000000	OSD area 6
IEP2_OSD_AREA_CONF7	0x011C	W	0x00000000	OSD area 7
IEP2_ME_CONFIG0	0x0120	W	0x001443A4	ME search configuration
IEP2_ME_LIMIT_CONFIG	0x0124	W	0x00001B25	ME search limit
IEP2_MV_TRU_LIST0	0x0128	W	0x00000000	MV trust list0~3
IEP2_MV_TRU_LIST1	0x012C	W	0x00000000	MV trust list4~7
IEP2_EEDI_CONFIG0	0x0130	W	0x0000000C	EEDI configuration register0
IEP2_BLE_CONFIG0	0x0134	W	0x00000001	BLE configuration register0
IEP2_COMB_CONFIG0	0x0138	W	0x001004FF	COMB DECT configuration register0
IEP2_DIL_MTN_TAB0	0x0140	W	0x00000000	DIL_MTN_TAB0 table value
IEP2_DIL_MTN_TAB1	0x0144	W	0x00000000	DIL_MTN_TAB1 table value
IEP2_DIL_MTN_TAB2	0x0148	W	0x00000000	DIL_MTN_TAB2 table value
IEP2_DIL_MTN_TAB3	0x014C	W	0x00000000	DIL_MTN_TAB3 table value
IEP2_DIL_MTN_TAB4	0x0150	W	0x01010000	DIL_MTN_TAB4 table value
IEP2_DIL_MTN_TAB5	0x0154	W	0x06050302	DIL_MTN_TAB5 table value
IEP2_DIL_MTN_TAB6	0x0158	W	0x0F0D0A08	DIL_MTN_TAB6 table value
IEP2_DIL_MTN_TAB7	0x015C	W	0x1C191512	DIL_MTN_TAB7 table value
IEP2_DIL_MTN_TAB8	0x0160	W	0x2B282420	DIL_MTN_TAB8 table value
IEP2_DIL_MTN_TAB9	0x0164	W	0x3634312E	DIL_MTN_TAB9 table value
IEP2_DIL_MTN_TAB10	0x0168	W	0x3D3C3A38	DIL_MTN_TAB10 table value
IEP2_DIL_MTN_TAB11	0x016C	W	0x40403F3E	DIL_MTN_TAB11 table value
IEP2_DIL_MTN_TAB12	0x0170	W	0x40404040	DIL_MTN_TAB12 table value
IEP2_DIL_MTN_TAB13	0x0174	W	0x40404040	DIL_MTN_TAB13 table value
IEP2_DIL_MTN_TAB14	0x0178	W	0x40404040	DIL_MTN_TAB14 table value
IEP2_DIL_MTN_TAB15	0x017C	W	0x40404040	DIL_MTN_TAB15 table value

Name	Offset	Size	Reset Value	Description
IEP2_RO_PD_TCNT	0x0400	W	0x00000000	Pulldown detection top field counter
IEP2_RO_PD_BCNT	0x0404	W	0x00000000	Pulldown detection bottom field counter
IEP2_RO_FF_CUR_TCNT	0x0408	W	0x00000000	Frame field detection current frame top field counter
IEP2_RO_FF_CUR_BCNT	0x040C	W	0x00000000	Frame field detection current frame bottom field counter
IEP2_RO_FF_NXT_TCNT	0x0410	W	0x00000000	Frame field detection next frame top field counter
IEP2_RO_FF_NXT_BCNT	0x0414	W	0x00000000	Frame field detection next frame bottom field counter
IEP2_RO_FF_BLE_TCNT	0x0418	W	0x00000000	Frame field detection current and next frame blend top field counter
IEP2_RO_FF_BLE_BCNT	0x041C	W	0x00000000	Frame field detection current and next frame blend bottom field counter
IEP2_RO_FF_COMB_NZ	0x0420	W	0x00000000	Frame field detection current frame combine detection none zero number
IEP2_RO_FF_COMB_F	0x0424	W	0x00000000	Frame field detection current frame combine detection number
IEP2_RO_OSD_NUM	0x0428	W	0x00000000	OSD area detection number
IEP2_RO_OUT_COMB_CNT	0x042C	W	0x00000000	Deinterlace output combine detection
IEP2_RO_FF_GRADT_TCNT	0x0430	W	0x00000000	Frame field detection, gradient top field counter
IEP2_RO_FF_GRADT_BCNT	0x0434	W	0x00000000	Frame field detection, gradt bottom field counter
IEP2_RO_MC_VLD_CNT	0x0438	W	0x00000000	MC valid counter
IEP2_RO_OSD_AREA0_X	0x0440	W	0x00000000	OSD area detection area0 x
IEP2_RO_OSD_AREA0_Y	0x0444	W	0x00000000	OSD area detection area0 y
IEP2_RO_OSD_AREA1_X	0x0448	W	0x00000000	OSD area detection area1 x
IEP2_RO_OSD_AREA1_Y	0x044C	W	0x00000000	OSD area detection area1 y
IEP2_RO_OSD_AREA2_X	0x0450	W	0x00000000	OSD area detection area2 x
IEP2_RO_OSD_AREA2_Y	0x0454	W	0x00000000	OSD area detection area2 y
IEP2_RO_OSD_AREA3_X	0x0458	W	0x00000000	OSD area detection area3 x
IEP2_RO_OSD_AREA3_Y	0x045C	W	0x00000000	OSD area detection area3 y
IEP2_RO_OSD_AREA4_X	0x0460	W	0x00000000	OSD area detection area4 x
IEP2_RO_OSD_AREA4_Y	0x0464	W	0x00000000	OSD area detection area4 y
IEP2_RO_OSD_AREA5_X	0x0468	W	0x00000000	OSD area detection area5 x
IEP2_RO_OSD_AREA5_Y	0x046C	W	0x00000000	OSD area detection area5 y
IEP2_RO_OSD_AREA6_X	0x0470	W	0x00000000	OSD area detection area6 x
IEP2_RO_OSD_AREA6_Y	0x0474	W	0x00000000	OSD area detection area6 y
IEP2_RO_OSD_AREA7_X	0x0478	W	0x00000000	OSD area detection area7 x
IEP2_RO_OSD_AREA7_Y	0x047C	W	0x00000000	OSD area detection area7 y
IEP2_RO_MV_HIST_BIN0	0x0480	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN1	0x0484	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN2	0x0488	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN3	0x048C	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN4	0x0490	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN5	0x0494	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN6	0x0498	W	0x00000000	MV histogram

Name	Offset	Size	Reset Value	Description
IEP2_RO_MV_HIST_BIN7	0x049C	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN8	0x04A0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN9	0x04A4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN10	0x04A8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN11	0x04AC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN12	0x04B0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN13	0x04B4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN14	0x04B8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN15	0x04BC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN16	0x04C0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN17	0x04C4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN18	0x04C8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN19	0x04CC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN20	0x04D0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN21	0x04D4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN22	0x04D8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN23	0x04DC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN24	0x04E0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN25	0x04E4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN26	0x04E8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN27	0x04EC	W	0x00000000	MV histogram
IEP2_PERF_LATENCY_CTRL0	0x0600	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_LATENCY_CTRL1	0x0604	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_MAX_LATENCY_NUM	0x0608	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_LATENCY_SAMP_NUM	0x060C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_LATENCY_ACC_SUM	0x0610	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_AXI_TOTAL_BYTE	0x0614	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_WR_AXI_TOTAL_BYTE	0x0618	W	0x00000000	Only exist when this IP has axi_performance monitor feature

Name	Offset	Size	Reset Value	Description
IEP2_PERF_WORKING_CNT	0x061C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_MMU_DTE_ADDR	0x0800	W	0x00000000	MMU DTE address
IEP2_MMU_STATUS	0x0804	W	0x00000018	MMU status
IEP2_MMU_CMD	0x0808	W	0x00000000	MMU command
IEP2_MMU_PAGE_FAULT_ADDR	0x080C	W	0x00000000	Page fault address
IEP2_MMU_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU zap one line
IEP2_MMU_INT_RAWSTAT	0x0814	W	0x00000000	MMU interruption raw status
IEP2_MMU_INT_CLEAR	0x0818	W	0x00000000	MMU interruption clear
IEP2_MMU_INT_MASK	0x081C	W	0x00000000	MMU interruption mask
IEP2_MMU_INT_STATUS	0x0820	W	0x00000000	MMU interruption status
IEP2_MMU_AUTO_GATING	0x0824	W	0x00000001	MMU auto gating configure
IEP2_MMU_ID	0x0828	W	0x00000000	MMU ID

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

8.4.2 Detail Registers Description

IEP2_FRM_START

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_iep_frm_en Frame start, Write 1, frame work enable, frame end self clear

IEP2_IEP_CONFIG0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_iep_init_dis 1'b1: Frame start not initial 1'b0: Frame start initial
21	W1C	0x0	sys_iep_sreset_p Write 1 to global reset iep, auto clear
20	RW	0x0	sw_iep_rst_protect_dis DMA bus error, default protect soft reset 1'b0: Protect reset 1'b1: Direct reset
19:17	RO	0x0	reserved
16	RW	0x0	sw_iep_debug_data_en If assert this bit, the debug signals will have data(just for power saving)
15:14	RO	0x0	reserved
13:12	RW	0x0	sw_iep_dst_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10, 2'b11: Reserved
11:10	RO	0x0	reserved
9:8	RW	0x3	sw_iep_dst_fmt 2'b00, 2'b01: Reserved 2'b10: YUV422 2'b11: YUV420
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	sw_iep_src_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10, 2'b11: P
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_iep_src_fmt 2'b00,2'b01: Reserved 2'b10: YUV422 2'b11: YUV420

IEP2_GATING_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x1	sw_reg_clk_on Reg clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
10	RW	0x0	sw_dma_clk_on Aclk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
9	RW	0x0	sw_ram_clk_on All ram clk always on 1'b0: Clk gating 1'b1: Clk always on
8	RW	0x0	sw_ctrl_clk_on CTRL clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
7	RW	0x0	sw_out_clk_on OUT clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
6	RW	0x0	sw_ble_clk_on BLE clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
5	RW	0x0	sw_eedi_clk_on EEDI clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
4	RW	0x0	sw_mc_clk_on MC clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
3	RW	0x0	sw_me_clk_on ME clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
2	RW	0x0	sw_dect_clk_on DECT clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
1	RW	0x0	sw_md_clk_on MD clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on
0	RW	0x0	sw_iep_clk_on IEP clk is auto gating, if write 1, clk always on, not gating

IEP2_STATUS

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	W1C	0x0	ro_arst_finish_done IEP protect safety reset success status, write 1 clear or frame start clear.

IEP2_INT_EN

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sw_iep_timeout_int_en Timeout interruption enable
4	RW	0x1	sw_iep_bus_error_en Bus error interruption enable
3:2	RO	0x0	reserved
1	RW	0x0	sw_iep_osd_max_en Frame process OSD detection done interrupt 1'b0: Inactive 1'b1: Active
0	RW	0x1	sw_iep_frm_done_en Frame process done interrupt 1'b0: Inactive 1'b1: Active

IEP2_INT_CLR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	W1C	0x0	sw_iep_timeout_int_clr Time out interruption clear
4	W1C	0x0	sw_iep_bus_error_clr Bus error interruption clear
3:2	RO	0x0	reserved
1	W1C	0x0	sw_iep_osd_max_clr OSD max interruption clear
0	W1C	0x0	sw_iep_frm_done_clr Frame process done interrupt clear

IEP2_INT_STS

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ro_timeout_sts Timeout error interruption status
4	RO	0x0	ro_bus_error_sts Bus error interruption status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_sts Frame process OSD detection done interrupt status
0	RO	0x0	ro_frm_done_sts Frame process done interrupt status

IEP2_INT_RAW_STS

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5	RO	0x0	ro_timeout_raw Timeout interruption raw status
4	RO	0x0	ro_bus_error_raw Bus error interruption raw status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_raw OSD max interruption raw status
0	RO	0x0	ro_frm_done_raw Frame done interruption raw status

IEP2_VIR_SRC_IMG_WIDTH

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_iep_src_vir_uv_stride Source uv virtual image width(word align)
15:0	RW	0x0000	sw_iep_src_vir_y_stride Source y virtual image width(word align)

IEP2_VIR_DST_IMG_WIDTH

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_iep_dst_vir_stride Destination virtual image width(word align)

IEP2_SRC_IMG_SIZE

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_iep_src_pic_height Source and destination image height(pixel align and need minus 1, for example 1080 need configuration 1079)
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_iep_src_pic_width Source and destination image width(pixel align and need minus 1, for example 1920 need configuration 1919)

IEP2_DIL_CONFIG0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x1	sw_dil_mv_hist_en Deinterlace MV histogram enable. 1'b1: Deinterlace need MV histogram 1'b0: MV histogram not work

Bit	Attr	Reset Value	Description
16	RW	0x0	sw_dil_roi_en Deinterlace ROI function enable bit 1'b1: Deinterlace use ROI mode 1'b0: ROI not work When ROI mode enable,each tile has 4bit for ROI mode 4'b0000: Normal mode 4'b0001: Bypass mode 4'b0010: EEDI only mode 4'b0011: Ma only mode 4'b0100: Ma mc mode(no cc) 4'b0101: Mc EEDI mode 4'b0110:4'b0111:Reserved 4'b1xxx: Mc only mode(MC's MV will be appointed by global MV based on roi[2:0])
15	RW	0x1	sw_dil_comb_en Deinterlace output result combine dectection, if is combine block back to original data, else select deinterlace result. 1'b1: Output data combine detection enable 1'b0: Output data not combine detection
14:13	RO	0x0	reserved
12	RW	0x1	sw_dil_memc_en Deinterlace use ME, MC result. 1'b1: ME, MC work enable 1'b0: ME, MC not work enable
11	RW	0x1	sw_dil_osd_en On screen display detection enable. 1'b1: OSD detection enable 1'b0: OSD not detection(下同)
10	RW	0x1	sw_dil_pd_en Pulldown detection enable. 1'b1: Pulldown detection enable 1'b0: Pulldown not dect
9	RW	0x1	sw_dil_ff_en Frame field detection work enable. 1'b1: Frame field detection enable 1'b0: Frame field not dect
8	RW	0x1	sw_dil_md_pre_en 1'b1: MD use previous frame data enable 1'b0: MD only use current frame data to calculate
7:6	RO	0x0	reserved
5	RW	0x0	sw_dil_field_order Field display order. 1'b0: TFF, top field display first 1'b1: BFF, bottom field display first
4	RW	0x0	sw_dil_out_mode Output deinterlace result to DDR, line mode or tile mode. 1'b0: LINE mode 1'b1: TILE mode

Bit	Attr	Reset Value	Description
3:0	RW	0x1	sw_dil_mode 4'b0000: DIL disable 4'b0001: I5O2 mode 4'b0010: I5O1T mode 4'b0011: I5O1B mode 4'b0100: I2O2 mode 4'b0101: I1O1T mode 4'b0110: I1O1B mode 4'b0111: Pulldown recovery mode 4'b1000: Bypass mode 4'b1001: Dectect only mode Other: Reserved

IEP2_IEP_TIMEOUT_CFG
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_iep_timeout_en IEP timeout enable
30:0	RW	0x0065b9aa	sw_iep_timeout_cnt When sw_iep_timeout_en ==1, timeout_cnt == sw_iep_timeout_cnt, IEP timeout

IEP2_IEP_VERSION_INFO
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x2	major Used for IP structure version information
27:20	RO	0x00	minor Big feature change under same structure
19:0	RO	0x00000	svnbuild RTL current SVN number

IEP2_DBG_FRM_CNT
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	dbg_frm_cnt Self increase one after a frame operation is finished. Write arbitrary value to clear to zero.

IEP2_DBG_TIMEOUT_CNT
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RO	0x00000000	dbg_timeout_cnt When sw_iep_timeout_en==1, frame counter, frame start auto clear

IEP2_SRC_ADDR_CURY
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_cury Current frame luma address, frame address

IEP2_SRC_ADDR_NXTY

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxty Next frame luma addr, frame address

IEP2_SRC_ADDR_PREY
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_prey Start address of source previous image(Y), frame address

IEP2_SRC_ADDR_CURUV
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_curuv Start address of source current image(UV), SP mode UV frame address or U P mode frame address.

IEP2_SRC_ADDR_CURV
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_curv Start address of source current image(V), P mode V frame address

IEP2_SRC_ADDR_NXTUV
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxtuv Start address of source next image(UV), SP mode UV frame address or U P mode frame address.

IEP2_SRC_ADDR_NXTV
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxtv Start address of source next image(V), P mode V frame address

IEP2_SRC_ADDR_PREUV
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_preuv Start address of source previous image(UV), SP mode UV frame address or U P mode frame address.

IEP2_SRC_ADDR_PREV
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_prev Start address of source previous image(V), P mode V frame address.

IEP2_SRC_ADDR_MD
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_md Md address, save previous frame MD gradient

IEP2_SRC_ADDR_MV
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_mv Md addr, save previous frame MV

IEP2_ROI_ADDR
Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_addr_roi ROI address base

IEP2_DST_ADDR_TOPY
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_topy DST top frame luma start address

IEP2_DST_ADDR_BOTY
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_boty Dst bottom frame luma start address

IEP2_DST_ADDR_TOPC
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_topc DST top frame chroma start address, UV save together

IEP2_DST_ADDR_BOTC
Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_botc Dst bottom frame chroma start addr, uv save together

IEP2_DST_ADDR_MD
Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_md MD addr, save previous frame md gradt, and also save current frame md grad

IEP2_DST_ADDR_MV
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_mv Output MV addr, save previous frame MV and also save current frame MV

IEP2_MD_CONFIG0

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	sw_md_theta GRADtc = CLIP(GRADtf -sw_md_theta, 0, 255);
7:4	RW	0x4	sw_md_r Gradtf *md_r*63/(gradtf*md_r*63 + gradv)
3:0	RW	0x4	sw_md_lambda Current grad * md_lambda/8 + pre grad*(8-md_lambda)/8, value range from 0~8

IEP2_DECT_CONFIG0
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x3c	sw_osd_gradv_thr Origial data grad compare with gradv thr, if more than gradv_thr, may be OSD area
23:16	RW	0x3c	sw_osd_gradh_thr Origial data grad compare with gradh thr, if more than gradh_thr, may be OSD area
15:12	RO	0x0	reserved
11:8	RW	0x0	sw_osd_area_num OSD area number, frame field dect, pulldown not detection this area, combine detection also use this value, 0~8
7:0	RW	0x1e	sw_dect_resi_thr For resi to bin, frame field, pulldown, OSD detection use this value

IEP2_OSD_LIMIT_CONFIG
Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_osd_pos_limit_num OSD constrain area detection number, real value = OSD_pos_num + 1
3:1	RO	0x0	reserved
0	RW	0x0	sw_osd_pos_limit_en OSD area constrain detection enable

IEP2_OSD_LIMIT_AREA0
Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area0 OSD constrain area 0 [6:0]: OSD constrain area0 x start, 16pixel number [13:7]: OSD constrain area0 x end, 16pixel number [22:14]: OSD constrain area0 y start, 4 pixel number [31:23]: OSD constrain area0 y end, 4 pixel number

IEP2_OSD_LIMIT_AREA1
Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area1 OSD limite area 1 [6:0]: OSD constrain area0 x start, 16pixel number [13:7]: OSD constrain area0 x end, 16pixel number [22:14]: OSD constrain area0 y start, 4 pixel number [31:23]: OSD constrain area0 y end, 4 pixel number

IEP2_OSD_CONFIG0
Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x002	sw_osd_line_num Dectecting line number should more than OSD_line_num * 4, this lines may be OSD area
15:11	RO	0x00	reserved
10:0	RW	0x032	sw_osd_pec_thr A line should more than OSD_per_thr, this line may be OSD area

IEP2_OSD_AREA_CONF0
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end0 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta0 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end0 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta0 OSD area x start, 16pixel number

IEP2_OSD_AREA_CONF1
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end1 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta1 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end1 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta1 OSD area x start, 16pixel number

IEP2_OSD_AREA_CONF2
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end2 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta2 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end2 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta2 OSD area x start, 16pixel number

IEP2_OSD_AREA_CONF3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end3 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta3 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end3 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta3 OSD area x start, 16pixel number

IEP2_OSD_AREA_CONF4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end4 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta4 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end4 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta4 OSD area x start, 16pixel number

IEP2_OSD_AREA_CONF5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end5 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta5 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end5 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta5 OSD area x start, 16pixel number

IEP2_OSD_AREA_CONF6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end6 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta6 OSD area y start, 4 pixel number
13:7	RW	0x00	sw_osd_x_end6 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta6 OSD area x start, 16pixel number

IEP2_OSD_AREA_CONF7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end7 OSD area y end, 4 pixel number
22:14	RW	0x000	sw_osd_y_sta7 OSD area y start, 4 pixel number

Bit	Attr	Reset Value	Description
13:7	RW	0x00	sw_osd_x_end7 OSD area x end, 16pixel number
6:0	RW	0x00	sw_osd_x_sta7 OSD area x start, 16pixel number

IEP2_ME_CONFIG0

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x14	sw_me_thr_offset me_thr = me_thr(from md module) - sw_me_thr_offset. This signal is signed from(-128 ~ 127)
15:12	RW	0x4	sw_mv_similar_num_thr0 MV similar check result = MV_similar_invld_num < sw_mv_similar_num_thr0
11:8	RW	0x3	sw_mv_similar_thr Surround MV similar = |cur_MV - surround_MV| < sw_mv_similar_thr
7:4	RW	0xa	sw_mv_bonus MVc calc MV, the same MV range value
3:0	RW	0x4	sw_me_pena Balance resi and grad, grad*me_pena/8, me_pena value range from 0~8

IEP2_ME_LIMIT_CONFIG

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x1b	sw_mv_right_limt MV right range limit, from 0~27, default 27
7:6	RO	0x0	reserved
5:0	RW	0x25	sw_mv_left_limt MV left range limite, from -27~0, default-27

IEP2_MV_TRU_LIST0

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list3_mv MV trust list MV3
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list3_vld MV trust list MV3 valid
23:18	RW	0x00	sw_mv_tru_list2_mv MV trust list MV2
17	RO	0x0	reserved
16	RW	0x0	sw_mv_tru_list2_vld MV trust list MV2 valid
15:10	RW	0x00	sw_mv_tru_list1_mv MV trust list MV1
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list1_vld MV trust list MV1 valid
7:2	RW	0x00	sw_mv_tru_list0_mv MV trust list MV0

Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list0_vld MV trust list MV0 valid

IEP2_MV_TRU_LIST1

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list7_mv MV trust list MV7
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list7_vld MV trust list MV7 valid
23:18	RW	0x00	sw_mv_tru_list6_mv MV trust list MV6
17	RO	0x0	reserved
16	RW	0x0	sw_mv_tru_list6_vld MV trust list MV6 valid
15:10	RW	0x00	sw_mv_tru_list5_mv MV trust list MV5
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list5_vld MV trust list MV5 valid
7:2	RW	0x00	sw_mv_tru_list4_mv MV trust list MV4
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list4_vld MV trust list MV4 valid

IEP2_EEDI_CONFIG0

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0c	sw_eedi_thr0 EEDI thr0

IEP2_BLE_CONFIG0

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x1	sw_ble_backtoma_num Left and right column of frame will back to MA, give up MC

IEP2_COMB_CONFIG0

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	sw_comb_cnt_thr Top or bottom frame combine detection compare with original combine dect
23:22	RO	0x0	reserved
21:16	RW	0x10	sw_comb_feature_thr Top or bottom frame combine detection compare with original combine dect

Bit	Attr	Reset Value	Description
15:8	RW	0x04	sw_comb_t_thr Different line compare use comb_t_thr
7:0	RW	0xff	sw_comb_osd_vld OSD area detection combine block back to original [0] area0,[1]area1....[7]area7 1'b1: Back to original 1'b0: Not back to original

IEP2_DIL_MTN_TAB0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab03 The MTN table member of number 03
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab02 The MTN table member of number 02
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab01 The MTN table member of number 01
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab00 The MTN table member of number 00

IEP2_DIL_MTN_TAB1

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab07 The MTN table member of number 07
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab06 The MTN table member of number 06
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab05 The MTN table member of number 05
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab04 The MTN table member of number 04

IEP2_DIL_MTN_TAB2

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab11 The MTN table member of number 11
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab10 The MTN table member of number 10
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab09 The MTN table member of number 09
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	sw_mtn_sub_tab08 The MTN table member of number 08

IEP2_DIL_MTN_TAB3
Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab15 The MTN table member of number 15
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab14 The MTN table member of number 14
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab13 The MTN table member of number 13
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab12 The MTN table member of number 12

IEP2_DIL_MTN_TAB4
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x01	sw_mtn_sub_tab19 The MTN table member of number 19
23	RO	0x0	reserved
22:16	RW	0x01	sw_mtn_sub_tab18 The MTN table member of number 18
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab17 The MTN table member of number 17
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab16 The MTN table member of number 16

IEP2_DIL_MTN_TAB5
Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x06	sw_mtn_sub_tab23 The MTN table member of number 23
23	RO	0x0	reserved
22:16	RW	0x05	sw_mtn_sub_tab22 The MTN table member of number 22
15	RO	0x0	reserved
14:8	RW	0x03	sw_mtn_sub_tab21 The MTN table member of number 21
7	RO	0x0	reserved
6:0	RW	0x02	sw_mtn_sub_tab20 The MTN table member of number 20

IEP2_DIL_MTN_TAB6
Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x0f	sw_mtn_sub_tab27 The MTN table member of number 27
23	RO	0x0	reserved
22:16	RW	0x0d	sw_mtn_sub_tab26 The MTN table member of number 26
15	RO	0x0	reserved
14:8	RW	0x0a	sw_mtn_sub_tab25 The MTN table member of number 25
7	RO	0x0	reserved
6:0	RW	0x08	sw_mtn_sub_tab24 The MTN table member of number 24

IEP2_DIL_MTN_TAB7
Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	sw_mtn_sub_tab31 The MTN table member of number 31
23	RO	0x0	reserved
22:16	RW	0x19	sw_mtn_sub_tab30 The MTN table member of number 30
15	RO	0x0	reserved
14:8	RW	0x15	sw_mtn_sub_tab29 The MTN table member of number 29
7	RO	0x0	reserved
6:0	RW	0x12	sw_mtn_sub_tab28 The MTN table member of number 28

IEP2_DIL_MTN_TAB8
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x2b	sw_mtn_sub_tab35 The MTN table member of number 35
23	RO	0x0	reserved
22:16	RW	0x28	sw_mtn_sub_tab34 The MTN table member of number 34
15	RO	0x0	reserved
14:8	RW	0x24	sw_mtn_sub_tab33 The MTN table member of number 33
7	RO	0x0	reserved
6:0	RW	0x20	sw_mtn_sub_tab32 The MTN table member of number 32

IEP2_DIL_MTN_TAB9
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x36	sw_mtn_sub_tab39 The MTN table member of number 39
23	RO	0x0	reserved
22:16	RW	0x34	sw_mtn_sub_tab38 The MTN table member of number 38

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:8	RW	0x31	sw_mtn_sub_tab37 The MTN table member of number 37
7	RO	0x0	reserved
6:0	RW	0x2e	sw_mtn_sub_tab36 The MTN table member of number 36

IEP2_DIL_MTN_TAB10

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x3d	sw_mtn_sub_tab43 The MTN table member of number 43
23	RO	0x0	reserved
22:16	RW	0x3c	sw_mtn_sub_tab42 The MTN table member of number 42
15	RO	0x0	reserved
14:8	RW	0x3a	sw_mtn_sub_tab41 The MTN table member of number 41
7	RO	0x0	reserved
6:0	RW	0x38	sw_mtn_sub_tab40 The MTN table member of number 40

IEP2_DIL_MTN_TAB11

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab47 The MTN table member of number 47
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab46 The MTN table member of number 46
15	RO	0x0	reserved
14:8	RW	0x3f	sw_mtn_sub_tab45 The MTN table member of number 45
7	RO	0x0	reserved
6:0	RW	0x3e	sw_mtn_sub_tab44 The MTN table member of number 44

IEP2_DIL_MTN_TAB12

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab51 The MTN table member of number 51
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab50 The MTN table member of number 50
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab49 The MTN table member of number 49
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab48 The MTN table member of number 48

IEP2_DIL_MTN_TAB13
Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab55 The MTN table member of number 55
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab54 The MTN table member of number 54
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab53 The MTN table member of number 53
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab52 The MTN table member of number 52

IEP2_DIL_MTN_TAB14
Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab59 The MTN table member of number 59
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab58 The MTN table member of number 58
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab57 The MTN table member of number 57
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab56 The MTN table member of number 56

IEP2_DIL_MTN_TAB15
Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab63 The MTN table member of number 63
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab62 The MTN table member of number 62
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab61 The MTN table member of number 61
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab60 The MTN table member of number 60

IEP2_RO_PD_TCNT
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_tcnt Pulldown detection top field counter

IEP2_RO_PD_BCNT

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_bcnt Pulldown detection bottom field counter

IEP2_RO_FF_CUR_TCNT

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_tcnt Frame field detection current frame top field counter

IEP2_RO_FF_CUR_BCNT

Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_bcnt Frame field detection current frame bottom field counter

IEP2_RO_FF_NXT_TCNT

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_tcnt Frame field detection next frame top field counter

IEP2_RO_FF_NXT_BCNT

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_bcnt Frame field detection next frame bottom field counter

IEP2_RO_FF_BLE_TCNT

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_tcnt Frame field detection current and next frame blend top field counter

IEP2_RO_FF_BLE_BCNT

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_bcnt Frame field detection current and next frame blend bottom field counter

IEP2_RO_FF_COMB_NZ

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_nz Frame field detection current frame none zero number

IEP2_RO_FF_COMB_F

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_comb_f Frame field detection current frame combine detection number

IEP2_RO_OSD_NUM

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	ro_dect_osd_cnt OSD area detection number

IEP2_RO_OUT_COMB_CNT

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_out_osd_comb_cnt Top frame and bottom frame OSD area combine number
15:0	RO	0x0000	ro_out_comb_cnt Top frame and bottom frame combine number

IEP2_RO_FF_GRADT_TCNT

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_tcnt Frame field detection,gradt top field counter

IEP2_RO_FF_GRADT_BCNT

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_bcnt Frame field detection,gradt bottom field counter

IEP2_RO_MC_VLD_CNT

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	ro_mc_vld_cnt OSD area detection number

IEP2_RO_OSD_AREA0_X

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end0 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta0 1 pixel

IEP2_RO_OSD_AREA0_Y

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26:16	RO	0x000	ro_y_end0 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta0 1 pixel

IEP2_RO_OSD_AREA1_X
Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta1 1 pixel

IEP2_RO_OSD_AREA1_Y
Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta1 1 pixel

IEP2_RO_OSD_AREA2_X
Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta2 1 pixel

IEP2_RO_OSD_AREA2_Y
Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta2 1 pixel

IEP2_RO_OSD_AREA3_X
Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end3 1 pixel
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10:0	RO	0x000	ro_x_sta3 1 pixel

IEP2_RO_OSD_AREA3_Y
Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end3 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta3 1 pixel

IEP2_RO_OSD_AREA4_X
Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta4 1 pixel

IEP2_RO_OSD_AREA4_Y
Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta4 1 pixel

IEP2_RO_OSD_AREA5_X
Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end5 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta5 1 pixel

IEP2_RO_OSD_AREA5_Y
Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end5 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta5 1 pixel

IEP2_RO_OSD_AREA6_X

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end6 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta6 1 pixel

IEP2_RO_OSD_AREA6_Y

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end6 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta6 1 pixel

IEP2_RO_OSD_AREA7_X

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta7 1 pixel

IEP2_RO_OSD_AREA7_Y

Address: Operational Base + offset (0x047C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta7 1 pixel

IEP2_RO_MV_HIST_BIN0

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist01 Mv_histogram01
15:0	RO	0x0000	ro_mv_hist00 Mv_histogram00

IEP2_RO_MV_HIST_BIN1

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist03 Mv_histogram03
15:0	RO	0x0000	ro_mv_hist02 Mv_histogram02

IEP2_RO_MV_HIST_BIN2
Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist05 Mv_histogram05
15:0	RO	0x0000	ro_mv_hist04 Mv_histogram04

IEP2_RO_MV_HIST_BIN3
Address: Operational Base + offset (0x048C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist07 Mv_histogram07
15:0	RO	0x0000	ro_mv_hist06 Mv_histogram06

IEP2_RO_MV_HIST_BIN4
Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist09 Mv_histogram09
15:0	RO	0x0000	ro_mv_hist08 Mv_histogram08

IEP2_RO_MV_HIST_BIN5
Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist11 Mv_histogram11
15:0	RO	0x0000	ro_mv_hist10 Mv_histogram10

IEP2_RO_MV_HIST_BIN6
Address: Operational Base + offset (0x0498)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist13 Mv_histogram13
15:0	RO	0x0000	ro_mv_hist12 Mv_histogram12

IEP2_RO_MV_HIST_BIN7
Address: Operational Base + offset (0x049C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist15 Mv_histogram15
15:0	RO	0x0000	ro_mv_hist14 Mv_histogram14

IEP2_RO_MV_HIST_BIN8
Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist17 Mv_histogram17
15:0	RO	0x0000	ro_mv_hist16 Mv_histogram16

IEP2_RO_MV_HIST_BIN9
Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist19 Mv_histogram19
15:0	RO	0x0000	ro_mv_hist18 Mv_histogram18

IEP2_RO_MV_HIST_BIN10
Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist21 Mv_histogram21
15:0	RO	0x0000	ro_mv_hist20 Mv_histogram20

IEP2_RO_MV_HIST_BIN11
Address: Operational Base + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist23 Mv_histogram23
15:0	RO	0x0000	ro_mv_hist22 Mv_histogram22

IEP2_RO_MV_HIST_BIN12
Address: Operational Base + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist25 Mv_histogram25
15:0	RO	0x0000	ro_mv_hist24 Mv_histogram24

IEP2_RO_MV_HIST_BIN13
Address: Operational Base + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist27 Mv_histogram27
15:0	RO	0x0000	ro_mv_hist26 Mv_histogram26

IEP2_RO_MV_HIST_BIN14
Address: Operational Base + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist29 Mv_histogram29
15:0	RO	0x0000	ro_mv_hist28 Mv_histogram28

IEP2_RO_MV_HIST_BIN15
Address: Operational Base + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist31 Mv_histogram31

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ro_mv_hist30 Mv_histogram30

IEP2_RO_MV_HIST_BIN16
Address: Operational Base + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist33 Mv_histogram33
15:0	RO	0x0000	ro_mv_hist32 Mv_histogram32

IEP2_RO_MV_HIST_BIN17
Address: Operational Base + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist35 Mv_histogram35
15:0	RO	0x0000	ro_mv_hist34 Mv_histogram34

IEP2_RO_MV_HIST_BIN18
Address: Operational Base + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist37 Mv_histogram37
15:0	RO	0x0000	ro_mv_hist36 Mv_histogram36

IEP2_RO_MV_HIST_BIN19
Address: Operational Base + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist39 Mv_histogram39
15:0	RO	0x0000	ro_mv_hist38 Mv_histogram38

IEP2_RO_MV_HIST_BIN20
Address: Operational Base + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist41 Mv_histogram41
15:0	RO	0x0000	ro_mv_hist40 Mv_histogram40

IEP2_RO_MV_HIST_BIN21
Address: Operational Base + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist43 Mv_histogram43
15:0	RO	0x0000	ro_mv_hist42 Mv_histogram42

IEP2_RO_MV_HIST_BIN22
Address: Operational Base + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist45 Mv_histogram45
15:0	RO	0x0000	ro_mv_hist44 Mv_histogram44

IEP2_RO_MV_HIST_BIN23
Address: Operational Base + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist47 Mv_histogram47
15:0	RO	0x0000	ro_mv_hist46 Mv_histogram46

IEP2_RO_MV_HIST_BIN24
Address: Operational Base + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist49 Mv_histogram49
15:0	RO	0x0000	ro_mv_hist48 Mv_histogram48

IEP2_RO_MV_HIST_BIN25
Address: Operational Base + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist51 Mv_histogram51
15:0	RO	0x0000	ro_mv_hist50 Mv_histogram50

IEP2_RO_MV_HIST_BIN26
Address: Operational Base + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist53 Mv_histogram54
15:0	RO	0x0000	ro_mv_hist52 Mv_histogram53

IEP2_RO_MV_HIST_BIN27
Address: Operational Base + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist55 Mv_histogram55
15:0	RO	0x0000	ro_mv_hist54 Mv_histogram54

IEP2_PERF_LATENCY_CTRL0
Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr Axi Read latency threshold
7:4	RW	0x0	sw_rd_latency_id Axi read channel id for latency AXI_PERF test

Bit	Attr	Reset Value	Description
3	RW	0x0	sw_axi_cnt_type 1'b0: AXI transfer test 1'b1: DDR align transfer test
2	RW	0x0	sw_axi_perf_frm_type 1'b0: Clear by software configuration 1'b1: Clear by frame end or by software configuration
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enalbe Note: user need write 1 to this bit and then write 0 to generate a clear pulse.
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

IEP2_PERF_LATENCY_CTRL1
Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type 1'b0: Count all write channels 1'b1: Count sw_aw_count_id write channel only
2	RW	0x0	sw_ar_cnt_id_type 1'b0: Count all read channels 1'b1: Count sw_ar_count_id read channel only
1:0	RW	0x0	sw_addr_align_type 2'b00: 16-Byte align 2'b01: 32-Byte align 2'b10: 64-Byte align 2'b11: 128-Byte align

IEP2_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rd_max_latency_num AXI max read latency(unit: cycles)

IEP2_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x060C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num AXI read latency total sample number

IEP2_PERF_RD_LATENCY_ACC_SUM
Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum AXI read latency (>sw_rd_latency_thr) total number

IEP2_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0614)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_rd_axi_total_byte AXI active total read bytes/DDR align read bytes

IEP2_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_wr_axi_total_byte AXI active total write bytes/ddr align write bytes

IEP2_PERF_WORKING_CNT
Address: Operational Base + offset (0x061C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	perf_working_cnt RKIP working counter

IEP2_MMU_DTE_ADDR
Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU dte address

IEP2_MMU_STATUS
Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RW	0x0	mmu_page_fault_is_write The direction of access for last page fault. 1'b0: Read 1'b1: Write
4	RW	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty
3	RW	0x1	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: The MMU can be idle in page fault mode.
2	RW	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command
1	RW	0x0	mmu_page_fault_active MMU page fault mode currently enabled. The mode is enabled by command
0	RW	0x0	mmu_paging_enabled MMU page enable

IEP2_MMU_CMD
Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	mmu_cmd The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled. 3'b000: Enable paging 3'b001: Disable paging 3'b010: Turn on stall mode 3'b011: Turn off stall mode 3'b100: Zap the entire page table cache 3'b101: Leave page fault mode 3'b110: Reset the MMU

IEP2_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_page_fault_addr mmu_page_fault_address

IEP2_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_zap_one_line Address to be invalidated from the page table cache

IEP2_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

IEP2_MMU_INT_CLEAR

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error_clear Read bus error interrupt clear, and write 1 to this register can clear read bus error interrupt.
0	RW	0x0	page_fault_clear Page fault interrupt clear, and write 1 to this register can clear page fault interrupt.

IEP2_MMU_INT_MASK

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error_int_en MMU read bus error interruption enable
0	RW	0x0	page_fault_int_en PAGE fault interruption enable

IEP2_MMU_INT_STATUS

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

IEP2_MMU_AUTO_GATING
Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_auto_gating When it is 1, the MMU will auto gating itself

IEP2_MMU_ID
Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	mmu_axi_id MMU ID configurable
3:1	RO	0x0	reserved
0	RW	0x0	reg_load_mmu_en Just for frame asynchronous using

8.5 Application Notes

Input source definition constraint
The input source definition must be 16x4 aligned, which means the image width 16 aligned and image height 4 aligned.

Normal configuration flow

- Set IEP2 related signals based on current video source information and deinterlace mode (must open frame done interruption by asserting the sw_iep_frm_done_en signal)
- Set frame start by setting signal sw_iep_frm_en = 1
- Wait for IEP2 frame done interruption
- Read back many kinds of Detection data and MVHIST, analyze these data, get the global MV, OSD information etc
- Configure the MV, OSD information back
- Set frame start for deinterlace loop

Chapter 9 DisplayPort Transmitter Controller (DPTX)

9.1 Overview

The DisplayPort Transmitter Controller (DPTX), which provides support for next generation video display interface technology. The Video Electronics Standards Association (VESA) defines the DisplayPort standard as an open digital communications interface for use in internal as well as external connections, such as:

- Interfaces within a PC or monitor (internal)
- External display connections, including interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display.

DPTX is compliant with the DisplayPort Specification Version 1.4 and supports both HDCP 1.3 and HDCP 2.2 standards. The DPTX digital controller interfaces with the DisplayPort/USB Type-C combo PHY, enabling the integration of a complete DisplayPort Interface in a USB Type-C environment.

9.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

DPTX supports the following features:

- General Features
  - DisplayPort 1.4a
  - Main Link: 1/2/4 lanes
  - Main Link: RBR/HBR/HBR2/HBR3
  - 1Mbps AUX channel
  - Single Stream Transport (SST)
  - Type-C support (alternate mode)
  - HDCP 2.2, HDCP 1.3
  - Quad Pixel Mode
  - YCrCb (3 formats), RGB support
  - Up to 48 bits per pixel
  - Support for Register based SDP (Secondary Data Packets)
  - Native AUX, I2C over AUX
  - AMBA APB Interface for internal register access and AUX access
- Video-Related Features
  - Video formats
    - CEA-861-F
    - VESA DMT
    - VESA CVT
  - Colorimetry
    - Supports up to 8/10 bits per color component
    - Supports RBG, YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0
  - Pixel clock up to 594MHz
- Audio-Related Features
  - Up to 192 KHz, 24 bits per sample LPCM
  - Up to 8 audio channels
  - I2S, S/PDIF interface supported
  - High Bit-Rate audio @768 KHz
- DPTX are not support the following features:
  - DSC(Display Stream Compression)
  - Multistream Transport (MST)
  - Dual Mode Support

9.3 Function Description

9.3.1 Architecture Overview

Fig.65-1 shows the architecture overview of DPTX.

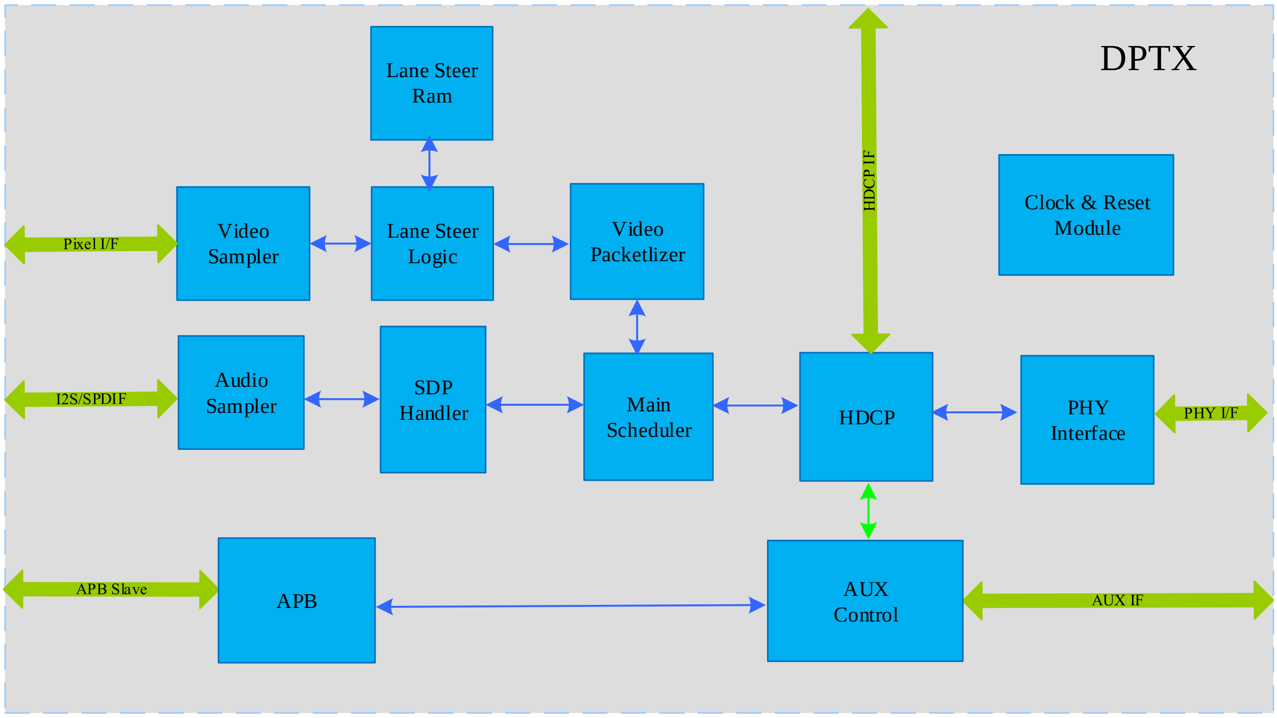

Fig. 9-1 DPTX Architecture Overview

The following sections describe the various blocks and their functionalities. DPTX uses a 32 bits internal data path for the main link.

9.3.2 Video Pixel Sampler

The video pixel sampler captures video pixel data on the video interface based on the various video formats, deep color modes. It outputs the captured video pixel data to the Video lane steering module as three separate color components.

Input data coming is registered once before it goes through a 3-stage pipeline. The 3-stage pipeline is required to capture the three-color components in various input video formats. The default delay in the video sampler is 4 cycles, which includes 3 stage pipeline and 1 stage input registering.

The video pixel sampler also gives the hsync and vsync to the lane steering logic based on what is presented on the video interface. To maintain the same pipeline delay, the hsync and vsync signals also go through the lane steering FIFO. On the rising edge and on the falling edge of the hsync and vsync a separate entry is pushed into the lane steering FIFO. When the packetizer pops out the hsync/vsync entry, it generates the hsync/vsync signals to the main scheduler.

The video is input on a 48-bit interface for supporting up to 16 bits per component mode. The data inputs are MSB aligned and for 6 bits per component mode; only the MSB 6 bits are valid for each component. The input video is sampled by the video sampler. The video sampler manipulates the video format that is input to the core, and then presents the data to the lane steering logic. The video sampler has pipelines to assemble the data and present to the lane steering logic.

9.3.3 Lane Steering Logic

The lane steering logic interfaces between the video pixel sampler and the Video packetizer. The lane steering logic takes three pixel components from the video pixel sampler and splits it into 32/64/128-bit data for each of up to four lanes in single/dual/quad pixel modes and sends it to the video Packetizer module.

The lane steering logic contains internal pipelines to assemble the data coming in from the video pixel sampler and push this data into the lane steering FIFOs in a 32/64/128-bit format. The lane steering FIFO is a 2-clock FIFO, with the pixel_clk being the write clock and the link clock being the read clock. The 32/64/128-bit data is pushed in simultaneously for all lanes. There is separate lane steering logic modules to take care of different video modes like RGB,YCbCr etc.

In the lane steering logic, the video data crosses the clock domains, from the pixel clock

(pixel_clk) domain to the link clock (link_clk) domain.
This module contains a dual clock FIFO per lane which is 39-bit wide. The lane steering FIFO is popped out by the video packetizer. The packetizer and the downstream logics run on the link clock. When the PHY interface is operating at 40 bits, then the link clock is the same as the phy_clk. But if the PHY interface is running at 20bits, then the link clock is half of the phy_clk. The video packetizer is instantiated per lane.
The lane_steer_fsm state machine in this module controls the data packing. This state machine looks at the input pixel pipeline and packs the data into 32 bits of data for each lane and pushes them into a 2-clock FIFO. The FIFO is written by the video packetizer on the pixel clock and read on the link clock. On seeing the lane steering FIFO being non empty, the video packetizer waits for threshold amount of link clock. By default, it waits for 16 clocks which is equivalent to 64 symbols (since the data width is 32), where 64 is the Transfer unit size. This threshold value could be changed by reprogramming VIDEO_CONFIG5 register. After waiting for the threshold number of link clocks, the packetizer pops out the data and send to the main scheduler. The packetizer keeps track of the transfer unit count. If the symbols transmitted is greater than the average number of symbols that is define for a particular video format (defined in VIDOE_CONFIG5.AVERAGE_SYMBOLS_PER_TU) and link rate, or if the FIFO is empty, it inserts fillers into the transfer unit until the transfer unit size of 64 is reached. During this filling time, data gets accumulated in the lane steering FIFO. During the transmission of the valid symbols, data gets filled into the FIFO and also gets popped out. The rate at which the push/pop happens varies.
The lane steering logic uses 12-stage pipelining. Each of the color components (R/G/B) go through the 12-stage pipelining. The 12 stages are required only for 6bpp mode with 4 lanes. Because this is not a configurable option, these pipeline stages are always present. If the number of lanes configured is less than 4, only a 5-stage pipeline is required.

9.3.4 Video Packetizer

The video packetizer takes data from the Video Lane Splitter to form packets based on the Tranfer Unit. The Transfer Unit Size is fixed to 64 bytes and internal data width is 32 bytes. The number of valid bytes to pack in a Transfer Unit is governed by the register fields AVERGAE_BYTES_PER_TU and AVERAGE_BYTES_PER_TU_FRAC in the VIDEO_CONFIG5 register. The software calculates this value based on the pixel rate for a given video format and the link rates, and then programs the value into the register.
The video packetizer acts on each lane. A 4-lane configuration contains four instances of the packetizer. Each instance of the packetizer must also know the total number of lanes for the packetizing logic.
The video packetizer works on a single clock domain, the link clock (link_clk).
When the lane steering FIFO goes non-empty, the packetizer waits for threshold amount of link clocks which is equivalent to a Transfer Unit. The threshold accumulates pixels in the lane steering FIFO. After threshold amounts of clocks, the packetizer transmits the pixels until the FIFO becomes empty. After average_bytes_per_tu bytes has been transmitted, based on Valid symbols per TU and TU size, video packetizer module inserts dummy data symbols and the corresponding framing symbols if required. For the following TU, it does not wait for 16 clocks, and transmits the available data in the FIFO. When the dummy data symbols are being inserted the video packetizer stops reading the lane steering FIFO.
When the Lane steering logic FIFO has a threshold amount of data, it starts reading data and transmits to the Link. The threshold is controlled by the VIDEO_CONFIG5.INIT_THRESHOLD. The FIFO must not get empty while active video is being transmitted. When the packetizer sees that the FIFO is almost empty or when average_bytes_per_tu bytes have been transmitted, it starts to insert fillers until the end of transfer unit. It also adds zero padding towards the end of active video period. The data output from the Video packetizer is multiplexed with SDP data from the SDP packetizer inside the main scheduler.
The packetizer works in the single stream mode. The data from the lane steering FIFO directly go to the scheduler. In SST mode, the lane steering FIFO is popped by the SST packetizer. But in MST mode this pop function needs to be handled by the Rate governor module through the scheduler.
When a stream is enabled but there is no pixel data on the pixel interface OR stream is not

enabled in MST mode, the stream symbol sequence generator generates the SF symbols in its VC payload timeslot and every 1024 time slot VB-ID should be inserted. This is done by the scheduler. Scheduler is in the VBLANK state during this time. In SST mode, this functionality is handled by the scheduler.

9.3.5 Main Scheduler

The main scheduler multiplexes the data coming from the video and the secondary data packets (SDP) stream. It also inserts the blanking-start and blanking-end symbols. The main scheduler maintains a timer module that tracks the start and end of each horizontal and vertical blanking.

When the data valid goes low, indicating the end of active pixels, the main scheduler inserts blanking-start control symbol and follows it up with the VB-ID information. When the data valid goes high, indicating valid pixels, the main scheduler inserts blanking-start control symbol and follows it up with the pixel transmission.

The main scheduler

- Keeps track of active video period and the blanking intervals
- Multiplexes the data from the video stream and the SDP stream to the link based on blanking intervals.
- Uses video_daten and various programmed timing parameters to derive the horizontal and vertical intervals.
- Is responsible for transmitting the blanking start (BS) and blanking end (BE) control symbols at the blanking boundary.
- Gives control to the SDP scheduler for scheduling the SDP streams at the blanking intervals.
- Transmits VB-ID, Mvid and Mauid at the start of the blanking intervals
- Gives arbitration to SDP streams, in the absence of video stream, so that dummy symbols are inserted from the SDP packetizer (Figure 2-11 of DP 1.3 spec).
- The main scheduler module also takes care of generating the video timestamp values Mvid and Nvid.

With the fixed priority arbitration, the lower numbered register sets get priority over higher numbered register sets. The SDP module frames the SDP packet based on the information programmed in the SDP register set, and also calculates the ECC for the SDP.

9.3.6 Audio Sampler

The audio sampler is responsible for capturing the audio input received, and writing it into the audio FIFO for processing by the SDP module.

9.3.6.1 I2S Interface

I2S is one of the interfaces available in the DPTX for interfacing the audio stream.

The width of the audio samples is programmable through audio register AUD_CONFIG1. I2s_data_width, to be 16 to 24 bits.

The following control bits are to be transmitted in the audio stream as per IEC specification:

- P - Parity bit
- C - Channel Status
- U - User Data
- V – Validity
- PR - Start of Block Preamble (2 bits used to indicate Preamble for start of block. The PR bit in the audio stream SDP is encoded using this bit).
  - 00: Subframe 1 and start of audio block
  - 01: Subframe 1
  - 10: Subframe 2

Each I2S data supports two audio channels. For DPTX, there are 4 i2sdata signals for supporting up to 8 audio channels, with a maximum sample frequency of 192Khz (non HBR).

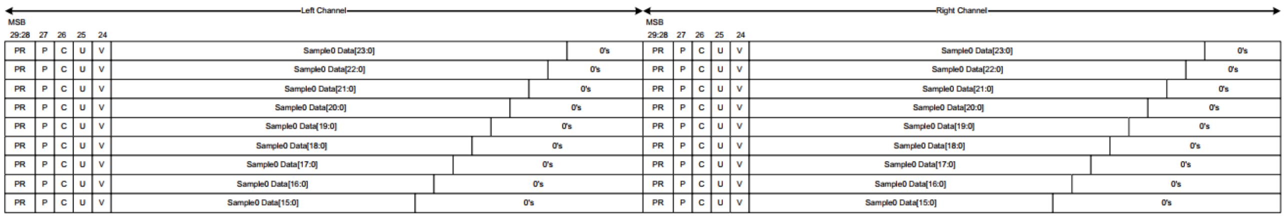

Fig. 65-2 i2s Data Input Format

Each audio sample per channel is 22 to 30 bits including preamble, control bits (auxiliary bits) and the sample data itself 16-24 bits). In one sampling frequency period, 2 sub-frames are provided or 2 samples (for the left and right channels). Since the input clock is 512 *fs, the remaining data in the subframe is ignored by the core.

High Bit Rate (HBR) Audio Support over I2S Interface

For supporting HBR audio over the I2S interface, perform the following steps:

1. Split the stream in four sub-streams by sending the stream to a FIFO with four outputs each. Each sub stream consists of a pair of samples.
2. Apply the i2sclk clock to the I2S interface with a frequency of 512*fs/4 (for example, 98.3 MHz for a 768 kHz input).
3. Set the I2S sample width to 22 bits by using the AUD_CONFIG1. I2s_data_width field register.
4. Configure the I2S interface by using the AUD_CONFIG1.audio_inf_select register. Enable all the four channels so that each channel carries a pair of samples using AUD_CONFIG1. i2s_in_en.
5. Map the I2S data sample, sampleI2S[21:0], in the following way: data[21:0] = {PR,P,C,U,V,
dataHBR[15:0]} (Where PR,P,C,U,V are IEC61937 parameters, PR is the encoded preamble, and data[15:0] is the actual HBR sample data.)
6. The I2S data must be driven according to the following table.

9.3.6.2 SPDIF Interface

The SPDIF interface uses a clock (spdifclk_i) and serial data (spdifdata_i]) to transfer audio samples / audio stream into the DPTX. Each bits of the ispdif[3:0] data corresponds to a pair of channels. Data input on the SPDIF must be BMC coded. The spdifclk_i must be synchronous to the ispdifdata_i and the frequency must be 512*fs, where fs is the original audio sampling frequency.

Each audio sample per channel is 32 bits including preamble, control bits (auxiliary bits) and the sample data itself 16-24 bits). In one sampling frequency period, 2 sub-frames are provided or 2 samples (for the left and right channels) or 64 bits. Since the SPDIF data input is BMC (Bi-Phase mark coding) coded, it takes 2 input clocks to represent a bit. So, one frame (or 2 sub frames) are represented in 128 clocks. Since the input clock is 512 *fs, the remaining data is zero coded.

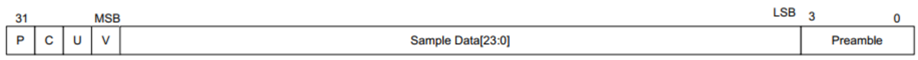

Fig. 65-3 SPDIF Data Input Format

The High Bit Rate Audio is fed on the SPDIF interface in the standard 2-channel format, with ispdifdata[0] only used for data transmission.

9.3.7 PHY Interface Layer

The controller supports Pipe complaint interface which can be used for interfacing with Synopsys PHY with the PCC logic inside the PHY.

The behavior of phy_powerdown, phy_laneX_phystatus, and phy_rate is similar to the signals in the PIPE 3.0 Spec with some minor modifications. The controller supports both 20- and 40-bit wide data interface to the PHY. The output from the main scheduler goes to the PHY interface unit. The PHY interface unit has the scrambler, the 8b/10 encoder and the training pattern generator unit. The training pattern generator is responsible for generating the patterns during link training at the request of the software. The link training is driven by the software. The software instructs the PHY interface unit and sequences it through each step of the link training. The PHY interface unit also has PCC (Power and clock control) module which is specific to interfacing with Synopsys PHY. This module is responsible for taking care of the power down changes and the clock multiplexing based on the data rate of the link. The PHY interface unit also has a Rocket IO wrapper which is used for interfacing to the rocket IO for prototyping.

9.3.8 AUX Channel Interface

The AUX channel interface is used by the DPTX controller for AUX transfers.
The AUX module uses a 16 MHz input AUX clock for oversampling and regenerating the AUX data from the serial interface in AUX Rx. The AUX module also has the Manchester encoder and decoder. Various registers are provided for the software to get notification on aux transaction completion or error status.
The AUX channel is responsible for executing the AUX transfers as requested by the software driver, via the APB interface, or by internal modules via a dedicated internal interface. The request by the software is initiated by programming the AUX registers which are implemented in the APB clock domain. Once a write to the AUX_CMD register is detected, the AUX channel initiates an AUX transfer and sets the AUX_REPLY_RECEIVED bit in the AUX_STATUS register. The transmitted data is encoded using a Manchester-II encoder. When the encoder is not driving the bus, then the transmit enable for the bidirectional AUX is not asserted. This interface runs at a nominal 1MHz (1Mbps). For a 16MHz clock for AUX is used, then each UI requires 16 clock periods to generate. The encoder generates the following sequence before any data stream is to be transmitted:

- Pre-charge: 16 zeros
- Pre-amble: 16 zeros
- AUX_SYNC_END: 2 High periods followed by 2 Low periods
- Data to be transmitted
- AUX_STOP: 2 High periods followed by 2 Low periods

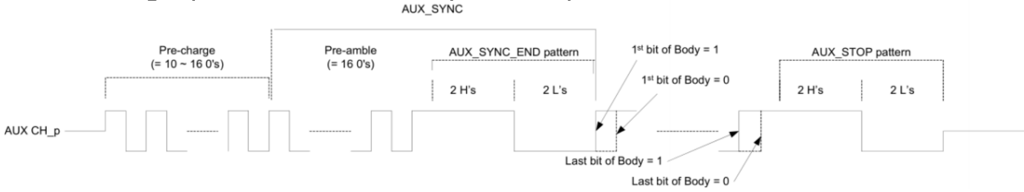

Fig. 65-4 AUX sequence

When all the data is transmitted, the AUX channel waits for a response. A 400uSec timer starts to limit the reply wait time. The Sink reply is captured & latched into the AUX status and data registers implemented in the APB block but also available on the internal bus to be consumed by the internal requesters. It's the SW responsibility to interpret the status and decide about the next transfer. The internal requests from the HDCP modules are limited to Native AUX. The internal requesters are expected to interpret correctly the ACK/NACK/DEFER responses, then decide how to proceed. The AUX_REPLY_RECEIVED bit is reset after the reply is received or timeout occurred.
Once the SW initiates an AUX request, some checks are performed to make sure its a legal request. The AUX_CMD.AUX_CMD_TYPE setting are compared with the 8 possible legal commands and the AUX_CMD.AUX_Byte_Length is checked so that:

- Read request is 1 byte
- Write does not exceed 16 bytes (1 + N, where N is 1-16)

9.3.9 Secondary Data Packet (SDP)

This section explains the how SDPs other than the Audio Stream SDPs are handled by the DPTX.
The DPTX controller has various software programmable registers through which the driver programs the header and the payload of the various SDPs, then programs the SDP Vertical/Horizontal & Manual control registers to enable specific SDP transmission and set whether the SDP is transmitted in the vertical, horizontal or both blanking intervals. The Manual control is used to control whether a SDP is transmitted once or continuously in the specified intervals.
DPTX always transmits the SDP as size of 32 bytes. Payloads less than this size are padded with zeros to make it 32 bytes.

- **Vendor Specific Infoframe Scheduling**

According to DP spec 1.3, section 2.2.5.1, the source should comply with the CEA861-F spec

for transmission of any Infoframe. As per CEA861-F, a source should support transmission of more than one VSIFs in a vertical blanking interval. DPTX SDP register banks allows transmission of more than one VSIFs in a vertical blanking interval. CEA861-F also talks about transmitting the version1/version2, where version2 used to indicate a change in the payload of the VSIF. This is also supported by the controller. The driver has to make sure that the multiple VSIFs to be transmitted in a vertical interval has to be programmed from a lower to higher continuously in the SDP register bank. For example if there are 4 VSIFs to be transmitted in an interval, then the 1 to 4 VSIFs should be programmed in SDP register bank N to N+4, where the first VSIF should be programmed in register bank N and fourth VSIF should be programmed in register bank N+4.
Either auto or manual mode can be used to transmit the VSIFs. If not using manual mode, then the specific register banks should be disabled before making a change and re enabling.

- **Audio Timestamp SDP**

Audio Timestamp SDP payload, which has the Maud and Naud values are generated by the hardware. There is no separate register for programming the payload for Audio Timestamp SPDs. The software still needs to set the corresponding auto enable bit in the Replace this with SDP_VERTICAL/HORIZONTAL_CTRL register for enabling the transmission of the Audio Timestamp SDP.
In the absence of Main video stream, controller makes sure that the Audio Timestamp SDP is transmitted once every 512th BS symbol set.

- **Audio Stream SDPs**

The audio samples are packed into the audio stream SDP in a 2-channel format or an 8-channel format. 2 channel mode is only used when only channel 1 /2 are active. In this case the AUD_CONFIG1.num_channels should be set to 2, and AUD_CONFIG1.audio_data_in_en should have a value of only 1. 8 channel mode is used whenever audio samples are available for channels 3-8. In this case AUD_CONFIG1.num_channels should be set to 8 and the AUD_CONFIG1.audio_data_in_en can be set to any value based on which channels the samples are available on.
In an 8 channel operation if only 4 channels have samples active (AUD_CONFIG1.audio_data_in_en[3:0] == 4'b1001), then the audio stream SDPs are transmitted in an 8-channel mode and data for channels 3,4,5,6 are zeroed out. The sample present bit for these channels are still set.
Zero padding of sample data at the audio interface is required in case the number of transmitted audio channels is odd. No zero padding is required if the corresponding AUD_CONFIG1.AUDIO_DATA_IN_EN is set to 1’b0.
In the absence of Main video stream, controller makes sure that the Audio Infoframe SDP if enabled, is transmitted once every 512th BS symbol set.

9.3.10 High-Bandwidth Digital Content Protection (HDCP)

The DPTX core can be configured to support HDCP. When HDCP is enabled, it can be programmed to support HDCP 2.2 or HDCP 1.3 authentication protocols.
The HDCP 2.2 core contains a processor to fetch the instructions and data from the system memory. So, the HDCP core has a DMA master AXI interface.
This module is responsible for reading the ciphers and using them to encrypt the data. When encryption is enabled, this module reads cipher from HDCP1.3 or HDCP2.2 block based on the mode of operation and XORs the cipher with data; control symbols are bypassed.
It also maintains the Link verification pattern. Link verification pattern is shifted by one on every blanking interval and reset when encryption is disabled.
There is also a debug option to bypass encryption by not XORing the data with cipher with encryption enabled. This is only for debug purpose and must be locked using the HDCPCFG.HDCP_LOCK bit

9.3.10.1 Overview of HDCP 2.2

On NACK, DEFER response or ACK response with fewer bytes from sink, the ESM retries the entire AUX transaction — but not the full HDCP transaction. For example, when the ESM reads 522-byte Rx certificate and has successfully read the first 128 bytes, then it does a 16-byte read request for bytes 129-144 and gets a NACK, DEFER, or ACK with fewer than 16 bytes. It then re-attempts from byte 129, not from byte 1 (and not from byte (129 + # of bytes received)).

The SHALE hardware can be programmed to break up transfers into chunks of 4, 8 or 16 bytes but this is a static configuration parameter and cannot be adjusted on the fly. Re-attempts are always done with the same transaction size.
Retrying authentication is the responsibility of the application software controlling the ESM. When it has been determined that the Rx is 2.2 capable, the Tx retries infinitely until the device is disconnected or HDCP is wiggled. Retries are done at the rate of the send cert timeout (100 ms), so it is effective immediately.

9.3.10.2 Overview of HDCP 1.3

All AUX transfer requests from authentication and revocation state machine are handled in this module. It is responsible for forming the aux transfer commands and holding the values read in internal registers for use by authentication and revocation state machine (KSV list read is stored in the revocation RAM).
On NACK, DEFER response or ACK response with fewer bytes from sink, the transfer is retried
automatically from the point where the transfer stopped. For example, if HDCP1.3 reads 16 bytes, but sinks return 1byte with NAK response, HDCP1.3 retries only for the remaining 15bytes.
When seven consecutive NACK or DEFER response is received, HDCP interrupt event is generated.

- HDCP1.3 Encryption Signaling block implements the display port encryption signaling defined in HDCP1.3 spec.
- HDCP API Interface register Bank contains registers related to KSVs, AN, DPK programming, SHA calculation and GPIO status.
- HDCP SFR register Bank contains HDCP configuration register, HDCP observation register, HDCP interrupt related registers.
- HDCP1.3 DPK registers are used when ROM less configuration is chosen. DPKs are programmed by software and are stored in this module. It is used by cipher module for the keys.

Controller retries authentication indefinitely until the HDCP enable bit is reset by the application.

9.4 Register Description

9.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

9.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DPTX_VERSION_NUMBER	0x0000	W	0x3231312A	Version Number Register
DPTX_VERSION_TYPE	0x0004	W	0x65613038	Version Type Register
DPTX_CONFIG_REG1	0x0100	W	0x02212D0D	RTL Configuration Parameter Register 1
DPTX_CONFIG_REG2	0x0104	W	0x08001000	RTL Configuration Parameter Register 2
DPTX_CONFIG_REG3	0x0108	W	0x0000016C	RTL Configuration Parameter Register 3
DPTX_CCTL	0x0200	W	0x00000004	Global Control Register
DPTX_SOFT_RESET_CTRL	0x0204	W	0x00000000	Software Initiated Reset Register
DPTX_VSAMPLE_CTRL	0x0300	W	0x00000000	Video Sampler Control Register
DPTX_VSAMPLE_STUFF_CTRL1	0x0304	W	0x00000000	Video Sampler Data Stuff Control Register
DPTX_VSAMPLE_STUFF_CTRL2	0x0308	W	0x00000000	Stuff Control for RCR/GY Data Register
DPTX_VINPUT_POLARITY_CTRL	0x030C	W	0x00000000	Video Input Polarity Control Register

Name	Offset	Size	Reset Value	Description
DPTX_VIDEO_CONFIG1	0x0310	W	0x02800280	Video Configuration Register1
DPTX_VIDEO_CONFIG2	0x0314	W	0x002D01E0	Video Configuration Register2
DPTX_VIDEO_CONFIG3	0x0318	W	0x00600010	Video Configuration Register3
DPTX_VIDEO_CONFIG4	0x031C	W	0x0002000A	Video Configuration Register4
DPTX_VIDEO_CONFIG5	0x0320	W	0x00030796	Video Configuration Register5
DPTX_VIDEO_MSA1	0x0324	W	0x00230090	Main Stream Attribute Register 1
DPTX_VIDEO_MSA2	0x0328	W	0x00000000	Main Stream Attribute Register 2
DPTX_VIDEO_MSA3	0x032C	W	0x00000000	Main Stream Attribute Register 3
DPTX_VIDEO_HBLANK_INTERVAL	0x0330	W	0x00000000	Hblank Interval Symbol Register
DPTX_AUD_CONFIG1	0x0400	W	0x12001202	Audio Input Control Register
DPTX_SDP_VERTICAL_CTRL	0x0500	W	0x00000000	Secondary Data Packets Vertical Blanking Register
DPTX_SDP_HORIZONTAL_CTRL	0x0504	W	0x00000000	Secondary Data Packets Horizontal Blanking Register
DPTX_SDP_STATUS_REGISTER	0x0508	W	0x00000000	Secondary Data Packets Status Register
DPTX_SDP_MANUAL_CTRL	0x050C	W	0x00000000	Manual Controlled Transmit of SDP
DPTX_SDP_STATUS_EN	0x0510	W	0x00000000	SDP Status Interrupt Enable Register
DPTX_SDP_REGISTER_BANK	0x0600	W	0x00000000	SDP Register bank
DPTX_PHYIF_CTRL	0x0A00	W	0x00060000	PHY Interface Control Register
DPTX_PHY_TX_EQ	0x0A04	W	0x00000000	PHY Pre-emphasis and Voltage Swing Control Register
DPTX_CUSTOMPAT0	0x0A08	W	0x00000000	Custom 80-bit pattern Position Register 0
DPTX_CUSTOMPAT1	0x0A0C	W	0x00000000	Custom 80-bit pattern Position Register 1
DPTX_CUSTOMPAT2	0x0A10	W	0x00000000	Highest 20-bits of the 80-bit pattern.
DPTX_HBR2_COMPLIANCE_SCRAMBLER_RESET	0x0A14	W	0x000000FC	CP2520 Pattern Length
DPTX_PHYIF_PWRDOWN_CTRL	0x0A18	W	0x00000000	Lane Powerdown Control
DPTX_AUX_CMD	0x0B00	W	0x00000000	AUX Configuration Register
DPTX_AUX_STATUS	0x0B04	W	0x00000000	AUX Status Register
DPTX_AUX_DATA0	0x0B08	W	0x00000000	AUX Data- First 4 bytes
DPTX_AUX_DATA1	0x0B0C	W	0x00000000	AUX Data Second 4 bytes.
DPTX_AUX_DATA2	0x0B10	W	0x00000000	AUX Data Third 4 bytes
DPTX_AUX_DATA3	0x0B14	W	0x00000000	AUX Data Fourth 4 bytes
DPTX_PHYREG_CMDADDR	0x0C00	W	0x00000000	PHY Address Register
DPTX_PHYREG_DATA	0x0C04	W	0x00000000	PHY Write and Read DATA
DPTX_TYPEC_CTRL	0x0C08	W	0x00000000	Type-C Control Register
DPTX_GENERAL_INTERRUPT	0x0D00	W	0x00000000	General Interrupt Register
DPTX_GENERAL_INTERRUPT_ENABLE	0x0D04	W	0x00000000	General Interrupt Enable Register
DPTX_HPD_STATUS	0x0D08	W	0x00000000	HPD Interrupt Status Register
DPTX_HPD_INTERRUPT_ENABLE	0x0D0C	W	0x00000000	HPD Interrupt Enable Register
DPTX_HDCPCFG	0x0E00	W	0x00000000	HDCP Config Register

Name	Offset	Size	Reset Value	Description
DPTX_HDCPOBS	0x0E04	W	0x00000000	HDCP Observation Register
DPTX_HDCPAPIINTCLR	0x0E08	W	0x00000000	HDCP Interrupt Clear Register
DPTX_HDCPAPIINTSTAT	0x0E0C	W	0x00000000	HDCP Interrupt Status Register
DPTX_HDCPAPIINTMSK	0x0E10	W	0x00000000	HDCP Interrupt Mask Register
DPTX_HDCPKSVMEMCTRL	0x0E18	W	0x00000000	HDCP KSV Memory Controller Register
DPTX_HDCP_REVOC_RAM_i	0x0E20	W	0xFFFFFFFF	HDCP Revocation RAM space
DPTX_HDCPREG_BKSV0	0x3600	W	0x00000000	HDCP BKSV Status Register 0
DPTX_HDCPREG_BKSV1	0x3604	W	0x00000000	HDCP BKSV Status Register 1
DPTX_HDCPREG_ANCONF	0x3608	W	0x00000000	HDCP AN Bypass Control Register
DPTX_HDCPREG_AN0	0x360C	W	0x00000000	HDCP Forced AN Register 0
DPTX_HDCPREG_AN1	0x3610	W	0x00000000	HDCP Forced AN Register 1
DPTX_HDCPREG_RMLCTL	0x3614	W	0x00000000	HDCP Encrypted Device Private Keys Control Register
DPTX_HDCPREG_RMLSTS	0x3618	W	0x00000000	HDCP Encrypted DPK Status Register
DPTX_HDCPREG_SEED	0x361C	W	0x00000000	HDCP Encrypted DPK Seed Register 0
DPTX_HDCPREG_DPK0	0x3620	W	0x00000000	HDCP Encrypted DPK Data Register 0
DPTX_HDCPREG_DPK1	0x3624	W	0x00000000	HDCP Encrypted DPK Data Register 1
DPTX_HDCP22GPIOSTS	0x3628	W	0x00000000	HDCP22 controller GPIO output status
DPTX_HDCP22GPIOCHNGSTS	0x362C	W	0x00000000	HDCP22 controller GPIO output change status
DPTX_HDCPREG_DPK_CRC	0x3630	W	0x00000000	HDCP Encrypted DPK Data CRC Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.3 Detail Registers Description

DPTX_VERSION_NUMBER

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x3231312a	VERSION_NUMBER Version Number of the DPTX

DPTX_VERSION_TYPE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x65613038	VERSION_TYPE Version type of the DPTX

DPTX_CONFIG_REG1

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	DSC The value of the parameter DPTX_DSC_EN
29	RO	0x0	GEN2_PHY The value of the parameter DPTX_COMBO_PHY_C10_GEN2.
28:25	RO	0x1	NUM_DSC_ENC The value of the parameter DPTX_NUM_DSC_ENC.

Bit	Attr	Reset Value	Description
24	RO	0x0	FEC_EN The value of the parameter DPTX_FEC_EN
23	RO	0x0	EDP_EN The value of the parameter DPTX_EDP_EN.
22	RO	0x0	DSC_EN Indicates if Internal DSC is enabled or not
21:19	RO	0x4	MP_MODE 3'b001: Single Pixel Mode. 3'b010: Dual Pixel Mode. 3'b100: Quad Pixel Mode.
18:16	RO	0x1	NUM_STREAMS 3'h1: SST Mode. 3'h2: Two Streams 3'h3: Three Streams 3'h4: Four Streams
15:14	RO	0x0	reserved_15_14 Reserved
13:12	RO	0x2	SYNC_DEPTH 2'b10: Indicates that 2 stage synchronizers being used 2'b11: Indicates that 3 stage synchronizers being used
11	RO	0x1	DPK_8BIT 1'b1: ROM width is 8 bits 1'b0: ROM width is 56bits
10	RO	0x1	DPK_ROMLESS When 1, disables the use of External ROM for storing Device Private Keys
9	RO	0x0	FPGA_EN When enabled, configures the core to have the audio and video generators instantiated inside the DPTX top level.
8:4	RO	0x10	SDP_REG_BANK_SIZE Specifies the number of SDP register banks supported. Enabling each register bank instantiates nine 32-bit registers for the transmission of 32Byte SDP packet.
3	RO	0x1	PHY_USED The value of the parameter DPTX_PHYIF_TYPE 1'b0: Vendor PHY 1'b1: PIPE Compliant PHY
2:1	RO	0x2	AUDIO_SELECT The value of parameter audio_select 2'b00: I2S Interface 2'b01: SPDIF Interface 2'b10: I2S and SPDIF Interface 2'b11: None
0	RO	0x1	HDCP_SELECT Reflects the hardware parameter hdcp_en 1'b0: No 1'b1: Yes

DPTX_CONFIG_REG2

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0800	DSC_MAX_NUM_LINES The value of the parameter DSC_MAX_NUM_LINES
15:0	RO	0x1000	DSC_MAX_PIXS_PER_LINE The value of the parameter DSC_MAX_PIXS_PER_LINE

DPTX_CONFIG_REG3
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved_31_9 Reserved
8:7	RO	0x2	PHY_TYPE 2'b00: Vendor PHY 2'b01: RocketIO FPGA Only 2'b10: Pipe Compliant PHY 2'b11: Reseved
6	RO	0x1	DSC_NATIVE_422_EN The value of the parameter DSC_NATIVE_422_EN
5	RO	0x1	DSC_NATIVE_420_EN The value of the parameter DSC_NATIVE_420_EN
4:0	RO	0x0c	DSC_MAX_BPC The value of the parameter DSC_MAX_BPC

DPTX_CCTL
Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	ENHANCE_FRAMING_WITH_FE When set controller follows enhanced framing with FEC as specified in section 3.5.1.1 of the DP1.4 spec. Configure this bit when enabling FEC on sink ie before setting FEC_READY bit in sink
28	RW	0x0	INITIATE_MST_ACT_SEQ Only used in MST mode and should be programmed to trigger the link to start an ACT sequence with the DPRX of the branch device immediately connected to the DPTX.
27	RW	0x0	ENABLE_eDP This bit is used to control the operation of the controller as an Embedded DisplayPort controller (eDP) or a standard DisplayPort Controller compliant with the DisplayPort Spec Ver 1.4. 1'b1: Controller operates in eDP mode 1'b0: Controller operates in standard DisplayPort mode eDP features are disabled by default. Program this bit only if you have chosen to enable eDP features by seeing the parameter DPTX_EDP_EN = 1. When eDP is enabled FEC should not be enabled (ENABLE_FEC should be 0).
26	RW	0x0	ENABLE_FEC This bit is used to enable the FEC feature. Set this bit to 1 to enable the FEC functionality. If FEC is disabled during core configuration (DPTX_FEC_EN=0), then writing to this bit has no effect.
25	RW	0x0	ENABLE_MST_MODE This bit is used for enabling the MST mode of operation.
24:17	RW	0x00	BS_512_SCALE_DOWN When SR_SCALE_DOWN is set, this controls the 512 scale down count.

Bit	Attr	Reset Value	Description
16	RW	0x0	SR_SCALE_DOWN "Every 512th BS symbol must be replaced with an SR symbol by a DPTX to reset the LFSR of the scrambler". For simulation, a scale down factor has been added and this bit controls the scaledown. When set to 1 the scrambler reset replaces Blanking Start after CCTL.BS_512_SCALE_DOWN value. When set to 0 scrambler reset replaces Blanking Start after 512 Blanking Starts
15:12	RO	0x0	reserved
11:8	RW	0x0	DEBUG_CONTROL Used for controlling the debug bus output. By configuring this register different signals selected to the output 64bits debug bus. No signal is selected and the output is '0' when the register is in its default state. 4'b0000: No signal is selected. 4'b0001: AUX 4'b0010: AUDIO 4'b0011: VIDEO 4'b0100: LINK 4'b0101: HDCP1.3 4'b0110: HDCP2.2 4'b0111: SDP 4'b1XXX: reserved
7	RO	0x0	reserved
6	RW	0x0	SEL_AUX_TIMEOUT_32MS When set to 1 the Aux timeout value is 3.2ms instead of 400us
5	RW	0x0	DISABLE_INTERLEAVING When set to 1 the nibble interleaving logic implemented as part of SDP packets generation is disabled.
4	RW	0x0	FORCE_HPD Used for testing only. It allows software to force the HPD value to 1 when writing 1. Otherwise does not impact the external HPD input.
3	RW	0x0	SCALE_DOWN_MODE When programmed to 1 the debounce filter on the HPD input is reduced from 100mSec in normal operation to 10uSec. This bit does not have any impact on the IRQ generation timing.
2	RW	0x1	DEFAULT_FAST_LINK_TRAIN_E When set after coming out of power on reset the controller starts fast link training for 1lane RBR rate without the driver intervention. The default video timings are set for 640x480 timing format 6bpc.
1	RW	0x0	ENHANCE_FRAMING_EN When set, controller follows enhanced framing. Configure this bit based on enhanced framing support of sink
0	RW	0x0	SCRAMBLE_DIS 1'b1: Disable scramble. 1'b0: Scramble enabled (default). When set, DPTX link does not scramble data on the main link. Enabling or disabling this bit resets the scrambler.

DPTX_SOFT_RESET_CTRL

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	AUDIO_SAMPLER_RESET_STREAM3 Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. This field is valid only for MST mode and is used for the reset of audio streams 3.
10	RW	0x0	AUDIO_SAMPLER_RESET_STREAM2 Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. This field is valid only for MST mode and is used for the reset of audio streams 2.
9	RW	0x0	AUDIO_SAMPLER_RESET_STREAM1 Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. This field is valid only for MST mode and is used for the reset of audio streams 1.
8:5	RW	0x0	VIDEO_RESET Software sets this bit to reset the video logic. In MST mode each bit controls the reset of a specific Video Stream. Bit5-8 controls the soft reset of Video stream-0 to 3.
4	RW	0x0	AUX_RESET Software sets this bit to start the aux channel reset.
3	RW	0x0	AUDIO_SAMPLER_RESET Software sets this bit to start the audio sampler reset. This also clears the audio FIFOs. In MST mode, this bit is used for Stream0.
2	RW	0x0	HDCP_MODULE_RESET Software sets this bit to start the HDCP module reset
1	RW	0x0	PHY_SOFT_RESET Software sets this bit to start the PHY reset process.
0	RW	0x0	CONTROLLER_RESET Software sets this bit to start the controller reset process. This also initiates a PHY reset.

DPTX_VSAMPLE_CTRL

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	STREAM_TYPE This is a per stream control defining the stream type. RepeaterAuth_Stream_Manage of HDCP2.2 specification. This field is valid only when HDCP MST are enabled.
24	RW	0x0	ENCRYPTION_ENABLE This is a per stream control to enable encryption. Setting ofthis bit has significance only when operating in MST mode or eDP. In non eDP SST operation, this bit has no significance. In MST mode or when eDP is enabled, this bit control the encryption to be used. In MST mode, this bit control HDCP encryption for a specific stream. HDCPCFG register controls the global enable of HDCP. In eDP mode this bit controls the enabling of ASSR feature as specified in section 3.5 of eDP1.4b spec and Section 2.10 of DP1.4 spec. When eDP is enabled, HDCP should be disabled and HDCPCFG[1] should not be set.
23	RW	0x0	ENABLE_DSC Set this bit to 1 to enable Display Stream Compression (DSC) on this specific stream. The software driver can set this bit only if DSC is enabled during configuration (DPTX_DSC_EN = 1 or 2). Otherwise writing 1 1 to this bit does not take effect.

Bit	Attr	Reset Value	Description
22:21	RW	0x0	PIXEL_MODE_SELECT This field is used to select the single/dual/quad pixel mode of operation. 2'b00: Single pixel mode (default) 2'b01: Dual pixel mode 2'b10: Quad pixel mode. 2'b11: Reserved.
20:16	RW	0x00	VIDEO_MAPPING Video input mapping color space/depth Video Input mapping (color space/color depth) with DSC disabled/enabled(VSAMPLE_CTRL.ENABLE_DSC=0/1): 0: RGB 6bits (Reserved) 1: RGB 8bits (RGB 8bits) 2: RGB 10bits (RGB 10bits) 3: RGB 12bits (RGB 12bits) 4: RGB 16bits (Reserved) 5: YCbCR4:4:4 8bits (YCbCr4:4:4 8bits) 6: YCbCr4:4:4 10bits (YCbCr4:4:4 10bits) 7: YCbCr4:4:4 12bits (YCbCr4:4:4 12bits) 8: YCbCr4:4:4 16bits (Reserved) 9: YCbCR4:2:2 8bits (Simple YCbCr4:2:2 8bits) 10: YCbCr4:2:2 10bits (Simple YCbCr4:2:2 10bits) 11: YCbCr4:2:2 12bits (Simple YCbCr4:2:2 12bits) 12: YCbCr4:2:2 16bits (Reserved) 13: YCbCR4:2:0 8bits (YCbCR4:2:0 8bits) 14: YCbCr4:2:0 10bits (YCbCR4:2:0 10bits) 15: YCbCr4:2:0 12bits (YCbCR4:2:0 12bits) 16: YCbCr4:2:0 16bits (Reserved) 17: YOnly 8bits (native YCbCr4:2:2 8bits) 18: YOnly 10bits (native YCbCr4:2:2 10bits) 19: YOnly 12bits (native YCbCr4:2:2 12bits) 20: YOnly 16bits (Reserved) 23: RAW 8bits. (Reserved) 24: RAW 10bits (Reserved) 25: RAW 12bits (Reserved) 27: RAW 16bits (Reserved) Others: Reserved.
15:6	RO	0x000	reserved
5	RW	0x0	VIDEO_STREAM_ENABLE 1'b0: Video stream Disable 1'b1: Video stream Enable When set to 0, no video stream is transmitted. Video inputs are ignored and NoVideoStream_flag in the VB-ID is set.
4	RW	0x0	INTERNAL_DE_GENERATOR 1'b1: Enable internal data generator 1'b0: Data enable signal available at the input. When the external logic which drives the pixel data does not generate the video data enable, then enabling this bit forces the controller to generate the video enable internally. Note: This feature is currently not supported and therefore should not be used.
3:0	RO	0x0	reserved

DPTX_VSAMPLE_STUFF_CTRL1
Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	BCB_STUFF_DATA Data to be stuffed on B/Cb data path.
15:3	RO	0x0000	reserved
2	RW	0x0	GY_DATA_STUFFING_EN Enable stuffing on internal G/Y data lines.
1	RW	0x0	RCR_DATA_STUFFING_EN Enable stuffing on internal R/Cr data lines.
0	RW	0x0	BCB_DATA_STUFFING_EN Enable stuffing on internal B/Cb data lines

DPTX_VSAMPLE_STUFF_CTRL2

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	GY_STUFF_DATA Data to be stuffed on G/Y data path.
15:0	RW	0x0000	RCR_STUFF_DATA Data to be stuffed on R/Cr data path.

DPTX_VINPUT_POLARITY_CTRL

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	DE_IN_POLARITY de input polarity 1'b1: Active low 1'b0: Active high
1	RW	0x0	HSYNC_IN_POLARITY Hsync input polarity 1'b1: Active high 1'b0: Active low
0	RW	0x0	VSYNC_IN_POLARITY Vsync input polarity 1'b1: Active high 1'b0: Active low

DPTX_VIDEO_CONFIG1

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0280	HACTIVE Input video Horizontal active pixel region width. Number of Horizontal active pixels [0...8191].
15:2	RW	0x00a0	HBLANK Input video Horizontal blanking pixel region width. Number of Horizontal blanking pixels [0...4095].
1	RW	0x0	I_P Input video mode 1'b1: Interlaced 1'b0: Progressive
0	RW	0x0	R_V_BLANK_IN_OSC Used for CEA861-D modes with fractional Vblank (for example, modes 5, 6, 7, 10, 11, 20, 21, and 22). For more modes, see the CEA861-D specification. Note: Set this field to 1 for video mode 39, although there is no Vblank oscillation. 1b: Active high

DPTX_VIDEO_CONFIG2

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RW	0x002d	VBLANK Input video Vertical blanking pixel region width. Number of Vertical blanking lines.
15:0	RW	0x01e0	VACTIVE Input video Vertical active pixel region width. This bit field holds bits 15:0 of number of Vertical active pixels.

DPTX_VIDEO_CONFIG3

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	RW	0x0060	H_SYNC_WIDTH Input video Hsync active pulse width. Integer number of pixel clock cycles [0...511].
15:0	RW	0x0010	H_FRONT_PORCH Input video Hsync active edge delay. Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...4095].

DPTX_VIDEO_CONFIG4

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0002	V_SYNC_WIDTH Input video Vsync active pulse width. Integer number of video lines [0...63].
15:0	RW	0x000a	V_FRONT_PORCH Input video Vsync active edge delay. Integer number of hsync pulses from "de" non active edge of the last "de" valid period. [0...255]. Specified in terms of number of lines. Value After Reset: 0

DPTX_VIDEO_CONFIG5

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:21	RW	0x0	INIT_THRESHOLD_HI Most Significant two bits of INT_THRESHOLD.
20	RW	0x0	ENABLE_3D_FRAME_FIELD_SE Set this bit to 1 if the video format being transmitted is 3D video format and Frame/Filed sequential 3D mode is used. Set this bit to 0 (default) if no 3D video is being transmitted, or Frame/Filed sequential 3D format is not being used. Refer to section "3D Stereo Mode Support" for more details.

Bit	Attr	Reset Value	Description
19:14	RW	0x0c	AVERAGE_BYTES_PER_TU_FR This is the fractional portion of the value calculated in the average bytes per TU. The first decimal value in the fractional part should be programmed here. For example, if the average bytes per TU is 24.34, then this field should be programmed to a value of 3. In SST mode only bits 19:16 is used. In MST mode, this field should be programmed with the fractional value of the VC payload size calculated by the Payload bandwidth manager. as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. The fractional value calculated times 64 should be programmed in this field. For example if the vc_payload_size calculated is 34.23, a value of 0.23*64 = 15 (14.72 rounded to the nearest integer) should be programmed here. For over 64 MTPs controller transmits AVERAGE_BYTES_PER_TU+1 timeslots with valid symbols for average_bytes_per_tu MTPs for this streams and for 64-average_bytes_per_tu MTPS AVERAGE_BYTES_PER_TU timeslots will have valid symbols. Here is an example for calculating the average_bytes_per_tu_frac in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu_frac = frac((peak_stream_bandwidth/link_bandwidth)*64))*64 = frac(4.475) *64= 0.47*64 = 30.08 . Program the frac value rounded to the nearest integer which is 30.
13:7	RW	0x0f	INIT_THRESHOLD This is the number of clock cycles the link should wait for the pixels to accumulate at the beginning of every video line before it starts transmitting. This threshold influences the link capability to maintain the avarge valid symbols per TU. For Non-DSC Mode: If the calculated average bytes per tu value is less than 6 then the threshold value should be programmed to 32. For RGB or YCbCr444 modes if the hblank is less than or equal to 80pixels, then a value of 12 should be used. For 4:2:0 mode if the hblank is less than 40, then a value of 3 should be used. For dual and quad pixel modes a value of 64 should be used. In all other cases the default value of 16 is sufficient. The link has a 32 bit data path and the 16 clocks is to wait for TU size clocks which is 16*4 = 64 (TU size) symbols. For DSC Mode: INIT_THRESHOLD = pixel_push_rate * link_pixel_clock_ratio * slot_count where Pixel Push rate = (8/bpp)*lane_count. slot_count for sst =average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled) slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. slot_count for mst = (32/lane_count) + average_bytes_per_tu + FEC symbols inserted per lane(13 in 1-lane and 7 in 2/4lane if fec is enabled, 0 if fec is disabled). Slot count is rounded to nearest multiples of 4(ceiling). If slot count calculated is greater than 64, then slot count is fixed to 64. bpp = PPS.bits_per_pixel in simple modes and PPS.bits_per_pixel/2 in native modes link_pixel_clock_ratio = link clock frequency in Mhz/ pixel clock frequency in Mhz.

Bit	Attr	Reset Value	Description
6:0	RW	0x16	AVERAGE_BYTES_PER_TU This is the average number of valid bytes in a transfer Unit. Driver should program this register based on the video format being transmitted and the link rate and lane configuration being used. Section 2.2.1.4 of the DP 1.43 spec give details on how this average symbol count should be calculated. In MST mode, this register is programmed with the calculated TS_INT as specified in Section 2.6.4.3 of DisplayPort 1.4 Spec. In MST mode, The driver programs the avarege_bytes_per_tu using the following equation. Average_bytes_per_tu= floor((Peak_stream_bandiwth/Link_bandwidth*64) Here is an example for calculating the Average_bytes_per_tu in MST mode for the video format VIC-1 (640x480) RGB, 8bpc, at a frame rate of 60Hz. The Link is assumed to be HBR 4 lanes. Peak_stream_bandwidth = Pixel_clock_frequency*bytes_per_pixel = 25.175*3 = 75.52MBps Link Bandwidth = link_rate * 100 * number_of_lanes .= 2.7 * 100 *4 = 1080MBps Average_bytes_per_tu = floor((peak_stream_bandwidth/link_bandwidth)*64) = floor((75.52/1080)*64)) = floor(4.475) = 4.

DPTX_VIDEO_MSA1

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RW	0x0023	VSTART Vertical start from the leading edge of Vsync, measured in line count. This is the vstart value that is specified in the MSA.This is same as vsync width + Vertical back porch.
15:0	RW	0x0090	HSTART Horizontal active start from leading edge of Hsync, measured in pixel count. This is the hstart value that is specified in the MSA. This is same as hsync width + Horizontal back porch.

DPTX_VIDEO_MSA2

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC0 Bit 24: Synchronous mode of operation. Pixel source reference clock and link reference clock are the same. 1'b0: Asynchronous mode 1'b1: Synchronous mode Bits 31:25: Colorimetry indicator field.
23:0	RW	0x000000	MVID MVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value

DPTX_VIDEO_MSA3

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	MISC1 24-Interlaced Vertical Total Even 26:25 Stereo Video Attribute 31:30-Pixel Encoding/colorimetry Format indicator field
23:0	RW	0x000000	NVID NVID value to be used in case of synchronous mode of operation (pixel source reference clock and link reference clock are the same). See section 2.2.3 of the DisplayPort 1.3 spec. This value goes in the MSA. If the clocks are asynchronous, controller internally calculates this value.

DPTX_VIDEO_HBLANK_INTERVAL

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	HBLANK_INTERVAL For MST mode the programmed value should be (Hblank/16 *average_bytes_per_tu*link_clk/pixel_clk. Link_clk and pixel_clk are in Mhz. The link clock is based on the internal 32 bit datapath. In SST mode, it should be hblank *link_clk/pixel_lk.

DPTX_AUD_CONFIG1

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x12	AUDIO_TIMESTAMP_VERSION_ Audio timestamp version number.This is used as HB3[7:2] of Audio Timestamp SDP. As per DP 1.3 Spec, this should be h'12. Some compliance testers still look for old values, and therefore added this register field.
23:16	RW	0x00	AUDIO_PACKET_ID Defines the first byte of the audio SDP and the audio time stamp SDP header. Used for associating the audio sdp to the timestamp with multiple audio streams.
15	RW	0x0	AUDIO_MUTE Controls the AudioMute_Flag in the VB-ID. 1'b1: Sets the AudioMute_Flag in VB-ID 1'b0: Clears the AudioMute_Flag in VB-ID.
14:12	RW	0x1	NUM_CHANNELS Number of audio channels 1'b0: 1channel 1'b1: 2channels others: 8channels.
11	RO	0x0	reserved
10	RW	0x0	HBR_MODE_ENABLE Audio input is operating in HBR mode if set to '1'. When audio_if_select is 1 (S/PDIF), 768kHz x 2 Channels x 16 bits is delivered to controller. When '0' (I2s) 192kHz x 8 x 16 bits in 8-channel is delivered to controller.

Bit	Attr	Reset Value	Description
9:5	RW	0x10	AUDIO_DATA_WIDTH Audio input data width audio_data_width4:0 Action 5'b00000-5'b01111: Not used 5'b10000: 16 bit data samples at input 5'b10001: 17 bit data samples at input 5'b10010: 18 bit data samples at input 5'b10011: 19 bit data samples at input 5'b10100: 20 bit data samples at input 5'b10101: 21 bit data samples at input 5'b10110: 22 bit data samples at input 5'b10111: 23 bit data samples at input 5'b11000: 24 bit data samples at input 5'b11001-5'b11111: Not Used
4:1	RW	0x1	AUDIO_DATA_IN_EN Specifies which of the audio data inputs are active. Used to control I2sSPDIF input data. audio_data_in_en0 and ispdfidata0i2sdata_i0 enabled indicates channels12 is active audio_data_in_en1, ispdfidata1, and i2sdata_i1 enabled indicates channels3 and channels4 are active. audio_data_in_en2, ispdfidata2, and i2sdata_i2 enabled indicates channels5 and channels6 are active. audio_data_in_en3, ispdfidata3, and i2sdata_i3 enabled indicates that channels7 and channels8 are active. Value of 0 is invalid.
0	RW	0x0	AUDIO_INF_SELECT 1'b0: I2S is the selected audio input interface (Default). 1'b1: SPDIF is the selected audio input interface.

DPTX_SDP_VERTICAL_CTRL

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATIO When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30	RW	0x0	DISABLE_EXT_SDP When set the external SDP interface is disabled. No external SDPs are transmitted. This bit is applicable for both the vertical and horizontal blanking.
29:25	RO	0x00	reserved
24	RW	0x0	EN_128BYTES_SDP_1 When set, register bank 1, 2, 3 and 4 are used to form a 128bytes SDP. The SW should program a single 4bytes header followed by 128bytes of data and set a single enable bit that corresponds to bank 1.
23:20	RO	0x0	reserved
19:2	RW	0x00000	EN_VERTICAL_SDP_N When set, DPTX sends out SDP during the vertical intervals, using the information provided in the SDP_REGISTER BANK[n*9-1: n*9]

Bit	Attr	Reset Value	Description
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during the vertical blanking period. When '1' audio stream is transmitted during vertical blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DPTX sends out audio timestamp SDP once every video frame during the vertical blanking period. This SDP is always transmitted as the first SDP in the blanking period. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_HORIZONTAL_CTRL
Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31	RW	0x0	FIXED_PRIORITY_ARBITRATION When this bit is set then the scheduler searches for the next SDP to transmit based on fixed priority, otherwise it uses Round-Robin arbitration. Fixed priority means that lower numbered register sets has higher priority than higher numbered register sets.
30:20	RO	0x000	reserved
19:2	RW	0x00000	EN_HORIZONTAL_SDP_N When set, DPTX sends out SDP during the horizontal intervals, using the information provided in the SDP_REGISTER BANK[n*9-1: n*9]
1	RW	0x0	EN_AUDIO_STREAM_SDP When cleared, no Audio stream is sent during horizontal blanking. When '1' audio stream is transmitted during horizontal blanking period.
0	RW	0x0	EN_AUDIO_TIMESTAMP_SDP When set, DPTX sends out audio timestamp SDP once every horizontal blanking. Payload for the audio timestamp SDP and the header are internally generated by the controller.

DPTX_SDP_STATUS_REGISTER
Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	W1C	0x00000	SDP_N_TX_STATUS Status indicating the transmission of corresponding Nth SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
1	W1C	0x0	AUDIO_STREAM_SDP_STATUS Status indicating the transmission of an audio SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.
0	W1C	0x0	AUDIO_TIMESTAMP_SDP_STAT Status indicating the transmission of an audio timestamp SDP. Set to 1 by the hardware in both Auto and Manual modes. Software writes a 1 to clear this bit.

DPTX_SDP_MANUAL_CTRL
Address: Operational Base + offset (0x050C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	MANUAL_MODE_SDP Setting this bit when the corresponding bit in the SDP_VERTICAL_CTRL/SDP_HORIZONTAL_CTRL registers causes the corresponding SDP to be transmitted once. After the transmission, both corresponding enable bits are reset. If the transmission done during the Vertical or the Horizontal blanking period then the enable bit in both the SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers are reset. This provides the Software the ability to decide whether an SDP is transmitted once during the Vertical period, or Horizontal period or whichever comes first.

DPTX_SDP_STATUS_EN
Address: Operational Base + offset (0x0510)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:2	RW	0x00000	SDP_STATUS_EN Setting this bit to 1 enables interrupt generation due to transmission of the corresponding SDP
1	RW	0x0	AUDIO_STREAM_SDP_STATUS Setting this bit to 1 enables interrupt generation due to transmission of an audio SPD
0	RW	0x0	AUDIO_TIMESTAMP_SDP_STAT Setting this bit to 1 enables interrupt generation due to transmission of a audio timestamp SPD

DPTX_SDP_REGISTER_BANK
Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SDP_REGS The register bank is split to SDPs where each SDP is the size of nine 32bits registers. The first register contains the SDP header and the other eight the data payload. For example, if DPTX_NUM_SDP_REGISTER_BANKS is 10, then 90 32bits registers are defined. The register set [8:0] specifies s SDP which is transmitted if the corresponding bit in SDP_AUTOEN_CTRL is set, whether the corresponding bit located at [2]. The next SDP, registers[17:9] are enabled by bit [3] in SDP_AUTOEN_CTRL.

DPTX_PHYIF_CTRL
Address: Operational Base + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:26	RW	0x0	EDP_PHY_RATE Support for the eDP rates. 3'b000: PHY rates as defined by bits 5:4 of this register (PHYRATE) are used. 3'b001: R216(2.16Gbps) 3'b010: R243(2.43Gbps) 3'b011: R324(3.24Gbps) 3'b100: R432(4.32Gbps)

Bit	Attr	Reset Value	Description
25	RW	0x0	PHY_WIDTH This bit is used to configure the data width of the main link interface to the PHY. 1'b0: 20-bit interface 1'b1: 40-bit interface The power-on reset value of this bit can be configured by parameter.
24:21	RO	0x0	reserved
20:17	RW	0x3	PHY_POWERDOWN PHY power-down control. The value written in this field controls the Powerdown on all the lanes. 4'h0: Powered on 4'h2: Intermediate P2 power state for switching rates. 4'h3: PHY is powered down phy_clk might stop 4'hC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved.
16	RW	0x0	SSC_DIS Disable SSC on the PHY.
15:12	RW	0x0	PHY_BUSY Status from the PHY per lane: Bit 12: Lane 0 Bit 13: Lane 1 Bit 14: Lane 2 Bit 15: Lane 3 This bit for each lane is set when a power state change or rate change is requested and cleared when the PHY sends a phy_laneX_phystatus pulse. This bit is also be set when phy_reset is asserted and cleared when phy_laneX_phystatus drops to 0 after reset finishes. No changes to PHY_RATE or PHY_POWERDOWN are to occur when PHY_BUSY is high. PHY_BUSY only go high in response to PHY_RATE PHY_POWERDOWN or a reset. PHY_BUSY must go high if phy_laneX_phystatus is set. The time between when this signal asserts till deassertion is specific to PHY implementation. Software can implement a timeout that is appropriate to the PHY. Generally, this is 100ms.
11:8	RW	0x0	XMIT_ENABLE Enable transmitter on the PHY per lane. If TPS_SEL is 0 then main link provides the data to be transmitted. If PHY_POWERDOWN is not 0 then the transmitter is not enabled on the PHY interface. Bit 8: Lane 0 Bit 9: Lane 1 Bit 10: Lane 2 Bit 11: Lane 3
7:6	RW	0x0	PHY_LANES Number of lanes active: 2'b00: 1 Lane 2'b01: 2 Lanes 2'b10: 4 Lanes

Bit	Attr	Reset Value	Description
5:4	RW	0x0	PHYRATE Rate setting for the PHY. If the Synopsys Combo PHY is used, the software must first program PHY_POWERDOWN to 2 or 3 first and waiting for PHYBUSY to clear. Afterwards, rate can be changed along with PHY_POWERDOWN. 2'b00: RBR 1.62 Gbs 2'b01: HBR 2.7 Gbs 2'b10: HBR2 5.4 Gbs 2'b11: HBR3 8.1 Gbs
3:0	RW	0x0	TPS_SEL Selects the training pattern to be transmitted to the PHY: 4'h0: No training pattern is transmitted. Main link data is transmitted instead. 4'h1: TPS1, D10.2 4'h2: TPS2 4'h3: TPS3 4'h4: TPS4, CP2520 Pattern 3 4'h5: Symbol Error Rate Measurement pattern 4'h6: PRBS7 4'h7: Custom 80-bit pattern. CUSTOMPAT0, CUSTOMPAT1, and CUSTOMPAT2 must be set to a valid pattern before this select is programmed 4'h8: CP2520 Pattern 1 - As defined by PHY CTS 1.2b 4'h9: CP2520 Pattern 2- - As defined by

DPTX_PHY_TX_EQ

Address: Operational Base + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	LANE3_TX_POST_CUR2 Lane 3 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2
21:20	RW	0x0	LANE3_TX_VSWING Lane 3 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
19:18	RW	0x0	LANE3_TX_PREEMP Lane 3 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
17:16	RW	0x0	LANE2_TX_POST_CUR2 Lane 2 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2

Bit	Attr	Reset Value	Description
15:14	RW	0x0	LANE2_TX_VSWING Lane 2 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	LANE2_TX_PREEMP Lane 2 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	LANE1_TX_POST_CUR2 Lane 1 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b10: Level 1 2'b10: Level 2
9:8	RW	0x0	LANE1_TX_VSWING Lane 1 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	LANE1_TX_PREEMP Lane 1 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	LANE0_TX_POST_CUR2 Lane 0 Pre-emphasis Post Cursor2 Level. Controls the phy_lane0_tx_post_cur21:0 output. 2'b00: Level 0 2'b10: Level 1 2'b10: Level 2
3:2	RW	0x0	LANE0_TX_VSWING Lane 0 Voltage Swing Level. Controls the phy_lane0_tx_vswing1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	LANE0_TX_PREEMP Lane 0 Pre-emphasis Level. Directly controls the phy_lane0_tx_pre_emp1:0 output. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

DPTX_CUSTOMPAT0

Address: Operational Base + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	CUSTOM80B_0 Lower 30-bits of the 80-bit pattern. This corresponds to 29:0 of the 80-bit pattern. Note: All 80-bits of CUSTOMPAT0 CUSTOMPAT1 and CUSTOMPAT2 must be programmed. The symbol at 9:0 is transmitted first.

DPTX_CUSTOMPAT1

Address: Operational Base + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	CUSTOM80B_1 Next 30-bits of the 80-bit pattern. This corresponds to 59:30 of the 80-bit pattern. Note: All 80-bits of CUSTOMPAT0 CUSTOMPAT1 and CUSTOMPAT2 must be programmed.

DPTX_CUSTOMPAT2

Address: Operational Base + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	CUSTOM80B_2 Highest 20-bits of the 80-bit pattern. This corresponds to 79:60 of the 80-bit pattern. Note: All 80-bits of CUSTOMPAT0 CUSTOMPAT1 and CUSTOMPAT2 must be programmed.

DPTX_HBR2_COMPLIANCE_SCRAMBLER_RESET

Address: Operational Base + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x00fc	NUM_SR_ZEROS Number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence SR-BF-BFSR when CP2520 Pattern 1, 2, or 3 is transmitted. Count includes the reset sequence. Value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence. Default value is required for PHY CTS is 16'd252 = SR sequence 4 + 248 zeros

DPTX_PHYIF_PWRDOWN_CTRL

Address: Operational Base + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	PER_LANE_PWRDOWN_CTL_E Per lane power-down control enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	POWER_DOWN_CTRL_LANE3 PowerDown control for Lane-3. 4’h0: Powered on 4’h2: Intermediate P2 power state for switching rates. 4’h3: PHY is powered down phy_clk might stop 4’hC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved
11:8	RW	0x0	POWER_DOWN_CTRL_LANE2 PowerDown control for Lane-2. 4’h0: Powered on 4’h2: Intermediate P2 power state for switching rates. 4’h3: PHY is powered down phy_clk might stop 4’hC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved
7:4	RW	0x0	POWER_DOWN_CTRL_LANE1 PowerDown control for Lane-1. 4’h0: Powered on 4’h2: Intermediate P2 power state for switching rates. 4’h3: PHY is powered down phy_clk might stop 4’hC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved
3:0	RW	0x0	POWER_DOWN_CTRL_LANE0 PowerDown control for Lane-0. 4’h0: Powered on 4’h2: Intermediate P2 power state for switching rates. 4’h3: PHY is powered down phy_clk might stop 4’hC: P4 Power state. PHY is powered down, reference clock can be stopped. Others: Reserved

DPTX_AUX_CMD

Address: Operational Base + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	AUX_CMD_TYPE AUX Channel Command: 4'b1000: Native Write 4'b1001: Native Read 4'b0100: I2C MOT Write 4'b0101: I2C MOT Read 4'b0000: I2C Write 4'b0001: I2C Read 4'b0010: I2C Write Status update 4'b0110: I2C MOT Write Status update All other values are reserved and triggers an interrupt, INTERRUPTS.AUX_CMD_INVALID
27:8	RW	0x00000	AUX_ADDR AUX Address
7:5	RO	0x0	reserved
4	RW	0x0	I2C_ADDR_ONLY A value of '1' indicates an I2C over aux address only transfer.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	AUX_LEN_REQ AUX Length Number of bytes to transmit. 0-15 indicating between 1 to 16 bytes of data. A value of '0' should be programmed for an I2C over aux address only

DPTX_AUX_STATUS

Address: Operational Base + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	AUX_STATE Reflects the current state of the AUX state machine. Used for hardware debug only.
27:25	RO	0x0	AUX_REPLY_ERR_CODE Error code. Valid when sink aux reply error is detected. Used for hardware debug purpose only.
24	RW	0x0	SINK_DISCONNECT_WHILE_AC The bit is set to 1 if the SINK disconnect was detected while active AUX transfer
23:19	RO	0x00	AUX_BYTES_READ The number of valid bytes received as a reply from the SINK
18	RW	0x0	AUX_REPLY_ERR The bit is set to 1 if a reply error is detected. An error could be an illegal Manchester code, or if the source and sink are out of sync. The specific error code is in bits 27:25 of this register.
17	RO	0x0	AUX_TIMEOUT The bit is set to 1 if no reply is received within 400us after a request has been sent on the AUX channel.
16	RO	0x0	AUX_REPLY_RECEIVED If '1' then Indicates an active AUX transfer. When '0' indicates that an AUX_REPLY has been received and the AUX status/data registers are valid. Note: If the AUX transfer was not successful such that the AUX transfer timed out or an error detected then the Status & Data registers might not have valid values.
15:8	RO	0x00	AUX_M The second byte received from the Sink as a reply to an AUX transfer. This value is the number of bytes written.
7:0	RO	0x00	AUX_STATUS The first byte received from the Sink as a reply to an AUX transfer. The higher 4-bits are the actual reply: 4'b0000: AUX/I2C ACK 4'b0001: AUX NACK 4'b0010: AUX Defer 4'b0100: I2C NACK 4'b1000: I2C DEFER

DPTX_AUX_DATA0

Address: Operational Base + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUX_DATA0 AUX Data - First 4 bytes. If only 1 byte is to be written in the transaction, then only 3:0 has valid data

DPTX_AUX_DATA1

Address: Operational Base + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUX_DATA1 AUX Data Second 4 bytes

DPTX_AUX_DATA2
Address: Operational Base + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUX_DATA2 AUX Data Third 4 bytes

DPTX_AUX_DATA3
Address: Operational Base + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	AUX_DATA3 AUX Data Fourth 4 bytes

DPTX_PHYREG_CMDADDR
Address: Operational Base + offset (0x0C00)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHY_READ Initiate the read into the PHY register. This bit self-clears when the read completes and PHYREG_DATA contains valid read data.
30	RW	0x0	PHY_WRITE Initiate the write into the PHY register. This bit self-clears when the write completes in the hardware.
29:16	RO	0x0000	reserved
15:0	RW	0x0000	PHY_ADDRESS Address bus for the PHY register interface

DPTX_PHYREG_DATA
Address: Operational Base + offset (0x0C04)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHY_DONE Indicates that the data is ready to be read from the PHYREG_DATA register if a read was initiated or that a write was completed
30:16	RO	0x0000	reserved
15:0	RW	0x0000	PHY_DATA Address bus for the PHY register interface

DPTX_TYPEC_CTRL
Address: Operational Base + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	TYPEC_INTERRUPT_STATUS This is the interrupt status pin for TYPE-C. On a type-C interrupt software reads this register to confirm a Type-C interrupt. Writing 1 by the software clears the TYPE-C interrupt.
1	RO	0x0	TYPEC_DISABLE_STATUS This is a read only register bit which directly reflects the status of the primary input pin tca_disable_i. After receiving a TYPE_C interrupt, software reads this register bit to get the status of the tca_disable.

Bit	Attr	Reset Value	Description
0	RW	0x0	TYPEC_DISABLE_ACK This register bit controls the primary output pin tca_disable_ack_o. The value in this register is directly reflected on the output. Software sets or clears this bit based on the Type-C interrupt.

DPTX_GENERAL_INTERRUPT

Address: Operational Base + offset (0x0D00)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	DSC_EVENT An DSC event has occurred. Please read DSC register DSCINTSTAT to see the cause of the event. To reset the bit software need to clear the status at the source, in the DSCINTSTAT by writing to DSCINTSTAT register
29:27	RO	0x0	reserved
26	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM3 Indicates that the video lane steering FIFO for stream2 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream2. This bit is used for debug only
25	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM3 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream3. This is an vindication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream3.
24	RW	0x0	SDP_EVENT_STREAM3 An event indicating the completion of transmission of an SDP for stream3. For details on the specific SDPs that got transmitted refer to SDP Status register for stream3. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream3.
23:21	RO	0x0	reserved
20	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM2 Indicates that the video lane steering FIFO for stream2 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream2. This bit is used for debug only
19	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM2 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream2. This is an indication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream2.
18	RO	0x0	SDP_EVENT_STREAM2 An event indicating the completion of transmission of an SDP for stream2. For details on the specific SDPs that got transmitted refer to SDP Status register for stream2. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream2.
17:15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM1 Indicates that the video lane steering FIFO for stream1 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream1. This bit is used for debug only
13	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM1 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream1. This is an indication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream1.
12	RO	0x0	SDP_EVENT_STREAM1 An event indicating the completion of transmission of an SDP for stream1. For details on the specific SDPs that got transmitted refer to SDP Status register for stream1. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream1.
11:8	RO	0x0	reserved
7	RO	0x0	TYPE_C_EVENT Indicates an event related to Type-C assit block. This could be an indication that the Type-C assit input pin tca_disable has changed. Read TYPE-C_CTRL register for more details.To reset this bit software need to clear the status in TYPEC_CTRL register by writing 1 to TYPEC_INTERRUPT_STATUS bit.
6	W1C	0x0	VIDEO_FIFO_OVERFLOW_STREAM0 Indicates that the video lane steering FIFO for stream0 gets an overflow. The likely cause is that the bytes_per TU programmed in the VIDEO_CONFIG5.AVERAGE_BYTES_PER_TU is wrong or the lane/rate chosen for the video format is not correct for stream0. This bit is used for debug only
5	RW	0x0	AUDIO_FIFO_OVERFLOW_STREAM0 Indicates that one or more of the audio sampler FIFOs are getting into overflow condition for stream0. This is an indication that the audio samples are not getting drained out and is an indication that the bandwidth of the selected audio does not match with the video format being used for stream0.
4	RO	0x0	SDP_EVENT_STREAM0 An event indicating the completion of transmission of an SDP for stream0. For details on the specific SDPs that got transmitted refer to SDP Status register for stream0. To reset the bit the SW needs to clear the status at the source, in the SDP status register for stream0.
3	W1C	0x0	AUX_CMD_INVALID After initiating an AUX request, this bit is set to 1, if the command or length was invalid. The AUX request is not sent out on the AUX Channel if this bit is set
2	RO	0x0	HDCP_EVENT An HDCP event has occurred. Please read HDCP register HDCPAPIINTSTAT to see the cause of the event. To reset the bit software needs to clear the status at the source, in the HDCPAPIINTSTAT by writing to HDCPAPIINTCLR register.
1	W1C	0x0	AUX_REPLY_EVENT After initiating an AUX request this bit is set to 1 after receiving a reply.

Bit	Attr	Reset Value	Description
0	RO	0x0	HPD_EVENT This bit indicates that an HPD event is captured in the HPD status register. To reset the bit the SW needs to clear the status at the source in the HPD status register.

DPTX_GENERAL_INTERRUPT_ENABLE

Address: Operational Base + offset (0x0D04)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	DSC_EVENT_EN Enable for DSC event. Set to 1 to enable events related to DSC.
29:27	RO	0x0	reserved
26	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM3 Enable for VIDEO_FIFO_OVERFLOW for stream3. Set 1 to mask this event.
25	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM3 Enable for AUDIO_FIFO_OVERFLOW for stream23. Set 1 to enable this event.
24	RW	0x0	SDP_EVENT_EN_STREAM3 Global enable for SDP event for stream3. Set 1 to enable the SDP event.
23:21	RO	0x0	reserved
20	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM2 Enable for VIDEO_FIFO_OVERFLOW for stream2. Set 1 to mask this event.
19	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM2 Enable for AUDIO_FIFO_OVERFLOW for stream2. Set 1 to enable this event.
18	RW	0x0	SDP_EVENT_EN_STREAM2 Global enable for SDP event for stream2. Set 1 to enable the SDP event.
17:15	RO	0x0	reserved
14	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM1 Enable for VIDEO_FIFO_OVERFLOW for stream1. Set 1 to mask this event.
13	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM1 Enable for AUDIO_FIFO_OVERFLOW for stream1. Set 1 to enable this event.
12	RW	0x0	SDP_EVENT_EN_STREAM1 Global enable for SDP event for stream1. Set 1 to enable the SDP event.
11:8	RO	0x0	reserved
7	RW	0x0	TYPE_C_EVENT_EN Enable for TYPE_C_EVENT Set to 1 to enable this event.
6	RW	0x0	VIDEO_FIFO_OVERFLOW_EN_STREAM0 Enable for VIDEO_FIFO_OVERFLOW for stream0. Set 1 to mask this event.
5	RW	0x0	AUDIO_FIFO_OVERFLOW_EN_STREAM0 Enable for AUDIO_FIFO_OVERFLOW for stream0. Set 1 to enable this event.
4	RW	0x0	SDP_EVENT_EN_STREAM0 Global enable for SDP event for stream0. Set 1 to enable the SDP event.

Bit	Attr	Reset Value	Description
3	RW	0x0	AUX_CMD_INVALID_EN Enable for AUX_CMD_INVALID. Set to 1 to enable this event.
2	RW	0x0	HDCP_EVENT_EN Enable for HDCP event. Set to 1 to enable events related to HDCP.
1	RW	0x0	AUX_REPLY_EVENT_EN Enable for Set to 1 to enable this event.
0	RW	0x0	HPD_EVENT_EN Enable for HPD_EVENT. Set to 1 to enable this event.

DPTX_HPD_STATUS

Address: Operational Base + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	HPD_TIMER This field is the raw HPD timer value. Resets to 0 whenever HPD toggles and starts counting afterwards. If no other event occurs this timer increments until a plug/unplug event is detected. The unit of measure is in microseconds. This value is used for debugging.
11:9	RO	0x0	HPD_STATE The HPD state machine state. Used for debug but SW can also use the info to determine the status after receiving an interrupt. SOURCE_STATE_IDLE= 3'd0 Sink is not connected SOURCE_STATE_UNPLUG= 3'd1 HPD gets deasserted after being in the plugged state. In this state for 2mSec. SOURCE_STATE_HPD_TIMEOUT= 3'd4 The HPD is deasserted for more than 2mSec but less than 100mSec SOURCE_STATE_PLUG = 3'd7 HPD is high, the Sink is connected
8	RO	0x0	HPD_STATUS Current status of the HPD input. This value must be qualified with the HPD_TIMER.
7:4	RO	0x0	reserved
3	W1C	0x0	HPD_UNPLUG_ERR Unplug detected. This bit is set to 1 after the HPD is deasserted for less than 250uSec.
2	W1C	0x0	HPD_HOT_UNPLUG Unplug detected. This bit is set to 1 after the HPD is deasserted for at least 2mSec.
1	W1C	0x0	HPD_HOT_PLUG Hot plug detected. This bit is asserted after the sink is plugged and asserts HPD for at least 100mSec. It is also asserted If the sink was plugged then deasserts HPD for more than 2mSec but less than 100mSec. In this case this bit is set as soon as HPD is asserted by the sink. No debounce time is implemented.
0	W1C	0x0	HPD_IRQ IRQ from the HPD. This bit is set to 1 after a low pulse on HPD has been detected between 0.25-2.0 ms

DPTX_HPD_INTERRUPT_ENABLE

Address: Operational Base + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	HPD_UNPLUG_ERR_EN Enable for HPD_UNPLUG_ERR. Setting to 1 enables this event to assert the interrupt output.
2	RW	0x0	HPD_UNPLUG_EN Enable for HPD_UNPLUG. Setting to 1 enables this event to assert the interrupt output.
1	RW	0x0	HPD_PLUG_EN Enable for HPD_PLUG. Setting to 1 enables this event to assert the interrupt output.
0	RW	0x0	HPD_IRQ_EN Enable for IRQ_HPD. Setting to 1 enables this event to assert the interrupt output.

DPTX_HDCPCFG
Address: Operational Base + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	DPCD12PLUS DPCD revision of Sink is 1.2 or higher. Updated by software after reading the DPCD revision
6	RW	0x0	CP_IRQ CP_IRQ indication to HDCP controller. Software sets this bit on CP_IRQ interrupt
5	RW	0x0	BYPENCRYPTION Bypasses all the data encryption stages.
4	RW	0x0	HDCP_LOCK Lock the HDCP bypass and encryption disable mechanisms: 1b0: The default 1b0 value enables you to bypass HDCP through bit 5 by encryption of the HDCPCFG register or to disable the encryption through bit 3 encryption disable of HDCPCFG register. 1b1: You can still write to the bit by encryption of HDCPCFG or encryption disable bit of HDCPCFG but you cannot enable the bypass or disable encryption. Once you set the value to 1b1 you can change the value back to 1b0 only by issuing a master reset to the DPTX.
3	RW	0x0	ENCRYPTIONDISABLE Disable encryption without losing authentication
2	RW	0x0	ENABLE_HDCP_13 1'b0: Default HDCP 2.2 is enabled 1'b1: HDCP 1.3 is enabled
1	RW	0x0	ENABLE_HDCP Enable HDCP functionality. This signal is tied to I_px_gpio_in[0] of HDCP2.2 Controller clears this bit under the following condition Re-authentication request from the sink.
0	RO	0x0	reserved

DPTX_HDCPOBS
Address: Operational Base + offset (0x0E04)

Bit	Attr	Reset Value	Description
31	W1C	0x0	HDCP22_RE_AUTHENTICATION_REQ Indicates that the Sink has requested a re-authentication. Cleared when software writes a 1 to this bit.

Bit	Attr	Reset Value	Description
30	W1C	0x0	HDCP22_AUTHENTICATION_FAILED Set to 1 when by the hardware when the authentication is failed. Cleared when software writes a 1.
29	W1C	0x0	HDCP22_AUTHENTICATION_SUCCESS Set to 1 when by the hardware when the authentication is succeeded. Cleared when software writes a 1.
28	RO	0x0	HDCP22_CAPABLE_SINK 1'b1: HDCP 22 sink 1'b0: Sink not HDCP22 capable. If enable_hdcp_13 is set and this bit is already set then controller clears it. Re-authentication request also clears this bit.
27	W1C	0x0	HDCP22_SINK_CAP_CHECK_C Sets when the capability check is complete. Cleared when software writes a 1 to this bit.
26:24	RO	0x0	HDCP22_STATE Status of HDCP operation 3'B001: Initializing 3'B010: Authenticating 3'B011: Authenticated 3'B100: not Authenticated
23	W1C	0x0	HDCP22_BOOTED Status indicting the HDCP22 has booted. Cleared when software writes a 1 to this bit.
22:19	RO	0x0	HDCP13_BSTATUS Status indicting the HDCP22 has booted. Cleared when software writes a 1 to this bit.
18	RO	0x0	REPEATER Register read from attached sink device: Bcap bit 1
17	RO	0x0	HDCP_CAPABLE Register read from attached sink device: Bcap bit 0
16:14	RO	0x0	STATEE Observability register informs in which state the cipher machine is on.
13:11	RO	0x0	STATEOEG Observability register informs in which state the DPES machine is on.
10:8	RO	0x0	STATER Observability register informs in which state the revocation machine is on.
7:4	RO	0x0	STATEA Observability register informs in which state the authentication machine is on.
3:1	RO	0x0	SUBSTATEA Observability register informs in which sub-state the authentication is on
0	RO	0x0	HDCPENGAGED Informs that the current DP link has the HDCP protocol fully engaged.

DPTX_HDCPAPIINTCLR

Address: Operational Base + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	WO	0x0	HDCP22_GPIOINT Clears the interruption related to HDCP22 GPIO output status change.
7	WO	0x0	HDCP_ENGAGED Clears the interruption related to HDCP authentication process successful.
6	WO	0x0	HDCP_FAILED Clears the interruption related to HDCP authentication process failed.
5	WO	0x0	KSVSHA1CALCDONEINT Clears the interruption related to SHA1 verification has been done.
4	WO	0x0	AUXRESPNACK7TIMES Clears the interrupt related to aux transfer NAK response for 7 times.
3	WO	0x0	AUXRESPTIMEOUT Clears the interrupt related to aux transfer response timeout.
2	WO	0x0	AUXRESPDEFER7TIMES Clears the interrupt related to aux transfer defer response for 7 times.
1	RO	0x0	reserved
0	WO	0x0	KSVACCESSINT Clears the interrupt related to KSV memory access grant for Read-Write access.

DPTX_HDCPAPIINTSTAT
Address: Operational Base + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	HDCP22_GPIOINT Notifies a change in HDCP22 GPIO Output status.
7	RO	0x0	HDCP_ENGAGED Notifies that the HDCP authentication process was successful.
6	RO	0x0	HDCP_FAILED Notifies that the HDCP authentication process was failed.
5	RO	0x0	KSVSHA1CALCDONEINT Notifies that the HDCP13TCTRL controller SHA1 verification has been done. The status ready to be read.
4	RO	0x0	AUXRESPNACK7TIMES Notifies that the aux transfer initiated by HDCP13TCTRL received nack response continuously for 7 times.
3	RO	0x0	AUXRESPTIMEOUT Notifies that the aux transfer initiated by HDCP13TCTRL did not receive a response and timeout.
2	RO	0x0	AUXRESPDEFER7TIMES Notifies that the aux transfer initiated by HDCP13TCTRL received defer response continuously for 7 times
1	RO	0x0	reserved
0	RO	0x0	KSVACCESSINT Notifies that the KSV memory access has been guaranteed for Read-Write access.

DPTX_HDCPAPIINTMSK
Address: Operational Base + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	HDCP22_GPIOINT Masks the interruption related to HDCP22 GPIO output status change.
7	RW	0x0	HDCP_ENGAGED Masks the interruption related to HDCP authentication process successful.
6	RW	0x0	HDCP_FAILED Masks the interruption related to HDCP authentication process failed.
5	RW	0x0	KSVSHA1CALCDONEINT Masks the interruption related to SHA1 verification has been done.
4	RW	0x0	AUXRESPNACK7TIMES Masks the interrupt related to aux transfer nack response for 7 times.
3	RW	0x0	AUXRESPTIMEOUT Masks the interrupt related to aux transfer defer response for 7 times.
2	RW	0x0	AUXRESPDEFER7TIMES Masks the interrupt related to aux transfer defer response for 7 times.
1	RO	0x0	reserved
0	RW	0x0	KSVACCESSINT Masks the interrupt related to KSV memory access grant for Read-Write access.

DPTX_HDCPKSVMEMCTRL

Address: Operational Base + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	KSVSHA1STATUS Notification whether the KSV list message digest is correct from the controller: 1b1: if digest message verification failed 1b0: if digest message verification succeeded.
3:2	RO	0x0	reserved
1	RO	0x0	KSVMEMACCESS Notification that the KSV memory access has been guaranteed.
0	RW	0x0	KSVMEMREQUEST Request access to the KSV memory; must be de-asserted after the access is completed by the system.

DPTX_HDCP_REVOC_RAM_i

Address: Operational Base + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	REVOC_RAM_BYTE3 Byte 3 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff
23:16	RW	0xff	REVOC_RAM_BYTE2 Byte 2 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff
15:8	RW	0xff	REVOC_RAM_BYTE1 Byte 1 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff

Bit	Attr	Reset Value	Description
7:0	RW	0xff	REVOC_RAM_BYTE0 Byte 0 of HDCP revocation ram dword If memory access has not been granted (see register a_ksvmemctrl) the value read is 8hff

DPTX_HDCPREG_BKSV0
Address: Operational Base + offset (0x3600)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HDCPREG_BKSV0 Contains the value of BKSV[31:0].

DPTX_HDCPREG_BKSV1
Address: Operational Base + offset (0x3604)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	HDCPREG_BKSV1 Contains the value of BKSV[39:32].

DPTX_HDCPREG_ANCONF
Address: Operational Base + offset (0x3608)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	OANBYPASS 1'b1: The value of AN used in the HDCP engine comes from the hdcpreg_an0 to hdcpreg_an7 registers. 1'b0: The value of AN used in the HDCP engine comes from the random number input.

DPTX_HDCPREG_AN0
Address: Operational Base + offset (0x360C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCPREG_AN0 Contains the value of AN[31:0]

DPTX_HDCPREG_AN1
Address: Operational Base + offset (0x3610)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCPREG_AN1 Contains the value of AN[63:32]

DPTX_HDCPREG_RMLCTL
Address: Operational Base + offset (0x3614)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ODPK_DECRYPT_ENABLE When set 1b1 this bit activates the decryption of the Device Private keys.

DPTX_HDCPREG_RMLSTS
Address: Operational Base + offset (0x3618)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	IDPK_WR_OK_STS When high 1b1 it indicates that a DPK write is allowed.

Bit	Attr	Reset Value	Description
5:0	RO	0x00	IDPK_DATA_INDEX Current Device Private Key being written plus one. Position 0 is occupied by the AKSV.

DPTX_HDCPREG_SEED

Address: Operational Base + offset (0x361C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	HDCPREG_SEED Decryption seed value

DPTX_HDCPREG_DPK0

Address: Operational Base + offset (0x3620)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	DPK_DATA Encrypted DPK value. dpk[31:0] When this byte is written, a strobe signal is generated that triggers the decryption and/or storage of the DPK word on the DPK internal RAM memory.

DPTX_HDCPREG_DPK1

Address: Operational Base + offset (0x3624)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	WO	0x000000	DPK_DATA encrypted DPK value. dpk[55:32]

DPTX_HDCP22GPIOSTS

Address: Operational Base + offset (0x3628)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	HDCP22GPIOOUTSTS HDCP22 GPIO OUT Status

DPTX_HDCP22GPIOCHNGSTS

Address: Operational Base + offset (0x362C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	HDCP22GPIOOUTCHNGSTS HDCP22 GPIO OUT change status. If set indicates a change in HDCP22 GPIO output status. Write 1 to clear it

DPTX_HDCPREG_DPK_CRC

Address: Operational Base + offset (0x3630)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DPK_CRC CRC32 value calculated over encrypted DPK. Application can read this value, compare it against the CRC calculated in application to confirm that the DPK write to controller was successful without any errors.

9.5 Interface Description

9.6 Application Notes

9.6.1 Programming Flow After POR

The driver performs the following steps after power-on reset:

9.6.1.1 Assert PHY Reset

1. Set the PHY soft reset by setting the SOFT_RESET_CTRL[1] register.
2. Refer the PHY document to know if anything else need to be reset at this time.
3. Wait for 5us to make sure that the soft reset takes effect and then clear the PHY soft reset bit by writing a 0 to this bit.
4. Wait for the PHYIF_CTRL.PHY_BUSY register to be 0.
5. Ensure that GENERAL_INTERRUPT_ENABLE.HPD_EVENT are cleared.

9.6.1.2 Wait for HPD (Hot Plug Detect) interrupt

Interrupt is asserted and when driver reads the GENERAL_INTERRUPT register, finds HPD_EVENT bit set. This interrupt is generated when the Sink is disconnected and with an HPD transition from 0 to 1 and has stayed at 1 for greater than 0.25ms. This section indicates how the software should handle the interrupt.

1. Software receives an interrupt and reads the GENERAL_INTERRUPT register. GENERAL_INTERRUPTS.HPD_EVENT is set. It should also see that HPD_STATUS.HPD_STATUS is 1.
2. The software should set PHYIF_CTRL.PHY_LANEX_POWERDOWN to 0 to power on the PHY for all enabled lanes.
3. Software clears the interrupt by writing 1 to GENERAL_INTERRUPTS.HPD_EVENT

9.6.1.3 Read Hardware Parameter

Read the DPTX_CONFIG_REG1, DPTX_CONFIG_REG2, DPTX_CONFIG_REG3 register to get the DPTX configuration parameters.

9.6.1.4 Read Edid of the Sink

EDID reads are done using I2C over AUX transactions. See I2C AUX Channel Read/Write for details about initiating I2C over AUX read.

9.6.1.5 Read Sink DPCD registers

Read the sink DPCD register to get at least the following sink information. DPCD registers are read using Native AUX transactions. See NATIVE AUX Channel Read/Write for details about using the Aux channel to read the DPCD.

- Read Sink Rceiver Capability (DPCD address 000000 – 000FF)

This gives the sink supported link rate, lane count, enhance_frame_cap, extended_receiver_capability_present, and so on.

- Read Sink Extended Reciver Capability (DPCD address 02200 – 022FF)

Extended Receiver capability is read only if the sink supports it. Link rate, lane count, enhance_frame_cap.

9.6.1.6 Program Sink DPCD Link Configuration registers

Link configuration registers are programmed based on the Sink setting read during Step-5, and the Video format being transmitted. It also depends on the source configs (Step-3).

9.6.1.7 Initiate link training

- Disable the fast link training if enabled. Fast link training is enabled by default.
- Follow the steps specified in "Full Link Bringup Sequence,"for initiating link training.

9.6.1.8 Configure Video mode

After reading and having parsed the EDID data (step 4), program the controller with the video timings based on the video mode the sink supports and the trained link is able to support. In the single stream (SST) mode, use only stream-0, and program only the corresponding registers. If there is no video stream to transmit, then this setup is not required. Set VSAMPLE_CTRL.video_stream_enable bit to 0 forces the controller to send IDLE patterns.

Follow these steps for every active stream:

1. Program the VSAMPLE_CTRL.video_mapping bit to set the video_mapping input mode (RGB/YCbCr), based on what is supported by the sink.
2. Program the video timing information
   a. Set the Hsync/vsync polarity by programming VINPUT_POLARITY_CTRL register.

b. Program the VIDEO_CONFIG1 register by specifying the following
   - R_v_blank_in_osc – Fractional vblank.
   - I_P – Interlaced/Progressive
   - Hblank – Horizontal blanking period in pixels.
   - Hactive – Horizontal active video period in pixels.

c. Program the VIDEO_CONFIG2 register by specifying the following
   - Vactive – Vertical active video period in terms of pixels.
   - Vblank – Vertical blanking period in terms of vertical blanking lines.

d. Program the VIDEO_CONFIG3 register by specifying the following
   - H_front_porch – The horizontal front porch in terms of pixels.
   - H_sync_width – hsync active pulse width in terms of pixels.

e. Program the VIDEO_CONFIG4 register by specifying the following
   - V_front_porch – The vertical front porch in terms of number of lines.
   - V_sync_width – vsync active pulse width in terms of number of lines.

f. Program the VIDEO_CONFIG5 register by specifying the following
   Specify the Average number of symbols per TU, and average bytes per TU fractional values. Driver should program this register field based on the video format being transmitted and the link rate and lane configuration being used. Section 2.2.1.4 of the DP 1.4 spec gives details about how this average symbol count should be calculated.

3. Program the core for Main Stream Attribute parameters
   a. Program the Stream_N.VIDEO_MSA1 register with the following values
      - Hstart – Horizontal active start from the leading edge of hsync.
      - Vstart – Vertical active start from the leading edge of vsync.
   b. Program the Stream_N.VIDEO_MSA2 register with the following values
      - Mvid – MVID value to be transmitted in the synchronous mode of operation.
      - MISC0 – Specifies synchronous/asynchronous mode of operation and other colormetry values to be transmitted in the MSA.
   c. Program the Stream_N.VIDEO_MSA3 register with the following values
      - Nvid – MVID value to be transmitted in the synchronous mode of operation.
      - MISC1 – Specifies synchronous/asynchronous mode of operation and other colormetry values to be transmitted in the MSA.

9.6.1.9 Configure Audio mode

From step 4, the audio configuration of the Sink are read and the controller is configured to set up the audio mode accordingly by the following steps.

- Program the AUDIO_CONFIG1 register specifying the audio configuration controls
  - audio_inf_select – Select the primary Audio interface option, I2S or SPDIF.
  - audio_data_in_en – Specify which of the data input pins are active. For example for the i2s interface if all 8 channels are supported then all 4 data inputs must be enabled by writing h’F to this field.
  - Audio_data_width – Specify the audio sample data width (16 to 24 bits).
  - hbr_mode_enable – Specify if High Bit Rate audio is to be enabled or not
- Enable transmission of Audio Stream SDP by setting the SDP_VERTICAL_CTRL/SDP_HORIZONTAL_CTRL register bits 1 and 0. From this time, the audio sampler is enabled and the audio samples presented at the I2S/SPDIF inputs are sampled in to the audio FIFOs. Before the audio stream is enabled, the I2S or SPDIF data could be active. But these samples are not transmitted on the main link by the controller.

9.6.1.10 Configure SDPs (Secondary Data Packets)

- Program the SDP_REGISTER_BANK registers with the header and payload of the SPD that are required to be transmitted.
- Program the SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers to indicate when the specific SDP register set need to be transmitted. Also specify the priority by using Bit 31 of these registers.
- If Manual control is required, then program the SDP_MANUAL_CTRL register.

9.6.1.11 Configure HDCP2.2

The following steps must be followed for configuring the HDCP.

1. Program the Synopsys HDCP2.2 controller for the HDCP2.2 initialization. Check the Synopsys HDCP2.2 controller for details.
2. After booting the HDCP2.2 controller, Enable HDCP by setting the HDCPCFG[1] register.
3. Wait for HDCP22 GPIO status change interrupt and check HDCP sink capability by checking the HDCPOBS[28:27] bits.
4. If the sink is not HDCP2.2, go to Step12. If the sink is HDCP2.2 then Call the HL_tx_authenticate() function in the HDCP2.2 library to start the authentication process.
5. Wait for HDCP interrupt and check the authentication status by reading the HDCPOBS register bits 29 and 30.
6. If the authentication is successful, then mainstream are encrypted after this. If authentication is not successful, then it is up to the driver to take the next action.

9.6.1.12 Configure HDCP1.3

1. Configure device private keys when DPTX_HDCP_DPK_ROMLESS configuration parameter is set to true.ie Go to step 13 and return
2. Set HDCPCFG. DPCD12PLUS to 1 if the DPCD revision is 1.2 or higher
3. Write the revocation list to memory.ie Go to step 14 and return
4. Write HDCP_CONFIG [2] to enable HDCP1.3 functionality.
5. Wait for HDCP interrupt indicating authentication success/failure (HDCPAPIINTSTAT.HDCPENGAGED)
6. If authentication is successful, mainstream is encrypted after this. If authentication is not successful, then it is up to the driver to take the next action.

9.6.1.13 Configure Device private keys

1. Disable decryption logic HDCPREG_RMLCTL.ODPK_DECRYPT_ENABLE=0
2. Poll for HDCPREG_RMLSTS. IDPK_WR_OK_STS=1
3. Write unencrypted AKSV[39:32] in HDCPREG_DPK1
4. Write unencrypted AKSV[31:0] in HDCPREG_DPK0
5. Poll for HDCPREG_RMLSTS. IDPK_WR_OK_STS=1 and HDCPREG_RMLSTS. IDPK_DATA_INDEX=1
6. Enable decryption logic HDCPREG_RMLCTL.ODPK_DECRYPT_ENABLE=1
7. Write encryption seed ENC_KEY[15:0] in HDCPREG_SEED
8. Set DPK index value = 1
9. Write DPK[DPK Index value][55:32] to HDCPREG_DPK1
10. Write DPK[DPK Index value][31:0] to HDCPREG_DPK0
11. Poll for HDCPREG_RMLSTS. IDPK_WR_OK_STS=1 and HDCPREG_RMLSTS. IDPK_DATA_INDEX= (DPK Index value+1)
12. Increment DPK Index value by 1
13. Repeat step h to step m till DPK index value reaches 40
14. Read CRC32 value calculated by controller over unencrypted DPKs in HDCPREG_DPK_CRC register
15. Compare the CRC from controller with the original CRC to check for DPK programming result.

9.6.1.14 Program Revocation list

Revocation list is stored in a 8-bit data width SPRAM, though the memory data width is 8-bis, it can only be accessed through 32-bit register read writes so the 8-bit values need to accumulated and written as 32-bit values, do read modify writes if the address does not start at a dword boundary.

Following steps illustrate how it is done.

1. Read HDCP_REVOC_LIST[0]|HDCP_REVOC_SIZE[0:1]|HDCP_VH[19] values by doing a 32-bit register read to address 0x10B8. Keep HDCP_VH[19] unmodified, update HDCP_REVOC_LIST[0]|HDCP_REVOC_SIZE[0:1] and write back the values to the same 32-bit register
2. Set revocation list loop count to 0
3. Write HDCP_REVOC_LIST[2+revocation list loop count: 5+revocation list loop count] by

doing a 32-bit register write to address 0x10BC+(revocaltion list loop count*4)
4. Increment revocation list loop count
5. If (revocation list loop count *4+2) is greater than HDCP_REVOC_SIZE repeat steps step b through step e, else exit

9.6.2 Programming Flow After Re-Authentication Request/Link Integrity Failure from Sink Application

The re-authentication/Link Integrity Failure condition is detected by the driver under the following condition.

- HPD Interrupt is generated. After an interrupt is received, read the INTERRUPTS and see if HPD_EVENT is set. Then check that HPD_STATUS is 1. Clear the HPD_STATUS
- Read the DPCD register and check DPCD.CP_IRQ bit to be set. Write 1 to DPCD.CP_IRQ register field to clear the interrupt. If CP_IRQ is set proceed to next step
- Set the HDCPCFG.CPIRQ bit and clear it after 10 clock cycles.

Controller internally reads Bstatus and checks for Link Integrity failure or re-authentication request and initiates authentication if any of the bits are set. Controller stops encryption at the next CPSR boundary.

9.6.3 Programming Flow After a Hot Unplug Event

This interrupt is generated when the Sink is connected and HPD transition from 1 to 0 staying at 0 for greater than 2 ms. This section indicates how the software handles the interrupt.

1. Software receives an interrupt and reads the GENERAL_INTERRUPT register. GENERAL_INTERRUPT.HPD_EVENT is set. It should also see that HPD_STATUS.HPD_STATUS is 0.
2. The software clears PHYIF_CTRL.XMIT_ENABLE on all lanes to turn off the transmitter. Optionally, PHYIF_CTRL.PHY_LANEX_POWERDOWN can be set to 3 for all enabled lanes to save power.
3. Software clears the interrupt by writing 1 to GENERAL_INTERRUPT.HPD_EVENT.

9.6.4 Programming Flow After a Hot Unplug Event

Follow these steps for Hot plug event after an unplug event:

- Program HDCP soft reset and release it (SOFT_RESET_CTRL.HDCP_MODULE_RESET=1). This step is needed as the HDCP controller is unaware of the unplug event and needs to be reset.
- If audio is enabled, then it should be disabled along with the audio timestamp SDPs by clearing bits 0 and 1 of SDP_VERTICAL_CTRL and SDP_HORIZONTAL_CTRL registers. In addition, the audio sampler should be reset by writing to SOFT_RESET_CTRL. AUDIO_SAMPLER_RESET.
- Follow steps 4 to steps 7. This includes the EDID and DPCP reads.
- steps 8 to steps 11 might be required based on the previous steps.

9.6.5 Programming Flow Sequence for HDCP

Figure 65-5 shows the programming flow sequence for HDCP.

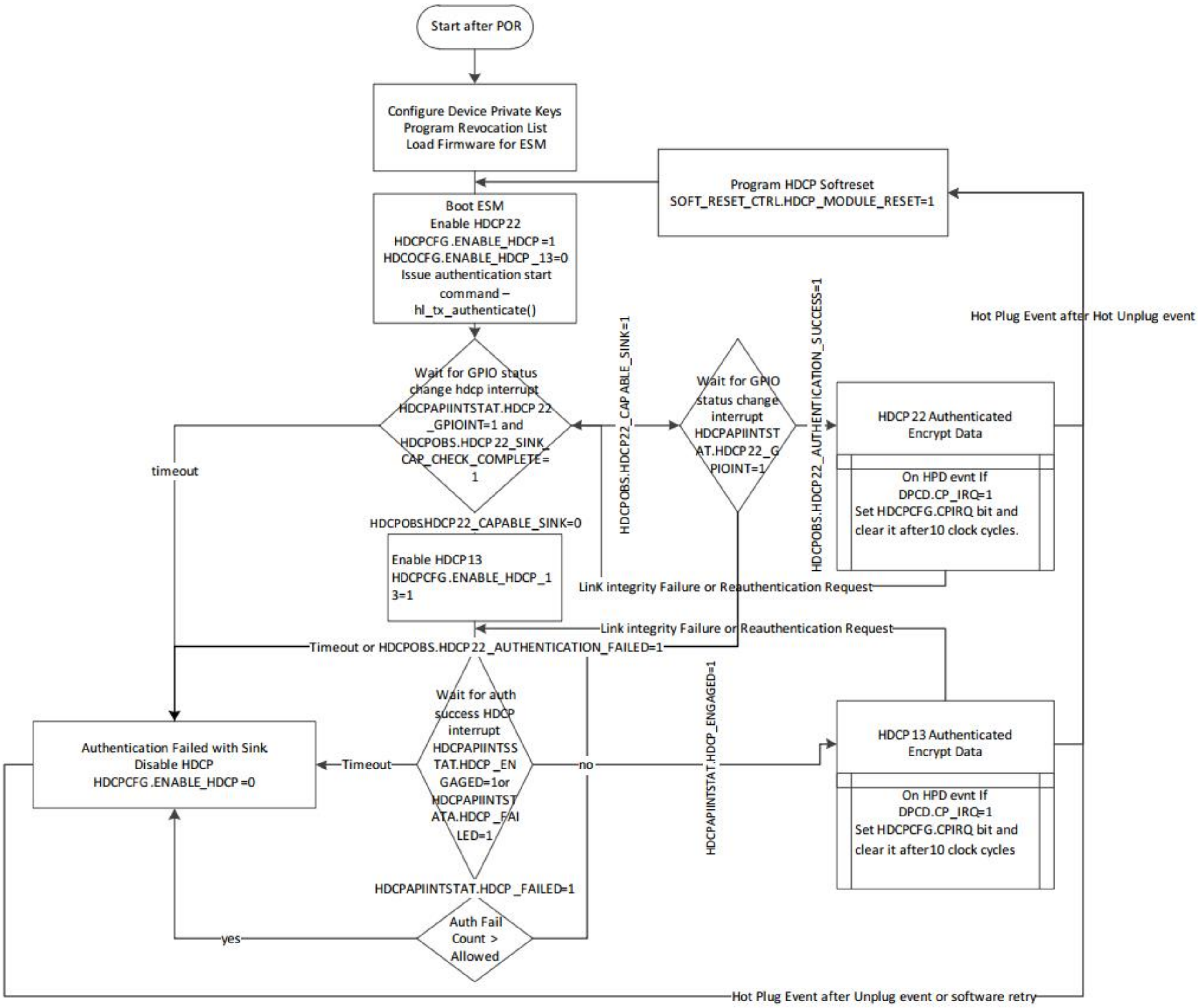

Fig. 65-5 Programming Flow Sequence for HDCP

9.6.6 Link training Sequence

9.6.6.1 Initialization Without Link Training

This initialization sequence assumes that the PHY does not need to go through the link training sequence. This is used to speed up RTL simulation or if the DP Sink Device is capable of receiving Main-Link signal without link training.

1. Set the PHY soft reset. Clear after 5us.
2. Ensure that PHYIF_CTRL.PHY_LANEX_POWERDOWN=0 for all enabled lanes.
3. Set PHYIF_CTRL.PHY_LANES to the desired number of lanes and PHYIF_CTRL.PHY_RATE to the desired rate.
4. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4’h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0
5. Program the predetermined pre-emphasis and voltage swing values into the PHY_TX_EQ registers if required.
6. Enable the transmitter by setting PHYIF_CTRL.XMIT_EN for each enabled lane.

9.6.6.2 Basic Link Bring up Sequence with Fast Link Training

This sequence is applicable if the PHY is to use predetermined pre-emphasis and swing values. This sequence occurs if the Sink DPCD 00003h NO_AUX_TRANSACTION_LINK_TRAINING is read to be 1 and if the source policy is to initiate TPS1 and TPS2/3/4 for 500us each.

1. Set the PHY soft reset. Wait for the read to return 0.
2. Ensure that GENERAL_INTERRUPT_ENABLE.HPD_EVENT is cleared.

3. Wait for the sink to be connected
   a. After an interrupt is received, read the INTERRUPTS and see if HPD_EVENT is set. Then check that HPD_STATUS.HPD_STATUS is 1. This indicates that the Sink has been connected.
   b. If IRQ_HPD is received instead of HPD_EVENT and DPCD Revision is 1.2 or greater, then check LINK_SERVICE_IRQ_VECTOR_ESI0.RX_CAP_CHANGED bit. This also indicates that the Sink has been connected. Also recheck if NO_AUX_TRANSACTION_LINK_TRAINING is still set. If it is cleared, then do a full link training process.
4. Ensure that PHYIF_CTRL.PHY_LANEX_POWERDOWN=0 for all enabled lanes.
5. Based on the highest link rate, highest number of lanes supported, and Source policy, set PHYIF_CTRL.PHY_LANES, and PHYIF_CTRL.PH_YRATE.
6. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4’h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0
7. Program the predetermined pre-emphasis and voltage swing values into the PHY_TX_EQ registers if required.
8. Set PHYIF_CTRL.TPS_SEL=1 to send TPS1
9. Enable the transmitter by setting PHYIF_CTRL.XMIT_EN for each enabled lane.
10. Wait for 500us.
11. Set PHYIF_CTRL.TPS_SEL to the following:
    a. 2 if HBR is the highest desired rate
    b. 3 if HBR2 is the highest desired rate
    c. 4 if HBR3 is the highest desired rate
12. Wait for 500us.
13. Set PHYIF_CTRL.TPS_SEL to 0

9.6.6.3 Full Link Bring up Sequence

By default, fast link training is enabled, which allows the controller to transmit fail safe video format, as specified in section “Fast Link Training”. This feature should be disabled by clearing the CCTL.DEFAULT_FAST_LINK_TRAIN_EN register bit.
The default value of PHY power state from the controller is P3. For any PHY rate change operation, the power state must be P3 or P2.

1. Based on the highest link rate, highest number of lanes supported, and Source policy, set PHYIF_CTRL.PHY_LANES, and PHYIF_CTRL.PHY_RATE. If Rocket IO PHY is used, set PHYIF_CTRL.SSC_DIS=1.
2. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4’h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0.
3. Set PHYIF_CTRL.TPS_SEL=0 to force the transmitted pattern to none.
   While using a PHY with Pipe Interface (DPTX_PHYIF_TYPE=2), transition the unused lanes to P3 before going to step 4. For example, if the number of lanes programmed in step 1 is 1, then the lanes 2, 3, and 4 should be transitioned to P3. Use the PHYIF_POWERDOWN_CTRL[0] register at offset 0xA18 for this. The PHYIF_PWRDOWN_CTRL[0].PER_LANE_PWRDOWN_CTL_EN register should be set to 1. The PHYIF_CTRL.PHY_POWERDOWN register is not used for controlling individual lanes powerdown.
4. Program the pre-emphasis and voltage swing values into the PHY_TX_EQ registers corresponding to voltage swing level 0 and pre-emphasis level 0 for all enabled lanes.
5. Set PHYIF_CTRL.TPS_SEL=1 to send TPS1.
6. Enable the transmitter by setting PHYIF_CTRL.XMIT_EN for each enabled lane.
7. Set the following DPCD registers on the Sink – using AUX Channel Interface Registers:
   a. LINK_BW_SET register (DPCD Address 00100h) to the desired rate.
   b. LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0) to the desired # of lanes.
   c. DOWNSPREAD_CTRL register (DPCD Address 00107h), SPREAD_AMP must be set to 1

for a regular PHY and 0 for Rocket IO.
d. MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) to 01h.
e. TRAINING_PATTERN_SET register (DPCD Address 00102h) to 21h.
f. TRAINING_LANEx_SET register (DPCD Addresses 00103h through 00106h) for each lane to voltage swing level 0 and pre-emphasis level 0.
g. Note that TRAINING_PATTERN_SET and TRAINING_LANEx_SET registers must be written in one AUX CH burst write transaction.

8. Read the DPCD Sink TRAINING_AUX_RD_INTERVAL field in the TRAINING_AUX_RD_INTERVAL register (DPCD Address 0000Eh, bits 6:0) and wait the specified time period before reading the LANEx_CR_DONE bit of the lane in the LANEx_y_STATUS register (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate).
   a. If LANEx_CR_DONE is not set for all enabled lane, then read for ADJUST_REQUEST_LANEx_y register (DPCD Address(es) 00206h and 00207h) for all enabled lanes, then set the local register PHY_TX_EQ to the requested level. Wait TRAINING_AUX_RD_INTERVAL and then re-read LANEx_CR_DONE.
   b. if LANEx_CR_DONE is still not set and the same voltage and swing levels have been tried 5times, then reduce the link rate by one level. Set PHYIF_CTRL.PHY_RATE accordingly. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. Repeat <XREF>.
   c. If the rate is already reduced to RBR, but LANEx_CR_DONE is only set for 1 or 2 lanes, then set PHYIF_CTRL.PHY_LANES to match, and PHYIF_CTRL.PHY_RATE to the high supported rate. Repeat <XREF>. Training fails if LANEx_CR_DONE is never set for any lane.
   d. If LANEx_CR_DONE is set for all enabled lanes, then move on to the next step.
9. Set PHYIF_CTRL.TPS_SEL to the following
   - if HBR is the highest desired rate
   - 3 if HBR2 is the highest desired rate
   - 4 if HBR3 is the highest desired rate
10. Write the following to the DPCD sink registers: 22h for TPS2, 23h for TPS3, or 07h for TPS4 to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and the current drive setting to the TRAINING_LANEx_SET register (DPCD Addresses 00103h through 00106h). Ensure that scrambling (CCTL.SCRAMBLE_DISABLE = 0) is enabled if TPS4 is transmitted.
11. Wait TRAINING_AUX_RD_INTERVAL, and then read the following:
   - LANEx_CR_DONE
   - LANEx_CHANNEL_EQ_DONE bit in the LANEx_y_STATUS register (DPCD Address 00202h, bits 1 and 5, and DPCD Address 00203h, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
   - LANEx_SYMBOL_LOCKED bit in the LANEx_y_STATUS register (DPCD Address 00202h, bits 2 and 6, and DPCD Address 00203h, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
   - INTERLANE_ALIGN_DONE bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively)
12. Wait TRAINING_AUX_RD_INTERVAL, and then read the following:
   - If some of the register values are still 0, then ADJUST_REQUEST_LANEx_y register (DPCD Address(es) 00206h and 00207h) and adjust PHY_TX_EQ according the requested drive level settings. Repeat step 9.
   - If after 5 iterations, the EQ bits are not set, then reduce rate. Set PHYIF_CTRL.PHY_RATE accordingly. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. Repeat step 9.
   - If the rate is already reduced to RBR, then do the following:
     Clear the TRAINING_PATTERN_SET register (DPCD Address 00102h).
     Set PHYIF_CTRL.TPS_SEL =1 and set PHY_TX_EQ to default voltage swing and pre-emphasis (400mV, no pre-emphasis).
     Write 21h to the TRAINING_PATTERN_SET register (and appropriate values to the

TRAINING_LANEx_SET register (DPCD Addresses 00103h through 00106h)) to initiate training

13. Set PHYIF_CTRL.TPS_SEL to 0 when finished. Set DPCD Sink TRAINING_PATTERN_SET register to 00h.

9.6.6.4 Combo PHY

- For rate changes, PHYIF_CTRL.PHY_LANE0_POWERDOWN must be set to 2 or 3 and PHYIF_CTRL.PHY_BUSY must be low before PHYIF_CTRL.PHY_RATE is changed. P2 can be used to change rates more quickly than P3.
- Only PHYIF_CTRL.PHY_LANE0_POWERDOWN is used for the Combo PHY. PHYIF_CTRL.PHY_LANE{1,2,3}_POWERDOWN have no effect.
- Every bit of PHYIF_CTRL.PHY_BUSY[15:13] is the same as PHYIF_CTRL.PHY_BUSY[12].

9.6.7 AUX Channel Access

1. If write set AUX_DATA 0/1/2/3 first. Then write the CMD register with the desired CMD_TYPE, ADDR and LENGTH. Note the CMD register is transmitted as-is over the AUX channel so make sure unused bits are ‘0’.
2. Once the write to the CMD register is done, the request is queued for execution and additional writes to the data/cmd registers are disabled. The register bit AUX_STATUS.AUX_REPLY_RECEIVED is set to indicate the AUX channel is ACTIVE/BUSY.
3. Wait for an interrupt, and check to see if GENERAL_INTERRUPT.AUX_REPLY_EVENT is set. Alternatively, if INTERRUPT_ENABLE.AUX_REPLY_EVENT_EN is reset, software can poll AUX_STATUS.AUX_REPLY_RECEIVED to see if a response has been received. This bit resets to ‘0’ when the AUX transfer completes.
4. If GENERAL_INTERRUPT.AUX_REPLY_EVENT=1, then software can read AUX_STATUS to find the outcome of the AUX transfer.
   - If the AUX_STATUS.AUX_STATUS is AUX ACK then the AUX request is fully executed and read data is available in AUX_DATA0/1/2/3.
   - If it is AUX WRITE NACK, then the software can read AUX_STATUS.AUX_M indicates the number of bytes that are written.
5. If AUX_STATUS.AUX_TIMEOUT is set or the AUX_STATUS.AUX_STATUS is AUX NACK or AUX DEFER, then AUX_DATA0/1/2/3 are not valid.
6. Clear GENERAL_INTERRUPT.AUX_REPLY_EVENT.
7. If the SINK response is other than ACK, it is the SW responsibility to follow the DP spec and continue with the appropriate AUX request.

9.6.8 Test 80-bit Custom Pattern Programming

1. Read DPCD TEST_80BIT_CUSTOM_PATTERN (00250h to 025Bh)
2. Program CUSTOMPAT0/1/2 according to the TEST_80BIT_CUSTOM_PATTERN[79:0] read from the DPCD.
3. Based on the desired link rate, highest number of lanes supported, and Source policy, set PHYIF_CTRL.PHY_LANES and PHYIF_CTRL.PHY_RATE.
4. Wait until PHYIF_CTRL.PHY_BUSY is cleared for the desired lanes that have been enabled. For example, if 4 lanes are enabled, then wait until PHYIF_CTRL.PHY_BUSY[3:0]=4’h0. If only 1 lane enabled, then wait until PHYIF_CTRL.PHY_BUSY[0]=0
5. Set PHYIF_CTRL.XMIT_ENABLE for each enabled lane to enable the transmission.
6. You can check the CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_CAP is supported and set CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_EN=1 along with the DURATION_CTRL=1. (DPCD 0025Bh). This step can be omitted for standalone testing with an oscilloscope.

9.6.9 INIT_THRESHOLD Value Calculation

The INIT_THRESHOLD determines how many clock cycles the link packetizer logic should wait after the pixel data is available in the lane steering FIFO, before reading it and transmitting it on the link. Based on the lane steering logic push rate and the link rate, this value changes for various modes of operations. The calculated value should be programmed into the INIT_THRESHOLD, and INIT_THRESHOLD_HI fields of the VIDEO_CONFIG5 register.

Chapter 10 CRYPTO

10.1 Overview

CRYPTO is a hardware accelerator for encrypting or decrypting. It supports the most commonly used algorithm: DES/3DES, AES, SHA1, SHA256, MD5 and PKA.
The CRYPTO is divided into NSCRYPTO(CRYPTO for nonsecure) and SCRYPTO(CRYPTO for secure). NSCRYPTO is different from SCRYPTO base address and has the same function. SCRYPTO has more characteristics than NSCRYPTO.
The CRYPTO supports following features:

- Support Link List Item (LLI) DMA transfer
- Support SHA-1, SHA-256/224, SHA-512/384, MD5, SM3 with hardware padding
- Support HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
- Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
- Support DES & TDES cipher
- Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support SM4 ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES/TDES ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
- Support up to 8-channels configuration
- Support generating random numbers
- SCRYPTO AES/DES/TDES/SM4/HASH supports lockstep error monitoring
- SCRYPTO AES/DES/TDES/SM4 supports anti side channel attack
- SCRYPTO supports receiving KEY from KEYLAD

10.2 Block Diagram

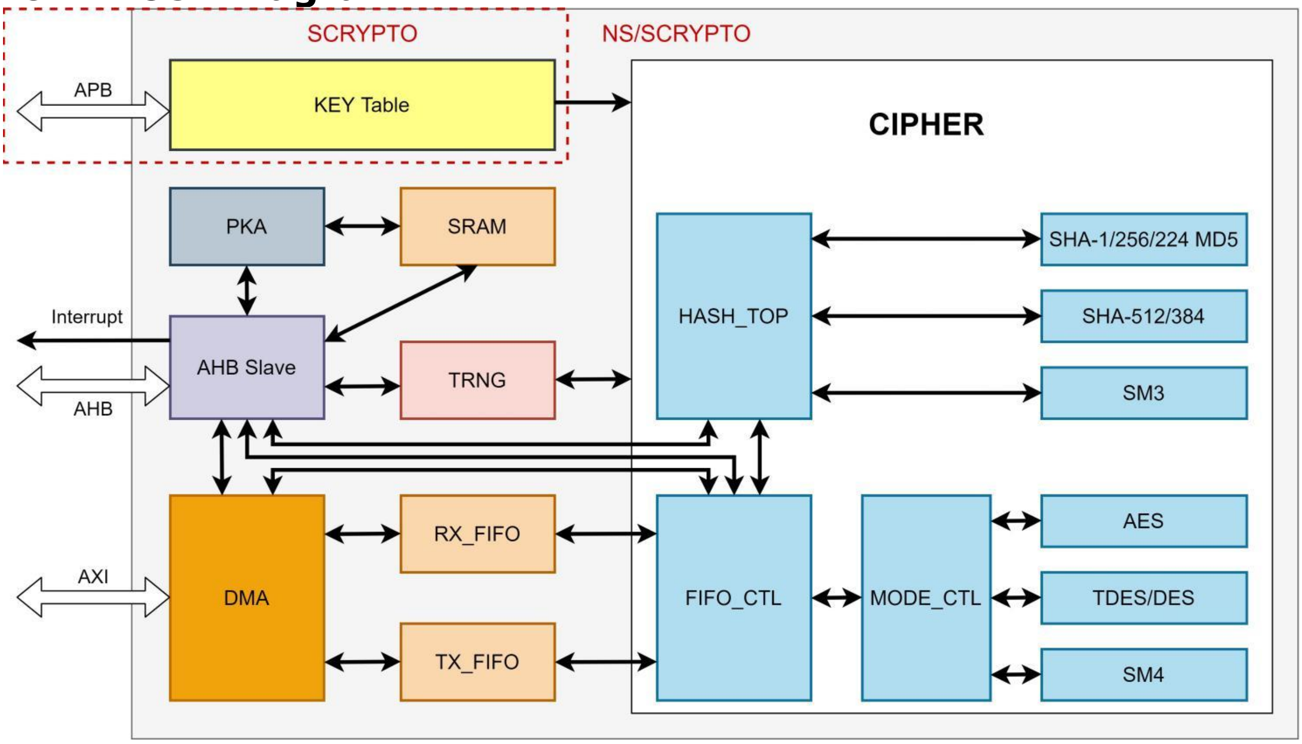

Fig. 10-1 CRYPTO Architecture

CRYPTO contains several modules: AHB_Slave, DMA, CIPHER, PKA. SCRYPTO also contains a special module: KEY_Table.

AHB_Slave

AHB_Slave is used to configure registers. This module is in HCLK domain.

DMA

DMA is used to transfer data from external memory to RX_FIFO, or from TX_FIFO to external memory. DMA uses 64-bits AXI3 protocol with max burst length to 16. LLI transfer is also supported for performance and convenience consideration. This module is in ACLK domain.

CIPHER
CIPHER contains AES, SM4, DES/TDES and HASH engines. And it also supports various mode operations. The source data is either from RX_FIFO, or from other engine output. The result data is sending either to TX_FIFO, or Registers in module AHB_Slave. This module is in CLK_CORE domain.

PKA
PKA is used to accelerate mathematical operations for big numbers. It supports - Modular arithmetic (addition, subtraction, multiplication and division), Regular arithmetic (addition, subtraction, multiplication and division), Modular inversion, Modular exponentiation, □ Logical operations (AND, OR, XOR, SHIFT). PKA has a SRAM which is used to store source, result and intermediate data for PKA operations. The software driver could use PKA operations to implement complicate calculation, such as RSA, ECC etc. It could support up to 4096 bits RSA modular exponentiation calculation. This module is in CLK_PKA domain.

TRNG
TRNG is used to collects random bits from the ring oscillator, up to 256 random bits per time. In SCRYPTO, TRNG also provides CIPHER with mask to prevent side channel attack. This module is in CLK_RNG domain.

KEY_Table
KEY Table is an extra module of SCRYPTO compared with NSCRYPTO. KEY Table is used to receive and temporarily store the KEY sent by KEYLAD through APB, and provide the KEY to CIPHER operation. This module is in PCLK domain.

10.3 Register Description

10.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

10.3.2 Registers Summary

The register prefixed with CRYPTO is the same function register of NSCRYPTO and SCRYPTO. The register with prefix of NSCRYPTO and SCRYPTO is the register that NSCRYPTO and SCRYPTO are different or need to be distinguished.

Name	Offset	Size	Reset Value	Description
CRYPTO_CLK_CTL	0x0000	W	0x00000001	Clock Control Register
CRYPTO_RST_CTL	0x0004	W	0x00000000	Reset Control Register
NSCRYPTO_DMA_INT_EN	0x0008	W	0x00000000	DMA Interrupt Enable Register
SCRYPTO_DMA_INT_EN	0x0008	W	0x00000000	DMA Interrupt Enable Register
NSCRYPTO_DMA_INT_ST	0x000C	W	0x00000000	DMA Interrupt Status Register
SCRYPTO_DMA_INT_ST	0x000C	W	0x00000000	DMA Interrupt Status Register
CRYPTO_DMA_CTL	0x0010	W	0x00000000	DMA Control Register
CRYPTO_DMA_LLI_ADDR	0x0014	W	0x00000000	DMA LIST Start Address Register
CRYPTO_DMA_ST	0x0018	W	0x00000000	DMA Status Register
CRYPTO_DMA_STATE	0x001C	W	0x00000000	DMA State Register
CRYPTO_DMA_LLI_RADDR	0x0020	W	0x00000000	DMA LLI Read Address Register
CRYPTO_DMA_SRC_RADDR	0x0024	W	0x00000000	DMA Source Data Read Address Register
CRYPTO_DMA_DST_WADDR	0x0028	W	0x00000000	DMA Destination Data Read Address Register
CRYPTO_DMA_ITEM_ID	0x002C	W	0x00000000	DMA Descriptor ID Register
CRYPTO_FIFO_CTL	0x0040	W	0x00000003	FIFO Control Register

Name	Offset	Size	Reset Value	Description
CRYPTO_BC_CTL	0x0044	W	0x00000000	Block Cipher Control Register
CRYPTO_HASH_CTL	0x0048	W	0x00000004	Hash Control Register
CRYPTO_CIPHER_ST	0x004C	W	0x00000000	Cipher Status Register
CRYPTO_CIPHER_STATE	0x0050	W	0x00000400	Cipher Current State Register
CRYPTO_CHn_IV_0	0x0100 +n*0x10	W	0x00000000	Channel n IV Register 0
CRYPTO_CHn_IV_1	0x0104 +n*0x10	W	0x00000000	Channel n IV Register 1
CRYPTO_CHn_IV_2	0x0108 +n*0x10	W	0x00000000	Channel n IV Register 2
CRYPTO_CHn_IV_3	0x010C +n*0x10	W	0x00000000	Channel n IV Register 3
CRYPTO_CHn_KEY_0	0x0180 +n*0x10	W	0x00000000	Channel n KEY Register 0
CRYPTO_CHn_KEY_1	0x0184 +n*0x10	W	0x00000000	Channel n KEY Register 1
CRYPTO_CHn_KEY_2	0x0188 +n*0x10	W	0x00000000	Channel n KEY Register 2
CRYPTO_CHn_KEY_3	0x018C +n*0x10	W	0x00000000	Channel n KEY Register 3
CRYPTO_CHn_PC_LEN_0	0x0280 +n*0x8	W	0x00000000	Channel n PC Length Register 0
CRYPTO_CHn_PC_LEN_1	0x0284 +n*0x8	W	0x00000000	Channel n PC Length Register 1
CRYPTO_CHn_AAD_LEN_0	0x02C0 +n*0x8	W	0x00000000	Channel n AAD Length Register 0
CRYPTO_CHn_AAD_LEN_1	0x02C4 +n*0x8	W	0x00000000	Channel n AAD Length Register 1
CRYPTO_CHn_IV_LEN_0	0x0300 +n*0x4	W	0x00000000	Channel n IV Length Register 0
CRYPTO_CHn_TAG_0	0x0320 +n*0x10	W	0x00000000	Channel n Tag Register 0
CRYPTO_CHn_TAG_1	0x0324 +n*0x10	W	0x00000000	Channel n Tag Register 1
CRYPTO_CHn_TAG_2	0x0328 +n*0x10	W	0x00000000	Channel n Tag Register 2
CRYPTO_CHn_TAG_3	0x032C +n*0x10	W	0x00000000	Channel n Tag Register 3
CRYPTO_HASH_DOUT_n	0x03A0 +n*0x4	W	0x00000000	HASH Data Output Register n
CRYPTO_TAG_VALID	0x03E0	W	0x00000000	TAG Valid Register
CRYPTO_HASH_VALID	0x03E4	W	0x00000000	HASH Output Valid Register
NSCRYPTO_RNG_CTL	0x0400	W	0x0000000C	RNG Control Register
SCRYPTO_RNG_CTL	0x0400	W	0x00000019	RNG Control Register
CRYPTO_RNG_SAMPLE_CNT	0x0404	W	0x00000000	RNG Sample Counter Register
CRYPTO_RNG_DOUT_n	0x0410 +n*0x4	W	0x00000000	RNG Data Output Register n
CRYPTO_RAM_CTL	0x0480	W	0x00000000	RAM Control Register
CRYPTO_RAM_ST	0x0484	W	0x00000001	RAM Status Register
CRYPTO_DEBUG_CTL	0x04A0	W	0x00000000	PKA Debug Control Register
CRYPTO_DEBUG_ST	0x04A4	W	0x00000001	PKA Debug Status Register

Name	Offset	Size	Reset Value	Description
CRYPTO_DEBUG_MONITOR	0x04A8	W	0x0000FEEF	PKA Debug Monitor Bus Register
SCRYPTO_RNG_START	0x0520	W	0x00000000	RNG start
SCRYPTO_RNG_ST	0x0524	W	0x00000000	RNG work status
SCRYPTO_RNG_INTEN	0x0528	W	0x00000000	RNG interrupt enable
SCRYPTO_RNG_INTST	0x052C	W	0x00000000	RNG interrupt status
SCRYPTO_KEY_SEL	0x0610	W	0x00000000	Operation key select
SCRYPTO_LOCKSTEP_FLAG	0x0618	W	0x00000000	Lockstep mistake flag
SCRYPTO_LOCKSTEP_EN	0x061C	W	0x00000000	Lockstep check enable
NSCRYPTO_AES_VERSION	0x0680	W	0x000707FF	AES_VERSION code is 0x0007_07ff
SCRYPTO_AES_VERSION	0x0680	W	0x000707FF	AES_VERSION code is 0x0007_07ff
NSCRYPTO_DES_VERSION	0x0684	W	0x00030033	DES_VERSION code is 0x0003_0033
SCRYPTO_DES_VERSION	0x0684	W	0x00030033	DES_VERSION code is 0x0003_0033
NSCRYPTO_SM4_VERSION	0x0688	W	0x000007FF	SM4_VERSION code is 0x0000_07ff
SCRYPTO_SM4_VERSION	0x0688	W	0x000007FF	SM4_VERSION code is 0x0000_07ff
NSCRYPTO_HASH_VERSION	0x068C	W	0x000001FF	HASH_VERSION code is 0x0000_01ff
SCRYPTO_HASH_VERSION	0x068C	W	0x000001FF	HASH_VERSION code is 0x0000_01ff
NSCRYPTO_HMAC_VERSION	0x0690	W	0x0000001F	HMAC_VERSION code is 0x0000_001f
SCRYPTO_HMAC_VERSION	0x0690	W	0x0000001F	HMAC_VERSION code is 0x0000_001f
NSCRYPTO_RNG_VERSION	0x0694	W	0x01000000	RNG_VERSION code is 0x0100_0000
SCRYPTO_RNG_VERSION	0x0694	W	0x02000000	RNG_VERSION code is 0x0200_0000
NSCRYPTO_PKA_VERSION	0x0698	W	0x01000000	PKA_VERSION code is 0x0100_0000
SCRYPTO_PKA_VERSION	0x0698	W	0x01000000	PKA_VERSION code is 0x0100_0000
NSCRYPTO_CRYPTO_VERSION	0x06F0	W	0x02000001	CRYPTO_VERSION code is 0x0200_0001
SCRYPTO_CRYPTO_VERSION	0x06F0	W	0x02000002	CRYPTO_VERSION code is 0x0200_0002
CRYPTO_PKA_MEM_MAPn	0x0800 +n*0x4	W	0x00000000	PKA Memory Map n Register
CRYPTO_PKA_OPCODE	0x0880	W	0x00000000	PKA Operation Code Register
CRYPTO_N_NP_T0_T1_ADDR	0x0884	W	0x000FF820	N_NP_T0_T1_ADDR Register
CRYPTO_PKA_STATUS	0x0888	W	0x00000001	PKA Status Register
CRYPTO_PKA_SW_RESET	0x088C	W	0x00000000	software reset of PKA
CRYPTO_PKA_Ln	0x0890 +n*0x4	W	0x00000000	PKA Length n Register
CRYPTO_PKA_PIPE_RDY	0x08B0	W	0x00000001	PKA pipe is ready for new opcode
CRYPTO_PKA_DONE	0x08B4	W	0x00000001	PKA Done Register
CRYPTO_PKA_MON_SELECT	0x08B8	W	0x00000000	PKA Monitor Select Register

Name	Offset	Size	Reset Value	Description
CRYPTO_PKA_DEBUG_REG_EN	0x08BC	W	0x00000000	PKA Debug Enable Register
CRYPTO_DEBUG_CNT_ADDR	0x08C0	W	0x00000000	Debug Counter Address Register
CRYPTO_DEBUG_EXT_ADDR	0x08C4	W	0x00000000	Debug Extra Address Register
CRYPTO_PKA_DEBUG_HALT	0x08C8	W	0x00000000	PKA Debug Halt State Register
CRYPTO_PKA_MON_READ	0x08D0	W	0x0000FEEF	PKA Monitor Read Register
CRYPTO_PKA_INT_ENA	0x08D4	W	0x00000000	PKA Interrupt Enable Register
CRYPTO_PKA_INT_ST	0x08D8	W	0x00000000	PKA Interrupt Status Register
CRYPTO_SRAM_ADDR	0x1000	W	0x00000000	SRAM Base Address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.3.3 Detail Registers Description

CRYPTO_CLK_CTL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	auto_clkgate_en CRYPTO will gate unused Block Cipher and HASH module automatically 1'b0: Disable 1'b1: Enable

CRYPTO_RST_CTL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:3	RO	0x0000	reserved
2	R/W SC	0x0	sw_pka_reset Software set this bit to start a reset to PKA module. After the reset is done, CRYPTO will clear this bit.
1	R/W SC	0x0	sw_rng_reset Software set this bit to start a reset to TRNG module. After the reset is done, CRYPTO will clear this bit.
0	R/W SC	0x0	sw_cc_reset Software set this bit to start a reset to Symmetric Cipher and HASH module. After the reset is done, CRYPTO will clear this bit.

NSCRYPTO_DMA_INT_EN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	zero_len_int_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	list_err_int_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	src_err_int_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	dst_err_int_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	src_item_done_int_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	dst_item_done_int_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	list_done_int_en 1'b0: Disable 1'b1: Enable

SCRYPTO_DMA_INT_EN
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lockstep_int_en 1'b0: Disable 1'b1: Enable
6	RW	0x0	zero_len_int_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	list_err_int_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	src_err_int_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	dst_err_int_en 1'b0: Disable 1'b1: Enable
2	RW	0x0	src_item_done_int_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	dst_item_done_int_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	list_done_int_en 1'b0: Disable 1'b1: Enable

NSCRYPTO_DMA_INT_ST
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	W1C	0x0	zero_len 1'b1: Indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use 1'b0: Nothing
5	W1C	0x0	list_err 1'b1: Indicate that DMA has met an error response when transfer list descriptors. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use 1'b0: Nothing
4	W1C	0x0	src_err 1'b1: Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use 1'b0: Nothing
3	W1C	0x0	dst_err 1'b1: Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use 1'b0: Nothing
2	W1C	0x0	src_item_done 1'b1:Indicate that DMA has completed a read transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use 1'b0: Nothing
1	W1C	0x0	dst_item_done 1'b1: Indicate that DMA has completed a write transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use 1'b0: Nothing
0	W1C	0x0	list_done 1'b1: Indicate that DMA has completed all the transfers which the list descriptors pointed to. After the bit is read, the application should write 1 to clear this bit for next time use 1'b0: Nothing

SCRYPTO_DMA_INT_ST

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	lockstep_flag 1'b0: Nothing 1'b1: Indicate that crypto was attacked
6	RW	0x0	zero_len 1'b0: nothing 1'b1: indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use

Bit	Attr	Reset Value	Description
5	RW	0x0	list_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer list descriptors. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
4	W1C	0x0	src_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
3	W1C	0x0	dst_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
2	W1C	0x0	src_item_done 1'b0: Nothing 1'b1: Indicate that DMA has completed a read transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use
1	W1C	0x0	dst_item_done 1'b0: Nothing 1'b1: Indicate that DMA has completed a write transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use
0	W1C	0x0	list_done 1'b0: Nothing 1'b1: Indicate that DMA has completed all the transfers which the list descriptors pointed to. After the bit is read, the application should write 1 to clear this bit for next time use

CRYPTO_DMA_CTL
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:2	RO	0x0000	reserved
1	R/WSC	0x0	dma_restart If DMA data for next stage is not ready, application could pause DMA by descriptor commands. DMA will stop prefetching next descriptor. The application could restart DMA by asserting this bit when DMA data for next state is ready. CRYPTO will continue with previous transfer, and clear the bit automatically.
0	R/WSC	0x0	dma_start DMA asserts the bit to start DMA transfer, then CRYPTO will clear the bit automatically.

CRYPTO_DMA_LLI_ADDR
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_lli_addr When DMA_CTL start asserted, CRYPTO will read the address to get the 1'st descriptor. It should be 8-bytes align. We suggest dma_lli_addr 64-byte align for best performance consideration.

CRYPTO_DMA_ST
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dma_busy 1'b0: DMA idle 1'b1: DMA busy

CRYPTO_DMA_STATE
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RO	0x0	dma_lli_state For debug use only 2'b00: IDLE STATE 2'b01: FETCH STATE 2'b10: WORK STATE Others: Reserved
3:2	RO	0x0	dma_src_state For debug use only 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved
1:0	RO	0x0	dma_dst_state For debug use only 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved

CRYPTO_DMA_LLI_RADDR
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_lli_raddr For debug use only It indicates the current DMA LLI read address

CRYPTO_DMA_SRC_RADDR
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_src_raddr For debug use only It indicates the current DMA source read address

CRYPTO_DMA_DST_WADDR
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_dst_waddr For debug use only It indicates the current DMA destination write address

CRYPTO_DMA_ITEM_ID
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	dma_item_id For debug use only It indicates the current descriptor ID

CRYPTO_FIFO_CTL
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	dout_byteswap 1'b0: Little endian 1'b1: Big endian
0	RW	0x1	din_byteswap 1'b0: Little endian 1'b1: Big endian

CRYPTO_BC_CTL
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	WO	0x000	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES

Bit	Attr	Reset Value	Description
7:4	RW	0x0	mode For AES 4'h0: ECB 4'h1: CBC 4'h2: CTS 4'h3: CTR 4'h4: CFB 4'h5: OFB 4'h6: XTS 4'h7: CCM 4'h8: GCM 4'h9: CMAC 4'hA: CBC-MAC Others: Reserved For TDES/DES 4'h0: ECB 4'h1: CBC 4'h4: CFB 4'h5: OFB Others: Reserved
3:2	RW	0x0	key_size For AES 2'b00: 128 bit 2'b01: 192 bit 2'b10: 256 bit 2'b11: reserved For TDES/DES, it is reserved
1	RW	0x0	decrypt 1'b0: Encrypt 1'b1: Decrypt
0	RW	0x0	bc_enable 1'b0: Disable 1'b1: Enable

CRYPTO_HASH_CTL

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	WO	0x00	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	hash_cipher_sel 4'h0: SHA-1 4'h1: MD-5 4'h2: SHA-256 4'h3: SHA-224 4'h4: SM3 4'h8: SHA-512 4'h9: SHA-384 4'hA: SHA-512/224 4'hB: SHA-512/256 Others: Reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	hmac_enable CRYPTO supports HMAC-SHA1, HMAC-SHA256, HMAC_SHA512, HMAC-MD5, HMAC-SM3 1'b0: Disable 1'b1: Enable Note: If hmac_enable set '1' hash_cipher_sel must set 0x6 when chose HMAC-SM3 mode hash_cipher_sel set the corresponding value when chose other mode
2	RW	0x1	hw_pad_enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	hash_src_sel 1'b0: From RX-FIFO 1'b1: From TX-FIFO
0	RW	0x0	hash_enable 1'b0: Disable 1'b1: Enable

CRYPTO_CIPHER_ST

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	otp_key_valid Indicate if otp_key is valid. 1'b0: Invalid 1'b1: Valid
1	RO	0x0	hash_busy 1'b0: Idle 1'b1: Busy
0	RO	0x0	block_cipher_busy 1'b0: Idle 1'b1: Busy

CRYPTO_CIPHER_STATE

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:10	RO	0x01	hash_state For debug use only 5'h01: IDLE State 5'h02: IPAD State 5'h04: TEXT State 5'h08: OPAD State 5'h10: OPAD EXT State
9:8	RO	0x0	gcm_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State

Bit	Attr	Reset Value	Description
7:6	RO	0x0	ccm_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State
5:4	RO	0x0	parallel_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved
3:2	RO	0x0	mac_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved
1:0	RO	0x0	serial_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State 2'b11: Reserved

CRYPTO_CHn_IV_0
Address: Operational Base + offset (0x0100+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_0 Channel n range from 0 to 7 CHn_IV_0 address = 0x0100 + 0x10 * n For CTR Mode, IV stands for counter For XTS Mode, IV stands for tweak

CRYPTO_CHn_IV_1
Address: Operational Base + offset (0x0104+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_1 Channel n range from 0 to 7 CHn_IV_1 address = 0x0104 + 0x10 * n For CTR Mode, IV stands for counter For XTS Mode, IV stands for tweak

CRYPTO_CHn_IV_2
Address: Operational Base + offset (0x0108+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_2 Channel n range from 0 to 7 CHn_IV_2 address = 0x0108 + 0x10 * n For CTR Mode, IV stands for counter For XTS Mode, IV stands for tweak

CRYPTO_CHn_IV_3
Address: Operational Base + offset (0x010C+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_3 Channel n range from 0 to 7 CHn_IV_3 address = 0x010c + 0x10 * n For CTR Mode, IV stands for counter For XTS Mode, IV stands for tweak

CRYPTO_CHn_KEY_0
Address: Operational Base + offset (0x0180+n*0x10)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_0 Channel n range from 0 to 7 CHn_KEY_0 address = 0x0180 + 0x10 * n

CRYPTO_CHn_KEY_1
Address: Operational Base + offset (0x0184+n*0x10)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_1 Channel n range from 0 to 7 CHn_KEY_1 address = 0x0184 + 0x10 * n

CRYPTO_CHn_KEY_2
Address: Operational Base + offset (0x0188+n*0x10)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_2 Channel n range from 0 to 7 CHn_KEY_2 address = 0x0188 + 0x10 * n

CRYPTO_CHn_KEY_3
Address: Operational Base + offset (0x018C+n*0x10)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_3 Channel n range from 0 to 7 CHn_KEY_3 address = 0x018c + 0x10 * n

CRYPTO_CHn_PC_LEN_0
Address: Operational Base + offset (0x0280+n*0x8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pc_len_0 Channel n range from 0 to 7 CHn_PC_LEN_0 address = 0x0280 + 0x8 * n Length in byte unit

CRYPTO_CHn_PC_LEN_1
Address: Operational Base + offset (0x0284+n*0x8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:0	RW	0x00000000	chn_pc_len_1 Channel n range from 0 to 7 CHn_PC_LEN_1 address = 0x0284 + 0x8 * n Length in byte unit

CRYPTO_CHn_AAD_LEN_0
Address: Operational Base + offset (0x02C0+n*0x8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_aad_len_0 Channel n range from 0 to 7 CHn_AAD_LEN_0 address = 0x02c0 + 0x8 * n Length in byte unit

CRYPTO_CHn_AAD_LEN_1
Address: Operational Base + offset (0x02C4+n*0x8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	chn_aad_len_1 Channel n range from 0 to 7 CHn_AAD_LEN_1 address = 0x02c4 + 0x8 * n Length in byte unit

CRYPTO_CHn_IV_LEN_0
Address: Operational Base + offset (0x0300+n*0x4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	chn_iv_len Channel n range from 0 to 7 CHn_IV_LEN_0 address = 0x0300 + 0x4 * n Length in byte unit. Up to 16 byte IV for GCM

CRYPTO_CHn_TAG_0
Address: Operational Base + offset (0x0320+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_0 Channel n range from 0 to 7 CHn_TAG_0 address = 0x0320 + 0x10 * n When the corresponding TAG_VALID is high, TAG value is valid

CRYPTO_CHn_TAG_1
Address: Operational Base + offset (0x0324+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_1 Channel n range from 0 to 7 CHn_TAG_1 address = 0x0324 + 0x10 * n When the corresponding TAG_VALID is high, TAG value is valid

CRYPTO_CHn_TAG_2
Address: Operational Base + offset (0x0328+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_2 Channel n range from 0 to 7 CHn_TAG_2 address = 0x0328 + 0x10 * n When the corresponding TAG_VALID is high, TAG value is valid

CRYPTO_CHn_TAG_3

Address: Operational Base + offset (0x032C+n*0x10)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_3 Channel n range from 0 to 7 CHn_TAG_3 address = 0x032c + 0x10 * n When the corresponding TAG_VALID is high, TAG value is valid

CRYPTO_HASH_DOUT_n

Address: Operational Base + offset (0x03A0+n*0x4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_n HASH dout n range from 0 to 15 HASH_DOUT_n address = 0x03a0 + 0x4 * n n'th output word for all hash function, in big endian

CRYPTO_TAG_VALID

Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	ch7_tag_valid When channel 7 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 7 tag is invalid 1'b1: Channel 7 tag is valid
6	W1C	0x0	ch6_tag_valid When channel 6 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 6 tag is invalid 1'b1: Channel 6 tag is valid
5	W1C	0x0	ch5_tag_valid When channel 5 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 5 tag is invalid 1'b1: Channel 5 tag is valid
4	W1C	0x0	ch4_tag_valid When channel 4 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 4 tag is invalid 1'b1: Channel 4 tag is valid

Bit	Attr	Reset Value	Description
3	W1C	0x0	ch3_tag_valid When channel 3 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 3 tag is invalid 1'b1: Channel 3 tag is valid
2	W1C	0x0	ch2_tag_valid When channel 2 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b0: Channel 2 tag is invalid 1'b1: Channel 2 tag is valid
1	W1C	0x0	ch1_tag_valid When channel 1 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 1 tag is invalid 1'b1: Channel 1 tag is valid
0	W1C	0x0	ch0_tag_valid When channel 0 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 0 tag is invalid 1'b1: Channel 0 tag is valid

CRYPTO_HASH_VALID
Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	hash_valid When HASH calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: HASH_DOUT is invalid 1'b1: HASH_DOUT is valid

NSCRYPTO_RNG_CTL
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	WO	0x00	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	rng_len 2'b00: 64 bit 2'b01: 128 bit 2'b10: 192 bit 2'b11: 256 bit

Bit	Attr	Reset Value	Description
3:2	RW	0x3	ring_sel There are 4 OSC rings choice to decide the RNG output data 2'b00: Slowest OSC ring 2'b01: Faster than OSC ring 0 2'b10: Faster than OSC ring 1 2'b11: Fastest OSC ring
1	RW	0x0	rng_enable 1'b0: Disable 1'b1: Enable
0	R/W SC	0x0	rng_start The application triggers this bit to start collect RNG output data. After RNG is started, CRYPTO will clear the bit automatically 1'b0: Do nothing 1'b1: Start

SCRYPTO_RNG_CTL
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	WO	0x000	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:8	RO	0x00	reserved
7:5	RW	0x0	mode Register for RNG mode selected If want to generate random numbers, this bit segment must be 0x4
4:3	RW	0x3	rng_len TRNG output length select 2'b00: 64 bit 2'b01: 128 bit 2'b10: 192 bit 2'b11: 256 bit
2:1	RW	0x0	ring_sel There are 4 OSC rings choice to decide the RNG output data 2'b00: Slowest OSC ring 2'b01: Faster than OSC ring 0 2'b10: Faster than OSC ring 1 2'b11: Fastest OSC ring
0	RW	0x1	rng_enable TRNG OSC ring enable 1'b0: Disable 1'b1: Enable

CRYPTO_RNG_SAMPLE_CNT
Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rng_sample_cnt RNG collects OSC ring output bit every rng_sample_cnt time. The value of rng_sample_cnt affects RNG output data rate, the value more bigger, the rate more slower.

CRYPTO_RNG_DOUT_n

Address: Operational Base + offset (0x0410+n*0x4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_n RNG dout n range from 0 to 7 RNG_DOUT_n address = 0x0410 + 0x4 * n The 32'th OSC ring bit is captured in RNG_DOUT_0.bit31

CRYPTO_RAM_CTL
Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	ram_pka_rdy Indicate whether ram is controlled by PKA engine 1'b0: RAM is controlled by CPU 1'b1: RAM is controlled by CRYPTO PKA engine

CRYPTO_RAM_ST
Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	clk_ram_rdy Indicate whether clk_ram is stable, and ready for use 1'b0: Not stable 1'b1: Stable

CRYPTO_DEBUG_CTL
Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	pka_debug_mode 1'b0: PKA is in normal mode 1'b1: PKA is in debug mode

CRYPTO_DEBUG_ST
Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_debug_clk_en For debug use only 1'b0: Disable 1'b1: Enable

CRYPTO_DEBUG_MONITOR
Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000feef	pka_monitor_bus For debug use only.

SCRYPTO_RNG_START

Address: Operational Base + offset (0x0520)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual 1’b0: Write access disable 1’b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	rng_start The application triggers this bit to make RNG working. After RNG is started, CRYPTO will clear the bit automatically. 1'b0: Do nothing 1'b1: Start

SCRYPTO_RNG_ST

Address: Operational Base + offset (0x0524)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	rng_st RNG work state 1'b0: IDLE 1'b1: BUSY

SCRYPTO_RNG_INTEN

Address: Operational Base + offset (0x0528)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	cpinten Mode completed interrupt enable 1'b0: Disable the interrupt 1'b1: Enable the interrupt

SCRYPTO_RNG_INTST

Address: Operational Base + offset (0x052C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	cpints Mode completed interrupt status 1'b0: Interrupt is inactive 1'b1: Interrupt is active Write 1 clear to 0

SCRYPTO_KEY_SEL

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	key_sel Select which key to use as the operation key 32'h5a5a5a5a: Key table key Others: Normal key

SCRYPTO_LOCKSTEP_FLAG

Address: Operational Base + offset (0x0618)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	lockstep_flag Indicates whether CIPHER has been attacked 1'b0: Not under attack 1'b1: Under attack

SCRYPTO_LOCKSTEP_EN

Address: Operational Base + offset (0x061C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	lockstep_en Enable lockstep check 1'b0: Disable 1'b1: Enable If disable, lockstep_flag field of DMA_INT_ST register will never pull up

NSCRYPTO_AES_VERSION

Address: Operational Base + offset (0x0680)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x1	aes256_flag Whether the AES supports AES256 1'b0: No support 1'b1: Support
17	RO	0x1	aes192_flag Whether the AES supports AES192 1'b0: No support 1'b1: Support
16	RO	0x1	aes128_flag Whether the AES supports AES128 1'b0: No support 1'b1: Support
15:11	RO	0x00	reserved
10	RO	0x1	cbc-mac_flag Whether the AES supports CBC-MAC 1'b0: No support 1'b1: Support
9	RO	0x1	cmac_flag Whether the AES supports CMAC 1'b0: No support 1'b1: Support
8	RO	0x1	gcm_flag Whether the AES supports GCM 1'b0: No support 1'b1: Support
7	RO	0x1	ccm_flag Whether the AES supports CCM 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
6	RO	0x1	xts_flag Whether the AES supports XTS 1'b0: No support 1'b1: Support
5	RO	0x1	ofb_flag Whether the AES supports OFB 1'b0: No support 1'b1: Support
4	RO	0x1	cfb_flag Whether the AES supports CFB 1'b0: No support 1'b1: Support
3	RO	0x1	ctr_flag Whether the AES supports CTR 1'b0: No support 1'b1: Support
2	RO	0x1	cts_flag Whether the AES supports CTS 1'b0: No support 1'b1: Support
1	RO	0x1	cbc_flag Whether the AES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the AES supports ECB 1'b0: No support 1'b1: Support

SCRYPTO_AES_VERSION

Address: Operational Base + offset (0x0680)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x1	aes256_flag Whether the AES supports AES256 1'b0: No support 1'b1: Support
17	RO	0x1	aes192_flag Whether the AES supports AES192 1'b0: No support 1'b1: Support
16	RO	0x1	aes128_flag Whether the AES supports AES128 1'b0: No support 1'b1: Support
15:11	RO	0x00	reserved
10	RO	0x1	cbc-mac_flag Whether the AES supports CBC-MAC 1'b0: No support 1'b1: Support
9	RO	0x1	cmac_flag Whether the AES supports CMAC 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
8	RO	0x1	gcm_flag Whether the AES supports GCM 1'b0: No support 1'b1: Support
7	RO	0x1	ccm_flag Whether the AES supports CCM 1'b0: No support 1'b1: Support
6	RO	0x1	xts_flag Whether the AES supports XTS 1'b0: No support 1'b1: Support
5	RO	0x1	ofb_flag Whether the AES supports OFB 1'b0: No support 1'b1: Support
4	RO	0x1	cfb_flag Whether the AES supports CFB 1'b0: No support 1'b1: Support
3	RO	0x1	ctr_flag Whether the AES supports CTR 1'b0: No support 1'b1: Support
2	RO	0x1	cts_flag Whether the AES supports CTS 1'b0: No support 1'b1: Support
1	RO	0x1	cbc_flag Whether the AES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the AES supports ECB 1'b0: No support 1'b1: Support

NSCRYPTO_DES_VERSION

Address: Operational Base + offset (0x0684)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x1	eee_flag Whether the DES supports EEE mode 1'b0: No support 1'b1: Support
16	RO	0x1	tdes_flag Whether the DES supports TDES 1'b0: No support 1'b1: Support
15:6	RO	0x000	reserved
5	RO	0x1	ofb_flag Whether the DES supports OFB 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
4	RO	0x1	cfb_flag Whether the DES supports CFB 1'b0: No support 1'b1: Support
3:2	RO	0x0	reserved
1	RO	0x1	cbc_flag Whether the DES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the DES supports ECB 1'b0: No support 1'b1: Support

SCRYPTO_DES_VERSION
Address: Operational Base + offset (0x0684)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x1	eee_flag Whether the DES supports EEE mode 1'b0: No support 1'b1: Support
16	RO	0x1	tdes_flag Whether the DES supports TDES 1'b0: No support 1'b1: Support
15:6	RO	0x000	reserved
5	RO	0x1	ofb_flag Whether the DES supports OFB 1'b0: No support 1'b1: Support
4	RO	0x1	cfb_flag Whether the DES supports CFB 1'b0: No support 1'b1: Support
3:2	RO	0x0	reserved
1	RO	0x1	cbc_flag Whether the DES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the DES supports ECB 1'b0: No support 1'b1: Support

NSCRYPTO_SM4_VERSION
Address: Operational Base + offset (0x0688)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RO	0x1	cbc-mac_flag Whether the SM4 supports CBC-MAC 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
9	RO	0x1	cmac_flag Whether the SM4 supports CMAC 1'b0: No support 1'b1: Support
8	RO	0x1	gcm_flag Whether the SM4 supports GCM 1'b0: No support 1'b1: Support
7	RO	0x1	ccm_flag Whether the SM4 supports CCM 1'b0: No support 1'b1: Support
6	RO	0x1	xts_flag Whether the SM4 supports XTS 1'b0: No support 1'b1: Support
5	RO	0x1	ofb_flag Whether the SM4 supports OFB 1'b0: No support 1'b1: Support
4	RO	0x1	cfb_flag Whether the SM4 supports CFB 1'b0: No support 1'b1: Support
3	RO	0x1	ctr_flag Whether the SM4 supports CTR 1'b0: No support 1'b1: Support
2	RO	0x1	cts_flag Whether the SM4 supports CTS 1'b0: No support 1'b1: Support
1	RO	0x1	cbc_flag Whether the SM4 supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the SM4 supports ECB 1'b0: No support 1'b1: Support

SCRYPTO_SM4_VERSION

Address: Operational Base + offset (0x0688)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RO	0x1	cbc-mac_flag Whether the SM4 supports CBC-MAC 1'b0: No support 1'b1: Support
9	RO	0x1	cmac_flag Whether the SM4 supports CMAC 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
8	RO	0x1	gcm_flag Whether the SM4 supports GCM 1'b0: No support 1'b1: Support
7	RO	0x1	ccm_flag Whether the SM4 supports CCM 1'b0: No support 1'b1: Support
6	RO	0x1	xts_flag Whether the SM4 supports XTS 1'b0: No support 1'b1: Support
5	RO	0x1	ofb_flag Whether the SM4 supports OFB 1'b0: No support 1'b1: Support
4	RO	0x1	cfb_flag Whether the SM4 supports CFB 1'b0: No support 1'b1: Support
3	RO	0x1	ctr_flag Whether the SM4 supports CTR 1'b0: No support 1'b1: Support
2	RO	0x1	cts_flag Whether the SM4 supports CTS 1'b0: No support 1'b1: Support
1	RO	0x1	cbc_flag Whether the SM4 supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the SM4 supports ECB 1'b0: No support 1'b1: Support

NSCRYPTO_HASH_VERSION

Address: Operational Base + offset (0x068C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x1	sm3_flag Whether the HASH supports SM3 1'b0: No support 1'b1: Support
7	RO	0x1	md5_flag Whether the HASH supports MD5 1'b0: No support 1'b1: Support
6	RO	0x1	sha512-256_flag Whether the HASH supports SHA-512/256 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
5	RO	0x1	sha512-224_flag Whether the HASH supports SHA-512/224 1'b0: No support 1'b1: Support
4	RO	0x1	sha512_flag Whether the HASH supports SHA-512 1'b0: No support 1'b1: Support
3	RO	0x1	sha384_flag Whether the HASH supports SHA-384 1'b0: No support 1'b1: Support
2	RO	0x1	sha256_flag Whether the HASH supports SHA-256 1'b0: No support 1'b1: Support
1	RO	0x1	sha224_flag Whether the HASH supports SHA-224 1'b0: No support 1'b1: Support
0	RO	0x1	sha1_flag Whether the HASH supports SHA-1 1'b0: No support 1'b1: Support

SCRYPTO_HASH_VERSION
Address: Operational Base + offset (0x068C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x1	sm3_flag Whether the HASH supports SM3 1'b0: No support 1'b1: Support
7	RO	0x1	md5_flag Whether the HASH supports MD5 1'b0: No support 1'b1: Support
6	RO	0x1	sha512-256_flag Whether the HASH supports SHA-512/256 1'b0: No support 1'b1: Support
5	RO	0x1	sha512-224_flag Whether the HASH supports SHA-512/224 1'b0: No support 1'b1: Support
4	RO	0x1	sha512_flag Whether the HASH supports SHA-512 1'b0: No support 1'b1: Support
3	RO	0x1	sha384_flag Whether the HASH supports SHA-384 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
2	RO	0x1	sha256_flag Whether the HASH supports SHA-256 1'b0: No support 1'b1: Support
1	RO	0x1	sha224_flag Whether the HASH supports SHA-224 1'b0: No support 1'b1: Support
0	RO	0x1	sha1_flag Whether the HASH supports SHA-1 1'b0: No support 1'b1: Support

NSCRYPTO_HMAC_VERSION

Address: Operational Base + offset (0x0690)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x1	sm3_flag Whether the HMAC supports SM3 1'b0: No support 1'b1: Support
3	RO	0x1	md5_flag Whether the HMAC supports MD5 1'b0: No support 1'b1: Support
2	RO	0x1	sha512_flag Whether the HMAC supports SHA-512 1'b0: No support 1'b1: Support
1	RO	0x1	sha256_flag Whether the HMAC supports SHA-256 1'b0: No support 1'b1: Support
0	RO	0x1	sha1_flag Whether the HMAC supports SHA-1 1'b0: No support 1'b1: Support

SCRYPTO_HMAC_VERSION

Address: Operational Base + offset (0x0690)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x1	sm3_flag Whether the HMAC supports SM3 1'b0: No support 1'b1: Support
3	RO	0x1	md5_flag Whether the HMAC supports MD5 1'b0: No support 1'b1: Support
2	RO	0x1	sha512_flag Whether the HMAC supports SHA-512 1'b0: No support 1'b1: Support

Bit	Attr	Reset Value	Description
1	RO	0x1	sha256_flag Whether the HMAC supports SHA-256 1'b0: No support 1'b1: Support
0	RO	0x1	sha1_flag Whether the HMAC supports SHA-1 1'b0: No support 1'b1: Support

NSCRYPTO_RNG_VERSION

Address: Operational Base + offset (0x0694)

Bit	Attr	Reset Value	Description
31:0	RO	0x01000000	rng_version_code RNG version code is 0x0100_0000.

SCRYPTO_RNG_VERSION

Address: Operational Base + offset (0x0694)

Bit	Attr	Reset Value	Description
31:0	RW	0x02000000	rng_version_code RNG version code is 0x0200_0000.

NSCRYPTO_PKA_VERSION

Address: Operational Base + offset (0x0698)

Bit	Attr	Reset Value	Description
31:0	RO	0x01000000	pka_version_code PKA version code is 0x0100_0000.

SCRYPTO_PKA_VERSION

Address: Operational Base + offset (0x0698)

Bit	Attr	Reset Value	Description
31:0	RW	0x01000000	pka_version_code PKA version code is 0x0100_0000.

NSCRYPTO_CRYPTO_VERSION

Address: Operational Base + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:0	RO	0x02000001	nscrypto_version_code NSCRYPTO version code is 0x0200_0001.

SCRYPTO_CRYPTO_VERSION

Address: Operational Base + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x02000002	scrypto_version_code SCRYPTO version code is 0x0200_0002.

CRYPTO_PKA_MEM_MAPn

Address: Operational Base + offset (0x0800+n*0x4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_mapn MAP n range from 0 to 31 PKA_MEM_MAPn address = 0x0800 + 0x4 * n Memory map n [11:2], bit[1:0] is stuck to 0
1:0	RO	0x0	reserved

CRYPTO_PKA_OPCODE

Address: Operational Base + offset (0x0880)

Bit	Attr	Reset Value	Description
31:27	WO	0x00	opcode Defines the PKA operation 5'h04: Add, Inc 5'h05: Sub, Dec, Neg 5'h06: ModAdd, ModInc 5'h07: ModSub, ModDec, ModNeg 5'h08: AND, TST0, CLR0 5'h09: OR, COPY, SET0 5'h0A: XOR, FLIP0, INVERT, COMPARE 5'h0B: SHR0 5'h0D: SHR1 5'h0E: SHL0 5'h0F: SHL1 5'h10: MulLow 5'h11: ModMul 5'h12: ModMulN 5'h13: ModExp 5'h14: Division 5'h15: Div 5'h16: ModDiv 5'h00: Terminate
26:24	WO	0x0	len The virtual length address 0-7 Virtual address 0 point to PKA_L0 Virtual address 1 point to PKA_L1 ... Virtual address 7 point to PKA_L7
23:18	WO	0x00	reg_a Operand A virtual address 0-15 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
17:12	WO	0x00	reg_b Operand B virtual address 0-15 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
11:6	WO	0x00	reg_r Result register virtual address 0-15 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
5:0	WO	0x00	tag Tag

CRYPTO_N_NP_T0_T1_ADDR

Address: Operational Base + offset (0x0884)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x1f	reg_t1 Virtual address of temporary register number 1 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
14:10	RW	0x1e	reg_t0 Virtual address of temporary register number 0 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
9:5	RW	0x01	reg_np Virtual address of register np Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
4:0	RW	0x00	reg_n Virtual address of register n Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15

CRYPTO_PKA_STATUS

Address: Operational Base + offset (0x0888)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:14	RO	0x00	tag Tag of the Last Operation
13:9	RO	0x00	opcode The last OPCODE
8	RO	0x0	pka_cpu_busy PKA is busy memory control is by PKA
7	RO	0x0	modinv_of_zero Modular inverse of zero flag
6	RO	0x0	alu_sign_out Sign of the last operation(MSB)
5	RO	0x0	alu_carry Carry of the last ALU operation
4	RO	0x0	div_by_zero Division by 0
3	RO	0x0	alu_mod_ovflw Modular overflow flag
2	RO	0x0	alu_out_zero ALU out is 0
1	RO	0x0	pka_busy PKA is busy
0	RO	0x1	pipe_is_busy PKA ready signal 1'b0: Pipe full 1'b1: PKA ready for new command

CRYPTO_PKA_SW_RESET

Address: Operational Base + offset (0x088C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	pka_sw_reset PKA software reset the reset mechanism will take about four PKA clocks until the reset line is de-asserted.

CRYPTO_PKA_Ln
Address: Operational Base + offset (0x0890+n*0x4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_ln Length n range from 0 to 7 PKA_Ln address = 0x0890 + 0x4 * n PKA length n, in bit unit

CRYPTO_PKA_PIPE_RDY
Address: Operational Base + offset (0x08B0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_pipe_rdy PKA pipe is ready for new opcode.

CRYPTO_PKA_DONE
Address: Operational Base + offset (0x08B4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_done PKA operation is completed and pipe is empty.

CRYPTO_PKA_MON_SELECT
Address: Operational Base + offset (0x08B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	pka_mon_select PKA monitor select which PKA FSM monitor is being output.

CRYPTO_PKA_DEBUG_REG_EN
Address: Operational Base + offset (0x08BC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pka_debug_reg_en Enable all the debug mechanism when set.

CRYPTO_DEBUG_CNT_ADDR
Address: Operational Base + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	R/W SC	0x00000	debug_cnt_addr The clock counter initial values. clock is disabled when counter expires. Triggered when pka_debug_en is set.

CRYPTO_DEBUG_EXT_ADDR
Address: Operational Base + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	debug_ext_addr Disable the debug Mechanism.

CRYPTO_PKA_DEBUG_HALT
Address: Operational Base + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pka_debug_halt In debug mode: PKA is in halt state.

CRYPTO_PKA_MON_READ
Address: Operational Base + offset (0x08D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000feef	pka_mon_read This is the PKA monitor bus register output.

CRYPTO_PKA_INT_ENA
Address: Operational Base + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pka_int_ena 1'b0: Disable pka interrupt 1'b1: Enable pka interrupt

CRYPTO_PKA_INT_ST
Address: Operational Base + offset (0x08D8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	pka_int_st Indicate that PKA operation completes. After the bit is read, the application should write 1 to clear this bit for next time use.

CRYPTO_SRAM_ADDR
Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sram_addr Sram address starts from 0x1000 to 0x1fff. When RAM_CTL.ram_pka_rdy == 0, application could access sram. Otherwise, application can't.

10.4 Application Note

10.4.1 Clock & Reset

There are 4 clock domains in CRYPTO. The clock and reset signals are described in the following table.

Table 10-1 CRYPTO Clock & Reset Description

Signal	Attr	Description
hclk	clock	AHB clock
aclk	clock	AXI master clock
pclk(SCRYPTO only)	clock	APB master clock
clk_core	clock	Cipher work clock

Signal	Attr	Description
clk_pka	clock	PKA work clock
clk_rng	clock	TRNG work clock
hresetn	reset	Asynchronously assert, synchronously de-assert to hclk, low active
aresetn	reset	Asynchronously assert, synchronously de-assert to aclk, low active
presetn(SCRYPTO only)	reset	Asynchronously assert, synchronously de-assert to pclk, low active
resetn_core	reset	Asynchronously assert, synchronously de-assert to clk_core, low active
resetn_pka	reset	Asynchronously assert, synchronously de-assert to clk_pka, low active
resetn_rng	reset	Asynchronously assert, synchronously de-assert to clk_rng, low active

Each function need different clocks. The applications could gate the un-used clock to save power. Please see the following table for detail information.

Table 10-2 CRYPTO Clock & Reset Description

Operation	HCLK	ACLK	CLK_CORE	CLK_PKA
AES	ON	ON	ON	OFF
DES/TDES	ON	ON	ON	OFF
SM4	ON	ON	ON	OFF
HASH/HMAC	ON	ON	ON	OFF
PKA	ON	OFF	OFF	ON

Even when CLK_CORE is on, CRYPTO is doing some cipher job. And CRYPTO could still be able to automatically gate most parts of un-used blocks to save more power, if CRYPTO_CLK_CTL. auto_clkgate_en is set to ‘1’. The default value for this bit is also ‘1’. Application could do a soft reset to a certain clock domain. Please refer to “Chapter CRU” for more details.

10.4.2 Performance

Cipher performance is shown in the following table.

Table 10-3 CRYPTO Performance Description

Algorithm	block size (Byte)	clk_core frequency (Mhz)	cycle	serial max throughput (MBps)	parallel max throughput (MBps)
DES	8	350	18	155	622
TDES	8	350	55	50	203
AES-128	16	350	12	466	1866
AES-192	16	350	14	400	1600
AES-256	16	350	16	350	1400
SM4	16	350	34	164	658
SM3	64	350	66	339	NA
SHA-1	64	350	81	276	NA

Algorithm	block size (Byte)	clk_core frequency (Mhz)	cycle	serial max throughput (MBps)	parallel max throughput (MBps)
MD5	64	350	65	344	NA
SHA-256/224	64	350	65	344	NA
SHA-512/384/ 512_224/ 512_256	128	350	81	553	NA
RSA-2048	NA	350	130K	NA	NA

There are 2 column throughput rates in the table, 1 is serial mode, the other is parallel mode. In parallel mode, there are 4 engines working at the same time. So the speed is 4 times than serial mode. Parallel mode includes ECB/CTR/XTS both encryption and decryption mode, CFB/CBC/CTS only decryption mode. Other modes are serial. HASH doesn't have parallel mode.
For RSA-2048, the time-consuming MODEXP operation needs about 130K clock cycles.

10.4.3 DMA

DMA supports Link List Item (LLI) DMA transaction.

- Each item contains 8 bytes, and start address should be 8 bytes align
- We suggest that DATA start address is 8 bytes align
- Total DATA length is byte align
- Support segmenting HASH/HMAC DATA into multi sections. We suggest that each section DATA length is a multiple of 64 bytes, except this section is the last section

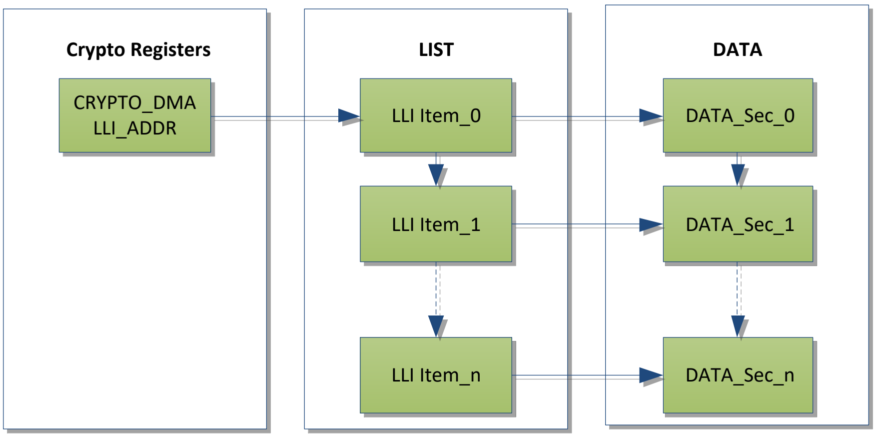

Fig. 10-2 LLI DMA Usage

As shown in the Figure above, Register CRYPTO_DMA_LLI_ADDR points to 1'st LLI item in external memory. Each LLI item contains DATA address, length, control information and next LLI item pointer, except the last LLI item. The last item doesn't have the next LLI Item pointer. After the last LLI item is finished, DMA will go to idle state.
LLI item definition is shown in the following table.

Table 10-4 LLI Item Description

offset	Def	Description
0x00	SRC_ADDRESS[31:0]	Source data start address
0x04	SRC_LENGTH[31:0]	Source data length, in byte unit
0x08	DST_ADDRESS[31:0]	Destination data start address

offset	Def	Description
0x0c	DST_LENGTH[31:0]	Destination data length, in byte unit
0x10	USER_DEFINE[31:0]	Used in cipher block
0x14	IV_OFFSET	IV offset
0x18	DMA_CTRL[31:0]	Used in DMA block
0x1c	NEXT_ADDRESS[31:0]	Next LLI item address. When DMA_CTRL.LAST = “1”, NEXT_ADDRESS is invalid

DMA_CTRL: the definition is shown in the following table.

Table 10-5 LLI Item dma_ctl Description

Bit	Def	Definition
[31:24]	ITEM_ID[7:0]	Used to identify LLI items
[23:16]	Reserved	Reserved
[15:11]	Reserved	Reserved
10	Source_item_done enable	When source data fetch is completed, CRYPTO_DMA_INT_ST.source_item_done will assert if this bit is set
9	Dst_item_done enable	When destination data fetch is completed, CRYPTO_DMA_INT_ST.dst_item_done will assert if this bit is set
8	List_done enable	When all LLI items transfer is completed, CRYPTO_DMA_INT_ST.list_done will assert if this bit is set
[7:2]	Reserved	Reserved
1	PAUSE	Indicate DMA will hold on after executes current item. DMA won’t go on unless CRYPTO_DMA_CTL.restart is configured
0	LAST	Indicate current item is the last one. After executes current item, DMA will return to IDLE state

Table 10-6 LLI Item user_define Description

Bit	Signal	Description
31:7	Reserved	Reserved
6:4	Chnl_num	Channel number, from 0 to 7
3	String_attr	Indicate current item's attribution 1: ADA; 0: PC(plaintext or ciphertext)
2	String_last	Indicate current item is the string last item
1	String_start	Indicate current item is the string first item
0	Cipher_start	Indicate current item is the cipher first item

10.4.4 Hash and cipher operation

NSCRYPTO and SCRYPTO have the same function of hash and cipher.

10.4.5 TRNG

- **How to start**

After configuring other registers, NSCRYPTO starts random number generation after configuring rng_start bit segment of register NSCRYPTO_RNG_CTL. For SCRYPTO, after other register are configured and rng_enable bit segment of register SCRYPTO_RNG_CTL is configured, SCRYPTO_RNG_START register must be configured to start random number generation.

- **First start in SCRYPTO**

SCRYPTO will automatically generate a random number after reset release. Only after the first random number generation is completed can the register be configured to generate a new random number.

- **Interrupt in SCRYPTO**

SCRYPTO will set register SCRYPTO_RNG_INTEN after generating random number. If register SCRYPTO_RNG_INTST is configured, SCRYPTO will set interrupt signal.

10.4.6 Lockstep in SCRYPTO

When SCRYPTO's SCRYPTO_LOCKSTEP_EN register is configured, SCRYPTO_LOCKSTEP_FLAG register will be set when SCRYPTO is attacked. When SCRYPTO_LOCKSTEP_FLAG register is set, only reset SCRYPTO can clear the register.

10.4.7 KEY Table in SCRYPTO

KEY Table is used to receive and temporarily store the KEY sent by KEYLAD through APB, and provide the KEY to CIPHER operation. If SCRYPTO uses the KEY in the KEY Table as the KEY of the CIPHER operation, it also needs to configure the SCRYPTO_KEY_SEL register to be the value of 0x5a5a5a5a.

10.4.8 Multi-Channel Map

There are 8-channel configurations for AES or DES/TDES operation. For different key-size, the map is different. Please find the register map in the following table.

Table 10-7 LLI Item user_define Description

Cipher sel	chnl num	key	iv(tag/...)
AES-128/ DES	0	CH0_KEY0-3/ CH0_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	n	CHn_KEY0-3/ CHn_KEY0-1	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	7	CH7_KEY0-3/ CH7_KEY0-1	CH7_IV0-3/ CH7_IV0-1
AES-192/ TDES	0	CH0_KEY0-3, CH1_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	1	CH2_KEY0-3, CH3_KEY0-1	CH1_IV0-3/ CH1_IV0-1
AES-192/ TDES	2	CH4_KEY0-3, CH5_KEY0-1	CH2_IV0-3/ CH2_IV0-1
AES-192/ TDES	3	CH6_KEY0-3, CH7_KEY0-1	CH3_IV0-3/ CH3_IV0-1
AES-192/ TDES	4-7	not supported	not supported
AES-256	0	CH0_KEY0-3, CH1_KEY0-3	CH0_IV0-3/ CH0_IV0-1
AES-256	1	CH2_KEY0-3, CH3_KEY0-3	CH1_IV0-3/ CH1_IV0-1

Cipher sel	chnl num	key	iv(tag/...)
AES-256	2	CH4_KEY0-3, CH5_KEY0-3	CH2_IV0-3/ CH2_IV0-1
AES-256	3	CH6_KEY0-3, CH7_KEY0-3	CH3_IV0-3/ CH3_IV0-1
AES-256	4-7	not supported	not supported

In AES-XTS mode, there are 2 keys, and only AES-128 and AES-256 mode are. Please refer to the following table for detail information.

Table 10-8 LLI Item user_define Description

Cipher sel	chnl num	key1	key2	tweak
AES-128	0	CH0_KEY0-3	CH4_KEY0-3	CH0_IV0-3
AES-128	1	CH1_KEY0-3	CH5_KEY0-3	CH1_IV0-3
AES-128	2	CH2_KEY0-3	CH6_KEY0-3	CH2_IV0-3
AES-128	3	CH3_KEY0-3	CH7_KEY0-3	CH3_IV0-3
AES-128	4-7	not supported	not supported	not supported
AES-128	NA	not supported	not supported	not supported
AES-256	0	CH0_KEY0-3, CH1_KEY0-3	CH4_KEY0-CH5_KEY3	CH0_IV0-3
AES-256	1	CH2_KEY0-3, CH3_KEY0-3	CH6_KEY0-CH7_KEY3	CH1_IV0-3
AES-256	2-7	not supported	not supported	not supported

10.4.9 HASH Data Path

HASH and AES could run in parallel way. There are 2 paths lead to AES-HASH function. One is AES-HASH-RX mode, the other is AES-HASH-TX mode.

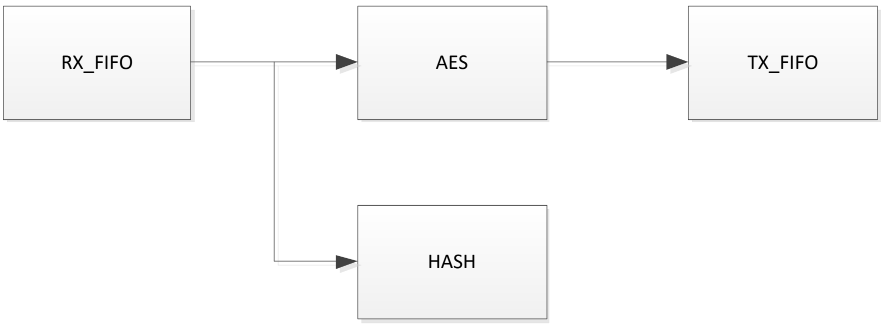

Fig. 10-3 AES-HASH-RX mode

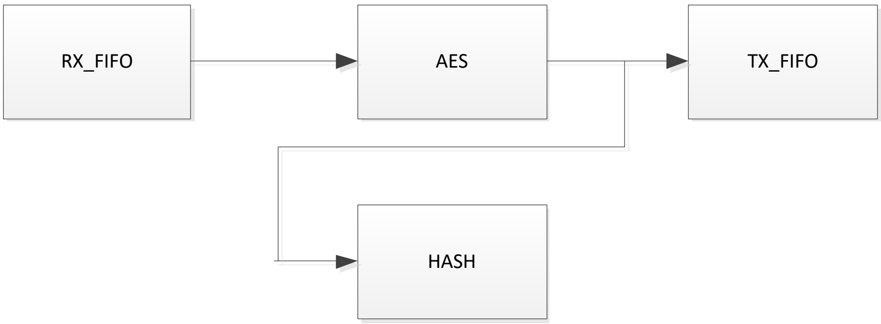

Fig. 10-4 AES-HASH-TX mode

As shown in the figures above, we could facilitate operations in some cases. For example, secure boot, we need both AES and HASH operations for the same blocks of data. The data HASH gets from RX_FIFO or TX_FIFO is byte swapped if the byte swap function is configured.

10.4.10 Program Steps

The application could succeed various CRYPTO operations if they program properly.

- Program the LLI address to DMA_LLI_ADDR
- Program KEY, IV, or other parameter if needed
- Program BC_CTL or HASH_CTL for control information
- Prepare LLI Item
- Enable interrupt, or do nothing

All these operations could be in any order

- Program DMA_CTL.start to start the operation

This step should be the last configuration step. After this register is configured, other registers should not be changed

- Wait interrupt asserted, or just poll the DMA_INT_ST bits
- Program DMA_INT_ST to clear interrupt status, and get the result

The application could also use LLI.pause when the next LLI item is not ready. After the new item is prepared, the application could program DMA_CTL.restart to continue previous operation

Chapter 11 PCIe Controller

11.1 Overview

The PCI Express (PCIe) is a high performance, general purpose I/O interconnect defined for a wide variety of future computing and communication platforms. The PCIe designed to be used as a general-purpose serial I/O interconnect in multiple market segments, including desktop, mobile, server, storage, and embedded communications. The PCIe controller implements the three PCI Express protocol layers (Transaction layer, Data Link layer, and the MAC portion of the physical layer). It also implements the application-dependent functionality of the PCI Express Transaction Layer for packet transmission, which is located between application logic and the PCI Express protocol layers.

The PCIe controller is compliant with PCI Express Specifications 1.1, 2.1, 3.0. The PCIe controller subsystem consists of 5 controllers, refer to Block Diagram for details.

PCIe controller subsystem supports the following features:

- Compatible with PCI Express Base Specification Revision 3.0
- Including 5 PCIe controllers
  - PCIe3_4L DM mode
    - Maximum payload size is 256 bytes
    - 16 ATU inbound regions, 16 ATU outbound regions
    - Up to Gen3 X4 link
    - Embedded 2-Channel DMA(2ch Read, 2ch Write) with Hardware Flow Control
    - Separate Refclk with Independent Spread Spectrum Clocking (SRIS) when working with Gen 3 PHY
  - PCIe3_2L RC mode
    - Maximum payload size is 256 bytes
    - 16 ATU inbound regions, 16 ATU outbound regions
    - Up to Gen3 X2 link
    - Separate Refclk with Independent Spread Spectrum Clocking (SRIS) when working with Gen 3 PHY
  - PCIe3_1L0/1L1/1L2 RC mode
    - Maximum payload size is 256 bytes
    - 8 ATU inbound regions, 8 ATU outbound regions
    - Up to Gen3 X1 link when connecting with Gen3 PHY, and Gen2 X1 link when connecting with Combo PIPE PHY
    - Separate Refclk with Independent Spread Spectrum Clocking (SRIS) when connecting with Gen 3 PHY
- The following optional features of the specification
  - Alternative Routing-ID Interpretation (ARI)
  - Address Translation Services (ATS) by your application
  - TLP Prefix
  - Dynamic Power Allocation (DPA)
  - L1 Substates (L1SS)
  - Resizable BAR (RBAR) with Expanded RBAR and VF Resizable BAR support
  - Separate Refclk with Independent Spread Spectrum Clocking (SRIS)
  - Gen3 Receiver Impedance
  - PCI Express Active State Power Management (ASPM)
  - PCI Express Advanced Error Reporting (AER) with Multiple Header Logging
- Support Latency Tolerance Reporting (LTR)
- Support Optimized Buffer Flush and Fill (OBFF)
- Internal Datapath Operating at 62.5 MHz, 125 MHz, 250MHz
- Advanced Power and Clock Management
- Internal Address Translation Unit
- Internal MSI-X Generation Module
- Automatic Lane Reversal
- Up-configure Support

- RAS DES (Debug, Error Injection, and Statistics)
- ECRC Generation and Checking
- Configuration Intercept Controller to allow your application to modify CFG access from wire
- Store-and-forward Queue Modes for Rx TLPs
- Configurable Filtering Rules for Posted, Non-posted, and Completion Traffic
- Configurable BAR Filtering, I/O Filtering, Configuration Filtering and Completion Lookup/Timeout
- Three Application Transmit Clients
- MSI with Per-Vector Masking (PVM), Extended message data for MSI
- MSI-X with Per-Vector Masking (PVM)

11.2 Block Diagram

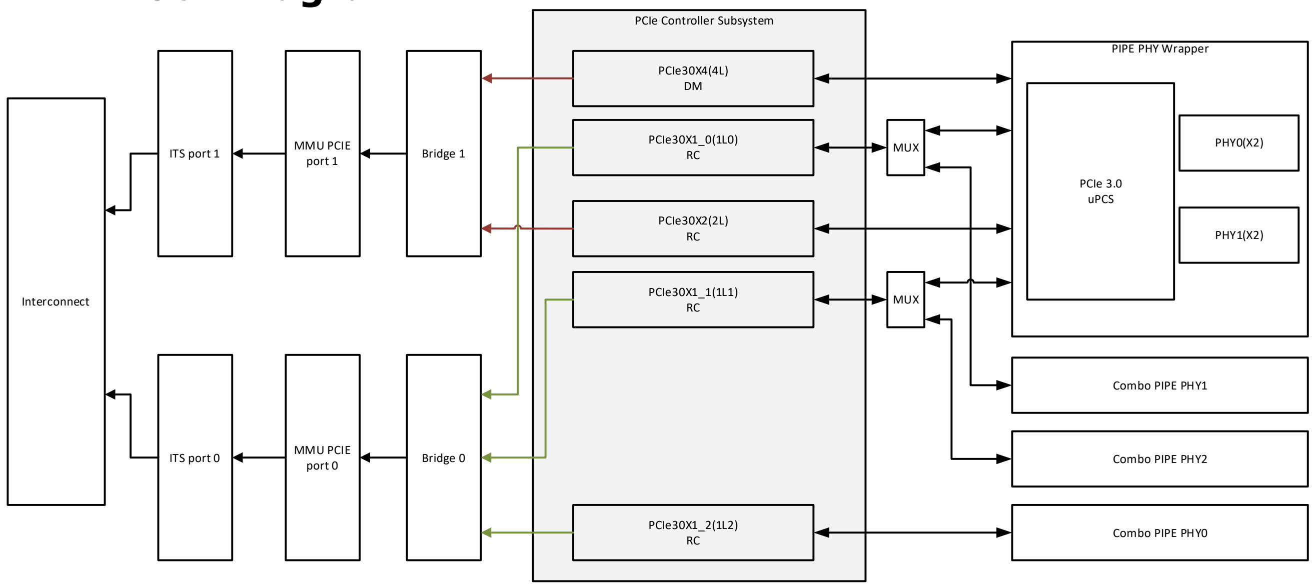

Fig. 11-1 PCIe Controller Subsystem Block Diagram

The PCIe controller subsystem consists of 5 controllers, the 4L and 2L is located in PD_PCIE, 1L0/1/2 is in PD_PHP. PD_PCIE belongs to PD_PHP, so, PD_PCIE should be power down before PD_PHP if the system wants to power PD_PHP. For detail multiplexers of the PHY subsystem, refer to Chapter Multi-PHY.

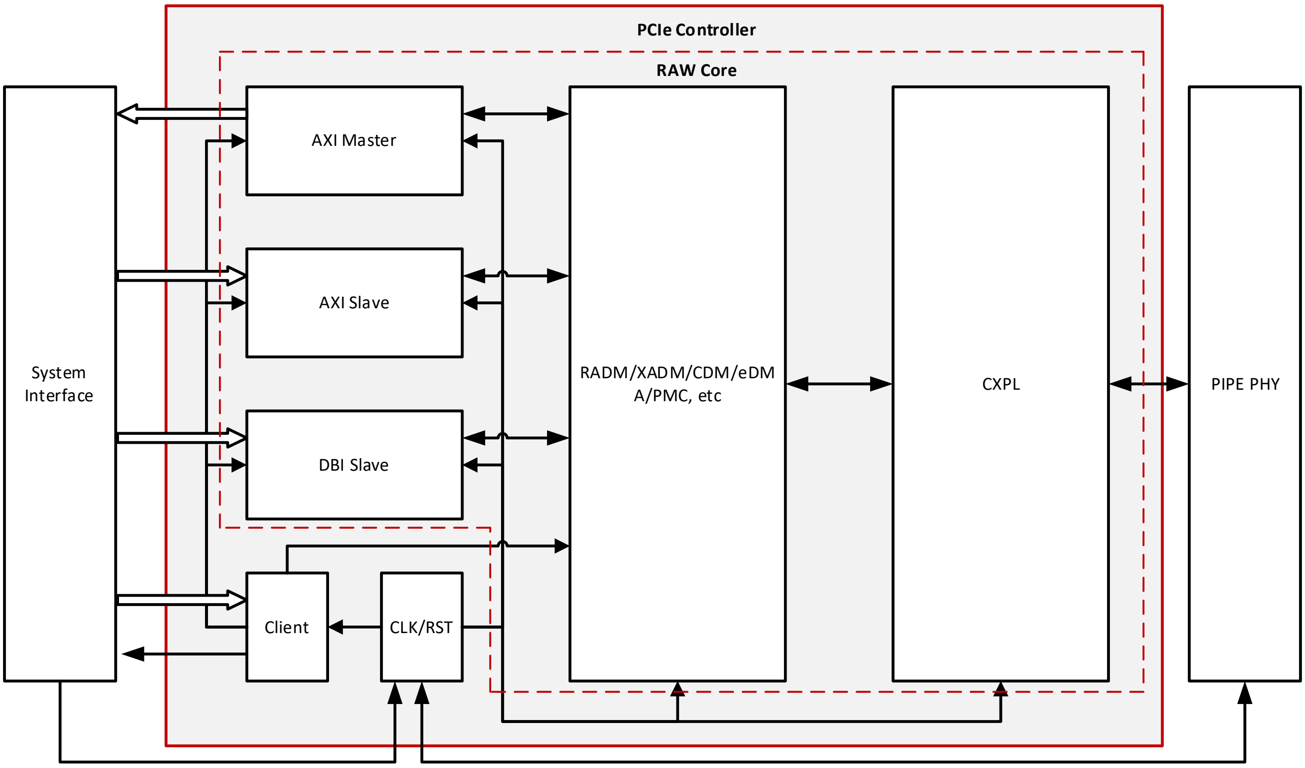

Fig. 11-2 PCIe Controller Architecture Overview

Each Controller consists of RAW core and some application glue logic, like Client and CLK/RST block. The RAW core implements of the PCIe protocol and mode-specific features, including several AXI bus interface, RADM/XADM/CDM/eDMA/PMC/CXPL.

11.3 Function Description

11.3.1 Application Interface and AXI Bridge

Application Interface comprises with four standard interfaces: one AXI master interface, two AXI slave interface and one APB interface. These interface bridging capability for directly adding a PCI Express link to an AXI system fabric.

The AXI bridge module acts as a bridge between the standard AXI interfaces and the PCIe controller native interfaces. The bridge interconnects the AXI interfaces within an AXI-embedded system with a remote PCIe link, as either a root complex port or as an endpoint port.

The AXI master interfaces enable a remote PCIe device to read and write to an AXI slave (in System Interface) connected to the AXI bridge. The AXI link slave interface enables an AXI master (in System Interface) to read and write through the AXI bridge to a remote PCIe device. The DBI slave enables an AXI master (in System Interface) to access the controller’s registers. The APB enables Application to access the Client registers.

11.3.2 Client

Client Logic Consists of some additional logic used for application to interact with PCIe Controller. For example, applications can access client registers to send/receive PCIe Message, request to enter/exit PM state, deal with interrupts, configure some basic operation mode, read some basic debug information, and so on. For more details, please refer to Client registers description and application notes for more information.

11.3.3 eDMA

The RC system CPU, or the EP application CPU, can offload the transferring of large blocks of data to the embedded DMA controller, leaving the CPU free to perform other tasks. The embedded DMA have one read channel and one write channel. It can simultaneously perform the two types of memory transactions:

- DMA write: Transfer (copy) of a block of data from local (application) memory to remote (link partner) memory.

- DMA read: Transfer (copy) of a block of data from remote (link partner) memory to local (application) memory.

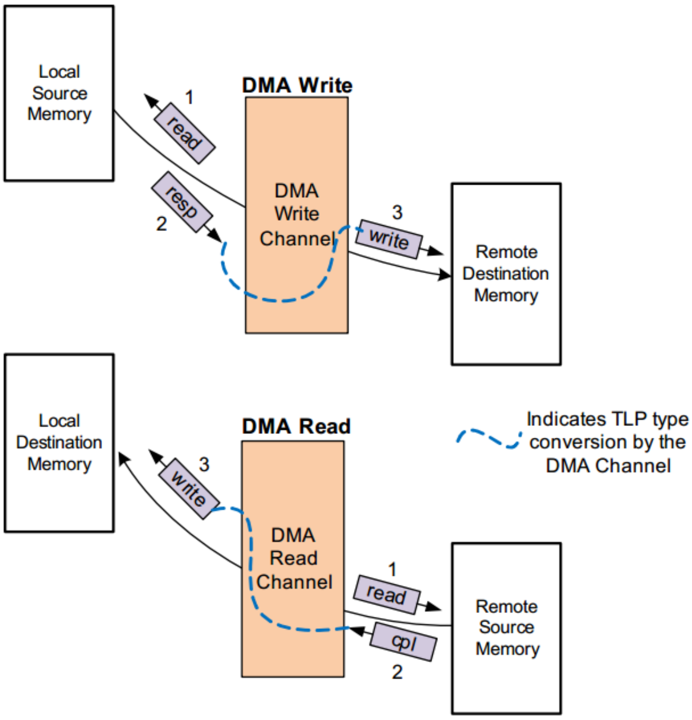

Fig. 11-3 System Level View of PCIe EDMA

Therefore, the EDMA supports full duplex operation, processing read and write transfers at the same time, and in parallel with normal (non-DMA) traffic. Upon completion of a DMA transfer or an error, the DMA optionally interrupts the local CPU or sends an interrupt MWr (Memory Write) to the remote CPU. The DMA is highly configurable and can be programed by using the local DBI AXI Slave interface.

The EDMA provides a linked list (LL) mode to efficiently move data from source to destination with minimal intervention from the local CPU. For details, please refer to DMA Registers Description and Application notes for more information.

11.3.4 CXPL

PCIe Core deal with the PCIe protocol, and consists of three main modules:

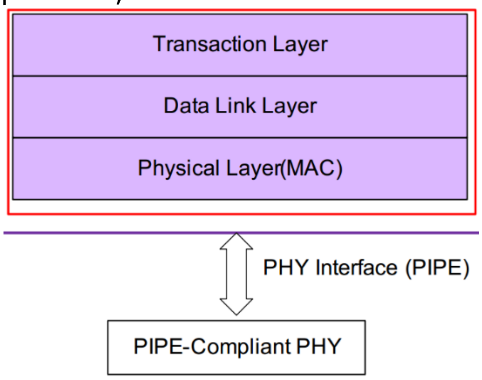

Fig. 11-4 PCIe Core Architecture Overview

The PCIe Core implements the basic functionality for the PCI Express physical, link, and transaction layers. This module implements a large part of the transaction layer logic, all of the data link layer logic, and the MAC portion of the physical layer, including the link training and status state machine (LTSSM). The Core connects to the external PHY through the standard PIPE interface.

11.3.5 PMC

PCIe Controller support PCIe ASPM, L1 Substate and PCI PM. For proper understanding of PCIe Power Management, you should be familiar with Power Management of the PCI Express Base Specification, and PCI-SIG Engineering Change Notice ECN L1 Substates with CLKREQ#. For application details, please refer to Application Notes for more information.

11.3.6 XADM

Transmit Application-Dependent Module (XADM) implements the application-specific functionality of the PCI Express transaction layer for packet transmission. Its functions include:

- TLP Arbitration
- TLP Formation
- Flow Control (FC) Credit checking

The transmit path uses a cut-through architecture. It does not implement transmit buffering/queues (other than the retry buffer). The controller maintains an internal Target Completion Lookup Table to store certain TLP header information from the Rx request

11.3.7 RADM

Receive Application-Dependent Module (RADM) implements application-specific functionality of the PCI Express transaction layer for packet reception. Its functions include:

- Sorting/filtering of received TLPs. The filtering rules and routing are configurable.
- Buffering and queuing of the received TLPs.
- Routing of received TLP to the controller's receive interfaces.

The RADM maintains a Receive Completion Lookup Table (LUT) for completion tracking and completion-timeout monitoring of Tx non-posted requests. It indicates a timeout when an expected Rx completion does not arrive within the timeout period.

11.3.8 CDM

Configuration-Dependent Module (CDM) implements:

- Standard PCI Express configuration space
- Controller-specific register space (Port Logic Registers

11.4 Register Description

PCIe Registers can be accessed by either local CPU through AXI DBI bus or remote RC device through PCIe link or both. The way through local CPU will be mentioned as 'DBI' and the way through PCIe link will be mentioned as 'wire' in this section.

Some read-only registers can be made temporarily R/W when you write 1 to the DBI_RO_WR_EN bit of the MISC_CONTROL_1_OFF register. These registers will be specifically mentioned in their description if they have this feature.

11.4.1 Internal Address Mapping

PCIe local address mapping is listed in this section.

Table 11-1 PCIe3_4L DM G3 Client and Core Register Address Mapping

Base Address	Name	Device	Address Length	Offset Address Range
0xF5000000	PCIe3_4L_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xa40000000	PCIe3_4L_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xF0000000	PCIe3_4L_S	PCIe Outbound Memory	16M BYTE	0x0000000~0xffffff
0x900000000	PCIe3_4L_S	PCIe Outbound Memory	1G BYTE	0x00000000~0x3fffffff
0xFE150000	PCIe3_4L_APB	Client Register	64K BYTE	0x0000~0xffff

Table 11-2 PCIe3_2L RC G3 Client and Core Register Address Mapping

Base Address	Name	Device	Address Length	Offset Address Range
0xF5400000	PCIe3_2L_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xa40400000	PCIe3_2L_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff

Base Address	Name	Device	Address Length	Offset Address Range
0xF1000000	PCIe3_2L_S	PCIe Outbound Memory	32M BYTE	0x0000000~0x1ffffff
0x940000000	PCIe3_2L_S	PCIe Outbound Memory	1G BYTE	0x00000000~0x3fffffff
0xFE160000	PCIe3_2L_APB	Client Register	64K BYTE	0x0000~0xffff

Table 11-3 PCIe3_1L0 RC G2 Client and Core Register Address Mapping

Base Address	Name	Device	Address Length	Offset Address Range
0xF5800000	PCIe3_1L0_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xa40800000	PCIe3_1L0_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xF2000000	PCIe3_1L0_S	PCIe Outbound Memory	32M BYTE	0x0000000~0x1ffffff
0x980000000	PCIe3_1L0_S	PCIe Outbound Memory	1G BYTE	0x00000000~0x3fffffff
0xFE170000	PCIe3_1L0_APB	Client Register	64K BYTE	0x0000~0xffff

Table 11-4 PCIe3_1L1 RC G2 Client and Core Register Address Mapping

Base Address	Name	Device	Address Length	Offset Address Range
0xF5C00000	PCIe3_1L1_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xa40c00000	PCIe3_1L1_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xF3000000	PCIe3_1L1_S	PCIe Outbound Memory	32M BYTE	0x0000000~0x1ffffff
0x9c0000000	PCIe3_1L1_S	PCIe Outbound Memory	1G BYTE	0x00000000~0x3fffffff
0xFE180000	PCIe3_1L1_APB	Client Register	64K BYTE	0x0000~0xffff

Table 11-5 PCIe3_1L2 RC G2 Client and Core Register Address Mapping

Base Address	Name	Device	Address Length	Offset Address Range
0xF6000000	PCIe3_1L2_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xa41000000	PCIe3_1L2_DBI	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xF4000000	PCIe3_1L2_S	PCIe Outbound Memory	32M BYTE	0x0000000~0x1ffffff
0xa00000000	PCIe3_1L2_S	PCIe Outbound Memory	1G BYTE	0x00000000~0x3fffffff

Base Address	Name	Device	Address Length	Offset Address Range
0xFE190000	PCIe3_1L2_APB	Client Register	64K BYTE	0x0000~0xffff

Core Register map is as follows:
RC mode:

Table 11-6 PCIe3_4L DM Core Register Map in RC mode

Offset	Register Block	Description
0x0000	TYPE1_HDR	PCI-Compatible Configuration Space Header Type1
0x0040	PM_CAP	PCI Power Management Capability Structure
0x0050	MSI_CAP	MSI Capability Structure
0x0070	PCIE_CAP	PCI Express Capability Structure
0x00b0	MSIX_CAP	MSI-X Capability Structure
0x0100	AER_CAP	Advanced Error Reporting Capability Structure
0x0148	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0190	L1SUB_CAP	L1 Substates Capability Structure
0x01d0	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x02d0	VSECDMA_CAP	PF DMA Capability Structure
0x0700	PORT_LOGIC	Port Logic
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability Structure
0x300000	ATU_CAP	ATU Port Logic Structure
0x380000	DMA_CAP	DMA Port Logic Structure

EP mode:

Table 11-7 PCIe3_4L DM Core Register Map in EP mode

Offset	Register Block	Description
0x0000	TYPE0_HDR	PCI-Compatible Configuration Space Header Type0
0x0040	PM_CAP	PCI Power Management Capability Structure
0x0050	MSI_CAP	MSI Capability Structure
0x0070	PCIE_CAP	PCI Express Capability Structure
0x00b0	MSIX_CAP	MSI-X Capability Structure
0x0100	AER_CAP	Advanced Error Reporting Capability Structure
0x0148	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0168	ATS_CAP	Address Translation Services Capability Structure
0x0178	PRS_EXT_CAP	PRS Capability Structure
0x0188	LTR_CAP	Latency Tolerance Reporting Capability Structure
0x0190	L1SUB_CAP	L1 Substates Capability Structure
0x01a0	DPA_CAP	DPA Capability Structure
0x01d0	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x02d0	VSECDMA_CAP	PF DMA Capability Structure
0x02e8	RESBAR_CAP	Resizable BAR Capability Structure
0x0700	PORT_LOGIC	Port Logic
0x200e00	ELBI_APP	ELBI Application Register
0x100000	TYPE0_HDR_DBI2	DBI2 Shadow Block: PF PCI-

Offset	Register Block	Description
		Compatible Configuration Space Header Type0
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability
0x300000	ATU_CAP	ATU Port Logic Structure
0x380000	DMA_CAP	DMA Port Logic Structure
0x2000	ATU_CAP	BAR4: ATU Port Logic Structure
0x0000	DMA_CAP	BAR4: DMA Port Logic Structure
0x0e00	ELBI_APP	CFG: ELBI Application Register
0x4000	MSI-X Table	BAR4: MSI-X Table
0x5000	MSI-X PBA	BAR4: MSI-X PBA
0x300000	MSI-X Table	MSI-X Table, when setting dbi_msix_table_access_ctrl to 1. The dbi_msix_table_access_ctrl should be de-asserted if no access
0x308000	MSI-X PBA	MSI-X PBA, when setting dbi_msix_table_access_ctrl to 1. The dbi_msix_table_access_ctrl should be de-asserted if no access

Table 11-8 PCIe3_2L RC Core Register Map in RC mode

Offset	Register Block	Description
0x0000	TYPE1_HDR	PCI-Compatible Configuration Space Header Type1
0x0040	PM_CAP	PCI Power Management Capability Structure
0x0050	MSI_CAP	MSI Capability Structure
0x0070	PCIE_CAP	PCI Express Capability Structure
0x00b0	MSIX_CAP	MSI-X Capability Structure
0x0100	AER_CAP	Advanced Error Reporting Capability Structure
0x0148	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0180	L1SUB_CAP	L1 Substates Capability Structure
0x0190	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x0700	PORT_LOGIC	Port Logic
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability Structure
0x300000	ATU_CAP	ATU Port Logic Structure

Table 11-9 PCIe3_1Ln RC Core Register Map in RC mode

Offset	Register Block	Description
0x0000	TYPE1_HDR	PCI-Compatible Configuration Space Header Type1
0x0040	PM_CAP	PCI Power Management Capability Structure
0x0050	MSI_CAP	MSI Capability Structure
0x0070	PCIE_CAP	PCI Express Capability Structure
0x00b0	MSIX_CAP	MSI-X Capability Structure
0x0100	AER_CAP	Advanced Error Reporting Capability Structure
0x0148	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0180	L1SUB_CAP	L1 Substates Capability Structure
0x0190	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x0700	PORT_LOGIC	Port Logic

Offset	Register Block	Description
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability Structure
0x300000	ATU_CAP	ATU Port Logic Structure

11.4.2 PCIE_CLIENT Register

11.4.2.1 PCIE_CLIENT Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_GENERAL_CON	0x0000	W	0x00000000	General Control Register
PCIE_CLIENT_INTR_STATUS_MSG_RX	0x0004	W	0x00000000	Interrupt Status Register Related to Message Reception
PCIE_CLIENT_INTR_STATUS_LEGACY	0x0008	W	0x00000000	Interrupt Status Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_STATUS_ERR	0x000C	W	0x00000000	Interrupt Status Register Related to Error Detection
PCIE_CLIENT_INTR_STATUS_MISC	0x0010	W	0x00000000	Interrupt Status Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_STATUS_PMC	0x0014	W	0x00000000	Interrupt Status Register Related Power Management Control
PCIE_CLIENT_INTR_MASK_MSG_RX	0x0018	W	0x00007737	Interrupt Mask Register Related to Message Reception
PCIE_CLIENT_INTR_MASK_LEGACY	0x001C	W	0x000000FF	Interrupt Mask Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_MASK_ERR	0x0020	W	0x0000177F	Interrupt Mask Register Related to Error Detection
PCIE_CLIENT_INTR_MASK_MISC	0x0024	W	0x0000FFFF	Interrupt Mask Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_MASK_PMC	0x0028	W	0x000001FF	Interrupt Mask Register Related Power Management Control
PCIE_CLIENT_POWER_CON	0x002C	W	0x00000008	Power Management Control Register
PCIE_CLIENT_POWER_STATUS	0x0030	W	0x00000000	Power Management Status Register
PCIE_CLIENT_MSG_GEN_CON	0x0034	W	0x00000000	Message Generation Control Register
PCIE_CLIENT_MSI_GEN_CON	0x0038	W	0x00000000	MSI Generation Control Register
PCIE_CLIENT_MSI_GEN_FNUM_TC	0x0040	W	0x00000000	MSI Function Number and TC set Register
PCIE_CLIENT_RBAR_SIZE_INFO0	0x0044	W	0x00000000	Resizable BAR2 to BAR0 Size Information Register
PCIE_CLIENT_RBAR_SIZE_INFO1	0x0048	W	0x00000000	Resizable BAR5 to BAR3 Size Information Register
PCIE_CLIENT_DMA_HSHAKE_TOGG	0x004C	W	0x00000000	DMA Handshake Toggle Register
PCIE_CLIENT_VEN_MSG_RX_INFO0	0x0050	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_RX_INFO1	0x0054	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_VEN_MSG_RX_INFO2	0x0058	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_TX_CFG0	0x005C	W	0x00000000	Vendor Message Transmit Configuration Register 0
PCIE_CLIENT_VEN_MSG_TX_CFG1	0x0060	W	0x00000000	Vendor Message Transmit Configuration Register 1
PCIE_CLIENT_VEN_MSG_TX_CFG2	0x0064	W	0x00000000	Vendor Message Transmit Configuration Register 2
PCIE_CLIENT_LTR_MSG_TX_INFO	0x0068	W	0x00000000	LTR Message Transmit Data Register
PCIE_CLIENT_APP_ERR_RPT_INFO0	0x006C	W	0x00000000	Application Error Report Information Register 0
PCIE_CLIENT_APP_ERR_RPT_INFO1	0x0070	W	0x00000000	Application Error Report Information Register 1
PCIE_CLIENT_APP_ERR_RPT_INFO2	0x0074	W	0x00000000	Application Error Report Information Register 2
PCIE_CLIENT_APP_ERR_RPT_INFO3	0x0078	W	0x00000000	Application Error Report Information Register 3
PCIE_CLIENT_APP_ERR_RPT_INFO4	0x007C	W	0x00000000	Application Error Report Information Register 4
PCIE_CLIENT_OBFF_WAKE_ELE_CFG	0x0080	W	0xB4F05064	OBFF Wake Configuration Register
PCIE_CLIENT_OBFF_WAKE_DEBUG	0x0084	W	0x00000000	OBFF Wake Decoder Debug Register
PCIE_CLIENT_RX_CPL_TIME_OUT_INFO	0x0088	W	0x00000000	RX CPL Timeout Information
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0	0x008C	W	0x00000000	TX CPL Timeout Information 0
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1	0x0090	W	0x00000000	TX CPL Timeout Information 1
PCIE_CLIENT_LOCAL_CRU_CTRL	0x009C	W	0x00000000	Local Clock and Reset Control Register
PCIE_CLIENT_GENERAL_DEBUG_CON	0x0100	W	0x00000000	General Debug Control Register
PCIE_CLIENT_GENERAL_DEBUG_INFO	0x0104	W	0x00000000	General Debug Information Register
PCIE_CLIENT_SLC_DEBUG_INFO_CMN	0x0108	W	0x00000000	Silicon Debug Information Common Register
PCIE_CLIENT_SLC_DEBUG_INFO_LN	0x010C	W	0x00000000	Silicon Debug Information Lane N Register
PCIE_CLIENT_SLC_DEBUG_INFO_V0	0x0114	W	0x00000000	Silicon Debug Information Virtual Channel 0 Register
PCIE_CLIENT_DIAG_STATUS_BUS_SEL	0x0118	W	0x00000000	Diagnostic Status Bus Select Register
PCIE_CLIENT_DIAG_STATUS_BUS_INFO	0x011C	W	0x00000000	Diagnostic Status Bus Information Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_CON	0x0140	W	0x00000000	CDM RASDES Control Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN	0x0144	W	0x00000000	CDM RASDES Information Common Data Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_LN	0x0148	W	0x00000000	Lane N CDM RASDES Information Register

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_CDM_RASDES_TBA_CON	0x0150	W	0x00000000	CDM RASDES TBA Control Register
PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN	0x0154	W	0x00000000	CDM RASDES TBA Common Information Register
PCIE_CLIENT_HOT_RESET_CTRL	0x0180	W	0x00000000	Hot Reset Control Register
PCIE_CLIENT_INTR_EN_MSG_RX	0x0190	W	0x00007737	Interrupt Enable Register Related to Message Reception
PCIE_CLIENT_INTR_EN_LEGACY	0x0194	W	0x000000FF	Interrupt Enable Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_EN_ERR	0x0198	W	0x0000177F	Interrupt Enable Register Related to Error Detection
PCIE_CLIENT_INTR_EN_MISC	0x019C	W	0x0000FFFF	Interrupt Enable Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_EN_PMC	0x01A0	W	0x000001FF	Interrupt Enable Register Related Power Management Control
PCIE_CLIENT_AXI_MSTR_MISC_CON	0x0200	W	0x00000000	AXI Master Sideband Signals Control Register
PCIE_CLIENT_AXI_SLV_ATU_BYPASS	0x0204	W	0x00000000	Address Translate Unit Bypass set Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR	0x0208	W	0x00000000	AXI Slave Write Address Sideband Signals HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR3	0x020C	W	0x00000000	AXI Slave Write Address Sideband Signals 3rd HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR4	0x0210	W	0x00000000	AXI Slave Write Address Sideband Signals 4th HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_TAG	0x0214	W	0x00000000	AXI Slave Write Request Tag Register
PCIE_CLIENT_AXI_SLV_MISC_INFO	0x0218	W	0x00000000	AXI Slave Read Address and Write Data Sideband Signals Control Register
PCIE_CLIENT_AXI_SLV_AW_TLP_PRFX	0x0220	W	0x00000000	AXI Slave Write TLP Prefix
PCIE_CLIENT_AXI_SLV_AR_TLP_PRFX	0x0224	W	0x00000000	AXI Slave Read TLP Prefix
PCIE_CLIENT_DBI_MISC_CON	0x0270	W	0x00000000	DBI Miscellaneous Control Register
PCIE_CLIENT_PORT_BDF	0x0274	W	0x00000000	Port BDF Register
PCIE_CLIENT_LTSSM_STATUS	0x0300	W	0x00000000	LTSSM Status Register
PCIE_CLIENT_DBG_FIFO_MODE_CON	0x0310	W	0x00000000	Debug FIFO Mode Control Register
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0	0x0320	W	0x00000000	Debug FIFO Pattern hit Data Register 0
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1	0x0324	W	0x00000000	Debug FIFO Pattern hit Data Register 1
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0	0x0328	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 0
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1	0x032C	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 1
PCIE_CLIENT_DBG_FIFO_STATUS	0x0350	W	0x00000000	Debug FIFO Status Register

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_CFG_ERR_STATUS	0x0354	W	0x00000000	Configuration Error Status
PCIE_CLIENT_TLP_PRFX_LOG0	0x0380	W	0x00000000	TLP Prefixes Log Register 0
PCIE_CLIENT_TLP_PRFX_LOG1	0x0384	W	0x00000000	TLP Prefixes Log Register 1
PCIE_CLIENT_TLP_PRFX_LOG2	0x0388	W	0x00000000	TLP Prefixes Log Register 2
PCIE_CLIENT_TLP_PRFX_LOG3	0x038C	W	0x00000000	TLP Prefixes Log Register 3
PCIE_CLIENT_CLIENT_VER	0x0800	W	0x00050610	Client Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.2.2 PCIE_CLIENT Detail Registers Description

PCIE_CLIENT_GENERAL_CON

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	mem_auto_clk_gating_disable Control the memory auto clock gating when it is inactive. 1'b0: Auto gating enable 1'b1: Auto gating disable
13	RW	0x0	link_req_rst_grt_sel Link down reset request grant control select: 1'b1: From client grf GENERAL_CON bit 3 1'b0: From pcie grf PCIE_CON0 bit 2 Reserved after r5p6 (version 50600).
12	R/W SC	0x0	app_hdr_valid Alias "app_err_report" in old client version. One-clock-cycle pulse indicating that the data app_hdr_log, app_err_bus, app_err_func_num, and app_tlp_prfx_log is valid. Set 1 to report application error to controller. It is a self-clear bit to generate a pulse to controller. Application should provide error information in VEN_ERR_INFOx registers before setting this bit.
11	RW	0x0	app_sris_mode SRIS operating mode 1'b0: non-SRIS mode 1'b1: SRIS mode
10	RW	0x0	app_dbi_ro_wr_disable DBI Read-only Write Disable 1'b0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. 1'b1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only

Bit	Attr	Reset Value	Description
9	RW	0x0	tx_lane_flip_en Performs manual lane reversal for transmit lanes. For use whenautomatic lane reversal does not occur because lane 0 is not detected. In most cases, tx_lane_flip_en should be wired to a static value at thechip level. For more information, see 'Lane Reversal and Broken Lanes'. This signal is only used in Conventional PCIe mode. When in M-PCIe mode, mpcie_tx_lane_flip_en is used. 1'b0: Disable 1'b1: Enable
8	RW	0x0	rx_lane_flip_en Performs manual lane reversal for receive lanes. For use when automatic lane reversal does not occur because lane 0 is not detected. In most cases, rx_lane_flip_en should be wired to a static value at the chip level. For more information, see 'Lane Reversal and Broken Lanes'. This signal is only used in Conventional PCIe mode. When in M-PCIe mode, mpcie_rx_lane_flip_en is used. 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	device_type Device/port type. Indicates the specific type of this PCI Express function. It is also used to set the 'Device/Port Type' field of the 'PCI Express Capabilities Register'. The controller uses this input to determine the operating mode of the controller at run time. Defined encodings are: 4'h0: PCI Express endpoint 4'h1: Legacy PCI Express endpoint 4'h4: Root port of PCI Express root complex
3	RW	0x0	link_req_rst_grt Link down reset request grant control. 1'b0: Disable link down reset request grant 1'b1: Enable link down reset request grant Reserved after r5p6(version 50600).
2	RW	0x0	app_ltssm_enable Driven low by your application after cold, warm, or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin. When your application has finished reprogramming the controller configuration registers using the DBI, it asserts app_ltssm_enable to allow the LTSSM to continue link establishment. Can also be used to delay hot resetting of the controller until you have read out any register status.
1	RW	0x0	app_req_retry_en Provides a capability to defer incoming configuration requests until initialization is complete. When app_req_retry_en is asserted, the controller completes incoming configuration requests with a configuration request retry status. Other incoming requests are not affected. When the Readiness Notification mechanism is supported, DRS messaging is blocked when app_req_retry_en=1. When app_req_retry_en=0 and app_drs_ready=1, the controller autonomously transmits a DRS message when the link transitions from DL_Down to DL_Up.

Bit	Attr	Reset Value	Description
0	R/W SC	0x0	app_init_rst Request from your application to send a hot reset to the upstream port. The hot reset request is sent when a single cycle pulse is applied to this pin. In an upstream port, you should set this input to '0'.

PCIE_CLIENT_INTR_STATUS_MSG_RX

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	W1 C	0x0	obff_cpu_active_int Interrupt indicates that the controller received an 'CPU Active' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. One-clock-cycle pulse that indicates that the controller received a 'CPU Active' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
13	W1 C	0x0	obff_obff_int Interrupt indicates that the controller received an 'OBFF' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. if cfg_obff_en is not equal to 2'b11, then radm_msg_obff One-clock-cycle pulse that indicates that the controller received an 'OBFF' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
12	W1 C	0x0	obff_idle_int Interrupt indicates that the controller received an 'IDLE' OBFF message. 1'b0: No interrupt 1'b1: Interrupt EP only. if cfg_obff_en is not equal to 2'b11, then radm_msg_idle One-clock-cycle pulse that indicates that the controller received an 'IDLE' OBFF message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message. Only usable in an upstream port.
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	W1C	0x0	pm_turnoff_int Interrupt indicates that the controller received a PME Turnoff message. 1'b0: No interrupt 1'b1: Interrupt EP mode only. radm_pm_turnoff One-clock-cycle pulse that indicates that the controller received a PME Turnoff message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no indication is given for the second message.
9	W1C	0x0	pm_to_ack_int Interrupt indicates that the controller received a PME_TO_Ack message. 1'b0: No interrupt 1'b1: Interrupt RC mode only. radm_pm_to_ackOne-clock-cycle pulse that indicates that the controller received a PME_TO_Ack message. Upstream port: Reserved.
8	W1C	0x0	pm_pme_int Interrupt indicates that the controller received a PM_PME message. 1'b0: No interrupt 1'b1: Interrupt RC mode only. radm_pm_pme One-clock-cycle pulse that indicates that the controller received a PM_PME message.
7:6	RO	0x0	reserved
5	W1C	0x0	cfg_pme_msi_int Interrupt that indicates the controller received a cfg_pme_msi pulse. 1'b0: No interrupt 1'b1: Interrupt cfg_pme_msi asserted when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. The PME Interrupt Enable bit in Root Control register is set to 1. 3. The PME Status bit in Root Status register is set to 1. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
4	RO	0x0	cfg_pme_int Asserted when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0. 2. The PME Interrupt Enable bit in the Root Control register is set to 1. 3. The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2	W1C	0x0	ltr_msg_int Interrupt that indicates the controller received a LTR message. The LTR message information is available in PL_LTR_LATENCY_OFF registers. 1'b0: No interrupt 1'b1: Interrupt radm_msg_ltr One-clock-cycle pulse that indicates that the controller received an LTR message. The controller makes the message header available the radm_msg_payload output. It is also available the app_ltr_latency output. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
1	W1C	0x0	unlock_msg_int Interrupt indicates that the controller received an unlock message. 1'b0: No interrupt 1'b1: Interrupt radm_msg_unlock One-cycle pulse that indicates that the controller received an Unlock message. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
0	W1C	0x0	ven_msg_int Interrupt that indicates radm_vendor_msg One-cycle pulse is received. The message header is available in VEN_MSG_RX_INFO registers. 1'b0: No interrupt 1'b1: Interrupt radm_vendor_msg One-cycle pulse that indicates the controller received a vendor-defined message. The controller makes the message header available the radm_msg_payload output. When FX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then both bits are asserted.

PCIE_CLIENT_INTR_STATUS_LEGACY

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	tx_intd_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTD Message to the upstream device. The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTD Message to the upstream device. The signal deassert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTD Message to the upstream device. EP mode only.

Bit	Attr	Reset Value	Description
6	RO	0x0	tx_intc_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTC Message to the upstream device. The signal assert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTC Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTC Message to the upstream device. The signal deassert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTC Message to the upstream device. EP mode only.
5	RO	0x0	tx_intb_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTB Message to the upstream device. The signal assert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTB Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTB Message to the upstream device. The signal deassert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTB Message to the upstream device. EP mode only.
4	RO	0x0	tx_inta_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTA Message to the upstream device. The signal assert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTA Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTA Message to the upstream device. The signal deassert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTA Message to the upstream device. EP mode only.
3	RO	0x0	rx_intd_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTD Message from the downstream device. radm_intd_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTD Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTD Message from the downstream device. radm_intd_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTD Message from the downstream device. RC mode only.

Bit	Attr	Reset Value	Description
2	RO	0x0	rx_intc_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTC Message from the downstream device. radm_intc_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTC Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTC Message from the downstream device. radm_intc_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTC Message from the downstream device. RC mode only.
1	RO	0x0	rx_intb_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTB Message from the downstream device. radm_intb_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTB Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTB Message from the downstream device. radm_intb_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTB Message from the downstream device. RC mode only.
0	RO	0x0	rx_inta_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTA Message from the downstream device. radm_inta_asserted One-clock-cycle pulse that indicates that the controller received an Assert_INTA Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTA Message from the downstream device. radm_inta_deasserted One-clock-cycle pulse that indicates that the controller received a Deassert_INTA Message from the downstream device. RC mode only.

PCIE_CLIENT_INTR_STATUS_ERR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	W1C	0x0	radm_qoverflow_int Pulse radm_qoverflow indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism 1'b0: No interrupt 1'b1: Interrupt
11	RO	0x0	reserved
10	W1C	0x0	f_err_rx_int One-clock-cycle radm_fatal_err pulse that indicates that the controller received an ERR_FATAL message. 1'b0: No interrupt 1'b1: Interrupt RC mode only.

Bit	Attr	Reset Value	Description
9	W1C	0x0	nf_err_rx_int One-clock-cycle radm_nonfatal_err pulse that indicates that the controller received an ERR_NONFATAL message. 1'b0: No interrupt 1'b1: Interrupt RC mode only.
8	W1C	0x0	cor_err_rx_int One-clock-cycle radm_correctable_err pulse that indicates that the controller received an ERR_COR message. The controller makes the message header available the radm_msg_payload output. 1'b0: No interrupt 1'b1: Interrupt RC mode only.
7	RO	0x0	reserved
6	W1C	0x0	f_err_sent_int cfg_send_f_err indicates Sent Fatal Error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained a fatal error, and that can not be corrected, has been received by the EndPoint. 1'b0: No interrupt 1'b1: Interrupt EP mode only.
5	W1C	0x0	nf_err_sent_int cfg_send_nf_err indicates Sent Non-Fatal Error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained a non-fatal error, and that can not be corrected, has been received by the EndPoint. 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	cor_err_sent_int cfg_send_cor_err indicates sent correctable error. Controller has sent a message towards the Root Complex indicating that an Rx TLP that contained an error, and that can be corrected, has been received by the EndPoint 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	tx_cpl_timeout_int trgt_cpl_timeout indicates that the application has not generated a completion for an incoming request within the required time interval. Information about the timed-out completion is available the trgt_timeout_* outputs listed later. When a completion timeout occurs, the controller does not clear the corresponding entry from the completion lookup table. The default completion timeout value is approximately 10 ms. 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	rx_cpl_timeout_int radm_cpl_timeout indicates that the completion TLP for a request has not been received within the expected time window. 1'b0: No interrupt 1'b1: Interrupt Can find the timed-out completion information in RX_CPL_TIME_OUT_INFO register.

Bit	Attr	Reset Value	Description
1	W1C	0x0	aer_rc_err_msi The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. A reported error condition causes a bit to be set in the Root Error Status register. 3. The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. RC mode only.
0	RO	0x0	aer_rc_err_int Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred. Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi. RC mode only.

PCIE_CLIENT_INTR_STATUS_MISC

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ep_elbi_app_int Interrupt generated by ELBI application register access. 1'b0: No interrupt 1'b1: Interrupt
14	RO	0x0	link_eq_req_int Interrupt indicating to your application that the Link Equalization Request bit in the Link Status 2 Register has been set and the Link Equalization Request Interrupt Enable (Link Control 3 Register bit 1) is set. cfg_link_eq_req_int 1'b1: Interrupt 1'b0: No interrupt
13	W1C	0x0	rbar_update_int Indicates that a resizable BAR control register has been updated: 1 bit per Physical function. 1'b0: No interrupt 1'b1: Interrupt

Bit	Attr	Reset Value	Description
12	W1C	0x0	dpa_sub_upd_int DPA Substate-Updated Indication Signal Bus. The controller asserts "dpa_substate_update" for one core_clk cycle when the Substate Control field of the DPA Control Register has been updated with a new value for the associated function. The controller asserts it when the updated value of the Substate Control field does not match the Substate Status field of the Status Register when the Substate Control Enable bit field of the Status Register is set to "1". Note: Your application logic is required to do the following: 1. Detect the one cycle pulse on the signal for the relevant function. 2. Read the function's substate control register to determine the software's target substate (transition). 3. Read the function's transition latency value, unit, and indicator. Calculate the maximum transition latency for the substate transition. 4. Execute the substate transition and complete it within the maximum transition latency. 5. Update the substate status after completing the transition through a DBI write. The controller updates the substate status during the substate transition if the transition is from a lower power substate to a higher; the status is the higher power substate during the substate transition.
11	RO	0x0	edma_rd_int DMA read channel interrupt. Indicates that the DMA transfer has completed or that an error has occurred. This is a level interrupt. For more information, see 'Interrupts and Error Handling'. 1'b0: No interrupt 1'b1: Interrupt
10	RO	0x0	edma_wr_int DMA write channel interrupt. Indicates that the DMA transfer has completed or that an error has occurred. This is a level interrupt. For more information, see 'Interrupts and Error Handling'. 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	bw_mgt_msi The controller sets this pin when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Bandwidth Management Status register (Link Control Status register bit 14) is updated 3. The Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set. reuse-pragma begin Attr Description This pin is set as a notification when the Link Bandwidth Management Status register (Link Status register bit 14) is updated and the Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set and in addition the msi or msix are enabled . This bit is not applicable to, and is reserved, for endpoint devices and upstream ports of Switches. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.

Bit	Attr	Reset Value	Description
8	RO	0x0	bw_mgt_int The controller asserts cfg_bw_mgt_int when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0, and 2. The Bandwidth Management Interrupt Enable bit in the Link Control register is set to 1, and 3. The Bandwidth Management Interrupt Status bit in the Link Status register is set to 1. The cfg_bw_mgt_msi output is a pulse signal (only asserted for one clock cycle); but cfg_bw_mgt_int is a level signal. For upstream port: Reserved.
7	W1C	0x0	link_auto_bw_msi The controller sets this pin when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Autonomous Bandwidth Status register (Link Status register bit 15) is updated. 3. The Link Autonomous Bandwidth Interrupt Enable (Link Control register bit 11) is set. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.
6	RO	0x0	link_auto_bw_int The controller asserts cfg_link_auto_bw_int when all of the following conditions are true: 1. The INTx assertion disable bit in the Command register is 0, and 2. The Link Autonomous Bandwidth Interrupt Enable bit in the Link Control register is set to 1, and 3. The Link Autonomous Bandwidth Interrupt Status bit in the Link Status register is set to 1. The cfg_link_auto_bw_msi output is a pulse signal (only asserted for one clock cycle); but cfg_link_auto_bw_int is a level signal. For upstream port: Reserved.
5	W1C	0x0	hp_msi The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: 1. MSI or MSI-X is enabled. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).

Bit	Attr	Reset Value	Description
4	RO	0x0	hp_int The controller asserts hp_int when all of the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.
3	W1C	0x0	hp_pme_int The controller asserts hp_pme when all of the following conditions are true: 1. The PME Enable bit in the Power Management Control and Status register is set to 1. 2. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled.
2	W1C	0x0	link_req_rst_not_int Early version of the link_req_rst_not signal. For more information, see the 'Warm and Hot Resets' section in the Architecture chapter of the Databook. smlh_req_rst_not. 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	dll_link_up_int Data link layer up/down indicator (rdlh_link_up): This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Link is down 1'b1: Link is up
0	W1C	0x0	phy_link_up_int PHY "smlh_link_up" Link up/down indicator. 1'b0: Link is down 1'b1: Link is up

PCIE_CLIENT_INTR_STATUS_PMC

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	W1C	0x0	pm_dstate_update_int Interrupt indicates that the current power management D-state have changed. The current power management D-state of pm_dstate the function: 1. 000b: D0 2. 001b: D1 3. 010b: D2 4. 011b: D3 5. 100b: Uninitialized 6. Other values: Not applicable There are 3 bits of pm_dstate for each configured function. 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	linkst_out_l0s_int Power management is in L0s state. Indicates in L0_STALL state when M-PCIe Interrupt that indicates link has entered L0s state (falling edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	linkst_out_l2_int Power management is in L2 state. Interrupt that indicates link has entered L2 state (falling edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	linkst_out_l1_int Power management is in L1 state. Interrupt that indicates link has entered L1 state (falling edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	linkst_out_l1sub_int Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used in DWC_pcie_clkrst.v (see 'Clock Generation and Gating Design Example') to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. Interrupt indicates link has entered L1 substate (falling edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	linkst_in_l0s_int Power management is in L0s state. Indicates in L0_STALL state when M-PCIe Interrupt that indicates link has entered L0s state (rising edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt

Bit	Attr	Reset Value	Description
2	W1C	0x0	linkst_in_l2_int Power management is in L2 state. Interrupt that indicates link has entered L2 state (rising edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	linkst_in_l1_int Power management is in L1 state. Interrupt that indicates link has entered L1 state (rising edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	linkst_in_l1sub_int Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used in (see 'Clock Generation and Gating Design Example') to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. Interrupt indicates link has entered L1 substate (rising edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: No interrupt 1'b1: Interrupt

PCIE_CLIENT_INTR_MASK_MSG_RX
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	obff_cpu_active_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
13	RW	0x1	obff_obff_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
12	RW	0x1	obff_idle_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RO	0x0	reserved
10	RW	0x1	pm_turnoff_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	pm_to_ack_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

Bit	Attr	Reset Value	Description
8	RW	0x1	pm_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7:6	RO	0x0	reserved
5	RW	0x1	cfg_pme_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	cfg_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RO	0x0	reserved
2	RW	0x1	ltr_msg_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	unlock_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	ven_msg_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_LEGACY
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	tx_intd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	tx_intc_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	tx_intb_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	tx_inta_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	rx_intd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

Bit	Attr	Reset Value	Description
2	RW	0x1	rx_intc_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	rx_intb_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	rx_inta_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_ERR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	radm_qoverflow_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RO	0x0	reserved
10	RW	0x1	f_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	nf_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
8	RW	0x1	cor_err_rx_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7	RO	0x0	reserved
6	RW	0x1	f_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	nf_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	cor_err_sent_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	tx_cpl_timeout_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

Bit	Attr	Reset Value	Description
2	RW	0x1	rx_cpl_timeout_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	aer_rc_err_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	aer_rc_err_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_MISC
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	ep_elbi_app_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
14	RW	0x1	link_eq_req_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
13	RW	0x1	rbar_update_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
12	RW	0x1	dpa_sub_upd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
11	RW	0x1	edma_rd_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
10	RW	0x1	edma_wr_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
9	RW	0x1	bw_mgt_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
8	RW	0x1	bw_mgt_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

Bit	Attr	Reset Value	Description
7	RW	0x1	link_auto_bw_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	link_auto_bw_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
5	RW	0x1	hp_msi_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	hp_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	hp_pme_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	link_req_rst_not_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	dll_link_up_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	phy_link_up_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_INTR_MASK_PMC

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	pm_dstate_update_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
7	RW	0x1	linkst_out_l0s_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
6	RW	0x1	linkst_out_l2_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

Bit	Attr	Reset Value	Description
5	RW	0x1	linkst_out_l1_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
4	RW	0x1	linkst_out_l1sub_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
3	RW	0x1	linkst_in_l0s_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
2	RW	0x1	linkst_in_l2_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
1	RW	0x1	linkst_in_l1_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask
0	RW	0x1	linkst_in_l1sub_int_mask Mask bit of interrupt. 1'b0: Interrupt unmask 1'b1: Interrupt mask

PCIE_CLIENT_POWER_CON
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_req_n_con Valid when clk_req_n_bypass set to 1. 1'b1: Tristate CLKREQ# 1'b0: Pull down CLKREQ#
12	RW	0x0	clk_req_n_bypass 1'b0: clk_req_n does not bypass, CLKREQ# driven by controller 1'b1: clk_req_n bypass, CLKREQ# driven by bit 13 of POWER_CON
11:10	RW	0x0	p2_cpm_disable 2'b00: When phy in P2 power state, enable clock PM for both L1 and L2 2'b01: When phy in P2 power state, enable clock PM for L2 but disable for L1 2'b10: When phy in P2 power state, disable clock PM for L2 but enable for L1 2'b11: When phy in P2 power state, disable clock PM for both L1 and L2 Reserved after r5p6(version 50600).

Bit	Attr	Reset Value	Description
9	RW	0x0	app_clk_pm_en Clock PM feature enabled by application. Used to inhibit the programming of the Clock PM in Link Control Register. For more information, see 'L1 with Clock PM (L1 with REFCLK removal/PLL Off)'.
8	RW	0x0	sys_aux_pwr_det Auxiliary Power Detected. Used to report to the host software that auxiliary power (Vaux) is present. 1'b0: Auxiliary power is not present 1'b1: Auxiliary power is present
7	RO	0x0	reserved
6	RW	0x0	app_l1sub_disable The application can set this input to 1'b1 to prevent entry to L1 Sub-states. This pin is used to gate the L1 sub-state enable bits from the L1 PM Substates Control 1 Register.
5	RW	0x0	app_xfer_pending Indicates that your application has transfers pending. 1'b1: There are transactions outside the controller that the controller needs to transmit. For EP mode, prevents generation of requests to enter L1. Triggers exit if already in L1. For RC mode, triggers exit if already in L1. 1'b0: There are no transactions outside the controller. Indicates that your application has transfers pending and prevents the controller from entering L1. If the entry into L1 is already in progress, assertion of app_xfer_pending causes an exit from L1. This is a level signal used to inform the controller about the state of external queues and pipeline stages that contain transactions to be transmitted by the controller. The controller uses this information to determine when to enter/exit L1. When this signal is asserted, it indicates that there are transactions outside the controller that the controller needs to transmit. When de-asserted, it indicates that there are no transactions outside the controller. The controller responds to an assertion on this signal as follows: 1. Upstream Ports: Prevents generation of requests to enter L1. Triggers exit if already in L1. 2. Downstream Ports: Triggers exit if already in L1. You can instruct the controller to exit L1 by asserting either or both of app_xfer_pending and app_req_exit_l1. The controller only samples app_req_exit_l1 when the controller is already in the L1 state.
4	R/W SC	0x0	app_req_exit_l1 1'b0: Self clear to generate a pulse to controller. 1'b1: Application request to Exit L1. Application request to Exit L1. Request from your application to exit L1. It is only effective when L1 is enabled.

Bit	Attr	Reset Value	Description
3	RW	0x1	app_ready_entr_l23 1'b0: Application not ready to enter L23. 1'b1: Application ready to enter L23. Application Ready to Enter L23. Indication from your application that it is ready to enter the L23 state. The app_ready_entr_l23 signal is provided for applications that must control L23 entry (in case certain tasks must be performed before going into L23). The controller delays sending PM_Enter_L23 (in response to PM_Turn_Off) until this signal becomes active. When this signal has been asserted by the application, it must be kept asserted until L2 entry has completed. Hardwire to 1 for applications that do not require this feature. Note: The controller ignores this input in RC mode.
2	R/W SC	0x0	app_req_entr_l1 Application request to Enter L1 ASPM state. 1'b0: Self clear to generate a pulse to controller 1'b1: Application request to enter L1 state Application request to Enter L1 ASPM state. The app_req_entr_l1 signal is for use by applications that need to control L1 entry instead of using the L1 entry timer as defined in the PCI Express Specification. It is only effective when L1 is enabled. The controller latches this request when in L0 or L0s; to be acted upon later. Note: The controller ignores this input in RC mode.
1	R/W SC	0x0	app_pm_xmt_pme Wake Up. If PME is enabled and PME support is configured for current PMCSR D-state asserting this signal (apps_pm_xmt_pme) causes the controller to wake from either L1 or L2 state. When the controller has transitioned back to the L0 state it transmits a PME message and set the PME_Status. Upon receiving the PME message the root complex should clear the PME_Status and change the D-state back to D0.
0	RW	0x0	app_clk_req_n Indicates that the application logic is ready to have reference clock removed. In designs which support reference clock removal through either L1 PM Sub-states or L1 CPM, the application should set this signal to 1'b1 if it supports reference clock removal. If the application does not want to remove reference clock it should set this signal to 1'b0. This signal should be asserted or de-asserted when L1 CPM or L1 Sub-states are being configured, it should not be changed dynamically during L1. Indicates that the application is ready to have reference clock removed. 1'b0: Application does not want to remove reference clock 1'b1: Application is ready to have reference clock removed

PCIE_CLIENT_POWER_STATUS

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	pm_clkreq_in Status of wire CLKREQ# GPIO.
27	RO	0x0	pm_clkreq_out Status of CLKREQ# output drive signal.

Bit	Attr	Reset Value	Description
26	RO	0x0	pm_wake_in Status of wire WAKE# GPIO.
25	RO	0x0	pm_wake_out The wake state of the wake_out 1'b0: Controller is not in wake process or Link already back to L0 1'b1: Controller assert WAKE# signal to request to make link back to L0 EP only.
24	RO	0x0	pm_linkst_in_l0s Power management is in L0s state. 1'b0: Power management is not in L0s. 1'b1: Power management is in L0s.
23	RO	0x0	pm_linkst_in_l2 Power management is in L2 state. 1'b0: Power management is not in L2 1'b1: Power management is in L2
22	RO	0x0	pm_linkst_in_l1 Power management is in L1 state. 1'b0: Power management is not in L1 1'b1: Power management is in L1
21	RO	0x0	pm_linkst_in_l1sub Power management is in L1 substate. Indicates when the link has entered L1 substates. It is used in (see 'Clock Generation and Gating Design Example') to ensure that the switching back of aux_clk from AUXCLK to PCLK occurs only after L1 substates have been exited. For L1.2 this signal is de-asserted at the end of the L1.2.Exit state, after the t_power_on constraint has been satisfied. External logic can use the transition high to low on this signal to initiate REFCLK restore. 1'b0: Power management is not in L1 substate 1'b1: Power management is in L1 substate
20	RO	0x0	reserved
19:17	RO	0x0	pm_l1sub_state Power management L1 sub-states FSM state. For debugging purposes, not for system operation. 3'b000: L1_U 3'b001: L1_0 3'b010: L1_0_WAIT4_ACK 3'b011: L1_0_WAIT4_CLKREQ 3'b100: L1_N_ENTRY 3'b101: L1_N 3'b110: L1_N_EXIT 3'b111: L1_N_ABORT
16:15	RO	0x0	reserved
14:10	RO	0x00	pm_slave_state Power management slave FSM state. For debugging purposes, not for system operation.
9	RO	0x0	reserved
8:4	RO	0x00	pm_master_state Power management master FSM state. For debugging purposes, not for system operation.
3	RO	0x0	reserved
2:0	RO	0x0	pm_curnt_state Indicates the current power state. For debugging purposes, not for system operation.

PCIE_CLIENT_MSG_GEN_CON

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	R/W SC	0x0	obff_cpu_active_msg_req Request controller to generate a "CPU Active" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
13	R/W SC	0x0	obff_obff_msg_req Request controller to generate a "OBFF" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
12	R/W SC	0x0	obff_idle_msg_req Request controller to generate a "IDLE" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
11:9	RO	0x0	reserved
8	R/W SC	0x0	app_ltr_msg_req Indicates that your application is requesting to send an LTR message. Once asserted, app_ ltr_msg_req must remain asserted until the controller asserts app_ltr_msg_grant. Set to request controller to send a LTR Message. This bit clears automatically when request is granted by controller. Application should put LTR message information ready in LTR_MSG_TX_INFO register before setting this bit.
7:6	RO	0x0	reserved
5	R/W SC	0x0	app_unlock_msg Request from your application to generate an Unlock message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
4	R/W SC	0x0	apps_pm_xmt_turnoff Request from your application to generate a PM_Turn_Off message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	legacy_int_req When legacy_int_req (sys_int) goes from low to high, the controller generates an Assert_INTx Message. When sys_int goes from high to low, the controller generates a Deassert_INTx Message. There is a separate sys_int input bit for each function in your controller configuration. The Interrupt Pin register for the corresponding function determines which INTx Message the controller generates (INTA, INTB, INTC, or INTD). Legacy and native PCIe devices capable of generating an interrupt must support both Assert_INTx/Deassert_INTx and MSI or MSI-X. sys_int is intended to generate a message that emulates the legacy PCI Interrupts.
0	R/W SC	0x0	ven_msg_req Set to request controller to send a vendor-defined Message. This bit clears automatically when request is granted by controller. Application should put vendor message information ready in VEN_MSG_TX_CFGx registers before setting this bit. Request from your application to send a vendor-defined Message. Once asserted, ven_msg_req must remain asserted until the controller asserts ven_msg_grant.

PCIE_CLIENT_MSI_GEN_CON
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	R/W SC	0x00000000	msi_gen_req 32 bits write only MSI generation request signals. MSB has the highest priority and LSB has the lowest priority. Write 1 to a certain bit request the controller send a MSI interrupt. Software should use MSI capability register to access MSI mask or pending status.

PCIE_CLIENT_MSI_GEN_FNUM_TC
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	ven_msi_tc Traffic Class of the MSI request, valid when ven_msi_req is asserted.
3	RO	0x0	reserved
2:0	RW	0x0	ven_msi_func_num The function number of the MSI request.

PCIE_CLIENT_RBAR_SIZE_INFO0
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	bar2_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RO	0x00	bar1_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
7:6	RO	0x0	reserved
5:0	RO	0x00	bar0_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.

PCIE_CLIENT_RBAR_SIZE_INFO1
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	bar5_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
15:14	RO	0x0	reserved
13:8	RO	0x00	bar4_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.
7:6	RO	0x0	reserved
5:0	RO	0x00	bar3_size_info BAR size field from each of the resizable BAR control registers, per function. For BARs that are not resizable the corresponding bits in cfg_rbar_size is set to 0.

PCIE_CLIENT_DMA_HSHAKE_TOGG
Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	dma_rdxfer_done_togg DMA read engine descriptor transfer done toggle signal. One bit for each implemented DMA read channel. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles.
11:8	RO	0x0	dma_wdxfer_done_togg DMA write engine descriptor transfer done toggle signal. One bit for each implemented DMA write channel. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles.
7:4	RW	0x0	app_rdxfer_go_togg DMA read engine descriptor transfer go toggle signal. One bit for each implemented DMA read channel. This signal is ignored whenever a DMA channel operates in non-linked mode.
3:0	RW	0x0	app_wdxfer_go_togg DMA Write engine descriptor transfer go toggle signal. One bit for each implemented DMA write channel. This signal is ignored whenever a DMA channel operates in non-linked mode.

PCIE_CLIENT_VEN_MSG_RX_INFO0
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	ven_msg_req_id The requester ID of the received Message(radm_msg_req_id). Bit[15:8]: Bus number Bit[7:3]: Device number Bit[2:0]: Function number

PCIE_CLIENT_VEN_MSG_RX_INFO1
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_l The third double word of the Vendor Defined Message header. Received message header information. When a vendor-defined or ltr message is received (radm_vendor_msg=1 or radm_ltr_msg=1), the controller maps radm_msg_payload to the Rx TLP header dwords as follows: When RX_TLP =1 Bit[31:0] = bytes 12-15 (4th dword), where [7:0] =byte 15 Bit[63:32] = bytes 8-11 (3rd dword)

PCIE_CLIENT_VEN_MSG_RX_INFO2
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_h The fourth double word of the Vendor Defined Message header. Received message header information. When a vendor-defined or ltr message is received (radm_vendor_msg=1 or radm_ltr_msg=1), the controller maps radm_msg_payload to the Rx TLP header dwords as follows: When RX_TLP =1 Bit[31:0] = bytes 12-15 (4th dword), where [7:0] =byte 15 Bit[63:32] = bytes 8-11 (3rd dword)

PCIE_CLIENT_VEN_MSG_TX_CFG0
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	ven_msg_code The Message Code for the vendor-defined Message TLP.
23:16	RW	0x00	ven_msg_tag Tag for the vendor-defined Message TLP.
15:11	RO	0x00	reserved
10:9	RW	0x0	ven_msg_attr The Attributes field for the vendor-defined Message TLP. bit1: Relaxed ordering. bit0: No snoop.
8	RW	0x0	ven_msg_ep The Poisoned TLP (EP) bit for the vendor-defined Message TLP.
7:5	RW	0x0	ven_msg_tc The Traffic Class field for the vendor-defined Message TLP.
4:0	RW	0x00	ven_msg_type The TYPE field for the vendor-defined Message TLP.

PCIE_CLIENT_VEN_MSG_TX_CFG1
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_l The third double word of the Vendor Defined Message header. Third and fourth dwords of the Vendor Defined Message header where: 1. Bytes 8-11 (third header dword) =ven_msg_data[63:32] 2. Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15 For more information, see the 'Endianness' advanced information chapter.

PCIE_CLIENT_VEN_MSG_TX_CFG2
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_h The fourth double word of the Vendor Defined Message header. Third and fourth dwords of the Vendor Defined Message header where: 1. Bytes 8-11 (third header dword) =ven_msg_data[63:32] 2. Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15 For more information, see the 'Endianness' advanced information chapter.

PCIE_CLIENT_LTR_MSG_TX_INFO
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_ltr_msg_latency LTR message that your application is requesting to send. The message format is defined in the PCI Express Specification.

PCIE_CLIENT_APP_ERR_RPT_INFO0
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log0 The header(bit 0 to bit 31) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO1
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log1 The header(bit 32 to bit 63) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO2
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log2 The header(bit 64 to bit 95) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO3
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_hdr_log3 The header (bit 96 to bit 127) of the TLP that contained the error. The header of the TLP that contained the error indicated app_err_bus, valid when 1. app_hdr_valid is asserted. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register.

PCIE_CLIENT_APP_ERR_RPT_INFO4
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	app_err_advisory Indicates that your application error is an advisory error. Your application should assert app_err_advisory under either of the following conditions: 1. The controller is configured to mask completion timeout errors, your application is reporting a completion timeout error app_err_bus, and your application intends to resend the request. In such cases the error is an advisory error, as described in PCI Express Specification. When your application does not intend to resend the request, then your application must keep app_err_advisory de-asserted when reporting a completion timeout error. 2. The controller is configured to forward poisoned TLPs to your application and your application is going to treat the poisoned TLP as a normal TLP, as described in PCI Express Specification. Upon receipt of a poisoned TLP, your application must report the error app_err_bus, and either assert app_err_advisory (to indicate an advisory error) or de-assert app_err_advisory (to indicate that your application is dropping the TLP). For more information, see the PCI Express Specification to determine when an application error is an advisory error. 1'b0: Application error is not an advisory error 1'b1: Application error is an advisory error
15:13	RO	0x0	reserved
12:0	RW	0x0000	app_err_bus The type of error that application detected. The controller combines the values err_bus bits with the internally detected error signals to set the corresponding bit in the Un-correctable or Correctable Error Status Registers [0]: Malformed TLP [1]: Receiver Overflow [2]: Unexpected completion [3]: Completer abort [4]: Completion Timeout [5]: Unsupported request [6]: ECRC Check Failed [7]: Poisoned TLP received [8]: AtomicOp Egress Blocked [9]: Un-correctable Internal Error [10]: Corrected Internal Error [11]: TLP Prefix Blocked Error Status: only valid for RC and when CX_NPRFX >0 [12]: ACS Violation: only valid when CX_ACS_ENABLE =1 For more information, see 'Application Error Reporting Interface'.

PCIE_CLIENT_OBFF_WAKE_ELE_CFG

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0xb4	wk_min_f2f_wdt Configure the minimum falling edge to falling edge width. The minimum value Specification define is 700ns. Application set this value equals to wk_min_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).

Bit	Attr	Reset Value	Description
23:16	RW	0xf0	wk_max_f2f_wdt Configure the maximum falling edge to falling edge width. The maximum value Specification define is 1000ns. Application set this value equals to wk_max_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
15:8	RW	0x50	wk_mim_pls_wdt Configure the minimum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The minimum value Specification define is 300ns. Application set this value equals to wk_mim_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
7:0	RW	0x64	wk_max_pls_wdt Configure the maximum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The maximum value Specification define is 500ns. Application set this value equals to wk_max_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2). Setting this value less than 50% of {wk_max_f2f_wdt * core_clock_period}.

PCIE_CLIENT_OBFF_WAKE_DEBUG
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	obff_wake_dec_err Error state of OBFF decoder FSM, used for debug.
7:4	RO	0x0	obff_wake_dec_state Current state of OBFF decoder FSM, used for debug.
3	RW	0x0	obff_wake_dec_cpu 1'b0: Do not initialize to CPU ACTIVE state 1'b1: Initialize the OBFF decoder to CPU ACTIVE state when obff_wake_dec_init is set
2	RW	0x0	obff_wake_dec_obff 1'b0: Do not initialize to OBFF state 1'b1: Initialize the OBFF decoder to OBFF state when obff_wake_dec_init is set
1	RW	0x0	obff_wake_dec_idle 1'b0: Do not initialize to IDLE state 1'b1: Initialize the OBFF decoder to IDLE state when obff_wake_dec_init is set
0	RW	0x0	obff_wake_dec_init 1'b0: Do not initialize the OBFF decoder 1'b1: Initialize the OBFF decoder

PCIE_CLIENT_RX_CPL_TIME_OUT_INFO
Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	radm_timeout_cpl_tag The Tag field of the timeout completion (radm_timeout_cpl_tag).
23:12	RO	0x000	radm_timeout_cpl_len Length (in bytes) of the timeout completion. For a split completion, it indicates the number of bytes remaining to be delivered when the completion timeout (radm_timeout_cpl_len).
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:8	RO	0x0	radm_timeout_cpl_attr The Attributes field of the timeout completion (radm_timeout_cpl_attr).
7	RO	0x0	reserved
6:4	RO	0x0	radm_timeout_cpl_tc The Traffic Class of the timed-out completion (radm_timeout_cpl_tc).
3	RO	0x0	reserved
2:0	RO	0x0	radm_timeout_func_num The function Number of the timed-out completion (radm_timeout_func_num). Function numbering starts at '0'.

PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0
Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RO	0x000	trgt_timeout_cpl_len The Length of the timeout completion (trgt_timeout_cpl_len).
11:10	RO	0x0	reserved
9:8	RO	0x0	trgt_timeout_cpl_attr The Attributes value of the timeout completion (trgt_timeout_cpl_attr).
7	RO	0x0	reserved
6:4	RO	0x0	trgt_timeout_cpl_tc The TC of the timeout completion (trgt_timeout_cpl_tc).
3	RO	0x0	reserved
2:0	RO	0x0	trgt_timeout_func_num The function number of the timed-out completion. Function numbering starts at '0' (trgt_timeout_cpl_func_num).

PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	trgt_lookup_empty When this signal is asserted with radm_trgt1_hv, it indicates that the target completion LUT is not full. The application can use this signal to determine a back-pressure mechanism to the controller so that there is not an overflow condition when the number of outstanding non-posted transactions received is more than expected. Your application logic must drive trgt1_radm_halt with the logical OR of your application halt signal and the inverse of this output.
15:8	RO	0x00	trgt_lookup_id The target completion LUT lookup ID for the incoming request TLP. When using the optional target completion lookup table feature, the application must save the lookup ID and assert the same lookup ID client0/1/2_cpl_lookup_id when generating a completion for the request.
7:0	RO	0x00	trgt_timeout_lookup_id The target completion LUT lookup ID of the timeout completion

PCIE_CLIENT_LOCAL_CRU_CTRL
Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	radm_gate_disable Disable the radm_clk gating in local cru.
12	RW	0x0	aux_gate_disable Disable the aux_clk gating in local cru. Reserved after r5p6 (version 50600)
11	RW	0x0	link_down_gate_disable Disable the link down clock gating in local cru. Reserved after r5p6 (version 50600)
10	RW	0x0	dbi_aclk_gate_disable Disable the dbi_aclk gating in local cru. Reserved after r5p6 (version 50600)
9	RW	0x0	slv_aclk_gate_disable Disable the slv_aclk gating in local cru. Reserved after r5p6 (version 50600)
8	RW	0x0	mstr_aclk_gate_disable Disable the mstr_aclk gating in local cru. Reserved after r5p6 (version 50600)
7:4	RO	0x0	reserved
3	RW	0x0	pcie_pm_phy_req_disable Mask the phy reset request from controller pm. Reserved after r5p6 (version 50600)
2	RW	0x0	pcie_pm_srst_req_disable Mask the sticky reset request from controller pm. Reserved after r5p6 (version 50600)
1	RW	0x0	pcie_pm_nsrst_req_disable Mask the non-sticky reset request from controller pm. Reserved after r5p6 (version 50600)
0	RW	0x0	pcie_pm_crst_req_disable Mask the core reset request from controller pm. Reserved after r5p6 (version 50600)

PCIE_CLIENT_GENERAL_DEBUG_CON
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	sd_hold_ltssm app_ras_des_sd_hold_ltssm Hold and release LTSSM. For as long as this signal is '1', the controller stays in the current LTSSM. 1'b0: Release LTSSM 1'b1: Hold LTSSM

Bit	Attr	Reset Value	Description
5	RW	0x0	dbg_pba MSIX PBA RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the PBA. You can also use the MSIX_RAM_CTRL_DBG_PBA field in MSIX_RAM_CTRL_OFF to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire array linearly from the base address of the BAR (indicated by the BIR) in function 0. When you assert dbg_table and dbg_pba simultaneously, you can access the traffic class (TC) information bits. For more information, see the Interrupts section in the "Controller Operations" chapter of the Databook.
4	RW	0x0	dbg_table MSIX Table RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the Table. You can also use the MSIX_RAM_CTRL_DBG_TABLE field in MSIX_RAM_CTRL_OFF to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. When you assert dbg_table and dbg_pba simultaneously, you can access the traffic class (TC) information bits. For more information, see the Interrupts section in the "Controller Operations" chapter of the Databook.
3	RO	0x0	reserved
2:0	RW	0x0	diag_ctrl_bus Diagnostic Control Bus 1. x01: Insert LCRC error by inverting the LSB of LCRC 2. x10: Insert ECRC error by inverting the LSB of ECRC 2.1 The rising edge of these two signals ([1:0]) enable the controller to assert an LCRC or ECRC to the packet that it currently being transferred. 2.2 When LCRC or ECRC error packets are transmitted by the controller, the controller asserts diag_status_bus[lcrc_err_asserted] or diag_status_bus[ecrc_err_asserted] to report that the requested action has been completed. This handshake between control and status allows your application to control a specific packet being injected with an CRC or ECRC error. 2.3 The LCRC and ECRC errors are generated by simply inverting the last bit of the LCRC or ECRC value. 3. 1xx: Select Fast Link Mode. 3.1 Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation purposes. Forces the LTSSM training (link initialization) to use shorter timeouts and to link up faster. 3.2 The default scaling factor is 1024 for all internal timers. The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. 3.3 Fast Link Mode can also be activated by setting the FAST_LINK_MODE field in the PORT_LINK_CTRL_OFF register. 3.4 For more information, see the "Fast Link Simulation Mode" section in the "Integrating the Controller with the PHY or Application RTL or Verification IP" chapter of the User Guide.

PCIE_CLIENT_GENERAL_DEBUG_INFO
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	smlh_ltssm_state Current state of the LTSSM.
9	RO	0x0	reserved
8	RO	0x0	radm_q_not_empty Level indicating that the receive queues contain TLP header/data. 1'b0: Receive queues do not contain TLP header/data 1'b1: Receive queues contain TLP header/data
7	RO	0x0	radm_xfer_pending Receive request pending status. Indicates Receive TLP requests are pending, that is, requests sent to the RTRGT1 or RTRGT0 interfaces are awaiting a response from your application. For debugging purposes. 1'b0: Receive TLP requests are not pending 1'b1: Receive TLP requests are pending
6	RO	0x0	edma_xfer_pending eDMA transfer pending status. Indicates eDMA Write or Read Channel transfers are pending, that is, DMA Write or Read Channels have not finished transferring data. For debugging purposes. 1'b0: eDMA DBI transfer not pending 1'b1: eDMA transfer pending
5	RO	0x0	brdg_dbi_xfer_pending AXI Slave DBI transfer pending status. Indicates AXI DBI Slave Read or Write transfers are pending, that is, AXI Slave transfers are awaiting a response from the controller. For debugging purposes. 1'b0: AXI Slave DBI transfer not pending 1'b1: AXI Slave DBI transfer pending
4	RO	0x0	brdg_slv_xfer_pending AXI Slave non-DBI transfer pending status. Indicates AXI non-DBI Slave Read or Write transfers are pending, that is, AXI Slave transfers are awaiting a response from the controller. For debugging purposes. 1'b0: AXI Slave non-DBI transfer not pending 1'b1: AXI Slave non-DBI transfer pending
3	RO	0x0	reserved
2	RO	0x0	radm_idle RADM activity status signal. The controller creates the en_radm_clk_g output by gating this signal with the output of the RADM_CLK_GATING_EN field in the CLOCK_GATING_CTRL_OFF register. For debug purposes only. 1'b0: RADM is not idle in status 1'b1: RADM is in idle status
1	RO	0x0	rdlh_link_up Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Data link layer down 1'b1: Data link layer up

Bit	Attr	Reset Value	Description
0	RO	0x0	smlh_link_up PHY Link up/down indicator. 1'b0: PHY link is down 1'b1: PHY link is up

PCIE_CLIENT_SLC_DEBUG_INFO_CMN

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 78 bit of common silicon debug information: 3'b000: Select bit 15 to 0 3'b001: Select bit 31 to 16 3'b010: Select bit 47 to 32 3'b011: Select bit 63 to 48 3'b100: Select bit 79 to 64 Other: Reserved
27:16	RO	0x000	reserved
15:0	RO	0x0000	cdm_ras_des_sd_info_common Common debug signal bus that is used in RAS D.E.S. silicon debug Bit [78]: init_eq_pending_g4: Level: Equalization sequence Gen5 Bit [77:75]: l1sub_state: Level: L1 sub state Bit [74]: init_eq_pending_g4: Level: Equalization sequence Gen4 Bit [73]: init_eq_pending: Level: Equalization sequence Gen3 Bit [72:61]: xdlh_curnt_seqnum [11:0]: Level: Tx TLP SEQ# Bit [60:49]: rdlh_curnt_rx_ack_seqnum[11:0]: Level: Rx ACK SEQ# Bit [48]: rdlh_vc0_initfc2_status: Level: Init-FC Flag2 VC0 Bit [47]: rdlh_vc0_initfc1_status: Level: Init-FC Flag1 VC0 Bit [46:45]: rdlh_dlcntrl_state [1:0]: Level: DLCM Bit [44:37]: latched_ts_nfts[7:0]: Level: Latched NFTS Bit [36:34]: ltssm_powerdown[1:0]: Level: PIPE: Power Down Bit [33:18]: smlh_ltssm_variable [15:0]: Level: LTSSM Variable Bit [17]: pm_pme_resend_flag: Pulse: PME Re-Send flag Bit [16]: smlh_lane_reversed: Level: Lane Reversal Operation Bit [15:9]: rmlh_framing_err_ptr[6:0]: Pulse: 1st Framing Error Pointer Bit [8:5]: pm_slave_state[3:0]: Level: PM Internal State (Slave) Bit [4:0]: pm_master_state[4:0]: Level: PM Internal State (Master)

PCIE_CLIENT_SLC_DEBUG_INFO_LN

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 78 bit of Lane N silicon debug information: 3'b000: Select bit 15 to 0 3'b001: Select bit 31 to 16 3'b010: Select bit 47 to 32 3'b011: Select bit 63 to 48 3'b100: Select bit 79 to 64 Others: Reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x0	lane_sel cdm_ras_des_sd_info_li source selects 4'h0: Lane 0 4'h1: Lane 1 4'h2: Lane 2 4'h3: Lane 3
23:16	RO	0x00	reserved
15:0	RO	0x0000	cdm_ras_des_sd_info_li 16 of total 78-bit lane N silicon debug information, selected by bus_select field. [77:76]: eq_convergence_sts [1:0]: Level: Equalization convergence information Gen3 [75]: eqpa_violate_rule_123[2]: Level: Rule C Violation Event Status Gen3 [74]: eqpa_violate_rule_123[1]: Level: Rule B Violation Event Status Gen3 [73]: eqpa_violate_rule_123[0]: Level: Rule A Violation Event Status Gen3 [72]: mac_cdm_ras_des_reject_rtx: Level: Receive Reject Coefficient Event status Gen3 [71:64]: phy_cdm_ras_des_fomfeedback: Level: Current Figure of Merit Gen3 [63:61]: mac_cdm_ras_des_pset_lrx: Level: Current Local Receiver Preset Hint Gen3 [60:55]: mac_cdm_ras_des_coef_ltx[5:0]: Level: Current Local Transmitter Pre Cursor coefficient Gen3 [54:49]: mac_cdm_ras_des_coef_ltx[11:6]: Level: Current Local Transmitter Cursor coefficient Gen3 [48:43]: mac_cdm_ras_des_coef_ltx[17:12]: Level: Current Local Transmitter Post Cursor coefficient Gen3 [42:37]: mac_cdm_ras_des_coef_rtx[5:0]: Level: Current Remote Transmitter Pre Cursor coefficient Gen3 [36:31]: mac_cdm_ras_des_coef_rtx[11:6]: Level: Current Remote Transmitter Cursor coefficient Gen3 [30:25]: mac_cdm_ras_des_coef_rtx[17:12]: Level: Current Remote Transmitter Post Cursor coefficient Gen3 [24:19]: mac_cdm_ras_des_lf: Level: Remote Device LF Gen3 [18:13]: mac_cdm_ras_des_fs: Level: Remote Device FS Gen3 [12:5]: rmlh_deskew_fifo_ptr: Level: Deskew Pointer [4]: mac_phy_rxpolarity: Level: PIPE: RxPolarity [3]: latched_rxdetected: Level: PIPE: Detect Lane [2]: phy_mac_rxvalid_rxburst: Level: PIPE: RxValid/RxBurst [1]: phy_mac_rxelec_rxh8exit: Level: PIPE: RxElecIdle/RxHibern8ExitType1 [0]: mac_phy_txelec_txburst: Level: PIPE: TxElecIdle/TxBurst

PCIE_CLIENT_SLC_DEBUG_INFO_V0
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16bit of total 240 bit of virtual channel 0 silicon debug information: 4'd0: Select bit 15 to 0 4'd1: Select bit 31 to 16 ... 4'd14: Select bit 239 to bit 224 Other: Reserved
27:16	RO	0x000	reserved
15:0	RO	0x0000	cdm_ras_des_sd_info_vi 16 of total 240-bit l1 silicon debug information, selected by bus_select field. [239:228]: rtlh_fc_allctd_cpld: Level: Credit Allocated (CD) [227:220]: rtlh_fc_allctd_cplh: Level: Credit Allocated (CH) [219:208]: rtlh_fc_allctd_npd: Level: Credit Allocated (ND) [207:200]: rtlh_fc_allctd_nph: Level: Credit Allocated (NH) [199:188]: rtlh_fc_allctd_pd: Level: Credit Allocated (PD) [187:180]: rtlh_fc_allctd_ph: Level: Credit Allocated (PH) [179:168]: rtlh_fc_rcvd_cpld: Level: Credit Received (CD) [167:160]: rtlh_fc_rcvd_cplh: Level: Credit Received (CH) [159:148]: rtlh_fc_rcvd_npd: Level: Credit Received (ND) [147:140]: rtlh_fc_rcvd_nph: Level: Credit Received (NH) [139:128]: rtlh_fc_rcvd_pd: Level: Credit Received (PD) [127:120]: rtlh_fc_rcvd_ph: Level: Credit Received (PH) [119:108]: xadm_fc_limit_cpld: Level: Credit Limit (CD) [107:100]: xadm_fc_limit_cplh: Level: Credit Limit (CH) [99:88]: xadm_fc_limit_npd: Level: Credit Limit (ND) [87:80]: xadm_fc_limit_nph: Level: Credit Limit (NH) [79:68]: xadm_fc_limit_pd: Level: Credit Limit (PD) [67:60]: xadm_fc_limit_ph: Level: Credit Limit (PH) [59:48]: xadm_fc_cnsmd_cpld: Level: Credit Consumed (CD) [47:40]: xadm_fc_cnsmd_cplh: Level: Credit Consumed (CH) [39:28]: xadm_fc_cnsmd_npd: Level: Credit Consumed (ND) [27:20]: xadm_fc_cnsmd_nph: Level: Credit Consumed (NH) [19:8]: xadm_fc_cnsmd_pd: Level: Credit Consumed (PD) [7:0]: xadm_fc_cnsmd_ph: Level: Credit Consumed (PH)

PCIE_CLIENT_DIAG_STATUS_BUS_SEL
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	diag_bus_sel Select the 32bit of total 1024 bit of diag_status_bus that present on register DIAG_STATUS_BUS_INFO. 5'd0: bit 31 to 0 5'd1: bit 63 to 32 ... 5'd31: bit 1023 to 992

PCIE_CLIENT_DIAG_STATUS_BUS_INFO
Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	diag_status_bus 32 bit of total 1024-bit width diag_status_bus. Selected by DIAG_STATUS_BUS_SEL register. Contains all the important status signals from each controller module. Debug only.

PCIE_CLIENT_CDM_RASDES_EC_INFO_CON

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	cdm_rasdes_ec_info_lane_sel cdm_ras_des_ec_info_li source selects 4'h0: Lane 0 4'h1: Lane 1 4'h2: Lane 2 4'h3: Lane 3
3:0	RW	0x0	cdm_rasdes_ec_info_con Select the 32bit rasdes_ec_info_cmn 4'd0: Select bit 31 to 0 4'd1: Select bit 63 to 32 ..... Others: Reserved

PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cdm_ras_des_ec_info_common Common event signal bus that is used in RAS D.E.S. event counters

PCIE_CLIENT_CDM_RASDES_EC_INFO_LN

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	cdm_ras_des_ec_info_li Lanei event signal bus that is used in RAS D.E.S. event counters.

PCIE_CLIENT_CDM_RASDES_TBA_CON

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	app_ras_des_tba_ctrl Controls the start/end of time-based analysis. You must only set the pins to the required value for the duration of one clock cycle. This signal must be 2'b00 while the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register is controlled by the DBI interface or the accesses from the wire side. 2'b00: No action 2'b01: Start 2'b10: End. This setting is only used when the TIME_BASED_DURATION_SELECT field of TIME_BASED_ANALYSIS_CONTROL_REG is set to "manual control". 2'b11: Reserved These pins also set the contents of the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register.

PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	cdm_ras_des_tba_info_common Common event signal status bus used in RAS D.E.S. time-based analysis. Indicates the internal signals that are used in the time-based analysis. The results are in TIME_BASED_ANALYSIS_DATA_REG. Each bit indicates the state that the controller stays in. All signals are level sensitive unless otherwise indicated. [6]: smlh_link_in_training: Config/Recovery [5]: pm_in_l12: L1.2 [4]: pm_in_l11: L1.1 [3]: smlh_in_l1: L1 [2]: smlh_in_l0: L0 [1]: smlh_in_rl0s: Rx L0s [0]: smlh_in_l0s: Tx L0s

PCIE_CLIENT_HOT_RESET_CTRL

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	app_ltssm_enable_enhance Set "1" to enable ltssm_enbale enhance mode. Available after version 50600.
3	RW	0x0	app_dly2_done Set "1" to end the delaying of the link training after Hot Reset. This bit is self-cleared. Available after version 50600.
2	RW	0x0	app_dly1_done Set "1" to end the delaying of the controller Hot Reset. This bit is self-cleared. Available after version 50600.

Bit	Attr	Reset Value	Description
1	RW	0x0	app_dly2_en Set "1" to enable delaying the link training after Hot Reset Available after version 50600.
0	RW	0x0	app_dly1_en Set "1" to enable delaying the controller Hot Reset Available after version 50600.

PCIE_CLIENT_INTR_EN_MSG_RX

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	obff_cpu_active_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
13	RW	0x1	obff_obff_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
12	RW	0x1	obff_idle_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RO	0x0	reserved
10	RW	0x1	pm_turnoff_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	pm_to_ack_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	pm_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7:6	RO	0x0	reserved
5	RW	0x1	cfg_pme_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

Bit	Attr	Reset Value	Description
4	RW	0x1	cfg_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RO	0x0	reserved
2	RW	0x1	ltr_msg_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	unlock_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	ven_msg_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_LEGACY
Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	tx_intd_int_en Reserved
6	RW	0x1	tx_intc_int_en Reserved
5	RW	0x1	tx_intb_int_en Reserved
4	RW	0x1	tx_inta_int_en Reserved
3	RW	0x1	rx_intd_int_en Reserved
2	RW	0x1	rx_intc_int_en Reserved
1	RW	0x1	rx_intb_int_en Reserved
0	RW	0x1	rx_inta_int_en Reserved

PCIE_CLIENT_INTR_EN_ERR
Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12	RW	0x1	radm_qoverflow_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RO	0x0	reserved
10	RW	0x1	f_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	nf_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	cor_err_rx_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
7	RO	0x0	reserved
6	RW	0x1	f_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	nf_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	cor_err_sent_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	tx_cpl_timeout_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
2	RW	0x1	rx_cpl_timeout_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	aer_rc_err_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

Bit	Attr	Reset Value	Description
0	RW	0x1	aer_rc_err_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_MISC
Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	ep_elbi_app_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
14	RW	0x1	link_eq_req_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
13	RW	0x1	rbar_update_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
12	RW	0x1	dpa_sub_upd_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
11	RW	0x1	edma_rd_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
10	RW	0x1	edma_wr_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
9	RW	0x1	bw_mgt_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
8	RW	0x1	bw_mgt_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

Bit	Attr	Reset Value	Description
7	RW	0x1	link_auto_bw_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
6	RW	0x1	link_auto_bw_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	hp_msi_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	hp_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	hp_pme_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
2	RW	0x1	link_req_rst_not_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	dll_link_up_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	phy_link_up_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_INTR_EN_PMC

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	pm_dstate_update_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

Bit	Attr	Reset Value	Description
7	RW	0x1	linkst_out_l0s_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
6	RW	0x1	linkst_out_l2_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
5	RW	0x1	linkst_out_l1_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
4	RW	0x1	linkst_out_l1sub_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
3	RW	0x1	linkst_in_l0s_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
2	RW	0x1	linkst_in_l2_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
1	RW	0x1	linkst_in_l1_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.
0	RW	0x1	linkst_in_l1sub_int_en Enable bit of interrupt. 1'b0: Interrupt status disable 1'b1: Interrupt status enable Available after version 50610.

PCIE_CLIENT_AXI_MSTR_MISC_CON

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	mstr_rmisc_ep AXI Master Read Response Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of standard AXI interface. For more information, see 'AXI Master Interface Sideband Signals'. All reserved bits must be connected to logic '0'. [1:0]: Reserved [2]: Reserved [6:3]: Reserved [7]: TLP's EP bit [12:8]: Reserved
3:2	RW	0x0	mstr_rmisc_info_cpl_stat AXI Master Read Response selection bus. This bus controls the response sent on the PCIe wire in the case of successful read requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. For more information, see the "Master AXI-to-PCIe Error Mapping" section in the AXI chapter of the Databook. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion) Your application must drive the same value on mstr_rmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_rmisc_info_cpl_stat to UR: 1. If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. 2. If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.
1:0	RW	0x0	mstr_bmisc_info_cpl_stat AXI Master Write Response selection bus. This controls the response to be sent on the wire in the case of successful write requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. For more information, see the "Master AXI-to-PCIe Error Mapping" section in the AXI chapter of the Databook. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion) Your application must drive the same value on mstr_bmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_bmisc_info_cpl_stat to UR: 1. If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. 2. If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.

PCIE_CLIENT_AXI_SLV_ATU_BYPASS
Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	slv_armisc_info_atu_bypass AXI Slave Read Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit. 1'b0: Not bypass 1'b1: AXI slave read address ATU bypass
0	RW	0x0	slv_awmisc_info_atu_bypass AXI Slave Write Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit. 1'b0: Not bypass 1'b1: AXI slave write address ATU bypass

PCIE_CLIENT_AXI_SLV_AWMISC_HDR
Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	slv_awmisc_info AXI Slave Write Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more information, see 'AXI Slave Interface Sideband Signals'. You must set all reserved bits to '0'.[4:0]: TLP's TYPE. For more information, see 'I/O and CFG Transaction Handling' [5]: Serialize NP Requests [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit [12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's Function number. Function numbering starts at '0'. Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more information, see slv_awmisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled. For a configuration transfer, you must drive the bus number, device number, function number, and register number onto the address bus as follows: bus_number = addr[31:24] dev_number = addr[23:19] func_number = addr[18:16] ext_reg_number = addr[11:8] reg_number = addr[7:2]

PCIE_CLIENT_AXI_SLV_AWMISC_HDR3
Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_3dw AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.

PCIE_CLIENT_AXI_SLV_AWMISC_HDR4
Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_4dw AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.

PCIE_CLIENT_AXI_SLV_AWMISC_TAG
Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	slv_awmisc_info_p_tag AXI Slave Write Request Tag. Sets the TAG number for output posted requests. It is expected that your application normally sets this to '0' except when generating ATS invalidate requests.

PCIE_CLIENT_AXI_SLV_MISC_INFO
Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	slv_wmisc_info_ep AXI Slave Write Data transaction related misc information. This is an optional signal that your application can use to poison write requests. When asserted, the controller sets the Poisoned TLP (EP) bit in the TLP header of the current and subsequent Write Data transactions. It is not a part of the standard AXI interface. For more information, see "AXI Slave Interface Sideband Signals" section in the Databook.

Bit	Attr	Reset Value	Description
21:0	RW	0x000000	slv_armisc_info AXI Slave Read Transaction Associated Miscellaneous Information. This is a signal that the application can optionally use. It is not part of the standard AXI interface. For more information, see 'AXI Slave Interface Sideband Signals'. You must set all reserved bits to '0'. [4:0]: TLP's TYPE [5]: Serialize NP Requests [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit [12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's function number. Function numbering starts at '0'. Not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. For more information, see slv_armisc_info_func_num. This field is only present when multifunction support (CX_NFUNC > 1) is enabled. For a configuration transfer, you must drive the bus number, device number, function number, and register number onto the address bus as follows: bus_number = addr[31:24] dev_number = addr[23:19] func_number = addr[18:16] ext_reg_number = addr[11:8] reg_number = addr[7:2]

PCIE_CLIENT_AXI_SLV_AW_TLP_PRFX
Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_tlpprfx AXI Slave Write Request TLP Prefixes. The field [31:0] represents the first prefix to be transmitted. The optional TLP prefixes are implemented as little endian. Using the example of a controller with just one prefix (CX_NPRFX =1), this means that slv_awmisc_info_tlpprfx[31:0] has prefix byte #0 in the lower byte position of the dword slv_awmisc_info_tlpprfx[31:0]. That is, FMT =bits 7:5, and Type =bits 4:0. Your application is responsible for passing Local and End-End prefixes in the correct order for transmission. Local prefixes must precede End-End prefixes. Any parity bits that your application appends (when RAS data protection is enabled) to the most significant bits are routed but not checked by the controller. The controller passes along and appends to the prefix, any protection codes it receives, when datapath protection is enabled. Available after version 50610.

PCIE_CLIENT_AXI_SLV_AR_TLP_PRFX
Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	slv_armisc_info_tlpprfx AXI Slave Read Request TLP Prefixes. The field [31:0] represents the first prefix to be transmitted. The optional TLP prefixes are implemented as little endian. Using the example of a controller with just one prefix (CX_NPRFX =1), this means that slv_armisc_info_tlpprfx[31:0] has prefix byte #0 in the lower byte position of the dword slv_armisc_info_tlpprfx[31:0]. That is, FMT =bits 7:5, and Type =bits 4:0. Your application is responsible for passing Local and End-End prefixes in the correct order for transmission. Local prefixes must precede End-End prefixes. Any parity bits that your application appends (when RAS data protection is enabled) to the most significant bits are routed but not checked by the controller. The controller passes along and appends to the prefix, any protection codes it receives, when datapath protection is enabled. Available after version 50610.

PCIE_CLIENT_DBI_MISC_CON
Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	dbi_msix_table_access_ctrl Control the bit 30 of the DBI awaddr. Set 1 to enable access, and shoud clear to 0 when access done.

PCIE_CLIENT_PORT_BDF
Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	app_bus_dev Bus number. Your application must drive this signal to set the bus number in the Requester ID for RC port and Switch DSP port.
7:3	RW	0x00	app_dev_num Device number. Your application must drive this signal to set the device number in the Requester ID for RC port and Switch DSP port.
2:0	RO	0x0	reserved

PCIE_CLIENT_LTSSM_STATUS
Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

Bit	Attr	Reset Value	Description
22:20	RO	0x0	pm_current_data_rate The current link operating rate. 3'b000: 2.5 GT/s signaling rate 3'b001: 5.0 GT/s signaling rate 3'b010: 8.0 GT/s signaling rate for PCIe mode or ESM data rate0 for ESM mode 3'b011: 16.0 GT/s signaling rate for PCIe mode or ESM data rate1 for ESM mode 3'b100: 32.0 GT/s signaling rate
19:18	RO	0x0	reserved
17	RO	0x0	rdlh_link_up Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. 1'b0: Link is down 1'b1: Link is up
16	RO	0x0	smlh_link_up PHY Link up/down indicator: 1'b0: Link is down 1'b1: Link is up
15:11	RO	0x00	reserved
10:8	RO	0x0	l1sub_state Power management L1 sub-states FSM state.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RO	0x00	smlh_ltssm_state smlh_ltssm_state Current state of the LTSSM. Encoding is defined as follows: 6'h00: S_DETECT_QUIET 6'h01: S_DETECT_ACT 6'h02: S_POLL_ACTIVE 6'h03: S_POLL_COMPLIANCE 6'h04: S_POLL_CONFIG 6'h05: S_PRE_DETECT_QUIET 6'h06: S_DETECT_WAIT 6'h07: S_CFG_LINKWD_START 6'h08: S_CFG_LINKWD_ACEPT 6'h09: S_CFG_LANENUM_WAI 6'h0A: S_CFG_LANENUM_ACEPT 6'h0B: S_CFG_COMPLETE 6'h0C: S_CFG_IDLE 6'h0D: S_RCVRY_LOCK 6'h0E: S_RCVRY_SPEED 6'h0F: S_RCVRY_RCVRCFG 6'h10: S_RCVRY_IDLE 6'h11: S_L0 6'h12: S_L0S 6'h13: S_L123_SEND_EIDLE 6'h14: S_L1_IDLE 6'h15: S_L2_IDLE 6'h16: S_L2_WAKE 6'h17: S_DISABLED_ENTRY 6'h18: S_DISABLED_IDLE 6'h19: S_DISABLED 6'h1A: S_LPBK_ENTRY 6'h1B: S_LPBK_ACTIVE 6'h1C: S_LPBK_EXIT 6'h1D: S_LPBK_EXIT_TIMEOUT 6'h1E: S_HOT_RESET_ENTRY 6'h1F: S_HOT_RESET 6'h20: S_RCVRY_EQ0 6'h21: S_RCVRY_EQ1 6'h22: S_RCVRY_EQ2 6'h23: S_RCVRY_EQ3

PCIE_CLIENT_DBG_FIFO_MODE_CON
Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	dbg_fifo_hit_mode Hit mode control. Bit0 enable pattern 0 match mode Bit1 enable pattern 1 match mode Bit2 enable pattern 0 transition mode
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	dbg_fifo_mode Debug FIFO store debug status mode 2'b00: Default 2'b01: If hit pattern, disable FIFO write 2'b10: If FIFO full, disable FIFO write 2'b11: Reserved
3	RO	0x0	reserved
2	RW	0x0	dbg_fifo_l1sub_en Debug FIFO enable for L1SS 1'b0: Disable 1'b1: Enable
1	RW	0x0	dbg_fifo_ltssm_en Debug FIFO enable for LTSSM 1'b0: Disable 1'b1: Enable
0	RW	0x0	dbg_fifo_en Debug FIFO enable 1'b0: Disable 1'b1: Enable

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0
Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ptn_hit_data0 Hit mode data pattern 0

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1
Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ptn_hit_data1 Hit mode data pattern 1

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0
Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data0 Transition state data 0

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1
Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data1 Transition state data 1

PCIE_CLIENT_DBG_FIFO_STATUS
Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

Bit	Attr	Reset Value	Description
22:20	RO	0x0	dbg_pm_current_data_rate The current link operating rate. 3'b000: 2.5 GT/s signaling rate 3'b001: 5.0 GT/s signaling rate 3'b010: 8.0 GT/s signaling rate for PCIe mode or ESM data rate0 for ESM mode 3'b011: 16.0 GT/s signaling rate for PCIe mode or ESM data rate1 for ESM mode 3'b100: 32.0 GT/s signaling rate Available after version 50610.
19	RO	0x0	reserved
18:16	RO	0x0	dbg_space2empty Debug FIFO space to empty.
15	RO	0x0	reserved
14	RO	0x0	dbg_fifo_wr_overfollow Debug FIFO overfollow flag 1'b0: Not overfollow 1'b1: Overfollow
13	RO	0x0	dbg_fifo_full Debug FIFO full flag 1'b0: Not full 1'b1: Full
12	RO	0x0	dgb_fifo_empty Debug FIFO empty flag 1'b0: Not empty 1'b1: Empty
11	RO	0x0	reserved
10:8	RO	0x0	dbg_fifo_l1sub_state Power management L1 sub-states FSM state.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RO	0x00	dbg_fifo_ltssm_state smlh_ltssm_state Current state of the LTSSM. Encoding is defined as follows: 6'h00: S_DETECT_QUIET 6'h01: S_DETECT_ACT 6'h02: S_POLL_ACTIVE 6'h03: S_POLL_COMPLIANCE 6'h04: S_POLL_CONFIG 6'h05: S_PRE_DETECT_QUIET 6'h06: S_DETECT_WAIT 6'h07: S_CFG_LINKWD_START 6'h08: S_CFG_LINKWD_ACEPT 6'h09: S_CFG_LANENUM_WAI 6'h0A: S_CFG_LANENUM_ACEPT 6'h0B: S_CFG_COMPLETE 6'h0C: S_CFG_IDLE 6'h0D: S_RCVRY_LOCK 6'h0E: S_RCVRY_SPEED 6'h0F: S_RCVRY_RCVRCFG 6'h10: S_RCVRY_IDLE 6'h11: S_L0 6'h12: S_L0S 6'h13: S_L123_SEND_EIDLE 6'h14: S_L1_IDLE 6'h15: S_L2_IDLE 6'h16: S_L2_WAKE 6'h17: S_DISABLED_ENTRY 6'h18: S_DISABLED_IDLE 6'h19: S_DISABLED 6'h1A: S_LPBK_ENTRY 6'h1B: S_LPBK_ACTIVE 6'h1C: S_LPBK_EXIT 6'h1D: S_LPBK_EXIT_TIMEOUT 6'h1E: S_HOT_RESET_ENTRY 6'h1F: S_HOT_RESET 6'h20: S_RCVRY_EQ0 6'h21: S_RCVRY_EQ1 6'h22: S_RCVRY_EQ2 6'h23: S_RCVRY_EQ3

PCIE_CLIENT_CFG_ERR_STATUS

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	cfg_uncor_internal_err_sts Indication from the controller that the controller has detected an Uncorrectable Internal Error.
11	RO	0x0	cfg_rcvr_overflow_err_sts Indication from the controller that the controller has detected an Receiver Overflow Error.
10	RO	0x0	cfg_fc_protocol_err_sts Indication from the controller that the controller has detected an Flow Control Protocol Error.

Bit	Attr	Reset Value	Description
9	RO	0x0	cfg_mlf_tlp_err_sts Indication from the controller that the controller detected an Malformed TLP Error.
8	RO	0x0	cfg_surprise_down_err_sts Indication from the controller that the controller detected an Surprise Down Error.
7	RO	0x0	cfg_dl_protocol_err_sts Indication from the controller that the controller detected an Data Link Protocol Error.
6	RO	0x0	cfg_ecrc_err_sts Indication from the controller that the controller detected an ECRC Error.
5	RO	0x0	cfg_corrected_internal_err_sts Indication from the controller that the controller detected an Corrected Internal Error.
4	RO	0x0	cfg_replay_number_rollover_err_sts Indication from the controller that the controller detected an REPLAY_NUMBER Rollover Error.
3	RO	0x0	cfg_replay_timer_timeout_err_sts Indication from the controller that the controller detected an Replay Timer Timeout.
2	RO	0x0	cfg_bad_dllp_err_sts Indication from the controller that the controller detected an Bad DLLP Error.
1	RO	0x0	cfg_bad_tlp_err_sts Indication from the controller that the controller detected an Bad TLP Error.
0	RO	0x0	cfg_rcvr_err_sts Indication from the controller that the controller detected an Receiver Error.

PCIE_CLIENT_TLP_PRFX_LOG0
Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_0 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG1
Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_1 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG2
Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_2 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_TLP_PRFX_LOG3
Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_tlp_prfx_log_3 End-End TLP prefixes of the TLP that contained an error. Valid when 1. app_hdr_valid is asserted. The header of the TLP that contained the error indicated on app_err_bus. For Corrected Internal and Uncorrectable Internal errors (app_err_bus[10:9]),and receiver Overflow (app_err_bus[1]), the header information this input is not logged by the controller. 2. app_dpc_err_valid is asserted. The header of the TLP that contained the error indicated on app_dpc_err_bus. When DPC RP PIO extensions are supported, it is used to update DPC RP PIO Header Log Register. Available after version 50610.

PCIE_CLIENT_CLIENT_VER
Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RO	0x00050610	version Client version ID

11.4.3 Downstream Port Register

11.4.3.1 DSP_PCIE_TYPE1 Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_TYPE1_DEV_ID_VEND_ID_REG	0x0000	W	0x18081D87	Device ID and Vendor ID Register
DSP_PCIE_TYPE1_STATUS_COMMAND_REG	0x0004	W	0x00100000	Status and Command Register
DSP_PCIE_TYPE1_CLASS_CODE_REV_ID_REG	0x0008	W	0x00000001	Class Code and Revision ID Register
DSP_PCIE_TYPE1_BIST_HDR_TYPE_LAT_CACHE_LINE_SIZE_REG	0x000C	W	0x00010000	BIST, Header Type, Latency Timer, and Cache Line Size Register
DSP_PCIE_TYPE1_BAR0_REG	0x0010	W	0x00000000	BAR0 Register
DSP_PCIE_TYPE1_BAR1_REG	0x0014	W	0x00000000	BAR0 Register
DSP_PCIE_TYPE1_SEC_LAT_TIMER_SUB_BUS_SEC_BUS_PRI_BUS_REG	0x0018	W	0x00000000	Secondary Latency Timer, Subordinate Bus Number, Secondary Bus Number, and Primary Bus Number Register
DSP_PCIE_TYPE1_SEC_STAT_IO_LIMIT_IO_BASE_REG	0x001C	W	0x00000000	Secondary Status, and I/O Limit and Base Register
DSP_PCIE_TYPE1_MEM_LIMIT_MEM_BASE_REG	0x0020	W	0x00000000	Memory Limit and Base Register
DSP_PCIE_TYPE1_PREF_MEM_LIMIT_PREF_MEM_BASE_REG	0x0024	W	0x00010001	Prefetchable Memory Limit and Base Register
DSP_PCIE_TYPE1_PREF_BASE_UPPER_REG	0x0028	W	0x00000000	Prefetchable Base Upper 32 Bits Register
DSP_PCIE_TYPE1_PREF_LIMIT_UPPER_REG	0x002C	W	0x00000000	Prefetchable Limit Upper 32 Bits Register
DSP_PCIE_TYPE1_IO_LIMIT_UPPER_IO_BASE_UPPER_REG	0x0030	W	0x00000000	I/O Limit and Base Upper 16 Bits Register
DSP_PCIE_TYPE1_CAP_PTR_REG	0x0034	W	0x00000040	Capabilities Pointer Register
DSP_PCIE_TYPE1_EXP_ROM_BASE_REG	0x0038	W	0x00000000	Expansion ROM Base Address Register
DSP_PCIE_TYPE1_BRIDGE_CTRL_INT_PIN_INT_LINE_REG	0x003C	W	0x000001FF	Bridge Control, Interrupt Pin, and Interrupt Line Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.2 DSP_PCIE_TYPE1 Detail Registers Description

DSP_PCIE_TYPE1_DEV_ID_VEND_ID_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x1808	DEVICE_ID Device ID. The Device ID register identifies the particular Function. This identifier is allocated by the vendor. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x3588 Testable: unconstrained
15:0	RW	0x1d87	VENDOR_ID Vendor ID. The Vendor ID register identifies the manufacturer of the Function. Valid vendor identifiers are allocated by the PCI-SIG to ensure uniqueness. It is not permitted to populate this register with a value of FFFFh, which is an invalid value for Vendor ID. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1d87 Testable: unconstrained

DSP_PCIE_TYPE1_STATUS_COMMAND_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	W1C	0x0	DETECTED_PARITY_ERROR Detected Parity Error. The bit is set when the Poisoned TLP is received by a Function's primary side. Values: 0x1 (SET): This bit is set by a Function whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response bit in the Command register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
30	W1C	0x0	SIGNALED_SYS_ERROR Signaled System Error. Values: 0x1 (SET): This bit is set when a Function sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR# Enable bit in the Command register is 1b. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
29	W1C	0x0	RCVD_MASTER_ABORT Received Master Abort. This bit is set when a Requester receives a Completion with Unsupported Request Completion status. The bit is set when the Unsupported Request is received by a Function's primary side. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
28	W1C	0x0	RCVD_TARGET_ABORT Received Target Abort. This bit is set when a Requester receives a Completion with Completer Abort Completion status. The bit is set when the Completer Abort is received by a Function's primary side. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
27	W1C	0x0	SIGNALED_TARGET_ABORT Signaled Target Abort. This bit is set when a Function completes a Posted or Non-Posted Request as a Completer Abort error. This applies to a Function when the Completer Abort was generated by its primary side. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
26:25	RO	0x0	DEV_SEL_TIMING DEVSEL Timing. This field was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires it to 00b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
24	W1C	0x0	MASTER_DPE Master Data Parity Error. This bit is set by a Function if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: Port receives a Poisoned Completion going downstream Port transmits a Poisoned Request upstream If the Parity Error Response bit is 0b, this bit is never set. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23	RO	0x0	FAST_B2B_CAP Fast Back-to-Back Transactions Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0
22	RO	0x0	reserved
21	RO	0x0	FAST_66MHZ_CAP 66 MHz Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0
20	RO	0x1	CAP_LIST Capabilities List. Indicates the presence of an Extended Capability list item. Since all PCI Express device Functions are required to implement the PCI Express Capability structure, the controller hardwires this bit to 1b. Value After Reset: 0x1
19	RO	0x0	INT_STATUS Interrupt Status. INTx emulation interrupts forwarded by Functions from the secondary side are not reflected in this bit. Setting the Interrupt Disable bit has no effect on the state of this bit. For Functions that do not generate INTx interrupts, the controller hardwires this bit to 0b. Values: 0x1 (SET): Indicates that an INTx emulation interrupt is pending internally in the Function. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
18:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	INT_EN Interrupt Disable. Controls the ability of a Function to generate INTx emulation interrupts. Note: Any INTx emulation interrupts already asserted by the Function must be deasserted when this bit is set. INTx interrupts use virtual wires that must, if asserted, be deasserted using the appropriate Deassert_INTx message(s) when this bit is set. Only the INTx virtual wire interrupt(s) associated with the Function(s) for which this bit is set are affected. For Functions that generate INTx interrupts on their own behalf, this bit is required. This bit has no effect on interrupts forwarded from the secondary side. For Functions that do not generate INTx interrupts on their own behalf this bit is optional. If this bit is not implemented, the controller hardwires it to 0b. Values: 0x1 (SET): When set, Functions are prevented from asserting INTx interrupts. Value After Reset: 0x0
9	RO	0x0	reserved
8	RW	0x0	SERREN SERR# Enable. Note: The errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control register. In addition, this bit controls transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error Messages forwarded from the secondary interface. This bit does not affect the transmission of forwarded ERR_COR messages. Values: 0x1 (SET): This bit enables reporting upstream of Non-fatal and Fatal errors detected by the Function. Value After Reset: 0x0
7	RO	0x0	IDSEL IDSEL Stepping/Wait Cycle Control. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
6	RW	0x0	PERREN Parity Error Response. This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Status register. Values: 0x1 (ENABLE): Parity Error Response enable 0x0 (DISABLE): Parity Error Response disable Value After Reset: 0x0
5	RO	0x0	VGAPS VGA Palette Snoop. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0
4	RO	0x0	MWI_EN Memory Write and Invalidate. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. For PCI Express to PCI/PCI-X Bridges, refer to the PCI Express to PCI/PCI-X Bridge Specification for requirements for this register. Value After Reset: 0x0
3	RO	0x0	SCO Special Cycle Enable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0
2	RW	0x0	BME Bus Master Enable. This bit controls forwarding of Memory or I/O requests by a port in the Upstream direction. When this bit is 0b, Memory and I/O Requests received at a Root Port must be handled as Unsupported Requests (UR) For Non-Posted Requests a Completion with UR completion status must be returned. This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O Requests is not controlled by this bit. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
1	RW	0x0	MSE Memory Space Enable. This bit controls a Function's response to Memory Space accesses received on its primary side. You cannot write to this register if your configuration has no MEM BARs; that is, the internal signal has_mem_bar =0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: !has_mem_bar ? RO : RW Values: 0x1 (SET): The Function is enabled to decode the address and further process Memory Space accesses. 0x0 (CLEAR): All received Memory Space accesses are caused to be handled as Unsupported Requests. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RW	0x0	IO_EN IO Space Enable. This bit controls a Function's response to I/O Space accesses received on its primary side. You cannot write to this register if your configuration has no IO BARs; that is, the internal signal has_io_bar =0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: !has_io_bar ? RO : RW Values: 0x1 (SET): The Function is enabled to decode the address and further process I/O Space accesses. 0x0 (CLEAR): All received I/O accesses are caused to be handled as Unsupported Requests. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_TYPE1_CLASS_CODE_REV_ID_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BASE_CLASS_CODE Base Class Code. A code that broadly classifies the type of operation the Function performs. Encodings for base class, are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
23:16	RW	0x00	SUBCLASS_CODE Sub-Class Code. Specifies a base class sub-class, which identifies more specifically the operation of the Function. Encodings for sub-class are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
15:8	RW	0x00	PROGRAM_INTERFACE Programming Interface. This field identifies a specific register level programming interface (if any) so that device independent software can interact with the Function. Encodings for interface are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are reserved. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
7:0	RW	0x01	REVISION_ID Revision ID. The value of this field specifies a Function specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Revision ID should be viewed as a vendor defined extension to the Device ID. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

DSP_PCIE_TYPE1_BIST_HDR_TYPE_LAT_CACHE_LINE_SIZE_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	BIST BIST. This register is used for control and status of BIST. Functions that do not support BIST must hardwire the register to 00h. A Function whose BIST is invoked must not prevent normal operation of the PCI Express Link. Bit descriptions: [31]: BIST Capable. When set, this bit indicates that the Function supports BIST. When Clear, the Function does not support BIST. [30]: Start BIST. If BIST Capable is set, set this bit to invoke BIST. The Function resets the bit when BIST is complete. Software is permitted to fail the device if this bit is not Clear (BIST is not complete) 2 seconds after it had been set. Writing this bit to 0b has no effect. The controller hardwires this bit to 0b if BIST Capable is clear. [29:28]: Reserved. [27:24]: Completion Code. This field encodes the status of the most recent test. A value of 0000b means that the Function has passed its test. Non-zero values mean the Function failed. Function-specific failure codes can be encoded in the non-zero values. This field's value is only meaningful when BIST Capable is set and Start BIST is Clear. This field must be hardwired to 0000b if BIST Capable is clear. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
23	RO	0x0	MULTI_FUNC Multi-Function Device. Except where stated otherwise, it is recommended that this bit be set if there are multiple Functions, and clear if there is only one Function. Note: This register field is sticky. Values: 0x1 (SET): Indicates that the device may contain multiple Functions, but not necessarily. Software is permitted to probe for Functions other than Function 0. 0x0 (CLEAR): Software must not probe for Functions other than Function 0 unless explicitly indicated by another mechanism, such as an ARI or SR-IOV Capability structure. Value After Reset: 0x0
22:16	RO	0x01	HEADER_TYPE Header Layout. This field identifies the layout of the second part of the predefined header. The controller uses 000 0001b encoding. The encoding 000 0010b is reserved. This encoding was originally described in the PC Card Standard Electrical Specification and is used in previous versions of the programming model. Careful consideration should be given to any attempt to re-purpose it. Value After Reset: 0x1
15:8	RO	0x00	LATENCY_MASTER_TIMER Latency Timer. This register is also referred to as Primary Latency Timer. The Latency Timer was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this register to 00h. Value After Reset: 0x0
7:0	RW	0x00	CACHE_LINE_SIZE Cache Line Size. The Cache Line Size register is programmed by the system firmware or the operating system to system cache line size. However, legacy conventional PCI software may not always be able to program this register correctly especially in the case of Hot-Plug devices. This read-write register is implemented for legacy compatibility purposes but has no effect on any PCI Express device behavior. Value After Reset: 0x0

DSP_PCIE_TYPE1_BAR0_REG
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR0_START BAR0 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	RW	0x0	BAR0_PREFETCH BAR0 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
2:1	RW	0x0	BAR0_TYPE BAR0 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RW	0x0	BAR0_MEM_IO BAR0 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_TYPE1_BAR1_REG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR1_START BAR1 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	RW	0x0	BAR1_PREFETCH BAR1 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
2:1	RW	0x0	BAR1_TYPE BAR1 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RW	0x0	BAR1_MEM_IO BAR1 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_TYPE1_SEC_LAT_TIMER_SUB_BUS_SEC_BUS_PRI_BUS_REG
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	SEC_LAT_TIMER Secondary Latency Timer. This register does not apply to PCI Express. The controller hardwires it to 00h. Value After Reset: 0x0
23:16	RW	0x00	SUB_BUS Subordinate Bus Number. The Subordinate Bus Number register is used to record the bus number of the highest numbered PCI bus segment which is behind (or subordinate to) the bridge. Configuration software programs the value in this register. The bridge uses this register in conjunction with the Secondary Bus Number register to determine when to respond to and pass on a Type 1 configuration transaction on the primary interface to the secondary interface. Value After Reset: 0x0
15:8	RW	0x00	SEC_BUS Secondary Bus Number. The Secondary Bus Number register is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected. Configuration software programs the value in this register. The bridge uses this register to determine when to respond to and convert a Type 1 configuration transaction on the primary interface into a Type 0 transaction on the secondary interface. Value After Reset: 0x0
7:0	RW	0x00	PRIM_BUS Primary Bus Number. This register is not used by PCI Express Functions. It is implemented for compatibility with legacy software. Value After Reset: 0x0

DSP_PCIE_TYPE1_SEC_STAT_IO_LIMIT_IO_BASE_REG

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31	W1C	0x0	SEC_STAT_DPE Detected Parity Error. This bit is set by a Function when a Poisoned TLP is received by its secondary side, regardless of the state the Parity Error Response Enable bit in the Bridge Control register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
30	W1C	0x0	SEC_STAT_RCVD_SYS_ERR Received System Error. This bit is set when the secondary side of a Function receives an ERR_FATAL or ERR_NONFATAL message. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
29	W1C	0x0	SEC_STAT_RCVD_MSTR_ABRT Received Master Abort. This bit is set when the secondary side of a Function (for requests initiated by the Type 1 header Function itself) receives a Completion with Unsupported Request Completion status. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
28	W1C	0x0	SEC_STAT_RCVD_TRGT_ABRT Received Target Abort. This bit is set when the secondary side of a Function (for requests initiated by the Type 1 header Function itself) receives a Completion with Completer Abort Completion status. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
27	W1C	0x0	SEC_STAT_SIG_TRGT_ABRT Signaled Target Abort. This bit is set when the secondary side of the Function (for Requests completed by the Type 1 header Function itself) completes a Posted or Non-Posted request as a Completer Abort error. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
26:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24	W1C	0x0	SEC_STAT_MDPE Master Data Parity Error. This bit is set by a Function if the Parity Error Response Enable bit in the Bridge Control register is set, and either of the following two conditions occurs: Port receives a Poisoned Completion coming Upstream Port transmits a Poisoned Request Downstream If the Parity Error Response Enable bit is clear, this bit is never set. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:16	RO	0x00	reserved
15:12	RW	0x0	IO_LIMIT I/O Limit Address. These bits correspond to the address[15:12] of IO address range. For the purpose of address decoding, the bridge assumes that the lower 12 address bits, address[11:0], of the I/O limit address (not implemented in the I/O Limit register) are FFFh. The I/O Limit register can be programmed to a smaller value than the I/O Base register, if there are no I/O addresses on the secondary side of the bridge. In this case, the bridge will not forward any I/O transactions from the primary bus to the secondary and will forward all I/O transactions from the secondary bus to the primary bus. Value After Reset: 0x0
11:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RO	0x0	IO_DECODE_BIT8 I/O Addressing Encode (IO Limit Address). This bit encodes the IO addressing capability of the bridge. Note: For 16bit I/O address decoding, the bridge must still perform a full 32-bit decode of the I/O address (that is, check that Address[31:16] are 0000h). In this case, the I/O address range supported by the bridge will be restricted to the first 64 KB of I/O Space (0000 0000h to 0000 FFFFh). For 16bit I/O address decoding, the bridge assumes that the upper 16 address bits, Address[31:16], of the I/O limit address (not implemented in I/O Limit register) are zero. For 32bit I/O address decoding, and the I/O Limit Upper 16 Bits hold the upper 16 bits, corresponding to Address[31:16], of the 32-bit Limit address. In this case, system configuration software is permitted to locate the I/O address range supported by the bridge anywhere in the 4-GB I/O Space. The 4-KB alignment and granularity restrictions still apply when the bridge supports 32-bit I/O addressing. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Values: 0x0 (_16b_SUP_IO_ADDR): The bridge supports only 16-bit I/O addressing (for ISA compatibility). 0x1 (_32b_SUP_IO_ADDR): The bridge supports 32-bit I/O addressing. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
7:4	RW	0x0	IO_BASE I/O Base Address. These bits correspond to the address[15:12] of IO address range. For the purpose of address decoding, the bridge assumes that the lower 12 address bits, address[11:0], of the I/O base address (not implemented in the I/O Base register) are zero. Value After Reset: 0x0
3:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	IO_DECODE I/O Addressing Encode (IO Base Address). This bit encodes the IO addressing capability of the bridge. Note: For 16bit I/O address decoding, the bridge must still perform a full 32-bit decode of the I/O address (that is, check that Address[31:16] are 0000h). In this case, the I/O address range supported by the bridge will be restricted to the first 64 KB of I/O Space (0000 0000h to 0000 FFFFh). For 16bit I/O address decoding, the bridge assumes that the upper 16 address bits, Address[31:16], of the I/O limit address (not implemented in I/O Limit register) are zero. For 32bit I/O address decoding, and the I/O Limit Upper 16 Bits hold the upper 16 bits, corresponding to Address[31:16], of the 32-bit Limit address. In this case, system configuration software is permitted to locate the I/O address range supported by the bridge anywhere in the 4-GB I/O Space. The 4-KB alignment and granularity restrictions still apply when the bridge supports 32-bit I/O addressing. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Values: 0x0 (_16b_SUP_IO_ADDR): The bridge supports only 16-bit I/O addressing (for ISA compatibility). 0x1 (_32b_SUP_IO_ADDR): The bridge supports 32-bit I/O addressing. Value After Reset: 0x0 Testable: unconstrained

DSP_PCIE_TYPE1_MEM_LIMIT_MEM_BASE_REG

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	MEM_LIMIT Memory Limit Address. These bits correspond to the upper 12 address bits, Address[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, Address[19:0], of the memory limit address (not implemented in the Memory Limit register) are F FFFFh. The Memory Limit register must be programmed to a smaller value than the Memory Base register if there is no memory-mapped address space on the secondary side of the bridge. Value After Reset: 0x0
19:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:4	RW	0x000	MEM_BASE Memory Base Address. These bits correspond to the upper 12 address bits, Address[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, Address[19:0], of the memory base address (not implemented in the Memory Base register) are zero. Value After Reset: 0x0
3:0	RO	0x0	reserved

DSP_PCIE_TYPE1_PREF_MEM_LIMIT_PREF_MEM_BASE_REG
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	PREF_MEM_LIMIT Prefetchable Memory Limit Address. If the Prefetchable Memory Limit register indicates support for 32-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read-only register that returns zero when read. If the Prefetchable Memory Limit registers indicate support for 64-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read/write register which must be initialized by configuration software. If a 64-bit prefetchable memory address range is supported, the Prefetchable Limit Upper 32 Bits register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit limit addresses which specify the prefetchable memory address range. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
19:17	RO	0x0	reserved
16	RO	0x1	PREF_MEM_LIMIT_DECODE Prefetchable Memory Limit Decode. This bit encodes whether or not the bridge supports 64-bit addresses. Note: This bit is a copy of the PREF_MEM_DECODE bit and always reflects the current value of that bit. Values: 0x0 (SUP_32b_ADDR): Indicates that the bridge supports only 32 bit addresses. 0x1 (SUP_64b_ADDR): Indicates that the bridge supports 64 bit addresses. Prefetchable Limit Upper 32 Bits registers holds the rest of the 64-bit prefetchable limit address. Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:4	RW	0x000	PREF_MEM_BASE Prefetchable Memory Base Address. If the Prefetchable Memory Base register indicates support for 32-bit addressing, then the Prefetchable Base Upper 32 Bits register is implemented as a read-only register that returns zero when read. If the Prefetchable Memory Base register indicates support for 64-bit addressing, then the Prefetchable Limit Upper 32 Bits register is implemented as a read/write register which must be initialized by configuration software. If a 64-bit prefetchable memory address range is supported, the Prefetchable Base Upper 32 Bits register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3:1	RO	0x0	reserved
0	RW	0x1	PREF_MEM_DECODE Prefetchable Memory Base Decode. This bit encodes whether or not the bridge supports 64-bit addresses. Note: By default the bit is set to 1'b1 indicating that 64-bit addresses are supported. If the bridge only supports 32-bit prefetchable memory address range, or if there is no prefetchable memory address range, then the configuration parameter MEM_DECODE_64_0 must be changed to 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (SUP_32b_ADDR): Indicates that the bridge supports only 32 bit addresses. 0x1 (SUP_64b_ADDR): Indicates that the bridge supports 64 bit addresses. Prefetchable Base Upper 32 Bits registers holds the rest of the 64-bit prefetchable base address. Value After Reset: 0x1 Testable: unconstrained

DSP_PCIE_TYPE1_PREF_BASE_UPPER_REG
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PREF_MEM_BASE_UPPER Prefetchable Base Upper 32 Bit. If the Prefetchable Memory Base register indicates support for 32-bit addressing, then this register is implemented as read-only register that returns zero when read. If the Prefetchable Memory Base register indicate support for 64-bit addressing, then this register is implemented as read/write register which must be initialized by configuration software. This register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range. Note: The access attributes of this field are as follows: Wire: No access. Dbi: PREF_MEM_LIMIT_PREF_MEM_BASE_REG.PREF_MEM_DECODE ? RW : RO Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_TYPE1_PREF_LIMIT_UPPER_REG
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	PREF_MEM_LIMIT_UPPER Prefetchable Limit Upper 32 Bit. If the Prefetchable Memory Limit register indicate support for 64-bit addressing, then this register is implemented as read/write register which must be initialized by configuration software. This register specifies the upper 32 bits, corresponding to Address[63:32], of the 64-bit base addresses which specify the prefetchable memory address range. Note: The access attributes of this field are as follows: Wire: No access. Dbi: PREF_MEM_LIMIT_PREF_MEM_BASE_REG.PREF_MEM_DECODE ? RW : RO Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_TYPE1_IO_LIMIT_UPPER_IO_BASE_UPPER_REG
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	IO_LIMIT_UPPER I/O Base Upper 16 Bits. If the I/O Base register indicates support for 16-bit I/O address decoding, then this register is implemented as a read-only register which return zero when read. If the I/O base register indicates support for 32-bit I/O addressing, then this register must be initialized by configuration software. If 32-bit I/O address decoding is supported, this register specifies the upper 16 bits, corresponding to Address[31:16], of the 32-bit base address, that specify the I/O address range. See the PCI-to-PCI Bridge Architecture Specification for additional details. Note: The access attributes of this field are as follows: Wire: No access. Dbi: SEC_STAT_IO_LIMIT_IO_BASE_REG.IO_DECODE ? RW : RO Value After Reset: 0x0 Testable: writeAsRead
15:0	RW	0x0000	IO_BASE_UPPER I/O Limit Upper 16 Bits. If the I/O Limit register indicates support for 16-bit I/O address decoding, then this register is implemented as a read-only register which return zero when read. If the I/O Limit register indicates support for 32-bit I/O addressing, then this register must be initialized by configuration software. If 32-bit I/O address decoding is supported, this register specifies the upper 16 bits, corresponding to Address[31:16], of the 32-bit limit address, that specify the I/O address range. See the PCI-to-PCI Bridge Architecture Specification for additional details). Note: The access attributes of this field are as follows: Wire: No access. Dbi: SEC_STAT_IO_LIMIT_IO_BASE_REG.IO_DECODE ? RW : RO Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_TYPE1_CAP_PTR_REG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x40	CAP_POINTER Capabilities Pointer. This register is used to point to a linked list of capabilities implemented by this Function. Since all PCI Express Functions are required to implement the PCI Express Capability structure, this register must point to a valid capability structure and either this structure is the PCI Express Capability structure, or a subsequent list item points to the PCI Express Capability structure. The bottom two bits are Reserved and must be set to 00b. Software must mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x40 Testable: unconstrained

DSP_PCIE_TYPE1_EXP_ROM_BASE_REG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	EXP_ROM_BASE_ADDRESS Expansion ROM Base Address. Upper 21 bits of the Expansion ROM base address. The number of bits (out of these 21) that a Function actually implements depends on how much address space the Function requires. The mask for this ROM BAR exists (if implemented) as a shadow register at this address. The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the second register at this address. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R
10:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ROM_BAR_VALIDATION_DETAILS Expansion ROM Validation Details. The field contains optional, implementation-specific details associated with Expansion ROM Validation. If validation is in progress (Expansion ROM Validation Status is 001b), non-zero values of this field represent implementation-specific indications of the phase of the validation progress (e.g., 50% complete). The value 0000b indicates that no validation progress information is provided. If validation is completed (Expansion ROM Validation Status 010b to 111b inclusive), non-zero values in this field represent additional implementation-specific information. The value 0000b indicates that no information is provided. When validation is supported and this field is not implemented, this field must be hardwired to 0000b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3:1	RW	0x0	ROM_BAR_VALIDATION_STATUS Expansion ROM Validation Status. When this field is non-zero, it indicates the status of hardware validation of the Expansion ROM contents. If the Function does not support validation, this field must be hardwired to 000b. It is optional whether an implementation is capable of returning Validation Status values 011b, 101b, 110b, or 111b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (ZERO): Validation not supported. 0x1 (ONE): Validation in Progress. 0x2 (TWO): Validation Pass Valid contents, trust test was not performed. 0x3 (THREE): Validation Pass Valid and trusted contents. 0x4 (FOUR): Validation Fail Invalid contents. 0x5 (FIVE): Validation Fail Valid but untrusted contents (e.g., Out of Date, Expired or Revoked Certificate). 0x6 (SIX): Warning Pass Validation Passed with implementation-specific warning. Valid contents, trust test was not performed. 0x7 (SEVEN): Warning Pass Validation Passed with implementation-specific warning. Valid and trusted contents. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	ROM_BAR_ENABLE Expansion ROM Enable. This bit controls whether or not the Function accepts accesses to its expansion ROM. The Memory Space Enable bit in the Command register has precedence over the Expansion ROM Enable bit. A Function must claim accesses to its expansion ROM only if both the Memory Space Enable bit and the Expansion ROM Enable bit are set. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R Values: 0x1 (ONE): Address decoding is enabled using the parameters in the other part of the Expansion ROM Base Address register. 0x0 (ZERO): Function's expansion ROM address space is disabled. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_TYPE1_BRIDGE_CTRL_INT_PIN_INT_LINE_REG

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	SBR Secondary Bus Reset. Setting this bit triggers a hot reset on the corresponding PCI Express Port. Software must ensure a minimum reset duration (Trst) as defined in the PCI Local Bus Specification. Software and systems must honor first-access-following-reset timing requirements, unless the Readiness Notifications mechanism is used or if the Immediate Readiness bit in the relevant Function's Status Register register is set. Port configuration registers must not be changed, except as required to update Port status. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
21	RO	0x0	MSTR_ABORT_MODE Master Abort Mode. This bit was originally described in the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
20	RO	0x0	VGA_16B_DEC VGA 16 bit decode. This bit only has meaning if VGA Enable bit is set. This bit enables system configuration software to select between 10-bit and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary. For Functions that do not support VGA, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Values: 0x0 (_10b_ADDR_DECODE): Execute 10-bit address decodes on VGA I/O accesses 0x1 (_16b_ADDR_DECODE): Execute 16-bit address decodes on VGA I/O accesses Value After Reset: 0x0

Bit	Attr	Reset Value	Description
19	RO	0x0	VGA_EN VGA Enable. Modifies the response by the bridge to VGA compatible addresses. If the VGA Enable bit is set, the bridge will positively decode and forward the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): Memory accesses in the range 000A 0000h to 000B FFFFh I/O addresses in the first 64 KB of the I/O address space (Address[31:16] are 0000h) where Address[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases determined by the setting of VGA 16-bit Decode) If the VGA Enable bit is set, forwarding of these accesses is independent of the I/O address range and memory address ranges defined by the I/O Base and Limit registers, the Memory Base and Limit registers, and the Prefetchable Memory Base and Limit registers of the bridge. (Forwarding of these accesses is also independent of the setting of the ISA Enable bit (in the Bridge Control register) when the VGA Enable bit is set. Forwarding of these accesses is qualified by the I/O Space Enable and Memory Space Enable bits in the Command register.) For Functions that do not support VGA, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Values: 0x0 (NO_FRWD_VGA): Do not forward VGA compatible memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges 0x1 (FRWD_VGA): Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the I/O Space Enable and Memory Space Enable bits are set) independent of the I/O and memory address ranges and independent of the ISA Enable bit Value After Reset: 0x0

Bit	Attr	Reset Value	Description
18	RW	0x0	ISA_EN ISA Enable. Modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions will be forwarded if they address the last 768 bytes in each 1-KB block. Values: 0x0 (FRWD_DSP): Forward downstream all I/O addresses in the address range defined by the I/O Base and I/O Limit registers 0x1 (FRWD_USP): Forward upstream ISA I/O addresses in the address range defined by the I/O Base and I/O Limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1-KB block. Value After Reset: 0x0
17	RW	0x0	SERR_EN SERR# Enable. This bit controls forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary. Value After Reset: 0x0
16	RW	0x0	PERE Parity Error Response Enable. This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Secondary Status register. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x01	INT_PIN Interrupt PIN. The Interrupt Pin register register that identifies the legacy interrupt Message(s) the Function uses. All encodings other than the defined encodings are reserved. PCI Express defines one legacy interrupt Message for a single Function device and up to four legacy interrupt Messages for a multi-Function device. For a single Function device, only INTA may be used. Any Function on a multi-Function device can use any of the INTx Messages. If a device implements a single legacy interrupt Message, it must be INTA; if it implements two legacy interrupt Messages, they must be INTA and INTB; and so forth. For a multi-Function device, all Functions may use the same INTx Message or each may have its own (up to a maximum of four Functions) or any combination thereof. A single Function can never generate an interrupt request on more than one INTx Message. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (INTA): Map to legacy interrupt Messages for INTA 0x2 (INTB): Map to legacy interrupt Messages for INTB 0x3 (INTC): Map to legacy interrupt Messages for INTC 0x4 (INTD): Map to legacy interrupt Messages for INTD 0x0 (NO_INT): Indicates that the Function uses no legacy interrupt Message(s). Value After Reset: 0x1 Testable: unconstrained
7:0	RW	0xff	INT_LINE Interrupt Line. The Interrupt Line register communicates interrupt line routing information. The register must be implemented by any Function that uses an interrupt pin. Values in this register are programmed by system software and are system architecture specific. The Function itself does not use this value; rather the value in this register is used by device drivers and operating systems. Value After Reset: 0xff

11.4.3.3 DSP_PCIE_PM Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_PM_CAP_ID_NXT_PTR_REG	0x0000	W	0x07C35001	Power Management Capabilities Register
DSP_PCIE_PM_CON_STATUS_REG	0x0004	W	0x00000008	Power Management Control and Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.4 DSP_PCIE_PM Detail Registers Description

DSP_PCIE_PM_CAP_ID_NXT_PTR_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	PME_SUPPORT PME_Support. This 5-bit field indicates the power states in which the function may generate a PME and/or forward PME messages. A value of 0b for any bit indicates that the function is not capable of asserting PME while in that power state. bit(27) X XXX1b - PME can be generated from D0 bit(28) X XX1Xb - PME can be generated from D1 bit(29) X X1XXb - PME can be generated from D2 bit(30) X 1XXXb - PME can be generated from D3hot bit(31) 1 XXXXb - PME can be generated from D3cold Bit 31 (PME can be asserted from D3cold) represents a special case. Functions that set this bit require some sort of auxiliary power source. Implementation specific mechanisms are recommended to validate that the power source is available before setting this bit. Each bit that corresponds to a supported D-state must be set for PCI-PCI Bridge structures representing Ports on Root Complexes/Switches to indicate that the Bridge will forward PME Messages. Bit 31 must only be set if the Port is still able to forward PME Messages when main power is not available. The read value from this field is the write value && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where D1_SUPPORT and D2_SUPPORT are fields in this register. The reset value PME_SUPPORT_n && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where PME_SUPPORT_n is a configuration parameter. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1b Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
26	RW	0x1	D2_SUPPORT D2_Support. If this bit is set, this function supports the D2 Power Management state. Functions that do not support D2 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
25	RW	0x1	D1_SUPPORT D1_Support. If this bit is set, this function supports the D1 Power Management state. Functions that do not support D1 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
24:22	RW	0x7	AUX_CURR Aux_Current. This 3 bit field reports the Vaux auxiliary current requirements for the function. If this function implements the Data Register, the controller hardwires this field to 000b. If PME_Support is 0 xxxxb (PME assertion from D3cold is not supported), the controller hardwires this field to 0000b. For functions where PME_Support is 1 xxxxb (PME assertion from D3cold is supported), and which do not implement the Data field, the encodings defined in Values: apply: Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x7 (_370mA_): 375mA Vaux Max. Current Required 0x6 (_320mA_): 320mA Vaux Max. Current Required 0x5 (_270mA_): 270mA Vaux Max. Current Required 0x4 (_220mA_): 220mA Vaux Max. Current Required 0x3 (_160mA_): 160mA Vaux Max. Current Required 0x2 (_100mA_): 100mA Vaux Max. Current Required 0x1 (_055mA_): 55mA Vaux Max. Current Required 0x0 (SELF_): 0 self powered Value After Reset: 0x7 Testable: unconstrained
21	RW	0x0	DSI Device Specific Initialization. The DSI bit indicates whether special initialization of this function is required. When set, indicates that the function requires a device specific initialization sequence following a transition to the D0uninitialized state. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19	RO	0x0	PME_CLK PME Clock. Does not apply to PCI Express, the controller hardwires it to 0b. Note: This register field is sticky. Value After Reset: 0x0
18:16	RW	0x3	PM_SPEC_VER Version. This field provides the Power Management specification version. The controller hardwires this field to 011b for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0>. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x3 Testable: unconstrained
15:8	RW	0x50	PM_NEXT_POINTER Next Capability Pointer. This field provides an offset into the function's configuration space pointing to the location of next item in the capabilities list. If there are no additional items in the capabilities list, this field is set to 00h. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x50 Testable: unconstrained
7:0	RO	0x01	PM_CAP_ID Capability ID. This field returns 01h to indicate that this is the PCI Power Management Capability. Each function may have only one item in its capability list with Capability ID set to 01h. Value After Reset: 0x1

DSP_PCIE_PM_CON_STATUS_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DATA_REG_ADD_INFO Data. This field is used to report the state dependent data requested by the Data_Select field. The value of this field is scaled by the value reported by the Data_Scale field. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
23	RO	0x0	BUS_PWR_CLK_CON_EN Bus Power/Clock Control Enable. If this field is set, Bus Power/Clock Control is Enable. Value After Reset: 0x0
22	RO	0x0	B2_B3_SUPPORT B2B3 Support for D3hot. If this field is set, B2B3 support for D3hot is available. Value After Reset: 0x0
21:16	RO	0x00	reserved
15	W1C	0x0	PME_STATUS PME_Status. This bit is set when the function normally generates a PME signal. The value of this bit is not affected by the value of the PME_En bit. If PME_Support bit 31 of the Power Management Capabilities register is clear, this bit is permitted to be hardwired to 0b. Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this register value is not modified by Conventional Reset or FLR. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14:13	RO	0x0	DATA_SCALE Data_Scale. This field indicates the scaling factor to be used when interpreting the value of the Data field. The value and meaning of this field varies depending on which data value has been selected by the Data_Select field. For more details, see 7.5.2.3 section of PCI Express Base Specification. Value After Reset: 0x0
12:9	RO	0x0	DATA_SELECT Data_Select. This 4-bit field is used to select which data is to be reported through the Data and Data_Scale field. If the Data field is not implemented, this field must be hardwired to 0000b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	PME_ENABLE PME_En. When set, the function is permitted to generate a PME. When clear, the function is not permitted to generate a PME. If PME_Support is 1 xxxxb (PME generation from D3cold) or the function consumes Aux power and Aux power is available this bit is RWS and the bit is not modified by Conventional Reset or FLR. If PME_Support is 0 xxxxb, this field is not sticky (RW). If PME_Support is 0 0000b, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
7:4	RO	0x0	reserved
3	RW	0x1	NO_SOFT_RST No_Soft_Reset. This bit indicates the state of the function after writing the PowerState field to transition the function from D3hot to D0. When set, this transition preserves internal function state. The function is in D0Active and no additional software intervention is required. When clear, this transition results in undefined internal function state. Regardless of this bit, functions that transition from D3hot to D0 by Fundamental Reset will return to D0Uninitialized with only PME context preserved if PME is supported and enabled. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	POWER_STATE PowerState. This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. You can write to this register; however, the read-back value is the actual power state, not the write value. If you attempt to write an unsupported, optional state to this field, the write operation completes normally; however, the data is discarded and no state change occurs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (D0): D0 power state 0x1 (D1): D1 power state 0x2 (D2): D2 power state 0x3 (D3hot): D3hot D3hot power state Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

11.4.3.5 DSP_PCIE_MSI Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_MSI_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x018A7005	MSI Capability Header and Message Control Register
DSP_PCIE_MSI_CAP_OFF_04H_REG	0x0004	W	0x00000000	Message Address Register for MSI (Offset 04h)
DSP_PCIE_MSI_CAP_OFF_08H_REG	0x0008	W	0x00000000	Message Address Register for MSI (Offset 08h)
DSP_PCIE_MSI_CAP_OFF_0CH_REG	0x000C	W	0x00000000	Message Address Register for MSI (Offset 0Ch)
DSP_PCIE_MSI_CAP_OFF_10H_REG	0x0010	W	0x00000000	Message Address Register for MSI (Offset 10h)
DSP_PCIE_MSI_CAP_OFF_14H_REG	0x0014	W	0x00000000	Message Address Register for MSI (Offset 14h)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.6 DSP_PCIE_MSI Detail Registers Description

DSP_PCIE_MSI_CAP_ID_NEXT_CTRL_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	PCI_MSI_EXT_DATA_EN Extended Message Data Enable. If set, the function is enabled to provide Extended Message Data. If clear, the function is not enabled to provide Extended Message Data. Note: The access attributes of this field are as follows: Wire: No access. Dbi: PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_MSI_EXT_DATA_CAP ? RW : RO Value After Reset: 0x0 Testable: writeAsRead
25	RO	0x0	PCI_MSI_EXT_DATA_CAP Extended Message Data Capable. If set, the function is capable of providing Extended Message Data. If clear, the function does not support providing Extended Message Data. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
24	RO	0x1	PCI_PVM_SUPPORT Per-Vector Masking Capable. If set, the function supports MSI Per-Vector Masking. If clear, the function does not support MSI Per-Vector Masking. This bit must be set if the function is a PF or VF within an SR-IOV Device. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
23	RO	0x1	PCI_MSI_64_BIT_ADDR_CAP 64 bit address capable. If set, the function is capable of sending a 64-bit message address. If clear, the function is not capable of sending a 64-bit message address. This bit must be set if the function is a PCI Express Endpoint. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
22:20	RW	0x0	PCI_MSI_MULTIPLE_MSG_EN Multiple Message Enable. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). The number of allocated vectors is aligned to a power of two. If a function requests four vectors (indicated by a Multiple Message Capable encoding of 010b), system software can allocate either four, two, or one vector by writing a 010b, 001b, or 000b to this field, respectively. When MSI is enabled, a function will be allocated at least 1 vector. All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (_1_VECTOR): 1 vector allocated 0x1 (_2_VECTOR): 2 vectors allocated 0x2 (_4_VECTOR): 4 vectors allocated 0x3 (_8_VECTOR): 8 vectors allocated 0x4 (_16_VECTOR): 16 vectors allocated 0x5 (_32_VECTOR): 32 vectors allocated Value After Reset: 0x0

Bit	Attr	Reset Value	Description
19:17	RW	0x5	PCI_MSI_MULTIPLE_MSG_CAP Multiple Message Capable. System software reads this field to determine the number of requested vectors. The number of requested vectors must be aligned to a power of two (if a function requires three vectors, it requests four by initializing this field to 010b). All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (_1_VECTOR): 1 vector requested 0x1 (_2_VECTOR): 2 vectors requested 0x2 (_4_VECTOR): 4 vectors requested 0x3 (_8_VECTOR): 8 vectors requested 0x4 (_16_VECTOR): 16 vectors requested 0x5 (_32_VECTOR): 32 vectors requested Value After Reset: 0x5 Testable: unconstrained
16	RW	0x0	PCI_MSI_ENABLE MSI Enable. If set and the MSI-X Enable bit in the MSI-X Message Control register is clear, the function is permitted to use MSI to request service and is prohibited from using INTx interrupts. System configuration software sets this bit to enable MSI. A device driver is prohibited from writing this bit to mask a function's service request. For more details on control of INTx interrupts, see section 7.5.1.1 of PCI Express Base Specification. If clear, the function is prohibited from using MSI to request service. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x70	PCI_MSI_CAP_NEXT_OFFSET Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x70 Testable: unconstrained
7:0	RO	0x05	PCI_MSI_CAP_ID Capability ID. Indicates the MSI Capability structure. This field returns a Capability ID of 05h indicating that this is an MSI Capability structure. Value After Reset: 0x5

DSP_PCIE_MSI_CAP_OFF_04H_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	PCI_MSI_CAP_OFF_04H Message Address - System-specified message address. If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG register) is set, the contents of this field specify the DWORD-aligned address (Address[31:02]) for the MSI transaction. Address[1:0] are set to 00b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
1:0	RO	0x0	reserved

DSP_PCIE_MSI_CAP_OFF_08H_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0AH For a function that supports a 32-bit message address, this field contains Extended Message Data (System-specified message data). For the MSI Capability structures without per-vector masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is outside the MSI Capability structure and undefined. For the MSI Capability structures with Per-vector Masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is RsvdP. If the Extended Message Data Enable bit (bit 26 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the DWORD Memory Write transaction uses Extended Message Data for the upper 16 bits; otherwise, it uses 0000h for the upper 16 bits. For a function that supports a 64-bit message address, it contains upper 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: Wire: No access. Dbi: PCI_MSI_64_BIT_ADDR_CAP || `DEFAULT_EXT_MSI_DATA_CAPABLE ? R/W : R Value After Reset: 0x0 Testable: writeAsRead
15:0	RW	0x0000	PCI_MSI_CAP_OFF_08H For a function that supports a 32-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. For a function that supports a 64-bit message address, it contains lower 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_MSI_CAP_OFF_0CH_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0EH For a function that supports a 32-bit message address, this field contains the upper Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). Note: The access attributes of this field are as follows: Wire: No access. Dbi: (!MSI_64_EN && MSI_PVM_EN_VALUE) ? RW: MSI_64_EN && DEFAULT_EXT_MSI_DATA_CAPABLE ? RW : RO Value After Reset: 0x0 Testable: writeAsRead
15:0	RW	0x0000	PCI_MSI_CAP_OFF_0CH For a function that supports a 32-bit message address, this field contains the lower Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. Note: The access attributes of this field are as follows: Wire: No access. Dbi: PCI_MSI_64_BIT_ADDR_CAP || MSI_PVM_EN ? R/W : R Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_MSI_CAP_OFF_10H_REG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	PCI_MSI_CAP_OFF_10H Used for MSI when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For 32-bit contains Pending Bits. For 64-bit, contains Mask Bits. Note: The access attributes of this field are as follows: Wire: No access. Dbi: PCI_MSI_64_BIT_ADDR_CAP && MSI_PVM_EN ? R/W : R Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_MSI_CAP_OFF_14H_REG
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	PCI_MSI_CAP_OFF_14H Pending Bits. For each pending bit that is set, the function has a pending associated message. Value After Reset: 0x0

11.4.3.7 DSP_PCIE_CAP Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	0x0000	W	0x1042B010	PCI Express Capabilities, ID, Next Pointer Register
DSP_PCIE_CAP_DEVICE_CAPABILITIES_REG	0x0004	W	0x00008FC0	Device Capabilities Register
DSP_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS	0x0008	W	0x00002010	Device Control and Status Register
DSP_PCIE_CAP_LINK_CAPABILITIES_REG	0x000C	W	0x00726C43	Link Capabilities Register
DSP_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG	0x0010	W	0x10000000	Link Control and Status Register
DSP_PCIE_CAP_SLOT_CAPABILITIES_REG	0x0014	W	0x00000000	Slot Capabilities Register. Exists Only in RC Mode
DSP_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS	0x0018	W	0x000003C0	Slot Control and Status Register. Exists Only in RC Mode
DSP_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG	0x001C	W	0x00010000	Root Control and Capabilities Register. Exists Only in RC Mode
DSP_PCIE_CAP_ROOT_STATUS_REG	0x0020	W	0x00000000	Root Status Register. Exists Only in RC Mode
DSP_PCIE_CAP_DEVICE_CAPABILITIES2_REG	0x0024	W	0x007C0830	Device Capabilities 2 Register
DSP_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG	0x0028	W	0x00000000	Device Control 2 and Status 2 Register

Name	Offset	Size	Reset Value	Description
DSP_PCIE_CAP_LINK_CAPABILITIES2_REG	0x002C	W	0x0000000E	Link Capabilities 2 Register
DSP_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG	0x0030	W	0x00010003	Link Control 2 and Status 2 Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.8 DSP_PCIE_CAP Detail Registers Description

DSP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x08	PCIE_INT_MSG_NUM PCIE Interrupt Message Number. Interrupt Message Number. This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x8 Testable: unconstrained

Bit	Attr	Reset Value	Description
24	RW	0x0	PCIE_SLOT_IMP Slot Implemented. When set, this bit indicates that the Link associated with this Port is connected to a slot (as compared to being connected to a system-integrated device or being disabled). This bit is valid for Downstream Ports. This bit is undefined for Upstream Ports. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
23:20	RO	0x4	PCIE_DEV_PORT_TYPE Device/Port Type. Indicates the specific type of this PCI Express function. Note: Different functions in a Multi-Function Device can generally be of different types. Defined encodings for functions that implement a Type 00h PCI Configuration Space header are: Defined encodings for functions that implement a Type 01h PCI Configuration Space header are: All other encodings are Reserved. Note: Different Endpoint types have notably different requirements in Section 1.3.2 of PCI Express Base Specification regarding I/O resources, Extended Configuration Space, and other capabilities. Values: 0x0 (PCIE_EP): PCI Express Endpoint 0x1 (PCIE_LEGACY_EP): Legacy PCI Express Endpoint 0x4 (ROOT_PORT_PCIE_RC): Root Port of PCI Express Root Complex 0x5 (USP_PCIE_SWITCH): Upstream Port of PCI Express Switch 0x6 (DSP_PCIE_SWITCH): Downstream Port of PCI Express Switch Value After Reset: 0x4 Testable: untestable Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
19:16	RO	0x2	PCIE_CAP_REG Capability Version. Indicates PCI-SIG defined PCI Express Capability structure version number. A version of the specification that changes the PCI Express Capability structure in a way that is not otherwise identifiable (for example, through a new Capability field) is permitted to increment this field. All such changes to the PCI Express Capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as functions reporting any such Capability Version numbers will contain a PCI Express Capability structure that is compatible with that piece of software. The controller hardwires this field to 2h for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0. Note: This register field is sticky. Value After Reset: 0x2
15:8	RW	0xb0	PCIE_CAP_NEXT_PTR Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0xb0 Testable: unconstrained
7:0	RO	0x10	PCIE_CAP_ID Capability ID. Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. Value After Reset: 0x10

DSP_PCIE_CAP_DEVICE_CAPABILITIES_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28	RW	0x0	PCIE_CAP_FLR_CAP Function Level Reset Capability. A value of 1b indicates the function supports the optional Function Level Reset mechanism described in section 6.6.2 of the PCI Express Base Specification. This bit applies to Endpoints only. For all other function types the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
27:26	RO	0x0	PCIE_CAP_CAP_SLOT_PWR_LMT_SCALE Captured Slot Power Limit Scale. Captured Slot Power Limit Scale (Upstream Ports only). Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit Message or hardwired to 00b (for more details, see section 6.9 of PCI Express Base Specification). Values: 0x0 (_1.0X): 1.0x 0x1 (_0.1X): 0.1x 0x2 (_0.01X): 0.01x 0x3 (_0.001X): 0.001x Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
25:18	RO	0x00	PCIE_CAP_CAP_SLOT_PWR_LMT_VALUE Captured Slot Power Limit Value. Captured Slot Power Limit Value (Upstream Ports only). In combination with the Captured Slot Power Limit Scale value, specifies the upper limit on power available to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Captured Slot Power Limit Scale field except when the Captured Slot Power Limit Scale field equals 00b (1.0x) and the Captured Slot Power Limit Value exceeds EFh, then alternative encodings are used (for more details, see section 7.5.3.9 of PCI Express Base Specification). This value is set by the Set_Slot_Power_Limit Message or hardwired to 00h (for more details, see section 6.9 of PCI Express Base Specification). Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
17:16	RO	0x0	reserved
15	RO	0x1	PCIE_CAP_ROLE_BASED_ERR_REPORT Role-Based Error Reporting. When set, this bit indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be set by all functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
14:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:9	RO	0x7	PCIE_CAP_EP_L1_ACCPT_LATENCY Endpoint L1 Acceptable Latency. This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L1 Acceptable Latency number to compare against the L1 Exit Latencies reported (see below) by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L1 entry can be used with no loss of performance. For functions other than Endpoints, this field is Reserved and the controller hardwires it to 000b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W (Sticky) else R(Sticky) Note: This register field is sticky. Values: 0x0 (MAX_1US): Maximum of 1 us 0x1 (MAX_2US): Maximum of 2 us 0x2 (MAX_4US): Maximum of 4 us 0x3 (MAX_8US): Maximum of 8 us 0x4 (MAX_16US): Maximum of 16 us 0x5 (MAX_32US): Maximum of 32 us 0x6 (MAX_64US): Maximum of 64 us 0x7 (NO_LIMIT): No limit Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
8:6	RW	0x7	PCIE_CAP_EP_L0S_ACCPT_LATENCY Endpoint L0s Acceptable Latency. This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L0s entry can be used with no loss of performance. For functions other than Endpoints, this field is Reserved and the controller hardwires it to 000b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (MAX_64NS): Maximum of 64 ns 0x1 (MAX_128NS): Maximum of 128 ns 0x2 (MAX_256NS): Maximum of 256 ns 0x3 (MAX_512NS): Maximum of 512 ns 0x4 (MAX_1US): Maximum of 1 us 0x5 (MAX_2US): Maximum of 2 us 0x6 (MAX_4US): Maximum of 4 us 0x7 (NO_LIMIT): No limit Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
5	RO	0x0	PCIE_CAP_EXT_TAG_SUPP Extended Tag Field Supported. This bit, in combination with the 10-Bit Tag Requester Supported bit in the Device Capabilities 2 register, indicates the maximum supported size of the Tag field as a Requester. This bit must be set if the 10-Bit Tag Requester Supported bit is set. Note: 8-bit Tag field generation must be enabled by the Extended Tag Field Enable bit in the Device Control register of the Requester Function before 8-bit Tags can be generated by the Requester. See Section 2.2.6.2 of PCI Express Base Specification for interactions with enabling the use of 10-Bit Tags. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (_5b_TAG): 5-bit Tag field supported 0x1 (_8b_TAG): 8-bit Tag field supported Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
4:3	RW	0x0	PCIE_CAP_PHANTOM_FUNC_SUPPORT Phantom Functions Supported. This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers (called Phantom Functions) with the Tag identifier (see Section 2.2.6.2 of PCI Express Base Specification for a description of Tag Extensions). With every Function in an ARI Device, the Phantom Functions Supported field must be set to 00b. The remainder of this field description applies only to non-ARI Multi-Function Devices. This field indicates the number of most significant bits of the Function Number portion of Requester ID that are logically combined with the Tag identifier. Note: Phantom Function support for the function must be enabled by the Phantom Functions Enable field in the Device Control register before the Function is permitted to use the Function Number field in the Requester ID for Phantom Functions. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (NO_PHNATOM_FUNC): No Function Number bits are used for Phantom Functions. Multi-Function Devices are permitted to implement up to 8 independent functions. 0x1 (MAX_1_PHANTOM_PER_FUNC): The most significant bit of the Function number in Requester ID is used for Phantom Functions; a Multi-Function Device is permitted to implement Functions 0-3. Functions 0, 1, 2, and 3 are permitted to use Function Numbers 4, 5, 6, and 7 respectively as Phantom Functions. 0x2 (MAX_3_PHANTOM_PER_FUNC): The two most significant bits of Function Number in Requester ID are used for Phantom Functions; a Multi-Function Device is permitted to implement Functions 0-1. Function 0 is permitted to use Function Numbers 2, 4, and 6 for Phantom Functions. Function 1 is permitted to use Function Numbers 3, 5, and 7 as Phantom Functions. 0x3 (SINGLE_FUNC_MAX_7_PHANTOM_FUNC): All 3 bits of Function Number in Requester ID used for Phantom Functions. The device must have a single Function 0 that is permitted to use all other Function Numbers as Phantom Functions. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
2:0	RW	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE Max_Payload_Size Supported. This field indicates the maximum payload size that the function can support for TLPs. All encodings other than the defined encodings are reserved. The functions of a Multi-Function Device are permitted to report different values for this field. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (MAX_128B_SIZE): 128 bytes max payload size 0x1 (MAX_256B_SIZE): 256 bytes max payload size 0x2 (MAX_512B_SIZE): 512 bytes max payload size 0x3 (MAX_1024B_SIZE): 1024 bytes max payload size 0x4 (MAX_2048B_SIZE): 2048 bytes max payload size 0x5 (MAX_4096B_SIZE): 4096 bytes max payload size Value After Reset: 0x1 Testable: unconstrained

DSP_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	PCIE_CAP_TRANS_PENDING Transactions Pending. Endpoints: When set, this bit indicates that the function has issued Non-Posted Requests that have not been completed. A Function reports this bit cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR. Root and Switch Ports: The controller hardwires this bit to 0b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
20	RO	0x0	PCIE_CAP_AUX_POWER_DETECTED AUX Power Detected. Functions that require Aux power report this bit as set if Aux power is detected by the function. This bit is derived by sampling the sys_aux_pwr_det input. Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
19	RW	0x0	PCIE_CAP_UNSUPPORTED_REQ_DETECTED Unsupported Request Detected. This bit indicates that the function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function Device, each function indicates status of errors as perceived by the respective function. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
18	W1C	0x0	PCIE_CAP_FATAL_ERR_DETECTED Fatal Error Detected. This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
17	W1C	0x0	PCIE_CAP_NON_FATAL_ERR_DETECTED Non-Fatal Error Detected. This bit indicates status of Non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
16	W1C	0x0	PCIE_CAP_CORR_ERR_DETECTED Correctable Error Detected. This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x2	PCIE_CAP_MAX_READ_REQ_SIZE Max_Read_Request_Size. This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For functions that do not generate Read Requests larger than 128 bytes and functions that do not generate Read Requests on their own behalf, the controller implements this field as Read Only (RO) with a value of 000b. Values: 0x0 (MAX_128B_SIZE): 128 bytes maximum Read Request size 0x1 (MAX_256B_SIZE): 256 bytes maximum Read Request size 0x2 (MAX_512B_SIZE): 512 bytes maximum Read Request size 0x3 (MAX_1024B_SIZE): 1024 bytes maximum Read Request size 0x4 (MAX_2048B_SIZE): 2048 bytes maximum Read Request size 0x5 (MAX_4096B_SIZE): 4096 bytes maximum Read Request size 0x6 (RESERVED1): RESERVED 0x7 (RESERVED2): RESERVED Value After Reset: 0x
11	RO	0x0	PCIE_CAP_EN_NO_SNOOP Enable No Snoop. If this bit is set, the function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency (see section 2.2.6.5 in PCI Express Base Specification). Note: Setting this bit to 1b should not cause a function to set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. The controller hardwires this bit 0b if a function would never set the No Snoop attribute in transactions it initiates. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0

Bit	Attr	Reset Value	Description
10	RW	0x0	PCIE_CAP_AUX_POWER_PM_EN Aux Power PM Enable. This bit is derived by sampling the sys_aux_pwr_det input. When set this bit, enables a function to draw Aux power independent of PME Aux power. Functions that require Aux power on legacy operating systems should continue to indicate PME Aux power requirements. Aux power is allocated as requested in the Aux_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register (PMCSR). For Multi-Function devices, a component is allowed to draw Aux power if at least one of the functions has this bit set. Note: Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this bit is not modified by Conventional Reset. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
9	RO	0x0	PCIE_CAP_PHANTOM_FUNC_EN Phantom Functions Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, If this bit is set, it enables a function to use unclaimed functions as Phantom functions to extend the number of outstanding transaction identifiers If this bit is clear, the function is not allowed to use Phantom functions For more details, see section 2.2.6.2 of PCI Express Base Specification. Software should not change the value of this bit while the function has outstanding Non-Posted Requests; otherwise, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_PHANTOM_FUNC_SUPPORT ? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
8	RO	0x0	PCIE_CAP_EXT_TAG_EN Extended Tag Field Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, If the Extended Tag Field Enable bit is set, the function is permitted to use an 8-bit Tag field as a Requester If the Extended Tag Field Enable bit is clear, the Function is restricted to a 5-bit Tag field See section 2.2.6.2 of PCI Express Base Specification for required behavior when the 10-Bit Tag Requester Enable bit is set. If software changes the value of the Extended Tag Field Enable bit while the function has outstanding Non-Posted Requests, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_EXT_TAG_SUPP ? RW : RO Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
7:5	RW	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE_CS Max_Payload_Size. This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported field (PCIE_CAP_MAX_PAYLOAD_SIZE) in the Device Capabilities (DEVICE_CAPABILITIES_REG) register (for more details, see section 7.5.3.3 of PCI Express Base Specification). This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For Functions that support only the 128-byte max payload size, the controller hardwires this field to 000b. System software is not required to program the same value for this field for all the Functions of a Multi-Function device (for more details, see section 2.2.2 of PCI Express Base Specification). For ARI Devices, Max_Payload_Size is determined solely by the setting in Function0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (MAX_128B_SIZE): 128 bytes maximum Read Request size 0x1 (MAX_256B_SIZE): 256 bytes maximum Read Request size 0x2 (MAX_512B_SIZE): 512 bytes maximum Read Request size 0x3 (MAX_1024B_SIZE): 1024 bytes maximum Read Request size 0x4 (MAX_2048B_SIZE): 2048 bytes maximum Read Request size 0x5 (MAX_4096B_SIZE): 4096 bytes maximum Read Request size 0x6 (RESERVED1): RESERVED 0x7 (RESERVED2): RESERVED Value After Reset: 0x0

Bit	Attr	Reset Value	Description
4	RW	0x1	PCIE_CAP_EN_REL_ORDER Enable Relaxed Ordering. If this bit is set, the function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering (for more details, see section 2.2.6.4 and section 2.4 of PCI Express Base Specification). For a function that never sets the Relaxed Ordering attribute in transactions it initiates as a Requester, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
3	RW	0x0	PCIE_CAP_UNSUPPORT_REQ_REP_EN Unsupported Request Reporting Enable. This bit, in conjunction with other bits, controls the signaling of Unsupported Request Errors by sending error Messages (for more details, see section 6.2.5 and section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each Function from point-of-view of the respective Function. Value After Reset: 0x0
2	RW	0x0	PCIE_CAP_FATAL_ERR_REPORT_EN Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_FATAL Messages (for more details, see section 6.2.5 and section 6.2.6 of of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL Message is generated. Value After Reset: 0x0
1	RW	0x0	PCIE_CAP_NON_FATAL_ERR_REPORT_EN Non-Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages (for more details, see section 6.2.5 and Section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each function from point-of-view of the respective Function. For a Root Port, the reporting of Non-fatal errors is internal to the root. No external ERR_NONFATAL Message is generated. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	PCIE_CAP_CORR_ERR_REPORT_EN Correctable Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_COR Messages (for more details, see section 6.2.5, section 6.2.6, and section 6.2.10.2 of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated. Value After Reset: 0x0

DSP_PCIE_CAP_LINK_CAPABILITIES_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	PCIE_CAP_PORT_NUM Port Number. This field indicates the PCI Express Port number for the given PCI Express Link. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
23	RO	0x0	reserved
22	RW	0x1	PCIE_CAP_ASPM_OPT_COMPLIANCE ASPM Optionality Compliance. For a description of this standard PCIe register field, see the PCI Express Specification. Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R
21	RW	0x1	PCIE_CAP_LINK_BW_NOT_CAP ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
20	RO	0x1	PCIE_CAP_DLL_ACTIVE_REP_CAP Data Link Layer Link Active Reporting Capable. For a Downstream Port, the controller hardwires this bit to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable bit of the Slot Capabilities register) or a Downstream Port that supports Link speeds greater than 5.0 GT/s, the controller hardwires this bit to 1b. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Value After Reset: 0x1
19	RW	0x0	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP Surprise Down Error Reporting Capable. For a Downstream Port, this bit must be set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
18	RO	0x0	PCIE_CAP_CLOCK_POWER_MAN Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a Multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the Multi-Function device indicate a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
17:15	RW	0x4	PCIE_CAP_L1_EXIT_LATENCY L1 Exit Latency. This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from ASPM L1 to L0. If ASPM L1 is not supported, the value is undefined. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: CX_NFTS !=CX_COMM_NFTS DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (LESS_THAN_1US): Less than 1us 0x1 (_1US_TO_2US): 1 us to less than 2 us 0x2 (_2US_TO_4US): 2 us to less than 4 us 0x3 (_4US_TO_8US): 4 us to less than 8 us 0x4 (_8US_TO_16US): 8 us to less than 16 us 0x5 (_16US_TO_32US): 16 us to less than 32 us 0x6 (_32US_TO_64US): 32 us to 64 us 0x7 (GREATER_THAN_64US): More than 64 us Value After Reset: 0x4 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
14:12	RW	0x6	PCIE_CAP_L0S_EXIT_LATENCY L0s Exit Latency. This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. If L0s is not supported, the value is undefined; however, see the Implementation Note "Potential Issues With Legacy Software When L0s is Not Supported" in section 5.4.1.1 of PCI Express Base Specification for the recommended value. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: CX_NFTS !=CX_COMM_NFTS DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (LESS_THAN_64NS): Less than 64 ns 0x1 (_64NS_TO_128NS): 64 ns to less than 128 ns 0x2 (_128NS_TO_256NS): 128 ns to less than 256 ns 0x3 (_256NS_TO_512NS): 256 ns to less than 512 ns 0x4 (_512NS_TO_1US): 512 ns to less than 1 us 0x5 (_1US_TO_2US): 1 us to less than 2 us 0x6 (_2US_TO_4US): 2 us to 4 us 0x7 (GREATER_THAN_4US): More than 4 us Value After Reset: 0x6 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:10	RW	0x3	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT Active State Power Management (ASPM) Support. This field indicates the level of ASPM supported on the given PCI Express Link. For more details on ASPM support requirements, see section 5.4.1 of PCI Express Base Specification. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (NO_ASPM_SUP): No ASPM Support 0x1 (L0S_SUP): L0s Supported 0x2 (L1_SUP): L1 Supported 0x3 (L0S_L1_SUP): L0s and L1 Supported Value After Reset: 0x2 Testable: unconstrained

Bit	Attr	Reset Value	Description
9:4	RW	0x04	PCIE_CAP_MAX_LINK_WIDTH Maximum Link Width. This field indicates the maximum Link width (xN - corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. All encodings other than the defined encodings are reserved. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (X1): x1 0x2 (X2): x2 0x4 (X4): x4 0x8 (X8): x8 0xc (X12): x12 0x10 (X16): x16 0x20 (X32): x32 Value After Reset: 0x4 Testable: unconstrained

Bit	Attr	Reset Value	Description
3:0	RW	0x3	PCIE_CAP_MAX_LINK_SPEED Max Link Speed. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. All encodings other than the defined encodings are reserved. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (SUP_LINK_SPEED_FIELD_BIT_0): Supported Link Speeds Vector field bit 0 0x2 (SUP_LINK_SPEED_FIELD_BIT_1): Supported Link Speeds Vector field bit 1 0x3 (SUP_LINK_SPEED_FIELD_BIT_2): Supported Link Speeds Vector field bit 2 0x4 (SUP_LINK_SPEED_FIELD_BIT_3): Supported Link Speeds Vector field bit 3 0x5 (SUP_LINK_SPEED_FIELD_BIT_4): Supported Link Speeds Vector field bit 4 0x6 (SUP_LINK_SPEED_FIELD_BIT_5): Supported Link Speeds Vector field bit 5 0x7 (SUP_LINK_SPEED_FIELD_BIT_6): Supported Link Speeds Vector field bit 6 Value After Reset: 0x3 Testable: unconstrained

DSP_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	W1C	0x0	PCIE_CAP_LINK_AUTO_BW_STATUS Link Autonomous Bandwidth Status. This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Value After Reset: 0x0 Reset Mask: 0x0

Bit	Attr	Reset Value	Description
30	W1C	0x0	PCIE_CAP_LINK_BW_MAN_STATUS Link Bandwidth Management Status. This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: A Link retraining has completed following a write of 1b to the Retrain Link bit. Note: This bit is set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. The default value of this bit is 0b. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
29	RO	0x0	PCIE_CAP_DLL_ACTIVE Data Link Layer Link Active. This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the Data Link Layer Link Active Reporting Capable bit is 1b. Otherwise, the controller hardwires it to 0b. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
28	RW	0x1	PCIE_CAP_SLOT_CLK_CONFIG Slot Clock Configuration. This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference clock on the connector, this bit must be clear. For a Multi-Function Device, each Function must report the same value for this bit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x1 Testable: unconstrained
27	RO	0x0	PCIE_CAP_LINK_TRAINING Link Training. This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches, and the controller hardwires it to 0b. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:20	RO	0x00	PCIE_CAP_NEGO_LINK_WIDTH Negotiated Link Width. This field indicates the negotiated width of the given PCI Express Link. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up. Values: 0x1 (X1): x1 0x2 (X2): x2 0x4 (X4): x4 0x8 (X8): x8 0xc (X12): x12 0x10 (X16): x16 0x20 (X32): x32 Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
19:16	RO	0x0	PCIE_CAP_LINK_SPEED Current Link Speed. This field indicates the negotiated Link speed of the given PCI Express Link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up. Values: 0x1 (SUP_LINK_SPEED_FIELD_BIT_0): Supported Link Speeds Vector field bit 0 0x2 (SUP_LINK_SPEED_FIELD_BIT_1): Supported Link Speeds Vector field bit 1 0x3 (SUP_LINK_SPEED_FIELD_BIT_2): Supported Link Speeds Vector field bit 2 0x4 (SUP_LINK_SPEED_FIELD_BIT_3): Supported Link Speeds Vector field bit 3 0x5 (SUP_LINK_SPEED_FIELD_BIT_4): Supported Link Speeds Vector field bit 4 0x6 (SUP_LINK_SPEED_FIELD_BIT_5): Supported Link Speeds Vector field bit 5 0x7 (SUP_LINK_SPEED_FIELD_BIT_6): Supported Link Speeds Vector field bit 6 Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
15:14	RW	0x0	PCIE_CAP_DRS_SIGNALING_CONTROL DRS Signaling Control. Indicates the mechanism used to report reception of a DRS message. Must be implemented for Downstream Ports with the DRS Supported bit Set in the Link Capabilities 2 Register. Encodings are: If DRS Supported is set, receiving a DRS Message will set DRS Message Received in the Link Status 2 Register but will otherwise have no effect If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, and either MSI or MSI-X is enabled, an MSI or MSI-X interrupt is generated using the vector in Interrupt Message Number (section 7.5.3.2) If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, the Port must send an FRS Message Upstream with the FRS Reason field set to DRS Message Received. Behavior is undefined if this field is set to 10b and the FRS Supported bit in the Device Capabilities 2 Register is Clear. Behavior is undefined if this field is set to 11b. For Downstream Ports with the DRS Supported bit clear in the Link Capabilities 2 register, the controller hardwires this field to 00b. This field is Reserved for Upstream Ports. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES2_REG.DRS_SUPPORTED ? RW : RO Values: 0x0 (DRS_NOT_REPORTED): DRS not Reported 0x1 (DRS_INTRRUPT_EN): DRS Interrupt Enabled 0x2 (FRS_EN): DRS to FRS Signaling Enabled Value After Reset: 0x0 Testable: writeAsRead
13:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	PCIE_CAP_LINK_AUTO_BW_INT_EN Link Autonomous Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
10	RW	0x0	PCIE_CAP_LINK_BW_MAN_INT_EN Link Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
9	RW	0x0	PCIE_CAP_HW_AUTO_WIDTH_DISABLE Hardware Autonomous Width Disable. When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. For components that do not implement the ability autonomously to change Link width, the ciontroller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	PCIE_CAP_EN_CLK_POWER_MAN Enable Clock Power Management. Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: For a non-ARI Multi-Function Device, power-management-configuration software must only Set this bit if all Functions of the Multi-Function Device indicate a 1b in the Clock Power Management bit of the Link Capabilities register. The component is permitted to use the CLKREQ# signal to power manage Link clock only if this bit is Set for all Functions. For ARI Devices, Clock Power Management is enabled solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. The CLKREQ# signal may also be controlled via the L1 PM Substates mechanism. Such control is not affected by the setting of this bit. For Downstream Ports and components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities register), the controller hardwires this bit to 0b. The write value is gated with the PCIE_CAP_CLOCK_POWER_MAN field in LINK_CAPABILITIES_REG. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_CLOCK_POWER_MAN ? RWS : ROS Note: This register field is sticky. Values: 0x0 (PM_DISABLE_LOW_CLKREQ): Clock power management is disabled and device must hold CLKREQ# signal low. 0x1 (CLKREQ_IN_USE): When this bit is set, the device is permitted to use CLKREQ# signal to power manage Link clock according to protocol defined in appropriate form factor specification. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
7	RW	0x0	PCIE_CAP_EXTENDED_SYNCH Extended Synch. When set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state (see section 4.2.4.5 of PCI Express Base Specification) and when in the Recovery state (see section 4.2.6.4.1 of PCI Express Base Specification). This mode provides external devices (for example, logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. For Multi-Function devices if any function has this bit set, then the component must transmit the additional Ordered Sets when exiting L0s or when in Recovery. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6	RW	0x0	PCIE_CAP_COMMON_CLK_CONFIG Common Clock Configuration. When set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. For non-ARI Multi-Function Devices, software must program the same value for this bit in all Functions. If not all Functions are Set, then the component must as a whole assume that its reference clock is not common with the Upstream component. For ARI Devices, Common Clock Configuration is determined solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies. After changing the value in this bit in both components on a Link, software must trigger the Link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
5	RW	0x0	PCIE_CAP_RETRAIN_LINK Retrain Link. A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. If the LTSSM is already in Recovery or Configuration, re-entering Recovery is permitted but not required. If the Port is in DPC when a write of 1b to this bit occurs, the result is undefined. Reads of this bit always return 0b. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. This bit is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read. Note: The access attributes of this field are as follows: Wire: No access. Dbi: see description Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_LINK_DISABLE Link Disable. This bit disables the Link by directing the LTSSM to the Disabled state when set; this bit is Reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. After clearing this bit, software must honor timing requirements defined in Section 6.6.1 with respect to the first Configuration Read following a Conventional Reset. In a DSP that supports crosslink, the controller gates the write value with the CROSS_LINK_EN field in PORT_LINK_CTRL_OFF. Note: The access attributes of this field are as follows: Wire: No access. Dbi: CX_CROSSLINK_ENABLE=1 && PORT_LINK_CTRL_OFF.CROSS_LINK_EN=1||CX_CROSSLINK_ENABLE=0 && dsp=1? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	PCIE_CAP_RCB Read Completion Boundary (RCB). Root Ports: Indicates the RCB value for the Root Port. Refer to section 2.3.1.1 of PCI Express Base Specification for the definition of the parameter RCB. The controller hardwires this bit for a Root Port and returns its RCB support capabilities. Endpoints and Bridges: Optionally set by configuration software to indicate the RCB value of the Root Port Upstream from the Endpoint or Bridge. Refer to Section 2.3.1.1 of PCI Express Base Specification for the definition of the parameter RCB is same as Root Port. Configuration software must only set this bit if the Root Port Upstream from the Endpoint or Bridge reports an RCB value of 128 bytes (a value of 1b in the Read Completion Boundary bit). For functions that do not implement this feature, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Values: 0x0 (_64B): 64 byte 0x1 (_128B): 128 byte Value After Reset: 0x0 Testable: unconstrained
2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	PCIE_CAP_ACTIVE_STATE_LINK_PM_CONTROL Active State Power Management (ASPM) Control. This field controls the level of ASPM enabled on the given PCI Express Link. See section 5.4.1.3 of PCI Express Base Specification for requirements on when and how to enable ASPM. Note: "L0s Entry Enabled" enables the Transmitter to enter L0s. If L0s is supported, the Receiver must be capable of entering L0s even when the Transmitter is disabled from entering L0s (00b or 10b). ASPM L1 must be enabled by software in the Upstream component on a Link prior to enabling ASPM L1 in the Downstream component on that Link. When disabling ASPM L1, software must disable ASPM L1 in the Downstream component on a Link prior to disabling ASPM L1 in the Upstream component on that Link. ASPM L1 must only be enabled on the Downstream component if both components on a Link support ASPM L1. For Multi-Function Devices (including ARI Devices), it is recommended that software program the same value for this field in all Functions. For non-ARI Multi-Function Devices, only capabilities enabled in all Functions are enabled for the component as a whole. For ARI Devices, ASPM Control is determined solely by the setting in Function0, regardless of Function 0's D-state. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Software must not enable L0s in either direction on a given Link unless components on both sides of the Link each support L0s; otherwise, the result is undefined. Values: 0x0 (DISABLED): Disabled 0x1 (L0S_ENTRY_EN): L0s Entry Enabled 0x2 (L1_ENTRY_En): L1 Entry Enabled 0x3 (L0S_L1_ENTRY_EN): L0s and L1 Entry Enabled Value After Reset: 0x0

DSP_PCIE_CAP_SLOT_CAPABILITIES_REG
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	PCIE_CAP_PHY_SLOT_NUM Physical Slot Number. This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
18	RW	0x0	PCIE_CAP_NO_CMD_CPL_SUPPORT No Command Completed Support. When set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
17	RW	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK Electromechanical Interlock Present. When set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
16:15	RW	0x0	PCIE_CAP_SLOT_POWER_LIMIT_SCALE Slot Power Limit Scale. Specifies the scale used for the Slot Power Limit Value (for more details, see Section 6.9 of PCI Express Base Specification). This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Values: 0x0 (_1.0X): 1.0x 0x1 (_0.1X): 0.1x 0x2 (_0.01X): 0.01x 0x3 (_0.001X): 0.001x Value After Reset: 0x0 Testable: unconstrained
14:7	RW	0x00	PCIE_CAP_SLOT_POWER_LIMIT_VALUE Slot Power Limit Value. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot (for more detais, see Section 6.9 of PCI Express Base Specification) or by other means to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b (1.0x) and Slot Power Limit Value exceeds EFh, the alternative encodings defined in Values: are used. Value F3h to FFh are Reserved for Slot Power Limit values above 300 W. This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Values: 0xf0 (_250W_LIMIT): 250 W Slot Power Limit 0xf1 (_275W_LIMIT): 275 W Slot Power Limit 0xf2 (_300W_LIMIT): 300 W Slot Power Limit Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
6	RW	0x0	PCIE_CAP_HOT_PLUG_CAPABLE Hot-Plug Capable. When set, this bit indicates that this slot is capable of supporting hot-plug operations. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
5	RW	0x0	PCIE_CAP_HOT_PLUG_SURPRISE Hot-Plug Surprise. When set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
4	RW	0x0	PCIE_CAP_POWER_INDICATOR Power Indicator Present. When set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
3	RW	0x0	PCIE_CAP_ATTENTION_INDICATOR Attention Indicator Present. When set, this bit indicates that an Attention Indicator is electrically controlled by the chassis. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
2	RW	0x0	PCIE_CAP_MRL_SENSOR MRL Sensor Present. When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
1	RW	0x0	PCIE_CAP_POWER_CONTROLLER Power Controller Present. When set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor). Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
0	RW	0x0	PCIE_CAP_ATTENTION_INDICATOR_BUTTON Attention Button Present. When set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained

DSP_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	W1C	0x0	PCIE_CAP_DLL_STATE_CHANGED Data Link Layer State Changed. This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
23	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_STATUS Electromechanical Interlock Status. If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock. Values: 0x0 (DISENGAGED): Electromechanical Interlock Disengaged 0x1 (ENGAGED): Electromechanical Interlock Engaged Value After Reset: 0x0
22	RO	0x0	PCIE_CAP_PRESENCE_DETECT_STATE Presence Detect State. This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. This bit must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), the controller hardwires this bit to 1b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Values: 0x0 (EMPTY_SLOT): Slot Empty 0x1 (ADAPTER_PRESENT_IN_SLOT): Adapter Present in slot Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
21	RO	0x0	PCIE_CAP_MRL_SENSOR_STATE MRL Sensor State. This bit reports the status of the MRL sensor if implemented. Encodings are define as above. Values: 0x0 (MRL_CLOSED): MRL Closed 0x1 (MRL_OPEN): MRL Open Value After Reset: 0x0

Bit	Attr	Reset Value	Description
20	W1C	0x0	PCIE_CAP_CMD_CPLD Command Completed. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, the controller hardwires this bit to 0b. Value After Reset: 0x0
19	W1C	0x0	PCIE_CAP_PRESENCE_DETECTED_CHANGED Presence Detect Changed. This bit is set when the value reported in the Presence Detect State bit is changed. Value After Reset: 0x0
18	W1C	0x0	PCIE_CAP_MRL_SENSOR_CHANGED MRL Sensor Changed. If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set. Value After Reset: 0x0
17	W1C	0x0	PCIE_CAP_POWER_FAULT_DETECTED Power Fault Detected. If a Power Controller that supports power fault detection is implemented, this bit issSet when the Power Controller detects a power fault at this slot. Note: Depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set. Value After Reset: 0x0
16	W1C	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED Attention Button Pressed. If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set. Value After Reset: 0x0
15:13	RO	0x0	reserved
12	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED_EN Data Link Layer State Changed Enable. If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11	WO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_CTRL Electromechanical Interlock Control. If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
10	RW	0x0	PCIE_CAP_POWER_CONTROLLER_CTRL Power Controller Control. If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. Note: In some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. If the Power Controller Present bit in the Slot Capabilities register is clear, then writes to this bit have no effect and the read value of this bit is undefined. Values: 0x0 (PWR_ON): Power On 0x1 (PWR_OFF): Power Off Value After Reset: 0x0
9:8	RW	0x3	PCIE_CAP_POWER_INDICATOR_CTRL Power Indicator Control. If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Power Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b. Values: 0x0 (RESERVED): Reserved 0x1 (ON): On 0x2 (BLINK): Blink 0x3 (OFF): Off Value After Reset: 0x3

Bit	Attr	Reset Value	Description
7:6	RW	0x3	PCIE_CAP_ATTENTION_INDICATOR_CTRL Attention Indicator Control. If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b. Values: 0x0 (RESERVED): Reserved 0x1 (ON): On 0x2 (BLINK): Blink 0x3 (OFF): Off Value After Reset: 0x3
5	RW	0x0	PCIE_CAP_HOT_PLUG_INT_EN Hot-Plug Interrupt Enable. When set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is clear, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
4	RW	0x0	PCIE_CAP_CMD_CPL_INT_EN Command Completed Interrupt Enable. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), when set, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, the controller hardwires this bit must to 0b. Write value is gated with PCIE_CAP_NO_CMD_CPL_SUPPORT field in SLOT_CAPABILITIES_REG. Note: The access attributes of this field are as follows: Wire: No access. Dbi: SLOT_CAPABILITIES_REG.PCIE_CAP_NO_CMD_CPL_SUPPORT ? RO : RW Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	PCIE_CAP_PRESENCE_DETECT_CHANGE_EN Presence Detect Changed Enable. When set, this bit enables software notification on a presence detect changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
2	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED_EN MRL Sensor Changed Enable. When set, this bit enables software notification on a MRL sensor changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
1	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED_EN Power Fault Detected Enable. When set, this bit enables software notification on a power fault event (for more details, see Section 6.7.3 of PCI Express Base Specification). If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
0	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED_EN Attention Button Pressed Enable. When set to 1b, this bit enables software notification on an attention button pressed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0

DSP_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x1	PCIE_CAP_CRS_SW_VISIBILITY CRS Software Visibility Capable. When set, this bit indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W (Sticky) else R (Sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved
4	RW	0x0	PCIE_CAP_CRS_SW_VISIBILITY_EN CRS Software Visibility Enable. When set, this bit enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). For Root Ports that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: ROOT_CONTROL_ROOT_CAPABILITIES_REG.PCIE_CAP_CRS_SW_VISIBILITY ? RW : RO Value After Reset: 0x0 Testable: writeAsRead
3	RW	0x0	PCIE_CAP_PME_INT_EN PME Interrupt Enable. When set, this bit enables PME interrupt generation upon receipt of a PME Message as reflected in the PME Status bit (for more details, see Table 7-29 of PCI Express Base Specification). A PME interrupt is also generated if the PME Status bit is set when this bit is changed from clear to set. Value After Reset: 0x0
2	RW	0x0	PCIE_CAP_SYS_ERR_ON_FATAL_ERR_EN System Error on Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Fatal error (ERR_FATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific. Value After Reset: 0x0
1	RW	0x0	PCIE_CAP_SYS_ERR_ON_NON_FATAL_ERR_EN System Error on Non-Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Non-fatal error (ERR_NONFATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific. Value After Reset: 0x0
0	RW	0x0	PCIE_CAP_SYS_ERR_ON_CORR_ERR_EN System Error on Correctable Error Enable. If set, this bit indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific. Value After Reset: 0x0

DSP_PCIE_CAP_ROOT_STATUS_REG
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	PCIE_CAP_PME_PENDING PME Pending. This bit indicates that another PME is pending when the PME Status bit is s et. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the PME Requester ID field appropriately. The PME Pending bit is cleared by hardware if no more PMEs are pending. Value After Reset: 0x0
16	W1C	0x0	PCIE_CAP_PME_STATUS PME Status. This bit indicates that PME was asserted by the PME Requester indicated in the PME Requester ID field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1b. Value After Reset: 0x0
15:0	RO	0x0000	PCIE_CAP_PME_REQ_ID PME Requester ID. This field indicates the PCI Requester ID of the last PME Requester. This field is only valid when the PME Status bit is set. Value After Reset: 0x0

DSP_PCIE_CAP_DEVICE_CAPABILITIES2_REG

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:22	RW	0x1	PCIE_CAP2_CFG_MAX_END2END_TLP_PRFXS Max End-End TLP Prefixes. Indicates the maximum number of End-End TLP Prefixes supported by this Function. For more details, see Section 2.2.10.2 of PCI Express Base Specification. If End-End TLP Prefix Supported is clear, this field is RsvdP. Different Root Ports that have the End-End TLP Prefix Supported bit set are permitted to report different values for this field. For Switches where End-End TLP Prefix Supported is set, this field must be 00b indicating support for up to four End-End TLP Prefixes. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (ONE_END_END_TLP_PREFIX): 1 End-End TLP Prefix 0x2 (TWO_END_END_TLP_PREFIX): 2 End-End TLP Prefixes 0x3 (THREE_END_END_TLP_PREFIX): 3 End-End TLP Prefixes 0x0 (FOUR_END_END_TLP_PREFIX): 4 End-End TLP Prefixes Value After Reset: 0x1 Testable: unconstrained
21	RW	0x1	PCIE_CAP2_CFG_END2END_TLP_PRFX_SUPPORT End-End TLP Prefix Supported. Indicates whether End-End TLP Prefix support is offered by a Function. Values are: All Ports of a Switch must have the same value for this bit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (NO_SUP): No Support 0x1 (SUP): Support is provided to receive TLPs containing End-End TLP Prefixes. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
20	RW	0x1	PCIE_CAP2_CFG_EXTND_FMT_SUPPOR Extended Fmt Field Supported. If set, the Function supports the 3-bit definition of the Fmt field. If clear, the Function supports a 2-bit definition of the Fmt field. For more details, see section 2.2 of PCI Express Base Specification. Must be set for Functions that support End-End TLP Prefixes. All Functions in an Upstream Port must have the same value for this bit. Each Downstream Port of a component may have a different value for this bit. It is strongly recommended that Functions support the 3-bit definition of the Fmt field. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:18	RO	0x3	PCIE_CAP_OBFF_SUPPORT OBFF Supported. This field indicates if OBFF is supported and, if so, what signaling mechanism is used. The value reported in this field must indicate support for WAKE# signaling only if: for a Downstream Port, driving the WAKE# signal for OBFF is supported and the connector or component connected Downstream is known to receive that same WAKE# signal for an Upstream Port, receiving the WAKE# signal for OBFF is supported and, if the component is on an add-in-card, that the component is connected to the WAKE# signal on theconnector. Root Ports, Switch Ports, and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this field. For Bridges and Ports that do not implement this capability, the controller hardwires this field to 00b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky. Values: 0x0 (NOT_SUP): OBFF Not Supported 0x1 (SUP_USING_MSG): OBFF supported using Message signaling only 0x2 (SUP_USING_WAKE): OBFF supported using WAKE# signaling only 0x3 (SUP_USING_MSG_AND_WAKE): OBFF supported using WAKE# and Message signaling Value After Reset: 0x3 Testable: unconstrained
17	RO	0x0	PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT 10-Bit Tag Requester Supported. If this bit is set, the Function supports 10-Bit Tag Requester capability; otherwise, the Function does not. This bit must not be set if the 10-Bit Tag Completer Supported bit is clear. Note: 10-Bit Tag field generation must be enabled by the 10-Bit Tag Requester Enable bit in the Device Control 2 register of the Requester Function before 10-Bit Tags can be generated by the Requester. For more details, see section 2.2.6.2. of PCI Express Base Specification. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
16	RO	0x0	PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT 10-Bit Tag Completer Supported. If this bit is set, the Function supports 10-Bit Tag Completer capability; otherwise, the Function does not. For more details, see section 2.2.6.2. of PCI Express Base Specification. Value After Reset: 0x0
15:14	RO	0x0	PCIE_CAP2_LN_SYS_CLS LN System CLS. Applicable only to Root Ports and RCRBs; must be 00b for all other Function types. This field indicates if the Root Port or RCRB supports LN protocol as an LN Completer, and if so, what cacheline size is in effect. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (LN_COMPLETER_NO_SUP): LN Completer either not supported or not in effect 0x1 (LN_COMPLETER_64B_CACHE): LN Completer with 64-byte cachelines in effect 0x2 (LN_COMPLETER_128B_CACHE): LN Completer with 128-byte cachelines in effect Value After Reset: 0x0
13	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_1 TPH Completer Supported Bit 1. Value After Reset: 0x0
12	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_0 TPH Completer Supported Bit 0. Value of this bit along with TPH Completer Supported Bit 1 indicates Completer support for TPH or Extended TPH. Applicable only to Root Ports and Endpoints. For all other Functions, this field is Reserved. For more details, see section 6.17 of PCI Express Base Specification. Values: 0x0 (TPH_EXT_TPH_CMPL_NOT_SUP_OR_RSVD): TPH and Extended TPH Completer not supported (if TPH Completer Supported Bit is 0) or Reserved ((if TPH Completer Supported Bit is 1). 0x1 (TPH_SUP_EXT_TPH_NOT_SUP_OR_BOTH_SUPP): TPH Completer supported; Extended TPH Completer not supported(if TPH Completer Supported Bit is 0) or Both TPH and Extended TPH Completer supported ((if TPH Completer Supported Bit is 1). Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11	RW	0x1	PCIE_CAP_LTR_SUPP LTR Mechanism Supported. A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. Root Ports, Switches and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this bit. For Bridges and other Functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
10	RO	0x0	PCIE_CAP_NO_RO_EN_PR2PR_PAR No RO-enabled PR-PR Passing. If this bit is set, the routing element never carries out the passing permitted by Table 2-39 of PCI Express Base Specification entry A2b that is associated with the Relaxed Ordering Attribute field being Set. This bit applies only for Switches and RCs that support peer-to-peer traffic between Root Ports. This bit applies only to Posted Requests being forwarded through the Switch or RC and does not apply to traffic originating or terminating within the Switch or RC itself. All Ports on a Switch or RC must report the same value for this bit. For all other functions, this bit must be 0b. Value After Reset: 0x1
9	RO	0x0	PCIE_CAP_128_CAS_CPL_SUPP 128-bit CAS Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification. Value After Reset: 0x0
8	RO	0x0	PCIE_CAP_64_ATOMIC_CPL_SUPP 64-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
7	RO	0x0	PCIE_CAP_32_ATOMIC_CPL_SUPP 32-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification. Value After Reset: 0x0
6	RO	0x0	PCIE_CAP_ATOMIC_ROUTING_SUPP AtomicOp Routing Supported. Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports; must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification. Value After Reset: 0x0
5	RO	0x1	PCIE_CAP_ARI_FORWARD_SUPPORT ARI Forwarding Supported. Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. For more details, see section 6.13 of PCI Express Base Specification. Value After Reset: 0x1
4	RO	0x1	PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT Completion Timeout Disable Supported. A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports. For all other Functions this field is Reserved and the controller hardwires this bit to 0b. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_RANGE Completion Timeout Ranges Supported. This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50 us to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s Bits are set according to the list below to show timeout value ranges supported. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms. Values: 0x0 (NOT_SUP): Completion Timeout programming not supported, the Function must implement a timeout value in the range 50 us to 50 ms. 0x1 (RANGE_A): Range A 0x2 (RANGE_B): Range B 0x3 (RANGE_A_B): Ranges A and B 0x6 (RANGE_B_C): Ranges B and C 0x7 (RANGE_A_B_C): Ranges A, B, and C 0xe (RANGE_B_C_D): Ranges B, C, and D 0xf (RANGE_A_B_C_D): Ranges A, B, C, and D Value After Reset: 0x0

DSP_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	PCIE_CTRL2_CFG_END2END_TLP_PFX_BLCK End-End TLP Prefix Blocking. Controls whether the routing function is permitted to forward TLPs containing an End-End TLP Prefix. This bit affects TLPs that exit the Switch/Root Complex using the associated Port. It does not affect TLPs forwarded internally within the Switch/Root Complex. It does not affect TLPs that enter through the associated Port, that originate in the associated Port or originate in a Root Complex Integrated Device integrated with the associated Port. Blocked TLPs are reported by the TLP Prefix Blocked Error. This bit is hardwired to 1b in Root Ports that support End-End TLP Prefixes but do not support forwarding of End-End TLP Prefixes. This bit is applicable to Root Ports and Switch Ports where the End-End TLP Prefix Supported bit is set. This bit is not applicable and is RsvdP in all other cases. Note: The access attributes of this field are as follows: Wire: No access. Dbi: DEVICE_CAPABILITIES2_REG.PCIE_CAP2_CFG_END2END_TLP_PRFX_SUPPORT ? RW : RO Values: 0x0 (FORWARDING_EN): Forwarding Enabled, Function is permitted to send TLPs with End-End TLP Prefixes. 0x1 (FORWARDING_BL): Forwarding Blocked, Function is not permitted to send TLPs with End-End TLP Prefixes. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
14:13	RW	0x0	PCIE_CAP_OBFF_EN OBFF Enable. This field enables the OBFF mechanism and selects the signaling method. For more details on these encodings, see section 6.19 of PCI Express Base Specification. This field is required for all Ports that support the OBFF Capability. For a Multi-Function Device associated with an Upstream Port of a Device that implements OBFF, the field in Function 0 is of type RW, and only Function 0 controls the Component's behavior. In all other Functions of that Device, this field is of type RsvdP. Ports that do not implement OBFF are permitted to hardwire this field to 00b Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_OBFF_SUPPORT) then R/W else R Values: 0x0 (DISABLED): Disabled 0x1 (EN_USING_MSG_SIG_A): Enabled using Message signaling [Variation A] 0x2 (EN_USING_MSG_SIG_B): Enabled using Message signaling [Variation B] 0x3 (EN_USING_WAKE_SIG): Enabled using WAKE# signaling Value After Reset: 0x0 Testable: writeAsRead
12:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	PCIE_CAP_LTR_EN LTR Mechanism Enable. When set to 1b, this bit enables Upstream Ports to send LTR messages and Downstream Ports to process LTR Messages. For a Multi-Function Device associated with an Upstream Port of a device that implements LTR, the bit in Function 0 is RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is RsvdP. Functions that do not implement the LTR mechanism are permitted to hardwire this bit to 0b. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. The write value is gated with the PCIE_CAP_LTR_SUPP field of DEVICE_CAPABILITIES2_REG. Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_LTR_SUPP) then R/W else R Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
9:6	RO	0x0	reserved
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT_CS ARI Forwarding Enable. When set, the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. For more details, see Section 6.13 of PCI Express Base Specification. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_CPL_TIMEOUT_DISABLE Completion Timeout Disable. When set, this bit disables the Completion Timeout mechanism. This bit is required for all Functions that support the Completion Timeout Disable Capability. Functions that do not support this optional capability are permitted to hardwire this bit to 0b Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding Requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding Requests. If this is done, it is permitted to base the start time for each Request on either the time this bit was cleared or the time each Request was issued. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_VALUE Completion Timeout Value. In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and controller hardwires it to 0000b. A Function that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50 us to 50 ms. Functions that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Ranges Supported field. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms. Values available if Range A (50 us to 10 ms) programmability range is supported: Values available if Range B (10 ms to 250 ms) programmability range is supported: Values available if Range C (250 ms to 4 s) programmability range is supported: Values available if the Range D (4 s to 64 s) programmability range is supported: Software is permitted to change the value in this field at any time. For Requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding Requests, and is permitted to base the start time for each Request either on when this value was changed or on when each request was issued. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (DEFAULT): Default range: 50 us to 50 ms 0x1 (_50_TO_100_US): 50 us to 100 us 0x2 (_1_TO_10_MS): 1 ms to 10 ms 0x5 (_16_TO_55_MS): 16 ms to 55 ms 0x6 (_65_TO_210_MS): 65 ms to 210 ms 0x9 (_260_TO_900_MS): 260 ms to 900 ms 0xa (_1_TO_3_5_S): 1 s to 3.5 s 0xd (_4_TO_13_S): 4 s to 13 s 0xe (_17_TO_64_S): 17 s to 64 s Value After Reset: 0x0

DSP_PCIE_CAP_LINK_CAPABILITIES2_REG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RO	0x0	PCIE_CAP_CROSS_LINK_SUPPORT Crosslink Supported. When set to 1b, this bit indicates that the associated Port supports crosslinks (for more details, see section 4.2.6.3.1 of PCI Express Base Specification). When set to 0b on a Port that supports Link speeds of 8.0 GT/s or higher, this bit indicates that the associated Port does not support crosslinks. When set to 0b on a Port that only supports Link speeds of 2.5 GT/s or 5.0 GT/s, this bit provides no information regarding the Port's level of crosslink support. It is recommended that this bit be Set in any Port that supports crosslinks even though doing so is only required for Ports that also support operating at 8.0 GT/s or higher Link speeds. Note: Software should use this bit when referencing fields whose definition depends on whether or not the Port supports crosslinks (for more details, see section 7.7.3.4 of PCI Express Base Specification). Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions. Value After Reset: 0x0
7:1	RO	0x07	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR Supported Link Speeds Vector. This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. For more details, see section 8.2.1 of PCI Express Base Specification. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bit 4 32.0 GT/s Bits 6:5 RsvdP Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions. This field has a default of (PCIE_CAP_MAX_LINK_SPEED == 0101) ? 0011111 : (PCIE_CAP_MAX_LINK_SPEED == 0100) ? 0001111 : (PCIE_CAP_MAX_LINK_SPEED == 0011) ? 0000111 : (PCIE_CAP_MAX_LINK_SPEED == 0010) ? 0000011 : 0000001 where PCIE_CAP_MAX_LINK_SPEED is a field in the LINK_CAPABILITIES_REG register. Value After Reset: 0x7 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
0	RO	0x0	reserved

DSP_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	W1C	0x0	PCIE_CAP_LINK_EQ_REQ Link Equalization Request 8.0 GT/s. This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link. For more details, see sections 4.2.3 and 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
20	RO	0x0	PCIE_CAP_EQ_CPL_P3 EEqualization 8.0 GT/s Phase 3 Successful. When set to 1b, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
19	RO	0x0	PCIE_CAP_EQ_CPL_P2 Equalization 8.0 GT/s Phase 2 Successful. When set to 1b, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
18	RO	0x0	PCIE_CAP_EQ_CPL_P1 Equalization 8.0 GT/s Phase 1 Successful. When set to 1b, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
17	RO	0x0	PCIE_CAP_EQ_CPL Equalization 8.0 GT/s Complete. When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 8.0 GT/s data rate has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
16	RO	0x1	PCIE_CAP_CURR_DEEMPHASIS Current De-emphasis Level. When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For components that support speeds greater than 2.5 GT/s, Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions of the Port. In M-PCIe mode this register is always 0x0. In C-PCIe mode, its contents are derived by sampling the PIPE. Values: 0x1 (_3_5DB): -3.5 dB 0x0 (_6DB): -6 dB Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:12	RW	0x0	PCIE_CAP_COMPLIANCE_PRESET Compliance Preset/De-emphasis. For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. The encodings are defined in section 4.2.3.2 of PCI Express Base Specification . Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This field sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. When the Link is operating at 2.5 GT/s, the setting of this field has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this field to 0000b. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. This field is intended for debug and compliance testing purposes. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (_3_5_DB): -3.5 dB (for 5.0 GT/s Data Rate) 0x0 (_6_DB): -6 dB (for 5.0 GT/s Data Rate) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11	RW	0x0	PCIE_CAP_COMPLIANCE_SOS Compliance SOS. When set to 1b, the LTSSM is required to send SKP Ordered Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
10	RW	0x0	PCIE_CAP_ENTER_MODIFIED_COMPLIANCE Enter Modified Compliance. When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
9:7	RW	0x0	PCIE_CAP_TX_MARGIN Transmit Margin, This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see Chapter 4 of PCI Express Base Specification for details of how the Transmitter voltage level is determined in various states). 001b-111b: As defined in Section 8.3.4 not all encodings are required to be implemented. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 000b. This field is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: This register field is sticky. Values: 0x0 (NORMAL_RANGE): Normal operating range Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
6	RO	0x0	PCIE_CAP_SEL_DEEMPHASIS Selectable De-emphasis. When the Link is operating at 5.0 GT/s speed, this bit is used to control the transmit de-emphasis of the link in specific situations. For more details, see section 4.2.6 of PCI Express Base Specification. When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (_3_5_DB): -3.5 dB 0x0 (_6_DB): -6 dB Value After Reset: 0x0 Testable: unconstrained
5	RW	0x0	PCIE_CAP_HW_AUTO_SPEED_DISABLE Hardware Autonomous Speed Disable. When set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_ENTER_COMPLIANCE Enter Compliance. Software is permitted to force a Link to enter Compliance mode (at the speed indicated in the Target Link Speed field and the de-emphasis/preset level indicated by the Compliance Preset/De-emphasis field) by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3:0	RW	0x3	PCIE_CAP_TARGET_LINK_SPEED Target Link Speed. For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the desired target Link speed. All encodings other than the defined encodings are reserved. If a value is written to this field that does not correspond to a supported speed (as indicated by the Supported Link Speeds Vector), the result is undefined. If either of the Enter Compliance or Enter Modified Compliance bits are implemented, then this field must also be implemented. The default value of this field is the highest Link speed supported by the component (as reported in the Max Link Speed field of the Link Capabilities register) unless the corresponding platform/form factor requires a different default value. For both Upstream and Downstream Ports, this field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a Link into compliance mode. For Upstream Ports, if the Enter Compliance bit is Clear, this field is permitted to have no effect. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0000b. In M-PCIe mode, the contents of this field are derived from other registers. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (SUP_LINK_SPEED_VECTOR_BIT_0): Supported Link Speeds Vector field bit 0 0x2 (SUP_LINK_SPEED_VECTOR_BIT_1): Supported Link Speeds Vector field bit 1 0x3 (SUP_LINK_SPEED_VECTOR_BIT_2): Supported Link Speeds Vector field bit 2 0x4 (SUP_LINK_SPEED_VECTOR_BIT_3): Supported Link Speeds Vector field bit 3 0x5 (SUP_LINK_SPEED_VECTOR_BIT_4): Supported Link Speeds Vector field bit 4 0x6 (SUP_LINK_SPEED_VECTOR_BIT_5): Supported Link Speeds Vector field bit 5 0x7 (SUP_LINK_SPEED_VECTOR_BIT_6): Supported Link Speeds Vector field bit 6 Value After Reset: 0x3 Testable: unconstrained

11.4.3.9 DSP_PCIE_MSIX Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_MSIX_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x003F0011	MSI-X Capability ID, Next Pointer, Control Registers
DSP_PCIE_MSIX_TABLE_OFFSET_REG	0x0004	W	0x00020004	MSI-X Table Offset and BIR Register
DSP_PCIE_MSIX_PBA_OFFSET_REG	0x0008	W	0x00028004	MSI-X PBA Offset and BIR Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.10 DSP_PCIE_MSIX Detail Registers Description

DSP_PCIE_MSIX_CAP_ID_NEXT_CTRL_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	PCI_MSIX_ENABLE MSI-X Enable. If Set and the MSI Enable bit in the MSI Message Control Register for MSI is Clear, the Function is permitted to use MSI-X to request service and is prohibited from using INTx interrupts (if implemented). System configuration software Sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a Function's service request. If Clear, the Function is prohibited from using MSI-X to request service. Value After Reset: 0x0
30	RW	0x0	PCI_MSIX_FUNCTION_MASK Function Mask. If Set, all of the vectors associated with the Function are masked, regardless of their per-vector Mask bit values. If Clear, each vector's Mask bit determines whether the vector is masked or not. Setting or Clearing the MSI-X Function Mask bit has no effect on the value of the per-vector Mask bits. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
29:27	RO	0x0	reserved

Bit	Attr	Reset Value	Description
26:16	RW	0x03f	PCI_MSIX_TABLE_SIZE MSI-X Table Size. System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1. For example, a returned value of 000 0000 0011b indicates a table size of 4. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table Size" (PCI_MSIX_TABLE_SIZE field in SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_TABLE_SIZE field in the PF PCI_MSIX_CAP_ID_NEXT_CTRL_REG register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x7f Testable: unconstrained
15:8	RW	0x00	PCI_MSIX_CAP_NEXT_OFFSET MSI-X Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
7:0	RO	0x11	PCI_MSIX_CAP_ID MSI-X Capability ID. This field indicates the MSI-X Capability structure. This field must return a Capability ID of 11h indicating that this is an MSI-X Capability structure. Value After Reset: 0x11

DSP_PCIE_MSIX_TABLE_OFFSET_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RW	0x00004000	PCI_MSIX_TABLE_OFFSET MSI-X Table Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table Offset" (PCI_MSIX_TABLE_OFFSET field in SHADOW_MSIX_TABLE_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_TABLE_OFFSET field in the PF MSIX_TABLE_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x4000 Testable: unconstrained

Bit	Attr	Reset Value	Description
2:0	RW	0x4	PCI_MSIX_BIR MSI-X Table BAR Indicator Register Field. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI , is used to map the Function's MSI-X Table into Memory Space. All encodings other than the defined encodings are reserved. For a 64-bit Base Address Register , the Table BIR indicates the lower DWORD. For Functions with Type 1 Configuration Space headers, BIR values 2 through 5 are also Reserved. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table BAR Indicator Register" (PCI_MSIX_BIR field in SHADOW_MSIX_TABLE_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_BIR field in the PF MSIX_TABLE_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (BAR_10): Base Address Register 10h 0x1 (BAR_14): Base Address Register 14h 0x2 (BAR_18): Base Address Register 18h 0x3 (BAR_1C): Base Address Register 1Ch 0x4 (BAR_20): Base Address Register 20h 0x5 (BAR_24): Base Address Register 24h Value After Reset: 0x4 Testable: unconstrained

DSP_PCIE_MSIX_PBA_OFFSET_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RW	0x00005000	PCI_MSIX_PBA_OFFSET MSI-X PBA Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. SRIOV Note: All VFs in a single PF have the same value for "MSI-X PBA Offset" (PCI_MSIX_PBA_OFFSET field in SHADOW_MSIX_PBA_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_PBA_OFFSET field in the PF MSIX_PBA_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x5000 Testable: unconstrained
2:0	RW	0x4	PCI_MSIX_PBA_BIR MSI-X PBA BIR. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the Table BIR . SRIOV Note: All VFs in a single PF have the same value for "MSI-X PBA BIR" (PCI_MSIX_PBA_BIR field in SHADOW_MSIX_PBA_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_PBA_BIR field in the PF MSIX_PBA_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x4 Testable: unconstrained

11.4.3.11 DSP_PCIE_AER Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_AER_EXT_CAP_HDR_OFF	0x0000	W	0x14820001	Advanced Error Reporting Extended Capability Header

Name	Offset	Size	Reset Value	Description
DSP_PCIE_AER_UNCORR_ERR_STATUS_OFF	0x0004	W	0x00000000	Uncorrectable Error Status Register
DSP_PCIE_AER_UNCORR_ERR_MASK_OFF	0x0008	W	0x00400000	Uncorrectable Error Mask Register
DSP_PCIE_AER_UNCORR_ERR_SEV_OFF	0x000C	W	0x00462030	Uncorrectable Error Severity Register
DSP_PCIE_AER_CORR_ERR_STATUS_OFF	0x0010	W	0x00000000	Correctable Error Status Register
DSP_PCIE_AER_CORR_ERR_MASK_OFF	0x0014	W	0x0000E000	Correctable Error Mask Register
DSP_PCIE_AER_ADV_ERR_CAP_CTRL_OFF	0x0018	W	0x000000A0	Advanced Error Capabilities and Control Register
DSP_PCIE_AER_HDR_LOG_0_OFF	0x001C	W	0x00000000	Header Log Register 0
DSP_PCIE_AER_HDR_LOG_1_OFF	0x0020	W	0x00000000	Header Log Register 1
DSP_PCIE_AER_HDR_LOG_2_OFF	0x0024	W	0x00000000	Header Log Register 2
DSP_PCIE_AER_HDR_LOG_3_OFF	0x0028	W	0x00000000	Header Log Register 3
DSP_PCIE_AER_ROOT_ERR_CMD_OFF	0x002C	W	0x00000000	Root Error Command Register. Exits only in RC mode
DSP_PCIE_AER_ROOT_ERR_STATUS_OFF	0x0030	W	0x48000000	Root Error Status Register. Exists only in RC mode
DSP_PCIE_AER_ERR_SRC_ID_OFF	0x0034	W	0x00000000	Error Source Identification Register.Exists only in RC mode
DSP_PCIE_AER_TLP_PREFIX_LOG_1_OFF	0x0038	W	0x00000000	TLP Prefix Log Register 1
DSP_PCIE_AER_TLP_PREFIX_LOG_2_OFF	0x003C	W	0x00000000	TLP Prefix Log Register 2
DSP_PCIE_AER_TLP_PREFIX_LOG_3_OFF	0x0040	W	0x00000000	TLP Prefix Log Register 3
DSP_PCIE_AER_TLP_PREFIX_LOG_4_OFF	0x0044	W	0x00000000	TLP Prefix Log Register 4

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.12 DSP_PCIE_AER Detail Registers Description

DSP_PCIE_AER_EXT_CAP_HDR_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x148	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x148 Testable: unconstrained
19:16	RW	0x2	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the End-End TLP Prefix Supported bit is set and must be 1h or 2h otherwise. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x2 Testable: unconstrained
15:0	RW	0x0001	CAP_ID AER Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

DSP_PCIE_AER_UNCORR_ERR_STATUS_OFF

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	W1C	0x0	TLP_PRFX_BLOCKED_ERR_STATUS TLP Prefix Blocked Error Status. Status bit for TLP Prefix Blocked Error. Note: Not supported. Note: This register field is sticky. Value After Reset: 0x0
22	W1C	0x0	INTERNAL_ERR_STATUS Unsupported Request Error Status. This field represents status of Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
21	RO	0x0	reserved
20	W1C	0x0	UNSUPPORTED_REQ_ERR_STATUS Unsupported Request Error Status. This field represents status of Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
19	W1C	0x0	ECRC_ERR_STATUS ECRC Error Status. This field represents status of ECRC Error. Note:If CX_ECRC_ENABLE=0 the register field always reads 0. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
18	W1C	0x0	MALF_TLP_ERR_STATUS Malformed TLP Status. This field represents status of Malformed TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
17	W1C	0x0	REC_OVERFLOW_ERR_STATUS Receiver Overflow Status. Status bit for Receiver Overflow. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
16	W1C	0x0	UNEXP_CMPLT_ERR_STATUS Unexpected Completion Status. Status bit for Unexpected Completion. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15	W1C	0x0	CMPLT_ABORT_ERR_STATUS Completer Abort Status. Status bit for Completer Abort. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
14	W1C	0x0	CMPLT_TIMEOUT_ERR_STATUS Completion Timeout Status. Status for Completion Timeout. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
13	W1C	0x0	FC_PROTOCOL_ERR_STATUS Flow Control Protocol Error Status. Status bit for Flow Control Protocol Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
12	W1C	0x0	POIS_TLP_ERR_STATUS Poisoned TLP Status. Status bit for Poisoned TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:6	RO	0x00	reserved
5	W1C	0x0	SURPRISE_DOWN_ERR_STATUS Surprise Down Error Status (Optional). Status bit for Surprise Down Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
4	W1C	0x0	DL_PROTOCOL_ERR_STATUS Data Link Protocol Error Status. Status bit for Data Link Protocol Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
3:0	RO	0x0	reserved

DSP_PCIE_AER_UNCORR_ERR_MASK_OFF
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	TLP_PRFX_BLOCKED_ERR_MASK TLP Prefix Blocked Error Mask. Mask bit for TLP Prefix Blocked Error. Note: Not supported. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
24	RO	0x0	ATOMIC_EGRESS_BLOCKED_ERR_MASK AtomicOp Egress Block Mask (Optional). Mask bit for AtomicOp Egress Block Error. Note: This register field is sticky. Value After Reset: 0x0
23	RO	0x0	reserved
22	RW	0x1	INTERNAL_ERR_MASK Uncorrectable Internal Error Mask (Optional). Mask bit for Uncorrectable Internal Error. Note: This register field is sticky. Value After Reset: 0x1
21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	UNSUPPORTED_REQ_ERR_MASK Unsupported Request Error Mask. Mask bit for Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0
19	RW	0x0	ECRC_ERR_MASK ECRC Error Mask (Optional). Mask bit for ECRC Error. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
18	RW	0x0	MALF_TLP_ERR_MASK Malformed TLP Mask. Mask bit for Malformed TLP. Note: This register field is sticky. Value After Reset: 0x0
17	RW	0x0	REC_OVERFLOW_ERR_MASK Receiver Overflow Mask (Optional). This field represents Receiver Overflow Mask. Note: This register field is sticky. Value After Reset: 0x0
16	RW	0x0	UNEXP_CMPLT_ERR_MASK Unexpected Completion Mask. Mask bit for Unexpected Completion Error. Note: This register field is sticky. Value After Reset: 0x0
15	RW	0x0	CMPLT_ABORT_ERR_MASK Completer Abort Error Mask (Optional). Mask bit for Completer Abort Error. Note: This register field is sticky. Value After Reset: 0x0
14	RW	0x0	CMPLT_TIMEOUT_ERR_MASK Completion Timeout Error Mask. Mask bit for Completion Timeout Error. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
13	RW	0x0	FC_PROTOCOL_ERR_MASK Flow Control Protocol Error Mask. Mask bit for Flow Control Protocol Error. Note: This register field is sticky. Value After Reset: 0x0
12	RW	0x0	POIS_TLP_ERR_MASK Poisoned TLP Error Mask. Mask bit for Poisoned TLP Error. Note: This register field is sticky. Value After Reset: 0x0
11:6	RO	0x00	reserved
5	RO	0x0	SURPRISE_DOWN_ERR_MASK Surprise Down Error Mask. Mask bit for Surprise Down Error. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
4	RW	0x0	DL_PROTOCOL_ERR_MASK Data Link Protocol Error Mask. This field informs whether Data Link Protocol Error is masked or not. Note: This register field is sticky. Value After Reset: 0x0
3:0	RO	0x0	reserved

DSP_PCIE_AER_UNCORR_ERR_SEV_OFF
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

Bit	Attr	Reset Value	Description
25	RW	0x0	TLP_PRFX_BLOCKED_ERR_SEVERITY TLP Prefix Blocked Error Severity (Optional). Severity bit for TLP Prefix Blocked Error. Note: Not supported. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
24	RW	0x0	ATOMIC_EGRESS_BLOCKED_ERR_SEVERITY AtomicOp Egress Blocked Severity (Optional). For a description of this standard PCIe register field, see the PCI Express Specification.
23	RO	0x0	reserved
22	RW	0x1	INTERNAL_ERR_SEVERITY Uncorrectable Internal Error Severity (Optional). Severity bit for Uncorrectable Internal Error. Note: This register field is sticky. Value After Reset: 0x1
21	RO	0x0	reserved
20	RW	0x0	UNSUPPORTED_REQ_ERR_SEVERITY Unsupported Request Error Severity. Severity bit for Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0
19	RW	0x0	ECRC_ERR_SEVERITY ECRC Error Severity (Optional). Severity bit for ECRC Error. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
18	RW	0x1	MALF_TLP_ERR_SEVERITY Malformed TLP Severity. Severity bit for Malformed TLP. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
17	RW	0x1	REC_OVERFLOW_ERR_SEVERITY Receiver Overflow Error Severity (Optional). Severity bit for Receiver Overflow Error. Note: This register field is sticky. Value After Reset: 0x1
16	RW	0x0	UNEXP_CMPLT_ERR_SEVERITY Unexpected Completion Error Severity. Severity bit for Unexpected Completion Error. Note: This register field is sticky. Value After Reset: 0x0
15	RW	0x0	CMPLT_ABORT_ERR_SEVERITY Completer Abort Error Severity (Optional). Severity bit for Completer Abort Error. Note: This register field is sticky. Value After Reset: 0x0
14	RW	0x0	CMPLT_TIMEOUT_ERR_SEVERITY Completion Timeout Error Severity. Severity bit for Completion Timeout Error. Note: This register field is sticky. Value After Reset: 0x0
13	RW	0x1	FC_PROTOCOL_ERR_SEVERITY Flow Control Protocol Error Severity (Optional). Severity bit for Flow Control Protocol Error. Note: This register field is sticky. Value After Reset: 0x1
12	RW	0x0	POIS_TLP_ERR_SEVERITY Poisoned TLP Severity. Severity bit for Poisoned TLP. Note: This register field is sticky. Value After Reset: 0x0
11:6	RO	0x00	reserved

Bit	Attr	Reset Value	Description
5	RW	0x1	SURPRISE_DOWN_ERR_SVRITY Surprise Down Error Severity (Optional). Severity bit for Surprise Down Error. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	DL_PROTOCOL_ERR_SEVERITY Data Link Protocol Error Severity. Severity bit for Data Link Protocol Error. Note: This register field is sticky. Value After Reset: 0x1
3:0	RO	0x0	reserved

DSP_PCIE_AER_CORR_ERR_STATUS_OFF

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	HEADER_LOG_OVERFLOW_STATUS Header Log Overflow Error Status (Optional). This field provides status of Header Log Overflow Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14	W1C	0x0	CORRECTED_INT_ERR_STATUS Corrected Internal Error Status (Optional). This field provides status of Corrected Internal Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
13	W1C	0x0	ADVISORY_NON_FATAL_ERR_STATUS Advisory Non-Fatal Error Status. Status bit for Advisory Non-Fatal Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
12	W1C	0x0	RPL_TIMER_TIMEOUT_STATUS Replay Timer Timeout Status. Status bit for Replay Timer Timeout. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:9	RO	0x0	reserved
8	W1C	0x0	REPLAY_NO_ROLEOVER_STATUS REPLAY_NUM Rollover Status. Status bit for REPLAY_NUM Rollover. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	W1C	0x0	BAD_DLLP_STATUS Bad DLLP Status. Status bit for Bad DLLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
6	W1C	0x0	BAD_TLP_STATUS Bad TLP Status. Status bit for Bad TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:1	RO	0x00	reserved
0	W1C	0x0	RX_ERR_STATUS Receiver Error Status (Optional). This field provides status of Receiver Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_CORR_ERR_MASK_OFF

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x1	HEADER_LOG_OVERFLOW_MASK Header Log Overflow Error Mask (Optional). Masking bit for Header Log Overflow Error. Note: This register field is sticky. Value After Reset: 0x1
14	RW	0x1	CORRECTED_INT_ERR_MASK Corrected Internal Error Mask (Optional). Masking bit for Corrected Internal Error Mask. Note: This register field is sticky. Value After Reset: 0x1
13	RW	0x1	ADVISORY_NON_FATAL_ERR_MASK Advisory Non-Fatal Error Mask. Masking bit for Advisory Non-Fatal Error. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
12	RW	0x0	RPL_TIMER_TIMEOUT_MASK Replay Timer Timeout Mask. Masking bit for Replay Timer Timeout. Note: This register field is sticky. Value After Reset: 0x0
11:9	RO	0x0	reserved
8	RW	0x0	REPLAY_NO_ROLEOVER_MASK REPLAY_NUM Rollover Mask. Masking bit for REPLAY_NUM Rollover. Note: This register field is sticky. Value After Reset: 0x0
7	RW	0x0	BAD_DLLP_MASK ad DLLP Mask. Masking bit for Bad DLLP. Note: This register field is sticky. Value After Reset: 0x0
6	RW	0x0	BAD_TLP_MASK Bad TLP Mask. Masking bit for Bad TLP. Note: This register field is sticky. Value After Reset: 0x0
5:1	RO	0x00	reserved
0	RW	0x0	RX_ERR_MASK Receiver Error Mask (Optional). Masking bit for Receiver Error. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_AER_ADV_ERR_CAP_CTRL_OFF

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	CTO_PRFX_HDR_LOG_CAP TLP Prefix Log Present. If Set, this bit indicates that the Function records the prefix/header of Request TLPs that experience a Completion Timeout error. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11	RW	0x0	TLP_PRFX_LOG_PRESENT Completion Timeout Prefix/Header Log Capable. If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is Clear. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
10	RO	0x0	MULTIPLE_HEADER_EN Multiple Header Recording Enable. When Set, this bit enables the Function to record more than one error header. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Value After Reset: 0x0
9	RO	0x0	MULTIPLE_HEADER_CAP Multiple Header Recording Capable. If Set, this bit indicates that the Function is capable of recording more than one error header. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	ECRC_CHECK_EN ECRC Check Enable. When Set, ECRC checking is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky. Value After Reset: 0x0
7	RO	0x1	ECRC_CHECK_CAP ECRC Check Capable. If Set, this bit indicates that the Function is capable of checking ECRC. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
6	RW	0x0	ECRC_GEN_EN ECRC Generation Enable. When Set, ECRC generation is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky. Value After Reset: 0x0
5	RO	0x1	ECRC_GEN_CAP ECRC Generation Capable. If Set, this bit indicates that the Function is capable of generating ECRC. Note: This register field is sticky. Value After Reset: 0x1
4:0	RO	0x00	FIRST_ERR_POINTER First Error Pointer. The First Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_HDR_LOG_0_OFF
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	FIRST_DWORD_FOURTH_BYTE Byte 3 of Header log register of First 32-bit Data Word. This field represents fourth byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	FIRST_DWORD_THIRD_BYTE Byte 2 of Header log register of First 32-bit Data Word. This field represents third byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	FIRST_DWORD_SECOND_BYTE Byte 1 of Header log register of First 32-bit Data Word. This field represents second byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:0	RO	0x00	FIRST_DWORD_FIRST_BYTE Byte 0 of Header log register of First 32-bit Data Word. This field represents first byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_HDR_LOG_1_OFF
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	SECOND_DWORD_FOURTH_BYTE Byte 3 of Header log register of Second 32-bit Data Word. This field represents fourth byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	SECOND_DWORD_THIRD_BYTE Byte 2 of Header log register of Second 32-bit Data Word. This field represents third byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	SECOND_DWORD_SECOND_BYTE Byte 1 of Header log register of Second 32-bit Data Word. This field represents second byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: tru
7:0	RO	0x00	SECOND_DWORD_FIRST_BYTE Byte 0 of Header log register of Second 32-bit Data Word. This field represents first byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_HDR_LOG_2_OFF
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	THIRD_DWORD_FOURTH_BYTE Byte 3 of Header log register of Third 32-bit Data Word. This field represents fourth byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	THIRD_DWORD_THIRD_BYTE Byte 2 of Header log register of Third 32-bit Data Word. This field represents third byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	THIRD_DWORD_SECOND_BYTE Byte 1 of Header log register of Third 32-bit Data Word. This field represents second byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:0	RO	0x00	THIRD_DWORD_FIRST_BYTE Byte 0 of Header log register of Third 32-bit Data Word. This field represents first byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_HDR_LOG_3_OFF

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	FOURTH_DWORD_FOURTH_BYTE Byte 3 of Header log register of Fourth 32-bit Data Word. This field represents fourth byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	FOURTH_DWORD_THIRD_BYTE Byte 2 of Header log register of Fourth 32-bit Data Word. This field represents third byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	FOURTH_DWORD_SECOND_BYTE Byte 1 of Header log register of Fourth 32-bit Data Word. This field represents second byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:0	RO	0x00	FOURTH_DWORD_FIRST_BYTE Byte 0 of Header log register of Fourth 32-bit Data Word. This field represents first byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_ROOT_ERR_CMD_OFF
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	FATAL_ERR_REPORTING_EN Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
1	RW	0x0	NON_FATAL_ERR_REPORTING_EN Non-Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs. Value After Reset: 0x0
0	RW	0x0	CORR_ERR_REPORTING_EN Correctable Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a correctable error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs (Root Complex integrated Endpoint). Value After Reset: 0x0

DSP_PCIE_AER_ROOT_ERR_STATUS_OFF

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x09	ADV_ERR_INT_MSG_NUM Advanced Error Interrupt Message Number. This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability. For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x9 Testable: unconstrained
26:7	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
6	W1C	0x0	FATAL_ERR_MSG_RX One or more Fatal Error Messages Received. Set when one or more Fatal Uncorrectable error Messages have been received. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5	W1C	0x0	NON_FATAL_ERR_MSG_RX One or more Non-Fatal Error Messages Received. Set when one or more Non-Fatal Uncorrectable error Messages have been received. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	W1C	0x0	FIRST_UNCORR_FATAL First Uncorrectable Error is Fatal. Set when the first Uncorrectable error Message received is for a Fatal error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	W1C	0x0	MUL_ERR_FATAL_NON_FATAL_RX Multiple Fatal or Non-Fatal Errors Received. Set when either a Fatal or a Non-fatal error is received and ERR_FATAL_NON_FATAL_RX is already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
2	W1C	0x0	ERR_FATAL_NON_FATAL_RX Fatal or Non-Fatal Error Received. Set when either a Fatal or a Non-fatal error Message is received and this bit is not already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	W1C	0x0	MUL_ERR_COR_RX Multiple Correctable Errors Received. Set when a Correctable error Message is received and ERR_COR_RX is already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	W1C	0x0	ERR_COR_RX Correctable Error Received. Set when a Correctable error Message is received and this bit is not already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_ERR_SRC_ID_OFF
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ERR_FATAL_NON_FATAL_SOURCE_ID Source of Fatal/Non-Fatal Error. Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received bit is not already set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ERR_COR_SOURCE_ID Source of Correctable Error. Loaded with the Requester ID indicated in the received ERR_COR Message when the ERR_COR Received bit is not already set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_AER_TLP_PREFIX_LOG_1_OFF
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_1_FOURTH_BYTE Byte 3 of Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_1_THIRD_BYTE Byte 2 Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.
15:8	RO	0x00	CFG_TLP_PFX_LOG_1_SECOND_BYTE Byte 1 Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_1_FIRST_BYTE Byte 0 Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.

DSP_PCIE_AER_TLP_PREFIX_LOG_2_OFF
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_2_FOURTH_BYTE Byte 3 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_2_THIRD_BYTE Byte 2 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.
15:8	RO	0x00	CFG_TLP_PFX_LOG_2_SECOND_BYTE Byte 1 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_2_FIRST_BYTE Byte 0 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.

DSP_PCIE_AER_TLP_PREFIX_LOG_3_OFF
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	CFG_TLP_PFX_LOG_3_FOURTH_BYTE Byte 3 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_3_THIRD_BYTE Byte 2 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.

Bit	Attr	Reset Value	Description
15:8	RO	0x00	CFG_TLP_PFX_LOG_3_SECOND_BYTE Byte 1 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_3_FIRST_BYTE Byte 0 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.

DSP_PCIE_AER_TLP_PREFIX_LOG_4_OFF
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_4_FOURTH_BYTE Byte 3 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_4_THIRD_BYTE Byte 2 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.
15:8	RO	0x00	CFG_TLP_PFX_LOG_4_SECOND_BYTE Byte 1 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_4_FIRST_BYTE Byte 0 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.

11.4.3.13 DSP_PCIE_SPCIE Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_SPCIE_CAP_HEADER_REG	0x0000	W	0x19010019	SPCIE Capability Header
DSP_PCIE_SPCIE_LINK_CONTROL3_REG	0x0004	W	0x00000000	Link Control 3 Register
DSP_PCIE_SPCIE_LANE_ERR_STATUS_REG	0x0008	W	0x00000000	Lane Error Status Register
DSP_PCIE_SPCIE_CAP_OFF_0CH_REG	0x000C	W	0x0F7F7F7F	Lane Equalization Control Register for lanes 1 and 0
DSP_PCIE_SPCIE_CAP_OFF_10H_REG	0x0010	W	0x7F7F7F7F	Lane Equalization Control Register for lanes 3 and 2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.14 DSP_PCIE_SPCIE Detail Registers Description

DSP_PCIE_SPCIE_CAP_HEADER_REG
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x190	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value. Value After Reset: 0x190 Testable: unconstrained
19:16	RW	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:0	RW	0x0019	EXTENDED_CAP_ID Secondary PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0x19 Testable: unconstrained

DSP_PCIE_SPCIE_LINK_CONTROL3_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	EQ_REQ_INT_EN Link Equalization Request Interrupt Enable. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (CLEAR): Clear 0x1 (SET): When Set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request 8.0 GT/s bit, the Link Equalization Request 16.0 GT/s bit, or the Link Equalization Request 32.0 GT/s bit has been set. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RO	0x0	PERFORM_EQ Perform Equalization. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is 1b and a 1b is written to the Retrain Link bit with the Target Link Speed field set to 8.0 GT/s or higher, the Downstream Port must perform Link Equalization. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

DSP_PCIE_SPCIE_LANE_ERR_STATUS_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	W1C	0x0	LANE_ERR_STATUS Lane Error Status Bits per Lane. Each bit indicates if the corresponding Lane detected a Lane-based error. A value of 1b indicates that a Lane based-error was detected on the corresponding Lane Number. For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ. For Ports that do not support 8.0 GT/s and do not set these bits based on 8b/10b errors , this field is permitted to be hardwired to 0 by the controller. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_SPCIE_CAP_OFF_0CH_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:28	RW	0x0	USP_RX_PRESET_HINT1 Upstream Port 8.0 GT/s Receiver Preset Hint 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
27:24	RW	0xf	USP_TX_PRESET1 Upstream Port 8.0 GT/s Transmitter Preset 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstrained
23	RO	0x0	reserved
22:20	RW	0x7	DSP_RX_PRESET_HINT1 Downstream Port 8.0 GT/s Receiver Preset Hint 1. Receiver preset hint 1 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:16	RW	0xf	DSP_TX_PRESET1 Downstream Port 8.0 GT/s Transmitter Preset 1. Transmitter preset 1 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstraine
15	RO	0x0	reserved
14:12	RW	0x7	USP_RX_PRESET_HINT0 Upstream Port 8.0 GT/s Receiver Preset Hint 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
11:8	RW	0xf	USP_TX_PRESET0 Upstream Port 8.0 GT/s Transmitter Preset 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstrained
7	RO	0x0	reserved
6:4	RW	0x7	DSP_RX_PRESET_HINT0 Downstream Port 8.0 GT/s Receiver Preset Hint 0. Receiver preset hint 0 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
3:0	RW	0xf	DSP_TX_PRESET0 Downstream Port 8.0 GT/s Transmitter Preset 0. Transmitter preset 0 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstrained

DSP_PCIE_SPCIE_CAP_OFF_10H_REG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x7	USP_RX_PRESET_HINT1 Upstream Port 8.0 GT/s Receiver Preset Hint 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
27:24	RW	0xf	USP_TX_PRESET1 Upstream Port 8.0 GT/s Transmitter Preset 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstrained
23	RO	0x0	reserved
22:20	RW	0x7	DSP_RX_PRESET_HINT1 Downstream Port 8.0 GT/s Receiver Preset Hint 1. Receiver preset hint 1 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:16	RW	0xf	DSP_TX_PRESET1 Downstream Port 8.0 GT/s Transmitter Preset 1. Transmitter preset 1 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstraine
15	RO	0x0	reserved
14:12	RW	0x7	USP_RX_PRESET_HINT0 Upstream Port 8.0 GT/s Receiver Preset Hint 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
11:8	RW	0xf	USP_TX_PRESET0 Upstream Port 8.0 GT/s Transmitter Preset 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstrained
7	RO	0x0	reserved
6:4	RW	0x7	DSP_RX_PRESET_HINT0 Downstream Port 8.0 GT/s Receiver Preset Hint 0. Receiver preset hint 0 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
3:0	RW	0xf	DSP_TX_PRESET0 Downstream Port 8.0 GT/s Transmitter Preset 0. Transmitter preset 0 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Value After Reset: 0xf Testable: unconstrained

11.4.3.15 DSP_PCIE_L1SUB Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_L1SUB_CAP_HEADER_REG	0x0000	W	0x1D01001E	L1 Substates Extended Capability Header
DSP_PCIE_L1SUB_CAPABILITY_REG	0x0004	W	0x00280A1F	L1 Substates Capability Register
DSP_PCIE_L1SUB_CONTROL1_REG	0x0008	W	0x00000A00	L1 Substates Control 1 Register
DSP_PCIE_L1SUB_CONTROL2_REG	0x000C	W	0x00000028	L1 Substates Control 2 Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.16 DSP_PCIE_L1SUB Detail Registers Description

DSP_PCIE_L1SUB_CAP_HEADER_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x1d0	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h, if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1d0 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:16	RW	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is depends on version of the specification. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
15:0	RW	0x001e	EXTENDED_CAP_ID L1SUB Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 PM Substates is 001Eh. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1e Testable: unconstrained

DSP_PCIE_L1SUB_CAPABILITY_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:19	RW	0x05	PWR_ON_VALUE_SUPPORT Port T Power On Value. Along with the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Value After Reset: 0x5 Testable: writeAsRead

Bit	Attr	Reset Value	Description
18	RO	0x0	reserved
17:16	RW	0x0	PWR_ON_SCALE_SUPPORT Port T Power On Scale. Specifies the scale used for the Port T_POWER_ON_VALUE field in the L1 PM Substates Capabilities register. Range of values are given below. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Values: 0x0 (_2us): Scale is 2us 0x1 (_10us): Scale is 10us 0x2 (_100us): Scale is 100us 0x3 (Reserved): Reserved Value After Reset: 0x0 Testable: writeAsRead
15:8	RW	0x0a	COMM_MODE_SUPPORT Port Common Mode Restore Time. Time (in us) required for this Port to re-establish common mode. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Value After Reset: 0xa Testable: writeAsRead
7:5	RO	0x0	reserved
4	RW	0x1	L1_PMSUB_SUPPORT L1 PM Substates ECN Supported. When Set this field indicates that this Port supports L1 PM Substates. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Value After Reset: 0x1

Bit	Attr	Reset Value	Description
3	RW	0x1	L1_1_ASPM_SUPPORT ASPM L11 Supported. When Set this field indicates that ASPM L1.1 is supported. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Value After Reset: 0x1
2	RW	0x1	L1_2_ASPM_SUPPORT ASPM L12 Supported. When Set this field indicates that ASPM L1.2 is supported. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Value After Reset: 0x1
1	RW	0x1	L1_1_PCIPM_SUPPORT PCI-PM L11 Supported. When Set this field indicates that PCI-PM L1.1 is supported, and must be Set by all Ports implementing L1 PM Substates. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Value After Reset: 0x1
0	RW	0x1	L1_2_PCIPM_SUPPORT PCI-PM L12 Supported. When Set this field indicates that PCI-PM L1.2 is supported. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Value After Reset: 0x1

DSP_PCIE_L1SUB_CONTROL1_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	L1_2_TH_SCA LTR L12 Threshold Scale. This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. Hardware operation is undefined if software writes a Not-Permitted value to this field. Required for all Ports Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP Value After Reset: 0x0 Testable: writeAsRead
28:26	RO	0x0	reserved
25:16	RW	0x000	L1_2_TH_VAL LTR L12 Threshold Value. Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled). Required for all Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP Value After Reset: 0x0 Testable: writeAsRead
15:8	RW	0x0a	T_COMMON_MODE Common Mode Restore Time. Sets value of TCOMMONMODE (in us), which must be used by the Downstream Ports for timing the re-establishment of common mode. This field is of type RsvdP for Upstream Ports. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RW : RSVDP Value After Reset: 0xa Testable: writeAsRead
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	L1_1_ASPM_EN ASPM L11 Enable. When Set this field, enables ASPM L1.1. For Ports for which the ASPM L1.1 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0
2	RW	0x0	L1_2_ASPM_EN ASPM L12 Enable. When Set this field, enables ASPM L1.2. For Ports for which the ASPM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0
1	RW	0x0	L1_1_PCIPM_EN PCI-PM L11 Enable. When Set this field, enables PCI-PM L1.1. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0
0	RW	0x0	L1_2_PCIPM_EN PCI-PM L12 Enable. When Set this field, enables PCI-PM L1.2. For Ports for which the PCI-PM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0

DSP_PCIE_L1SUB_CONTROL2_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:3	RW	0x05	T_POWER_ON_VALUE T Power On Value. Along with the T_POWER_ON_SCALE sets the minimum amount of time (in us) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON_SCALE field. Required for all Ports that support L1.2, otherwise this field is of type RsvdP.This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Value After Reset: 0x5 Testable: writeAsRead
2	RO	0x0	reserved
1:0	RW	0x0	T_POWER_ON_SCALE T Power On Scale. Specifies the scale used for T_POWER_ON_VALUE. Range of values are given below. Required for all Ports that support L1.2, otherwise this field is of type RsvdP. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Values: 0x0 (_2us): Scale is 2us 0x1 (_10us): Scale is 10us 0x2 (_100us): Scale is 100us 0x3 (Reserved): Reserved Value After Reset: 0x0 Testable: writeAsRead

11.4.3.17 DSP_PCIE_RAS_DES Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_RAS_DES_CAP_HEADER_REG	0x0000	W	0x2A01000B	Vendor-Specific Extended Capability Header

Name	Offset	Size	Reset Value	Description
DSP_PCIE_RAS_DES_VENDOR_SPECIFIC_HEADER_REG	0x0004	W	0x10040002	Vendor-Specific Header
DSP_PCIE_RAS_DES_EVENT_COUNTER_CONTROL_REG	0x0008	W	0x00000000	Event Counter Contro
DSP_PCIE_RAS_DES_EVENT_COUNTER_DATA_REG	0x000C	W	0x00000000	Event Counter Data
DSP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_CONTROL_REG	0x0010	W	0x00000000	Time-based Analysis Control
DSP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_REG	0x0014	W	0x00000000	Time-based Analysis Data
DSP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_63_32_REG	0x0018	W	0x00000000	Upper 32 bits of Time-based Analysis Data
DSP_PCIE_RAS_DES_EINJ_ENABLE_REG	0x0030	W	0x00000000	Error Injection Enable
DSP_PCIE_RAS_DES_EINJ0_CRC_REG	0x0034	W	0x00000000	Error Injection Control 0 (CRC Error)
DSP_PCIE_RAS_DES_EINJ1_SEQNUM_REG	0x0038	W	0x00000000	Error Injection Control 1 (Sequence Number Error)
DSP_PCIE_RAS_DES_EINJ2_DLLP_REG	0x003C	W	0x00000000	Error Injection Control 2 (DLLP Error)
DSP_PCIE_RAS_DES_EINJ3_SYMBOL_REG	0x0040	W	0x00000000	Error Injection Control 3 (Symbol Error)
DSP_PCIE_RAS_DES_EINJ4_FC_REG	0x0044	W	0x00000000	Error Injection Control 4 (FC Credit Error)
DSP_PCIE_RAS_DES_EINJ5_SP_TLP_REG	0x0048	W	0x00000000	Error Injection Control 5 (Specific TLP Error)
DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H0_REG	0x004C	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #0)
DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H1_REG	0x0050	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #1)
DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H2_REG	0x0054	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #2)
DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H3_REG	0x0058	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #3)
DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H0_REG	0x005C	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #0)
DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H1_REG	0x0060	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #1)
DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H2_REG	0x0064	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #2)

Name	Offset	Size	Reset Value	Description
DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H3_REG	0x0068	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #3)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H0_REG	0x006C	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #0)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H1_REG	0x0070	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #1)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H2_REG	0x0074	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #2)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H3_REG	0x0078	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #3)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H0_REG	0x007C	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #0)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H1_REG	0x0080	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #1)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H2_REG	0x0084	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #2)
DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H3_REG	0x0088	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #3)
DSP_PCIE_RAS_DES_EINJ6_TLP_REG	0x008C	W	0x00000000	Error Injection Control 6 (Packet Error)
DSP_PCIE_RAS_DES_SD_CONTROL1_REG	0x00A0	W	0x00000000	Silicon Debug Control 1
DSP_PCIE_RAS_DES_SD_CONTROL2_REG	0x00A4	W	0x00000000	Silicon Debug Control 2
DSP_PCIE_RAS_DES_SD_STATUS_L1LANE_REG	0x00B0	W	0x00180000	Silicon Debug Status(Layer1 Per-lane)
DSP_PCIE_RAS_DES_SD_STATUS_L1LTSSM_REG	0x00B4	W	0x00000200	Silicon Debug Status(Layer1 LTSSM)
DSP_PCIE_RAS_DES_SD_STATUS_PM_REG	0x00B8	W	0x00000000	Silicon Debug Status(PM)
DSP_PCIE_RAS_DES_SD_STATUS_L2_REG	0x00BC	W	0x00FFF000	Silicon Debug Status(Layer2)
DSP_PCIE_RAS_DES_SD_STATUS_L3FC_REG	0x00C0	W	0x00000000	Silicon Debug Status(Layer3 FC)
DSP_PCIE_RAS_DES_SD_STATUS_L3_REG	0x00C4	W	0x00000000	Silicon Debug Status(Layer3)
DSP_PCIE_RAS_DES_SD_EQ_CONTROL1_REG	0x00D0	W	0x00000000	Silicon Debug EQ Control 1
DSP_PCIE_RAS_DES_SD_EQ_CONTROL2_REG	0x00D4	W	0x00000000	Silicon Debug EQ Control 2
DSP_PCIE_RAS_DES_SD_EQ_CONTROL3_REG	0x00D8	W	0x00000000	Silicon Debug EQ Control 3
DSP_PCIE_RAS_DES_SD_EQ_STATUS1_REG	0x00E0	W	0x00000000	Silicon Debug EQ Status 1

Name	Offset	Size	Reset Value	Description
DSP_PCIE_RAS_DES_SD_EQ_STATUS2_REG	0x00E4	W	0x00000000	Silicon Debug EQ Status 2
DSP_PCIE_RAS_DES_SD_EQ_STATUS3_REG	0x00E8	W	0x00000000	Silicon Debug EQ Status 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.18 DSP_PCIE_RAS_DES Detail Registers Description

DSP_PCIE_RAS_DES_CAP_HEADER_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x2a0	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value Value After Reset: 0x2d0 Testable: writeAsRead
19:16	RW	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Value of this field is depends on the version of the specification. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15:0	RW	0x000b	EXTENDED_CAP_ID PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Vendor-Specific Extended Capability is 000Bh. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0xb Testable: writeAsRead

DSP_PCIE_RAS_DES_VENDOR_SPECIFIC_HEADER_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:20	RO	0x100	VSEC_LENGTH VSEC Length. This field indicates the number of bytes in the entire VSEC structure, including the Vendor-Specific Extended Capability Header, the Vendor-Specific Header, and the vendor-specific registers. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value Value After Reset: 0x100
19:16	RO	0x4	VSEC_REV VSEC Rev. This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x4
15:0	RO	0x0002	VSEC_ID VSEC ID. This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0x2

DSP_PCIE_RAS_DES_EVENT_COUNTER_CONTROL_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	EVENT_COUNTER_EVENT_SELECT Event Counter Data Select. This field in conjunction with the EVENT_COUNTER_LANE_SELECT field indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. 27-24: Group number(4-bit: 0..0x7) 23-16: Event number(8-bit: 0..0x13) within the Group .. For detailed definitions of Group number and Event number, see the RAS DES chapter in the Databook. Note: This register field is sticky. Values: 0x0 (EBUF_OVERFLOW): Ebuf Overflow 0x1 (EBUF_UNDERRUN): Ebuf Underrun 0x700 (TX_MEM_WRITE): Tx Memory Write 0x713 (RX_MSG_TLP): Rx Message TLP Value After Reset: 0x0 Testable: writeAsRead
15:12	RO	0x0	reserved
11:8	RW	0x0	EVENT_COUNTER_LANE_SELECT Event Counter Lane Select. This field in conjunction with EVENT_COUNTER_EVENT_SELECT indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
7	RO	0x0	EVENT_COUNTER_STATUS Event Counter Status. This register returns the current value of the Event Counter selected by the following fields: EVENT_COUNTER_EVENT_SELECT EVENT_COUNTER_LANE_SELECT Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6:5	RO	0x0	reserved
4:2	WO	0x0	EVENT_COUNTER_ENABLE Event Counter Enable. Enables/disables the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. By default, all event counters are disabled. You can enable/disable a specific Event Counter by writing the 'per event off' or 'per event on' codes. You can enable/disable all event counters by writing the 'all on' or 'all off' codes. The read value is always '0'. For other values no change. Values: 0x1 (PER_EVENT_OFF): per event off 0x3 (PER_EVENT_ON): per event on 0x5 (ALL_OFF): all off 0x7 (ALL_ON): all on Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
1:0	WO	0x0	EVENT_COUNTER_CLEAR Event Counter Clear. Clears the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. You can clear the value of a specific Event Counter by writing the 'per clear' code and you can clear all event counters at once by writing the 'all clear' code. The read value is always '0'. Other values are reserved. Values: 0x0 (NO_CHANGE): no change 0x1 (PER_CLEAR): per clear 0x2 (NO_CHANGE_2): no change 0x3 (ALL_CLEAR): all clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EVENT_COUNTER_DATA_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EVENT_COUNTER_DATA Event Counter Data. This register returns the data selected by the following fields: EVENT_COUNTER_EVENT_SELECT in EVENT_COUNTER_CONTROL_REG Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_CONTROL_REG
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	TIME_BASED_REPORT_SELECT Time-based Report Select. Selects what type of data is measured for the selected duration (TIME_BASED_DURATION_SELECT), and returned in TIME_BASED_ANALYSIS_DATA. Each type of data is measured using one of three types of units: Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x00] * TIME_BASED_ANALYSIS_DATA. Values 0-4 and 7-8 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Aux_clk Cycles. Total time in ps is [Period of platform specific clock] * TIME_BASED_ANALYSIS_DATA. Values 5, 6, and 9 correspond to aux_clk Cycles. Core_clk Cycles for 20GT/s, 25GT/s (CCIX ESM data rate). Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x10] * TIME_BASED_ANALYSIS_DATA. Values 10-14 and 17-18 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Data Bytes. Actual amount of bytes is 16 * TIME_BASED_ANALYSIS_DATA. Values 20-23 correspond to data bytes. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (ONE_CYCLE): Duration of 1 cycle 0x1 (TX_L0S): TxL0s 0x2 (RX_L0S): RxL0s 0x3 (L0): L0 0x4 (L1): L1 0x7 (CFG_RCVRY): Configuration/Recovery 0x8 (TX_RX_L0S): TxL0s and RxL0s 0x5 (L1_1): L1.1 0x6 (L1_2): L1.2 0x9 (L1_AUX): L1 aux 0x10 (_1_CYCLE): Duration of 1 cycle 0x11 (TX_L0S_): TxL0s 0x12 (RX_L0S_): RxL0s 0x13 (L0_): L0 0x14 (L1_): L1 0x17 (CFG_RCVRY_): Configuration/Recovery 0x18 (TX_RX_L0S_): TxL0s and RxL0s 0x20 (TX_PCIE_TLP): Tx PCIe TLP data payload Bytes 0x21 (RX_PCIE_TLP): Rx PCIe TLP data payload Bytes 0x22 (TX_CCIX_TLP): Tx CCIX TLP data payload Bytes 0x23 (RX_CCIX_TLP): Rx CCIX TLP data payload Bytes Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
23:16	RO	0x00	reserved
15:8	RW	0x00	TIME_BASED_DURATION_SELECT Time-based Duration Select. Selects the duration of time-based analysis. When "manual control" is selected and TIMER_START is set to '1', this analysis never stops until TIMER_STOP is set to '0'. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (MANUAL): Manual control 0x1 (_1_MS): 1ms 0x2 (_2_MS): 10ms 0x3 (_100_MS): 100ms 0x4 (_1_S): 1s 0x5 (_2_S): 2s 0x6 (_4_S): 4s 0xff (_4_US): 4us (Debug purpose) Value After Reset: 0x1 Testable: writeAsRead
7:1	RO	0x00	reserved
0	RW	0x0	TIMER_START Timer Start. This bit will be cleared automatically when the measurement is finished. Note: The app_ras_des_tba_ctrl input also sets the contents of this field and controls the measurement start/stop. Note: This register field is sticky. Values: 0x1 (START_RESTART): Start/Restart 0x0 (STOP): Stop Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_REG
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TIME_BASED_ANALYSIS_DATA Time Based Analysis Data. This register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG. The results are cleared when next measurement starts. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: untestable Volatile: true

DSP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_63_32_REG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	TIME_BASED_ANALYSIS_DATA_63_32 Upper 32 bits of Time Based Analysis Data. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ_ENABLE_REG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	ERROR_INJECTION6_ENABLE Error Injection6 Enable (Specific TLP Error). Enables insertion of errors into the packets that you select. You can set this bit to '1' when you have disabled RAS datapath protection (DP) by setting CX_RASDP = CX_RASDP_RAM_PROT =0. You can set this bit to '1' when you have disabled the address translation by setting ADDR_TRANSLATION_SUPPORT_EN=0. For more details, see the EINJ6_COMPARE_*_REG/EINJ6_CHANGE_*_REG/EINJ6_TLP_REG registers. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5	RW	0x0	ERROR_INJECTION5_ENABLE Error Injection5 Enable (TLP Duplicate/Nullify Error). Enables insertion of duplicate/nullified TLPs. For more details, see the EINJ5_SP_TLP_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
4	RW	0x0	ERROR_INJECTION4_ENABLE Error Injection4 Enable (FC Credit Update Error). Enables insertion of errors into UpdateFCs. For more details, see the EINJ4_FC_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	RW	0x0	ERROR_INJECTION3_ENABLE Error Injection3 Enable (Symbol DataK Mask Error or Sync Header Error). Enables DataK masking of special symbols or the breaking of the sync header. For more details, see the EINJ3_SYMBOL_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RW	0x0	ERROR_INJECTION2_ENABLE Error Injection2 Enable (DLLP Error). Enables insertion of DLLP errors. For more details, see the EINJ2_DLLP_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
1	RW	0x0	ERROR_INJECTION1_ENABLE Error Injection1 Enable (Sequence Number Error). Enables insertion of errors into sequence numbers. For more details, see the EINJ1_SEQNUM_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RW	0x0	ERROR_INJECTION0_ENABLE Error Injection0 Enable (CRC Error). Enables insertion of errors into various CRC. For more details, see the EINJ0_CRC_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ0_CRC_REG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	EINJ0_CRC_TYPE Error injection type. Selects the type of CRC error to be inserted. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (TLP_LCRC_ERR): (TX Path) New TLP's LCRC error injection 0x1 (_16b_CRC_ERR_ACK_NAK_DLLP): (TX Path) 16bCRC error injection of ACK/NAK DLLP 0x2 (_16b_CRC_ERR_UPD_FC): (TX Path) 16bCRC error injection of Update-FC DLLP 0x3 (TLP_ECRC_ERR): (TX Path) New TLP's ECRC error injection 0x4 (FCRC_ERR_TLP): (TX Path) TLP's FCRC error injection (128b/130b) 0x5 (PARITY_TSOS_ERR): (TX Path) Parity error of TSOS (128b/130b) 0x6 (PARITY_SKPOS_ERR): (TX Path) Parity error of SKPOS (128b/130b) 0x8 (LCRC_ERR): (RX Path) LCRC error injection 0xb (ECRC_ERR): (RX Path) ECRC error injection Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ0_COUNT Error injection count. Indicates the number of errors. This register is decremented when the errors have been inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION0_ENABLE in EINJ_ENABLE_REG returns 0b. If the counter value is 0x00 and ERROR_INJECTION0_ENABLE=1, the errors are inserted until ERROR_INJECTION0_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ1_SEQNUM_REG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	EINJ1_BAD_SEQNUM Bad sequence number. Indicates the value to add/subtract from the naturally-assigned sequence numbers. This value is represented by two's complement. For example: Set Type, SEQ# and Count EINJ1_SEQNUM_TYPE =0 (Insert errors into new TLPs) EINJ1_BAD_SEQNUM =0x1FFD (represents -3) EINJ1_COUNT =1 Enable Error Injection ERROR_INJECTION1_ENABLE =1 Send a TLP From the Core's Application Interface Assume SEQ#5 is given to the TLP. The SEQ# is Changed to #2 by the Error Injection Function in Layer2. 5 + (-3) = 2 The TLP with SEQ#2 is Transmitted to PCIe Link. Note: This register field is sticky. Values: 0xfff (MAX_VAL): +4095 0x1001 (MIN_VAL): -4095 Value After Reset: 0x0 Testable: writeAsRead
15:9	RO	0x00	reserved
8	RW	0x0	EINJ1_SEQNUM_TYPE Sequence number type. Selects the type of sequence number. Note: This register field is sticky. Values: 0x0 (TLP_ERR): Insertion of New TLP's SEQ# error 0x1 (ACK_NAK_DLLP_ERR): Insertion of ACK/NAK DLLP's SEQ# Error Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EINJ1_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION1_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION1_ENABLE=1, the errors are inserted until ERROR_INJECTION1_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ2_DLLP_REG

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	EINJ2_DLLP_TYPE DLLP Type. Selects the type of DLLP errors to be inserted. Note: This register field is sticky. Values: 0x0 (ACK_NACK_DLLP): ACK/NAK DLLP's transmission block 0x1 (UPD_FC_DLLP): Update FC DLLP's transmission block 0x2 (NAK_DLLP): Always Transmission for NAK DLLP 0x3 (RSVD): Reserved Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ2_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and the error is inserted, ERROR_INJECTION2_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION2_ENABLE =1, the errors are inserted until ERROR_INJECTION2_ENABLE is set to '0'. This register is affected only when EINJ2_DLLP_TYPE =2'10b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ3_SYMBOL_REG

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	EINJ3_SYMBOL_TYPE Error Type. 8b/10b encoding - Mask K symbol. It is not supported to insert errors into the first ordered-set after exiting from TxElecIdle when CX_FREQ_STEP_EN has been enabled. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (RSVD_OR_INVRT_SYNC_HDR): Invert sync header for 128b/130b encoding or this field is reserved for 8b/10b encoding. 0x1 (COM_PAD_TS1): COM/PAD(TS1 Order set) 0x2 (COM_PAD_TS2): COM/PAD(TS2 Order set) 0x3 (COM_FTS): COM/FTS(FTS Order set) 0x4 (COM_IDL): COM/IDL(E-Idle Order set) 0x5 (END_EDB): END/EDB Symbol 0x6 (STP_SDP): STP/SDP Symbol 0x7 (COM_SKP): COM/SKP(SKP Order set) Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ3_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION3_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION3_ENABLE =1, the errors are inserted until ERROR_INJECTION3_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ4_FC_REG

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	EINJ4_BAD_UPDFC_VALUE Bad update-FC credit value. Indicates the value to add/subtract from the UpdateFC credit. This value is represented by two's complement. Note: This register field is sticky. Values: 0xfff (MAX_VAL): +4095 0x1001 (MIN_VAL): -4095 Value After Reset: 0x0 Testable: writeAsRead
15	RO	0x0	reserved
14:12	RW	0x0	EINJ4_VC_NUMBER VC Number. Indicates target VC Number. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min Value 0x7 (MAX_VAL): Min Value Value After Reset: 0x0 Testable: writeAsRead
11	RO	0x0	reserved
10:8	RW	0x0	EINJ4_UPDFC_TYPE Update-FC type. Selects the credit type. Note: This register field is sticky. Values: 0x0 (POSTED_TLP_HDR): Posted TLP Header Credit value control 0x1 (NON_POSTED_TLP_HDR): Non-Posted TLP Header Credit value control 0x2 (CMPL_TLP_HDR): Completion TLP Header Credit value control 0x3 (RSERVED): Reserved 0x4 (POSTED_TLP_DATA): Posted TLP Data Credit value control 0x5 (NON_POSTED_TLP_DATA): Non-Posted TLP Data Credit value control 0x6 (CMPL_TLP_DATA): Completion TLP Data Credit value control 0x7 (RSVD): Reserved Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EINJ4_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION4_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION4_ENABLE =1, the errors are inserted until ERROR_INJECTION4_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ5_SP_TLP_REG
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	EINJ5_SPECIFIED_TLP Specified TLP. Selects the specified TLP to be inserted. Note: This register field is sticky. Values: 0x0 (DUPLICATE_DLLP): Generates duplicate TLPs by handling ACK DLLP as NAK DLLP. 0x1 (NULLIFIED_TLP): Generates Nullified TLP (Original TLP will be stored in retry buffer). Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ5_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION5_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION5_ENABLE =1, the errors are inserted until ERROR_INJECTION5_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H0_REG
Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H0 Packet Compare Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H1_REG
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H1 Packet Compare Point: 2nd DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H2_REG
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H2 Packet Compare Point: 3rd DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H3_REG
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H3 Packet Compare Point: 4th DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H0_REG
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H0 Packet Compare Value: 1st DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H1_REG

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H1 Packet Compare Value: 2nd DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H2_REG

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H2 Packet Compare Value: 3rd DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H3_REG

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H3 Packet Compare Value: 4th DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H0_REG

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H0 Packet Change Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H1_REG
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H1 Packet Change Point: 2nd DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H2_REG
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H2 Packet Change Point: 3rd DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H3_REG
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H3 Packet Change Point: 4th DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H0_REG
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H0 Packet Change Value: 1st DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H1_REG
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H1 Packet Change Value: 2nd DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H2_REG
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H2 Packet Change Value: 3rd DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H3_REG

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H3 Packet Change Value: 4th DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_EINJ6_TLP_REG

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:9	RW	0x0	EINJ6_PACKET_TYPE Packet type. Selects the TLP packets to inject errors into. All encodings other than the specified encodings are reserved. Note: This register field is sticky. Values: 0x0 (HEADER): TLP Header 0x1 (TLP_FIRST_4_DW): TLP Prefix 1st 4-DWORDs 0x2 (TLP_SECOND_DW): TLP Prefix 2nd -DWORDs Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
8	RW	0x0	EINJ6_INVERTED_CONTROL Inverted Error Injection Control. Encodded vlues given as above. Note: This register field is sticky. Values: 0x0 (REPLACE): EINJ6_CHANGE_VALUE_H[0/1/2/3] is used to replace bits specified by EINJ6_CHANGE_POINT_H[0/1/2/3]. 0x1 (IGNORE): EINJ6_CHANGE_VALUE_H[0/1/2/3] is ignored and inverts bits specified by EINJ6_CHANGE_POINT_H[0/1/2/3]. Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ6_COUNT Error Injection Count. Indicates the number of errors to insert. This counter is decremented while errors are been inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION6_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION6_ENABLE=1, errors are inserted until ERROR_INJECTION6_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_CONTROL1_REG

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	LOW_POWER_INTERVAL Low Power Entry Interval Time. Interval Time that the controller starts monitoring RXELECIDLE signal after L0s/L1/L2 entry. You should set the value according to the latency from receiving EIOS to, RXELECIDLE assertion at the PHY. Note: This register field is sticky. Values: 0x0 (_40NS): 40ns 0x1 (_160NS): 160ns 0x2 (_320NS): 320ns 0x3 (_640NS): 640ns Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21:20	RW	0x0	TX_EIOS_NUM Number of Tx EIOS. This register sets the number of transmit EIOS for L0s/L1 entry and Disable/Loopback/Hot-reset exit. The controller selects the greater value between this register and the value defined by the PCI-SIG specification. Note: This register field is sticky. Values: 0x0 (G2_2_EIOS_OTHER_SPEED_1_EIOS): (2.5GT/s, 8.0GT/s or higher) 1 or (5.0GT/s) 2 0x1 (G2_8_EIOS_OTHER_SPEED_4_EIOS): (2.5GT/s, 8.0GT/s or higher) 4 or (5.0GT/s) 8 0x2 (G2_16_EIOS_OTHER_SPEED_8_EIOS): (2.5GT/s, 8.0GT/s or higher) 8 or (5.0GT/s) 16 0x3 (G2_32_EIOS_OTHER_SPEED_16_EIOS): (2.5GT/s, 8.0GT/s or higher) 16 or (5.0GT/s) 32 Value After Reset: 0x0 Testable: writeAsRead
19:17	RO	0x0	reserved
16	RW	0x0	FORCE_DETECT_LANE_EN Force Detect Lane Enable. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set, the controller ignores receiver detection from PHY during LTSSM Detect state and uses FORCE_DETECT_LANE. Value After Reset: 0x0 Testable: writeAsRead
15:0	RW	0x0000	FORCE_DETECT_LANE Force Detect Lane. When the FORCE_DETECT_LANE_EN field is set, the controller ignores receiver detection from PHY during LTSSM Detect state and uses this value instead. Value represents lane number. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_SD_CONTROL2_REG

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	FRAMING_ERR_RECOVERY_DISABLE Framing Error Recovery Disable. This bit disables a transition to Recovery state when a Framing Error is occurred. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
15:11	RO	0x00	reserved
10	RW	0x0	DIRECT_LPBKSLV_TO_EXIT Direct Loopback Slave To Exit. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the LTSSM is in Loopback Slave Active State, the LTSSM transitions to Loopback Slave Exit state. Value After Reset: 0x0 Testable: writeAsRead
9	RW	0x0	DIRECT_POLCOMP_TO_DETECT Direct Polling.Compliance to Detect. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the LTSSM is in Polling Compliance State, the LTSSM transitions to Detect state. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
8	RW	0x0	DIRECT_RECIDLE_TO_CONFIG Direct Recovery.Idle to Configuration. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the LTSSM is in Recovery Idle State, the LTSSM transitions to Configuration state. Value After Reset: 0x0 Testable: writeAsRead
7:3	RO	0x00	reserved
2	RW	0x0	NOACK_FORCE_LINKDOWN Force LinkDown. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the controller detects REPLY_NUM rolling over 4 times, the LTSSM transitions to Detect State. Value After Reset: 0x0 Testable: writeAsRead
1	WO	0x0	RECOVERY_REQUEST Recovery Request. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set to '1' in L0 or L0s, the LTSSM starts transitioning to Recovery State. This request does not cause a speed change or re-equalization. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	HOLD_LTSSM Hold and Release LTSSM. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): As long as this field is '1', the controller stays in the current LTSSM. Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_SD_STATUS_L1LANE_REG

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DESKEW_POINTER Deskew Pointer. Indicates Deskew pointer of internal Deskew buffer of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved
20	RO	0x1	PIPE_TXELECIDLE PIPE:TxElecIdle. Indicates PIPE TXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
19	RO	0x1	PIPE_RXELECIDLE PIPE:RxElecIdle. Indicates PIPE RXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
18	RO	0x0	PIPE_RXVALID PIPE:RxValid. Indicates PIPE RXVALID signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17	RO	0x0	PIPE_DETECT_LANE PIPE:Detect Lane. Indicates whether PHY indicates receiver detection or not on selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
16	RO	0x0	PIPE_RXPOLARITY PIPE:RxPolarity. Indicates PIPE RXPOLARITY signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:4	RO	0x000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	LANE_SELECT Lane Select. Lane Select register for Silicon Debug Status Register of Layer1-PerLane. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_SD_STATUS_L1LTSSM_REG
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LTSSM_VARIABLE LTSSM Variable. Indicates internal LTSSM variables defined in the PCI Express Base Specification. For other value idle_to_rlock_transitioned. Note: This register field is sticky. Values: 0x0 (DIR_SPEED_CHANGE): directed_speed_change 0x1 (CHANGED_SPEED_RCVRY): changed_speed_recovery 0x2 (SUCCESSFUL_SPEED_NEGO): successful_speed_negotiation 0x3 (UPCFG_CAPABLE): upconfigure_capable; Set to '1' if both ports advertised the UpConfigure capability in the last Config.Complete. 0x4 (SEL_DE_EMPHASIS): select_deemphasis 0x5 (START_EQ_W_PRESET): start_equalization_w_preset 0x6 (EQ_DONE_8GT): equalization_done_8GT_data_rate 0x7 (EQ_DONE_16GT): equalization_done_16GT_data_rate Value After Reset: 0x0 Testable: untestable Volatile: true

Bit	Attr	Reset Value	Description
15	RO	0x0	LANE_REVERSAL Lane Reversal Operation. Receiver detected lane reversal. This field is only valid in the L0 LTSSM state. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14:11	RO	0x0	reserved
10:8	RO	0x2	PIPE_POWER_DOWN PIPE:PowerDown. Indicates PIPE PowerDown signal. Note: This register field is sticky. Value After Reset: 0x2 Testable: writeAsRead Volatile: true
7	W1C	0x0	FRAMING_ERR Framing Error. Indicates Framing Error detection status. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

6:0	RO	0x00	FRAMING_ERR_PTR First Framing Error Pointer. Identifies the first Framing Error using the following encoding. The field contents are only valid value when FRAMING_ERR =1. Received Unexpected Framing Token (Values 01h to 06h) Received Unexpected STP Token (Values 11h to 13h) Received Unexpected Block (Values 21h to 2Eh) All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x1 (STP_OR_SDP_OR_IDL_RECEIVED_NO_TLP_OR_DLLP): When non- STP/SDP/IDL Token was received and it was not in TLP/DLLP reception 0x2 (CURRENT_NO_VALID_EDB_PREVIOUS_VALID_EDB): When current token was not a valid EDB token and previous token was an EDB. (128/256 bit controller only) 0x3 (SDP_RECEIVED_NOT_EXPECTED): When SDP token was received but not expected. (128 bit & (x8 | x16) controller only) 0x4 (STP_RECEIVED_NOT_EXPECTED): When STP token was received but not expected. (128 bit & (x8 | x16) controller only) 0x5 (EDS_RECEIVED_NOT_EXPECTED): When EDS token was expected but not received or whenever an EDS token was received but not expected. 0x6 (FRE_ERR_DESKEW_PKT_IN_PROGRESS): When a framing error was detected in the deskew block while a packet has been in progress in token_finder. 0x11 (CRC_STP_NOT_MATCH): When Framing CRC in STP token did not match 0x12 (PARITY_STP_NOT_MATCH): When Framing Parity in STP token did not match. 0x13 (TLP_LENGTH_SMALLER_THEN_5DW): When Framing TLP Length in STP token was smaller than 5 DWORDs. 0x21 (RECEVING_OS_AFTER_SDS_IN_DATA_STREAM): When Receiving an OS Block following SDS in Datastream state 0x22 (AFTER_DATA_BLK_OS_BLK_NOT_SKP_EI_EIE): When Data Block followed by OS Block different from SKP, EI, EIE in Datastream state 0x23 (UNDEFINE_BLK_TYPE): When Block with an undefined Block Type in Datastream state 0x24 (DATA_STREAM_WITHOUT_3_CYCLE_DATA_STREAM_S): When Data Stream without data over three cycles in Datastream state 0x25 (OS_BLK_DURING_DATA_STREAM): When OS Block during Data Stream in Datastream state 0x26 (RXSTATUS_ERR_DATA_STREAM_STATE): When RxStatus Error was detected in Datastream state 0x27 (NOT_ALL_LANE_START_RECEVING_SKP_OS_SAME_T): When Not all active lanes receiving SKP OS starting at same cycle time in SKPOS state 0x28 (_2_BLK_TIMEOUT_SKP_OS_SKPOS_STATE): When a 2-Block timeout occurs for SKP OS in SKPOS state

Bit	Attr	Reset Value	Description
			0x29 (CONSECUTIVE_OS_WITHIN_DATA_IN_SKPOS_STATE): When Receiving consecutive OS Blocks within a Data Stream in SKPOS state 0x2a (PHYSTATUS_ERR_IN_SKPOS_STATE): When Phy status error was detected in SKPOS state 0x2b (NOT_ALL_LANE_START_RECEVING_EIOS_SAME_T): When Not all active lanes receiving EIOS starting at same cycle time in EIOS state 0x2c (AT_LEAST_1_SYM_IS_NOT_EIOS_FROM_4_SYM): When At least one Symbol from the first 4 Symbols is not EIOS Symbol in EIOS state (CX_NB=2 only) 0x2d (NOT_ALL_LANE_START_RECEVING_EIEOS_SAME_T): When Not all active lanes receiving EIEOS starting at same cycle time in EIEOS state 0x2e (NOT_16_EIEOS_SYM_RECEIVED): When Not full 16 eieos symbols are received in EIEOS state Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_STATUS_PM_REG
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	LATCHED_NFTS Latched N_FTS. Indicates the value of N_FTS in the received TS Ordered Sets from the Link Partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:13	RO	0x0	L1SUB_STATE L1Sub State. Indicates internal state machine of L1Sub state. Note: This register field is sticky. Values: 0x0 (S_L1_U): S_L1_U : idle state 0x1 (S_L1_0): S_L1_0 : wait for aux_clk_active 0x2 (S_L1_0_WAIT4_ACK): S_L1_0_WAIT4_ACK : wait for pclkack 0x3 (S_L1_0_WAIT4_CLKREQ): S_L1_0_WAIT4_CLKREQ : wait for clkreq 0x4 (S_L1_N_ENTRY): S_L1_N_ENTRY : check clkreq_in_n is de-asserted for t_power_off time (only for L1.2, reduces to one cycle for L1.1) 0x5 (S_L1_N): S_L1_N : L1 substate, turn off txcommonmode circuits (L1.2 only) and rx electrical idle detection circuits 0x6 (S_L1_N_EXIT): S_L1_N_EXIT : locally/remotely initiated exit, assert pclkreq, wait for pclkack 0x7 (S_L1_N_ABORT): S_L1_N_ABORT : wait for pclkack when aborting an attempt to enter L1_N Value After Reset: 0x0 Testable: writeAsRead Volatile: true
12	RW	0x0	PME_RESEND_FLAG PME Re-send flag. When the DUT sends a PM_PME message TLP, the DUT sets PME_Status bit. If host software does not clear PME_Status bit for 100ms(+50%/-5%), the DUT resends the PM_PME Message. This bit indicates that a PM_PME was resent. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:8	RO	0x0	INTERNAL_PM_SSTATE Internal PM State(Slave). Indicates internal state machine of Power Management Slave controller. Note: This register field is sticky. Values: 0x0 (S_IDLE): S_IDLE 0x1 (S_RESPOND_NAK): S_RESPOND_NAK 0x2 (S_BLOCK_TLP): S_BLOCK_TLP 0x3 (S_WAIT_LAST_TLP_ACK): S_WAIT_LAST_TLP_ACK 0x4 (S_WAIT_EIDLE): S_WAIT_EIDLE 0x5 (S_LINK_ENTR_L1): S_LINK_ENTR_L1 0x6 (S_L1): S_L1 0x7 (S_L1_EXIT): S_L1_EXIT 0x8 (S_L23RDY): S_L23RDY 0x9 (S_LINK_ENTR_L23): S_LINK_ENTR_L23 0xa (S_L23RDY_WAIT4ALIVE): S_L23RDY_WAIT4ALIVE 0xb (S_ACK_WAIT4IDLE): S_ACK_WAIT4IDLE 0xc (S_WAIT_LAST_PMDLLP): S_WAIT_LAST_PMDLLP Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RO	0x00	INTERNAL_PM_MSTATE Internal PM State(Master). Indicates internal state machine of Power Management Master controller. Note: This register field is sticky. Values: 0x0 (IDLE): IDLE 0x1 (L0): L0 0x2 (L0S): L0S 0x3 (ENTER_L0S): ENTER_L0S 0x4 (EXIT_L0S): L0S_EXIT 0x5 (WAIT_PMCSR_CPL_SENT): WAIT_PMCSR_CPL_SENT 0x8 (L1): L1 0x9 (L1_BLOCK_TLP): L1_BLOCK_TLP 0xa (L1_WAIT_LAST_TLP_ACK): L1_WAIT_LAST_TLP_ACK 0xb (L1_WAIT_PMDLLP_ACK): L1_WAIT_PMDLLP_ACK 0xc (L1_LINK_ENTR_L1): L1_LINK_ENTR_L1 0xd (L1_EXIT): L1_EXIT 0xf (PREP_4L1): PREP_4L1 0x10 (L23_BLOCK_TLP): L23_BLOCK_TLP 0x11 (L23_WAIT_LAST_TLP_ACK): L23_WAIT_LAST_TLP_ACK 0x12 (L23_WAIT_PMDLLP_ACK): L23_WAIT_PMDLLP_ACK 0x13 (L23_ENTR_L23): L23_ENTR_L23 0x14 (L23RDY): L23RDY 0x15 (PREP_4L23): PREP_4L23 0x16 (L23RDY_WAIT4ALIVE): L23RDY_WAIT4ALIVE 0x17 (L0S_BLOCK_TLP): L0S_BLOCK_TLP 0x18 (WAIT_LAST_PMDLLP): WAIT_LAST_PMDLLP 0x19 (WAIT_DSTATE_UPDATE): WAIT_DSTATE_UPDATE Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_STATUS_L2_REG

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	FC_INIT2 FC_INIT2. Indicates the controller is in FC_INIT2(VC0) state. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
26	RO	0x0	FC_INIT1 FC_INIT1. Indicates the controller is in FC_INIT1(VC0) state. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
25:24	RO	0x0	DLCMSM DLCMSM. Indicates the current DLCMSM. Note: This register field is sticky. Values: 0x0 (DL_INACTIVE): DL_INACTIVE 0x1 (DL_FC_INIT): DL_FC_INIT 0x3 (DL_ACTIVE): DL_ACTIVE Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:12	RO	0xfff	RX_ACK_SEQ_NO Tx Ack Sequence Number. Indicates ACKD_SEQ which is updated by receiving ACK/NAK DLLP. Note: This register field is sticky. Value After Reset: 0xfff Testable: writeAsRead Volatile: true
11:0	RO	0x000	TX_TLP_SEQ_NO Tx Tlp Sequence Number. Indicates next transmit sequence number for transmit TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_STATUS_L3FC_REG
Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	CREDIT_DATA1 Credit Data1. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. Rx: Credit Allocated Value Tx: Credit Limit Value. This value is valid when DLCMSM=0x3(DL_ACTIVE). Note: This register field is sticky. Value After Reset: 0x0 Testable: untestable Volatile: true
19:8	RO	0x000	CREDIT_DATA0 Credit Data0. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. Rx: Credit Received Value Tx: Credit Consumed Value Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved
6	RW	0x0	CREDIT_SEL_HD Credit Select(HeaderData). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_TLP_TYPE viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (HEADER_CREDIT): Header Credit 0x1 (DATA_CREDIT): Data Credit Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
5:4	RW	0x0	CREDIT_SEL_TLP_TYPE Credit Select(TLP Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (POSTED): Posted 0x1 (NON_POSTED): Non-Posted 0x2 (COMPLETION): Completion Value After Reset: 0x0 Testable: writeAsRead
3	RW	0x0	CREDIT_SEL_CREDIT_TYPE Credit Select(Credit Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (RX): Rx 0x1 (TX): Tx Value After Reset: 0x0 Testable: writeAsRead
2:0	RW	0x0	CREDIT_SEL_VC Credit Select(VC). This field in conjunction with the CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (MIN_VAL): VC0 0x7 (MAX_VAL): VC7 Value After Reset: 0x0

DSP_PCIE_RAS_DES_SD_STATUS_L3_REG

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	MFTLP_STATUS Malformed TLP Status. Indicates malformed TLP has occurred. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6:0	RO	0x00	MFTLP_POINTER First Malformed TLP Error Pointer. Indicates the element of the received first malformed TLP. This pointer is validated by MFTLP_STATUS. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x1 (ATMC_OP_ALIGN): AtomicOp address alignment 0x2 (ATMC_OP_OPERAND): AtomicOp operand 0x3 (ATMC_OP_BYTE_EN): AtomicOp byte enable 0x4 (TLP_LENGTH_MISMATCH): TLP length miss match 0x5 (MAX_PAYLOAD_SIZE): Max payload size 0x6 (TLP_WITHOUT_TC0): Message TLP without TC0 0x7 (INVALID_TC): Invalid TC 0x8 (UNXPCTD_ROUTE_BIT_MSG_TLP): Unexpected route bit in Message TLP 0x9 (UNXPCTD_CRS_STATUS_CMPL_TLP): Unexpected CRS status in Completion TLP 0xa (BYTE_ENABLE): Byte enable 0xb (MEM_ADDR_4KB_BOUNDARY): Memory Address 4KB boundary 0xc (TLP_PREFIX_RULES): TLP prefix rules 0xd (TRANSLATION_RULES): Translation request rules 0xe (INVALID_TLP_TYPE): Invalid TLP type 0xf (CMPL_RULES): Completion rules 0x7f (APPLICATION): Application Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_EQ_CONTROL1_REG
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	FOM_TARGET FOM Target. Indicates figure of merit target criteria value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2). This field is only valid when GEN3_EQ_FB_MODE is 0001b(Figure Of Merit). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	FOM_TARGET_ENABLE FOM Target Enable. Enables the FOM_TARGET fields. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
22:18	RO	0x00	reserved
17:16	RW	0x0	EVAL_INTERVAL_TIME Eval Interval Time. Indicates interval time of RxEqEval assertion. This field is used for EQ Master(DSP in EQ Phase3/USP in EQ Phase2). Note: This register field is sticky. Values: 0x0 (_500NS): 500ns 0x1 (_1US): 1us 0x2 (_2US): 2us 0x3 (_4US): 4us Value After Reset: 0x0 Testable: writeAsRead
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	EXT_EQ_TIMEOUT Extends EQ Phase2/3 Timeout. This field is used when the LTSSM is in Recovery.EQ2/3. When this field is set, the value of EQ2/3 timeout is extended. Note: This register field is sticky. Values: 0x0 (_24MS_OR_32MS): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] 24ms (default) or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] 32ms (default) 0x1 (_48MS_OR_56MS): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] 48ms (x2) or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] 56ms (32ms+24ms) 0x2 (_240MS_OR_248MS): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] 240ms (x10) or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] 248ms (32ms +9*24ms) 0x3 (NO_TIMEOUT): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] No timeout or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] No timeout Value After Reset: 0x0 Testable: writeAsRead
7:5	RO	0x0	reserved
4	RW	0x0	EQ_RATE_SEL EQ Status Rate Select. Setting this field in conjunction with the EQ_LANE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky. Values: 0x0 (_8GT): 8.0GT/s Speed (include ESM data rate) 0x1 (_16GT): 16.0GT/s Speed (include ESM data rate) 0x2 (_32GT): 32.0GT/s Speed Value After Reset: 0x0 Testable: writeAsRea

Bit	Attr	Reset Value	Description
3:0	RW	0x0	EQ_LANE_SEL EQ Status Lane Select. Setting this field in conjunction with the EQ_RATE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

DSP_PCIE_RAS_DES_SD_EQ_CONTROL2_REG
Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	FORCE_LOCAL_TX_PRESET_ENABLE Force Local Transmitter Preset Enable. Enables the FORCE_LOCAL_TX_PRESET field. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
29	RW	0x0	FORCE_LOCAL_RX_HINT_ENABLE Force Local Receiver Preset Hint Enable. Enables the FORCE_LOCAL_RX_HINT field. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
28	RW	0x0	FORCE_LOCAL_TX_COEF_ENABLE Force Local Transmitter Coefficient Enable. Enables the following fields: FORCE_LOCAL_TX_PRE_CURSOR FORCE_LOCAL_TX_CURSOR FORCE_LOCAL_TX_POST_CURSOR Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
27:24	RW	0x0	FORCE_LOCAL_TX_PRESET Force Local Transmitter Preset. Indicates initial preset value of USP in EQ Slave(EQ Phase2) instead of receiving EQ TS2. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved
20:18	RW	0x0	FORCE_LOCAL_RX_HINT Force Local Receiver Preset Hint. Indicates the RxPresetHint value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of received or set value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17:12	RW	0x00	FORCE_LOCAL_TX_POST_CURSOR Force Local Transmitter Post-Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:6	RW	0x00	FORCE_LOCAL_TX_CURSOR Force Local Transmitter Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RW	0x00	FORCE_LOCAL_TX_PRE_CURSOR Force Local Transmitter Pre-cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_EQ_CONTROL3_REG
Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	FORCE_REMOTE_TX_COEF_ENABLE Force Remote Transmitter Coefficient Enable. Enables the following fields: FORCE_REMOTE_TX_PRE_CURSOR FORCE_REMOTE_TX_CURSOR FORCE_REMOTE_TX_POST_CURSOR This function can only be used when GEN3_EQ_FB_MODE = 0000b(Direction Change) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
27:18	RO	0x000	reserved

Bit	Attr	Reset Value	Description
17:12	RW	0x00	FORCE_REMOTE_TX_POST_CURSOR Force Remote Transmitter Post-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:6	RW	0x00	FORCE_REMOTE_TX_CURSOR Force Remote Transmitter Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RW	0x00	FORCE_REMOTE_TX_PRE_CURSOR Force Remote Transmitter Pre-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_EQ_STATUS1_REG

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RO	0x0	EQ_REJECT_EVENT EQ Reject Event. Indicates that the controller receives two consecutive TS1 OS w/Reject=1b during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6	RO	0x0	EQ_RULEC_VIOLATION EQ Rule C Violation. Indicates that coefficients rule C violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rule C correspond to the rules c) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5	RO	0x0	EQ_RULEB_VIOLATION EQ Rule B Violation. Indicates that coefficients rule B violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules B correspond to the rules b) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
4	RO	0x0	EQ_RULEA_VIOLATION EQ Rule A Violation. Indicates that coefficients rule A violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules A correspond to the rules a) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	RO	0x0	reserved
2:1	RO	0x0	EQ_CONVERGENCE_INFO EQ Convergence Info. Indicates equalization convergence information. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Values: 0x0 (EQ_NOT_ATTEMPTED): Equalization is not attempted 0x1 (EQ_SUCCESSFUL): Equalization finished successfully 0x2 (EQ_UNSUCCESSFUL): Equalization finished unsuccessfully 0x3 (RSVD): Reserved Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RO	0x0	EQ_SEQUENCE EQ Sequence. Indicates that the controller is starting the equalization sequence. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_EQ_STATUS2_REG
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EQ_LOCAL_FOM_VALUE EQ Local Figure of Merit. Indicates Local maximum Figure of Merit value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved
20:18	RO	0x0	EQ_LOCAL_RX_HINT EQ Local Receiver Preset Hint. Indicates Local Receiver Preset Hint value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17:12	RO	0x00	EQ_LOCAL_POST_CURSOR EQ Local Post-Cursor. Indicates Local post cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:6	RO	0x00	EQ_LOCAL_CURSOR EQ Local Cursor. Indicates Local cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
5:0	RO	0x00	EQ_LOCAL_PRE_CURSOR EQ Local Pre-Cursor. Indicates Local pre cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_RAS_DES_SD_EQ_STATUS3_REG

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	EQ_REMOTE_FS EQ Remote FS. Indicates Remote FS value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:18	RO	0x00	EQ_REMOTE_LF EQ Remote LF. Indicates Remote LF value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17:12	RO	0x00	EQ_REMOTE_POST_CURSOR EQ Remote Post-Cursor. Indicates Remote post cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:6	RO	0x00	EQ_REMOTE_CURSOR EQ Remote Cursor. Indicates Remote cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RO	0x00	EQ_REMOTE_PRE_CURSOR EQ Remote Pre-Cursor. Indicates Remote pre cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

11.4.3.19 DSP_PCIE_VSECDMA Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_VSECDMA_EXT_CAP_HDR_OFF	0x0000	W	0x0001000B	PCIe Extended Capability ID, Capability Version, and Next Capability Offset Register
DSP_PCIE_VSECDMA_VENDOR_SPECIFIC_HDR_OFF	0x0004	W	0x01800006	Vendor Specific Header Register
DSP_PCIE_VSECDMA_DEVICE_INFORMATION_OFF	0x0008	W	0x00A80401	DMA and related AXI Bridge Implementation Information
DSP_PCIE_VSECDMA_NUM_CHAN_OFF	0x000C	W	0x00020002	Number of Implemented Channels Register
DSP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_LOW_OFF	0x0010	W	0x00000000	DMA Register Map Start Address Offset Low Register
DSP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_HIGH_OFF	0x0014	W	0x00000000	DMA Register Map Start Address Offset High Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.20 DSP_PCIE_VSECDMA Detail Registers Description

DSP_PCIE_VSECDMA_EXT_CAP_HDR_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
19:16	RW	0x1	CAP Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. A version of the specification that changes the Extended Capability in a way that is not otherwise identifiable (that is, through a new Capability field) is permitted to increment this field. All such changes to the Capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as Functions reporting any such Capability Version numbers will contain a Capability structure that is compatible with that piece of software. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15:0	RW	0x000b	ID PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0xb Testable: writeAsRead

DSP_PCIE_VSECDMA_VENDOR_SPECIFIC_HDR_OFF

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:20	RO	0x018	VSEC_LENGTH VSEC Length. This field indicates the number of bytes in the entire VSEC structure, including the Vendor-Specific Extended Capability Header, the Vendor-Specific Header, and the vendor-specific registers. Value After Reset: 0x18
19:16	RO	0x0	VSEC_REV VSEC Rev. This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field. Value After Reset: 0x0
15:0	RO	0x0006	VSEC_ID VSEC ID. This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field. Value After Reset: 0x6

DSP_PCIE_VSECDMA_DEVICE_INFORMATION_OFF

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	MASTER_PAGE_BOUNDARY_POINTER_WIDTH This field provides address page boundary information. It reports the value of CC_MSTR_PAGE_BOUNDARY_PW configuration parameter. Value After Reset: 0xd

Bit	Attr	Reset Value	Description
25:23	RO	0x1	MASTER_BURST_LENGTH Reports the CC_MSTR_BURST_LEN configuration parameter. Values: 0x0 (MSTR_BRSTLEN_8): 8 bits 0x1 (MSTR_BRSTLEN_16): 16 bits 0x2 (MSTR_BRSTLEN_32): 32 bits 0x3 (MSTR_BRSTLEN_64): 64 bits 0x4 (MSTR_BRSTLEN_128): 128 bits 0x5 (MSTR_BRSTLEN_256): 256 bits Value After Reset: 0x1
22:20	RO	0x2	MASTER_BUS_WIDTH This field provides information regarding the AXI master data bus width. It reports the value of MASTER_BUS_DATA_WIDTH configuration parameter. Values: 0x0 (MSTR_BUSWD_32): 32 bits 0x1 (MSTR_BUSWD_64): 64 bits 0x2 (MSTR_BUSWD_128): 128 bits 0x3 (MSTR_BUSWD_256): 256 bits 0x4 (MSTR_BUSWD_512): 512 bits Value After Reset: 0x2
19	RO	0x1	AXI This field provides information about AXI interface usage. It reports the value of AXI_POPULATED configuration parameter. Value After Reset: 0x1
18:16	RO	0x0	CHANNEL_SEPARATION If the MAP_FORMAT is set to HDMA_NATIVE, this field specifies the read write channel address separation. Other values are reserved. Values: 0x0 (CHSEP_256): 256 separated 0x1 (CHSEP_512): 512 separated 0x2 (CHSEP_1K): 1k separated 0x3 (CHSEP_2K): 2k separated 0x4 (CHSEP_4K): 4k separated 0x5 (CHSEP_8K): 8k separated 0x6 (CHSEP_16K): 16k separated 0x7 (CHSEP_32K): 32k separated Value After Reset: 0x0
15:11	RO	0x00	PFN Physical Function Number. This field provides information regarding the DMA register and physical function mapping. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
10:8	RO	0x4	BARN Bar Number. This field provides information regarding the DMA register and BAR number mapping. Value After Reset: 0x4
7:3	RO	0x00	reserved
2:0	RO	0x1	MAP_FORMAT Defines the register map format and features to be one of the following values: Other values are reserved. Values: 0x0 (EDMA_LEGACY_PL): Legacy DMA register map accessed by the port-logic registers 0x1 (EDMA_LEGACY_UNROLL): Legacy DMA register map, mapped to a PF/BAR 0x5 (HDMA_COMPATIBILITY_MODE): HDMA compatibility mode (CC_LEGACY_DMA_MAP =1) register map, mapped to a PF/BAR 0x7 (HDMA_NATIVE): HDMA native (CC_LEGACY_DMA_MAP =0) register map, mapped to a PF/BAR Value After Reset: 0x1

DSP_PCIE_VSECDMA_NUM_CHAN_OFF

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x002	NUM_DMA_RD_CHAN This field provides information regarding the number of implemented read channels. It reports the value of CC_NUM_DMA_RD_CHAN parameter. Value After Reset: 0x2
15:10	RO	0x00	reserved
9:0	RO	0x002	NUM_DMA_WR_CHAN This field provides information regarding the number of implemented write channels. It reports the value of CC_NUM_DMA_WR_CHAN parameter. Value After Reset: 0x2

DSP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_LOW_OFF

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	UNROLL_ADDR_OFFSET_LOW BAR address offset, 32-bit LSB. Value After Reset: 0x0

DSP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_HIGH_OFF

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	UNROLL_ADDR_OFFSET_HIGH BAR address offset, 32-bit MSB. Value After Reset: 0x0

11.4.3.21 DSP_PCIE_PL Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_PL_ACK_LATENCY_TIMER_OFF	0x0000	W	0x0C23040B	Ack Latency Timer and Replay Timer Register
DSP_PCIE_PL_VENDOR_SPEC_DLLP_OFF	0x0004	W	0xFFFFFFFF	Vendor Specific DLLP Register
DSP_PCIE_PL_PORT_FORCE_OFF	0x0008	W	0x00800004	Port Force Link Register
DSP_PCIE_PL_ACK_F_ASPM_CTRL_OFF	0x000C	W	0x1BD2D200	Ack Frequency and L0-L1 ASPM Control Register
DSP_PCIE_PL_PORT_LINK_CTRL_OFF	0x0010	W	0x00030120	Port Link Control Register
DSP_PCIE_PL_LANE_SKEW_OFF	0x0014	W	0x08000000	Lane Skew Register
DSP_PCIE_PL_TIMER_CTRL_MAX_FUNC_NUM_OFF	0x0018	W	0x00000000	Timer Control and Max Function Number Register
DSP_PCIE_PL_SYMBOL_TIMER_FILTER_1_OFF	0x001C	W	0x00000140	Symbol Timer Register and Filter Mask 1 Register
DSP_PCIE_PL_FILTER_MASK_2_OFF	0x0020	W	0x00000000	Filter Mask 2 Register
DSP_PCIE_PL_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF	0x0024	W	0x00000001	AMBA Multiple Outbound Decomposed NP SubRequests Control Register
DSP_PCIE_PL_PL_DEBUG0_OFF	0x0028	W	0x00000000	Debug Register 0
DSP_PCIE_PL_PL_DEBUG1_OFF	0x002C	W	0x00000000	Debug Register 1
DSP_PCIE_PL_TX_P_FC_CREDIT_STATUS_OFF	0x0030	W	0x00000000	Transmit Posted FC Credit Status
DSP_PCIE_PL_TX_NP_FC_CREDIT_STATUS_OFF	0x0034	W	0x00000000	Transmit Non-Posted FC Credit Status
DSP_PCIE_PL_TX_CPL_FC_CREDIT_STATUS_OFF	0x0038	W	0x00000000	Transmit Completion FC Credit Status
DSP_PCIE_PL_QUEUE_STATUS_OFF	0x003C	W	0x00000000	Queue Status
DSP_PCIE_PL_VC_TX_ARBI_1_OFF	0x0040	W	0x0000000F	VC Transmit Arbitration Register 1
DSP_PCIE_PL_VC_TX_ARBI_2_OFF	0x0044	W	0x00000000	VC Transmit Arbitration Register 2
DSP_PCIE_PL_VC0_P_RX_Q_CTRL_OFF	0x0048	W	0x45227110	Segmented-Buffer VC0 Posted Receive Queue Control
DSP_PCIE_PL_VC0_NP_RX_Q_CTRL_OFF	0x004C	W	0x0505C017	Segmented-Buffer VC0 Non-Posted Receive Queue Control
DSP_PCIE_PL_VC0_CPL_RX_Q_CTRL_OFF	0x0050	W	0x05000000	Segmented-Buffer VC0 Completion Receive Queue Control
DSP_PCIE_PL_GEN2_CTRL_OFF	0x010C	W	0x000102D2	Link Width and Speed Change Control Register

Name	Offset	Size	Reset Value	Description
DSP_PCIE_PL_PHY_STATUS_OFF	0x0110	W	0x00000000	PHY Status Register
DSP_PCIE_PL_PHY_CONTROL_OFF	0x0114	W	0x00000001	PHY Control Register
DSP_PCIE_PL_TRGT_MAP_CTRL_OFF	0x011C	W	0x00000047	Programmable Target Map Control Register
DSP_PCIE_PL_CLOCK_GATING_CTRL_OFF	0x018C	W	0x00000003	RADM clock gating enable control register
DSP_PCIE_PL_GEN3_RELATED_OFF	0x0190	W	0x00000000	Gen3 Control Register
DSP_PCIE_PL_GEN3_EQ_CONTROL_OFF	0x01A8	W	0x04059F61	Gen3 EQ Control Register
DSP_PCIE_PL_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF	0x01AC	W	0x00000040	Gen3 EQ Direction Change Feedback Mode Control Register
DSP_PCIE_PL_ORDER_RULE_CTRL_OFF	0x01B4	W	0x00000000	Order Rule Control Register
DSP_PCIE_PL_PIPE_LOOPBACK_CONTROL_OFF	0x01B8	W	0x0000000F	PIPE Loopback Control Register
DSP_PCIE_PL_MISC_CONTROL_1_OFF	0x01BC	W	0x00037F40	DBI Read-Only Write Enable Register
DSP_PCIE_PL_MULTI_LANE_CONTROL_OFF	0x01C0	W	0x00000080	UpConfigure Multi-lane Control Register
DSP_PCIE_PL_PHY_INTEROP_CTRL_OFF	0x01C4	W	0x0001E044	PHY Interoperability Control Register
DSP_PCIE_PL_TRGT_CPL_LUT_DELETE_ENTRY_OFF	0x01C8	W	0x00000000	TRGT_CPL_LUT Delete Entry Control Register
DSP_PCIE_PL_LINK_FLUSH_CONTROL_OFF	0x01CC	W	0x00000000	Link Reset Request Flush Control Register
DSP_PCIE_PL_AMBA_ERROR_RESPONSE_DEFAULT_OFF	0x01D0	W	0x00009C00	AXI Bridge Slave Error Response Register
DSP_PCIE_PL_AMBA_LINK_TIMEOUT_OFF	0x01D4	W	0x00000032	Link Down AXI Bridge Slave Timeout Register
DSP_PCIE_PL_AMBA_ORDERING_CTRL_OFF	0x01D8	W	0x00000000	AMBA Ordering Control
DSP_PCIE_PL_COHERENCY_CONTROL_1_OFF	0x01E0	W	0x00000000	ACE Cache Coherency Control Register 1
DSP_PCIE_PL_COHERENCY_CONTROL_2_OFF	0x01E4	W	0x00000000	ACE Cache Coherency Control Register 2
DSP_PCIE_PL_COHERENCY_CONTROL_3_OFF	0x01E8	W	0x00000000	ACE Cache Coherency Control Register 3
DSP_PCIE_PL_AXI_MSTR_MSG_ADDR_LOW_OFF	0x01F0	W	0x00000000	Lower 32-bits of the Programmable AXI Address
DSP_PCIE_PL_AXI_MSTR_MSG_ADDR_HIGH_OFF	0x01F4	W	0x00000000	Upper 32-bits of the Programmable AXI Address
DSP_PCIE_PL_PCIE_VERSION_NUMBER_OFF	0x01F8	W	0x3536302A	PCIe Controller IIP Release Version Number
DSP_PCIE_PL_PCIE_VERSION_TYPE_OFF	0x01FC	W	0x6C703035	PCIe Controller IIP Release Version Type
DSP_PCIE_PL_MSIX_ADDRESS_MATCH_LOW_OFF	0x0240	W	0x00000000	MSI-X Address Match Low Register

Name	Offset	Size	Reset Value	Description
DSP_PCIE_PL_MSIX_ADDRESS_MATCH_HIGH_OFF	0x0244	W	0x00000000	MSI-X Address Match High Register
DSP_PCIE_PL_MSIX_DOORBELL_OFF	0x0248	W	0x00000000	MSI-X Doorbell Register
DSP_PCIE_PL_MSIX_RAM_CTRL_OFF	0x024C	W	0x00000000	MSI-X RAM Power Mode and Debug Control Register
DSP_PCIE_PL_DTIM_CTRL0_OFF	0x03B0	W	0x001FFFFF	DTI Master Control Register 0
DSP_PCIE_PL_DTIM_CTRL1_OFF	0x03B4	W	0x00000000	DTI Master Control Register 1
DSP_PCIE_PL_DTIM_CTRL2_OFF	0x03B8	W	0x00000000	DTI Master Control Register 2
DSP_PCIE_PL_DTIM_CTRL3_OFF	0x03BC	W	0x00004210	DTI Master Control Register 3
DSP_PCIE_PL_DTIM_CTRL4_OFF	0x03C0	W	0x00000000	DTI Master Control Register 4
DSP_PCIE_PL_DTIM_CTRL5_OFF	0x03C4	W	0x00000000	DTI Master Control Register 5
DSP_PCIE_PL_DTIM_INT_STATUS_OFF	0x03CC	W	0x00000000	DTI Master Interrupt Status Register
DSP_PCIE_PL_DTIM_INT_EN_OFF	0x03D0	W	0x00000000	DTI Master Interrupt Enable Register
DSP_PCIE_PL_DTIM_INT_CLR_OFF	0x03D4	W	0x00000000	DTI Master Interrupt Clear Register
DSP_PCIE_PL_DTIM_INT_MSK_OFF	0x03D8	W	0x00000000	DTI Master Interrupt Mask Register
DSP_PCIE_PL_DTIM_MSI_ADDR_UPR_OFF	0x03DC	W	0x00000000	DTI Master MSI Upper Address Register
DSP_PCIE_PL_DTIM_MSI_ADDR_LWR_OFF	0x03E0	W	0x00000000	DTI Master MSI Lower Address Register
DSP_PCIE_PL_DTIM_MSI_DATA_OFF	0x03E4	W	0x00000000	DTI Master MSI Data Register
DSP_PCIE_PL_DTIM_ERR_LOG0_OFF	0x03E8	W	0x00000000	DTI Master Error Logging Register 0
DSP_PCIE_PL_DTIM_ERR_LOG1_OFF	0x03EC	W	0x00000000	DTI Master Error Logging Register 1
DSP_PCIE_PL_DTIM_ERR_LOG2_OFF	0x03F0	W	0x00000000	DTI Master Error Logging Register 2
DSP_PCIE_PL_DTIM_DIAG_OFF	0x03FC	W	0x00000010	DTI Master Debug Diagnostic Register
DSP_PCIE_PL_PL_APP_BUS_DEV_NUM_STATUS_OFF	0x0410	W	0x00000000	Application Driven bus and Device Number Register
DSP_PCIE_PL_PCIPM_TRAFFIC_CTRL_OFF	0x041C	W	0x00000000	TLP Traffic during Non-D0 State Control Register
DSP_PCIE_PL_PL_LTR_LATENCY_OFF	0x0430	W	0x00000000	LTR Latency Register
DSP_PCIE_PL_AUX_CLK_FREQ_OFF	0x0440	W	0x00000018	Auxiliary Clock Frequency Control Register
DSP_PCIE_PL_L1_SUBSTATES_OFF	0x0444	W	0x000000D2	L1 Substates Timing Register
DSP_PCIE_PL_POWERDOWN_CTRL_STATUS_OFF	0x0448	W	0x00000020	Powerdown Control and Status Register

Name	Offset	Size	Reset Value	Description
DSP_PCIE_PL_PIPE_RELATED_OFF	0x0490	W	0x00000000	PIPE Related Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.22 DSP_PCIE_PL Detail Registers Description

DSP_PCIE_PL_ACK_LATENCY_TIMER_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0c23	REPLAY_TIME_LIMIT Replay Timer Limit. The replay timer expires when it reaches this limit. The controller initiates a replay upon reception of a NAK or when the replay timer expires. For more details, see "Transmit Replay" in the Databook. You can modify the effective timer limit through the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-4, 3-5, and 3-6 of the PCI Express Base Specification. If there is a change in the payload size or link speed, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. Value After Reset: 0xc23 Testable: untestable Volatile: true

Bit	Attr	Reset Value	Description
15:0	RW	0x040b	ROUND_TRIP_LATENCY_TIME_LIMIT Ack Latency Timer Limit. The Ack latency timer expires when it reaches this limit. For more details, see "ACK/NAK Scheduling" in the Databook. You can modify the effective timer limit through the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-7, 3-8, and 3-9 of the PCI Express Base Specification. The limit must reflect the round trip latency from requester to completer. If there is a change in the payload size or link width, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. Value After Reset: 0x40b Testable: untestable Volatile: true

DSP_PCIE_PL_VENDOR_SPEC_DLLP_OFF
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	VENDOR_SPEC_DLLP Vendor Specific DLLP Register. You can use this register to send a specific PCI Express DLLP. Your application can write 8-bit DLLP Type and 24-bit Payload data into this register, and set the VENDOR_SPECIFIC_DLLP_REQ field of the PORT_LINK_CTRL_OFF, to send the DLLP. Bits[7:0]: DLLP Type Bits[31:8]: Vendor Defined Payload (24 bits) Note: This register field is sticky. Values: 0x0 (ZERO): Zero value 0xffffffff (MAX): Max value Value After Reset: 0xffffffff

DSP_PCIE_PL_PORT_FORCE_OFF
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x1	DO_DESKEW_FOR_SRIS Use the transitions from TS2 to Logical Idle Symbol, SKP OS to Logical Idle Symbol, EIEOS to Logical Idle Symbol, and FTS Sequence to SKP OS to do deskew instead of using received SKP OS or TS1 to TS2 transition if DO_DESKEW_FOR_SRIS is set to '1'. Note: This register field is sticky. Value After Reset: 0x1
22	RW	0x0	SUPPORT_PART_LANES_RXEI_EXIT Support LTSSM transition from Polling.Active to Polling.Config based on Rx 8 TSs on any lanes which are Rx EI exit too from base spec after 24ms timeout. This prevents some lanes detected but not Rx EI exit and LTSSM cannot move to Polling.Config. You must set the parameter CX_AUTO_LANE_FLIP_CTRL_EN true for the auto lanes reversal. Note: This register field is sticky. Values: 0x1 (SUPPORT): Any lanes receives 8 consecutive TS OSs, LTSSM moves from Polling.Active to Polling.Config. If all lanes do not receive 8 consecutive TS OSs and any predetermined lanes are still on Rx ElecIdle, LTSSM moves from Polling.Active to Polling.Compliance. 0x0 (UNSUPPORT): Any lanes receives 8 consecutive TS OS and all predetermined lanes have Rx ElecIdle exit, LTSSM moves from Polling.Active to Polling.Config. This is legacy mode from Base Spec. Any predetermined lanes are still on Rx ElecIdle, LTSSM moves from Polling.Active to Polling.Compliance. Value After Reset: 0x0
21:16	RW	0x00	LINK_STATE Forced LTSSM State. The LTSSM state that the controller is forced to when you set the FORCE_EN bit (Force Link). LTSSM state encoding is defined by the lts_state variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15	WO	0x0	FORCE_EN Force Link. The controller supports a testing and debug capability to allow your software to force the LTSSM state machine into a specific state, and to force the controller to transmit a specific Link Command. Asserting this bit triggers the following actions: Forces the LTSSM to the state specified by the Forced LTSSM State field. Forces the controller to transmit the command specified by the Forced Link Command field. This is a self-clearing register field. Reading from this register field always returns a '0'. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14:12	RO	0x0	reserved
11:8	RW	0x0	FORCED_LTSSM Forced Link Command. The link command that the controller is forced to transmit when you set FORCE_EN bit (Force Link). Link command encoding is defined by the ltssm_cmd variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky. Value After Reset: 0x0
7:0	RW	0x04	LINK_NUM Link Number. Not used for endpoint. Note: This register field is sticky. Value After Reset: 0x4

DSP_PCIE_PL_ACK_F_ASPM_CTRL_OFF

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30	RW	0x0	ENTER_ASPM ASPM L1 Entry Control. Note: This register field is sticky. Values: 0x1 (IDLE_TO_L1): Controller enters ASPM L1 after a period in which it has been idle. 0x0 (L0S_TO_L1): Controller enters ASPM L1 only after idle period during which both receive and transmit are in L0s. Value After Reset: 0x0
29:27	RW	0x3	L1_ENTRANCE_LATENCY L1 Entrance Latency. Note: Programming this timer with a value greater that 32us has no effect unless extended sync is used, or all of the credits are infinite. Note: This register field is sticky. Values: 0x0 (_1_US): 1 us 0x1 (_2_US): 2 us 0x2 (_4_US): 4 us 0x3 (_8_US): 8 us 0x4 (_16_US): 16 us 0x5 (_32_US): 32 us 0x6 (_64_US): 64Us 0x7 (_64US_): 64 us Value After Reset: 0x3
26:24	RW	0x3	L0S_ENTRANCE_LATENCY L0s Entrance Latency. Note: This register field is sticky. Values: 0x0 (_1_US): 1 us 0x1 (_2_US): 2 us 0x2 (_3_US): 3 us 0x3 (_4_US): 4 us 0x4 (_5_US): 5 us 0x5 (_6_US): 6 us 0x6 (_7_US): 7 US 0x7 (_7US_): 7 us Value After Reset: 0x3

Bit	Attr	Reset Value	Description
23:16	RO	0xd2	COMMON_CLK_N_FTS Common Clock N_FTS. This is the N_FTS when common clock is used. The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. This field is only writable (sticky) when all of the following configuration parameter equations are true: CX_NFTS !=CX_COMM_NFTS DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Values: 0x0 (ZERO): The controller does not support a value of zero; a value of zero can cause the LTSSM to go into the recovery state when exiting from L0s. 0xff (MAX_VAL): The maximum number of FTS ordered-sets that a component can request is 255. Value After Reset: 0xd2
15:8	RW	0xd2	ACK_N_FTS The number of Fast Training Sequence(N_FTS) ordered sets to be transmitted when transitioning from L0s to L0. Note: This register field is sticky. Values: 0x0 (ZERO): The controller does not support a value of zero; a value of zero can cause the LTSSM to go into the recovery state when exiting from L0s. 0xff (MAX_VAL): The maximum number of FTS ordered-sets that a component can request is 255. Value After Reset: 0xd2

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ACK_FREQ Ack Frequency. The controller accumulates the number of pending ACKs specified here (up to 255) before scheduling an ACK DLLP. 0: Indicates that this Ack Frequency Counter feature is turned off. The controller generates a low-priority ACK request for every TLP that it receives. The controller waits until the ACK Latency Timer expires, then converts the current low-priority ACK request to a high-priority ACK request and schedules the DLLP for transmission to the remote link partner. 1-255: Indicates that the controller will schedule a high-priority ACK after receiving this number of TLPs. It might schedule the ACK before receiving this number of TLPs if the ACK Latency Timer expires, but never later. For a typical system, you do not have to modify the default setting. For more details, see "ACK/NAK Scheduling" in the Databook. Note: This register field is sticky. Values: 0x0 (MIN_VAL): The value '0' indicates that this Ack Frequency Counter feature is turned off. 0xff (MAX_VAL): Any value between 1 and 255 indicates that the controller will schedule a high-priority ACK after receiving the specified number of TLPs. Value After Reset: 0x0

DSP_PCIE_PL_PORT_LINK_CTRL_OFF

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	TRANSMIT_LANE_REVERSALE_ENABLE TRANSMIT_LANE_REVERSALE_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
26	RW	0x0	EXTENDED_SYNCH EXTENDED_SYNCH is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
25	RW	0x0	CORRUPT_LCRC_ENABLE CORRUPT_LCRC_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
24	RW	0x0	BEACON_ENABLE BEACON_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
23:22	RO	0x0	reserved
21:16	RW	0x03	LINK_CAPABLE Link Mode Enable. Sets the number of lanes in the link that you want to connect to the link partner. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Predetermined Number of Lanes" field of the "Link Width and Speed Change Control Register". For more information, see "How to Tie Off Unused Lanes". For information on upsizing and downsizing the link width, see "Link Establishment". Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (X1): x1 0x3 (X2): x2 0x7 (X4): x4 0xf (X8): x8 0x1f (X16): x16 0x3f (X32): x32 (not supported) Value After Reset: 0x7 Testable: unconstrained
15:12	RO	0x0	reserved
11:8	RW	0x1	LINK_RATE LINK_RATE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
7	RW	0x0	FAST_LINK_MODE Fast Link Mode. Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation. Forces the LTSSM training (link initialization) to use shorter time-outs and to link up faster. The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. Fast Link Mode can also be activated by setting the diag_ctrl_bus[2] pin to '1'. For more details, see the "Fast Link Simulation Mode" section in the "Integrating the Controller with the PHY or Application RTL or Verification IP" chapter of the User Guide. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
6	RW	0x0	LINK_DISABLE LINK_DISABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
5	RW	0x1	DLL_LINK_EN DLL Link Enable. Note: This register field is sticky. Values: 0x1 (ENABLE): Enables link initialization. 0x0 (DISABLE): The controller does not transmit InitFC DLLPs and does not establish a link. Value After Reset: 0x1
4	RO	0x0	reserved
3	RW	0x0	RESET_ASSERT Reset Assert. Triggers a recovery and forces the LTSSM to the hot reset state (downstream port only). Note: This register field is sticky. Values: 0x1 (SET): Set 0x0 (CLEAR): Clear Value After Reset: 0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	LOOPBACK_ENABLE Loopback Enable. Turns on loopback. For more details, see "Loopback" in the Databook. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
1	RW	0x0	SCRAMBLE_DISABLE Scramble Disable. Turns off data scrambling. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
0	W1C	0x0	VENDOR_SPECIFIC_DLLP_REQ Vendor Specific DLLP Request. Reading from this self-clearing register field always returns a '0'. Values: 0x1 (SET): When software writes a '1' to this bit, the controller transmits the DLLP contained in the VENDOR_SPEC_DLLP field of VENDOR_SPEC_DLLP_OFF 0x0 (CLEAR): This is a self clearing register Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_LANE_SKEW_OFF
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	DISABLE_LANE_TO_LANE_DESKEW Disable Lane-to-Lane Deskew. Causes the controller to disable the internal Lane-to-Lane deskew logic. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
30:27	RW	0x1	IMPLEMENT_NUM_LANES Implementation-specific Number of Lanes. Set the implementation-specific number of lanes. The number of lanes to be used when in Loopback Master. The number of lanes programmed must be equal to or less than the valid number of lanes set in LINK_CAPABLE field. You must configure this field before initiating Loopback by writing in the LOOPBACK_ENABLE field. The controller will transition from Loopback.Entry to Loopback.Active after receiving two consecutive TS1 Ordered Sets with the Loopback bit asserted on the implementation specific number of lanes configured in this field. Note: This register field is sticky. Values: 0x0 (_1_LANE): 1 lane 0x1 (_2_LANE): 2 lanes 0x3 (_4_LANE): 4 lanes 0x7 (_8_LANE): 8 lanes 0xf (_16_LANE): 16 lanes Value After Reset: 0x3
26	RW	0x0	ELASTIC_BUFFER_MODE Selects Elasticity Buffer operating mode: Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (HALF_FULL): Nominal Half Full Buffer mode 0x1 (EMPTY): Nominal Empty Buffer Mode Value After Reset: 0x1

Bit	Attr	Reset Value	Description
25	RW	0x0	ACK_NAK_DISABLE Ack/Nak Disable. Prevents the controller from sending ACK and NAK DLLPs. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
24	RW	0x0	FLOW_CTRL_DISABLE Flow Control Disable. Prevents the controller from sending FC DLLPs. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
23:0	RW	0x000000	INSERT_LANE_SKEW INSERT_LANE_SKEW is an internally reserved field. Do not use. Note: This register field is sticky. Values: 0x0 (MIN): Zero value 0xff (MAX): Max value Value After Reset: 0x0

DSP_PCIE_PL_TIMER_CTRL_MAX_FUNC_NUM_OFF

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x0	FAST_LINK_SCALING_FACTOR Fast Link Timer Scaling Factor. Sets the scaling factor of LTSSM timer when FAST_LINK_MODE field in PORT_LINK_CTRL_OFF is set to '1'. Default is set by the hidden configuration parameter DEFAULT_FAST_LINK_SCALING_FACTOR which defaults to '0'. Note: This register field is sticky. Values: 0x0 (SF_1024): Scaling Factor is 1024 (1ms is 1us). When the LTSSM is in Config or L12 Entry State, 1ms timer is 2us, 2ms timer is 4us and 3ms timer is 6us. 0x1 (SF_256): Scaling Factor is 256 (1ms is 4us) 0x2 (SF_64): Scaling Factor is 64 (1ms is 16us) 0x3 (SF_16): Scaling Factor is 16 (1ms is 64us) Value After Reset: 0x2

Bit	Attr	Reset Value	Description
28:24	RW	0x00	UPDATE_FREQ_TIMER UPDATE_FREQ_TIMER is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
23:19	RW	0x00	TIMER_MOD_ACK_NAK Ack Latency Timer Modifier. Increases the timer value for the Ack latency timer in increments of 64 clock cycles. A value of '0' represents no modification to the timer value. For more details, see the ROUND_TRIP_LATENCY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. Note: This register field is sticky. Value After Reset: 0x0
18:14	RW	0x00	TIMER_MOD_REPLAY_TIMER Replay Timer Limit Modifier. Increases the time-out value for the replay timer in increments of 64 clock cycles at Gen1 or Gen2 speed, and in increments of 256 clock cycles at Gen3 speed. A value of '0' represents no modification to the timer limit. For more details, see the REPLAY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. At Gen3 speed, the controller automatically changes the value of this field to DEFAULT_GEN3_REPLAY_ADJ. Note: This register field is sticky. Value After Reset: 0xa Testable: writeAsRead Reset Mask: 0x0 Volatile: true
13:8	RO	0x00	reserved
7:0	RW	0x00	MAX_FUNC_NUM Maximum function number that can be used in a request. Configuration requests targeted at function numbers above this value are returned with UR (unsupported request). Note: This register field is sticky. Values: 0x0 (MIN): Zero value 0xff (MAX): Max value Value After Reset: 0x0

DSP_PCIE_PL_SYMBOL_TIMER_FILTER_1_OFF
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RW	0x0	CX_FLT_MASK_RC_CFG_DISCARD CX_FLT_MASK_RC_CFG_DISCARD 0: For RADM RC filter to not allow CFG transaction being received 1: For RADM RC filter to allow CFG transaction being received
30	RW	0x0	CX_FLT_MASK_RC_IO_DISCARD CX_FLT_MASK_RC_IO_DISCARD 0: For RADM RC filter to not allow IO transaction being received 1: For RADM RC filter to allow IO transaction being received
29	RW	0x0	CX_FLT_MASK_MSG_DROP CX_FLT_MASK_MSG_DROP 0: Drop MSG TLP (except for Vendor MSG). Send decoded message on the SII. 1: Do not Drop MSG (except for Vendor MSG). Send message TLPs to your application on TRGT1 and send decoded message on the SII. The default for this bit is the inverse of FLT_DROP_MSG. That is, if FLT_DROP_MSG =1, then the default of this bit is '0' (drop message TLPs). This bit only controls message TLPs other than Vendor MSGs. Vendor MSGs are controlled by Filter Mask Register 2, bits [1:0]. The controller never passes ATS Invalidate messages to the SII interface regardless of this filter rule setting. The controller passes all ATS Invalidate messages to TRGT1 (or AXI bridge master), as they are too big for the SII.
28	RW	0x0	CX_FLT_MASK_CPL_ECRC_DISCARD CX_FLT_MASK_CPL_ECRC_DISCARD Only used when completion queue is advertised with infinite credits and is in store-and-forward mode. 0: Discard completions with ECRC errors 1: Allow completions with ECRC errors to be passed up Reserved field for SW.
27	RW	0x0	CX_FLT_MASK_ECRC_DISCARD CX_FLT_MASK_ECRC_DISCARD 0: Discard TLPs with ECRC errors 1: Allow TLPs with ECRC errors to be passed up
26	RW	0x0	CX_FLT_MASK_CPL_LEN_MATCH CX_FLT_MASK_CPL_LEN_MATCH 0: Enforce length match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err 1: Mask length match for completions
25	RW	0x0	CX_FLT_MASK_CPL_ATTR_MATCH CX_FLT_MASK_CPL_ATTR_MATCH 0: Enforce attribute match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask attribute match for completions

Bit	Attr	Reset Value	Description
24	RW	0x0	CX_FLT_MASK_CPL_TC_MATCH CX_FLT_MASK_CPL_TC_MATCH 0: Enforce Traffic Class match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Traffic Class match for completions
23	RW	0x0	CX_FLT_MASK_CPL_FUNC_MATCH CX_FLT_MASK_CPL_FUNC_MATCH 0: Enforce function match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask function match for completions
22	RW	0x0	CX_FLT_MASK_CPL_REQID_MATCH CX_FLT_MASK_CPL_REQID_MATCH 0: Enforce Req. Id match for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Req. Id match for completions
21	RW	0x0	CX_FLT_MASK_CPL_TAGERR_MATCH CX_FLT_MASK_CPL_TAGERR_MATCH 0: Enforce Tag Error Rules for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Tag Error Rules for completions
20	RW	0x0	CX_FLT_MASK_LOCKED_RD_AS_UR CX_FLT_MASK_LOCKED_RD_AS_UR 0: Treat locked Read TLPs as UR for EP; Supported for RC 1: Treat locked Read TLPs as Supported for EP; UR for RC
19	RW	0x0	CX_FLT_MASK_CFG_TYPE1_REQ_AS_UR CX_FLT_MASK_CFG_TYPE1_REQ_AS_UR 0: Treat CFG type1 TLPs as UR for EP; Supported for RC 1: Treat CFG type1 TLPs as Supported for EP; UR for RC When CX_SRIOV_ENABLE is set then this bit is set to allow the filter to process Type 1 Config requests if the EP consumes more than one bus number.
18	RW	0x0	CX_FLT_MASK_UR_OUTSIDE_BAR CX_FLT_MASK_UR_OUTSIDE_BAR 0: Treat out-of-bar TLPs as UR 1: Do not treat out-of-bar TLPs as UR
17	RW	0x0	CX_FLT_MASK_UR_POIS CX_FLT_MASK_UR_POIS 0: Treat poisoned request TLPs as UR 1: Do not treat poisoned request TLPs as UR The native controller always passes poisoned completions to your application except when you are using the DMA read channel.

Bit	Attr	Reset Value	Description
16	RW	0x0	CX_FLT_MASK_UR_FUNC_MISMATCH CX_FLT_MASK_UR_FUNC_MISMATCH 0: Treat Function MisMatched TLPs as UR 1: Do not treat Function MisMatched TLPs as UR Note: This register field is sticky. Value After Reset: 0x0
15	RW	0x0	DISABLE_FC_WD_TIMER Disable FC Watchdog Timer. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
14:11	RW	0x0	EIDLE_TIMER EIDLE_TIMER is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
10:0	RW	0x140	SKP_INT_VAL SKP Interval Value. The number of symbol times to wait between transmitting SKP ordered sets. The controller waits the number of symbol times in this register plus 1, between transmitting SKP ordered sets. Your application must program this register accordingly. For example, if 1536 were programmed into this register (in a 250 MHz controller), then the controller actually transmits SKP ordered sets once every 1537 symbol times. The value programmed to this register is actually clock ticks and not symbol times. In a 125 MHz controller, programming the value programmed to this register should be scaled down by a factor of 2 (because one clock tick =two symbol times in this case). Note: This value is not used at Gen3 speed; the skip interval is hardcoded to 370 blocks. Note: This register field is sticky. Value After Reset: 0x140

DSP_PCIE_PL_FILTER_MASK_2_OFF

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	CX_FLT_MASK_CPL_IN_LUT_CHECK CX_FLT_MASK_CPL_IN_LUT_CHECK 0: Disable masking of checking if the tag of CPL is registered in LUT 1: Enable masking of checking if the tag of CPL is registered in LUT
8	RW	0x0	CX_FLT_MASK_POIS_ERROR_REPORTING CX_FLT_MASK_POIS_ERROR_REPORTING 0: Disable masking of error reporting for Poisoned TLPs 1: Enable masking of error reporting for Poisoned TLPs
7	RW	0x0	CX_FLT_MASK_PRS_DROP CX_FLT_MASK_PRS_DROP 0: Allow PRS message to pass through 1: Drop PRS Messages silently This bit is ignored when the CX_FLT_MASK_MSG_DROP bit in the MASK_RADM_1 field of the SYMBOL_TIMER_FILTER_1_OFF register is set to '1'.
6	RW	0x0	CX_FLT_UNMASK_TD CX_FLT_UNMASK_TD 0: Disable unmask TD bit if CX_STRIP_ECRC_ENABLE 1: Enable unmask TD bit if CX_STRIP_ECRC_ENABLE
5	RW	0x0	CX_FLT_UNMASK_UR_POIS_TRGT0 CX_FLT_UNMASK_UR_POIS_TRGT0 0: Disable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination 1: Enable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination
4	RW	0x0	CX_FLT_MASK_LN_VENMSG1_DROP CX_FLT_MASK_LN_VENMSG1_DROP 0: Allow LN message to pass through 1: Drop LN Messages silently
3	RW	0x0	CX_FLT_MASK_HANDLE_FLUSH CX_FLT_MASK_HANDLE_FLUSH 0: Disable controller Filter to handle flush request 1: Enable controller Filter to handle flush request
2	RW	0x0	CX_FLT_MASK_DABORT_4UCPL CX_FLT_MASK_DABORT_4UCPL 0: Enable DLLP abort for unexpected completion 1: Do not enable DLLP abort for unexpected completion
1	RW	0x0	CX_FLT_MASK_VENMSG1_DROP CX_FLT_MASK_VENMSG1_DROP 0: Vendor MSG Type 1 dropped silently 1: Vendor MSG Type 1 not dropped

Bit	Attr	Reset Value	Description
0	RW	0x0	CX_FLT_MASK_VENMSG0_DROP CX_FLT_MASK_VENMSG0_DROP 0: Vendor MSG Type 0 dropped with UR error reporting 1: Vendor MSG Type 0 not dropped

DSP_PCIE_PL_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	OB_RD_SPLIT_BURST_EN Enable AMBA Multiple Outbound Decomposed NP SubRequests. You should not clear this register unless your application master is requesting an amount of read data greater than Max_Read_Request_Size, and the remote device (or switch) is reordering completions that have different tags. For more details, see "AXI Bridge Ordering" in the AXI chapter of the Databook. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (DISABLE): This bit when set to '0' disables the possibility of having multiple outstanding non-posted requests that were derived from decomposition of an outbound AMBA request. 0x1 (ENABLE): Enable Value After Reset: 0x1

DSP_PCIE_PL_PL_DEBUG0_OFF
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DEB_REG_0 The value on cxpl_debug_info[31:0]. Values: 0x0 (ZERO): Zero value. 0xffffffff (MAX): Max value. Value After Reset: 0x0 Testable: untestable Reset Mask: 0x0 Volatile: true

DSP_PCIE_PL_PL_DEBUG1_OFF
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DEB_REG_1 The value on cxpl_debug_info[63:32]. Values: 0x0 (ZERO): Zero value. 0xffffffff (MAX): Max value. Value After Reset: 0x0 Testable: untestable Reset Mask: 0x0 Volatile: true

DSP_PCIE_PL_TX_P_FC_CREDIT_STATUS_OFF
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_P_HEADER_FC_CREDIT Transmit Posted Header FC Credits. The posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_P_DATA_FC_CREDIT Transmit Posted Data FC Credits. The posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

DSP_PCIE_PL_TX_NP_FC_CREDIT_STATUS_OFF

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_NP_HEADER_FC_CREDIT Transmit Non-Posted Header FC Credits. The non-posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_NP_DATA_FC_CREDIT Transmit Non-Posted Data FC Credits. The non-posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_TX_CPL_FC_CREDIT_STATUS_OFF

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_CPL_HEADER_FC_CREDIT Transmit Completion Header FC Credits. The Completion Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_CPL_DATA_FC_CREDIT Transmit Completion Data FC Credits. The Completion Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_QUEUE_STATUS_OFF
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	TIMER_MOD_FLOW_CONTROL_EN FC Latency Timer Override Enable. Note: This register field is sticky. Values: 0x1 (SET): When this bit is set, the value from the "FC Latency Timer Override Value" field in this register will override the FC latency timer value that the controller calculates according to the PCIe specification. 0x0 (CLEAR): Clear Value After Reset: 0x0
30:29	RO	0x0	reserved
28:16	RW	0x0000	TIMER_MOD_FLOW_CONTROL FC Latency Timer Override Value. When you set the "FC Latency Timer Override Enable" in this register, the value in this field will override the FC latency timer value that the controller calculates according to the PCIe specification. For more details, see "Flow Control" in the Databook. Note: This register field is sticky. Value After Reset: 0x0
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RO	0x0	RX_SERIALIZATION_Q_NON_EMPTY Receive Serialization Queue Not Empty. Values: 0x1 (SET): Indicates there is data in the serialization queue. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true
12:4	RO	0x000	reserved
3	W1C	0x0	RX_QUEUE_OVERFLOW Receive Credit Queue Overflow. Values: 0x1 (SET): Indicates insufficient buffer space available to write to the P/NP/CPL credit queue. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RO	0x0	RX_QUEUE_NON_EMPTY Receive Credit Queue Not Empty. Values: 0x1 (SET): Indicates there is data in one or more of the receive buffers. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	RO	0x0	TX_RETRY_BUFFER_NE Transmit Retry Buffer Not Empty. Values: 0x1 (SET): Indicates that there is data in the transmit retry buffer. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RO	0x0	RX_TLP_FC_CREDIT_NON_RETURN Received TLP FC Credits Not Returned. Values: 0x1 (SET): Indicates that the controller has received a TLP but has not yet sent an UpdateFC DLLP indicating that the credits for that TLP have been restored by the receiver at the other end of the link. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_VC_TX_ARBI_1_OFF
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	WRR_WEIGHT_VC_3 WRR Weight for VC3. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0
23:16	RW	0x00	WRR_WEIGHT_VC_2 WRR Weight for VC2. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0
15:8	RO	0x00	WRR_WEIGHT_VC_1 WRR Weight for VC1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0
7:0	RO	0x0f	WRR_WEIGHT_VC_0 WRR Weight for VC0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0xf

DSP_PCIE_PL_VC_TX_ARBI_2_OFF
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	WRR_WEIGHT_VC_7 WRR Weight for VC7. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0
23:16	RW	0x00	WRR_WEIGHT_VC_6 WRR Weight for VC6. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0
15:8	RW	0x00	WRR_WEIGHT_VC_5 WRR Weight for VC5. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0
7:0	RW	0x00	WRR_WEIGHT_VC_4 WRR Weight for VC4. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Value After Reset: 0x0

DSP_PCIE_PL_VC0_P_RX_Q_CTRL_OFF
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RW	0x0	VC_ORDERING_RX_Q VC Ordering for Receive Queues. Determines the VC ordering rule for the receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky. Values: 0x1 (STRICT_ORDERING): Strict ordering, higher numbered VCs have higher priority 0x0 (ROUND_ROBIN): Round robin Value After Reset: 0x0

Bit	Attr	Reset Value	Description
30	RW	0x1	TLP_TYPE_ORDERING_VC0 TLP Type Ordering for VC0. Determines the TLP type ordering rule for VC0 receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky. Values: 0x1 (PCIE_ORDERING_RULE): PCIe ordering rules (recommended) 0x0 (STRICT_ORDERING): Strict ordering: posted, completion, then non-posted Value After Reset: 0x1
29:28	RO	0x0	reserved
27:26	RW	0x1	VC0_P_DATA_SCALE VC0 Scale Posted Data Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
25:24	RW	0x1	VC0_P_HDR_SCALE VC0 Scale Posted Header Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
23:22	RO	0x0	reserved
21	RW	0x1	VC0_P_TLP_Q_MODE Reserved. Note: This register field is sticky. Value After Reset: 0x1
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:12	RO	0x27	VC0_P_HEADER_CREDIT VC0 Posted Header Credits. The number of initial posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xff (MAX_VAL): Max value Value After Reset: 0x5c
11:0	RO	0x110	VC0_P_DATA_CREDIT VC0 Posted Data Credits. The number of initial posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xfff (MAX_VAL): Max value Value After Reset: 0x110

DSP_PCIE_PL_VC0_NP_RX_Q_CTRL_OFF

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x1	VC0_NP_DATA_SCALE VC0 Scale Non-Posted Data Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1

Bit	Attr	Reset Value	Description
25:24	RW	0x1	VC0_NP_HDR_SCALE VC0 Scale Non-Posted Header Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
23	RO	0x0	reserved
22:21	RW	0x0	VC0_NP_TLP_Q_MODE Reserved. Note: This register field is sticky. Value After Reset: 0x1
20	RO	0x0	reserved
19:12	RO	0x5c	VC0_NP_HEADER_CREDIT VC0 Non-Posted Header Credits. The number of initial non-posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xff (MAX_VAL): Max value Value After Reset: 0x5c
11:0	RO	0x017	VC0_NP_DATA_CREDIT VC0 Non-Posted Data Credits. The number of initial non-posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xfff (MAX_VAL): Max value Value After Reset: 0x17

DSP_PCIE_PL_VC0_CPL_RX_Q_CTRL_OFF
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x1	VC0_CPL_DATA_SCALE VC0 Scale CPL Data Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
25:24	RW	0x1	VC0_CPL_HDR_SCALE VC0 Scale CPL Header Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
23	RO	0x0	reserved
22:21	RW	0x0	VC0_CPL_TLP_Q_MODE Reserved. Note: This register field is sticky. Value After Reset: 0x1
20	RO	0x0	reserved
19:12	RO	0x00	VC0_CPL_HEADER_CREDIT VC0 Completion Header Credits. The number of initial Completion header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xff (MAX_VAL): Max value Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11:0	RO	0x000	VC0_CPL_DATA_CREDIT VC0 Completion Data Credits. The number of initial Completion data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xfff (MAX_VAL): Max value Value After Reset: 0x0

DSP_PCIE_PL_GEN2_CTRL_OFF

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	FORCE_LANE_FLIP Enable to force the LANE_UNDER_TEST physical lane flips to logical lane 0. All the other physical lanes are turned off. The LINK_CAPABLE register must be set to 1 and only x1 link can be formed if the FORCE_LANE_FLIP register is set to 1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
29:25	RO	0x00	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	LANE_UNDER_TEST The Lane Under Test is the lane for Forced Lane Flip or for Loopback Eq. Only one lane is configured each time. The default of this field is the CX_DEFAULT_LANE_UNDER_TEST configuration parameter. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero 0x1 (MAX_VAL): CX_NL Value After Reset: 0x0
23	RW	0x0	SELECTABLE_DEEMPH_BIT_MUX The selectable deemphasis bit (Symbol 4 bit 6) of the transmitted TS2 Ordered Sets for DSP in Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP. Note: This register field is sticky. Values: 0x0 (FROM_LINK_CTRL_2_REG): The value from the Selectable De-emphasis field in the Link Control 2 register 0x1 (REQUESTED_BY_USP): The value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP Value After Reset: 0x0
22	RW	0x0	SELECT_DEEMPH_VAR_MUX The select_deemphasis variable for DSP on entry to Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by the Upstream Port in the eight consecutive TS1 Ordered Sets it received. Note: This register field is sticky. Values: 0x0 (REQUESTED_BY_USP): The value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP 0x1 (FROM_LINK_CTRL_2_REG): The value from the Selectable De-emphasis field in the Link Control 2 register Value After Reset: 0x0

Bit	Attr	Reset Value	Description
21	RW	0x0	GEN1_EI_INFERENCE Electrical Idle Inference Mode at Gen1 Rate. Programmable mode to determine inferred electrical idle (EI) in Recovery.Speed or Loopback.Active (as slave) state at Gen1 speed by looking for a '1' value on RxElecIdle instead of looking for a '0' on RxValid. If the PHY fails to deassert the RxValid signal in Recovery.Speed or Loopback.Active (because of corrupted EIOS for example), then EI cannot be inferred successfully in the controller by just detecting the condition RxValid=0. Note: This register field is sticky. Values: 0x0 (RXELECIDLE_TO_INFER): Use RxElecIdle signal to infer Electrical Idle 0x1 (RXVALID_TO_INFER): Use RxValid signal to infer Electrical Idle Value After Reset: 0x0
20	RW	0x0	SEL_DEEMPHASIS Used to set the de-emphasis level for upstream ports. This bit selects the level of de-emphasis the link operates at. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (N_6DB): -6 dB 0x1 (N_3_5DB): -3.5 dB Value After Reset: 0x0
19	RW	0x0	CONFIG_TX_COMP_RX Config Tx Compliance Receive Bit. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (SET): When set to 1, signals LTSSM to transmit TS ordered sets with the compliance receive bit assert (equal to '1'). 0x0 (CLEAR): Clear Value After Reset: 0x0

Bit	Attr	Reset Value	Description
18	RW	0x0	CONFIG_PHY_TX_CHANGE Config PHY Tx Swing. Controls the PHY transmitter voltage swing level. The controller drives the mac_phy_txswing output from this register bit field. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (FULL_SWING): Full Swing 0x1 (LOW_SWING): Low Swing Value After Reset: 0x0
17	RW	0x0	DIRECT_SPEED_CHANGE Directed Speed Change. When the speed change occurs, the controller will clear the contents of this field; and a read to this field by your software will return a '0'. To manually initiate the speed change: Write to LINK_CONTROL2_LINK_STATUS2_REG.PCIE_CAP_TARGET_LINK_SPEED in the local device Deassert this field Assert this field If you set the default of this field using the DEFAULT_GEN2_SPEED_CHANGE configuration parameter to '1', then the speed change is initiated automatically after link up, and the controller clears the contents of this field. If you want to prevent this automatic speed change, then write a lower speed value to the Target Link Speed field of the Link Control 2 register (LINK_CONTROL2_LINK_STATUS2_OFF.PCIE_CAP_TARGET_LINK_SPEED) through the DBI before link up. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x1 (SET): Writing '1' to this field instructs the LTSSM to initiate a speed change to Gen2 or Gen3 after the link is initialized at Gen1 speed. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
16	RW	0x1	AUTO_LANE_FLIP_CTRL_EN Enable Auto flipping of the lanes. You must set the CX_AUTO_LANE_FLIP_CTRL_EN configuration parameter to include the hardware for this feature in the controller. For more details, see the 'Lane Reversal' appendix in the Databook. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x1 Testable: unconstrained
15:13	RW	0x0	PRE_DET_LANE Predetermined Lane for Auto Flip. This field defines which physical lane is connected to logical Lane0 by the flip operation performed in Detect. This field is used to restrict the receiver detect procedure to a particular lane when the default detect and polling procedure performed on all lanes cannot be successful. A notable example of when it is useful to program this field to a value different from the default, is when a lane is asymmetrically broken, that is, it is detected in Detect LTSSM state but it cannot exit Electrical Idle in Polling LTSSM state. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (LANE0): Connect logical Lane0 to physical lane 0 or CX_NL-1 or CX_NL/2-1 or CX_NL/4-1 or CX_NL/8-1, depending on which lane is detected 0x1 (LANE1): Connect logical Lane0 to physical lane 1 0x2 (LANE3): Connect logical Lane0 to physical lane 3 0x3 (LANE7): connect logical lane0 to physical lane 7 0x4 (LANE15): Connect logical Lane0 to physical lane 15 Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
12:8	RW	0x02	NUM_OF_LANES Predetermined Number of Lanes. Defines the number of lanes which are connected and not bad. Used to limit the effective link width to ignore 'broken" or "unused" lanes that detect a receiver. Indicates the number of lanes to check for exit from Electrical Idle in Polling.Active and L2.Idle. It is possible that the LTSSM might detect a receiver on a bad or broken lane during the Detect Substate. However, it is also possible that such a lane might also fail to exit Electrical Idle and therefore prevent a valid link from being configured. This value is referred to as the "Predetermined Number of Lanes" in section 4.2.6.2.1 of the PCI Express Base Specification. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Link Mode Enable" field of PORT_LINK_CTRL_OFF. The value in this register is normally the same as the encoded value in PORT_LINK_CTRL_OFF. If you find that one of your used lanes is bad then you must reduce the value in this register. For more information, see "How to Tie Off Unused Lanes" in the Databook. For information on upsizing and downsizing the link width, see "Link Establishment" in the Databook. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (_1_LANE): 1 lane 0x2 (_2_LANE): 2 lanes 0x3 (_3_LANE): 3 lanes Value After Reset: 0x4 Testable: unconstrained
7:0	RW	0xd2	FAST_TRAINING_SEQ Sets the Number of Fast Training Sequences (N_FTS) that the controller advertises as its N_FTS during Gen2 or Gen3 link training. This value is used to inform the link partner about the PHY's ability to recover synchronization after a low power state. The number should be provided by the PHY vendor. Do not set N_FTS to zero; doing so can cause the LTSSM to go into the recovery state when exiting from L0s. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0xd2

DSP_PCIE_PL_PHY_STATUS_OFF
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PHY_STATUS PHY Status. Data received directly from the phy_cfg_status bus. These is a GPIO register reflecting the values on the static phy_cfg_status input signals. The usage is left completely to the user and does not in any way influence controller functionality. You can use it for any static sideband status signalling requirements that you have for your PHY. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

DSP_PCIE_PL_PHY_CONTROL_OFF
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000001	PHY_CONTROL PHY Control. Data sent directly to the cfg_phy_control bus. This is a GPIO register driving the values on the static cfg_phy_control output signals, and does not in any way influence controller functionality. It can be used for any static sideband control signaling requirements that you have for your PHY. Usage of this register and the associated GPIO bus is RESERVED when the controller is connected to a Synopsys PHY. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x1

DSP_PCIE_PL_TRGT_MAP_CTRL_OFF
Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	TARGET_MAP_INDEX The number of the PF Function on which the Target Values are set. This register does not respect the Byte Enable setting, any write will affect all register bits. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:7	RO	0x000	reserved
6	RW	0x1	TARGET_MAP_ROM Target Value for the ROM page of the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
5:0	RW	0x07	TARGET_MAP_PF Target Values for each BAR on the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits. Value After Reset: 0x2f Testable: writeAsRead Volatile: true

DSP_PCIE_PL_CLOCK_GATING_CTRL_OFF

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x1	AXI_CLK_GATING_EN AXI Clock Gating Enable. This register enables the AXI Bridge to autonomously enable and disable the AXI Master clock, the AXI Slave clock and the AXI DBI slave clock. The DWC_pcie_clk_rst.v module provides the gated clock, mstr_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, mstr_aclk_active, is asserted. For the AXI Slave this module provides the gated clock, slv_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, slv_aclk_active, is asserted. If the AXI DBI Slave is enabled (DBI_4SLAVE_POPULATED=1) the module provides the gated clock, dbi_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, dbi_aclk_active, is asserted. The controller de-asserts the clock enable signals when the respective AXI Master/Slave interfaces are idle. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable (default) Value After Reset: 0x1
0	RW	0x1	RADM_CLK_GATING_EN RADM Clock Gating Enable. This register, if set, enables the RADM to autonomously enable and disable its clock. The DWC_pcie_clk_rst.v module provides the gated clock, radm_clk_g, to the RADM and is enabled when the controllers clock enable signal, en_radm_clk_g, is asserted. The RADM clock is a gated version of the controller clock, core_clk. The controller de-asserts en_radm_clk_g when there is no Rx traffic, Rx queues and pre/post-queue pipelines are empty, RADM completion LUT is empty, and there are no FLR actions pending. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable (default) Value After Reset: 0x1

DSP_PCIE_PL_GEN3_RELATED_OFF

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	GEN3_EQ_INVREQ_EVAL_DIFF_DISABLE Eq InvalidRequest and RxEqEval Different Time Assertion Disable. Disable the assertion of Eq InvalidRequest and RxEqEval at different time. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
22:19	RO	0x0	reserved
18	RW	0x0	GEN3_DC_BALANCE_DISABLE DC Balance Disable. Disable DC Balance feature. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0
17	RW	0x0	GEN3_DLLP_XMT_DELAY_DISABLE DLLP Transmission Delay Disable. Disable delay transmission of DLLPs before equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
16	RW	0x0	GEN3_EQUALIZATION_DISABLE Equalization Disable. Disable equalization feature. This bit cannot be changed once the LTSSM starts link training. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	RXEQ_RGRDLESS_RXTS When set to '1', the controller as Gen3 EQ master asserts RxEqEval to instruct the PHY to do Rx adaptation and evaluation after a 500ns timeout from a new preset request. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: Wire: No access. Dbi: see description Note: This register field is sticky. Values: 0x0 (ASSERT_1US): mac_phy_rxeqeval asserts after 1us and 2 TS1 received from remote partner. 0x1 (ASSERT_500NS): mac_phy_rxeqeval asserts after 500ns regardless of TS's received or not. Value After Reset: 0x1 Testable: writeAsRead
12	RW	0x0	RXEQ_PH01_EN Rx Equalization Phase 0/Phase 1 Hold Enable. When this bit is set the upstream port holds phase 0 (the downstream port holds phase 1) for 10ms. Holding phase 0 or phase 1 can be used to allow sufficient time for Rx Equalization to be performed by the PHY. This bit is used during Virtex-7 Gen3 equalization. The programmable bits [RXEQ_PH01_EN, EQ_PHASE_2_3] can be used to obtain the following variations of the equalization procedure: Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: Wire: No access. Dbi: see description Note: This register field is sticky. Values: 0x0 (TX_EQ_23): Tx equalization only in phase 2/3 0x1 (NO_TX_EQ_NO_RX_EQ): No Tx equalization Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
11	RW	0x0	EQ_REDO Equalization Redo Disable. Disable autonomous mechanism for requesting to redo the equalization process. The received presets or coefficients mismatch in Recovery.RcvrLock after Recovery EQ phases causes the EQ redo requests. If the EQ redo is infinite or you do not want eq requests and redo, setting this bit to 1 will stop the EQ requests and EQ redo so that the link can go ahead to L0 state for packet trasmissions. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
10	RW	0x0	EQ_EIEOS_CNT Equalization EIEOS Count Reset Disable. Disable requesting reset of EIEOS count during equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Values: 0x1 (DISABLE): Disable Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
9	RW	0x0	EQ_PHASE_2_3 Equalization Phase 2 and Phase 3 Disable. This applies to downstream ports only. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: Wire: No access. Dbi: see description Note: This register field is sticky. Values: 0x1 (TX_EQ_23_RX_EQ_PH01): No Rx equalization 0x0 (NO_TX_EQ_RX_EQ_PH01): Rx equalization in phase 0/1 Value After Reset: 0x0 Testable: writeAsRead
8	RW	0x0	DISABLE_SCRAMBLER_GEN_3 Disable Scrambler for Gen3 and Gen4 Data Rate. The Gen3 and Gen4 scrambler/descrambler within the controller needs to be disabled when the scrambling function is implemented outside of the controller (for example within the PHY). Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0
7:2	RO	0x00	reserved
1	RW	0x0	NO_SEED_VALUE_CHANGE If this bit is set to 1, the seed value of LFSR for scrambler at Gen3 rate does not change after LinkUp = 1. This bit takes effect only when CX_AUTO_LANE_FLIP_CTRL_EN is supported. This feature requires both sides of the link support it. Note: this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky. Values: 0x1 (NO_CHANGE): Not Change Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	GEN3_ZRXDC_NONCOMPL Gen3 Receiver Impedance ZRX-DC Not Compliant. Receivers that operate at 8.0 GT/s with an impedance other than the range defined by the ZRX-DC parameter for 2.5 GT/s (40-60 Ohms) must meet additional behavior requirements in the following LTSSM states: Polling, Rx_L0s, L1, L2, and Disabled. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky. Values: 0x0 (RCVR_COMPLIES): The receiver complies with the ZRX-DC parameter for 2.5 GT/s when operating at 8 GT/s or higher. 0x1 (RCVR_NOT_COMPLIES): The receiver does not comply with the ZRX-DC parameter for 2.5 GT/s when operating at 8 GT/s or higher. Value After Reset: 0x1

DSP_PCIE_PL_GEN3_EQ_CONTROL_OFF
Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x1	GEN3_REQ_SEND_CONSEC_EIEOS_FOR_PSET_MAP Request controller to send back-to-back EIEOS in Recovery.RcvrLock state until presets to coefficients mapping is complete. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky. Values: 0x0 (DO_NOT_REQ): Do not request 0x1 (REQ): Request Value After Reset: 0x1 Testable: writeAsRead Volatile: true
25	RW	0x0	GEN3_EQ_PSET_REQ_AS_COEF GEN3_EQ_PSET_REQ_AS_COEF is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
24	RW	0x0	GEN3_EQ_FOM_INC_INITIAL_EVAL Include Initial FOM. Include or not the FOM feedback from the initial preset evaluation performed in the EQ Master, when finding the highest FOM among all preset evaluations. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (DO_NOT_INCLUDE): Do not include 0x1 (INCLUDE): Include Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:8	RW	0x059f	GEN3_EQ_PSET_REQ_VEC Preset Request Vector. Requesting of Presets during the initial part of the EQ Master Phase. Encoding scheme is as follows: Bit [15:0] =0x0: No preset is requested and evaluated in EQ Master Phase. Bit [i] =1: "Preset=i" is requested and evaluated in EQ Master Phase. 0000000000000000: No preset be requested and evaluated in EQ Master Phase 000000xxxxxxxxx1: Preset 0 is requested and evaluated in EQ Master Phase 000000xxxxxxxx1x: Preset 1 is requested and evaluated in EQ Master Phase 000000xxxxxxx1xx: Preset 2 is requested and evaluated in EQ Master Phase 000000xxxxxx1xxx: Preset 3 is requested and evaluated in EQ Master Phase 000000xxxxx1xxxx: Preset 4 is requested and evaluated in EQ Master Phase 000000xxxx1xxxxx: Preset 5 is requested and evaluated in EQ Master Phase 000000xxx1xxxxxx: Preset 6 is requested and evaluated in EQ Master Phase 000000xx1xxxxxxx: Preset 7 is requested and evaluated in EQ Master Phase 000000x1xxxxxxxx: Preset 8 is requested and evaluated in EQ Master Phase 00000x1xxxxxxxxx: Preset 9 is requested and evaluated in EQ Master Phase 000001xxxxxxxxxx: Preset 10 is requested and evaluated in EQ Master Phase All other encodings: Reserved Note: You must contact your PHY vendor to ensure 24 ms timeout does not occur in presets requests in EQ master phase, that is, you must set a proper value to the GEN3_EQ_PSET_REQ_VEC register so that the EQ tunning for Figure of Merit in the EQ master phase completes before 24 ms timeout. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x59f Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x1	GEN3_LOWER_RATE_EQ_REDO_ENABLE Support EQ redo and lower rate change. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky. Values: 0x0 (NO_SUP): Not supported 0x1 (SUP): Supported Value After Reset: 0x1 Testable: writeAsRead Volatile: true
5	RW	0x1	GEN3_EQ_EVAL_2MS_DISABLE Phase2_3 2 ms Timeout Disable. Determine behavior in Phase2 for USP (Phase3 if DSP) when the PHY does not respond within 2ms to the assertion of RxEqEval. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (ABORT_CURRENT_EVA): Abort the current evaluation, stop any attempt to modify the remote transmitter settings, Phase2 is terminated by the 24ms timeout 0x1 (IGNORE_2MS_TIMEOUT): Ignore the 2ms timeout and continue as normal. This is used to support PHYs that require more than 2ms to respond to the assertion of RxEqEval. Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
4	RW	0x0	GEN3_EQ_PHASE23_EXIT_MODE Behavior After 24 ms Timeout (when optimal settings are not found). For a USP: Determine next LTSSM state from Phase2 after 24ms Timeout 0: Recovery.Speed 1: Recovery.Equalization.Phase3 When optimal settings are not found then: Equalization Phase 2 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 Equalization Phase 2 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 Equalization Phase 2 Complete status bit is set in the "Link Status Register 2" For a DSP: Determine next LTSSM state from Phase3 after 24ms Timeout 0: Recovery.Speed 1: Recovery.Equalization.RcvrLock When optimal settings are not found then: Equalization Phase 3 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 Equalization Phase 3 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 Equalization Phase 3 Complete status bit is set in the "Link Status Register 2" Note: GEN3_EQ_PHASE23_EXIT_MODE = 1 affects Direction Change feed back mode. EQ requests for Figure Of Merit mode complete before 24 ms timeout. Please see GEN3_EQ_PSET_REQ_VEC Register for more. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (RCVRY_SPEED): Recovery.Speed 0x1 (RCVRY_EQ): USP: Recovery.Equalization.Phase3; DSP: Recovery.Equalization.RcvrLock Value After Reset: 0x1

Bit	Attr	Reset Value	Description
3:0	RW	0x1	GEN3_EQ_FB_MODE Feedback Mode. Other values are reserved. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is a shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (DIR_CHG): Direction Change 0x1 (FOM): Figure Of Merit Value After Reset: 0x1 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:14	RW	0x0	GEN3_EQ_FMDC_MAX_POST_CUSROR_DELTA Convergence Window Aperture for C+1. Post-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
13:10	RW	0x0	GEN3_EQ_FMDC_MAX_PRE_CUSROR_DELTA Convergence Window Aperture for C-1. Pre-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x0 Testable: unconstrained
9:5	RW	0x02	GEN3_EQ_FMDC_N_EVALS Convergence Window Depth. Number of consecutive evaluations considered in Phase 2/3 when determining if optimal coefficients have been found. Allowed range: 0,1,2,..16 up to a maximum of CX_GEN3_EQ_COEFQ_DEPTH. When set to 0, EQ Master is performed without sending any requests to the remote partner in Phase 2 for USP and Phase 3 for DSP. Therefore, the remote partner will not change its transmitter coefficients and will move to the next state. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x1f (MAX_VAL): Maximum of CX_GEN3_EQ_COEFQ_DEPTH Value After Reset: 0x2 Testable: unconstrained

Bit	Attr	Reset Value	Description
4:0	RW	0x00	GEN3_EQ_FMDC_T_MIN_PHASE23 Minimum Time (in ms) To Remain in EQ Master Phase. The LTSSM stays in EQ Master phase for at least this amount of time, before starting to check for convergence of the coefficients. Allowed values 0,1,...,24. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x18 (MAX_VAL): Max value Value After Reset: 0x0 Testable: unconstrained

DSP_PCIE_PL_ORDER_RULE_CTRL_OFF
Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CPL_PASS_P Completion Passing Posted Ordering Rule Control. Determines if CPL can pass halted P queue. Values: 0x0 (CPL_CAN_NOT_PASS): CPL can not pass P (recommended) 0x1 (CPL_CAN_PASS): CPL can pass P Value After Reset: 0x0
7:0	RW	0x00	NP_PASS_P Non-Posted Passing Posted Ordering Rule Control. Determines if NP can pass halted P queue. Values: 0x0 (NP_CAN_NOT_PASS): NP can not pass P (recommended). 0x1 (NP_CAN_PASS): NP can pass P Value After Reset: 0x0

DSP_PCIE_PL_PIPE_LOOPBACK_CONTROL_OFF
Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	PIPE_LOOPBACK PIPE Loopback Enable. Indicates RMMI Loopback if M-PCIe. Note: This register field is sticky. Value After Reset: 0x0
30:27	RO	0x0	reserved
26:24	RW	0x0	RXSTATUS_VALUE RXSTATUS_VALUE is an internally reserved field. Do not use. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
23:22	RO	0x0	reserved
21:16	RW	0x00	RXSTATUS_LANE RXSTATUS_LANE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
15:0	RW	0x000f	LPBK_RXVALID LPBK_RXVALID is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0xf

DSP_PCIE_PL_MISC_CONTROL_1_OFF
Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	PORT_LOGIC_WR_DISABLE Disable port logic register write from wire side. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
21	RW	0x0	P2P_ERR_RPT_CTRL Determines whether to enable Peer to Peer (P2P) error reporting. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable P2P error reporting 0x1 (ENABLE): Enable P2P error reporting Value After Reset: 0x0
20	RW	0x0	P2P_TRACK_CPL_TO_REG Determines whether to track completion of transmitted Non-Posted TLPs in P2P mode. Note: This register field is sticky. Values: 0x0 (DO_NOT_TRACk): Do not track completion 0x1 (TRACK): Track completion Value After Reset: 0x0
19:18	RW	0x0	TARGET_ABOVE_CONFIG_LIMIT_REG Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of this field. This field can have the following values: Note: This register field is sticky. Values: 0x1 (ELBI): ELBI 0x2 (TRGT1): TRGT1 Value After Reset: 0x1
17:8	RW	0x37f	CONFIG_LIMIT_REG Configuration requests are directed either to CDM or ELBI/RTRGT1 based on the value of this field. Configuration requests with an address less CONFIG_LIMIT_REG are directed to the CDM Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of TARGET_ABOVE_CONFIG_LIMIT_REG field. Your application must set a proper value for this field based on your extended configuration registers. For more details, see the "CDM/ELBI Register Space Access Through CFG Request" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Value After Reset: 0x37f

Bit	Attr	Reset Value	Description
7	RW	0x0	CFG_TLP_BYPASS_EN_REG Setting of this field defines how to decide the destination of Configuration requests. Note: When app_req_retry_en is asserted, the setting of this field is ignored. Note: This register field is sticky. Values: 0x1 (ONE): Configuration TLPs are routed according to the setting of TARGET_ABOVE_CONFIG_LIMIT_REG, regardless the value of CONFIG_LIMIT_REG. 0x0 (ZERO): Configuration TLPs are routed according to the setting of TARGET_ABOVE_CONFIG_LIMIT_REG, depending on the setting of CONFIG_LIMIT_REG. Refer to the definition of CONFIG_LIMIT_REG for details. Value After Reset: 0x0
6	RW	0x1	CPLQ_MNG_EN This field enables the Completion Queue Management feature. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x1
5	RW	0x0	ARI_DEVICE_NUMBER When ARI is enabled, this field enables use of the device ID. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
4	RW	0x0	DISABLE_AUTO_LTR_CLR_MSG Disable the autonomous generation of LTR clear message in upstream port. This field can have the following values: For more details, see "Latency Tolerance Reporting (LTR) Message Generation [EP Mode]" in "Message Generation" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (ALLOW): Allow the autonomous generation of LTR clear message. 0x1 (DISABLE): Disable the autonomous generation of LTR clear message. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
3	RW	0x0	SIMPLIFIED_REPLAY_TIMER Enables Simplified Replay Timer (Gen4). For more details, see "Transmit Replay" in "Transmit TLP Processing" section in the "Controller Operations" chapter of the Databook. Simplified Replay Timer can have the following Values: A value from 24,000 to 31,000 Symbol Times when Extended Synch is 0b. A value from 80,000 to 100,000 Symbol Times when Extended Synch is 1b. The Simplified Replay Timer value must not be changed while the link is in use. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
2	RW	0x0	UR_CA_MASK_4_TRGT1 When this field is set to '1', the controller suppresses error logging, error message generation, and CPL generation for non-posted requests TLPs (with UR filtering status) forwarded to your application (that is, when DEFAULT_TARGET =1). For more details, see "Advanced Error Handling For Received TLPs" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set Value After Reset: 0x0
1	RW	0x0	DEFAULT_TARGET Default target for an IO or MEM request with UR/CA/CRS received. Based on the value of this field the controller either drops or forwards these requests to your application. For more details, see "ECRC Handling" and "Request TLP Routing Rules" in "Receive Routing" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (DROP_IO_MEM_REQ): The controller drops all incoming I/O or MEM requests (after corresponding error reporting). A completion with UR status is generated for non-posted requests. 0x1 (FWD_IO_MEM_UR_CA_CRS): The controller forwards all incoming I/O or MEM requests with UR/CA/CRS status to your application. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	DBI_RO_WR_EN Write to RO Registers Using DBI. For more details, see "Writing to Read-Only Registers" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Your application can write to some RO and HwInit register fields through the DBI when you set this field to '1'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_MULTI_LANE_CONTROL_OFF
Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	UPCONFIGURE_SUPPORT Upconfigure Support. The controller sends this value as the Link Upconfigure Capability in TS2 Ordered Sets in Configuration.Complete state. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
6	RW	0x0	DIRECT_LINK_WIDTH_CHANGE Directed Link Width Change. If the upconfigure_capable variable is '1' and the PCIE_CAP_HW_AUTO_WIDTH_DISABLE bit in LINK_CONTROL_LINK_STATUS_REG is '0', the controller starts upconfigure or autonomous width downsizing (to the TARGET_LINK_WIDTH value) in the Configuration state. If TARGET_LINK_WIDTH value is 0x0, the controller does not start upconfigure or autonomous width downsizing in the Configuration state. The controller self-clears this field when the controller accepts this request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (CLEAR): Clear 0x1 (SET): The controller always moves to Configuration state through Recovery state when this bit is set to '1'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RW	0x00	TARGET_LINK_WIDTH Target Link Width. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (NOT_START): Controller does not start upconfigure or autonomous width downsizing in the Configuration state. 0x1 (X1): x1 0x2 (X2): x2 0x4 (X4): x4 0x8 (X8): x8 0x10 (X16): x16 0x20 (X32): x32 Value After Reset: 0x0

DSP_PCIE_PL_PHY_INTEROP_CTRL_OFF

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17:12	RW	0x1e	PHY_RST_TIMER Decide how many aux clock cycles the PHY reset lasts (0 to 63 aux clock cycles). Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3f (MAX_VAL): Max value Value After Reset: 0x1e
11	RO	0x0	reserved
10	RW	0x0	L1_CLK_SEL L1 Clock control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: This register field is sticky. Values: 0x1 (NO_REQ): Controller does not request aux_clk switch and core_clk gating in L1. 0x0 (CAN_REQ): Controller requests aux_clk switch and core_clk gating in L1. Value After Reset: 0x0
9	RW	0x0	L1_NOWAIT_P1 L1 entry control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (NO_WAIT_FOR_ACK): Controller does not wait for PHY to acknowledge transition to P1 before entering L1. 0x0 (WAIT_FOR_ACK): Controller waits for the PHY to acknowledge transition to P1 before entering L1. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
8	RW	0x0	L1SUB_EXIT_MODE L1 Exit Control Using phy_mac_pclkack_n. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. If PCLK as PHY input is selected, you should not write to this field and change the default value since PCLK as PHY input doesn't support any value other than the default. Note: This register field is sticky. Values: 0x1 (NO_WAIT_FOR_PCLKACK): Controller exits L1 without waiting for the PHY to assert phy_mac_pclkack_n. 0x0 (WAIT_FOR_PCLKACK): Controller waits for the PHY to assert phy_mac_pclkack_n before exiting L1. Value After Reset: 0x0
7	RO	0x0	reserved
6:0	RW	0x44	RXSTANDBY_CONTROL Rxstandby Control. Bits 0..5 determine if the controller asserts the RxStandby signal (mac_phy_rxstandby) in the indicated condition. Bit 6 enables the controller to perform the RxStandby/RxStandbyStatus handshake. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. [0]: Rx EIOS and subsequent T TX-IDLE-MIN [1]: Rate Change [2]: Inactive lane for upconfigure/downconfigure [3]: PowerDown=P1orP2 [4]: RxL0s.Idle [5]: EI Infer in L0 [6]: Execute RxStandby/RxStandbyStatus Handshake Note: This register field is sticky. Value After Reset: 0x44

DSP_PCIE_PL_TRGT_CPL_LUT_DELETE_ENTRY_OFF
Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31	RW	0x0	DELETE_EN This is a one-shot bit. This is a self-clearing register field. Reading from this register field always returns a '0'. Values: 0x0 (CLEAR): Clear 0x1 (SET): A '1' write to this bit triggers the deletion of the target completion LUT entry that is specified in the LOOK_UP_ID field. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:0	RW	0x00000000	LOOK_UP_ID This number selects one entry to delete of the TRGT_CPL_LUT. Value After Reset: 0x0

DSP_PCIE_PL_LINK_FLUSH_CONTROL_OFF
Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	AUTO_FLUSH_EN Enables automatic flushing of pending requests before sending the reset request to the application logic to reset the PCIe controller and the AXI Bridge. The flushing process is initiated if any of the following events occur: Hot reset request. A downstream port (DSP) can "hot reset" an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. Warm (Soft) reset request. Generated when exiting from D3 to D0 and cfg_pm_no_soft_rst=0. Link down reset request. A high to low transition on smlh_req_rst_not indicates the link has gone down and the controller is requesting a reset. If you disable automatic flushing, your application is responsible for resetting the PCIe controller and the AXI Bridge. For more details see "Warm and Hot Resets" section in the Architecture chapter of the Databook. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x1

DSP_PCIE_PL_AMBA_ERROR_RESPONSE_DEFAULT_OFF
Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:10	RW	0x27	AMBA_ERROR_RESPONSE_MAP AXI Slave Response Error Map. Allows you to selectively map the errors received from the PCIe completion (for non-posted requests) to the AXI slave responses, slv_rresp or slv_bresp. The recommended setting is SLVERR. CRS is always mapped to OKAY. [0] 0: UR (unsupported request) -> DECERR 1: UR (unsupported request) -> SLVERR [1] 0: CRS (configuration retry status) -> DECERR 1: CRS (configuration retry status) -> SLVERR [2] 0: CA (completer abort) -> DECERR 1: CA (completer abort) -> SLVERR [3]: RESERVED (0x0) [4]: RESERVED (0x0) [5] 0: Completion Timeout -> DECERR 1: Completion Timeout -> SLVERR. The AXI bridge internally drops (processes internally but not passed to your application) a completion that has been marked by the Rx filter as UC or MLF, and does not pass its status directly down to the slave interface. It waits for a timeout and then signals "Completion Timeout" to the slave interface. The controller sets the AXI slave read databus to 0xFFFF for all error responses. Note: This register field is sticky. Value After Reset: 0x27
9:5	RO	0x00	reserved
4:3	RW	0x0	AMBA_ERROR_RESPONSE_CRS CRS Slave Error Response Mapping. Determines the AXI slave response for CRS completions. For more details see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky. Values: 0x0 (OK_): OKAY 0x1 (OK_CRS_CMPL): OKAY with all FFFF_FFFF data for all CRS completions 0x2 (OK_READ_REQ): OKAY with FFFF_0001 data for CRS completions to vendor ID read requests, OKAY with FFFF_FFFF data for all other CRS completions 0x3 (SLVERR_DECERR): SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Value After Reset: 0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	AMBA_ERROR_RESPONSE_VENDORID Vendor ID Non-existent Slave Error Response Mapping. Determines the AXI slave response for errors on reads to non-existent Vendor ID register. For more details see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky. Values: 0x0 (_OK_): OKAY (with FFFF data). 0x1 (_ERR_): SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Value After Reset: 0x0
1	RO	0x0	reserved
0	RW	0x0	AMBA_ERROR_RESPONSE_GLOBAL Global Slave Error Response Mapping. Determines the AXI slave response for all error scenarios on non-posted requests. For more details see "Error Handling" in the AXI chapter of the Databook. The error response mapping is not applicable to Non-existent Vendor ID register reads. Note: This register field is sticky. Values: 0x0 (OK_): OKAY (with FFFF data for non-posted requests) 0x1 (ERR_): SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Value After Reset: 0x0

DSP_PCIE_PL_AMBA_LINK_TIMEOUT_OFF

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	LINK_TIMEOUT_ENABLE_DEFAULT Disable Flush. Note: This register field is sticky. Values: 0x0 (ENABLE): Enable 0x1 (DISABLE): You can disable the flush feature by setting this field to '1'. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x32	LINK_TIMEOUT_PERIOD_DEFAULT Timeout Value (ms). The timer will timeout and then flush the bridge TX request queues after this amount of time. The timer counts when there are pending outbound AXI slave interface requests and the PCIe TX link is not transmitting any of these requests. The timer is clocked by core_clk. Note: This register field is sticky. Value After Reset: 0x32

DSP_PCIE_PL_AMBA_ORDERING_CTRL_OFF

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	AX_MSTR_ZEROLREAD_FW AXI Master Zero Length Read Forward to the application. The DW PCIe controller AXI bridge is able to terminate in order with the Posted transactions the zero length read, implementing the PCIe express flush semantics of the Posted transactions. Values: 0x0 (_0_LN_RD_TERMINATE): The zero length Read is terminated at the DW PCIe AXI bridge master 0x1 (_0_LN_RD_FWD): The zero length Read is forward to the application. Value After Reset: 0x0
6:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:3	RW	0x0	AX_MSTR_ORDR_P_EVENT_SEL AXI Master Posted Ordering Event Selector. This field selects how the master interface determines when a P write is completed when enforcing the PCIe ordering rule, "NP must not pass P" at the AXI Master Interface. The AXI protocol does not support ordering between channels. Therefore, NP reads can pass P on your AXI bus fabric. This can result in an ordering violation when the read overtakes a P that is going to the same address. Therefore, the bridge master does not issue any NP requests until all outstanding P writes reach their destination. It does this by waiting for the all of the write responses on the B channel. This can affect the performance of the master read channel. For scenarios where the interconnect serializes the AXI master "AW", "W" and "AR" channels,you can increase the performance by reducing the need to wait until the complete Posted transaction has effectively reached the application slave. Note: This setting will not affect: MSI interrupt catcher and P data ordering. This is always driven by the B'last event. DMA read engine TLP ordering. This is always driven by the B'last event. NP write transactions which are always serialized with P write transactions. Values: 0x0 (B): B'last event: wait for the all of the write responses on the B channel thereby ensuring that the complete Posted transaction has effectively reached the application slave (default). 0x1 (AW): AW'last event: wait until the complete Posted transaction has left the AXI address channel at the bridge master. 0x2 (W): W'last event: wait until the complete Posted transaction has left the AXI data channel at the bridge master. 0x3 (RSVD): Reserved Value After Reset: 0x0
2	RO	0x0	reserved
1	RW	0x0	AX_SNP_EN AXI Serialize Non-Posted Requests Enable. This field enables the AXI Bridge to serialize same ID Non-Posted Read/Write Requests on the wire. Serialization implies one outstanding same ID NP Read or Write on the wire and used to avoid AXI RAR and WAW hazards at the remote link partner. For more details, see the "Optional Serialization of AXI Slave Non-posted Requests" section in the AXI chapter of the Databook. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
0	RO	0x0	reserved

DSP_PCIE_PL_COHERENCY_CONTROL_1_OFF
Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_LOW_ADDR Boundary Lower Address For Memory Type. Bits [31:0] of dword-aligned address of the boundary for Memory type. The two lower address LSBs are '00'. Addresses up to but not including this value are in the lower address space region; addresses equal or greater than this value are in the upper address space region. Note: This register field is sticky. Value After Reset: 0x0
1	RO	0x0	reserved
0	RW	0x0	CFG_MEMTYPE_VALUE Sets the memory type for the lower and upper parts of the address space: Note: This register field is sticky. Values: 0x0 (LOWER_PREPH): lower = Peripheral; upper = Memory 0x1 (LOWER_MEM): lower = Memory type; upper = Peripheral Value After Reset: 0x

DSP_PCIE_PL_COHERENCY_CONTROL_2_OFF
Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_HIGH_ADDR Boundary Upper Address For Memory Type. Bits [63:32] of the 64-bit dword-aligned address of the boundary for Memory type. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_COHERENCY_CONTROL_3_OFF
Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	CFG_MSTR_AWCACHE_VALUE Master Write CACHE Signal Value. Value of the individual bits in mstr_awcache when CFG_MSTR_AWCACHE_MODE is '1'. Note: Not applicable to message requests; for message requests the value of mstr_awcache is always '0000'. Note: This register field is sticky. Value After Reset: 0x0
26:23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:19	RW	0x0	CFG_MSTR_ARCACHE_VALUE Master Read CACHE Signal Value. Value of the individual bits in mstr_arcache when CFG_MSTR_ARCACHE_MODE is '1'. Note: This register field is sticky. Value After Reset: 0x0
18:15	RO	0x0	reserved
14:11	RW	0x0	CFG_MSTR_AWCACHE_MODE Master Write CACHE Signal Behavior. Defines how the individual bits in mstr_awcache are controlled. Note: for message requests the value of mstr_awcache is always "0000" regardless of the value of this bit. Note: This register field is sticky. Values: 0x0 (SET_BY_AXI_MASTER): set automatically by the AXI master 0x1 (SET_BY_FIELD): set by the value of the corresponding bit of the CFG_MSTR_AWCACHE_VALUE field Value After Reset: 0x0
10:7	RO	0x0	reserved
6:3	RW	0x0	CFG_MSTR_ARCACHE_MODE Master Read CACHE Signal Behavior. Defines how the individual bits in mstr_arcache are controlled. Note: This register field is sticky. Values: 0x0 (SET_BY_AXI_MASTER): set automatically by the AXI master 0x1 (SET_BY_FIELD): set by the value of the corresponding bit of the CFG_MSTR_ARCACHE_VALUE field Value After Reset: 0x0
2:0	RO	0x0	reserved

DSP_PCIE_PL_AXI_MSTR_MSG_ADDR_LOW_OFF

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	CFG_AXIMSTR_MSG_ADDR_LOW Lower 20-bits of the programmable AXI address for Messages. Note: This register field is sticky. Value After Reset: 0x0
11:0	RO	0x000	CFG_AXIMSTR_MSG_ADDR_LOW_RESERVED Reserved for future use. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_AXI_MSTR_MSG_ADDR_HIGH_OFF
Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_AXIMSTR_MSG_ADDR_HIGH Upper 32 bits of the programmable AXI address for Messages. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_PCIE_VERSION_NUMBER_OFF
Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3536302a	VERSION_NUMBER Version Number. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x3536302a

DSP_PCIE_PL_PCIE_VERSION_TYPE_OFF
Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x6c703035	VERSION_TYPE Version Type. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x6c703035

DSP_PCIE_PL_MSIX_ADDRESS_MATCH_LOW_OFF
Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	MSIX_ADDRESS_MATCH_LOW MSI-X Address Match Low Address. Note: This register field is sticky. Value After Reset: 0x0
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	MSIX_ADDRESS_MATCH_EN MSI-X Match Enable. Enable the MSI-X Address Match feature when the AXI bridge is present. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0

DSP_PCIE_PL_MSIX_ADDRESS_MATCH_HIGH_OFF
Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSIX_ADDRESS_MATCH_HIGH MSI-X Address Match High Address. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0

DSP_PCIE_PL_MSIX_DOORBELL_OFF
Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	WO	0x00	MSIX_DOORBELL_PF MSIX Doorbell Physical Function. This register determines the Physical Function for the MSI-X transaction. Value After Reset: 0x0
23:16	WO	0x00	MSIX_DOORBELL_VF MSIX Doorbell Virtual Function. This register determines the Virtual Function for the MSI-X transaction. Value After Reset: 0x0
15	WO	0x0	MSIX_DOORBELL_VF_ACTIVE MSIX Doorbell Virtual Function Active. This register determines whether a Virtual Function is used to generate the MSI-X transaction. Value After Reset: 0x0
14:12	WO	0x0	MSIX_DOORBELL_TC MSIX Doorbell Traffic Class. This register determines which traffic class to generate the MSI-X transaction with. Value After Reset: 0x0
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	WO	0x000	MSIX_DOORBELL_VECTOR MSI-X Doorbell Vector. This register determines which vector to generate the MSI-X transaction for. Value After Reset: 0x0

DSP_PCIE_PL_MSIX_RAM_CTRL_OFF
Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	MSIX_RAM_CTRL_DBG_PBA MSIX PBA RAM Debug Mode. You can also use the dbg_pba input to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable. Use this bit to activate the debug mode and allow direct read/write access to the PBA. Value After Reset: 0x0
24	RW	0x0	MSIX_RAM_CTRL_DBG_TABLE MSIX Table RAM Debug Mode. You can also use the dbg_table input to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable. Use this bit to activate the debug mode and allow direct read/write access to the Table. Value After Reset: 0x0
23:17	RO	0x00	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	MSIX_RAM_CTRL_BYPASS MSIX RAM Control Bypass. It is up to the application to ensure the RAMs are in the proper power state before trying to access them. Moreover, the application needs to observe all timing requirements of the RAM low power signals before trying to use the MSIX functionality. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): The bypass field, when set, disables the internal generation of low power signals for both RAMs. Value After Reset: 0x0
15:10	RO	0x00	reserved
9	RW	0x0	MSIX_RAM_CTRL_PBA_SD MSIX PBA RAM Shut Down. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_pba_sd output to signal your external logic to place the MSIX PBA RAM in Shut Down low-power mode. Value After Reset: 0x0
8	RW	0x0	MSIX_RAM_CTRL_PBA_DS MSIX PBA RAM Deep Sleep. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_pba_ds output to signal your external logic to place the MSIX PBA RAM in Deep Sleep low-power mode. Value After Reset: 0x0
7:2	RO	0x00	reserved
1	RW	0x0	MSIX_RAM_CTRL_TABLE_SD MSIX Table RAM Shut Down. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_table_sd output to signal your external logic to place the MSIX Table RAM in Shut Down low-power mode. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	MSIX_RAM_CTRL_TABLE_DS MSIX Table RAM Deep Sleep. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_table_ds output to signal your external logic to place the MSIX Table RAM in Deep Sleep low-power mode. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_CTRL0_OFF

Address: Operational Base + offset (0x03B0)

Bit	Attr	Reset Value	Description
31	RW	0x0	DTIM_CTRL0_IREQ_SW_FLUSH_EN Invalidate Request Software Flush Enable. If set enables software to flush pending DTI-ATS invalidate requests from the invalidate request queue. Software forces the flush by writing to the DTIM_CTRL1.INV_REQ_FLUSH_SID register. The flushing mechansim enables software to remove invalidate requests from the request queue in response to a UR from an Endpoint function. Prior to removing unsupported invalidate requests software should disable the hardware invalidate request timer (DTIM_CTRL0.IREQ_TMR_EN=0). To continue monitoring outstanding invalidate requests enable the timer once again. The timer restarts from its programmed timeout value (DTIM_CTRL5.IREQ_TMR_TRGT_TO). Note: Software initiated flushing does not result in a sync or timeout error. Note: This register field is sticky. Value After Reset: 0x0
30	RW	0x0	DTIM_CTRL0_IREQ_TMR_EN Invalidate Request Timer Enable. If set enables the DTIM to flush timed out DTI-ATS invalidate requests from the invalidate request queue. The invalidate request timer times each invalidation request sent on the wire. If disabled the responsibilty to flush the request is passed to software. Software writes to the DTIM_CTRL1.INV_REQ_FLUSH_SID register field to flush all pending requests associated with the particular Stream ID (SID). Subsequent received PCIe invalidate completions, associated with the particular SID, are treated as unexpected completions (completion received but no request pending). Timed out invalidate requests result in a sync error response to an outstanding sync request. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
29	RW	0x0	DTIM_CTRL0_IREQ_BYTE_ORDER Invalidate Request Byte Order. In normal operation PCIe data bytes are transmitted in little endian format, that is, PCIe data byte 0 is the first byte transmitted on the wire. The format of the DTI-ATS untranslated address and the PCIe untranslated address embedded in the two DWORD data field of the invalidate request message is defined in big endian format, that is, PCIe byte 0 contains the most significant byte of the address, byte 7. To align the DTI-ATS data byte order to PCIe data byte order the bytes are reversed. To be robust against misinterpretation of the byte order software can reverse the bytes by setting this bit. Note: This register field is sticky. Values: 0x0 (LITTLE_ENDIAN): DTI-ATS Invalidate Request data bytes are transmitted in little endian format. 0x1 (BIG_ENDIAN): DTI-ATS Invalidate Request data bytes are transmitted in big endian format. Value After Reset: 0x0
28	RW	0x0	DTIM_CTRL0_TRESP_BYTE_ORDER Translation Response Byte Order. In normal operation PCIe data bytes are transmitted in little endian format, that is, PCIe data byte 0 is the first byte transmitted on the wire. The format of the DTI-ATS translated address and the PCIe translated address embedded in the two DWORD data field of the translation completion is defined in big endian format, that is, PCIe byte 0 contains the most significant byte of the address, byte 7. To align the DTI-ATS data byte order to PCIe data byte order the bytes are reversed. To be robust against misinterpretation of the byte order software can reverse the bytes by setting this bit. Note: This register field is sticky. Values: 0x0 (LITTLE_ENDIAN): DTI-ATS Translation Response data bytes are transmitted in little endian format. 0x1 (BIG_ENDIAN): DTI-ATS Translation Response data bytes are transmitted in big endian format. Value After Reset: 0x0
27:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x1f	DTIM_CTRL0_TOK_TRANS_REQ Number of Translation Request Tokens Requested. Its default value is configured by the visible parameter, CC_DTIM_NUM_TRANS_TOKENS_REQUESTED. Software can overide this value at initialization time. The number of tokens requested is equal to TOK_TRANS_REQ + 1 (1 to 256). Note: This register field is sticky. Value After Reset: 0x1f
15:0	RW	0xffff	DTIM_CTRL0_ROOT_PORT_ID Root Port ID. Its default value is configured by the visible parameter, CC_ROOT_PORT_ID. Software can overide this value at initialization time. Note: This register field is sticky. Value After Reset: 0xffff

DSP_PCIE_PL_DTIM_CTRL1_OFF

Address: Operational Base + offset (0x03B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	DTIM_CTRL1_FLUSH_IREQ_GLOB Flush Invalidate Requests Global. Flushes all outstanding DTI-ATS invalidate requests. The flush is triggered when a 32-bit write to the DTIM_CTRL1 register is performed and FLUSH_IREQ_GLOB =1. Forcing the errored sync ack avoids deadlocking the SMMU in scenarios where the Endpoint function fails to complete the outstanding invalidate requests. In normal operation invalidate requests are flushed by hardware when the per Stream ID invalidate request timer expires. This field is primarily a test feature enabling software to force the sync ack to a pending sync request without having to wait for hardware to time out and flush all prior invalidate requests. Flushing outstanding DTI-ATS invalidate requests does not result in a timeout or a sync error (sync ack with its ERROR =1) if a sync request is outstanding. PCIe invalidate completions received after the flush sequence is complete are discarded and treated as unexpected completions (completion received but no request pending). If enabled, software is notified if unexpected completions are received. This field is valid if DTIM_CTRL0.FLUSH_CTRL_SW_EN is set. Note: This register field is sticky. Value After Reset: 0x0
30:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	DTIM_CTRL1_FLUSH_IREQ_SID Flush Invalidate Request Stream ID. Flushes all pending DTI-ATS invalidate requests, associated with a particuar Stream ID (SID/BDF), from the invalidate request queue. The flush is triggered when a 32-bit write to the DTIM_CTRL1 register is performed and FLUSH_IREQ_GLOB=0. FLUSH_IREQ_SID specifies the flushed Stream ID. This flushing mechanism enables software to remove invalidate requests from the request queue in response to a ERR_NONFATAL message from an Endpoint function. Software flushing of invalidate requests prior to a hardware invalidate request timeout does not result in a timeout error or a sync error (sync ack with its ERROR=1) if a sync request is outstanding. PCIe invalidate completions received with the flushed Stream ID are discarded and treated as unexpected completions (completion received but no request pending). If enabled, software is notified if unexpected completions are received. This field is valid if DTIM_CTRL0.FLUSH_CTRL_SW_EN is set. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_CTRL2_OFF

Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	DTIM_CTRL2_CONDIS_REQ Connect/Disconnect Request. Software initiates disconnection of the DTI-ATS interface when all ATC's have been invalidated and disabled and all outststanding page/translation requests have completed. The "Request Connect" and "Force Acknowledge" commands are used for debug purposes only. Note: This register field is sticky. Values: 0x0 (NOT_CARE): Don't care 0x1 (REQ_DISCONNECT): Request Disconnect 0x2 (REQ_CONNECT): Request Connect 0x3 (FORCE_ACK): Force Acknowledge Value After Reset: 0x0

DSP_PCIE_PL_DTIM_CTRL3_OFF

Address: Operational Base + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x4	DTIM_CTRL3_TREQ_WEIGHT AXI4 Master #0 Translation Request Priority Weighting. This value sets the priority of the DTI-ATS translation request messages being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x4
11	RO	0x0	reserved
10:8	RW	0x2	DTIM_CTRL3_PREQ_WEIGHT AXI4 Master #0 Page Request Priority Weighting. This value sets the priority of the DTI-ATS page request messages being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x2
7	RO	0x0	reserved
6:4	RW	0x1	DTIM_CTRL3_SREQ_WEIGHT DTI-ATS Sync Request Priority Weighting. This value sets the priority of the DTI-ATS sync acknowledge message being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x1
3	RO	0x0	reserved
2:0	RW	0x0	DTIM_CTRL3_IACK_WEIGHT DTI-ATS Invalidation Ack Priority Weighting. This value sets the priority of the DTI-ATS invalidate acknowledge message being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_CTRL4_OFF

Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	DTIM_CTRL4_TREQ_QOS_VC0 Translation Request Quality of Service Level VC0. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_CTRL5_OFF

Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DTIM_CTRL5_IREQ_TMR_TRGT_TO Invalidate Request Timeout Value (msec). The target timeout value is set to IREQ_TRGT_TO + 1. For example, programming this field to 15 sets the target timeout value to 16msec. The minimum target timeout value is 2msec. That is, IREQ_TRGT_TO must be greater than 0. The maximum target timeout value is 65536 msec. The target timeout value is the guaranteed minimum timeout value and must be set to an even number of msec. The timeout range is set at the target timeout value -0%, +50%. For example, if the target timeout value is set to 16msec then the timeout range is set at 16msec to 24msec. - This field is valid if DTIM_CTRL0.IREQ_TMR_EN is set. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_INT_STATUS_OFF

Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	DTIM_INT_STATUS_ERR_TRESP_OAS Translation Response Output Address Size Mismatch Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected a DTI-ATS translation response output address size mismatch error. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_TRESP_OAS_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
8	RO	0x0	DTIM_INT_STATUS_ERR_TRESP_UID Translation Response Unexpected ID Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected an unexpected DTI-ATS translation response. The translation response translation ID can not be associated with an outstanding DTI-ATS translation request. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_TRESP_UID_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:5	RO	0x0	reserved
4	RO	0x0	DTIM_INT_STATUS_ERR_ICPL_UC Invalidate Completion Unexpected Completion Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected an unexpected PCIe invalidate completion error. The PCIe invalidate completion tag can not be associated with an outstanding DTI-ATS invalidate request. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_ICPL_UC_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved
1	RO	0x0	DTIM_INT_STATUS_ERR_IREQ_OPERTN Invalidate Request Operation Code Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected an illegal DTI-ATS invalidate request operation code. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_OPERTN_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RO	0x0	DTIM_INT_STATUS_ERR_IREQ_TO Invalidate Request Timeout Error. Indicates that the Distributed Translation Interface Master (DTIM) has timed out one or more DTI-ATS invalidate requests. The Endpoint Translation Cache (ATC) has not returned one or more invalidate completions within an expected timeframe. The outstanding invalidate completion(s) are not expected to be received at this point in time. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_TO_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_DTIM_INT_EN_OFF
Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	DTIM_INT_EN_ERR_TRESP_OAS_INT_EN Translation Response Output Address Size Mismatch Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	DTIM_INT_EN_ERR_TRESP_UID_INT_EN Translation Response Unexpected ID Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0
7:5	RO	0x0	reserved
4	RW	0x0	DTIM_INT_EN_ERR_ICPL_UC_INT_EN Invalidate Completion Unexpected Completion Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0
3:2	RO	0x0	reserved
1	RW	0x0	DTIM_INT_EN_ERR_IREQ_OPERTN_INT_EN Invalidate Request Operation Code Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	DTIM_INT_EN_ERR_IREQ_TO_INT_EN Invalidate Request Timeout Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_INT_CLR_OFF
Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	WO	0x0	DTIM_INT_CLR_ERR_TRESP_OAS_INT_CLR Translation Response Output Address Size Mismatch Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_TRESP_OAS. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
8	WO	0x0	DTIM_INT_CLR_ERR_TRESP_UID_INT_CLR Translation Response Unexpected ID Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_TRESP_UID. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:5	RO	0x0	reserved
4	WO	0x0	DTIM_INT_CLR_ERR_ICPL_UC_INT_CLR Invalidate Completion Unexpected Completion Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_ICPL_UC. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved
1	WO	0x0	DTIM_INT_CLR_ERR_IREQ_OPERTN_INT_CLR Invalidate Request Operation Code Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_IREQ_OPERTN. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	WO	0x0	DTIM_INT_CLR_ERR_IREQ_TO_INT_CLR Invalidate Request Timeout Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_IREQ_TO. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_DTIM_INT_MSK_OFF
Address: Operational Base + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	DTIM_INT_MSK_ERR_TRESP_OAS_INT_MSK Translation Response Output Address Size Mismatch Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	DTIM_INT_MSK_ERR_TRESP_UID_INT_MSK Translation Response Unexpected ID Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
7:5	RO	0x0	reserved
4	RW	0x0	DTIM_INT_MSK_ERR_ICPL_UC_INT_MSK Invalidate Completion Unexpected Completion Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
3:2	RO	0x0	reserved
1	RW	0x0	DTIM_INT_MSK_ERR_IREQ_OPERTN_INT_MSK Invalidate Request Operation Code Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
0	RW	0x0	DTIM_INT_MSK_ERR_IREQ_TO_INT_MSK Invalidate Request Timeout Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_MSI_ADDR_UPR_OFF
Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DTIM_MSI_ADDR_UPR_MSI_ADDR MSI Target Address [63:32]. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_MSI_ADDR_LWR_OFF
Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	DTIM_MSI_ADDR_LWR_MSI_ADDR MSI Data. Note: This register field is sticky. Value After Reset: 0x0
1:0	RO	0x0	reserved

DSP_PCIE_PL_DTIM_MSI_DATA_OFF
Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DTIM_MSI_DATA_MSI_DATA MSI Data. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_PL_DTIM_ERR_LOG0_OFF
Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DTIM_ERR_LOG0_ERR_IREQ_OPCODE Invalidate Request Illegal Op Code. This field contains the DTI-ATS Invalidate Request "Operation" field and is set when an illegal invalidate request opcode is detected by the DTI Master. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_OPERTN_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RO	0x00	DTIM_ERR_LOG0_ERR_IREQ_TO_ITAG Invalidate Request Timeout ITAG. This field contains the itag associated with the first timed out DTI-ATS invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_TO_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:0	RO	0x0000	DTIM_ERR_LOG0_ERR_IREQ_TO_SID_LWR Invalidate Request Timeout Target SID/BDF. This field contains the target Stream/Device ID associated with the first timed out DTI-ATS invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_TO_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_DTIM_ERR_LOG1_OFF
Address: Operational Base + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RO	0x00	DTIM_ERR_LOG1_ERR_ICPL_UC_ITAG Unexpected Invalidate Completion ITAG. This field contains the PCIe invalidate completion itag associated with the first unexpected completion. A completion is unexpected if a completion is received from the Endpoint with a corresponding outstanding PCIe invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_ICPL_UC_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	DTIM_ERR_LOG1_ERR_ICPL_UC_REQ_ID Unexpected Invalidate Completion Requester ID. This field contains the PCIe invalidate completion Requester ID associated with the first unexpected completion. A completion is unexpected if a completion is received from the Endpoint with a corresponding outstanding PCIe invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_ICPL_UC_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_DTIM_ERR_LOG2_OFF
Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	DTIM_ERR_LOG2_ERR_TRESP_UR_TID Unexpected Translation Response ID. This field contains the DTI-ATS translation response translation ID associated with the first unexpeted translation response. A translation response is unexpected when a response is received without a corresponding outstanding translation request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_TRESP_UID_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_DTIM_DIAG_OFF
Address: Operational Base + offset (0x03FC)

Bit	Attr	Reset Value	Description
31	RO	0x0	DTIM_DIAG_SUP_PRI Indicates of DTI-ATS Page Request/Responses are supported by the SMMU. The field corresponds to the SUP_PRI field of the DTI_ATS_CONDIS_ACK message. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:25	RO	0x00	reserved

Bit	Attr	Reset Value	Description
24	RO	0x0	DTIM_DIAG_VERSION Acknowledged DTI-ATS Protocol Version. The field corresponds to the VERSION field of the DTI_ATS_CONDIS_ACK message. 0000: DTI-ATSv1 Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:20	RO	0x0	DTIM_DIAG_OAS Maximum address size permitted for translated addresses. The field corresponds to the OAS field of the DTI_ATS_CONDIS_ACK message. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
19:16	RO	0x0	reserved
15:8	RO	0x00	DTIM_DIAG_TOK_TREQ_GNT This field indicates the number of pre-allocated tokens for translation requests that have been granted by the SMMU. The number of translation tokens granted is equal to the value of this field plus one. The field corresponds to the TOK_TRANS_GNT field of the DTI_ATS_CONDIS_ACK message. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RO	0x0	DTIM_DIAG_IREQ_FLUSH_SID_LWR_Q_EMPTY Invalidation Request Flush SID Lower Queue Empty Flag. If set, this bit indicates that all outstanding invalidate requests associated with the flushed Endpoint function, DTIM_CTRL1.IREQ_FLUSH_SID_LWR, have been flushed from the invalidate request queue. The flag is set when the software initiated flush sequence completes. If subsequent in-flight invalidate requests are received post the flush sequence then this flag will be cleared. Further flushing of the invalidate request queue is required in this case. Note: It is expected the SMMU stops sending invalidate requests to the DTIM prior to triggering the flush sequence. At some point all in-flight invalidate requests associated with the Endpoint function will be flushed. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
5	RO	0x0	DTIM_DIAG_IREQ_FLUSH_DONE Invalidate Request Flush Done. Invalidate Request Flush Done. If set this bit indicates that the software initiated invalidate request queue flush sequence has completed. The flag is initially cleared by hardware when the flush sequence is initially triggerred by a write to the DTIM_CTRL1 register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	RO	0x1	DTIM_DIAG_IREQ_ORDRQ_EMPTY Invalidation Request Order Q Empty Flag. If set this bit indicates the DTI-ATS invalidate request queue is empty, that is, all invalidate requests have received a completion or invalidate request have not be sent to the DTIM or sent to the DTIM but discarded (broadcast DTI-ATS invalidate requests). Value After Reset: 0x1 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RO	0x0	DTIM_DIAG_CONDIS_STATE Connect/Disconnect FSM state. The field corresponds to the current state of the Connect/Disconnect FSM. The following encoding applies: Other value are reserved. Values: 0x0 (DISCONNECTED): DISCONNECTED 0x1 (REQ_CONNECT): REQ_CONNECT 0x2 (CONNECTED): CONNECTED 0x3 (REQ_DISCONNECT): REQ_DISCONNED Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_PL_APP_BUS_DEV_NUM_STATUS_OFF

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	RC_DSW_BUS_NUM This field reflects the value of bus number driven on app_bus_num input signal by your application. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:3	RO	0x00	RC_DSW_DEV_NUM This field reflects the value of device number driven on app_device_num input signal by your application. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:0	RO	0x0	reserved

DSP_PCIE_PL_PCIPM_TRAFFIC_CTRL_OFF

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	PCIPM_NEW_TLP_CLIENT2_BLOCKED This field indicates that all TLPs transmitted by Client 2 interface are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x0
2	RW	0x0	PCIPM_NEW_TLP_CLIENT1_BLOCKED This field indicates that all TLPs transmitted by Client 1 interface are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x0
1	RW	0x0	PCIPM_NEW_TLP_CLIENT0_BLOCKED This field indicates that all TLPs transmitted by Client 0 interface are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x0
0	RW	0x0	PCIPM_VDM_TRAFFIC_BLOCKED This field indicates that VDM Message TLPs are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x

DSP_PCIE_PL_PL_LTR_LATENCY_OFF

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31	RW	0x0	NO_SNOOP_LATENCY_REQUIRE No Snoop Latency Requirement. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
30:29	RO	0x0	reserved
28:26	RW	0x0	NO_SNOOP_LATENCY_SCALE No Snoop Latency Scale. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
25:16	RW	0x000	NO_SNOOP_LATENCY_VALUE No Snoop Latency Value. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15	RW	0x0	SNOOP_LATENCY_REQUIRE Snoop Latency Requirement. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
14:13	RO	0x0	reserved
12:10	RW	0x0	SNOOP_LATENCY_SCALE Snoop Latency Scale. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
9:0	RW	0x000	SNOOP_LATENCY_VALUE Snoop Latency Value. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_PL_AUX_CLK_FREQ_OFF

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x018	AUX_CLK_FREQ The aux_clk frequency in MHz. This value is used to provide a 1 us reference for counting time during low-power states with aux_clk when the PHY has removed the pipe_clk. Frequencies lower than 1 MHz are possible but with a loss of accuracy in the time counted. If the actual frequency (f) of aux_clk does not exactly match the programmed frequency (f_prog), then there is an error in the time counted by the controller that can be expressed in percentage as: err% = (f_prog/f-1)*100. For example if f=2.5 MHz and f_prog=3 MHz, then err% =(3/2.5-1)*100 =20%, meaning that the time counted by the controller on aux_clk will be 20% greater than the time in us programmed in the corresponding time register (for example T_POWER_ON). Note: This register field is sticky. Value After Reset: 0x18

DSP_PCIE_PL_L1_SUBSTATES_OFF
Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	L1SUB_LOW_POWER_CLOCK_SWITCH_MODE If the bit is set to 1'b1 the controller will delay the switching of aux_clk to the slow platform clock until it detects that the link partner has de-asserted CLKREQ#. Note: This register field is sticky. Values: 0x0 (CLEAR): The reference clock may be gated off when CLKREQ# is de-asserted. 0x1 (SET): The reference clock shall be kept running regardless of the CLKREQ# setting. Value After Reset: 0x0
7:6	RW	0x3	L1SUB_T_PCLKACK Max delay (in 1us units) between a MAC request to remove the clock on mac_phy_pclkreq_n and a PHY response on phy_mac_pclkack_n. If the PHY does not respond within this time the request is aborted. Range is 1..4 Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x3 (MAX_VAL): Max value Value After Reset: 0x3

Bit	Attr	Reset Value	Description
5:2	RW	0x4	L1SUB_T_L1_2 Duration (in 1us units) of L1.2. Range is 1..16. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x4
1:0	RW	0x2	L1SUB_T_POWER_OFF Duration (in 1us units) of L1.2.Entry. Range is 1..4. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x3 (MAX_VAL): Max value Value After Reset: 0x2

DSP_PCIE_PL_POWERDOWN_CTRL_STATUS_OFF

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	POWERDOWN_PHY_POWERDOWN This field represents the Powerdown value that has been acknowledged by the PHY. It is updated with the value of Powerdown driven by the controller, when the PHY has returned the Phystatus acknowledgment for the Powerdown transition. Value After Reset: 0x2 Testable: writeAsRead Volatile: true
7:4	RW	0x2	POWERDOWN_MAC_POWERDOWN This field represents the Powerdown value driven by the controller to the PHY. Value After Reset: 0x2 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	POWERDOWN_VMAIN_ACK Set this bit to 1 if you do not want to perform the handshake with the power-switch after PERST# assertion. By default the controller will perform the handshake with the power-switch if L1 power gating is enabled Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): If you do not want to perform the handshake with the power-switch after PERST# assertion. Value After Reset: 0x0
0	WO	0x0	POWERDOWN_FORCE This field is a one shot field. This field could be used for debug purposes in event that the P2 Powerdown transition does not complete. It will allow the controller to proceed with the transition to the P1 Powerdown state. This field always reads back as 1'b0. Values: 0x0 (CLEAR): Clear 0x1 (SET): Writing a value of 1 to this field causes the controller to complete the P2 Powerdown handshake regardless of whether the PHY has returned Phystatus. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_PL_PIPE_RELATED_OFF

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	PIPE_GARBAGE_DATA_MODE PIPE Garbage Data Mode. RxValid is deasserted a valid RxStartBlock is received at 128b/130b encoding a valid COM symbol is received at 8b/10b encoding Note: This register field is sticky. Values: 0x0 (COMPLIANT_MODE): PIPE Spec compliant mode: The MAC discards any symbols received after the electrical idle ordered-set until RxValid is deasserted. 0x1 (PHY_SUP_MODE): Special PHY Support mode: The MAC discards any symbols received after the electrical idle ordered-set until when any of the following three conditions are true: Value After Reset: 0x0
7:0	RO	0x00	reserved

11.4.3.23 DSP_PCIE_MSIX_CAP_DBI2 Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_MSIX_CAP_DBI2_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x007F0000	MSI-X Capability ID, Next Pointer, Control Registers
DSP_PCIE_MSIX_CAP_DBI2_MSIX_TABLE_OFFSET_REG	0x0004	W	0x00000000	MSI-X Table Offset and BIR Register
DSP_PCIE_MSIX_CAP_DBI2_MSIX_PBA_OFFSET_REG	0x0008	W	0x00000800	MSI-X PBA Offset and BIR Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.24 DSP_PCIE_MSIX_CAP_DBI2 Detail Registers Description

DSP_PCIE_MSIX_CAP_DBI2_PCI_MSIX_CAP_ID_NEXT_CTRL_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x07f	PCI_MSIX_TABLE_SIZE MSI-X Table Size in the shadow register. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x7f Testable: untestable Volatile: true
15:0	RO	0x0000	reserved

DSP_PCIE_MSIX_CAP_DBI2_MSIX_TABLE_OFFSET_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	PCI_MSIX_TABLE_OFFSET MSI-X Table Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: untestable Volatile: true
2:0	RW	0x0	PCI_MSIX_BIR MSI-X Table BAR Indicator Register Field. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI , is used to map the Function's MSI-X Table into Memory Space. All encodings other than the defined encodings are reserved. For a 64-bit Base Address Register , the Table BIR indicates the lower DWORD. For Functions with Type 1 Configuration Space headers, BIR values 2 through 5 are also Reserved. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Values: 0x0 (BAR_10): Base Address Register 10h 0x1 (BAR_14): Base Address Register 14h 0x2 (BAR_18): Base Address Register 18h 0x3 (BAR_1C): Base Address Register 1Ch 0x4 (BAR_20): Base Address Register 20h 0x5 (BAR_24): Base Address Register 24h Value After Reset: 0x0 Testable: untestable Volatile: true

DSP_PCIE_MSIX_CAP_DBI2_MSIX_PBA_OFFSET_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000100	PCI_MSIX_PBA_OFFSET MSI-X PBA Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Value After Reset: 0x100 Testable: untestable Volatile: true
2:0	RW	0x0	PCI_MSIX_PBA_BIR MSI-X PBA BIR. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the Table BIR . Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: untestable Volatile: true

11.4.3.25 DSP_PCIE_IATU Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_IATU_REGION_CTRL_1_OFF_OUTBOUND_i	0x0000	W	0x00000000	iATU Region Control 1 Register (for i = 0; i <= 15)
DSP_PCIE_IATU_REGION_CTRL_2_OFF_OUTBOUND_i	0x0004	W	0x00000000	iATU Region Control 2 Register (for i = 0; i <= 15)
DSP_PCIE_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_i	0x0008	W	0x00000000	iATU Lower Base Address Register (for i = 0; i <= 15)

Name	Offset	Size	Reset Value	Description
DSP_PCIE_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_i	0x000C	W	0x00000000	iATU Upper Base Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_LIMIT_ADDR_OFF_OUTBOUND_i	0x0010	W	0x0000FFF0	iATU Limit Address Registe (for i = 0; i <= 15)
DSP_PCIE_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i	0x0014	W	0x00000000	iATU Lower Target Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_i	0x0018	W	0x00000000	iATU Upper Target Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_i	0x0020	W	0x00000000	iATU Upper Limit Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_REGION_CTRL_1_OFF_INBOUND_i	0x0100	W	0x00000000	iATU Region Control 1 Register (for i = 0; i <= 15)
DSP_PCIE_IATU_REGION_CTRL_2_OFF_INBOUND_i	0x0104	W	0x00000000	iATU Region Control 2 Register (for i = 0; i <= 15)
DSP_PCIE_IATU_LWR_BASE_ADDR_OFF_INBOUND_i	0x0108	W	0x00000000	iATU Lower Base Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_UPPER_BASE_ADDR_OFF_INBOUND_i	0x010C	W	0x00000000	iATU Upper Base Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_LIMIT_ADDR_OFF_INBOUND_i	0x0110	W	0x0000FFF0	iATU Limit Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_LWR_TARGET_ADDR_OFF_INBOUND_i	0x0114	W	0x00000000	iATU Lower Target Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_i	0x0118	W	0x00000000	iATU Upper Target Address Register (for i = 0; i <= 15)
DSP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_i	0x0120	W	0x00000000	iATU Upper Limit Address Register (for i = 0; i <= 15)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.26 DSP_PCIE_IATU Detail Registers Description

DSP_PCIE_IATU_REGION_CTRL_1_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Function Number. When the address of an outbound TLP is matched to this region and the FUNC_BYPASS field in the "iATU Region Control 2 Register" is '0', then the function number used in generating the function part of the requester ID (RID) field of the TLP is taken from this 5-bit register. The value in this register must be 0x0 unless multifunction operation in the controller is enabled (CX_NFUNC > 1). When you are using the AXI Bridge, then this field is swapped before AXI decomposition occurs so that the correct "Max_Read_Request_Size" and "Max_Payload_Size" values are used. Note: This register field is sticky. Value After Reset: 0x0
19:18	RO	0x0	reserved
17:16	RW	0x0	AT AT. When the address of an outbound TLP is matched to this region, then the AT field of the TLP is changed to the value in this register. Only valid when the ATS_ENABLE configuration parameter is '1'. Note: This register field is sticky. Value After Reset: 0x0
15:14	RO	0x0	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky. Values: 0x1 (ENABLE): Maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE 0x0 (DISABLE): Maximum ATU Region size is 4 GB (default) Value After Reset: 0x0
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky. Value After Reset: 0x0
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_REGION_CTRL_2_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky. Value After Reset: 0x0
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0

Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky. Value After Reset: 0x0
27	RW	0x0	DMA_BYPASS DMA Bypass Mode. Allows request TLPs which are initiated by the DMA controller to pass through the iATU untranslated. Note: This field is reserved for the SW product. You must set it to '0'. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
26:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky. Values: 0x1 (FILL_BYTES): LWR_TARGET_RW in the iATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i register is used to fill bytes 8-to-11 (for 3 DWORD header) or bytes 12-to-15 (for 4 DWORD header) of the translated TLP header. 0x0 (FORM_ADDR): LWR_TARGET_RW in the iATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i register forms the new address of the translated region. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky. Values: 0x1 (NO_SUPPORT_FOR_DATA_TLP): Fmt[1] =0 so that only TLP type without data is sent. For example, a Msg instead of MsgD will be sent. 0x0 (SUPPORT_DATA_TLP): Fmt[1] =0/1 so that TLPs with or without data can be sent. Value After Reset: 0x0
21	RO	0x0	reserved
20	RW	0x0	SNP TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are TC PH TH ST AT Attr (IDO, RO and NS). Note: This register field is sticky. Value After Reset: 0x0
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
18:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky. Value After Reset: 0x0
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky. Value After Reset: 0x0
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE) Value After Reset: 0x0

DSP_PCIE_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_LIMIT_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky. Value After Reset: 0x0
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky. Value After Reset: 0xfff

Bit	Attr	Reset Value	Description
3:0	RO	0x0	CBUF_INCR Circular Buffer. Note: This register field is sticky. Value After Reset: 0xf

DSP_PCIE_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'. Value After Reset: 0x0
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_REGION_CTRL_1_OFF_INBOUND_i

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Function Number. MEM-I/O: When the Address and BAR matching logic in the controller indicate that a MEM-I/O transaction matches a BAR in the function corresponding to this value, then address translation proceeds. This check is only performed if the "Function Number Match Enable" bit of the "iATU Region Control 2 Register" is set. CFG0/CFG1: When the destination function number as specified in the routing ID of the TLP header matches the function, then address translation proceeds. This check is only performed if the "Function Number Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
19:18	RO	0x0	reserved
17:16	RW	0x0	AT When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "AT Match Enable" bit of the "iATU Region Control 2 Register" is set. Only valid when the ATS_ENABLE configuration parameter is '1'. Note: This register field is sticky. Value After Reset: 0x0
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky. Values: 0x1 (ENABLE): Maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE 0x0 (DISABLE): Maximum ATU Region size is 4 GB (default) Value After Reset: 0x0
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_REGION_CTRL_2_OFF_INBOUND_i
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky. Values: 0x0 (ZERO): The interpretation is dependent on TLP type, that is, MEM/IO, CFG0, or MSG/MSGD TLPs. 0x1 (ONE): The interpretation is dependent on TLP type, that is, MEM/IO, CFG0, or MSG/MSGD TLPs. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky. Values: 0x1 (ENABLE): Invert Mode Enable 0x0 (DISABLE): Invert Mode Disable Value After Reset: 0x0
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky. Values: 0x1 (ENABLE): CFG Shift Enable 0x0 (DISABLE): CFG Shift Disable Value After Reset: 0x0
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. MWr, MRd, and MRdLk TLPs are seen as identical The Routing field of Msg/MsgD TLPs is ignored FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky. Values: 0x1 (ENABLE): Fuzzy Type Match Enable 0x0 (DISABLE): Fuzzy Type Match Disable Value After Reset: 0x0
26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky. Values: 0x0 (NORMAL_RADM): Normal RADM filter response is used. 0x1 (UNSUP_REQ): Unsupported request (UR) 0x2 (COMPL_ABORT): Completer abort (CA) 0x3 (NOT_USED): Not used / undefined / reserved Value After Reset: 0x0
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky. Values: 0x1 (ENABLE): Message Code Match Enable (for Msg TLPS) or ST Match Enable (for Mem TLPs) 0x0 (DISABLE): Virtual Function Number Match Disable Value After Reset: 0x0
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19	RW	0x0	FUNC_NUM_MATCH_EN Function Number Match Enable. Ensures that a successful Function Number TLP field comparison match (see Function Number field of the "iATU Region Control 1 Register") occurs (in MEM-I/O and CFG0/CFG1 transactions) for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): Function Number Match Enable 0x0 (DISABLE): Function Number Match Disable Value After Reset: 0x0
18	RO	0x0	reserved
17	RW	0x0	AT_MATCH_EN AT Match Enable. Ensures that a successful AT TLP field comparison match (see AT field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Only valid when the ATS_ENABLE configuration parameter is '1'. Note: This register field is sticky. Values: 0x1 (ENABLE): AT Match Enable 0x0 (DISABLE): AT Match Disable Value After Reset: 0x0
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): ATTR Match Enable 0x0 (DISABLE): ATTR Match Disable Value After Reset: 0x0
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): TD Match Enable 0x0 (DISABLE): TD Match Disable Value After Reset: 0x0

Bit	Attr	Reset Value	Description
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): TC Match Enable 0x0 (DISABLE): TC Match Disable Value After Reset: 0x0
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
12:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	BAR_NUM BAR Number. When the BAR number of an inbound MEM or IO TLP " that is matched by the normal internal BAR address matching mechanism " is the same as this field, address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Match Mode" bit of the "iATU Region Control 2 Register" is set. IO translation would require either 00100b or 00101b in the inbound TLP TYPE; the BAR Number set in the range 000b - 101b and that BAR configured as an IO BAR. Note: This register field is sticky. Values: 0x0 (BAR0): BAR0 0x1 (BAR1): BAR1 0x2 (BAR2): BAR2 0x3 (BAR3): BAR3 0x4 (BAR4): BAR4 0x5 (BAR5): BAR5 0x6 (ROM): ROM 0x7 (RSVD): reserved Value After Reset: 0x0
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_LWR_BASE_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky. Value After Reset: 0x0
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE) Value After Reset: 0x0

DSP_PCIE_IATU_UPPER_BASE_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_LIMIT_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky. Value After Reset: 0xfff
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: 0000b: 0 (Default; legacy Single Address Location mode) 0001b: 4 0010b: 8 0011b: 16 0100b: 32 0101b: 64 0110b: 128 0111b: 256 1000b: 512 1001b: 1024 1010b: 2048 1011b: 4096 1100b: 8192 1101b: rsvd. 1110b: rsvd. 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer ? that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_LWR_TARGET_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky. Value After Reset: 0x0
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. Field size depends on log2(BAR_MASK+1) in BAR match mode. Value After Reset: 0x0

DSP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky. Value After Reset: 0x0

DSP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky. Value After Reset: 0x0

11.4.3.27 DSP_PCIE_DMA Registers Summary

Name	Offset	Size	Reset Value	Description
DSP_PCIE_DMA_CTRL_DATA_ARB_PRIOR_OFF	0x0000	W	0x00000688	DMA Arbitration Scheme for TRGT1 Interface
DSP_PCIE_DMA_CTRL_OFF	0x0008	W	0x00020002	DMA Number of Channels Register
DSP_PCIE_DMA_WRITE_ENGINE_EN_OFF	0x000C	W	0x00000000	DMA Write Engine Enable Register
DSP_PCIE_DMA_WRITE_DOORBELL_OFF	0x0010	W	0x00000000	DMA Write Doorbell Register
DSP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF	0x0018	W	0x00008421	DMA Write Engine Channel Arbitration Weight Low Register
DSP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF	0x001C	W	0x00000000	DMA Write Engine Channel Arbitration Weight High Register
DSP_PCIE_DMA_READ_ENGINE_EN_OFF	0x002C	W	0x00000000	DMA Read Engine Enable Register
DSP_PCIE_DMA_READ_DOORBELL_OFF	0x0030	W	0x00000000	DMA Read Doorbell Register
DSP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF	0x0038	W	0x00008421	DMA Read Engine Channel Arbitration Weight Low Register
DSP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF	0x003C	W	0x00008421	DMA Read Engine Channel Arbitration Weight High Register
DSP_PCIE_DMA_WRITE_INT_STATUS_OFF	0x004C	W	0x00000000	DMA Write Interrupt Status Register
DSP_PCIE_DMA_WRITE_INT_MASK_OFF	0x0054	W	0x00030003	DMA Write Interrupt Mask Register
DSP_PCIE_DMA_WRITE_INT_CLEAR_OFF	0x0058	W	0x00000000	DMA Write Interrupt Clear Register
DSP_PCIE_DMA_WRITE_ERR_STATUS_OFF	0x005C	W	0x00000000	DMA Write Error Status Register
DSP_PCIE_DMA_WRITE_DONE_IMWR_LOW_OFF	0x0060	W	0x00000000	DMA Write Done IMWr Address Low Register
DSP_PCIE_DMA_WRITE_DONE_IMWR_HIGH_OFF	0x0064	W	0x00000000	DMA Write Done IMWr Interrupt Address High Register
DSP_PCIE_DMA_WRITE_ABORT_IMWR_LOW_OFF	0x0068	W	0x00000000	DMA Write Abort IMWr Address Low Register
DSP_PCIE_DMA_WRITE_ABORT_IMWR_HIGH_OFF	0x006C	W	0x00000000	DMA Write Abort IMWr Address High Register

Name	Offset	Size	Reset Value	Description
DSP_PCIE_DMA_WRITE_CH01_IMWR_DATA_OFF	0x0070	W	0x00000000	DMA Write Channel 1 and 0 IMWr Data Register
DSP_PCIE_DMA_WRITE_CH23_IMWR_DATA_OFF	0x0074	W	0x00000000	DMA Write Channel 3 and 2 IMWr Data Register
DSP_PCIE_DMA_WRITE_CH45_IMWR_DATA_OFF	0x0078	W	0x00000000	DMA Write Channel 5 and 4 IMWr Data Register
DSP_PCIE_DMA_WRITE_CH67_IMWR_DATA_OFF	0x007C	W	0x00000000	DMA Write Channel 7 and 6 IMWr Data Register
DSP_PCIE_DMA_WRITE_LINKED_LIST_ERR_EN_OFF	0x0090	W	0x00000000	DMA Write Linked List Error Enable Register
DSP_PCIE_DMA_READ_INT_STATUS_OFF	0x00A0	W	0x00000000	DMA Read Interrupt Status Register
DSP_PCIE_DMA_READ_INT_MASK_OFF	0x00A8	W	0x00030003	DMA Read Interrupt Mask Register
DSP_PCIE_DMA_READ_INT_CLEAR_OFF	0x00AC	W	0x00000000	DMA Read Interrupt Clear Register
DSP_PCIE_DMA_READ_ERR_STATUS_LOW_OFF	0x00B4	W	0x00000000	DMA Read Error Status Low Register
DSP_PCIE_DMA_READ_ERR_STATUS_HIGH_OFF	0x00B8	W	0x00000000	DMA Read Error Status High Register
DSP_PCIE_DMA_READ_LINKED_LIST_ERR_EN_OFF	0x00C4	W	0x00000000	DMA Read Linked List Error Enable Register
DSP_PCIE_DMA_READ_DONE_IMWR_LOW_OFF	0x00CC	W	0x00000000	DMA Read Done IMWr Address Low Register
DSP_PCIE_DMA_READ_DONE_IMWR_HIGH_OFF	0x00D0	W	0x00000000	DMA Read Done IMWr Address High Register
DSP_PCIE_DMA_READ_ABORT_IMWR_LOW_OFF	0x00D4	W	0x00000000	DMA Read Abort IMWr Address Low Register
DSP_PCIE_DMA_READ_ABORT_IMWR_HIGH_OFF	0x00D8	W	0x00000000	DMA Read Abort IMWr Address High Register
DSP_PCIE_DMA_READ_CH01_IMWR_DATA_OFF	0x00DC	W	0x00000000	DMA Read Channel 1 and 0 IMWr Data Register
DSP_PCIE_DMA_READ_CH23_IMWR_DATA_OFF	0x00E0	W	0x00000000	DMA Read Channel 3 and 2 IMWr Data Register
DSP_PCIE_DMA_READ_CH45_IMWR_DATA_OFF	0x00E4	W	0x00000000	DMA Read Channel 5 and 4 IMWr Data Register
DSP_PCIE_DMA_READ_CH67_IMWR_DATA_OFF	0x00E8	W	0x00000000	DMA Read Channel 7 and 6 IMWr Data Register
DSP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_LOW_OFF	0x0108	W	0x00000000	DMA Write Engine Handshake Counter Channel 0/1/2/3 Register
DSP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF	0x010C	W	0x00000000	DMA Write Engine Handshake Counter Channel 4/5/6/7 Register
DSP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF	0x0118	W	0x00000000	DMA Read Engine Handshake Counter Channel 0/1/2/3 Register
DSP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF	0x011C	W	0x00000000	DMA Read Engine Handshake Counter Channel 4/5/6/7 Register
DSP_PCIE_DMA_WRITE_CHi_PWR_EN_OFF	0x0128	W	0x00000000	DMA Write Channel 0 Power Enable Register (for i = 0; i <= 7)

Name	Offset	Size	Reset Value	Description
DSP_PCIE_DMA_READ_CHi_PWR_EN_OFF	0x0168	W	0x00000000	DMA Read Channel 0 Power Enable Register (for i = 0; i <= 7)
DSP_PCIE_DMA_CH_CONTROL1_OFF_WRCH_i	0x0200	W	0x00000000	DMA Write Channel Control 1 Register (for i = 0; i <= 1)
DSP_PCIE_DMA_TRANSFER_SIZE_OFF_WRCH_i	0x0208	W	0x00000000	DMA Write Transfer Size Register
DSP_PCIE_DMA_SAR_LOW_OFF_WRCH_i	0x020C	W	0x00000000	DMA Write SAR Low Register
DSP_PCIE_DMA_SAR_HIGH_OFF_WRCH_i	0x0210	W	0x00000000	DMA Write SAR High Register (for i = 0; i <= 1)
DSP_PCIE_DMA_DAR_LOW_OFF_WRCH_i	0x0214	W	0x00000000	DMA Write DAR Low Register (for i = 0; i <= 1)
DSP_PCIE_DMA_DAR_HIGH_OFF_WRCH_i	0x0218	W	0x00000000	DMA Write DAR High Register (for i = 0; i <= 1)
DSP_PCIE_DMA_LLP_LOW_OFF_WRCH_i	0x021C	W	0x00000000	DMA Write Linked List Pointer Low Register (for i = 0; i <= 1)
DSP_PCIE_DMA_LLP_HIGH_OFF_WRCH_i	0x0220	W	0x00000000	DMA Write Linked List Pointer High Register (for i = 0; i <= 1)
DSP_PCIE_DMA_CH_CONTROL1_OFF_RDCH_i	0x0300	W	0x00000000	DMA Read Channel Control 1 Register (for i = 0; i <= 1)
DSP_PCIE_DMA_TRANSFER_SIZE_OFF_RDCH_i	0x0308	W	0x00000000	DMA Read Transfer Size Register (for i = 0; i <= 1)
DSP_PCIE_DMA_SAR_LOW_OFF_RDCH_i	0x030C	W	0x00000000	DMA Read SAR Low Register (for i = 0; i <= 1)
DSP_PCIE_DMA_SAR_HIGH_OFF_RDCH_i	0x0310	W	0x00000000	DMA Read SAR High Register (for i = 0; i <= 1)
DSP_PCIE_DMA_DAR_LOW_OFF_RDCH_i	0x0314	W	0x00000000	DMA Read DAR Low Register (for i = 0; i <= 1)
DSP_PCIE_DMA_DAR_HIGH_OFF_RDCH_i	0x0318	W	0x00000000	DMA Read DAR High Register (for i = 0; i <= 1)
DSP_PCIE_DMA_LLP_LOW_OFF_RDCH_i	0x031C	W	0x00000000	DMA Read Linked List Pointer Low Register (for i = 0; i <= 1)
DSP_PCIE_DMA_LLP_HIGH_OFF_RDCH_i	0x0320	W	0x00000000	DMA Read Linked List Pointer High Register (for i = 0; i <= 1)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3.28 DSP_PCIE_DMA Detail Registers Description

DSP_PCIE_DMA_CTRL_DATA_ARB_PRIOR_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	VERSION Reports the version of Register Map of eDMA. Value After Reset: 0x0
11:9	RW	0x3	RDBUFF_TRGT_WEIGHT DMA Read Channel MWr Requests. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x3

Bit	Attr	Reset Value	Description
8:6	RW	0x2	RD_CTRL_TRGT_WEIGHT DMA Read Channel MRd Requests (for LL element/descriptor access). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x2
5:3	RW	0x1	WR_CTRL_TRGT_WEIGHT DMA Write Channel MRd Requests (for DMA data requests and LL element/descriptor access). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
2:0	RW	0x0	RTRGT1_WEIGHT Non-DMA Rx Requests. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_CTRL_OFF

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	DIS_C2W_CACHE_RD Disable DMA Read Channel's "completion to memory write" context cache pre-fetch function. Note: For internal debugging only. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
24	RW	0x0	DIS_C2W_CACHE_WR Disable DMA Write Channel's "completion to memory write" context cache pre-fetch function. Note: For internal debugging only. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RO	0x2	NUM_DMA_RD_CHAN Number of Read Channels. You can read this register to determine the number of read channels configured. Value After Reset: 0x2
15:4	RO	0x000	reserved
3:0	RO	0x2	NUM_DMA_WR_CHAN Number of Write Channels. You can read this register to determine the number of write channels configured. Value After Reset: 0x2

DSP_PCIE_DMA_WRITE_ENGINE_EN_OFF
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH7 Enable Handshake for DMA Write Engine Channel 7. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
22	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH6 Enable Handshake for DMA Write Engine Channel 5. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
21	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH5 Enable Handshake for DMA Write Engine Channel 5. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
20	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH4 Enable Handshake for DMA Write Engine Channel 4. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
19	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH3 Enable Handshake for DMA Write Engine Channel 3. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
18	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH2 Enable Handshake for DMA Write Engine Channel 2. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
17	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH1 Enable Handshake for DMA Write Engine Channel 1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
16	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH0 Enable Handshake for DMA Write Engine Channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	DMA_WRITE_ENGINE DMA Write Engine Enable. For normal operation, you must initially set this bit to '1', before any other software setup action. You do not need to toggle or rewrite to this bit during normal operation. You should set this bit to '0' when you want to "Soft Reset" the DMA controller write logic. There are three possible reasons for resetting the DMA controller write logic: The "Abort Interrupt Status" bit is set in the DMA Write Interrupt Status Register (DMA_WRITE_INT_STATUS_OFF), and any of the bits in the DMA Write Error Status Register (DMA_WRITE_ERR_STATUS_OFF) are set. Resetting the DMA controller write logic re-initializes the control logic, ensuring that the next DMA write transfer is executed successfully. You have executed the procedure outlined in "Stop Bit", after which, the "Abort Interrupt Status" bit is set and the Channel Status(CS) field of the DMA Write Channel Control 1 Register (DMA_CH_CONTROL1_OFF_WRCH_i) is set to "Stopped". Resetting the DMA controller write logic re-initializes the control logic ensuring that the next DMA write transfer is executed successfully. During software development, when you incorrectly program the DMA write engine. To "Soft Reset" the DMA controller write logic, you must: De-assert the DMA write engine enable bit. Wait for the DMA to complete any in-progress TLP transfer, by waiting until a read on the DMA write engine enable bit returns a '0'. Assert the DMA write engine enable bit. This "Soft Reset" does not clear the DMA configuration registers. The DMA write transfer does not start until you write to the DMA Write Doorbell Register (DMA_WRITE_DOORBELL_OFF). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable (Soft Reset) Value After Reset: 0x0 Testable: untestable Volatile: true

DSP_PCIE_DMA_WRITE_DOORBELL_OFF
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	WR_STOP Stop. Set in conjunction with the Doorbell Number field. The DMA write channel stops issuing requests, sets the channel status to "Stopped", and asserts the "Abort" interrupt if it is enabled. Before setting the Stop bit, you must read the channel Status field (CS) of the DMA Write Channel Control 1 Register (DMA_CH_CONTROL1_OFF_WRCH_0) to ensure that the write channel is "Running" (transferring data). For more information, see "Stopping the DMA Transfer (Software Stop)". Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:3	RO	0x0000000	reserved
2:0	RW	0x0	WR_DOORBELL_NUM Doorbell Number. You must write the channel number to this register to start the DMA write transfer for that channel. The DMA detects a write to this register field even if the value of this field does not change. You do not need to toggle or write any other value to this register to start a new transfer. The range of this field is 0x0 to 0x7, where 0x0 corresponds to channel 0. Note: A write to this field triggers the controller to exit L1 substates. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

DSP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x01	WRITE_CHANNEL3_WEIGHT Channel 3 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
14:10	RW	0x01	WRITE_CHANNEL2_WEIGHT Channel 2 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
9:5	RW	0x01	WRITE_CHANNEL1_WEIGHT Channel 1 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
4:0	RW	0x01	WRITE_CHANNEL0_WEIGHT Channel 0 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1

DSP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x00	WRITE_CHANNEL7_WEIGHT Channel 7 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
14:10	RW	0x00	WRITE_CHANNEL6_WEIGHT Channel 6 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
9:5	RW	0x00	WRITE_CHANNEL5_WEIGHT Channel 5 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
4:0	RW	0x00	WRITE_CHANNEL4_WEIGHT Channel 4 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1

DSP_PCIE_DMA_READ_ENGINE_EN_OFF

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH7 Enable Handshake for DMA Read Engine Channel 7. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
22	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH6 Enable Handshake for DMA Read Engine Channel 6. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
21	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH5 Enable Handshake for DMA Read Engine Channel 5. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
20	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH4 Enable Handshake for DMA Read Engine Channel 4. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
19	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH3 Enable Handshake for DMA Read Engine Channel 3. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
18	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH2 Enable Handshake for DMA Read Engine Channel 2. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
17	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH1 Enable Handshake for DMA Read Engine Channel 1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
16	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH0 Enable Handshake for DMA Read Engine Channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:1	RO	0x0000	reserved
0	RW	0x0	DMA_READ_ENGINE DMA Read Engine Enable. 1: Enable 0: Disable (Soft Reset) For normal operation, you must initially set this bit to "1", before any other software setup actions. You do not need to toggle or rewrite to this bit during normal operation. You should set this field to "0" when you want to "Soft Reset" the DMA controller read logic. There are three possible reasons for resetting the DMA controller read logic: The "Abort Interrupt Status" bit is set (in the "DMA Read Interrupt Status Register" (DMA_READ_INT_STATUS_OFF), and any of the bits in the "DMA Read Error Status Low Register" (DMA_READ_ERR_STATUS_LOW_OFF) is set. Resetting the DMA controller read logic re-initializes the control logic, ensuring that the next DMA read transfer is executed successfully. You have executed the procedure outlined in "Stop Bit", after which, the "Abort Interrupt Status" bit is set and the channel Status field (CS) of the DMA read "DMA Channel Control 1 Register " (DMA_CH_CONTROL1_OFF_WRCH_0) is set to "Stopped". Resetting the DMA controller read logic re-initializes the control logic ensuring that the next DMA read transfer is executed successfully. During software development, when you incorrectly program the DMA read engine. To "Soft Reset" the DMA controller read logic, you must: De-assert the DMA read engine enable bit. Wait for the DMA to complete any in-progress TLP transfer, by waiting until a read on the DMA read engine enable bit returns a "0". Assert the DMA read engine enable bit. This "Soft Reset" does not clear the DMA configuration registers. The DMA read transfer does not start until you write to the "DMA Read Doorbell Register" (DMA_READ_DOORBELL_OFF). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DSP_PCIE_DMA_READ_DOORBELL_OFF
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31	RW	0x0	RD_STOP Stop. Set in conjunction with the Doorbell Number field. The DMA read channel stops issuing requests, sets the channel status to "Stopped", and asserts the "Abort" interrupt if it is enabled. Before setting the Stop bit, you must read the channel Status field (CS) of the DMA Channel Control 1 Register (DMA_CH_CONTROL1_OFF_RDCH_i) to ensure that the read channel is "Running" (transferring data). For more information, see "Stopping the DMA Transfer (Software Stop)". Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:3	RO	0x0000000	reserved
2:0	RW	0x0	RD_DOORBELL_NUM Doorbell Number. You must write 0x0 to this register to start the DMA read transfer for that channel. The DMA detects a write to this register field even if the value of this field does not change. The range of this field is 0x0 to 0x7, where 0x0 corresponds to channel 0. Note: A write to this field triggers the controller to exit L1 substates. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x01	READ_CHANNEL3_WEIGHT Channel 3 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
14:10	RW	0x01	READ_CHANNEL2_WEIGHT Channel 2 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
9:5	RW	0x01	READ_CHANNEL1_WEIGHT Channel 1 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
4:0	RW	0x01	READ_CHANNEL0_WEIGHT Channel 0 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1

DSP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x01	READ_CHANNEL7_WEIGHT Channel 7 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
14:10	RW	0x01	READ_CHANNEL6_WEIGHT Channel 6 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
9:5	RW	0x01	READ_CHANNEL5_WEIGHT Channel 5 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1
4:0	RW	0x01	READ_CHANNEL4_WEIGHT Channel 4 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x1

DSP_PCIE_DMA_WRITE_INT_STATUS_OFF

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	WR_ABORT_INT_STATUS Abort Interrupt Status. The DMA write channel has detected an error, or you manually stopped the transfer as described in "Error Handling Assistance by Remote Software". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA write interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved
7:0	RW	0x00	WR_DONE_INT_STATUS Done Interrupt Status. The DMA write channel has successfully completed the DMA transfer. For more details, see "Interrupts and Error Handling". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA write interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

DSP_PCIE_DMA_WRITE_INT_MASK_OFF
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x3	WR_ABORT_INT_MASK Abort Interrupt Mask. Prevents the Abort interrupt status field in the DMA write interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x3
15:2	RO	0x0000	reserved
1:0	RW	0x3	WR_DONE_INT_MASK Done Interrupt Mask. Prevents the Done interrupt status field in the DMA write interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x3

DSP_PCIE_DMA_WRITE_INT_CLEAR_OFF

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	WR_ABORT_INT_CLEAR Abort Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Abort interrupt status field of the DMA write interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1:0	WO	0x0	WR_DONE_INT_CLEAR Done Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Done interrupt status field of the DMA write interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_WRITE_ERR_STATUS_OFF

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	LINKLIST_ELEMENT_FETCH_ERR_DETECT Linked List Element Fetch Error Detected. The DMA write channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while reading a linked list element from local memory. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Write Interrupt Clear Register (DMA_WRITE_INT_CLEAR_OFF) to clear this error bit. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	APP_READ_ERR_DETECT Application Read Error Detected. The DMA write channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while reading data from it. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Write Interrupt Clear Register (DMA_WRITE_INT_CLEAR_OFF) to clear this error bit. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_WRITE_DONE_IMWR_LOW_OFF
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_DONE_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Done IMWr TLP. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_DONE_IMWR_HIGH_OFF
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_DONE_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Done IMWr TLP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_ABORT_IMWR_LOW_OFF
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_ABORT_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP it generates. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_ABORT_IMWR_HIGH_OFF
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_WRITE_ABORT_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Abort IMWr TLP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_CH01_IMWR_DATA_OFF
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_1_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	WR_CHANNEL_0_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_CH23_IMWR_DATA_OFF
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_3_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 3. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	WR_CHANNEL_2_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 2. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_CH45_IMWR_DATA_OFF
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_5_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 5. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	WR_CHANNEL_4_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 4. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_CH67_IMWR_DATA_OFF
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_7_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 7. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	WR_CHANNEL_6_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 6. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_LINKED_LIST_ERR_EN_OFF

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	WR_CHANNEL_LLLAIE Write Channel LL Local Abort Interrupt Enable (LLLAIE). You enable the write channel local abort interrupt through this bit. The LIE and RIE bits in the LL element enable the write channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:2	RO	0x0000	reserved
1:0	RW	0x0	WR_CHANNEL_LLRAIE Write Channel LL Remote Abort Interrupt Enable (LLRAIE). You enable the write channel remote abort interrupt through this bit. The LIE and RIE bits in the LL element enable the write channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_INT_STATUS_OFF

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	RD_ABORT_INT_STATUS Abort Interrupt Status. The DMA read channel has detected an error, or you manually stopped the transfer as described in "Stopping the DMA Transfer (Software Stop)". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. You can read the DMA Read Error Status Low Register (DMA_READ_ERR_STATUS_LOW_OFF) and DMA Read Error Status High Register (DMA_READ_ERR_STATUS_HIGH_OFF) to determine the source of the error. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA read interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved
7:0	RW	0x00	RD_DONE_INT_STATUS Done Interrupt Status. The DMA read channel has successfully completed the DMA read transfer. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA read interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_READ_INT_MASK_OFF
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x3	RD_ABORT_INT_MASK Abort Interrupt Mask. Prevents the Abort interrupt status field in the DMA read interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x3
15:2	RO	0x0000	reserved
1:0	RW	0x3	RD_DONE_INT_MASK Done Interrupt Mask. Prevents the Done interrupt status field in the DMA read interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x3

DSP_PCIE_DMA_READ_INT_CLEAR_OFF
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	WO	0x00	RD_ABORT_INT_CLEAR Abort Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Abort interrupt status field of the DMA read interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	WO	0x00	RD_DONE_INT_CLEAR Done Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Done interrupt status field of the DMA read interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_READ_ERR_STATUS_LOW_OFF

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	LINK_LIST_ELEMENT_FETCH_ERR_DETECT Linked List Element Fetch Error Detected. The DMA read channel has received an error response from the AXI bus while reading a linked list element from local memory. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this clears all bits in this register, and also the DMA Read Error Status High register (DMA_READ_ERR_STATUS_HIGH_OFF). Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	APP_WR_ERR_DETECT Application Write Error Detected. The DMA read channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while writing data to it. This error is fatal. You must restart the transfer from the beginning, as the channel context is corrupted, and the transfer is not rolled back. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this clears all bits in this register, and also the DMA Read Error Status High register (DMA_READ_ERR_STATUS_HIGH_OFF). Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_READ_ERR_STATUS_HIGH_OFF

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DATA_POISIONING Data Poisoning. The DMA read channel has detected data poisoning in the completion from the remote device (in response to the MRd request). The DMA read channel will drop the completion and then be halted. The CX_FLT_MASK_UR_POIS filter rule does not affect this behavior. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	CPL_TIMEOUT Completion Time Out. The DMA read channel has timed-out while waiting for the remote device to respond to the MRd request, or a malformed CplD has been received. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling" . Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	CPL_ABORT Completer Abort. The DMA read channel has received a PCIe completer abort completion status from the remote device in response to the MRd request. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
7:0	RO	0x00	UNSUPPORTED_REQ Unsupported Request. The DMA read channel has received a PCIe unsupported request completion status from the remote device in response to the MRd request. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_READ_LINKED_LIST_ERR_EN_OFF
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	RD_CHANNEL_LLLAIE Read Channel LL Local Abort Interrupt Enable (LLLAIE). You enable the read channel Local Abort interrupt through this bit. The LIE and RIE bits in the LL element enable the read channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:1	RO	0x0000	reserved
0	RW	0x0	RD_CHANNEL_LLRAIE Read Channel LL Remote Abort Interrupt Enable (LLRAIE). You enable the read channel Remote Abort interrupt through this bit. The LIE and RIE bits in the LL element enable the read channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_DONE_IMWR_LOW_OFF
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_DONE_LOW_REG The DMA uses this field to generate bits [63:32] of the address field for the Done IMWr TLP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_DONE_IMWR_HIGH_OFF

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_DONE_HIGH_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_ABORT_IMWR_LOW_OFF

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_ABORT_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_ABORT_IMWR_HIGH_OFF

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_ABORT_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Abort IMWr TLP. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_CH01_IMWR_DATA_OFF

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_1_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	RD_CHANNEL_0_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 0. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_CH23_IMWR_DATA_OFF
Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_3_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 2. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x
15:0	RW	0x0000	RD_CHANNEL_2_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 2. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x

DSP_PCIE_DMA_READ_CH45_IMWR_DATA_OFF
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_5_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 5. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	RD_CHANNEL_4_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 4. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_READ_CH67_IMWR_DATA_OFF

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_7_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 7. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	RD_CHANNEL_6_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 6. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_LOW_OFF

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH3 DMA handshake counter for DMA Write Engine Channel 3. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH2 DMA handshake counter for DMA Write Engine Channel 2. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH1 DMA handshake counter for DMA Write Engine Channel 1. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH0 DMA handshake counter for DMA Write Engine Channel 0. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH7 DMA handshake counter for DMA Write Engine Channel 7. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH6 DMA handshake counter for DMA Write Engine Channel 6. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH5 DMA handshake counter for DMA Write Engine Channel 5. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH4 DMA handshake counter for DMA Write Engine Channel 4. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

DSP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH3 DMA handshake counter for DMA Read Engine Channel 3. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH2 DMA handshake counter for DMA Read Engine Channel 2. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH1 DMA handshake counter for DMA Read Engine Channel 1. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH0 DMA handshake counter for DMA Read Engine Channel 0. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

DSP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH7 DMA handshake counter for DMA Read Engine Channel 7. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH6 DMA handshake counter for DMA Read Engine Channel 6. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH5 DMA handshake counter for DMA Read Engine Channel 5. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH4 DMA handshake counter for DMA Read Engine Channel 4. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

DSP_PCIE_DMA_WRITE_CHi_PWR_EN_OFF
Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_WRITE_CH0_PWR_EN DMA Write Channel 0 Power enable/disable. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0

DSP_PCIE_DMA_READ_CHi_PWR_EN_OFF
Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_READ_CH0_PWR_EN DMA Read Channel 0 Power enable/disable. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0

DSP_PCIE_DMA_CH_CONTROL1_OFF_WRCH_i
Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	DMA_AT Address Translation TLP Header Bit (AT). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
29:27	RW	0x0	DMA_TC Traffic Class TLP Header Bit (TC). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
26	RO	0x0	reserved
25	RW	0x0	DMA_RO Relaxed Ordering TLP Header Bit (RO). DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
24	RW	0x0	DMA_NS_SRC Source No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MRd (SAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23	RW	0x0	DMA_NS_DST Destination No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MWr (DAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
22	RW	0x0	DMA_MEM_TYPE Master AXI ACE-Lite Cache Coherency Control. This field sets the DMA channel memory type of the address space of the data transfer as follows: For more details, see "ACE-Lite Features and Limitations" section of the Databook. Irrespective of the value of this field, Linked list descriptor requests have this attribute set to 0x1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (PERIPHERAL): peripheral type 0x1 (MEM_TYPE): memory type Value After Reset: 0x0 Testable: writeAsRead Volatile: true
21:17	RO	0x00	reserved
16:12	RW	0x00	DMA_FUNC_NUM Function Number (FN). The controller uses this field when generating the requester ID for the MRd/MWr DMA TLP. When you have enabled SR-IOV, then this field is ignored if you have set the VFE field in the "DMA Write Channel Control 2 Register" (DMA_CH_CONTROL2_OFF_WRCH_0). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	LLE Linked List Enable (LLE). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x1 (ENABLE): Enable linked list operation 0x0 (DISABLE): Disable linked list operation Value After Reset: 0x0 Testable: writeAsRead Volatile: true
8	RW	0x0	CCS Consumer Cycle State (CCS). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". You must initialize this bit. The DMA updates this bit during linked list operation. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RO	0x0	CS Channel Status (CS). The channel status bits identify the current operational state of the DMA channel. The operation state encoding for each DMA channel is a s follows: Values: 0x0 (RESERVED): Reserved 0x1 (RUNNING): This channel is active and transferring data 0x2 (HALTED): An error condition has been detected, and the DMA has stopped this channel 0x3 (STOPPED): The DMA has transferred all data for this channel, or you have prematurely stopped this channel by writing to the Stop field of the DMA Write Doorbell Register (DMA_WRITE_DOORBELL_OFF) or DMA Read Doorbell Register (DMA_READ_DOORBELL_OFF) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	RW	0x0	RIE Remote Interrupt Enable (RIE). You must set this bit to enable the generation of the Done or Abort Remote interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the RIE of the LL element. The RIE bit in a LL element only enables the Done interrupt. In non-LL mode, the RIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	LIE Local Interrupt Enable (LIE). You must set this bit to enable the generation of the Done or Abort Local interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the LIE of the LL element. The LIE bit in a LL element only enables the Done interrupt. In non-LL mode, the LIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RW	0x0	LLP Load Link Pointer (LLP). Used in linked list mode only. Indicates that this linked list element is a link element, and its LL element pointer dwords are pointing to the next (non-contiguous) element. The DMA loads this field with the LLP of the linked list element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	RW	0x0	TCB Toggle Cycle Bit (TCB). Indicates to the DMA to toggle its interpretation of the CB. Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the TCB of the linked list element. this field is not defined in a data LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	CB Cycle Bit (CB). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the CB of the linked list element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_TRANSFER_SIZE_OFF_WRCH_i
Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_TRANSFER_SIZE DMA Transfer Size. You program this register with the size of the DMA transfer. The maximum DMA transfer size is 4Gbytes. The minimum transfer size is one byte (0x1). This field is automatically decremented by the DMA as the DMA write channel transfer progresses. This field indicates the number bytes remaining to be transferred. When all bytes are successfully transferred the current transfer size is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element. You can read this register to monitor the transfer progress, however in some scenarios this register is updated after a delay. For example, when less than 3 channels are doorbelled, this register is updated only after a descriptor finishes(linked list mode), or the transfer ends (non-linked list mode). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_SAR_LOW_OFF_WRCH_i
Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_LOW Source Address Register (lower 32 bits). Indicates the next address to be read from. The DMA increments the SAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The SAR is the address of the remote memory. DMA Write: The SAR is the address of the local memory. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_SAR_HIGH_OFF_WRCH_i
Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_HIGH Source Address Register (higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_DAR_LOW_OFF_WRCH_i
Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_LOW Destination Address Register (lower 32 bits). Indicates the next address to be written to. The DMA increments the DAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The DAR is the address of the local memory. DMA Write: The DAR is the address of the remote memory. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_DAR_HIGH_OFF_WRCH_i
Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_HIGH Destination Address Register (Higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

DSP_PCIE_DMA_LLP_LOW_OFF_WRCH_i
Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_LOW Lower bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list after the previous element is consumed. When the current element is a data element; this field is incremented by 6 DWORDS. When the current element is a link element; this field is overwritten by the LL Element Pointer of the element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_LLP_HIGH_OFF_WRCH_i
Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_HIGH Higher 32 bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list as elements are consumed. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_CH_CONTROL1_OFF_RDCH_i
Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	DMA_AT Address Translation TLP Header Bit (AT). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
29:27	RW	0x0	DMA_TC Traffic Class TLP Header Bit (TC). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
26	RO	0x0	reserved
25	RW	0x0	DMA_RO Relaxed Ordering TLP Header Bit (RO) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
24	RW	0x0	DMA_NS_SRC Source No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MRd (SAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23	RW	0x0	DMA_NS_DST Destination No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MWr (DAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
22	RW	0x0	DMA_MEM_TYPE Master AXI ACE-Lite Cache Coherency Control. This field sets the DMA channel memory type of the address space of the data transfer as follows: For more details, see "ACE-Lite Features and Limitations" section of the Databook. Irrespective of the value of this field, Linked list descriptor requests have this attribute set to 0x1. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x0 (PERIPHERAL): peripheral 0x1 (MEM_TYPE): main memory Value After Reset: 0x0 Testable: writeAsRead Volatile: true
21:17	RO	0x00	reserved

Bit	Attr	Reset Value	Description
16:12	RW	0x00	DMA_FUNC_NUM Function Number (FN). The controller uses this field when generating the requester ID for the MRd/MWr DMA TLP. When you have enabled SR-IOV, then this field is ignored if you have set the VFE field in the DMA Read Channel Control 2 Register (DMA_CH_CONTROL2_OFF_RDCH_0). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:10	RO	0x0	reserved
9	RW	0x0	LLE Linked List Enable (LLE). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Values: 0x1 (ENABLE): Enable linked list operation 0x0 (DISABLE): Disable linked list operation Value After Reset: 0x0 Testable: writeAsRead Volatile: true
8	RW	0x0	CCS Consumer Cycle State (CCS). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". You must initialize this bit. The DMA updates this bit during linked list operation. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RO	0x0	CS Channel Status (CS). The channel status bits identify the current operational state of the DMA channel. The operation state encoding for each DMA channel is a s follows: Values: 0x0 (RSVD): Reserved 0x1 (RUN): Running. This channel is active and transferring data. 0x2 (HALT): Halted. An error condition has been detected, and the DMA has stopped this channel. 0x3 (STOP): Stopped. The DMA has transferred all data for this channel, or you have prematurely stopped this channel by writing to the Stop field of the DMA Read Doorbell Register (DMA_WRITE_DOORBELL_OFF) or DMA Read Doorbell Register (DMA_READ_DOORBELL_OFF). Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	RW	0x0	RIE Remote Interrupt Enable (RIE). You must set this bit to enable the generation of the Done or Abort Remote interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the RIE of the LL element. The RIE bit in a LL element only enables the Done interrupt. In non-LL mode, the RIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	LIE Local Interrupt Enable (LIE). You must set this bit to enable the generation of the Done or Abort Local interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the LIE of the LL element. The LIE bit in a LL element only enables the Done interrupt. In non-LL mode, the LIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RW	0x0	LLP Load Link Pointer (LLP). Used in linked list mode only. Indicates that this linked list element is a link element, and its LL element pointer dwords are pointing to the next (non-contiguous) element. The DMA loads this field with the LLP of the linked list element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	RW	0x0	TCB Toggle Cycle Bit (TCB). Indicates to the DMA to toggle its interpretation of the CB. Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the TCB of the linked list element. this field is not defined in a data LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
0	RW	0x0	CB Cycle Bit (CB). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the CB of the linked list element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_TRANSFER_SIZE_OFF_RDCH_i
Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_TRANSFER_SIZE DMA Transfer Size. You program this register with the size of the DMA transfer. The maximum DMA transfer size is 4Gbytes. The minimum transfer size is one byte (0x1). This field is automatically decremented by the DMA as the DMA read channel transfer progresses. This field indicates the number bytes remaining to be transferred. When all bytes are successfully transferred the current transfer size is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element. You can read this register to monitor the transfer progress, however in some scenarios this register is updated after a delay. For example, when less than 3 channels are doorbelled, this register is updated only after a descriptor finishes(linked list mode), or the transfer ends (non-linked list mode). Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_SAR_LOW_OFF_RDCH_i
Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_LOW Source Address Register (Lower 32 bits). Indicates the next address to be read from. The DMA increments the SAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The SAR is the address of the remote memory. DMA Read: The SAR is the address of the local memory. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_SAR_HIGH_OFF_RDCH_i

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_HIGH Source Address Register (higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_DAR_LOW_OFF_RDCH_i

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_LOW Destination Address Register (Lower 32 bits). Indicates the next address to be written to. The DMA increments the DAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The DAR is the address of the local memory. DMA Read: The DAR is the address of the remote memory. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_DAR_HIGH_OFF_RDCH_i
Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_HIGH Destination Address Register (higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_LLP_LOW_OFF_RDCH_i
Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_LOW Lower bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list after the previous element is consumed. When the current element is a data element; this field is incremented by 6 DWORDS. When the current element is a link element; this field is overwritten by the LL Element Pointer of the element. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

DSP_PCIE_DMA_LLP_HIGH_OFF_RDCH_i
Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_HIGH Higher 32 bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list as elements are consumed. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

11.4.4 Upstream Port Register

11.4.4.1 USP_PCIE_TYPE0 Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_TYPE0_DEVICE_ID_VENDOR_ID_REG	0x0000	W	0x35881D87	Device ID and Vendor ID Register
USP_PCIE_TYPE0_STATUS_COMMAND_REG	0x0004	W	0x00100000	Status and Command Register
USP_PCIE_TYPE0_CLASS_CODE_REVISION_ID	0x0008	W	0x00000001	Class Code and Revision ID Register
USP_PCIE_TYPE0_BIST_HEADER_TYPE_LATENCY_CACHE_LINE_SIZE_REG	0x000C	W	0x00000000	BIST, Header Type, Latency Timer, and Cache Line Size Register
USP_PCIE_TYPE0_BAR0_REG	0x0010	W	0x00000000	BAR0 Register

Name	Offset	Size	Reset Value	Description
USP_PCIE_TYPE0_BAR1_REG	0x0014	W	0x00000000	BAR1 Register
USP_PCIE_TYPE0_BAR2_REG	0x0018	W	0x00000000	BAR2 Register
USP_PCIE_TYPE0_BAR3_REG	0x001C	W	0x00000000	BAR3 Register
USP_PCIE_TYPE0_BAR4_REG	0x0020	W	0x00000000	BAR4 Register
USP_PCIE_TYPE0_BAR5_REG	0x0024	W	0x00000000	BAR5 Register
USP_PCIE_TYPE0_CARDBUS_CIS_PTR_REG	0x0028	W	0x00000000	CardBus CIS Pointer Register
USP_PCIE_TYPE0_SUBSYSTEM_ID_SUBSYSTEM_VENDOR_ID_REG	0x002C	W	0x00000000	Subsystem ID and Subsystem Vendor ID Register
USP_PCIE_TYPE0_EXP_ROM_BASE_ADDR_REG	0x0030	W	0x00000000	Expansion ROM BAR Register
USP_PCIE_TYPE0_PCI_CAP_PTR_REG	0x0034	W	0x00000040	Capabilities Pointer Register
USP_PCIE_TYPE0_MAX_LATENCY_MIN_GRANT_INTERRUPT_PIN_INTERRUPT_LIN	0x003C	W	0x000001FF	Max_Lat, Min_Gnt, Interrupt Pin, and Interrupt Line Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.2 USP_PCIE_TYPE0 Detail Registers Description

USP_PCIE_TYPE0_DEVICE_ID_VENDOR_ID_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x3588	PCI_TYPE0_DEVICE_ID Device ID. The Device ID register identifies the particular Function. This identifier is allocated by the vendor. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.
15:0	RW	0x1d87	PCI_TYPE0_VENDOR_ID Vendor ID. The Vendor ID register identifies the manufacturer of the Function. Valid vendor identifiers are allocated by the PCI-SIG to ensure uniqueness. It is not permitted to populate this register with a value of FFFFh, which is an invalid value for Vendor ID. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky.

USP_PCIE_TYPE0_STATUS_COMMAND_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	W1C	0x0	DETECTED_PARITY_ERR Detected Parity Error. Values: 0x1 (SET): This bit is set by a Function whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response bit in the Command register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30	W1C	0x0	SIGNALED_SYS_ERR Signaled System Error. Values: 0x1 (SET): This bit is set when a Function sends an ERR_FATAL or ERR_NONFATAL message, and the SERR# Enable bit in the Command register is 1b. For Functions that do not send ERR_FATAL or ERR_NONFATAL messages, the controller hardwires this bit to 0b. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
29	W1C	0x0	RCVD_MASTER_ABORT Received Master Abort. Values: 0x1 (SET): This bit is set when a Requester receives a Completion with Unsupported Request Completion Status. For Functions that do not make Non-Posted Requests on their own behalf, the controller hardwires this bit to 0b. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
28	W1C	0x0	RCVD_TARGET_ABORT Received Target Abort. Values: 0x1 (SET): This bit is set when a Requester receives a Completion with Completer Abort Completion Status. For Functions that do not make Non-Posted Requests on their own behalf, the controller hardwires this bit to 0b. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
27	W1C	0x0	SIGNALED_TARGET_ABORT Signaled Target Abort. Values: 0x1 (SET): This bit is set when a Function completes a Posted or Non-Posted Request as a Completer Abort error. The controller hardwires this bit to 0b for Functions that do not signal Completer Abort. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
26:25	RO	0x0	DEV_SEL_TIMING DEVSEL Timing. This field was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this field to 00b.
24	W1C	0x0	MASTER_DPE Master Data Parity Error. This bit is set by a Function if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs: Function receives a Poisoned Completion Function transmits a Poisoned Request If the Parity Error Response bit is 0b, this bit is never set. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23	RO	0x0	FAST_B2B_CAP Fast Back to Back Transaction Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x
22	RO	0x0	reserved

Bit	Attr	Reset Value	Description
21	RO	0x0	FAST_66MHZ_CAP 66MHz Capable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0
20	RO	0x1	CAP_LIST Capabilities List. Indicates the presence of an Extended Capability list item. Since all PCI Express device Functions are required to implement the PCI Express Capability structure, the controller hardwires this bit to 1b. Value After Reset: 0x1
19	RO	0x0	INT_STATUS Emulation interrupt pending. When set, indicates that an INTx emulation interrupt is pending internally in the Function. Setting the Interrupt Disable bit has no effect on the state of this bit. For Functions that do not generate INTx interrupts, the controller hardwires this bit to 0b. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
18:11	RO	0x00	reserved
10	RW	0x0	PCI_TYPE0_INT_EN Interrupt Disable. Controls the ability of a Function to generate INTx emulation interrupts. When set, Functions are prevented from asserting INTx interrupts. Note: Any INTx emulation interrupts already asserted by the Function must be de-asserted when this bit is Set. INTx interrupts use virtual wires that must, if asserted, be de-asserted using the appropriate Deassert_INTx message(s) when this bit is set. Only the INTx virtual wire interrupt(s) associated with the Function(s) for which this bit is set are affected. For functions that generate INTx interrupts, this bit is required. For functions that do not generate INTx interrupts, this bit is optional. Value After Reset: 0x0
9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	PCI_TYPE0_SERREN SERR# Enable. When set, this bit enables reporting upstream of Non-fatal and Fatal errors detected by the Function. Note: The errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control register. Value After Reset: 0x0
7	RO	0x0	PCI_TYPE_IDSEL_STEPPING IDSEL Stepping/Wait Cycle Control. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0
6	RW	0x0	PCI_TYPE0_PARITY_ERR_EN Parity Error Response. This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Status register. Value After Reset: 0x0
5	RO	0x0	PCI_TYPE_VGA_PALETTE_SNOOP VGA Palette Snoop. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge architecture specification. Its functionality does not apply to PCI Express, the controller hardwires this bit to 0b. Value After Reset: 0x0
4	RO	0x0	PCI_TYPE_MWI_ENABLE Memory Write and Invalidate. This bit was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge architecture specification. Its functionality does not apply to PCI Express, the controller hardwires this bit to 0b. Value After Reset: 0x0
3	RO	0x0	PCI_TYPE0_SPECIAL_CYCLE_OPERATION Special Cycle Enable. This bit was originally described in the PCI Local Bus Specification. Its functionality does not apply to PCI Express. The controller hardwires this bit to 0b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	PCI_TYPE0_BUS_MASTER_EN Bus Master Enable. Controls the ability of a Function to issue Memory and I/O Read/Write requests. When this bit is set, the Function is allowed to issue Memory or I/O Requests. When this bit is clear, the Function is not allowed to issue any Memory or I/O Requests. Requests other than Memory or I/O Requests are not controlled by this bit. Note: MSI/MSI-X interrupt Messages are in-band memory writes, setting the Bus Master Enable bit to 0b disables MSI/MSI-X interrupt Messages as well. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
1	RW	0x0	PCI_TYPE0_MEM_SPACE_EN Memory Space Enable. Controls a Function's response to Memory Space accesses. When this bit is set, the Function is enabled to decode the address and further process Memory Space accesses. When this bit is clear, all received Memory Space accesses are caused to be handled as Unsupported Requests. For a Function does not support Memory Space accesses, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: !has_mem_bar ? RO : RW Dbi: !has_mem_bar ? RO : RW Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	PCI_TYPE0_IO_EN IO Space Enable. Controls a Function's response to I/O Space accesses. When this bit is set, the Function is enabled to decode the address and further process I/O Space accesses. When this bit is clear, all received I/O accesses are caused to be handled as Unsupported Requests. For a Function that does not support I/O Space accesses, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: !has_io_bar ? RO : RW Dbi: !has_io_bar ? RO : RW Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_CLASS_CODE_REVISION_ID

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BASE_CLASS_CODE Base Class Code. A code that broadly classifies the type of operation the Function performs. Encodings for base class, are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are Reserved. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
23:16	RW	0x00	SUBCLASS_CODE Sub-Class Code. Specifies a base class sub-class, which identifies more specifically the operation of the Function. Encodings for sub-class are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are Reserved. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:8	RW	0x00	PROGRAM_INTERFACE Programming Interface. This field identifies a specific register-level programming interface (if any) so that device independent software can interact with the Function. Encodings for interface are provided in the PCI Code and ID Assignment Specification. All unspecified encodings are Reserved. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
7:0	RW	0x01	REVISION_ID Revision ID. The value in this register specifies a Function specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Revision ID should be viewed as a vendor defined extension to the Device ID. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

USP_PCIE_TYPE0_BIST_HEADER_TYPE_LATENCY_CACHE_LINE_SIZE_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	BIST BIST. This register is used for control and status of BIST. For Functions that do not support BIST the controller hardwires the register to 00h. A Function whose BIST is invoked must not prevent normal operation of the PCI Express Link. Bit descriptions: [31]: BIST Capable. When Set, this bit indicates that the Function supports BIST. When Clear, the Function does not support BIST. [30]: Start BIST. If BIST Capable is Set, Set this bit to invoke BIST. The Function resets the bit when BIST is complete. Software is permitted to fail the device if this bit is not Clear (BIST is not complete) 2 seconds after it had been Set. Writing this bit to 0b has no effect. This bit must be hardwired to 0b if BIST Capable is Clear. [29:28]: Reserved. [27:24]: Completion Code. This field encodes the status of the most recent test. A value of 0000b means that the Function has passed its test. Non-zero values mean the Function failed. Function-specific failure codes can be encoded in the non-zero values. This field's value is only meaningful when BIST Capable is Set and Start BIST is Clear. This field must be hardwired to 0000b if BIST Capable is clear. Value After Reset: 0x0
23	RW	0x0	MULTI_FUNC Multi-Function Device. Except where stated otherwise, it is recommended that this bit be set if there are multiple Functions, and clear if there is only one Function. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): Indicates that the Device may contain multiple Functions, but not necessarily. Software is permitted to probe for Functions other than Function 0 0x0 (CLEAR): Software must not probe for Functions other than Function 0 unless explicitly indicated by another mechanism, such as an ARI or SR-IOV Capability structure. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
22:16	RO	0x00	HEADER_TYPE Header Layout. This field identifies the layout of the second part of the predefined header. The controller uses 000 0000b encoding. Value After Reset: 0x0
15:8	RO	0x00	LATENCY_MASTER_TIMER Latency Timer. The Latency Timer was originally described in the PCI Local Bus Specification and the PCI-to-PCI Bridge Architecture Specification. Its functionality does not apply to PCI Express. The controller hardwires this register to 00h. Value After Reset: 0x0
7:0	RW	0x00	CACHE_LINE_SIZE Cache Line Size. The Cache Line Size register is programmed by the system firmware or the operating system to system cache line size. However, legacy conventional PCI software may not always be able to program this register correctly especially in the case of Hot-Plug devices. This read-write register is implemented for legacy compatibility purposes but has no effect on any PCI Express device behavior. Value After Reset: 0x0

USP_PCIE_TYPE0_BAR0_REG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR0_START BAR0 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: R(Sticky)/W(Sticky) if enabled else R(Sticky) Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	BAR0_PREFETCH BAR0 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:1	RW	0x0	BAR0_TYPE BAR0 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	BAR0_MEM_IO BAR0 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_BAR1_REG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR1_START BAR1 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: R(Sticky)/W(Sticky) if enabled else R(Sticky) Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	BAR1_PREFETCH BAR1 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:1	RW	0x0	BAR1_TYPE BAR1 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	BAR1_MEM_IO BAR1 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_BAR2_REG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR2_START BAR2 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: R(Sticky)/W(Sticky) if enabled else R(Sticky) Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	BAR2_PREFETCH BAR2 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:1	RW	0x0	BAR2_TYPE BAR2 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	BAR2_MEM_IO BAR2 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_BAR3_REG
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR3_START BAR3 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: R(Sticky)/W(Sticky) if enabled else R(Sticky) Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	BAR3_PREFETCH BAR3 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:1	RW	0x0	BAR3_TYPE BAR3 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	BAR3_MEM_IO BAR3 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_BAR4_REG

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR4_START BAR4 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: R(Sticky)/W(Sticky) if enabled else R(Sticky) Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RO	0x0	BAR4_PREFETCH BAR4 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:1	RO	0x0	BAR4_TYPE BAR4 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RO	0x0	BAR4_MEM_IO BAR4 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_BAR5_REG

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	BAR5_START BAR5 Base Address. Memory Space: Base Address. IO Space: bits[31:2] are used to map the function into IO space/Base. Address. Note: The access attributes of this field are as follows: Wire: R(Sticky)/W(Sticky) if enabled else R(Sticky) Dbi: R(Sticky)/W(Sticky) if enabled else R(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	BAR5_PREFETCH BAR5 Prefetchable. Memory Space: Set to one if data is prefetchable. A Function is permitted to mark a range as prefetchable. If there are no side effects on reads, the function returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors. Bit must me clear otherwise. IO Space: Not applicable Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:1	RW	0x0	BAR5_TYPE BAR5 Type. Memory Space: Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space). The encodings defined in Values: apply. IO Space: Bit 1 is reserved and must return 0b on reads. Bits[31:2] are used to map the function into IO space. The encodings defined in Values: do not apply. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Values: 0x0 (BAR_32): Base register is 32 bits wide and can be mapped anywhere in the 32 address bit Memory Space. 0x1 (RSVD_1): Reserved. 0x2 (BAR_64): Base register is 64 bits wide and can be mapped anywhere in the 64 address bit Memory Space. 0x3 (RSVD_2): Reserved. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	BAR5_MEM_IO BAR5 Memory Space Indicator. This bit is used to determine whether the register maps into Memory or I/O Space. Base Address registers that map to Memory Space must return a 0b. Base Address registers that map to I/O Space must return a 1b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (BAR_ENABLED == 1) then (if [DBI_RO_WR_EN == 1] then R(Sticky)/W(Sticky) else R(Sticky)) else RO(Sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_CARDBUS_CIS_PTR_REG
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CARDBUS_CIS_POINTER CardBus CIS Pointer. Its functionality does not apply to PCI Express. It must be hardwired to 0000 0000h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

USP_PCIE_TYPE0_SUBSYSTEM_ID_SUBSYSTEM_VENDOR_ID_REG
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	SUBSYS_DEV_ID Subsystem ID. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	SUBSYS_VENDOR_ID Subsystem Vendor ID. Subsystem Vendor IDs can be obtained from the PCI SIG and are used to identify the vendor of the add-in card or subsystem. Values for the Subsystem ID are vendor-specific. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

USP_PCIE_TYPE0_EXP_ROM_BASE_ADDR_REG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	EXP_ROM_BASE_ADDRESS Expansion ROM Base Address. Upper 21 bits of the Expansion ROM base address. The number of bits (out of these 21) that a Function actually implements depends on how much address space the Function requires. Note: The access attributes of this field are as follows: Wire: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R Value After Reset: 0x0 Testable: writeAsRead Volatile: true
10:5	RO	0x00	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ROM_BAR_VALIDATION_DETAILS Expansion ROM Validation Details. The field contains optional, implementation-specific details associated with Expansion ROM Validation. If validation is in progress (Expansion ROM Validation Status is 001b), non-zero values of this field represent implementation-specific indications of the phase of the validation progress (for example, 50% complete). The value 0000b indicates that no validation progress information is provided. If validation is completed (Expansion ROM Validation Status 010b to 111b inclusive), non-zero values in this field represent additional implementation-specific information. The value 0000b indicates that no information is provided. When validation is supported and this field is not implemented, this field must be hardwired to 0000b. Note: The access attributes of this field are as follows: Wire: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3:1	RW	0x0	ROM_BAR_VALIDATION_STATUS Expansion ROM Validation Status. When this field is non-zero, it indicates the status of hardware validation of the Expansion ROM contents. If the Function does not support validation, this field must be hardwired to 000b. It is optional whether an implementation is capable of returning Validation Status values 011b, 101b, 110b, or 111b. Note: The access attributes of this field are as follows: Wire: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1 && DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (ZERO): Validation not supported. 0x1 (ONE): Validation in Progress. 0x2 (TWO): Validation Pass Valid contents, trust test was not performed. 0x3 (THREE): Validation Pass Valid and trusted contents. 0x4 (FOUR): Validation Fail Invalid contents. 0x5 (FIVE): Validation Fail Valid but untrusted contents (e.g., Out of Date, Expired or Revoked Certificate). 0x6 (SIX): Warning Pass Validation Passed with implementation-specific warning. Valid contents, trust test was not performed. 0x7 (SEVEN): Warning Pass Validation Passed with implementation-specific warning. Valid and trusted contents. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RO	0x0	ROM_BAR_ENABLE Expansion ROM Enable. This bit controls whether or not the Function accepts accesses to its expansion ROM. The Memory Space Enable bit in the Command register has precedence over the Expansion ROM Enable bit. A Function must claim accesses to its expansion ROM only if both the Memory Space Enable bit and the Expansion ROM Enable bit are set. Note: The access attributes of this field are as follows: Wire: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R Dbi: if (EXP_ROM_BAR_MASK_REG.ROM_BAR_ENABLED == 1) then R/W else R Values: 0x1 (ONE): When the bit is 1b, address decoding is enabled using the parameters in the other part of the Expansion ROM Base Address register. 0x0 (ZERO): When this bit is 0b, the Function's expansion ROM address space is disabled. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_TYPE0_PCI_CAP_PTR_REG
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x40	CAP_POINTER Capabilities Pointer. This register points to a valid capability structure. Either this structure is the PCI Express Capability structure, or a subsequent list item points to the PCI Express Capability structure. The bottom two bits are reserved, the controller sets it to 00b. Software must mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x40 Testable: unconstrained

USP_PCIE_TYPE0_MAX_LATENCY_MIN_GRANT_INTERRUPT_PIN_INTERRUPT_LIN
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x01	INT_PIN Interrupt Pin. The Interrupt Pin register identifies the legacy interrupt Message(s) the Function uses. All encodings other than the defined encodings are reserved. PCI Express defines one legacy interrupt Message for a single Function device and up to four legacy interrupt Messages for a multi-Function device. For a single Function device, only INTA may be used. Any Function on a multi-Function device can use any of the INTx Messages. If a device implements a single legacy interrupt Message, it must be INTA; if it implements two legacy interrupt Messages, they must be INTA and INTB; and so forth. For a multi-Function device, all Functions may use the same INTx Message or each may have its own (up to a maximum of four Functions) or any combination thereof. A single Function can never generate an interrupt request on more than one INTx Message. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (INTA): Map to legacy interrupt Messages for INTA 0x2 (INTB): Map to legacy interrupt Messages for INTB 0x3 (INTC): Map to legacy interrupt Messages for INTC 0x4 (INTD): Map to legacy interrupt Messages for INTD 0x0 (NO_INT): Indicates that the Function uses no legacy interrupt Message(s). Value After Reset: 0x1 Testable: unconstrained
7:0	RW	0xff	INT_LINE Interrupt Line. The Interrupt Line register communicates interrupt line routing information. The register must be implemented by any Function that uses an interrupt pin. Values in this register are programmed by system software and are system architecture specific. The Function itself does not use this value; rather the value in this register is used by device drivers and operating systems. Value After Reset: 0xff

11.4.4.3 USP_PCIE_PM Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_PM_CAP_ID_NXT_PTR_REG	0x0000	W	0x07C35001	Power Management Capabilities Register
USP_PCIE_PM_CON_STATUS_REG	0x0004	W	0x00000008	Power Management Control and Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

Double WORD (64 bits) access

11.4.4.4 USP_PCIE_PM Detail Registers Description

USP_PCIE_PM_CAP_ID_NXT_PTR_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	PME_SUPPORT PME_Support. This 5-bit field indicates the power states in which the function may generate a PME and/or forward PME messages. A value of 0b for any bit indicates that the function is not capable of asserting PME while in that power state. bit(27) X XXX1b - PME can be generated from D0 bit(28) X XX1Xb - PME can be generated from D1 bit(29) X X1XXb - PME can be generated from D2 bit(30) X 1XXXb - PME can be generated from D3hot bit(31) 1 XXXXb - PME can be generated from D3cold Bit 31 (PME can be asserted from D3cold) represents a special case. Functions that set this bit require some sort of auxiliary power source. Implementation specific mechanisms are recommended to validate that the power source is available before setting this bit. Each bit that corresponds to a supported D-state must be set for PCI-PCI Bridge structures representing Ports on Root Complexes/Switches to indicate that the Bridge will forward PME Messages. Bit 31 must only be set if the Port is still able to forward PME Messages when main power is not available. The read value from this field is the write value && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where D1_SUPPORT and D2_SUPPORT are fields in this register. The reset value PME_SUPPORT_n && (sys_aux_pwr_det, 1'b1, D2_SUPPORT, D1_SUPPORT, 1'b1), where PME_SUPPORT_n is a configuration parameter. Note: The access attributes of this field are as follows: Wire: R Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1b Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
26	RW	0x1	D2_SUPPORT D2_Support. If this bit is set, this function supports the D2 Power Management state. Functions that do not support D2 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
25	RW	0x1	D1_SUPPORT D1_Support. If this bit is set, this function supports the D1 Power Management state. Functions that do not support D1 must always return a value of 0b for this bit. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
24:22	RW	0x7	AUX_CURR Aux_Current. This 3 bit field reports the Vaux auxiliary current requirements for the function. If this function implements the Data Register, the controller hardwires this field to 000b. If PME_Support is 0 xxxxb (PME assertion from D3cold is not supported), the controller hardwires this field to 0000b. For functions where PME_Support is 1 xxxxb (PME assertion from D3cold is supported), and which do not implement the Data field, the encodings defined in Values: apply: Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x7 (_370mA_): 375mA Vaux Max. Current Required 0x6 (_320mA_): 320mA Vaux Max. Current Required 0x5 (_270mA_): 270mA Vaux Max. Current Required 0x4 (_220mA_): 220mA Vaux Max. Current Required 0x3 (_160mA_): 160mA Vaux Max. Current Required 0x2 (_100mA_): 100mA Vaux Max. Current Required 0x1 (_055mA_): 55mA Vaux Max. Current Required 0x0 (SELF_): 0 self powered Value After Reset: 0x7 Testable: unconstrained
21	RW	0x0	DSI Device Specific Initialization. The DSI bit indicates whether special initialization of this function is required. When set, indicates that the function requires a device specific initialization sequence following a transition to the D0uninitialized state. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19	RO	0x0	PME_CLK PME Clock. Does not apply to PCI Express, the controller hardwires it to 0b. Note: This register field is sticky. Value After Reset: 0x0
18:16	RW	0x3	PM_SPEC_VER Version. This field provides the Power Management specification version. The controller hardwires this field to 011b for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0>. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x3 Testable: unconstrained
15:8	RW	0x50	PM_NEXT_POINTER Next Capability Pointer. This field provides an offset into the function's configuration space pointing to the location of next item in the capabilities list. If there are no additional items in the capabilities list, this field is set to 00h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x50 Testable: unconstrained
7:0	RO	0x01	PM_CAP_ID Capability ID. This field returns 01h to indicate that this is the PCI Power Management Capability. Each function may have only one item in its capability list with Capability ID set to 01h. Value After Reset: 0x1

USP_PCIE_PM_CON_STATUS_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DATA_REG_ADD_INFO Data. This field is used to report the state dependent data requested by the Data_Select field. The value of this field is scaled by the value reported by the Data_Scale field. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
23	RO	0x0	BUS_PWR_CLK_CON_EN Bus Power/Clock Control Enable. If this field is set, Bus Power/Clock Control is Enable. Value After Reset: 0x0
22	RO	0x0	B2_B3_SUPPORT B2B3 Support for D3hot. If this field is set, B2B3 support for D3hot is available. Value After Reset: 0x0
21:16	RO	0x00	reserved
15	W1C	0x0	PME_STATUS PME_Status. This bit is set when the function normally generates a PME signal. The value of this bit is not affected by the value of the PME_En bit. If PME_Support bit 31 of the Power Management Capabilities register is clear, this bit is permitted to be hardwired to 0b. Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this register value is not modified by Conventional Reset or FLR. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14:13	RO	0x0	DATA_SCALE Data_Scale. This field indicates the scaling factor to be used when interpreting the value of the Data field. The value and meaning of this field varies depending on which data value has been selected by the Data_Select field. For more details, see 7.5.2.3 section of PCI Express Base Specification. Value After Reset: 0x0
12:9	RO	0x0	DATA_SELECT Data_Select. This 4-bit field is used to select which data is to be reported through the Data and Data_Scale field. If the Data field is not implemented, this field must be hardwired to 0000b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	PME_ENABLE PME_En. When set, the function is permitted to generate a PME. When clear, the function is not permitted to generate a PME. If PME_Support is 1 xxxxb (PME generation from D3cold) or the function consumes Aux power and Aux power is available this bit is RWS and the bit is not modified by Conventional Reset or FLR. If PME_Support is 0 xxxxb, this field is not sticky (RW). If PME_Support is 0 0000b, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
7:4	RO	0x0	reserved
3	RW	0x1	NO_SOFT_RST No_Soft_Reset. This bit indicates the state of the function after writing the PowerState field to transition the function from D3hot to D0. When set, this transition preserves internal function state. The function is in D0Active and no additional software intervention is required. When clear, this transition results in undefined internal function state. Regardless of this bit, functions that transition from D3hot to D0 by Fundamental Reset will return to D0Uninitialized with only PME context preserved if PME is supported and enabled. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	POWER_STATE PowerState. This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. You can write to this register; however, the read-back value is the actual power state, not the write value. If you attempt to write an unsupported, optional state to this field, the write operation completes normally; however, the data is discarded and no state change occurs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (D0): D0 power state 0x1 (D1): D1 power state 0x2 (D2): D2 power state 0x3 (D3hot): D3hot D3hot power state Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

11.4.4.5 USP_PCIE_MSI Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_MSI_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x018A7005	MSI Capability Header and Message Control Register
USP_PCIE_MSI_CAP_OFF_04H_REG	0x0004	W	0x00000000	Message Address Register for MSI (Offset 04h)
USP_PCIE_MSI_CAP_OFF_08H_REG	0x0008	W	0x00000000	Message Address Register for MSI (Offset 08h)
USP_PCIE_MSI_CAP_OFF_0CH_REG	0x000C	W	0x00000000	Message Address Register for MSI (Offset 0Ch)
USP_PCIE_MSI_CAP_OFF_10H_REG	0x0010	W	0x00000000	Message Address Register for MSI (Offset 10h)
USP_PCIE_MSI_CAP_OFF_14H_REG	0x0014	W	0x00000000	Message Address Register for MSI (Offset 14h)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.6 USP_PCIE_MSI Detail Registers Description

USP_PCIE_MSI_CAP_ID_NEXT_CTRL_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	PCI_MSI_EXT_DATA_EN Extended Message Data Enable. If set, the function is enabled to provide Extended Message Data. If clear, the function is not enabled to provide Extended Message Data. Note: The access attributes of this field are as follows: Wire: PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_MSI_EXT_DATA_CAP ? RW : RO Dbi: PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_MSI_EXT_DATA_CAP ? RW : RO Value After Reset: 0x0 Testable: writeAsRead
25	RO	0x0	PCI_MSI_EXT_DATA_CAP Extended Message Data Capable. If set, the function is capable of providing Extended Message Data. If clear, the function does not support providing Extended Message Data. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
24	RO	0x1	PCI_PVM_SUPPORT Per-Vector Masking Capable. If set, the function supports MSI Per-Vector Masking. If clear, the function does not support MSI Per-Vector Masking. This bit must be set if the function is a PF or VF within an SR-IOV Device. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
23	RO	0x1	PCI_MSI_64_BIT_ADDR_CAP 64 bit address capable. If set, the function is capable of sending a 64-bit message address. If clear, the function is not capable of sending a 64-bit message address. This bit must be set if the function is a PCI Express Endpoint. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
22:20	RW	0x0	PCI_MSI_MULTIPLE_MSG_EN Multiple Message Enable. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). The number of allocated vectors is aligned to a power of two. If a function requests four vectors (indicated by a Multiple Message Capable encoding of 010b), system software can allocate either four, two, or one vector by writing a 010b, 001b, or 000b to this field, respectively. When MSI is enabled, a function will be allocated at least 1 vector. All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (_1_VECTOR): 1 vector allocated 0x1 (_2_VECTOR): 2 vectors allocated 0x2 (_4_VECTOR): 4 vectors allocated 0x3 (_8_VECTOR): 8 vectors allocated 0x4 (_16_VECTOR): 16 vectors allocated 0x5 (_32_VECTOR): 32 vectors allocated Value After Reset: 0x0

Bit	Attr	Reset Value	Description
19:17	RW	0x5	PCI_MSI_MULTIPLE_MSG_CAP Multiple Message Capable. System software reads this field to determine the number of requested vectors. The number of requested vectors must be aligned to a power of two (if a function requires three vectors, it requests four by initializing this field to 010b). All encodings other than the defined encodings are reserved. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (_1_VECTOR): 1 vector requested 0x1 (_2_VECTOR): 2 vectors requested 0x2 (_4_VECTOR): 4 vectors requested 0x3 (_8_VECTOR): 8 vectors requested 0x4 (_16_VECTOR): 16 vectors requested 0x5 (_32_VECTOR): 32 vectors requested Value After Reset: 0x5 Testable: unconstrained
16	RW	0x0	PCI_MSI_ENABLE MSI Enable. If set and the MSI-X Enable bit in the MSI-X Message Control register is clear, the function is permitted to use MSI to request service and is prohibited from using INTx interrupts. System configuration software sets this bit to enable MSI. A device driver is prohibited from writing this bit to mask a function's service request. For more details on control of INTx interrupts, see section 7.5.1.1 of PCI Express Base Specification. If clear, the function is prohibited from using MSI to request service. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x70	PCI_MSI_CAP_NEXT_OFFSET Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x70 Testable: unconstrained
7:0	RO	0x05	PCI_MSI_CAP_ID Capability ID. Indicates the MSI Capability structure. This field returns a Capability ID of 05h indicating that this is an MSI Capability structure. Value After Reset: 0x5

USP_PCIE_MSI_CAP_OFF_04H_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	PCI_MSI_CAP_OFF_04H Message Address - System-specified message address. If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG register) is set, the contents of this field specify the DWORD-aligned address (Address[31:02]) for the MSI transaction. Address[1:0] are set to 00b. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
1:0	RO	0x0	reserved

USP_PCIE_MSI_CAP_OFF_08H_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0AH For a function that supports a 32-bit message address, this field contains Extended Message Data (System-specified message data). For the MSI Capability structures without per-vector masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is outside the MSI Capability structure and undefined. For the MSI Capability structures with Per-vector Masking, it must be implemented if the Extended Message Data Capable bit is set; otherwise, it is RsvdP. If the Extended Message Data Enable bit (bit 26 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the DWORD Memory Write transaction uses Extended Message Data for the upper 16 bits; otherwise, it uses 0000h for the upper 16 bits. For a function that supports a 64-bit message address, it contains upper 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: Wire: PCI_MSI_64_BIT_ADDR_CAP || `DEFAULT_EXT_MSI_DATA_CAPABLE ? R/W : R Dbi: PCI_MSI_64_BIT_ADDR_CAP || `DEFAULT_EXT_MSI_DATA_CAPABLE ? R/W : R Value After Reset: 0x0 Testable: writeAsRead
15:0	RW	0x0000	PCI_MSI_CAP_OFF_08H For a function that supports a 32-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. For a function that supports a 64-bit message address, it contains lower 16 bits of the Message Upper Address. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_MSI_CAP_OFF_0CH_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PCI_MSI_CAP_OFF_0EH For a function that supports a 32-bit message address, this field contains the upper Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). Note: The access attributes of this field are as follows: Wire: (!MSI_64_EN && MSI_PVM_EN_VALUE) ? RW: MSI_64_EN && DEFAULT_EXT_MSI_DATA_CAPABLE ? RW : RO Dbi: (!MSI_64_EN && MSI_PVM_EN_VALUE) ? RW: MSI_64_EN && DEFAULT_EXT_MSI_DATA_CAPABLE ? RW : RO Value After Reset: 0x0 Testable: writeAsRead
15:0	RW	0x0000	PCI_MSI_CAP_OFF_0CH For a function that supports a 32-bit message address, this field contains the lower Mask Bits when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For a function that supports a 64-bit message address, this field contains Message Data (System-specified message data). If the Message Enable bit (bit 16 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) is set, the function sends a DWORD Memory Write transaction using Message Data for the lower 16 bits. All 4 Byte Enables are set. The Multiple Message Enable field (bits 22:20 of the PCI_MSI_CAP_ID_NEXT_CTRL_REG) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010b indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000b, the Function is not permitted to modify the message data. Note: The access attributes of this field are as follows: Wire: PCI_MSI_64_BIT_ADDR_CAP || MSI_PVM_EN ? R/W : R Dbi: PCI_MSI_64_BIT_ADDR_CAP || MSI_PVM_EN ? R/W : R Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_MSI_CAP_OFF_10H_REG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	PCI_MSI_CAP_OFF_10H Used for MSI when the Per Vector Masking Capable bit (PCI_MSI_CAP_ID_NEXT_CTRL_REG.PCI_PVM_SUPPORT) is set. For 32-bit contains Pending Bits. For 64-bit, contains Mask Bits. Note: The access attributes of this field are as follows: Wire: PCI_MSI_64_BIT_ADDR_CAP && MSI_PVM_EN ? R/W : R Dbi: PCI_MSI_64_BIT_ADDR_CAP && MSI_PVM_EN ? R/W : R Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_MSI_CAP_OFF_14H_REG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	PCI_MSI_CAP_OFF_14H Pending Bits. For each pending bit that is set, the function has a pending associated message. Value After Reset: 0x0

11.4.4.7 USP_PCIE_CAP Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG	0x0000	W	0x1002B010	PCI Express Capabilities, ID, Next Pointer Register
USP_PCIE_CAP_DEVICE_CAPABILITIES_REG	0x0004	W	0x00008FC0	Device Capabilities Register
USP_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS	0x0008	W	0x00002010	Device Control and Status Register
USP_PCIE_CAP_LINK_CAPABILITIES_REG	0x000C	W	0x00726C43	Link Capabilities Register
USP_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG	0x0010	W	0x10000000	Link Control and Status Register
USP_PCIE_CAP_SLOT_CAPABILITIES_REG	0x0014	W	0x00000000	Slot Capabilities Register. Exists Only in RC Mode
USP_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS	0x0018	W	0x000003C0	Slot Control and Status Register. Exists Only in RC Mode
USP_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG	0x001C	W	0x00010000	Root Control and Capabilities Register. Exists Only in RC Mode
USP_PCIE_CAP_ROOT_STATUS_REG	0x0020	W	0x00000000	Root Status Register. Exists Only in RC Mode
USP_PCIE_CAP_DEVICE_CAPABILITIES2_REG	0x0024	W	0x007C0830	Device Capabilities 2 Register
USP_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG	0x0028	W	0x00000000	Device Control 2 and Status 2 Register

Name	Offset	Size	Reset Value	Description
USP_PCIE_CAP_LINK_CAPABILITIES2_REG	0x002C	W	0x0000000E	Link Capabilities 2 Register
USP_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG	0x0030	W	0x00010003	Link Control 2 and Status 2 Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.8 USP_PCIE_CAP Detail Registers Description

USP_PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x08	PCIE_INT_MSG_NUM PCIE Interrupt Message Number. Interrupt Message Number. This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the MSI Message Control register. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x8 Testable: unconstrained

Bit	Attr	Reset Value	Description
24	RW	0x0	PCIE_SLOT_IMP Slot Implemented. When set, this bit indicates that the Link associated with this Port is connected to a slot (as compared to being connected to a system-integrated device or being disabled). This bit is valid for Downstream Ports. This bit is undefined for Upstream Ports. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
23:20	RO	0x0	PCIE_DEV_PORT_TYPE Device/Port Type. Indicates the specific type of this PCI Express function. Note: Different functions in a Multi-Function Device can generally be of different types. Defined encodings for functions that implement a Type 00h PCI Configuration Space header are: Defined encodings for functions that implement a Type 01h PCI Configuration Space header are: All other encodings are Reserved. Note: Different Endpoint types have notably different requirements in Section 1.3.2 of PCI Express Base Specification regarding I/O resources, Extended Configuration Space, and other capabilities. Values: 0x0 (PCIE_EP): PCI Express Endpoint 0x1 (PCIE_LEGACY_EP): Legacy PCI Express Endpoint 0x4 (ROOT_PORT_PCIE_RC): Root Port of PCI Express Root Complex 0x5 (USP_PCIE_SWITCH): Upstream Port of PCI Express Switch 0x6 (DSP_PCIE_SWITCH): Downstream Port of PCI Express Switch Value After Reset: 0x4 Testable: untestable Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
19:16	RO	0x2	PCIE_CAP_REG Capability Version. Indicates PCI-SIG defined PCI Express Capability structure version number. A version of the specification that changes the PCI Express Capability structure in a way that is not otherwise identifiable (for example, through a new Capability field) is permitted to increment this field. All such changes to the PCI Express Capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as functions reporting any such Capability Version numbers will contain a PCI Express Capability structure that is compatible with that piece of software. The controller hardwires this field to 2h for functions compliant to PCI Express Base Specification, Revision 4.0, Version 1.0. Note: This register field is sticky. Value After Reset: 0x2
15:8	RW	0xb0	PCIE_CAP_NEXT_PTR Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0xb0 Testable: unconstrained
7:0	RO	0x10	PCIE_CAP_ID Capability ID. Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. Value After Reset: 0x10

USP_PCIE_CAP_DEVICE_CAPABILITIES_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28	RW	0x0	PCIE_CAP_FLR_CAP Function Level Reset Capability. A value of 1b indicates the function supports the optional Function Level Reset mechanism described in section 6.6.2 of the PCI Express Base Specification. This bit applies to Endpoints only. For all other function types the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
27:26	RO	0x0	PCIE_CAP_CAP_SLOT_PWR_LMT_SCALE Captured Slot Power Limit Scale. Captured Slot Power Limit Scale (Upstream Ports only). Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit Message or hardwired to 00b (for more details, see section 6.9 of PCI Express Base Specification). Values: 0x0 (_1.0X): 1.0x 0x1 (_0.1X): 0.1x 0x2 (_0.01X): 0.01x 0x3 (_0.001X): 0.001x Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
25:18	RO	0x00	PCIE_CAP_CAP_SLOT_PWR_LMT_VALUE Captured Slot Power Limit Value. Captured Slot Power Limit Value (Upstream Ports only). In combination with the Captured Slot Power Limit Scale value, specifies the upper limit on power available to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Captured Slot Power Limit Scale field except when the Captured Slot Power Limit Scale field equals 00b (1.0x) and the Captured Slot Power Limit Value exceeds EFh, then alternative encodings are used (for more details, see section 7.5.3.9 of PCI Express Base Specification). This value is set by the Set_Slot_Power_Limit Message or hardwired to 00h (for more details, see section 6.9 of PCI Express Base Specification). Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
17:16	RO	0x0	reserved
15	RO	0x1	PCIE_CAP_ROLE_BASED_ERR_REPORT Role-Based Error Reporting. When set, this bit indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be set by all functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
14:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:9	RO	0x7	PCIE_CAP_EP_L1_ACCPT_LATENCY Endpoint L1 Acceptable Latency. This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L1 Acceptable Latency number to compare against the L1 Exit Latencies reported (see below) by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L1 entry can be used with no loss of performance. For functions other than Endpoints, this field is Reserved and the controller hardwires it to 000b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W (Sticky) else R(Sticky) Note: This register field is sticky. Values: 0x0 (MAX_1US): Maximum of 1 us 0x1 (MAX_2US): Maximum of 2 us 0x2 (MAX_4US): Maximum of 4 us 0x3 (MAX_8US): Maximum of 8 us 0x4 (MAX_16US): Maximum of 16 us 0x5 (MAX_32US): Maximum of 32 us 0x6 (MAX_64US): Maximum of 64 us 0x7 (NO_LIMIT): No limit Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
8:6	RW	0x7	PCIE_CAP_EP_L0S_ACCPT_LATENCY Endpoint L0s Acceptable Latency. This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L0s entry can be used with no loss of performance. For functions other than Endpoints, this field is Reserved and the controller hardwires it to 000b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (MAX_64NS): Maximum of 64 ns 0x1 (MAX_128NS): Maximum of 128 ns 0x2 (MAX_256NS): Maximum of 256 ns 0x3 (MAX_512NS): Maximum of 512 ns 0x4 (MAX_1US): Maximum of 1 us 0x5 (MAX_2US): Maximum of 2 us 0x6 (MAX_4US): Maximum of 4 us 0x7 (NO_LIMIT): No limit Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
5	RO	0x0	PCIE_CAP_EXT_TAG_SUPP Extended Tag Field Supported. This bit, in combination with the 10-Bit Tag Requester Supported bit in the Device Capabilities 2 register, indicates the maximum supported size of the Tag field as a Requester. This bit must be set if the 10-Bit Tag Requester Supported bit is set. Note: 8-bit Tag field generation must be enabled by the Extended Tag Field Enable bit in the Device Control register of the Requester Function before 8-bit Tags can be generated by the Requester. See Section 2.2.6.2 of PCI Express Base Specification for interactions with enabling the use of 10-Bit Tags. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (_5b_TAG): 5-bit Tag field supported 0x1 (_8b_TAG): 8-bit Tag field supported Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
4:3	RW	0x0	PCIE_CAP_PHANTOM_FUNC_SUPPORT Phantom Functions Supported. This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers (called Phantom Functions) with the Tag identifier (see Section 2.2.6.2 of PCI Express Base Specification for a description of Tag Extensions). With every Function in an ARI Device, the Phantom Functions Supported field must be set to 00b. The remainder of this field description applies only to non-ARI Multi-Function Devices. This field indicates the number of most significant bits of the Function Number portion of Requester ID that are logically combined with the Tag identifier. Note: Phantom Function support for the function must be enabled by the Phantom Functions Enable field in the Device Control register before the Function is permitted to use the Function Number field in the Requester ID for Phantom Functions. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (NO_PHNATOM_FUNC): No Function Number bits are used for Phantom Functions. Multi-Function Devices are permitted to implement up to 8 independent functions. 0x1 (MAX_1_PHANTOM_PER_FUNC): The most significant bit of the Function number in Requester ID is used for Phantom Functions; a Multi-Function Device is permitted to implement Functions 0-3. Functions 0, 1, 2, and 3 are permitted to use Function Numbers 4, 5, 6, and 7 respectively as Phantom Functions. 0x2 (MAX_3_PHANTOM_PER_FUNC): The two most significant bits of Function Number in Requester ID are used for Phantom Functions; a Multi-Function Device is permitted to implement Functions 0-1. Function 0 is permitted to use Function Numbers 2, 4, and 6 for Phantom Functions. Function 1 is permitted to use Function Numbers 3, 5, and 7 as Phantom Functions. 0x3 (SINGLE_FUNC_MAX_7_PHANTOM_FUNC): All 3 bits of Function Number in Requester ID used for Phantom Functions. The device must have a single Function 0 that is permitted to use all other Function Numbers as Phantom Functions. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
2:0	RW	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE Max_Payload_Size Supported. This field indicates the maximum payload size that the function can support for TLPs. All encodings other than the defined encodings are reserved. The functions of a Multi-Function Device are permitted to report different values for this field. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (MAX_128B_SIZE): 128 bytes max payload size 0x1 (MAX_256B_SIZE): 256 bytes max payload size 0x2 (MAX_512B_SIZE): 512 bytes max payload size 0x3 (MAX_1024B_SIZE): 1024 bytes max payload size 0x4 (MAX_2048B_SIZE): 2048 bytes max payload size 0x5 (MAX_4096B_SIZE): 4096 bytes max payload size Value After Reset: 0x1 Testable: unconstrained

USP_PCIE_CAP_DEVICE_CONTROL_DEVICE_STATUS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	PCIE_CAP_TRANS_PENDING Transactions Pending. Endpoints: When set, this bit indicates that the function has issued Non-Posted Requests that have not been completed. A Function reports this bit cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR. Root and Switch Ports: The controller hardwires this bit to 0b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
20	RO	0x0	PCIE_CAP_AUX_POWER_DETECTED AUX Power Detected. Functions that require Aux power report this bit as set if Aux power is detected by the function. This bit is derived by sampling the sys_aux_pwr_det input. Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
19	RW	0x0	PCIE_CAP_UNSUPPORTED_REQ_DETECTED Unsupported Request Detected. This bit indicates that the function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function Device, each function indicates status of errors as perceived by the respective function. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
18	W1C	0x0	PCIE_CAP_FATAL_ERR_DETECTED Fatal Error Detected. This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
17	W1C	0x0	PCIE_CAP_NON_FATAL_ERR_DETECTED Non-Fatal Error Detected. This bit indicates status of Non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective Function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
16	W1C	0x0	PCIE_CAP_CORR_ERR_DETECTED Correctable Error Detected. This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a Multi-Function device, each function indicates status of errors as perceived by the respective function. For functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x2	PCIE_CAP_MAX_READ_REQ_SIZE Max_Read_Request_Size. This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For functions that do not generate Read Requests larger than 128 bytes and functions that do not generate Read Requests on their own behalf, the controller implements this field as Read Only (RO) with a value of 000b. Values: 0x0 (MAX_128B_SIZE): 128 bytes maximum Read Request size 0x1 (MAX_256B_SIZE): 256 bytes maximum Read Request size 0x2 (MAX_512B_SIZE): 512 bytes maximum Read Request size 0x3 (MAX_1024B_SIZE): 1024 bytes maximum Read Request size 0x4 (MAX_2048B_SIZE): 2048 bytes maximum Read Request size 0x5 (MAX_4096B_SIZE): 4096 bytes maximum Read Request size 0x6 (RESERVED1): RESERVED 0x7 (RESERVED2): RESERVED Value After Reset: 0x
11	RO	0x0	PCIE_CAP_EN_NO_SNOOP Enable No Snoop. If this bit is set, the function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency (see section 2.2.6.5 in PCI Express Base Specification). Note: Setting this bit to 1b should not cause a function to set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. The controller hardwires this bit 0b if a function would never set the No Snoop attribute in transactions it initiates. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0

Bit	Attr	Reset Value	Description
10	RW	0x0	PCIE_CAP_AUX_POWER_PM_EN Aux Power PM Enable. This bit is derived by sampling the sys_aux_pwr_det input. When set this bit, enables a function to draw Aux power independent of PME Aux power. Functions that require Aux power on legacy operating systems should continue to indicate PME Aux power requirements. Aux power is allocated as requested in the Aux_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register (PMCSR). For Multi-Function devices, a component is allowed to draw Aux power if at least one of the functions has this bit set. Note: Functions that consume Aux power must preserve the value of this sticky register when Aux power is available. In such functions, this bit is not modified by Conventional Reset. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
9	RO	0x0	PCIE_CAP_PHANTOM_FUNC_EN Phantom Functions Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, If this bit is set, it enables a function to use unclaimed functions as Phantom functions to extend the number of outstanding transaction identifiers If this bit is clear, the function is not allowed to use Phantom functions For more details, see section 2.2.6.2 of PCI Express Base Specification. Software should not change the value of this bit while the function has outstanding Non-Posted Requests; otherwise, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: DEVICE_CAPABILITIES_REG.PCIE_CAP_PHANTOM_FUNC_SUPPORT ? RW : RO Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_PHANTOM_FUNC_SUPPORT ? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
8	RO	0x0	PCIE_CAP_EXT_TAG_EN Extended Tag Field Enable. This bit, in combination with the 10-Bit Tag Requester Enable bit in the Device Control 2 register, determines how many Tag field bits a Requester is permitted to use. When the 10-Bit Tag Requester Enable bit is clear, If the Extended Tag Field Enable bit is set, the function is permitted to use an 8-bit Tag field as a Requester If the Extended Tag Field Enable bit is clear, the Function is restricted to a 5-bit Tag field See section 2.2.6.2 of PCI Express Base Specification for required behavior when the 10-Bit Tag Requester Enable bit is set. If software changes the value of the Extended Tag Field Enable bit while the function has outstanding Non-Posted Requests, the result is undefined. For functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: DEVICE_CAPABILITIES_REG.PCIE_CAP_EXT_TAG_SUPP ? RW : RO Dbi: DEVICE_CAPABILITIES_REG.PCIE_CAP_EXT_TAG_SUPP ? RW : RO Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
7:5	RW	0x0	PCIE_CAP_MAX_PAYLOAD_SIZE_CS Max_Payload_Size. This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported field (PCIE_CAP_MAX_PAYLOAD_SIZE) in the Device Capabilities (DEVICE_CAPABILITIES_REG) register (for more details, see section 7.5.3.3 of PCI Express Base Specification). This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with a size exceeding the set value. For Functions that support only the 128-byte max payload size, the controller hardwires this field to 000b. System software is not required to program the same value for this field for all the Functions of a Multi-Function device (for more details, see section 2.2.2 of PCI Express Base Specification). For ARI Devices, Max_Payload_Size is determined solely by the setting in Function0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (MAX_128B_SIZE): 128 bytes maximum Read Request size 0x1 (MAX_256B_SIZE): 256 bytes maximum Read Request size 0x2 (MAX_512B_SIZE): 512 bytes maximum Read Request size 0x3 (MAX_1024B_SIZE): 1024 bytes maximum Read Request size 0x4 (MAX_2048B_SIZE): 2048 bytes maximum Read Request size 0x5 (MAX_4096B_SIZE): 4096 bytes maximum Read Request size 0x6 (RESERVED1): RESERVED 0x7 (RESERVED2): RESERVED Value After Reset: 0x0

Bit	Attr	Reset Value	Description
4	RW	0x1	PCIE_CAP_EN_REL_ORDER Enable Relaxed Ordering. If this bit is set, the function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering (for more details, see section 2.2.6.4 and section 2.4 of PCI Express Base Specification). For a function that never sets the Relaxed Ordering attribute in transactions it initiates as a Requester, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
3	RW	0x0	PCIE_CAP_UNSUPPORT_REQ_REP_EN Unsupported Request Reporting Enable. This bit, in conjunction with other bits, controls the signaling of Unsupported Request Errors by sending error Messages (for more details, see section 6.2.5 and section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each Function from point-of-view of the respective Function. Value After Reset: 0x0
2	RW	0x0	PCIE_CAP_FATAL_ERR_REPORT_EN Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_FATAL Messages (for more details, see section 6.2.5 and section 6.2.6 of of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL Message is generated. Value After Reset: 0x0
1	RW	0x0	PCIE_CAP_NON_FATAL_ERR_REPORT_EN Non-Fatal Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages (for more details, see section 6.2.5 and Section 6.2.6 of PCI Express Base Specification). For a Multi-Function Device, this bit controls error reporting for each function from point-of-view of the respective Function. For a Root Port, the reporting of Non-fatal errors is internal to the root. No external ERR_NONFATAL Message is generated. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	PCIE_CAP_CORR_ERR_REPORT_EN Correctable Error Reporting Enable. This bit, in conjunction with other bits, controls sending ERR_COR Messages (for more details, see section 6.2.5, section 6.2.6, and section 6.2.10.2 of PCI Express Base Specification). For a Multi-Function device, this bit controls error reporting for each function from point-of-view of the respective function. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated. Value After Reset: 0x0

USP_PCIE_CAP_LINK_CAPABILITIES_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	PCIE_CAP_PORT_NUM Port Number. This field indicates the PCI Express Port number for the given PCI Express Link. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
23	RO	0x0	reserved
22	RW	0x1	PCIE_CAP_ASPM_OPT_COMPLIANCE ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
21	RW	0x1	PCIE_CAP_LINK_BW_NOT_CAP ASPM Optionality Compliance. This field must be set to 1b in all functions. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x1 Testable: unconstrained
20	RO	0x1	PCIE_CAP_DLL_ACTIVE_REP_CAP Data Link Layer Link Active Reporting Capable. For a Downstream Port, the controller hardwires this bit to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable bit of the Slot Capabilities register) or a Downstream Port that supports Link speeds greater than 5.0 GT/s, the controller hardwires this bit to 1b. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Value After Reset: 0x1
19	RW	0x0	PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP Surprise Down Error Reporting Capable. For a Downstream Port, this bit must be set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
18	RO	0x0	PCIE_CAP_CLOCK_POWER_MAN Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Clock Power Management. For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. L1 PM Substates defines other semantics for the CLKREQ# signal, which are managed independently of Clock Power Management. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a Multi-Function device associated with an Upstream Port, each Function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the Multi-Function device indicate a 1b in this bit. For ARI Devices, all Functions must indicate the same value in this bit. For Downstream Ports, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
17:15	RW	0x4	PCIE_CAP_L1_EXIT_LATENCY L1 Exit Latency. This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from ASPM L1 to L0. If ASPM L1 is not supported, the value is undefined. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: CX_NFTS !=CX_COMM_NFTS DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (LESS_THAN_1US): Less than 1us 0x1 (_1US_TO_2US): 1 us to less than 2 us 0x2 (_2US_TO_4US): 2 us to less than 4 us 0x3 (_4US_TO_8US): 4 us to less than 8 us 0x4 (_8US_TO_16US): 8 us to less than 16 us 0x5 (_16US_TO_32US): 16 us to less than 32 us 0x6 (_32US_TO_64US): 32 us to 64 us 0x7 (GREATER_THAN_64US): More than 64 us Value After Reset: 0x4 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
14:12	RW	0x6	PCIE_CAP_L0S_EXIT_LATENCY L0s Exit Latency. This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. If L0s is not supported, the value is undefined; however, see the Implementation Note "Potential Issues With Legacy Software When L0s is Not Supported" in section 5.4.1.1 of PCI Express Base Specification for the recommended value. Note: Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. There are two each of these register fields, this one and a shadow one at the same address. The Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG) determines which one is used by the controller and which one is accessed by a read request. Common Clock operation is supported (possible) in the controller when one or more of the following expressions is true: CX_NFTS !=CX_COMM_NFTS DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Common Clock operation is enabled in the controller when you set the Common Clock bit (PCIE_CAP_COMMON_CLK_CONFIG) of the Link Control Register (LINK_CONTROL_LINK_STATUS_REG). The assertion of CS2 (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) is required to write to the shadow field at this location. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (LESS_THAN_64NS): Less than 64 ns 0x1 (_64NS_TO_128NS): 64 ns to less than 128 ns 0x2 (_128NS_TO_256NS): 128 ns to less than 256 ns 0x3 (_256NS_TO_512NS): 256 ns to less than 512 ns 0x4 (_512NS_TO_1US): 512 ns to less than 1 us 0x5 (_1US_TO_2US): 1 us to less than 2 us 0x6 (_2US_TO_4US): 2 us to 4 us 0x7 (GREATER_THAN_4US): More than 4 us Value After Reset: 0x6 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:10	RW	0x3	PCIE_CAP_ACTIVE_STATE_LINK_PM_SUPPORT Active State Power Management (ASPM) Support. This field indicates the level of ASPM supported on the given PCI Express Link. For more details on ASPM support requirements, see section 5.4.1 of PCI Express Base Specification. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (NO_ASPM_SUP): No ASPM Support 0x1 (L0S_SUP): L0s Supported 0x2 (L1_SUP): L1 Supported 0x3 (L0S_L1_SUP): L0s and L1 Supported Value After Reset: 0x2 Testable: unconstrained

Bit	Attr	Reset Value	Description
9:4	RW	0x04	PCIE_CAP_MAX_LINK_WIDTH Maximum Link Width. This field indicates the maximum Link width (xN - corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. All encodings other than the defined encodings are reserved. Multi-Function devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (X1): x1 0x2 (X2): x2 0x4 (X4): x4 0x8 (X8): x8 0xc (X12): x12 0x10 (X16): x16 0x20 (X32): x32 Value After Reset: 0x4 Testable: unconstrained

Bit	Attr	Reset Value	Description
3:0	RW	0x3	PCIE_CAP_MAX_LINK_SPEED Max Link Speed. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. All encodings other than the defined encodings are reserved. Multi-Function Devices associated with an Upstream Port must report the same value in this field for all functions. In M-PCIe mode, the reset and dynamic values of this field are calculated by the controller. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (SUP_LINK_SPEED_FIELD_BIT_0): Supported Link Speeds Vector field bit 0 0x2 (SUP_LINK_SPEED_FIELD_BIT_1): Supported Link Speeds Vector field bit 1 0x3 (SUP_LINK_SPEED_FIELD_BIT_2): Supported Link Speeds Vector field bit 2 0x4 (SUP_LINK_SPEED_FIELD_BIT_3): Supported Link Speeds Vector field bit 3 0x5 (SUP_LINK_SPEED_FIELD_BIT_4): Supported Link Speeds Vector field bit 4 0x6 (SUP_LINK_SPEED_FIELD_BIT_5): Supported Link Speeds Vector field bit 5 0x7 (SUP_LINK_SPEED_FIELD_BIT_6): Supported Link Speeds Vector field bit 6 Value After Reset: 0x3 Testable: unconstrained

USP_PCIE_CAP_LINK_CONTROL_LINK_STATUS_REG
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	W1C	0x0	PCIE_CAP_LINK_AUTO_BW_STATUS Link Autonomous Bandwidth Status. This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: R Value After Reset: 0x0

Bit	Attr	Reset Value	Description
30	W1C	0x0	PCIE_CAP_LINK_BW_MAN_STATUS Link Bandwidth Management Status. This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: A Link retraining has completed following a write of 1b to the Retrain Link bit. Note: This bit is set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. The default value of this bit is 0b. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: R Value After Reset: 0x0
29	RO	0x0	PCIE_CAP_DLL_ACTIVE Data Link Layer Link Active. This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the Data Link Layer Link Active Reporting Capable bit is 1b. Otherwise, the controller hardwires it to 0b. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
28	RW	0x1	PCIE_CAP_SLOT_CLK_CONFIG Slot Clock Configuration. This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference clock on the connector, this bit must be clear. For a Multi-Function Device, each Function must report the same value for this bit. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x1 Testable: unconstrained
27	RO	0x0	PCIE_CAP_LINK_TRAINING Link Training. This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches, and the controller hardwires it to 0b. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: R Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:20	RO	0x00	PCIE_CAP_NEGO_LINK_WIDTH Negotiated Link Width. This field indicates the negotiated width of the given PCI Express Link. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up. Values: 0x1 (X1): x1 0x2 (X2): x2 0x4 (X4): x4 0x8 (X8): x8 0xc (X12): x12 0x10 (X16): x16 0x20 (X32): x32 Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
19:16	RO	0x0	PCIE_CAP_LINK_SPEED Current Link Speed. This field indicates the negotiated Link speed of the given PCI Express Link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. All encodings other than the defined encodings are reserved. The value in this field is undefined when the Link is not up. Values: 0x1 (SUP_LINK_SPEED_FIELD_BIT_0): Supported Link Speeds Vector field bit 0 0x2 (SUP_LINK_SPEED_FIELD_BIT_1): Supported Link Speeds Vector field bit 1 0x3 (SUP_LINK_SPEED_FIELD_BIT_2): Supported Link Speeds Vector field bit 2 0x4 (SUP_LINK_SPEED_FIELD_BIT_3): Supported Link Speeds Vector field bit 3 0x5 (SUP_LINK_SPEED_FIELD_BIT_4): Supported Link Speeds Vector field bit 4 0x6 (SUP_LINK_SPEED_FIELD_BIT_5): Supported Link Speeds Vector field bit 5 0x7 (SUP_LINK_SPEED_FIELD_BIT_6): Supported Link Speeds Vector field bit 6 Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
15:14	RW	0x0	PCIE_CAP_DRS_SIGNALING_CONTROL DRS Signaling Control. Indicates the mechanism used to report reception of a DRS message. Must be implemented for Downstream Ports with the DRS Supported bit Set in the Link Capabilities 2 Register. Encodings are: If DRS Supported is set, receiving a DRS Message will set DRS Message Received in the Link Status 2 Register but will otherwise have no effect If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, and either MSI or MSI-X is enabled, an MSI or MSI-X interrupt is generated using the vector in Interrupt Message Number (section 7.5.3.2) If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, the Port must send an FRS Message Upstream with the FRS Reason field set to DRS Message Received. Behavior is undefined if this field is set to 10b and the FRS Supported bit in the Device Capabilities 2 Register is Clear. Behavior is undefined if this field is set to 11b. For Downstream Ports with the DRS Supported bit clear in the Link Capabilities 2 register, the controller hardwires this field to 00b. This field is Reserved for Upstream Ports. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES2_REG.DRS_SUPPORTED ? RW : RO Values: 0x0 (DRS_NOT_REPORTED): DRS not Reported 0x1 (DRS_INTRRUPT_EN): DRS Interrupt Enabled 0x2 (FRS_EN): DRS to FRS Signaling Enabled Value After Reset: 0x0 Testable: writeAsRead
13:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	PCIE_CAP_LINK_AUTO_BW_INT_EN Link Autonomous Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
10	RW	0x0	PCIE_CAP_LINK_BW_MAN_INT_EN Link Bandwidth Management Interrupt Enable. When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. The write value is gated with the PCIE_CAP_LINK_BW_NOT_CAP field in LINK_CAPABILITIES_REG. This bit is not applicable and is Reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. For functions that do not implement the Link Bandwidth Notification Capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_LINK_BW_NOT_CAP ? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
9	RW	0x0	PCIE_CAP_HW_AUTO_WIDTH_DISABLE Hardware Autonomous Width Disable. When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. For components that do not implement the ability autonomously to change Link width, the ciontroller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	PCIE_CAP_EN_CLK_POWER_MAN Enable Clock Power Management. Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: For a non-ARI Multi-Function Device, power-management-configuration software must only Set this bit if all Functions of the Multi-Function Device indicate a 1b in the Clock Power Management bit of the Link Capabilities register. The component is permitted to use the CLKREQ# signal to power manage Link clock only if this bit is Set for all Functions. For ARI Devices, Clock Power Management is enabled solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. The CLKREQ# signal may also be controlled via the L1 PM Substates mechanism. Such control is not affected by the setting of this bit. For Downstream Ports and components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities register), the controller hardwires this bit to 0b. The write value is gated with the PCIE_CAP_CLOCK_POWER_MAN field in LINK_CAPABILITIES_REG. Note: The access attributes of this field are as follows: Wire: LINK_CAPABILITIES_REG.PCIE_CAP_CLOCK_POWER_MAN ? RWS : ROS Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_CLOCK_POWER_MAN ? RWS : ROS Note: This register field is sticky. Values: 0x0 (PM_DISABLE_LOW_CLKREQ): Clock power management is disabled and device must hold CLKREQ# signal low. 0x1 (CLKREQ_IN_USE): When this bit is set, the device is permitted to use CLKREQ# signal to power manage Link clock according to protocol defined in appropriate form factor specification. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
7	RW	0x0	PCIE_CAP_EXTENDED_SYNCH Extended Synch. When set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state (see section 4.2.4.5 of PCI Express Base Specification) and when in the Recovery state (see section 4.2.6.4.1 of PCI Express Base Specification). This mode provides external devices (for example, logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. For Multi-Function devices if any function has this bit set, then the component must transmit the additional Ordered Sets when exiting L0s or when in Recovery. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6	RW	0x0	PCIE_CAP_COMMON_CLK_CONFIG Common Clock Configuration. When set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. For non-ARI Multi-Function Devices, software must program the same value for this bit in all Functions. If not all Functions are Set, then the component must as a whole assume that its reference clock is not common with the Upstream component. For ARI Devices, Common Clock Configuration is determined solely by the setting in Function 0. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies. After changing the value in this bit in both components on a Link, software must trigger the Link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
5	RW	0x0	PCIE_CAP_RETRAIN_LINK Retrain Link. A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. If the LTSSM is already in Recovery or Configuration, re-entering Recovery is permitted but not required. If the Port is in DPC when a write of 1b to this bit occurs, the result is undefined. Reads of this bit always return 0b. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. This bit is not applicable and is Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read. Note: The access attributes of this field are as follows: Wire: see description Dbi: see description Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_LINK_DISABLE Link Disable. This bit disables the Link by directing the LTSSM to the Disabled state when set; this bit is Reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. After clearing this bit, software must honor timing requirements defined in Section 6.6.1 with respect to the first Configuration Read following a Conventional Reset. In a DSP that supports crosslink, the controller gates the write value with the CROSS_LINK_EN field in PORT_LINK_CTRL_OFF. Note: The access attributes of this field are as follows: Wire: CX_CROSSLINK_ENABLE=1 && PORT_LINK_CTRL_OFF.CROSS_LINK_EN=1||CX_CROSSLINK_ENABLE=0 && dsp=1 ? RW : RO Dbi: CX_CROSSLINK_ENABLE=1 && PORT_LINK_CTRL_OFF.CROSS_LINK_EN=1||CX_CROSSLINK_ENABLE=0 && dsp=1? RW : RO Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	PCIE_CAP_RCB Read Completion Boundary (RCB). Root Ports: Indicates the RCB value for the Root Port. Refer to section 2.3.1.1 of PCI Express Base Specification for the definition of the parameter RCB. The controller hardwires this bit for a Root Port and returns its RCB support capabilities. Endpoints and Bridges: Optionally set by configuration software to indicate the RCB value of the Root Port Upstream from the Endpoint or Bridge. Refer to Section 2.3.1.1 of PCI Express Base Specification for the definition of the parameter RCB is same as Root Port. Configuration software must only set this bit if the Root Port Upstream from the Endpoint or Bridge reports an RCB value of 128 bytes (a value of 1b in the Read Completion Boundary bit). For functions that do not implement this feature, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R/W Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Values: 0x0 (_64B): 64 byte 0x1 (_128B): 128 byte Value After Reset: 0x0 Testable: unconstrained
2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	PCIE_CAP_ACTIVE_STATE_LINK_PM_CONTROL Active State Power Management (ASPM) Control. This field controls the level of ASPM enabled on the given PCI Express Link. See section 5.4.1.3 of PCI Express Base Specification for requirements on when and how to enable ASPM. Note: "L0s Entry Enabled" enables the Transmitter to enter L0s. If L0s is supported, the Receiver must be capable of entering L0s even when the Transmitter is disabled from entering L0s (00b or 10b). ASPM L1 must be enabled by software in the Upstream component on a Link prior to enabling ASPM L1 in the Downstream component on that Link. When disabling ASPM L1, software must disable ASPM L1 in the Downstream component on a Link prior to disabling ASPM L1 in the Upstream component on that Link. ASPM L1 must only be enabled on the Downstream component if both components on a Link support ASPM L1. For Multi-Function Devices (including ARI Devices), it is recommended that software program the same value for this field in all Functions. For non-ARI Multi-Function Devices, only capabilities enabled in all Functions are enabled for the component as a whole. For ARI Devices, ASPM Control is determined solely by the setting in Function0, regardless of Function 0's D-state. The settings in the other Functions always return whatever value software programmed for each, but otherwise are ignored by the component. Software must not enable L0s in either direction on a given Link unless components on both sides of the Link each support L0s; otherwise, the result is undefined. Values: 0x0 (DISABLED): Disabled 0x1 (L0S_ENTRY_EN): L0s Entry Enabled 0x2 (L1_ENTRY_En): L1 Entry Enabled 0x3 (L0S_L1_ENTRY_EN): L0s and L1 Entry Enabled Value After Reset: 0x0

USP_PCIE_CAP_SLOT_CAPABILITIES_REG
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	PCIE_CAP_PHY_SLOT_NUM Physical Slot Number. This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
18	RW	0x0	PCIE_CAP_NO_CMD_CPL_SUPPORT No Command Completed Support. When set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
17	RW	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK Electromechanical Interlock Present. When set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
16:15	RW	0x0	PCIE_CAP_SLOT_POWER_LIMIT_SCALE Slot Power Limit Scale. Specifies the scale used for the Slot Power Limit Value (for more details, see Section 6.9 of PCI Express Base Specification). This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Values: 0x0 (_1.0X): 1.0x 0x1 (_0.1X): 0.1x 0x2 (_0.01X): 0.01x 0x3 (_0.001X): 0.001x Value After Reset: 0x0 Testable: unconstrained
14:7	RW	0x00	PCIE_CAP_SLOT_POWER_LIMIT_VALUE Slot Power Limit Value. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot (for more detais, see Section 6.9 of PCI Express Base Specification) or by other means to the adapter. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b (1.0x) and Slot Power Limit Value exceeds EFh, the alternative encodings defined in Values: are used. Value F3h to FFh are Reserved for Slot Power Limit values above 300 W. This register must be implemented if the Slot Implemented bit is set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Values: 0xf0 (_250W_LIMIT): 250 W Slot Power Limit 0xf1 (_275W_LIMIT): 275 W Slot Power Limit 0xf2 (_300W_LIMIT): 300 W Slot Power Limit Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
6	RW	0x0	PCIE_CAP_HOT_PLUG_CAPABLE Hot-Plug Capable. When set, this bit indicates that this slot is capable of supporting hot-plug operations. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
5	RW	0x0	PCIE_CAP_HOT_PLUG_SURPRISE Hot-Plug Surprise. When set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
4	RW	0x0	PCIE_CAP_POWER_INDICATOR Power Indicator Present. When set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
3	RW	0x0	PCIE_CAP_ATTENTION_INDICATOR Attention Indicator Present. When set, this bit indicates that an Attention Indicator is electrically controlled by the chassis. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
2	RW	0x0	PCIE_CAP_MRL_SENSOR MRL Sensor Present. When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
1	RW	0x0	PCIE_CAP_POWER_CONTROLLER Power Controller Present. When set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor). Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained
0	RW	0x0	PCIE_CAP_ATTENTION_INDICATOR_BUTTON Attention Button Present. When set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Value After Reset: 0x0 Testable: unconstrained

USP_PCIE_CAP_SLOT_CONTROL_SLOT_STATUS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	W1C	0x0	PCIE_CAP_DLL_STATE_CHANGED Data Link Layer State Changed. This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
23	RO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_STATUS Electromechanical Interlock Status. If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock. Values: 0x0 (DISENGAGED): Electromechanical Interlock Disengaged 0x1 (ENGAGED): Electromechanical Interlock Engaged Value After Reset: 0x0
22	RO	0x0	PCIE_CAP_PRESENCE_DETECT_STATE Presence Detect State. This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. This bit must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), the controller hardwires this bit to 1b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R Values: 0x0 (EMPTY_SLOT): Slot Empty 0x1 (ADAPTER_PRESENT_IN_SLOT): Adapter Present in slot Value After Reset: 0x1 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
21	RO	0x0	PCIE_CAP_MRL_SENSOR_STATE MRL Sensor State. This bit reports the status of the MRL sensor if implemented. Encodings are define as above. Values: 0x0 (MRL_CLOSED): MRL Closed 0x1 (MRL_OPEN): MRL Open Value After Reset: 0x0

Bit	Attr	Reset Value	Description
20	W1C	0x0	PCIE_CAP_CMD_CPLD Command Completed. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. If Command Completed notification is not supported, the controller hardwires this bit to 0b. Value After Reset: 0x0
19	W1C	0x0	PCIE_CAP_PRESENCE_DETECTED_CHANGED Presence Detect Changed. This bit is set when the value reported in the Presence Detect State bit is changed. Value After Reset: 0x0
18	W1C	0x0	PCIE_CAP_MRL_SENSOR_CHANGED MRL Sensor Changed. If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set. Value After Reset: 0x0
17	W1C	0x0	PCIE_CAP_POWER_FAULT_DETECTED Power Fault Detected. If a Power Controller that supports power fault detection is implemented, this bit issSet when the Power Controller detects a power fault at this slot. Note: Depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set. Value After Reset: 0x0
16	W1C	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED Attention Button Pressed. If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set. Value After Reset: 0x0
15:13	RO	0x0	reserved
12	RW	0x0	PCIE_CAP_DLL_STATE_CHANGED_EN Data Link Layer State Changed Enable. If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11	WO	0x0	PCIE_CAP_ELECTROMECH_INTERLOCK_CTRL Electromechanical Interlock Control. If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
10	RW	0x0	PCIE_CAP_POWER_CONTROLLER_CTRL Power Controller Control. If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. Note: In some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. If the Power Controller Present bit in the Slot Capabilities register is clear, then writes to this bit have no effect and the read value of this bit is undefined. Values: 0x0 (PWR_ON): Power On 0x1 (PWR_OFF): Power Off Value After Reset: 0x0
9:8	RW	0x3	PCIE_CAP_POWER_INDICATOR_CTRL Power Indicator Control. If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Power Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b. Values: 0x0 (RESERVED): Reserved 0x1 (ON): On 0x2 (BLINK): Blink 0x3 (OFF): Off Value After Reset: 0x3

Bit	Attr	Reset Value	Description
7:6	RW	0x3	PCIE_CAP_ATTENTION_INDICATOR_CTRL Attention Indicator Control. If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting, if required to, for the previous command to complete in which case the read value is undefined. Note: The default value of this field must be one of the non-Reserved values. If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 00b. Values: 0x0 (RESERVED): Reserved 0x1 (ON): On 0x2 (BLINK): Blink 0x3 (OFF): Off Value After Reset: 0x3
5	RW	0x0	PCIE_CAP_HOT_PLUG_INT_EN Hot-Plug Interrupt Enable. When set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is clear, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
4	RW	0x0	PCIE_CAP_CMD_CPL_INT_EN Command Completed Interrupt Enable. If Command Completed notification is supported (if the No Command Completed Support bit in the Slot Capabilities register is 0b), when set, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, the controller hardwires this bit must to 0b. Write value is gated with PCIE_CAP_NO_CMD_CPL_SUPPORT field in SLOT_CAPABILITIES_REG. Note: The access attributes of this field are as follows: Wire: No access. Dbi: SLOT_CAPABILITIES_REG.PCIE_CAP_NO_CMD_CPL_SUPPORT ? RO : RW Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	PCIE_CAP_PRESENCE_DETECT_CHANGE_EN Presence Detect Changed Enable. When set, this bit enables software notification on a presence detect changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
2	RW	0x0	PCIE_CAP_MRL_SENSOR_CHANGED_EN MRL Sensor Changed Enable. When set, this bit enables software notification on a MRL sensor changed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
1	RW	0x0	PCIE_CAP_POWER_FAULT_DETECTED_EN Power Fault Detected Enable. When set, this bit enables software notification on a power fault event (for more details, see Section 6.7.3 of PCI Express Base Specification). If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0
0	RW	0x0	PCIE_CAP_ATTENTION_BUTTON_PRESSED_EN Attention Button Pressed Enable. When set to 1b, this bit enables software notification on an attention button pressed event (for more details, see Section 6.7.3 of PCI Express Base Specification). If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Value After Reset: 0x0

USP_PCIE_CAP_ROOT_CONTROL_ROOT_CAPABILITIES_REG

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x1	PCIE_CAP_CRS_SW_VISIBILITY CRS Software Visibility Capable. When set, this bit indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W (Sticky) else R (Sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved
4	RW	0x0	PCIE_CAP_CRS_SW_VISIBILITY_EN CRS Software Visibility Enable. When set, this bit enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software (for more details, see section 2.3.1 of PCI Express Base Specification). For Root Ports that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: No access. Dbi: ROOT_CONTROL_ROOT_CAPABILITIES_REG.PCIE_CAP_CRS_SW_VISIBILITY ? RW : RO Value After Reset: 0x0 Testable: writeAsRead
3	RW	0x0	PCIE_CAP_PME_INT_EN PME Interrupt Enable. When set, this bit enables PME interrupt generation upon receipt of a PME Message as reflected in the PME Status bit (for more details, see Table 7-29 of PCI Express Base Specification). A PME interrupt is also generated if the PME Status bit is set when this bit is changed from clear to set. Value After Reset: 0x0
2	RW	0x0	PCIE_CAP_SYS_ERR_ON_FATAL_ERR_EN System Error on Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Fatal error (ERR_FATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific. Value After Reset: 0x0
1	RW	0x0	PCIE_CAP_SYS_ERR_ON_NON_FATAL_ERR_EN System Error on Non-Fatal Error Enable. If set, this bit indicates that a System Error should be generated if a Non-fatal error (ERR_NONFATAL) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific. Value After Reset: 0x0
0	RW	0x0	PCIE_CAP_SYS_ERR_ON_CORR_ERR_EN System Error on Correctable Error Enable. If set, this bit indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the Hierarchy Domain associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system is system specific. Value After Reset: 0x0

USP_PCIE_CAP_ROOT_STATUS_REG
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	PCIE_CAP_PME_PENDING PME Pending. This bit indicates that another PME is pending when the PME Status bit is s et. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the PME Requester ID field appropriately. The PME Pending bit is cleared by hardware if no more PMEs are pending. Value After Reset: 0x0
16	W1C	0x0	PCIE_CAP_PME_STATUS PME Status. This bit indicates that PME was asserted by the PME Requester indicated in the PME Requester ID field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1b. Value After Reset: 0x0
15:0	RO	0x0000	PCIE_CAP_PME_REQ_ID PME Requester ID. This field indicates the PCI Requester ID of the last PME Requester. This field is only valid when the PME Status bit is set. Value After Reset: 0x0

USP_PCIE_CAP_DEVICE_CAPABILITIES2_REG

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:22	RW	0x1	PCIE_CAP2_CFG_MAX_END2END_TLP_PRFXS Max End-End TLP Prefixes. Indicates the maximum number of End-End TLP Prefixes supported by this Function. For more details, see Section 2.2.10.2 of PCI Express Base Specification. If End-End TLP Prefix Supported is clear, this field is RsvdP. Different Root Ports that have the End-End TLP Prefix Supported bit set are permitted to report different values for this field. For Switches where End-End TLP Prefix Supported is set, this field must be 00b indicating support for up to four End-End TLP Prefixes. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x1 (ONE_END_END_TLP_PREFIX): 1 End-End TLP Prefix 0x2 (TWO_END_END_TLP_PREFIX): 2 End-End TLP Prefixes 0x3 (THREE_END_END_TLP_PREFIX): 3 End-End TLP Prefixes 0x0 (FOUR_END_END_TLP_PREFIX): 4 End-End TLP Prefixes Value After Reset: 0x1 Testable: unconstrained
21	RW	0x1	PCIE_CAP2_CFG_END2END_TLP_PRFX_SUPPORT End-End TLP Prefix Supported. Indicates whether End-End TLP Prefix support is offered by a Function. Values are: All Ports of a Switch must have the same value for this bit. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (NO_SUP): No Support 0x1 (SUP): Support is provided to receive TLPs containing End-End TLP Prefixes. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
20	RW	0x1	PCIE_CAP2_CFG_EXTND_FMT_SUPPOR Extended Fmt Field Supported. If set, the Function supports the 3-bit definition of the Fmt field. If clear, the Function supports a 2-bit definition of the Fmt field. For more details, see section 2.2 of PCI Express Base Specification. Must be set for Functions that support End-End TLP Prefixes. All Functions in an Upstream Port must have the same value for this bit. Each Downstream Port of a component may have a different value for this bit. It is strongly recommended that Functions support the 3-bit definition of the Fmt field. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:18	RO	0x3	PCIE_CAP_OBFF_SUPPORT OBFF Supported. This field indicates if OBFF is supported and, if so, what signaling mechanism is used. The value reported in this field must indicate support for WAKE# signaling only if: for a Downstream Port, driving the WAKE# signal for OBFF is supported and the connector or component connected Downstream is known to receive that same WAKE# signal for an Upstream Port, receiving the WAKE# signal for OBFF is supported and, if the component is on an add-in-card, that the component is connected to the WAKE# signal on theconnector. Root Ports, Switch Ports, and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this field. For Bridges and Ports that do not implement this capability, the controller hardwires this field to 00b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky. Values: 0x0 (NOT_SUP): OBFF Not Supported 0x1 (SUP_USING_MSG): OBFF supported using Message signaling only 0x2 (SUP_USING_WAKE): OBFF supported using WAKE# signaling only 0x3 (SUP_USING_MSG_AND_WAKE): OBFF supported using WAKE# and Message signaling Value After Reset: 0x3 Testable: unconstrained
17	RO	0x0	PCIE_CAP2_10_BIT_TAG_REQ_SUPPORT 10-Bit Tag Requester Supported. If this bit is set, the Function supports 10-Bit Tag Requester capability; otherwise, the Function does not. This bit must not be set if the 10-Bit Tag Completer Supported bit is clear. Note: 10-Bit Tag field generation must be enabled by the 10-Bit Tag Requester Enable bit in the Device Control 2 register of the Requester Function before 10-Bit Tags can be generated by the Requester. For more details, see section 2.2.6.2. of PCI Express Base Specification. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
16	RO	0x0	PCIE_CAP2_10_BIT_TAG_COMP_SUPPORT 10-Bit Tag Completer Supported. If this bit is set, the Function supports 10-Bit Tag Completer capability; otherwise, the Function does not. For more details, see section 2.2.6.2. of PCI Express Base Specification. Value After Reset: 0x0
15:14	RO	0x0	PCIE_CAP2_LN_SYS_CLS LN System CLS. Applicable only to Root Ports and RCRBs; must be 00b for all other Function types. This field indicates if the Root Port or RCRB supports LN protocol as an LN Completer, and if so, what cacheline size is in effect. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (LN_COMPLETER_NO_SUP): LN Completer either not supported or not in effect 0x1 (LN_COMPLETER_64B_CACHE): LN Completer with 64-byte cachelines in effect 0x2 (LN_COMPLETER_128B_CACHE): LN Completer with 128-byte cachelines in effect Value After Reset: 0x0
13	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_1 TPH Completer Supported Bit 1. Value After Reset: 0x0
12	RO	0x0	PCIE_CAP_TPH_CMPLT_SUPPORT_0 TPH Completer Supported Bit 0. Value of this bit along with TPH Completer Supported Bit 1 indicates Completer support for TPH or Extended TPH. Applicable only to Root Ports and Endpoints. For all other Functions, this field is Reserved. For more details, see section 6.17 of PCI Express Base Specification. Values: 0x0 (TPH_EXT_TPH_CMPL_NOT_SUP_OR_RSVD): TPH and Extended TPH Completer not supported (if TPH Completer Supported Bit is 0) or Reserved ((if TPH Completer Supported Bit is 1). 0x1 (TPH_SUP_EXT_TPH_NOT_SUP_OR_BOTH_SUPP): TPH Completer supported; Extended TPH Completer not supported(if TPH Completer Supported Bit is 0) or Both TPH and Extended TPH Completer supported ((if TPH Completer Supported Bit is 1). Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11	RW	0x1	PCIE_CAP_LTR_SUPP LTR Mechanism Supported. A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. Root Ports, Switches and Endpoints are permitted to implement this capability. For a Multi-Function Device associated with an Upstream Port, each Function must report the same value for this bit. For Bridges and other Functions that do not implement this capability, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(Sticky) else R(Sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
10	RO	0x0	PCIE_CAP_NO_RO_EN_PR2PR_PAR No RO-enabled PR-PR Passing. If this bit is set, the routing element never carries out the passing permitted by Table 2-39 of PCI Express Base Specification entry A2b that is associated with the Relaxed Ordering Attribute field being Set. This bit applies only for Switches and RCs that support peer-to-peer traffic between Root Ports. This bit applies only to Posted Requests being forwarded through the Switch or RC and does not apply to traffic originating or terminating within the Switch or RC itself. All Ports on a Switch or RC must report the same value for this bit. For all other functions, this bit must be 0b. Value After Reset: 0x1
9	RO	0x0	PCIE_CAP_128_CAS_CPL_SUPP 128-bit CAS Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. This bit must be set to 1b if the Function supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification. Value After Reset: 0x0
8	RO	0x0	PCIE_CAP_64_ATOMIC_CPL_SUPP 64-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
7	RO	0x0	PCIE_CAP_32_ATOMIC_CPL_SUPP 32-bit AtomicOp Completer Supported. Applicable to Functions with Memory Space BARs as well as all Root Ports; must be 0b otherwise. Includes FetchAdd, Swap, and CAS AtomicOps. This bit must be set to 1b if the Function supports this optional capability. For more details on additional RC requirements, see section 6.15.3.1 of PCI Express Base Specification. Value After Reset: 0x0
6	RO	0x0	PCIE_CAP_ATOMIC_ROUTING_SUPP AtomicOp Routing Supported. Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports; must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. For more details, see section 6.15 of PCI Express Base Specification. Value After Reset: 0x0
5	RO	0x1	PCIE_CAP_ARI_FORWARD_SUPPORT ARI Forwarding Supported. Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. For more details, see section 6.13 of PCI Express Base Specification. Value After Reset: 0x1
4	RO	0x1	PCIE_CAP_CPL_TIMEOUT_DISABLE_SUPPORT Completion Timeout Disable Supported. A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports. For all other Functions this field is Reserved and the controller hardwires this bit to 0b. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_RANGE Completion Timeout Ranges Supported. This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50 us to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s Bits are set according to the list below to show timeout value ranges supported. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms. Values: 0x0 (NOT_SUP): Completion Timeout programming not supported, the Function must implement a timeout value in the range 50 us to 50 ms. 0x1 (RANGE_A): Range A 0x2 (RANGE_B): Range B 0x3 (RANGE_A_B): Ranges A and B 0x6 (RANGE_B_C): Ranges B and C 0x7 (RANGE_A_B_C): Ranges A, B, and C 0xe (RANGE_B_C_D): Ranges B, C, and D 0xf (RANGE_A_B_C_D): Ranges A, B, C, and D Value After Reset: 0x0

USP_PCIE_CAP_DEVICE_CONTROL2_DEVICE_STATUS2_REG

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	PCIE_CTRL2_CFG_END2END_TLP_PFX_BLCK End-End TLP Prefix Blocking. Controls whether the routing function is permitted to forward TLPs containing an End-End TLP Prefix. This bit affects TLPs that exit the Switch/Root Complex using the associated Port. It does not affect TLPs forwarded internally within the Switch/Root Complex. It does not affect TLPs that enter through the associated Port, that originate in the associated Port or originate in a Root Complex Integrated Device integrated with the associated Port. Blocked TLPs are reported by the TLP Prefix Blocked Error. This bit is hardwired to 1b in Root Ports that support End-End TLP Prefixes but do not support forwarding of End-End TLP Prefixes. This bit is applicable to Root Ports and Switch Ports where the End-End TLP Prefix Supported bit is set. This bit is not applicable and is RsvdP in all other cases. Note: The access attributes of this field are as follows: Wire: No access. Dbi: DEVICE_CAPABILITIES2_REG.PCIE_CAP2_CFG_END2END_TLP_PRFX_SUPPORT ? RW : RO Values: 0x0 (FORWARDING_EN): Forwarding Enabled, Function is permitted to send TLPs with End-End TLP Prefixes. 0x1 (FORWARDING_BL): Forwarding Blocked, Function is not permitted to send TLPs with End-End TLP Prefixes. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
14:13	RW	0x0	PCIE_CAP_OBFF_EN OBFF Enable. This field enables the OBFF mechanism and selects the signaling method. For more details on these encodings, see section 6.19 of PCI Express Base Specification. This field is required for all Ports that support the OBFF Capability. For a Multi-Function Device associated with an Upstream Port of a Device that implements OBFF, the field in Function 0 is of type RW, and only Function 0 controls the Component's behavior. In all other Functions of that Device, this field is of type RsvdP. Ports that do not implement OBFF are permitted to hardwire this field to 00b Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: Wire: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_OBFF_SUPPORT) then R/W else R Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_OBFF_SUPPORT) then R/W else R Values: 0x0 (DISABLED): Disabled 0x1 (EN_USING_MSG_SIG_A): Enabled using Message signaling [Variation A] 0x2 (EN_USING_MSG_SIG_B): Enabled using Message signaling [Variation B] 0x3 (EN_USING_WAKE_SIG): Enabled using WAKE# signaling Value After Reset: 0x0 Testable: writeAsRead
12:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	PCIE_CAP_LTR_EN LTR Mechanism Enable. When set to 1b, this bit enables Upstream Ports to send LTR messages and Downstream Ports to process LTR Messages. For a Multi-Function Device associated with an Upstream Port of a device that implements LTR, the bit in Function 0 is RW, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is RsvdP. Functions that do not implement the LTR mechanism are permitted to hardwire this bit to 0b. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. The write value is gated with the PCIE_CAP_LTR_SUPP field of DEVICE_CAPABILITIES2_REG. Note: RW for function #0 and RsdvP for all other functions. Note: The access attributes of this field are as follows: Wire: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_LTR_SUPP) then R/W else R Dbi: if (pf=0 && DEVICE_CAPABILITIES2_REG.PCIE_CAP_LTR_SUPP) then R/W else R Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
9:6	RO	0x0	reserved
5	RO	0x0	PCIE_CAP_ARI_FORWARD_SUPPORT_CS ARI Forwarding Enable. When set, the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. For more details, see Section 6.13 of PCI Express Base Specification. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_CPL_TIMEOUT_DISABLE Completion Timeout Disable. When set, this bit disables the Completion Timeout mechanism. This bit is required for all Functions that support the Completion Timeout Disable Capability. Functions that do not support this optional capability are permitted to hardwire this bit to 0b Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding Requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding Requests. If this is done, it is permitted to base the start time for each Request on either the time this bit was cleared or the time each Request was issued. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
3:0	RO	0x0	PCIE_CAP_CPL_TIMEOUT_VALUE Completion Timeout Value. In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is Reserved and controller hardwires it to 0000b. A Function that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50 us to 50 ms. Functions that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Ranges Supported field. All encodings other than the defined encodings are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms. Values available if Range A (50 us to 10 ms) programmability range is supported: Values available if Range B (10 ms to 250 ms) programmability range is supported: Values available if Range C (250 ms to 4 s) programmability range is supported: Values available if the Range D (4 s to 64 s) programmability range is supported: Software is permitted to change the value in this field at any time. For Requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding Requests, and is permitted to base the start time for each Request either on when this value was changed or on when each request was issued. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (DEFAULT): Default range: 50 us to 50 ms 0x1 (_50_TO_100_US): 50 us to 100 us 0x2 (_1_TO_10_MS): 1 ms to 10 ms 0x5 (_16_TO_55_MS): 16 ms to 55 ms 0x6 (_65_TO_210_MS): 65 ms to 210 ms 0x9 (_260_TO_900_MS): 260 ms to 900 ms 0xa (_1_TO_3_5_S): 1 s to 3.5 s 0xd (_4_TO_13_S): 4 s to 13 s 0xe (_17_TO_64_S): 17 s to 64 s Value After Reset: 0x0

USP_PCIE_CAP_LINK_CAPABILITIES2_REG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RO	0x0	PCIE_CAP_CROSS_LINK_SUPPORT Crosslink Supported. When set to 1b, this bit indicates that the associated Port supports crosslinks (for more details, see section 4.2.6.3.1 of PCI Express Base Specification). When set to 0b on a Port that supports Link speeds of 8.0 GT/s or higher, this bit indicates that the associated Port does not support crosslinks. When set to 0b on a Port that only supports Link speeds of 2.5 GT/s or 5.0 GT/s, this bit provides no information regarding the Port's level of crosslink support. It is recommended that this bit be Set in any Port that supports crosslinks even though doing so is only required for Ports that also support operating at 8.0 GT/s or higher Link speeds. Note: Software should use this bit when referencing fields whose definition depends on whether or not the Port supports crosslinks (for more details, see section 7.7.3.4 of PCI Express Base Specification). Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions. Value After Reset: 0x0
7:1	RO	0x07	PCIE_CAP_SUPPORT_LINK_SPEED_VECTOR Supported Link Speeds Vector. This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. For more details, see section 8.2.1 of PCI Express Base Specification. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bit 3 16.0 GT/s Bit 4 32.0 GT/s Bits 6:5 RsvdP Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions. This field has a default of (PCIE_CAP_MAX_LINK_SPEED == 0101) ? 0011111 : (PCIE_CAP_MAX_LINK_SPEED == 0100) ? 0001111 : (PCIE_CAP_MAX_LINK_SPEED == 0011) ? 0000111 : (PCIE_CAP_MAX_LINK_SPEED == 0010) ? 0000011 : 0000001 where PCIE_CAP_MAX_LINK_SPEED is a field in the LINK_CAPABILITIES_REG register. Value After Reset: 0x7 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
0	RO	0x0	reserved

USP_PCIE_CAP_LINK_CONTROL2_LINK_STATUS2_REG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	W1C	0x0	PCIE_CAP_LINK_EQ_REQ Link Equalization Request 8.0 GT/s. This bit is set by hardware to request the 8.0 GT/s Link equalization process to be performed on the Link. For more details, see sections 4.2.3 and 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
20	RO	0x0	PCIE_CAP_EQ_CPL_P3 EEqualization 8.0 GT/s Phase 3 Successful. When set to 1b, this bit indicates that Phase 3 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
19	RO	0x0	PCIE_CAP_EQ_CPL_P2 Equalization 8.0 GT/s Phase 2 Successful. When set to 1b, this bit indicates that Phase 2 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
18	RO	0x0	PCIE_CAP_EQ_CPL_P1 Equalization 8.0 GT/s Phase 1 Successful. When set to 1b, this bit indicates that Phase 1 of the 8.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
17	RO	0x0	PCIE_CAP_EQ_CPL Equalization 8.0 GT/s Complete. When set to 1b, this bit indicates that the Transmitter Equalization procedure at the 8.0 GT/s data rate has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in section 4.2.6.4.2 of PCI Express Base Specification. For Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions. For components that only support speeds below 8.0 GT/s, the controller hardwires this bit to 0b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
16	RO	0x1	PCIE_CAP_CURR_DEEMPHASIS Current De-emphasis Level. When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For components that support speeds greater than 2.5 GT/s, Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions of the Port. In M-PCIe mode this register is always 0x0. In C-PCIe mode, its contents are derived by sampling the PIPE. Values: 0x1 (_3_5DB): -3.5 dB 0x0 (_6DB): -6 dB Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:12	RW	0x0	PCIE_CAP_COMPLIANCE_PRESET Compliance Preset/De-emphasis. For 8.0 GT/s and higher Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. The encodings are defined in section 4.2.3.2 of PCI Express Base Specification . Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This field sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. When the Link is operating at 2.5 GT/s, the setting of this field has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this field to 0000b. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. This field is intended for debug and compliance testing purposes. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (_3_5_DB): -3.5 dB (for 5.0 GT/s Data Rate) 0x0 (_6_DB): -6 dB (for 5.0 GT/s Data Rate) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11	RW	0x0	PCIE_CAP_COMPLIANCE_SOS Compliance SOS. When set to 1b, the LTSSM is required to send SKP Ordered Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 0b. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
10	RW	0x0	PCIE_CAP_ENTER_MODIFIED_COMPLIANCE Enter Modified Compliance. When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
9:7	RW	0x0	PCIE_CAP_TX_MARGIN Transmit Margin, This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see Chapter 4 of PCI Express Base Specification for details of how the Transmitter voltage level is determined in various states). 001b-111b: As defined in Section 8.3.4 not all encodings are required to be implemented. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. For components that support only the 2.5 GT/s speed, the controller hardwires this bit to 000b. This field is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this field only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value. Note: This register field is sticky. Values: 0x0 (NORMAL_RANGE): Normal operating range Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
6	RO	0x0	PCIE_CAP_SEL_DEEMPHASIS Selectable De-emphasis. When the Link is operating at 5.0 GT/s speed, this bit is used to control the transmit de-emphasis of the link in specific situations. For more details, see section 4.2.6 of PCI Express Base Specification. When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is not applicable and Reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (_3_5_DB): -3.5 dB 0x0 (_6_DB): -6 dB Value After Reset: 0x0 Testable: unconstrained
5	RW	0x0	PCIE_CAP_HW_AUTO_SPEED_DISABLE Hardware Autonomous Speed Disable. When set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
4	RW	0x0	PCIE_CAP_ENTER_COMPLIANCE Enter Compliance. Software is permitted to force a Link to enter Compliance mode (at the speed indicated in the Target Link Speed field and the de-emphasis/preset level indicated by the Compliance Preset/De-emphasis field) by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. For a Multi-Function Device associated with an Upstream Port, the bit in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this bit is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3:0	RW	0x3	PCIE_CAP_TARGET_LINK_SPEED Target Link Speed. For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the desired target Link speed. All encodings other than the defined encodings are reserved. If a value is written to this field that does not correspond to a supported speed (as indicated by the Supported Link Speeds Vector), the result is undefined. If either of the Enter Compliance or Enter Modified Compliance bits are implemented, then this field must also be implemented. The default value of this field is the highest Link speed supported by the component (as reported in the Max Link Speed field of the Link Capabilities register) unless the corresponding platform/form factor requires a different default value. For both Upstream and Downstream Ports, this field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a Link into compliance mode. For Upstream Ports, if the Enter Compliance bit is Clear, this field is permitted to have no effect. For a Multi-Function Device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0000b. In M-PCIe mode, the contents of this field are derived from other registers. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (SUP_LINK_SPEED_VECTOR_BIT_0): Supported Link Speeds Vector field bit 0 0x2 (SUP_LINK_SPEED_VECTOR_BIT_1): Supported Link Speeds Vector field bit 1 0x3 (SUP_LINK_SPEED_VECTOR_BIT_2): Supported Link Speeds Vector field bit 2 0x4 (SUP_LINK_SPEED_VECTOR_BIT_3): Supported Link Speeds Vector field bit 3 0x5 (SUP_LINK_SPEED_VECTOR_BIT_4): Supported Link Speeds Vector field bit 4 0x6 (SUP_LINK_SPEED_VECTOR_BIT_5): Supported Link Speeds Vector field bit 5 0x7 (SUP_LINK_SPEED_VECTOR_BIT_6): Supported Link Speeds Vector field bit 6 Value After Reset: 0x3 Testable: unconstrained

11.4.4.9 USP_PCIE_MSIX Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_MSIX_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x003F0011	MSI-X Capability ID, Next Pointer, Control Registers
USP_PCIE_MSIX_TABLE_OFFSET_REG	0x0004	W	0x00020004	MSI-X Table Offset and BIR Register
USP_PCIE_MSIX_PBA_OFFSET_REG	0x0008	W	0x00028004	MSI-X PBA Offset and BIR Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.10 USP_PCIE_MSIX Detail Registers Description

USP_PCIE_MSIX_CAP_ID_NEXT_CTRL_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	PCI_MSIX_ENABLE MSI-X Enable. If Set and the MSI Enable bit in the MSI Message Control Register for MSI is Clear, the Function is permitted to use MSI-X to request service and is prohibited from using INTx interrupts (if implemented). System configuration software Sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a Function's service request. If Clear, the Function is prohibited from using MSI-X to request service. Value After Reset: 0x0
30	RW	0x0	PCI_MSIX_FUNCTION_MASK Function Mask. If Set, all of the vectors associated with the Function are masked, regardless of their per-vector Mask bit values. If Clear, each vector's Mask bit determines whether the vector is masked or not. Setting or Clearing the MSI-X Function Mask bit has no effect on the value of the per-vector Mask bits. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
29:27	RO	0x0	reserved

Bit	Attr	Reset Value	Description
26:16	RW	0x03f	PCI_MSIX_TABLE_SIZE MSI-X Table Size. System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1. For example, a returned value of 000 0000 0011b indicates a table size of 4. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table Size" (PCI_MSIX_TABLE_SIZE field in SHADOW_PCI_MSIX_CAP_ID_NEXT_CTRL_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_TABLE_SIZE field in the PF PCI_MSIX_CAP_ID_NEXT_CTRL_REG register. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x7f Testable: unconstrained
15:8	RW	0x00	PCI_MSIX_CAP_NEXT_OFFSET MSI-X Next Capability Pointer. This field contains the offset to the next PCI Capability structure or 00h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
7:0	RO	0x11	PCI_MSIX_CAP_ID MSI-X Capability ID. This field indicates the MSI-X Capability structure. This field must return a Capability ID of 11h indicating that this is an MSI-X Capability structure. Value After Reset: 0x11

USP_PCIE_MSIX_TABLE_OFFSET_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RW	0x00004000	PCI_MSIX_TABLE_OFFSET MSI-X Table Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table Offset" (PCI_MSIX_TABLE_OFFSET field in SHADOW_MSIX_TABLE_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_TABLE_OFFSET field in the PF MSIX_TABLE_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x4000 Testable: unconstrained

Bit	Attr	Reset Value	Description
2:0	RW	0x4	PCI_MSIX_BIR MSI-X Table BAR Indicator Register Field. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI , is used to map the Function's MSI-X Table into Memory Space. All encodings other than the defined encodings are reserved. For a 64-bit Base Address Register , the Table BIR indicates the lower DWORD. For Functions with Type 1 Configuration Space headers, BIR values 2 through 5 are also Reserved. SRIOV Note: All VFs in a single PF have the same value for "MSI-X Table BAR Indicator Register" (PCI_MSIX_BIR field in SHADOW_MSIX_TABLE_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_BIR field in the PF MSIX_TABLE_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (BAR_10): Base Address Register 10h 0x1 (BAR_14): Base Address Register 14h 0x2 (BAR_18): Base Address Register 18h 0x3 (BAR_1C): Base Address Register 1Ch 0x4 (BAR_20): Base Address Register 20h 0x5 (BAR_24): Base Address Register 24h Value After Reset: 0x4 Testable: unconstrained

USP_PCIE_MSIX_PBA_OFFSET_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RW	0x00005000	PCI_MSIX_PBA_OFFSET MSI-X PBA Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. SRIOV Note: All VFs in a single PF have the same value for "MSI-X PBA Offset" (PCI_MSIX_PBA_OFFSET field in SHADOW_MSIX_PBA_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_PBA_OFFSET field in the PF MSIX_PBA_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x5000 Testable: unconstrained
2:0	RW	0x4	PCI_MSIX_PBA_BIR MSI-X PBA BIR. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the Table BIR . SRIOV Note: All VFs in a single PF have the same value for "MSI-X PBA BIR" (PCI_MSIX_PBA_BIR field in SHADOW_MSIX_PBA_OFFSET_REG). To write this common value, you must perform a DBI_CS2 write (that is, assert the dbi_cs2 input, or the CS2 address bit for the AXI bridge) while accessing the PCI_MSIX_PBA_BIR field in the PF MSIX_PBA_OFFSET_REG register. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x4 Testable: unconstrained

11.4.4.11 USP_PCIE_AER Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_AER_EXT_CAP_HDR_OFF	0x0000	W	0x14820001	Advanced Error Reporting Extended Capability Header
USP_PCIE_AER_UNCORR_ERR_STATUS_OFF	0x0004	W	0x00000000	Uncorrectable Error Status Register
USP_PCIE_AER_UNCORR_ERR_MASK_OFF	0x0008	W	0x00400000	Uncorrectable Error Mask Register
USP_PCIE_AER_UNCORR_ERR_SEV_OFF	0x000C	W	0x00462030	Uncorrectable Error Severity Register
USP_PCIE_AER_CORR_ERR_STATUS_OFF	0x0010	W	0x00000000	Correctable Error Status Register
USP_PCIE_AER_CORR_ERR_MASK_OFF	0x0014	W	0x0000E000	Correctable Error Mask Register
USP_PCIE_AER_ADV_ERR_CAP_CTRL_OFF	0x0018	W	0x000000A0	Advanced Error Capabilities and Control Register
USP_PCIE_AER_HDR_LOG_0_OFF	0x001C	W	0x00000000	Header Log Register 0
USP_PCIE_AER_HDR_LOG_1_OFF	0x0020	W	0x00000000	Header Log Register 1
USP_PCIE_AER_HDR_LOG_2_OFF	0x0024	W	0x00000000	Header Log Register 2
USP_PCIE_AER_HDR_LOG_3_OFF	0x0028	W	0x00000000	Header Log Register 3
USP_PCIE_AER_ROOT_ERR_CMD_OFF	0x002C	W	0x00000000	Root Error Command Register. Exits only in RC mode
USP_PCIE_AER_ROOT_ERR_STATUS_OFF	0x0030	W	0x48000000	Root Error Status Register. Exists only in RC mode
USP_PCIE_AER_ERR_SRC_ID_OFF	0x0034	W	0x00000000	Error Source Identification Register.Exists only in RC mode
USP_PCIE_AER_TLP_PREFIX_LOG_1_OFF	0x0038	W	0x00000000	TLP Prefix Log Register 1
USP_PCIE_AER_TLP_PREFIX_LOG_2_OFF	0x003C	W	0x00000000	TLP Prefix Log Register 2
USP_PCIE_AER_TLP_PREFIX_LOG_3_OFF	0x0040	W	0x00000000	TLP Prefix Log Register 3
USP_PCIE_AER_TLP_PREFIX_LOG_4_OFF	0x0044	W	0x00000000	TLP Prefix Log Register 4

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.12 USP_PCIE_AER Detail Registers Description

USP_PCIE_AER_EXT_CAP_HDR_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x148	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x148 Testable: unconstrained
19:16	RW	0x2	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the End-End TLP Prefix Supported bit is set and must be 1h or 2h otherwise. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x2 Testable: unconstrained
15:0	RW	0x0001	CAP_ID AER Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

USP_PCIE_AER_UNCORR_ERR_STATUS_OFF

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	W1C	0x0	TLP_PRFX_BLOCKED_ERR_STATUS TLP Prefix Blocked Error Status. Status bit for TLP Prefix Blocked Error. Note: Not supported. Note: This register field is sticky. Value After Reset: 0x0
22	W1C	0x0	INTERNAL_ERR_STATUS Unsupported Request Error Status. This field represents status of Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
21	RO	0x0	reserved
20	W1C	0x0	UNSUPPORTED_REQ_ERR_STATUS Unsupported Request Error Status. This field represents status of Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
19	W1C	0x0	ECRC_ERR_STATUS ECRC Error Status. This field represents status of ECRC Error. Note:If CX_ECRC_ENABLE=0 the register field always reads 0. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
18	W1C	0x0	MALF_TLP_ERR_STATUS Malformed TLP Status. This field represents status of Malformed TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
17	W1C	0x0	REC_OVERFLOW_ERR_STATUS Receiver Overflow Status. Status bit for Receiver Overflow. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
16	W1C	0x0	UNEXP_CMPLT_ERR_STATUS Unexpected Completion Status. Status bit for Unexpected Completion. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15	W1C	0x0	CMPLT_ABORT_ERR_STATUS Completer Abort Status. Status bit for Completer Abort. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
14	W1C	0x0	CMPLT_TIMEOUT_ERR_STATUS Completion Timeout Status. Status for Completion Timeout. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
13	W1C	0x0	FC_PROTOCOL_ERR_STATUS Flow Control Protocol Error Status. Status bit for Flow Control Protocol Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
12	W1C	0x0	POIS_TLP_ERR_STATUS Poisoned TLP Status. Status bit for Poisoned TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:6	RO	0x00	reserved
5	W1C	0x0	SURPRISE_DOWN_ERR_STATUS Surprise Down Error Status (Optional). Status bit for Surprise Down Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

Bit	Attr	Reset Value	Description
4	W1C	0x0	DL_PROTOCOL_ERR_STATUS Data Link Protocol Error Status. Status bit for Data Link Protocol Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
3:0	RO	0x0	reserved

USP_PCIE_AER_UNCORR_ERR_MASK_OFF

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	TLP_PRFX_BLOCKED_ERR_MASK TLP Prefix Blocked Error Mask. Mask bit for TLP Prefix Blocked Error. Note: Not supported. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
24	RO	0x0	ATOMIC_EGRESS_BLOCKED_ERR_MASK AtomicOp Egress Block Mask (Optional). Mask bit for AtomicOp Egress Block Error. Note: This register field is sticky. Value After Reset: 0x0
23	RO	0x0	reserved
22	RW	0x1	INTERNAL_ERR_MASK Uncorrectable Internal Error Mask (Optional). Mask bit for Uncorrectable Internal Error. Note: This register field is sticky. Value After Reset: 0x1
21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	UNSUPPORTED_REQ_ERR_MASK Unsupported Request Error Mask. Mask bit for Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0
19	RW	0x0	ECRC_ERR_MASK ECRC Error Mask (Optional). Mask bit for ECRC Error. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
18	RW	0x0	MALF_TLP_ERR_MASK Malformed TLP Mask. Mask bit for Malformed TLP. Note: This register field is sticky. Value After Reset: 0x0
17	RW	0x0	REC_OVERFLOW_ERR_MASK Receiver Overflow Mask (Optional). This field represents Receiver Overflow Mask. Note: This register field is sticky. Value After Reset: 0x0
16	RW	0x0	UNEXP_CMPLT_ERR_MASK Unexpected Completion Mask. Mask bit for Unexpected Completion Error. Note: This register field is sticky. Value After Reset: 0x0
15	RW	0x0	CMPLT_ABORT_ERR_MASK Completer Abort Error Mask (Optional). Mask bit for Completer Abort Error. Note: This register field is sticky. Value After Reset: 0x0
14	RW	0x0	CMPLT_TIMEOUT_ERR_MASK Completion Timeout Error Mask. Mask bit for Completion Timeout Error. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
13	RW	0x0	FC_PROTOCOL_ERR_MASK Flow Control Protocol Error Mask. Mask bit for Flow Control Protocol Error. Note: This register field is sticky. Value After Reset: 0x0
12	RW	0x0	POIS_TLP_ERR_MASK Poisoned TLP Error Mask. Mask bit for Poisoned TLP Error. Note: This register field is sticky. Value After Reset: 0x0
11:6	RO	0x00	reserved
5	RO	0x0	SURPRISE_DOWN_ERR_MASK Surprise Down Error Mask. Mask bit for Surprise Down Error. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
4	RW	0x0	DL_PROTOCOL_ERR_MASK Data Link Protocol Error Mask. This field informs whether Data Link Protocol Error is masked or not. Note: This register field is sticky. Value After Reset: 0x0
3:0	RO	0x0	reserved

USP_PCIE_AER_UNCORR_ERR_SEV_OFF

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

Bit	Attr	Reset Value	Description
25	RW	0x0	TLP_PRFX_BLOCKED_ERR_SEVERITY TLP Prefix Blocked Error Severity (Optional). Severity bit for TLP Prefix Blocked Error. Note: Not supported. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
24	RW	0x0	ATOMIC_EGRESS_BLOCKED_ERR_SEVERITY AtomicOp Egress Blocked Severity (Optional). For a description of this standard PCIe register field, see the PCI Express Specification.
23	RO	0x0	reserved
22	RW	0x1	INTERNAL_ERR_SEVERITY Uncorrectable Internal Error Severity (Optional). Severity bit for Uncorrectable Internal Error. Note: This register field is sticky. Value After Reset: 0x1
21	RO	0x0	reserved
20	RW	0x0	UNSUPPORTED_REQ_ERR_SEVERITY Unsupported Request Error Severity. Severity bit for Unsupported Request Error. Note: This register field is sticky. Value After Reset: 0x0
19	RW	0x0	ECRC_ERR_SEVERITY ECRC Error Severity (Optional). Severity bit for ECRC Error. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0
18	RW	0x1	MALF_TLP_ERR_SEVERITY Malformed TLP Severity. Severity bit for Malformed TLP. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
17	RW	0x1	REC_OVERFLOW_ERR_SEVERITY Receiver Overflow Error Severity (Optional). Severity bit for Receiver Overflow Error. Note: This register field is sticky. Value After Reset: 0x1
16	RW	0x0	UNEXP_CMPLT_ERR_SEVERITY Unexpected Completion Error Severity. Severity bit for Unexpected Completion Error. Note: This register field is sticky. Value After Reset: 0x0
15	RW	0x0	CMPLT_ABORT_ERR_SEVERITY Completer Abort Error Severity (Optional). Severity bit for Completer Abort Error. Note: This register field is sticky. Value After Reset: 0x0
14	RW	0x0	CMPLT_TIMEOUT_ERR_SEVERITY Completion Timeout Error Severity. Severity bit for Completion Timeout Error. Note: This register field is sticky. Value After Reset: 0x0
13	RW	0x1	FC_PROTOCOL_ERR_SEVERITY Flow Control Protocol Error Severity (Optional). Severity bit for Flow Control Protocol Error. Note: This register field is sticky. Value After Reset: 0x1
12	RW	0x0	POIS_TLP_ERR_SEVERITY Poisoned TLP Severity. Severity bit for Poisoned TLP. Note: This register field is sticky. Value After Reset: 0x0
11:6	RO	0x00	reserved

Bit	Attr	Reset Value	Description
5	RW	0x1	SURPRISE_DOWN_ERR_SVRITY Surprise Down Error Severity (Optional). Severity bit for Surprise Down Error. Note: The access attributes of this field are as follows: Wire: No access. Dbi: LINK_CAPABILITIES_REG.PCIE_CAP_SURPRISE_DOWN_ERR_REP_CAP ? RW : RO Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	DL_PROTOCOL_ERR_SEVERITY Data Link Protocol Error Severity. Severity bit for Data Link Protocol Error. Note: This register field is sticky. Value After Reset: 0x1
3:0	RO	0x0	reserved

USP_PCIE_AER_CORR_ERR_STATUS_OFF
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	HEADER_LOG_OVERFLOW_STATUS Header Log Overflow Error Status (Optional). This field provides status of Header Log Overflow Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14	W1C	0x0	CORRECTED_INT_ERR_STATUS Corrected Internal Error Status (Optional). This field provides status of Corrected Internal Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
13	W1C	0x0	ADVISORY_NON_FATAL_ERR_STATUS Advisory Non-Fatal Error Status. Status bit for Advisory Non-Fatal Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
12	W1C	0x0	RPL_TIMER_TIMEOUT_STATUS Replay Timer Timeout Status. Status bit for Replay Timer Timeout. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:9	RO	0x0	reserved
8	W1C	0x0	REPLAY_NO_ROLEOVER_STATUS REPLAY_NUM Rollover Status. Status bit for REPLAY_NUM Rollover. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	W1C	0x0	BAD_DLLP_STATUS Bad DLLP Status. Status bit for Bad DLLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
6	W1C	0x0	BAD_TLP_STATUS Bad TLP Status. Status bit for Bad TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:1	RO	0x00	reserved
0	W1C	0x0	RX_ERR_STATUS Receiver Error Status (Optional). This field provides status of Receiver Error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_CORR_ERR_MASK_OFF
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x1	HEADER_LOG_OVERFLOW_MASK Header Log Overflow Error Mask (Optional). Masking bit for Header Log Overflow Error. Note: This register field is sticky. Value After Reset: 0x1
14	RW	0x1	CORRECTED_INT_ERR_MASK Corrected Internal Error Mask (Optional). Masking bit for Corrected Internal Error Mask. Note: This register field is sticky. Value After Reset: 0x1
13	RW	0x1	ADVISORY_NON_FATAL_ERR_MASK Advisory Non-Fatal Error Mask. Masking bit for Advisory Non-Fatal Error. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
12	RW	0x0	RPL_TIMER_TIMEOUT_MASK Replay Timer Timeout Mask. Masking bit for Replay Timer Timeout. Note: This register field is sticky. Value After Reset: 0x0
11:9	RO	0x0	reserved
8	RW	0x0	REPLAY_NO_ROLEOVER_MASK REPLAY_NUM Rollover Mask. Masking bit for REPLAY_NUM Rollover. Note: This register field is sticky. Value After Reset: 0x0
7	RW	0x0	BAD_DLLP_MASK ad DLLP Mask. Masking bit for Bad DLLP. Note: This register field is sticky. Value After Reset: 0x0
6	RW	0x0	BAD_TLP_MASK Bad TLP Mask. Masking bit for Bad TLP. Note: This register field is sticky. Value After Reset: 0x0
5:1	RO	0x00	reserved
0	RW	0x0	RX_ERR_MASK Receiver Error Mask (Optional). Masking bit for Receiver Error. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_AER_ADV_ERR_CAP_CTRL_OFF

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	CTO_PRFX_HDR_LOG_CAP TLP Prefix Log Present. If Set, this bit indicates that the Function records the prefix/header of Request TLPs that experience a Completion Timeout error. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11	RW	0x0	TLP_PRFX_LOG_PRESENT Completion Timeout Prefix/Header Log Capable. If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is Clear. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
10	RO	0x0	MULTIPLE_HEADER_EN Multiple Header Recording Enable. When Set, this bit enables the Function to record more than one error header. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Note: This register field is sticky. Value After Reset: 0x0
9	RO	0x0	MULTIPLE_HEADER_CAP Multiple Header Recording Capable. If Set, this bit indicates that the Function is capable of recording more than one error header. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	ECRC_CHECK_EN ECRC Check Enable. When Set, ECRC checking is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky. Value After Reset: 0x0
7	RO	0x1	ECRC_CHECK_CAP ECRC Check Capable. If Set, this bit indicates that the Function is capable of checking ECRC. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
6	RW	0x0	ECRC_GEN_EN ECRC Generation Enable. When Set, ECRC generation is enabled. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b. Note: This register field is sticky. Value After Reset: 0x0
5	RO	0x1	ECRC_GEN_CAP ECRC Generation Capable. If Set, this bit indicates that the Function is capable of generating ECRC. Note: This register field is sticky. Value After Reset: 0x1
4:0	RO	0x00	FIRST_ERR_POINTER First Error Pointer. The First Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_HDR_LOG_0_OFF
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	FIRST_DWORD_FOURTH_BYTE Byte 3 of Header log register of First 32-bit Data Word. This field represents fourth byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	FIRST_DWORD_THIRD_BYTE Byte 2 of Header log register of First 32-bit Data Word. This field represents third byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	FIRST_DWORD_SECOND_BYTE Byte 1 of Header log register of First 32-bit Data Word. This field represents second byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:0	RO	0x00	FIRST_DWORD_FIRST_BYTE Byte 0 of Header log register of First 32-bit Data Word. This field represents first byte of First DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_HDR_LOG_1_OFF
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	SECOND_DWORD_FOURTH_BYTE Byte 3 of Header log register of Second 32-bit Data Word. This field represents fourth byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	SECOND_DWORD_THIRD_BYTE Byte 2 of Header log register of Second 32-bit Data Word. This field represents third byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	SECOND_DWORD_SECOND_BYTE Byte 1 of Header log register of Second 32-bit Data Word. This field represents second byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: tru
7:0	RO	0x00	SECOND_DWORD_FIRST_BYTE Byte 0 of Header log register of Second 32-bit Data Word. This field represents first byte of Second DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_HDR_LOG_2_OFF

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	THIRD_DWORD_FOURTH_BYTE Byte 3 of Header log register of Third 32-bit Data Word. This field represents fourth byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	THIRD_DWORD_THIRD_BYTE Byte 2 of Header log register of Third 32-bit Data Word. This field represents third byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	THIRD_DWORD_SECOND_BYTE Byte 1 of Header log register of Third 32-bit Data Word. This field represents second byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:0	RO	0x00	THIRD_DWORD_FIRST_BYTE Byte 0 of Header log register of Third 32-bit Data Word. This field represents first byte of Third DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_HDR_LOG_3_OFF
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	FOURTH_DWORD_FOURTH_BYTE Byte 3 of Header log register of Fourth 32-bit Data Word. This field represents fourth byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	FOURTH_DWORD_THIRD_BYTE Byte 2 of Header log register of Fourth 32-bit Data Word. This field represents third byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	FOURTH_DWORD_SECOND_BYTE Byte 1 of Header log register of Fourth 32-bit Data Word. This field represents second byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:0	RO	0x00	FOURTH_DWORD_FIRST_BYTE Byte 0 of Header log register of Fourth 32-bit Data Word. This field represents first byte of Fourth DW of Header. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_ROOT_ERR_CMD_OFF
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	FATAL_ERR_REPORTING_EN Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
1	RW	0x0	NON_FATAL_ERR_REPORTING_EN Non-Fatal Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs. Value After Reset: 0x0
0	RW	0x0	CORR_ERR_REPORTING_EN Correctable Error Reporting Enable. When Set, this bit enables the generation of an interrupt when a correctable error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port. Root Complex Event Collectors provide support for the above described functionality for RCiEPs (Root Complex integrated Endpoint). Value After Reset: 0x0

USP_PCIE_AER_ROOT_ERR_STATUS_OFF

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x09	ADV_ERR_INT_MSG_NUM Advanced Error Interrupt Message Number. This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability. For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined. Note: The access attributes of this field are as follows: Wire: No access. Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x9 Testable: unconstrained
26:7	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
6	W1C	0x0	FATAL_ERR_MSG_RX One or more Fatal Error Messages Received. Set when one or more Fatal Uncorrectable error Messages have been received. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5	W1C	0x0	NON_FATAL_ERR_MSG_RX One or more Non-Fatal Error Messages Received. Set when one or more Non-Fatal Uncorrectable error Messages have been received. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	W1C	0x0	FIRST_UNCORR_FATAL First Uncorrectable Error is Fatal. Set when the first Uncorrectable error Message received is for a Fatal error. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	W1C	0x0	MUL_ERR_FATAL_NON_FATAL_RX Multiple Fatal or Non-Fatal Errors Received. Set when either a Fatal or a Non-fatal error is received and ERR_FATAL_NON_FATAL_RX is already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
2	W1C	0x0	ERR_FATAL_NON_FATAL_RX Fatal or Non-Fatal Error Received. Set when either a Fatal or a Non-fatal error Message is received and this bit is not already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	W1C	0x0	MUL_ERR_COR_RX Multiple Correctable Errors Received. Set when a Correctable error Message is received and ERR_COR_RX is already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	W1C	0x0	ERR_COR_RX Correctable Error Received. Set when a Correctable error Message is received and this bit is not already Set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_ERR_SRC_ID_OFF

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ERR_FATAL_NON_FATAL_SOURCE_ID Source of Fatal/Non-Fatal Error. Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received bit is not already set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ERR_COR_SOURCE_ID Source of Correctable Error. Loaded with the Requester ID indicated in the received ERR_COR Message when the ERR_COR Received bit is not already set. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_AER_TLP_PREFIX_LOG_1_OFF

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_1_FOURTH_BYTE Byte 3 of Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_1_THIRD_BYTE Byte 2 Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.
15:8	RO	0x00	CFG_TLP_PFX_LOG_1_SECOND_BYTE Byte 1 Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_1_FIRST_BYTE Byte 0 Error TLP Prefix Log 1. For a description of this standard PCIe register field, see the PCI Express Specification.

USP_PCIE_AER_TLP_PREFIX_LOG_2_OFF

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_2_FOURTH_BYTE Byte 3 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_2_THIRD_BYTE Byte 2 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.
15:8	RO	0x00	CFG_TLP_PFX_LOG_2_SECOND_BYTE Byte 1 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_2_FIRST_BYTE Byte 0 Error TLP Prefix Log 2. For a description of this standard PCIe register field, see the PCI Express Specification.

USP_PCIE_AER_TLP_PREFIX_LOG_3_OFF

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	CFG_TLP_PFX_LOG_3_FOURTH_BYTE Byte 3 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_3_THIRD_BYTE Byte 2 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.

Bit	Attr	Reset Value	Description
15:8	RO	0x00	CFG_TLP_PFX_LOG_3_SECOND_BYTE Byte 1 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_3_FIRST_BYTE Byte 0 Error TLP Prefix Log 3. For a description of this standard PCIe register field, see the PCI Express Specification.

USP_PCIE_AER_TLP_PREFIX_LOG_4_OFF
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CFG_TLP_PFX_LOG_4_FOURTH_BYTE Byte 3 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.
23:16	RO	0x00	CFG_TLP_PFX_LOG_4_THIRD_BYTE Byte 2 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.
15:8	RO	0x00	CFG_TLP_PFX_LOG_4_SECOND_BYTE Byte 1 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.
7:0	RO	0x00	CFG_TLP_PFX_LOG_4_FIRST_BYTE Byte 0 Error TLP Prefix Log 4. For a description of this standard PCIe register field, see the PCI Express Specification.

11.4.4.13 USP_PCIE_SPCIE Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_SPCIE_CAP_HEADER_REG	0x0000	W	0x19010019	SPCIE Capability Header
USP_PCIE_SPCIE_LINK_CONTROL3_REG	0x0004	W	0x00000000	Link Control 3 Register
USP_PCIE_SPCIE_LANE_ERR_STATUS_REG	0x0008	W	0x00000000	Lane Error Status Register
USP_PCIE_SPCIE_CAP_OFF_0CH_REG	0x000C	W	0x047F747F	Lane Equalization Control Register for lanes 1 and 0
USP_PCIE_SPCIE_CAP_OFF_10H_REG	0x0010	W	0x747F747F	Lane Equalization Control Register for lanes 3 and 2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.14 USP_PCIE_SPCIE Detail Registers Description

USP_PCIE_SPCIE_CAP_HEADER_REG
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x190	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value. Value After Reset: 0x190 Testable: unconstrained
19:16	RW	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:0	RW	0x0019	EXTENDED_CAP_ID Secondary PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0x19 Testable: unconstrained

USP_PCIE_SPCIE_LINK_CONTROL3_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	EQ_REQ_INT_EN Link Equalization Request Interrupt Enable. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: R/W Values: 0x0 (CLEAR): Clear 0x1 (SET): When Set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request 8.0 GT/s bit, the Link Equalization Request 16.0 GT/s bit, or the Link Equalization Request 32.0 GT/s bit has been set. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RO	0x0	PERFORM_EQ Perform Equalization. This bit is RW for Downstream Ports and for Upstream Ports when Crosslink Supported is 1b. This bit is not applicable and is RsvdP for Upstream Ports when the Crosslink Supported bit is 0b. If the Port does not support 8.0 GT/s, this bit is permitted to be hardwired to 0b by the controller. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: R/W Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is 1b and a 1b is written to the Retrain Link bit with the Target Link Speed field set to 8.0 GT/s or higher, the Downstream Port must perform Link Equalization. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

USP_PCIE_SPCIE_LANE_ERR_STATUS_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	W1C	0x0	LANE_ERR_STATUS Lane Error Status Bits per Lane. Each bit indicates if the corresponding Lane detected a Lane-based error. A value of 1b indicates that a Lane based-error was detected on the corresponding Lane Number. For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ. For Ports that do not support 8.0 GT/s and do not set these bits based on 8b/10b errors , this field is permitted to be hardwired to 0 by the controller. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_SPCIE_CAP_OFF_0CH_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:28	RW	0x0	USP_RX_PRESET_HINT1 Upstream Port 8.0 GT/s Receiver Preset Hint 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
27:24	RW	0x4	USP_TX_PRESET1 Upstream Port 8.0 GT/s Transmitter Preset 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0xf Testable: unconstrained
23	RO	0x0	reserved
22:20	RW	0x7	DSP_RX_PRESET_HINT1 Downstream Port 8.0 GT/s Receiver Preset Hint 1. Receiver preset hint 1 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:16	RW	0xf	DSP_TX_PRESET1 Downstream Port 8.0 GT/s Transmitter Preset 1. Transmitter preset 1 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0xf Testable: unconstraine
15	RO	0x0	reserved
14:12	RW	0x7	USP_RX_PRESET_HINT0 Upstream Port 8.0 GT/s Receiver Preset Hint 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
11:8	RW	0x4	USP_TX_PRESET0 Upstream Port 8.0 GT/s Transmitter Preset 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0xf Testable: unconstrained
7	RO	0x0	reserved
6:4	RW	0x7	DSP_RX_PRESET_HINT0 Downstream Port 8.0 GT/s Receiver Preset Hint 0. Receiver preset hint 0 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
3:0	RW	0xf	DSP_TX_PRESET0 Downstream Port 8.0 GT/s Transmitter Preset 0. Transmitter preset 0 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0xf Testable: unconstrained

USP_PCIE_SPCIE_CAP_OFF_10H_REG
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x7	USP_RX_PRESET_HINT1 Upstream Port 8.0 GT/s Receiver Preset Hint 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
27:24	RW	0x4	USP_TX_PRESET1 Upstream Port 8.0 GT/s Transmitter Preset 1. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 1 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0xf Testable: unconstrained
23	RO	0x0	reserved
22:20	RW	0x7	DSP_RX_PRESET_HINT1 Downstream Port 8.0 GT/s Receiver Preset Hint 1. Receiver preset hint 1 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:16	RW	0xf	DSP_TX_PRESET1 Downstream Port 8.0 GT/s Transmitter Preset 1. Transmitter preset 1 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0xf Testable: unconstraine
15	RO	0x0	reserved
14:12	RW	0x7	USP_RX_PRESET_HINT0 Upstream Port 8.0 GT/s Receiver Preset Hint 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Receiver preset hint 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
11:8	RW	0x4	USP_TX_PRESET0 Upstream Port 8.0 GT/s Transmitter Preset 0. The write value is gated with the PCIE_CAP_CROSS_LINK_SUPPORT field of LINK_CAPABILITIES2_REG. Field contains the Transmitter preset 0 value sent or received during 8.0 GT/s Link Equalization. Case A: When Operating port is Downstream port and whether the Crosslink is supported or not, this field representss the value sent on Lane 0 during 8.0 GT/s equalization. Case B: When Operating port is Upstream port and Crosslink Supported bit is 0, this field is intended for debug and diagnostics. It contains the value captured from Lane 0 during Link Equalization. Case C: When Operating port is Upstream port and Crosslink Supported bit is 1, Field is not used or affected by the current Link Equalization. Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A applies. For case A and C, Field is HwInit. For case B, Field is RO. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Value After Reset: 0xf Testable: unconstrained
7	RO	0x0	reserved
6:4	RW	0x7	DSP_RX_PRESET_HINT0 Downstream Port 8.0 GT/s Receiver Preset Hint 0. Receiver preset hint 0 value that may be used as a suggested setting for 8.0 GT/s receiver equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0x7 Testable: unconstrained

Bit	Attr	Reset Value	Description
3:0	RW	0xf	DSP_TX_PRESET0 Downstream Port 8.0 GT/s Transmitter Preset 0. Transmitter preset 0 value used for 8.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. For an Upstream Port if Crosslink Supported is 0b, this field is RsvdP. Otherwise, this field is HwInit. Note: The access attributes of this field are as follows: Wire: RSVDP Dbi: RSVDP Value After Reset: 0xf Testable: unconstrained

11.4.4.15 USP_PCIE_ATS Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_ATS_CAP_HDR_REG	0x0000	W	0x0001000F	ATS Extended Capability Header
USP_PCIE_ATS_CAPABILITIES_CTRL_REG	0x0004	W	0x00000020	ATS Requester Capability Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.16 USP_PCIE_ATS Detail Registers Description

USP_PCIE_ATS_CAP_HDR_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	NEXT_OFFSET Next Capability Offset. The offset to the next PCI Extended Capability structure or 000h if no other items exist in the linked list of capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x178 Testable: unconstrained

Bit	Attr	Reset Value	Description
19:16	RW	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
15:0	RW	0x000f	CAP_ID ATS Extended Capability ID. This field must return a Capability ID of 000Fh indicating that this is an ATS Extended Capability structure. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0xf Testable: unconstrained

USP_PCIE_ATS_CAPABILITIES_CTRL_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	ENABLE Enable (E). When Set, the Function is enabled to cache translations. Behavior is undefined if this bit is Set, and the value of the PASID Enable, Execute Requested Permission Enable, or Privileged Mode Requested Enable bits are changed. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0 Testable: unconstrained
20:16	RW	0x00	STU Smallest Translation Unit (STU). This value indicates to the Function the minimum number of 4096-byte blocks that is indicated in a Translation Completions or Invalidate Requests. This is a power of 2 multiplier and the number of blocks is 2 STU. A value of 0 0000b indicates one block and a value of 1 1111b indicates 2^31 blocks (or 8 TB total). Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:7	RO	0x000	reserved
6	RW	0x0	GLOBAL_INVAL_SPPRTD Global Invalidate Supported. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): The Function supports Invalidation Requests that have the Global Invalidate bit Set. 0x0 (CLEAR): The Function ignores the Global Invalidate bit in all Invalidate Requests. This bit is 0b if the Function does not support the PASID TLP Prefix. Value After Reset: 0x0 Testable: unconstrained
5	RW	0x1	PAGE_ALIGNED_REQ Page Aligned Request. If Set, indicates the Untranslated Address is always aligned to a 4096 byte boundary. Setting this field is recommended. This field permits software to distinguish between implementations compatible with this specification and those compatible with an earlier version of this specification in which a Requester was permitted to supply anything in bits [11:2]. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
4:0	RW	0x00	INVALIDATE_Q_DEPTH Invalidate Queue Depth. The number of Invalidate Requests that the Function can accept before putting backpressure on the Upstream connection. If 0 0000b, the Function can accept 32 Invalidate Requests. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained

11.4.4.17 USP_PCIE_PRS_EXT Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_PRS_EXT_CAP_HDR_REG	0x0000	W	0x00000000	Page Request Services Capability Header
USP_PCIE_PRS_EXT_CONTROL_STATUS_REG	0x0004	W	0x00000000	Page Request Services Control and Status Register
USP_PCIE_PRS_EXT_REQ_CAPACITY_REG	0x0008	W	0x00000001	Page Request Services Outstanding Capacity
USP_PCIE_PRS_EXT_REQ_ALLOCATION_REG	0x000C	W	0x00000000	Page Request Services Outstanding Allocation

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.18 USP_PCIE_PRS_EXT Detail Registers Description

USP_PCIE_PRS_EXT_CAP_HDR_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	PRS_NEXT_OFFSET Page Request Services PCI Express Extended Capability Next Offset. The offset to the next PCI Extended Capability structure or 000h if no other items exist in the linked list of capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value Value After Reset: 0x188 Testable: unconstrained
19:16	RW	0x0	PRS_CAP_VERSION Page Request Services PCI Express Extended Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is depends on the version of the specification. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	PRS_CAP_ID Page Request Services PCI Express Extended Capability ID. This field indicates that the associated extended capability structure is a Page Request Extended Capability. This field must return a Capability ID of 0013h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0x13 Testable: unconstrained

USP_PCIE_PRS_EXT_CONTROL_STATUS_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	PRS_PASID The PASID TLP Prefix is required. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix . Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (CLEAR): The Function does not expect PASID TLP Prefixes on any PRG Response Message. 0x1 (SET): The Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding Page Requests had a PASID TLP Prefix. Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
24	RO	0x0	PRS_STOPPED PRS mechanism stopped requests for additional pages. This field is only meaningful if Enable is Clear. If Enable is Set, this field is undefined. When the Enable field is Cleared, after having been previously Set, the interface transitions to the stopping state and Clears this field. After all page requests currently outstanding at the Function(s) have completed, this field is Set and the interface enters the disabled state. If there were no outstanding page requests, this field may be Set immediately when Enable is Cleared. Resetting the interface will cause an immediate transition to the disabled state. While in the stopping state, receipt of a Response Failure message will result in the immediate transition to the disabled state (Setting this field). For SR-IOV, this field is Set only when all associated Functions (PF and VFs) have stopped issuing page requests. The cfg_prs_stopped output pin reflects the value of this register field. Values: 0x0 (CLEAR): The associated page request interface either has not stopped or has stopped issuing new Page Requests but has outstanding Page Requests. 0x1 (SET): The associated page request interface has stopped issuing additional page requests and that all previously issued Page Requests have completed. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
23:18	RO	0x00	reserved
17	W1C	0x0	PRS_UPRGI PRS has received a response with Unexpected Page Request Group Index. This field, when Set, indicates that the Function has received a PRG Response Message containing a PRG index that has no matching request. This field is Set by the Function and cleared when a one is written to the field. For SR-IOV, this field is Set in the PF if any associated Function (PF or VF) receives a PRG Response Message that does has no matching request. The cfg_prs_uprgi output pin reflects the value of this register field. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
16	W1C	0x0	PRS_RESP_FAILURE PRS has received a PRG response failure. This field, when Set, indicates that the Function has received a PRG Response Message indicating a Response Failure. The Function expects no further responses from the host (any received are ignored). This field is Set by the Function and Cleared when a one is written to the field. For SR-IOV, this field is Set in the PF if any associated Function (PF or VF) receives a PRG Response Message indicating Response Failure. The cfg_prs_response_failure output pin reflects the value of this register field. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:2	RO	0x0000	reserved
1	RO	0x0	PRS_RESET Page Request Services Reset. Reads of this field return 0b. The cfg_prs_reset output pin reflects the value of this register field. Values: 0x0 (CLEAR): No action is initiated if this field is written to 0b, or if this field is written with any value while the Enable field is set. 0x1 (SET): When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit counter and pending request state for the associated Page Request Interface. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RW	0x0	PRS_ENABLE Page Request Services Enabled. If both this field and the Stopped field are Clear, then the Page Request Interface will not issue new page requests, but has outstanding page requests that have been transmitted or are queued for transmission. When the Page Request Interface is transitioned from not-Enabled to Enabled, its status flags (Stopped, Response Failure, and Unexpected Response flags) are cleared. Enabling a Page Request Interface that has not successfully Stopped has indeterminate results. The cfg_prs_enable output pin reflects the value of this register field. Values: 0x0 (CLEAR): The Page Request Interface is not allowed to issue page requests. 0x1 (SET): Indicates that the Page Request Interface is allowed to make page requests. Value After Reset: 0x0

USP_PCIE_PRS_EXT_REQ_CAPACITY_REG
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000001	PRS_OUTSTANDING_CAPACITY Page Request Services Outstanding Capacity value. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x1 Testable: unconstrained

USP_PCIE_PRS_EXT_REQ_ALLOCATION_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PRS_OUTSTANDING_ALLOCATION Page Request Services Outstanding Allocation value. This Field contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue. The cfg_prs_outstanding_allocation output pin reflects the value of this register field. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0

11.4.4.19 USP_PCIE_LTR Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_LTR_CAP_HDR_REG	0x0000	W	0x16010018	LTR Extended Capability Header
USP_PCIE_LTR_LATENCY_REG	0x0004	W	0x00000000	LTR Max Snoop and No-Snoop Latency Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.20 USP_PCIE_LTR Detail Registers Description

USP_PCIE_LTR_CAP_HDR_REG
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x160	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x190 Testable: unconstrained
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is depends on version of the specification. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
15:0	RO	0x0018	CAP_ID LTR Extended Capacity ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability for the LTR Extended Capability is 0018h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x18 Testable: unconstrained

USP_PCIE_LTR_LATENCY_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:26	RW	0x0	MAX_NO_SNOOP_LAT_SCALE Max No-Snoop Latency Scale. This register provides a scale for the value contained within the Max No-Snoop LatencyValue field. Encoding is the same as the LatencyScale fields in the LTR Message. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. Hardware operation is undefined if software writes a Not Permitted value to this field. Value After Reset: 0x0
25:16	RW	0x000	MAX_NO_SNOOP_LAT Max No-Snoop Latency Value. Along with the Max No-Snoop LatencyScale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform?s maximum supported latency or less. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. Value After Reset: 0x0
15:13	RO	0x0	reserved
12:10	RW	0x0	MAX_SNOOP_LAT_SCALE Max Snoop Latency Scale. This register provides a scale for the value contained within the Max Snoop LatencyValue field. Encoding is the same as the LatencyScale fields in the LTR Message. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. Hardware operation is undefined if software writes a Not Permitted value to this field. Value After Reset: 0x0
9:0	RW	0x000	MAX_SNOOP_LAT Max Snoop Latency Value. Along with the Max Snoop LatencyScale field,this register specifies the maximum snoop latency that a device is permitted to request. Software should set this to the platform?s maximum supported latency or less. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. Value After Reset: 0x0

11.4.4.21 USP_PCIE_L1SUB Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_L1SUB_CAP_HEADER_REG	0x0000	W	0x1D01001E	L1 Substates Extended Capability Header
USP_PCIE_L1SUB_CAPABILITY_REG	0x0004	W	0x00280A1F	L1 Substates Capability Register
USP_PCIE_L1SUB_CONTROL1_REG	0x0008	W	0x00000A00	L1 Substates Control 1 Register
USP_PCIE_L1SUB_CONTROL2_REG	0x000C	W	0x00000028	L1 Substates Control 2 Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.22 USP_PCIE_L1SUB Detail Registers Description

USP_PCIE_L1SUB_CAP_HEADER_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x1d0	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h, if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1d0 Testable: unconstrained
19:16	RW	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field is depends on version of the specification. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained
15:0	RW	0x001e	EXTENDED_CAP_ID L1SUB Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 PM Substates is 001Eh. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1e Testable: unconstrained

USP_PCIE_L1SUB_CAPABILITY_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:19	RW	0x05	PWR_ON_VALUE_SUPPORT Port T Power On Value. Along with the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register sets the time (in us) that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON_SCALE field in the L1 PM Substates Capabilities register. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Value After Reset: 0x5 Testable: writeAsRead
18	RO	0x0	reserved
17:16	RW	0x0	PWR_ON_SCALE_SUPPORT Port T Power On Scale. Specifies the scale used for the Port T_POWER_ON_VALUE field in the L1 PM Substates Capabilities register. Range of values are given below. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Values: 0x0 (_2us): Scale is 2us 0x1 (_10us): Scale is 10us 0x2 (_100us): Scale is 100us 0x3 (Reserved): Reserved Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15:8	RW	0x0a	COMM_MODE_SUPPORT Port Common Mode Restore Time. Time (in us) required for this Port to re-establish common mode. Required for all Ports for which either the PCI-PM L1.2 Supported bit is Set, ASPM L1.2 Supported bit is Set, or both are Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Value After Reset: 0xa Testable: writeAsRead
7:5	RO	0x0	reserved
4	RW	0x1	L1_PMSUB_SUPPORT L1 PM Substates ECN Supported. When Set this field indicates that this Port supports L1 PM Substates. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: R/W (sticky) Value After Reset: 0x1
3	RW	0x1	L1_1_ASPM_SUPPORT ASPM L11 Supported. When Set this field indicates that ASPM L1.1 is supported. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: R/W (sticky) Value After Reset: 0x1
2	RW	0x1	L1_2_ASPM_SUPPORT ASPM L12 Supported. When Set this field indicates that ASPM L1.2 is supported. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: R/W (sticky) Value After Reset: 0x1
1	RW	0x1	L1_1_PCIPM_SUPPORT PCI-PM L11 Supported. When Set this field indicates that PCI-PM L1.1 is supported, and must be Set by all Ports implementing L1 PM Substates. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: R/W (sticky) Value After Reset: 0x1

Bit	Attr	Reset Value	Description
0	RW	0x1	L1_2_PCIPM_SUPPORT PCI-PM L12 Supported. When Set this field indicates that PCI-PM L1.2 is supported. Note: The access attributes of this field are as follows: Wire: HWINIT Dbi: R/W (sticky) Value After Reset: 0x1

USP_PCIE_L1SUB_CONTROL1_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	L1_2_TH_SCA LTR L12 Threshold Scale. This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. Hardware operation is undefined if software writes a Not-Permitted value to this field. Required for all Ports Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP Value After Reset: 0x0 Testable: writeAsRead
28:26	RO	0x0	reserved
25:16	RW	0x000	L1_2_TH_VAL LTR L12 Threshold Value. Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 (if enabled) or L1.2 (if enabled). Required for all Ports for which the ASPM L12 Supported bit is Set, otherwise this field is of type RsvdP. Note: The access attributes of this field are as follows: Wire: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT ? RW : RSVDP Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15:8	RW	0x0a	T_COMMON_MODE Common Mode Restore Time. Sets value of TCOMMONMODE (in us), which must be used by the Downstream Ports for timing the re-establishment of common mode. This field is of type RsvdP for Upstream Ports. Note: The access attributes of this field are as follows: Wire: No access. Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RW : RSVDP Value After Reset: 0xa Testable: writeAsRead
7:4	RO	0x0	reserved
3	RW	0x0	L1_1_ASPM_EN ASPM L11 Enable. When Set this field, enables ASPM L1.1. For Ports for which the ASPM L1.1 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0
2	RW	0x0	L1_2_ASPM_EN ASPM L12 Enable. When Set this field, enables ASPM L1.2. For Ports for which the ASPM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0
1	RW	0x0	L1_1_PCIPM_EN PCI-PM L11 Enable. When Set this field, enables PCI-PM L1.1. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0
0	RW	0x0	L1_2_PCIPM_EN PCI-PM L12 Enable. When Set this field, enables PCI-PM L1.2. For Ports for which the PCI-PM L1.2 Supported bit is clear, this bit is permitted to be hardwired to 0. Required for both Upstream and Downstream Ports. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the L1 PM Substates Supported field in the L1 PM Substates Capabilities Register is Set. Value After Reset: 0x0

USP_PCIE_L1SUB_CONTROL2_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x05	T_POWER_ON_VALUE T Power On Value. Along with the T_POWER_ON_SCALE sets the minimum amount of time (in us) that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON_SCALE field. Required for all Ports that support L1.2, otherwise this field is of type RsvdP.This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set. Note: The access attributes of this field are as follows: Wire: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Value After Reset: 0x5 Testable: writeAsRead
2	RO	0x0	reserved
1:0	RW	0x0	T_POWER_ON_SCALE T Power On Scale. Specifies the scale used for T_POWER_ON_VALUE. Range of values are given below. Required for all Ports that support L1.2, otherwise this field is of type RsvdP. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. The Port behavior is undefined if this field is modified when either the ASPM L1.2 Enable and/or PCI-PM L1.2 Enable bit(s) are set. Note: The access attributes of this field are as follows: Wire: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Dbi: L1SUB_CAPABILITY_REG.L1_2_ASPM_SUPPORT||L1SUB_CAPABILITY_REG.L1_2_PCIPM_SUPPORT ? RWS : RSVDP Values: 0x0 (_2us): Scale is 2us 0x1 (_10us): Scale is 10us 0x2 (_100us): Scale is 100us 0x3 (Reserved): Reserved Value After Reset: 0x0 Testable: writeAsRead

11.4.4.23 USP_PCIE_DPA Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_DPA_EXT_CAP_HDR_REG	0x0000	W	0x1A010016	DPA Extended Capability Header
USP_PCIE_DPA_CAP_REG	0x0004	W	0xFF801107	DPA Capability Register
USP_PCIE_DPA_LAT_IND_REG	0x0008	W	0x00000000	DPA Latency Indicator Register
USP_PCIE_DPA_STATUS_CNTRL_REG	0x000C	W	0x00000100	DPA Status and Control Register
USP_PCIE_DPA_PWR_ALLOC_ARRAY0	0x0010	W	0x1D1E1F20	DSP Substate Power Allocation Register 3~0
USP_PCIE_DPA_PWR_ALLOC_ARRAY4	0x0014	W	0x191A1B1C	DSP Substate Power Allocation Register 7~4

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.24 USP_PCIE_DPA Detail Registers Description

USP_PCIE_DPA_EXT_CAP_HDR_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x1a0	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1d0 Testable: unconstrained
19:16	RO	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:0	RO	0x0016	EXT_CAP_ID DPA Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the DPA Extended Capability is 0016h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x16 Testable: unconstrained

USP_PCIE_DPA_CAP_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	XLCY1 Transition Latency Value 1 (Xlcy1). This value is multiplied by the Transition Latency Unit to determine the maximum Transition Latency for the substate. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0xff
23:16	RW	0x80	XLCY0 Transition Latency Value 0 (Xlcy0). This value is multiplied by the Transition Latency Unit to determine the maximum Transition Latency for the substate. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x80
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x1	PAS Power Allocation Scale. The encodings provide the scale to determine power allocation per substate in Watts. The value corresponding to the substate in the Substate Power Allocation field is multiplied by this field to determine the power allocation for the substate. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (_10.0X): 10.0x 0x1 (_1.0X): 1.0x 0x2 (_0.1X): 0.1x 0x3 (_0.01X): 0.01x Value After Reset: 0x1
11:10	RO	0x0	reserved
9:8	RW	0x1	TLUNIT Transition Latency Unit (TLunit). A substate's Transition Latency Value is multiplied by the Transition Latency Unit to determine the maximum Transition Latency for the substate. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (_1MS): 1ms 0x1 (_10MS): 10ms 0x2 (_100MS): 100ms 0x3 (RSVD): Reserved Value After Reset: 0x1
7:5	RO	0x0	reserved
4:0	RW	0x07	SUBSTATE_MAX Maximum Substate Number. Value of this field indicates the maximum substate number, which is the total number of supported substates minus one. A value of 0 0000b indicates support for one substate. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x7

USP_PCIE_DPA_LAT_IND_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	X1_INDICATOR1 Transition Latency Indicator Bits. Each bit indicates which Transition Latency Value is associated with the corresponding substate. A value of 0b indicates Transition Latency Value 0 ; a value of 1b indicates Transition Latency Value 1. Only bits [Substate_Max :0] are defined. Bits above Substate_Max are RsvdP. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_DPA_STATUS_CNTRL_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	SUBSTATE_CONTROL Substate Control. This field can be used by the software to configure the Function substate. The software can write the substate value in this field to initiate a substate transition. When the Substate Control Enabled bit in the DPA Status Register is Set, this field determines the Function substate. When the Substate Control Enabled bit in the DPA Status Register is Clear, this field has no effect on the Function substate. Value After Reset: 0x0
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x1	SUBSTATE_CONTROL_EN Substate Control Enabled. This field can be used by the software to disable the Substate Control field in the DPA Control Register. Hardware sets this bit following a Conventional Reset or FLR. Software can clear this bit by writing a 1b to it. Software cannot set this bit directly. Note: The access attributes of this field are as follows: Wire: RW1C Dbi: R/W Values: 0x1 (SET): The Substate Control field determines the current substate. 0x0 (CLEAR): The Substate Control field has no effect on the current substate. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
7:5	RO	0x0	reserved
4:0	RW	0x00	SUBSTATE_STATUS Substate Status. This field indicates current substate for this Function. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DPA_PWR_ALLOC_ARRAY0
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x1d	PWR_ALLOC_VAL3 Substate Power Allocation Substate 3. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 3. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x1d

Bit	Attr	Reset Value	Description
23:16	RW	0x1e	PWR_ALLOC_VAL2 Substate Power Allocation Substate 2. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 2. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x1e
15:8	RW	0x1f	PWR_ALLOC_VAL1 Substate Power Allocation Substate 1. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 1. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x1f
7:0	RW	0x20	PWR_ALLOC_VAL0 Substate Power Allocation Substate 0. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 0. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x20

USP_PCIE_DPA_PWR_ALLOC_ARRAY4

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RW	0x19	PWR_ALLOC_VAL7 Substate Power Allocation Substate 7. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 7. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x19

Bit	Attr	Reset Value	Description
23:16	RW	0x1a	PWR_ALLOC_VAL6 Substate Power Allocation Substate 6. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 6. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x1a
15:8	RW	0x1b	PWR_ALLOC_VAL5 Substate Power Allocation Substate 5. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 5. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x1b
7:0	RW	0x1c	PWR_ALLOC_VAL4 Substate Power Allocation Substate 4. The value in this field is multiplied by the Power Allocation Scale to determine power allocation in Watts for the substate 4. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x1c

11.4.4.25 USP_PCIE_RAS_DES Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_RAS_DES_CAP_HEADER_REG	0x0000	W	0x2A01000B	Vendor-Specific Extended Capability Header
USP_PCIE_RAS_DES_VENDOR_SPECIFIC_HEADER_REG	0x0004	W	0x10040002	Vendor-Specific Header
USP_PCIE_RAS_DES_EVENT_COUNTER_CONTROL_REG	0x0008	W	0x00000000	Event Counter Contro
USP_PCIE_RAS_DES_EVENT_COUNTER_DATA_REG	0x000C	W	0x00000000	Event Counter Data
USP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_CONTROL_REG	0x0010	W	0x00000000	Time-based Analysis Control

Name	Offset	Size	Reset Value	Description
USP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_REG	0x0014	W	0x00000000	Time-based Analysis Data
USP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_63_32_REG	0x0018	W	0x00000000	Upper 32 bits of Time-based Analysis Data
USP_PCIE_RAS_DES_EINJ_ENABLE_REG	0x0030	W	0x00000000	Error Injection Enable
USP_PCIE_RAS_DES_EINJ0_CRC_REG	0x0034	W	0x00000000	Error Injection Control 0 (CRC Error)
USP_PCIE_RAS_DES_EINJ1_SEQNUM_REG	0x0038	W	0x00000000	Error Injection Control 1 (Sequence Number Error)
USP_PCIE_RAS_DES_EINJ2_DLLP_REG	0x003C	W	0x00000000	Error Injection Control 2 (DLLP Error)
USP_PCIE_RAS_DES_EINJ3_SYMBOL_REG	0x0040	W	0x00000000	Error Injection Control 3 (Symbol Error)
USP_PCIE_RAS_DES_EINJ4_FC_REG	0x0044	W	0x00000000	Error Injection Control 4 (FC Credit Error)
USP_PCIE_RAS_DES_EINJ5_SP_TLP_REG	0x0048	W	0x00000000	Error Injection Control 5 (Specific TLP Error)
USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H0_REG	0x004C	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #0)
USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H1_REG	0x0050	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #1)
USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H2_REG	0x0054	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #2)
USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H3_REG	0x0058	W	0x00000000	Error Injection Control 6 (Compare Point Header DWORD #3)
USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H0_REG	0x005C	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #0)
USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H1_REG	0x0060	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #1)
USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H2_REG	0x0064	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #2)
USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H3_REG	0x0068	W	0x00000000	Error Injection Control 6 (Compare Value Header DWORD #3)
USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H0_REG	0x006C	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #0)
USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H1_REG	0x0070	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #1)
USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H2_REG	0x0074	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #2)

Name	Offset	Size	Reset Value	Description
USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H3_REG	0x0078	W	0x00000000	Error Injection Control 6 (Change Point Header DWORD #3)
USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H0_REG	0x007C	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #0)
USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H1_REG	0x0080	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #1)
USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H2_REG	0x0084	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #2)
USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H3_REG	0x0088	W	0x00000000	Error Injection Control 6 (Change Value Header DWORD #3)
USP_PCIE_RAS_DES_EINJ6_TLP_REG	0x008C	W	0x00000000	Error Injection Control 6 (Packet Error)
USP_PCIE_RAS_DES_SD_CONTROL1_REG	0x00A0	W	0x00000000	Silicon Debug Control 1
USP_PCIE_RAS_DES_SD_CONTROL2_REG	0x00A4	W	0x00000000	Silicon Debug Control 2
USP_PCIE_RAS_DES_SD_STATUS_L1LANE_REG	0x00B0	W	0x00180000	Silicon Debug Status(Layer1 Per-lane)
USP_PCIE_RAS_DES_SD_STATUS_L1LTSSM_REG	0x00B4	W	0x00000200	Silicon Debug Status(Layer1 LTSSM)
USP_PCIE_RAS_DES_SD_STATUS_PM_REG	0x00B8	W	0x00000000	Silicon Debug Status(PM)
USP_PCIE_RAS_DES_SD_STATUS_L2_REG	0x00BC	W	0x00FFF000	Silicon Debug Status(Layer2)
USP_PCIE_RAS_DES_SD_STATUS_L3FC_REG	0x00C0	W	0x00000000	Silicon Debug Status(Layer3 FC)
USP_PCIE_RAS_DES_SD_STATUS_L3_REG	0x00C4	W	0x00000000	Silicon Debug Status(Layer3)
USP_PCIE_RAS_DES_SD_EQ_CONTROL1_REG	0x00D0	W	0x00000000	Silicon Debug EQ Control 1
USP_PCIE_RAS_DES_SD_EQ_CONTROL2_REG	0x00D4	W	0x00000000	Silicon Debug EQ Control 2
USP_PCIE_RAS_DES_SD_EQ_CONTROL3_REG	0x00D8	W	0x00000000	Silicon Debug EQ Control 3
USP_PCIE_RAS_DES_SD_EQ_STATUS1_REG	0x00E0	W	0x00000000	Silicon Debug EQ Status 1
USP_PCIE_RAS_DES_SD_EQ_STATUS2_REG	0x00E4	W	0x00000000	Silicon Debug EQ Status 2
USP_PCIE_RAS_DES_SD_EQ_STATUS3_REG	0x00E8	W	0x00000000	Silicon Debug EQ Status 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.26 USP_PCIE_RAS_DES Detail Registers Description

USP_PCIE_RAS_DES_CAP_HEADER_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x2a0	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value Value After Reset: 0x2d0 Testable: writeAsRead
19:16	RW	0x1	CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Value of this field is depends on the version of the specification. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15:0	RW	0x000b	EXTENDED_CAP_ID PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Vendor-Specific Extended Capability is 000Bh. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0xb Testable: writeAsRead

USP_PCIE_RAS_DES_VENDOR_SPECIFIC_HEADER_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:20	RO	0x100	VSEC_LENGTH VSEC Length. This field indicates the number of bytes in the entire VSEC structure, including the Vendor-Specific Extended Capability Header, the Vendor-Specific Header, and the vendor-specific registers. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value Value After Reset: 0x100
19:16	RO	0x4	VSEC_REV VSEC Rev. This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x4
15:0	RO	0x0002	VSEC_ID VSEC ID. This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0x2

USP_PCIE_RAS_DES_EVENT_COUNTER_CONTROL_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	EVENT_COUNTER_EVENT_SELECT Event Counter Data Select. This field in conjunction with the EVENT_COUNTER_LANE_SELECT field indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. 27-24: Group number(4-bit: 0..0x7) 23-16: Event number(8-bit: 0..0x13) within the Group .. For detailed definitions of Group number and Event number, see the RAS DES chapter in the Databook. Note: This register field is sticky. Values: 0x0 (EBUF_OVERFLOW): Ebuf Overflow 0x1 (EBUF_UNDERRUN): Ebuf Underrun 0x700 (TX_MEM_WRITE): Tx Memory Write 0x713 (RX_MSG_TLP): Rx Message TLP Value After Reset: 0x0 Testable: writeAsRead
15:12	RO	0x0	reserved
11:8	RW	0x0	EVENT_COUNTER_LANE_SELECT Event Counter Lane Select. This field in conjunction with EVENT_COUNTER_EVENT_SELECT indexes the Event Counter data returned by the EVENT_COUNTER_DATA_REG register. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
7	RO	0x0	EVENT_COUNTER_STATUS Event Counter Status. This register returns the current value of the Event Counter selected by the following fields: EVENT_COUNTER_EVENT_SELECT EVENT_COUNTER_LANE_SELECT Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6:5	RO	0x0	reserved
4:2	WO	0x0	EVENT_COUNTER_ENABLE Event Counter Enable. Enables/disables the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. By default, all event counters are disabled. You can enable/disable a specific Event Counter by writing the 'per event off' or 'per event on' codes. You can enable/disable all event counters by writing the 'all on' or 'all off' codes. The read value is always '0'. For other values no change. Values: 0x1 (PER_EVENT_OFF): per event off 0x3 (PER_EVENT_ON): per event on 0x5 (ALL_OFF): all off 0x7 (ALL_ON): all on Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
1:0	WO	0x0	EVENT_COUNTER_CLEAR Event Counter Clear. Clears the Event Counter selected by the EVENT_COUNTER_EVENT_SELECT and EVENT_COUNTER_LANE_SELECT fields in this register. You can clear the value of a specific Event Counter by writing the 'per clear' code and you can clear all event counters at once by writing the 'all clear' code. The read value is always '0'. Other values are reserved. Values: 0x0 (NO_CHANGE): no change 0x1 (PER_CLEAR): per clear 0x2 (NO_CHANGE_2): no change 0x3 (ALL_CLEAR): all clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EVENT_COUNTER_DATA_REG
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EVENT_COUNTER_DATA Event Counter Data. This register returns the data selected by the following fields: EVENT_COUNTER_EVENT_SELECT in EVENT_COUNTER_CONTROL_REG Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_CONTROL_REG
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	TIME_BASED_REPORT_SELECT Time-based Report Select. Selects what type of data is measured for the selected duration (TIME_BASED_DURATION_SELECT), and returned in TIME_BASED_ANALYSIS_DATA. Each type of data is measured using one of three types of units: Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x00] * TIME_BASED_ANALYSIS_DATA. Values 0-4 and 7-8 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Aux_clk Cycles. Total time in ps is [Period of platform specific clock] * TIME_BASED_ANALYSIS_DATA. Values 5, 6, and 9 correspond to aux_clk Cycles. Core_clk Cycles for 20GT/s, 25GT/s (CCIX ESM data rate). Total time in ps is [Value of TIME_BASED_ANALYSIS_DATA returned when TIME_BASED_REPORT_SELECT=0x10] * TIME_BASED_ANALYSIS_DATA. Values 10-14 and 17-18 correspond to Core_clk Cycles for 2.5GT/s, 5.0GT/s, 8.0GT/s, 16.0GT/s, 32GT/s. Data Bytes. Actual amount of bytes is 16 * TIME_BASED_ANALYSIS_DATA. Values 20-23 correspond to data bytes. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (ONE_CYCLE): Duration of 1 cycle 0x1 (TX_L0S): TxL0s 0x2 (RX_L0S): RxL0s 0x3 (L0): L0 0x4 (L1): L1 0x7 (CFG_RCVRY): Configuration/Recovery 0x8 (TX_RX_L0S): TxL0s and RxL0s 0x5 (L1_1): L1.1 0x6 (L1_2): L1.2 0x9 (L1_AUX): L1 aux 0x10 (_1_CYCLE): Duration of 1 cycle 0x11 (TX_L0S_): TxL0s 0x12 (RX_L0S_): RxL0s 0x13 (L0_): L0 0x14 (L1_): L1 0x17 (CFG_RCVRY_): Configuration/Recovery 0x18 (TX_RX_L0S_): TxL0s and RxL0s 0x20 (TX_PCIE_TLP): Tx PCIe TLP data payload Bytes 0x21 (RX_PCIE_TLP): Rx PCIe TLP data payload Bytes 0x22 (TX_CCIX_TLP): Tx CCIX TLP data payload Bytes 0x23 (RX_CCIX_TLP): Rx CCIX TLP data payload Bytes Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
23:16	RO	0x00	reserved
15:8	RW	0x00	TIME_BASED_DURATION_SELECT Time-based Duration Select. Selects the duration of time-based analysis. When "manual control" is selected and TIMER_START is set to '1', this analysis never stops until TIMER_STOP is set to '0'. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (MANUAL): Manual control 0x1 (_1_MS): 1ms 0x2 (_2_MS): 10ms 0x3 (_100_MS): 100ms 0x4 (_1_S): 1s 0x5 (_2_S): 2s 0x6 (_4_S): 4s 0xff (_4_US): 4us (Debug purpose) Value After Reset: 0x1 Testable: writeAsRead
7:1	RO	0x00	reserved
0	RW	0x0	TIMER_START Timer Start. This bit will be cleared automatically when the measurement is finished. Note: The app_ras_des_tba_ctrl input also sets the contents of this field and controls the measurement start/stop. Note: This register field is sticky. Values: 0x1 (START_RESTART): Start/Restart 0x0 (STOP): Stop Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_REG
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TIME_BASED_ANALYSIS_DATA Time Based Analysis Data. This register returns the data selected by the TIME_BASED_REPORT_SELECT field in TIME_BASED_ANALYSIS_CONTROL_REG. The results are cleared when next measurement starts. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: untestable Volatile: true

USP_PCIE_RAS_DES_TIME_BASED_ANALYSIS_DATA_63_32_REG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	TIME_BASED_ANALYSIS_DATA_63_32 Upper 32 bits of Time Based Analysis Data. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ_ENABLE_REG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	ERROR_INJECTION6_ENABLE Error Injection6 Enable (Specific TLP Error). Enables insertion of errors into the packets that you select. You can set this bit to '1' when you have disabled RAS datapath protection (DP) by setting CX_RASDP = CX_RASDP_RAM_PROT =0. You can set this bit to '1' when you have disabled the address translation by setting ADDR_TRANSLATION_SUPPORT_EN=0. For more details, see the EINJ6_COMPARE_*_REG/EINJ6_CHANGE_*_REG/EINJ6_TLP_REG registers. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5	RW	0x0	ERROR_INJECTION5_ENABLE Error Injection5 Enable (TLP Duplicate/Nullify Error). Enables insertion of duplicate/nullified TLPs. For more details, see the EINJ5_SP_TLP_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
4	RW	0x0	ERROR_INJECTION4_ENABLE Error Injection4 Enable (FC Credit Update Error). Enables insertion of errors into UpdateFCs. For more details, see the EINJ4_FC_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	RW	0x0	ERROR_INJECTION3_ENABLE Error Injection3 Enable (Symbol DataK Mask Error or Sync Header Error). Enables DataK masking of special symbols or the breaking of the sync header. For more details, see the EINJ3_SYMBOL_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RW	0x0	ERROR_INJECTION2_ENABLE Error Injection2 Enable (DLLP Error). Enables insertion of DLLP errors. For more details, see the EINJ2_DLLP_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
1	RW	0x0	ERROR_INJECTION1_ENABLE Error Injection1 Enable (Sequence Number Error). Enables insertion of errors into sequence numbers. For more details, see the EINJ1_SEQNUM_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RW	0x0	ERROR_INJECTION0_ENABLE Error Injection0 Enable (CRC Error). Enables insertion of errors into various CRC. For more details, see the EINJ0_CRC_REG register. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ0_CRC_REG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	EINJ0_CRC_TYPE Error injection type. Selects the type of CRC error to be inserted. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (TLP_LCRC_ERR): (TX Path) New TLP's LCRC error injection 0x1 (_16b_CRC_ERR_ACK_NAK_DLLP): (TX Path) 16bCRC error injection of ACK/NAK DLLP 0x2 (_16b_CRC_ERR_UPD_FC): (TX Path) 16bCRC error injection of Update-FC DLLP 0x3 (TLP_ECRC_ERR): (TX Path) New TLP's ECRC error injection 0x4 (FCRC_ERR_TLP): (TX Path) TLP's FCRC error injection (128b/130b) 0x5 (PARITY_TSOS_ERR): (TX Path) Parity error of TSOS (128b/130b) 0x6 (PARITY_SKPOS_ERR): (TX Path) Parity error of SKPOS (128b/130b) 0x8 (LCRC_ERR): (RX Path) LCRC error injection 0xb (ECRC_ERR): (RX Path) ECRC error injection Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ0_COUNT Error injection count. Indicates the number of errors. This register is decremented when the errors have been inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION0_ENABLE in EINJ_ENABLE_REG returns 0b. If the counter value is 0x00 and ERROR_INJECTION0_ENABLE=1, the errors are inserted until ERROR_INJECTION0_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ1_SEQNUM_REG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	EINJ1_BAD_SEQNUM Bad sequence number. Indicates the value to add/subtract from the naturally-assigned sequence numbers. This value is represented by two's complement. For example: Set Type, SEQ# and Count EINJ1_SEQNUM_TYPE =0 (Insert errors into new TLPs) EINJ1_BAD_SEQNUM =0x1FFD (represents -3) EINJ1_COUNT =1 Enable Error Injection ERROR_INJECTION1_ENABLE =1 Send a TLP From the Core's Application Interface Assume SEQ#5 is given to the TLP. The SEQ# is Changed to #2 by the Error Injection Function in Layer2. 5 + (-3) = 2 The TLP with SEQ#2 is Transmitted to PCIe Link. Note: This register field is sticky. Values: 0xfff (MAX_VAL): +4095 0x1001 (MIN_VAL): -4095 Value After Reset: 0x0 Testable: writeAsRead
15:9	RO	0x00	reserved
8	RW	0x0	EINJ1_SEQNUM_TYPE Sequence number type. Selects the type of sequence number. Note: This register field is sticky. Values: 0x0 (TLP_ERR): Insertion of New TLP's SEQ# error 0x1 (ACK_NAK_DLLP_ERR): Insertion of ACK/NAK DLLP's SEQ# Error Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EINJ1_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION1_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION1_ENABLE=1, the errors are inserted until ERROR_INJECTION1_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ2_DLLP_REG

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	EINJ2_DLLP_TYPE DLLP Type. Selects the type of DLLP errors to be inserted. Note: This register field is sticky. Values: 0x0 (ACK_NACK_DLLP): ACK/NAK DLLP's transmission block 0x1 (UPD_FC_DLLP): Update FC DLLP's transmission block 0x2 (NAK_DLLP): Always Transmission for NAK DLLP 0x3 (RSVD): Reserved Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ2_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and the error is inserted, ERROR_INJECTION2_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION2_ENABLE =1, the errors are inserted until ERROR_INJECTION2_ENABLE is set to '0'. This register is affected only when EINJ2_DLLP_TYPE =2'10b. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ3_SYMBOL_REG

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	EINJ3_SYMBOL_TYPE Error Type. 8b/10b encoding - Mask K symbol. It is not supported to insert errors into the first ordered-set after exiting from TxElecIdle when CX_FREQ_STEP_EN has been enabled. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x0 (RSVD_OR_INVRT_SYNC_HDR): Invert sync header for 128b/130b encoding or this field is reserved for 8b/10b encoding. 0x1 (COM_PAD_TS1): COM/PAD(TS1 Order set) 0x2 (COM_PAD_TS2): COM/PAD(TS2 Order set) 0x3 (COM_FTS): COM/FTS(FTS Order set) 0x4 (COM_IDL): COM/IDL(E-Idle Order set) 0x5 (END_EDB): END/EDB Symbol 0x6 (STP_SDP): STP/SDP Symbol 0x7 (COM_SKP): COM/SKP(SKP Order set) Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ3_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION3_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION3_ENABLE =1, the errors are inserted until ERROR_INJECTION3_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ4_FC_REG

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	EINJ4_BAD_UPDFC_VALUE Bad update-FC credit value. Indicates the value to add/subtract from the UpdateFC credit. This value is represented by two's complement. Note: This register field is sticky. Values: 0xfff (MAX_VAL): +4095 0x1001 (MIN_VAL): -4095 Value After Reset: 0x0 Testable: writeAsRead
15	RO	0x0	reserved
14:12	RW	0x0	EINJ4_VC_NUMBER VC Number. Indicates target VC Number. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min Value 0x7 (MAX_VAL): Min Value Value After Reset: 0x0 Testable: writeAsRead
11	RO	0x0	reserved
10:8	RW	0x0	EINJ4_UPDFC_TYPE Update-FC type. Selects the credit type. Note: This register field is sticky. Values: 0x0 (POSTED_TLP_HDR): Posted TLP Header Credit value control 0x1 (NON_POSTED_TLP_HDR): Non-Posted TLP Header Credit value control 0x2 (CMPL_TLP_HDR): Completion TLP Header Credit value control 0x3 (RSERVED): Reserved 0x4 (POSTED_TLP_DATA): Posted TLP Data Credit value control 0x5 (NON_POSTED_TLP_DATA): Non-Posted TLP Data Credit value control 0x6 (CMPL_TLP_DATA): Completion TLP Data Credit value control 0x7 (RSVD): Reserved Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EINJ4_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION4_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION4_ENABLE =1, the errors are inserted until ERROR_INJECTION4_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ5_SP_TLP_REG
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	EINJ5_SPECIFIED_TLP Specified TLP. Selects the specified TLP to be inserted. Note: This register field is sticky. Values: 0x0 (DUPLICATE_DLLP): Generates duplicate TLPs by handling ACK DLLP as NAK DLLP. 0x1 (NULLIFIED_TLP): Generates Nullified TLP (Original TLP will be stored in retry buffer). Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ5_COUNT Error injection count. Indicates the number of errors. This register is decremented as the errors are being inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION5_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION5_ENABLE =1, the errors are inserted until ERROR_INJECTION5_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H0_REG
Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H0 Packet Compare Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H1_REG
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H1 Packet Compare Point: 2nd DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H2_REG
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H2 Packet Compare Point: 3rd DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_COMPARE_POINT_H3_REG

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_POINT_H3 Packet Compare Point: 4th DWORD. Specifies which Tx TLP header DWORD#0 bits to compare with the corresponding bits in the Packet Compare Value registers (EINJ6_COMPARE_VALUE*). When all specified bits (in the Tx TLP header and EINJ6_COMPARE_VALUE*) match, the controller inserts errors into the TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H0_REG

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H0 Packet Compare Value: 1st DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H1_REG

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H1 Packet Compare Value: 2nd DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H2_REG

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H2 Packet Compare Value: 3rd DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_COMPARE_VALUE_H3_REG

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_COMPARE_VALUE_H3 Packet Compare Value: 4th DWORD. Specifies the value to compare against Tx the TLP header DWORD#0 bits specified in the Packet Compare Point registers (EINJ6_COMPARE_POINT*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H0_REG

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H0 Packet Change Point: 1st DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H1_REG
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H1 Packet Change Point: 2nd DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H2_REG
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H2 Packet Change Point: 3rd DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_POINT_H3_REG
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_POINT_H3 Packet Change Point: 4th DWORD. Specifies which Tx TLP header DWORD#0 bits to replace with the corresponding bits in the Packet Change Value registers (EINJ6_CHANGE_VALUE*). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H0_REG
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H0 Packet Change Value: 1st DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H1_REG
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H1 Packet Change Value: 2nd DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H2_REG
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H2 Packet Change Value: 3rd DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_CHANGE_VALUE_H3_REG

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EINJ6_CHANGE_VALUE_H3 Packet Change Value: 4th DWORD. Specifies replacement values for the Tx TLP header DWORD#0 bits defined in the Packet Change Point registers (EINJ6_CHANGE_POINT*). Only applies when the EINJ6_INVERTED_CONTROL field in EINJ6_TLP_REG is '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_EINJ6_TLP_REG

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:9	RW	0x0	EINJ6_PACKET_TYPE Packet type. Selects the TLP packets to inject errors into. All encodings other than the specified encodings are reserved. Note: This register field is sticky. Values: 0x0 (HEADER): TLP Header 0x1 (TLP_FIRST_4_DW): TLP Prefix 1st 4-DWORDs 0x2 (TLP_SECOND_DW): TLP Prefix 2nd -DWORDs Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
8	RW	0x0	EINJ6_INVERTED_CONTROL Inverted Error Injection Control. Encodded vlues given as above. Note: This register field is sticky. Values: 0x0 (REPLACE): EINJ6_CHANGE_VALUE_H[0/1/2/3] is used to replace bits specified by EINJ6_CHANGE_POINT_H[0/1/2/3]. 0x1 (IGNORE): EINJ6_CHANGE_VALUE_H[0/1/2/3] is ignored and inverts bits specified by EINJ6_CHANGE_POINT_H[0/1/2/3]. Value After Reset: 0x0 Testable: writeAsRead
7:0	RW	0x00	EINJ6_COUNT Error Injection Count. Indicates the number of errors to insert. This counter is decremented while errors are been inserted. If the counter value is 0x01 and error is inserted, ERROR_INJECTION6_ENABLE in EINJ_ENABLE_REG returns '0'. If the counter value is 0x00 and ERROR_INJECTION6_ENABLE=1, errors are inserted until ERROR_INJECTION6_ENABLE is set to '0'. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_CONTROL1_REG

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	LOW_POWER_INTERVAL Low Power Entry Interval Time. Interval Time that the controller starts monitoring RXELECIDLE signal after L0s/L1/L2 entry. You should set the value according to the latency from receiving EIOS to, RXELECIDLE assertion at the PHY. Note: This register field is sticky. Values: 0x0 (_40NS): 40ns 0x1 (_160NS): 160ns 0x2 (_320NS): 320ns 0x3 (_640NS): 640ns Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21:20	RW	0x0	TX_EIOS_NUM Number of Tx EIOS. This register sets the number of transmit EIOS for L0s/L1 entry and Disable/Loopback/Hot-reset exit. The controller selects the greater value between this register and the value defined by the PCI-SIG specification. Note: This register field is sticky. Values: 0x0 (G2_2_EIOS_OTHER_SPEED_1_EIOS): (2.5GT/s, 8.0GT/s or higher) 1 or (5.0GT/s) 2 0x1 (G2_8_EIOS_OTHER_SPEED_4_EIOS): (2.5GT/s, 8.0GT/s or higher) 4 or (5.0GT/s) 8 0x2 (G2_16_EIOS_OTHER_SPEED_8_EIOS): (2.5GT/s, 8.0GT/s or higher) 8 or (5.0GT/s) 16 0x3 (G2_32_EIOS_OTHER_SPEED_16_EIOS): (2.5GT/s, 8.0GT/s or higher) 16 or (5.0GT/s) 32 Value After Reset: 0x0 Testable: writeAsRead
19:17	RO	0x0	reserved
16	RW	0x0	FORCE_DETECT_LANE_EN Force Detect Lane Enable. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set, the controller ignores receiver detection from PHY during LTSSM Detect state and uses FORCE_DETECT_LANE. Value After Reset: 0x0 Testable: writeAsRead
15:0	RW	0x0000	FORCE_DETECT_LANE Force Detect Lane. When the FORCE_DETECT_LANE_EN field is set, the controller ignores receiver detection from PHY during LTSSM Detect state and uses this value instead. Value represents lane number. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_SD_CONTROL2_REG

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	FRAMING_ERR_RECOVERY_DISABLE Framing Error Recovery Disable. This bit disables a transition to Recovery state when a Framing Error is occurred. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
15:11	RO	0x00	reserved
10	RW	0x0	DIRECT_LPBKSLV_TO_EXIT Direct Loopback Slave To Exit. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the LTSSM is in Loopback Slave Active State, the LTSSM transitions to Loopback Slave Exit state. Value After Reset: 0x0 Testable: writeAsRead
9	RW	0x0	DIRECT_POLCOMP_TO_DETECT Direct Polling.Compliance to Detect. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the LTSSM is in Polling Compliance State, the LTSSM transitions to Detect state. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
8	RW	0x0	DIRECT_RECIDLE_TO_CONFIG Direct Recovery.Idle to Configuration. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the LTSSM is in Recovery Idle State, the LTSSM transitions to Configuration state. Value After Reset: 0x0 Testable: writeAsRead
7:3	RO	0x00	reserved
2	RW	0x0	NOACK_FORCE_LINKDOWN Force LinkDown. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set and the controller detects REPLY_NUM rolling over 4 times, the LTSSM transitions to Detect State. Value After Reset: 0x0 Testable: writeAsRead
1	WO	0x0	RECOVERY_REQUEST Recovery Request. Values: 0x0 (CLEAR): Clear 0x1 (SET): When this bit is set to '1' in L0 or L0s, the LTSSM starts transitioning to Recovery State. This request does not cause a speed change or re-equalization. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	HOLD_LTSSM Hold and Release LTSSM. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): As long as this field is '1', the controller stays in the current LTSSM. Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_SD_STATUS_L1LANE_REG

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DESKEW_POINTER Deskew Pointer. Indicates Deskew pointer of internal Deskew buffer of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved
20	RO	0x1	PIPE_TXELECIDLE PIPE:TxElecIdle. Indicates PIPE TXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
19	RO	0x1	PIPE_RXELECIDLE PIPE:RxElecIdle. Indicates PIPE RXELECIDLE signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
18	RO	0x0	PIPE_RXVALID PIPE:RxValid. Indicates PIPE RXVALID signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17	RO	0x0	PIPE_DETECT_LANE PIPE:Detect Lane. Indicates whether PHY indicates receiver detection or not on selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
16	RO	0x0	PIPE_RXPOLARITY PIPE:RxPolarity. Indicates PIPE RXPOLARITY signal of selected lane number(LANE_SELECT). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:4	RO	0x000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	LANE_SELECT Lane Select. Lane Select register for Silicon Debug Status Register of Layer1-PerLane. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_SD_STATUS_L1LTSSM_REG

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LTSSM_VARIABLE LTSSM Variable. Indicates internal LTSSM variables defined in the PCI Express Base Specification. For other value idle_to_rlock_transitioned. Note: This register field is sticky. Values: 0x0 (DIR_SPEED_CHANGE): directed_speed_change 0x1 (CHANGED_SPEED_RCVRY): changed_speed_recovery 0x2 (SUCCESSFUL_SPEED_NEGO): successful_speed_negotiation 0x3 (UPCFG_CAPABLE): upconfigure_capable; Set to '1' if both ports advertised the UpConfigure capability in the last Config.Complete. 0x4 (SEL_DE_EMPHASIS): select_deemphasis 0x5 (START_EQ_W_PRESET): start_equalization_w_preset 0x6 (EQ_DONE_8GT): equalization_done_8GT_data_rate 0x7 (EQ_DONE_16GT): equalization_done_16GT_data_rate Value After Reset: 0x0 Testable: untestable Volatile: true

Bit	Attr	Reset Value	Description
15	RO	0x0	LANE_REVERSAL Lane Reversal Operation. Receiver detected lane reversal. This field is only valid in the L0 LTSSM state. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14:11	RO	0x0	reserved
10:8	RO	0x2	PIPE_POWER_DOWN PIPE:PowerDown. Indicates PIPE PowerDown signal. Note: This register field is sticky. Value After Reset: 0x2 Testable: writeAsRead Volatile: true
7	W1C	0x0	FRAMING_ERR Framing Error. Indicates Framing Error detection status. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

6:0	RO	0x00	FRAMING_ERR_PTR First Framing Error Pointer. Identifies the first Framing Error using the following encoding. The field contents are only valid value when FRAMING_ERR =1. Received Unexpected Framing Token (Values 01h to 06h) Received Unexpected STP Token (Values 11h to 13h) Received Unexpected Block (Values 21h to 2Eh) All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x1 (STP_OR_SDP_OR_IDL_RECEIVED_NO_TLP_OR_DLLP): When non- STP/SDP/IDL Token was received and it was not in TLP/DLLP reception 0x2 (CURRENT_NO_VALID_EDB_PREVIOUS_VALID_EDB): When current token was not a valid EDB token and previous token was an EDB. (128/256 bit controller only) 0x3 (SDP_RECEIVED_NOT_EXPECTED): When SDP token was received but not expected. (128 bit & (x8 | x16) controller only) 0x4 (STP_RECEIVED_NOT_EXPECTED): When STP token was received but not expected. (128 bit & (x8 | x16) controller only) 0x5 (EDS_RECEIVED_NOT_EXPECTED): When EDS token was expected but not received or whenever an EDS token was received but not expected. 0x6 (FRE_ERR_DESKEW_PKT_IN_PROGRESS): When a framing error was detected in the deskew block while a packet has been in progress in token_finder. 0x11 (CRC_STP_NOT_MATCH): When Framing CRC in STP token did not match 0x12 (PARITY_STP_NOT_MATCH): When Framing Parity in STP token did not match. 0x13 (TLP_LENGTH_SMALLER_THEN_5DW): When Framing TLP Length in STP token was smaller than 5 DWORDs. 0x21 (RECEVING_OS_AFTER_SDS_IN_DATA_STREAM): When Receiving an OS Block following SDS in Datastream state 0x22 (AFTER_DATA_BLK_OS_BLK_NOT_SKP_EI_EIE): When Data Block followed by OS Block different from SKP, EI, EIE in Datastream state 0x23 (UNDEFINE_BLK_TYPE): When Block with an undefined Block Type in Datastream state 0x24 (DATA_STREAM_WITHOUT_3_CYCLE_DATA_STREAM_S): When Data Stream without data over three cycles in Datastream state 0x25 (OS_BLK_DURING_DATA_STREAM): When OS Block during Data Stream in Datastream state 0x26 (RXSTATUS_ERR_DATA_STREAM_STATE): When RxStatus Error was detected in Datastream state 0x27 (NOT_ALL_LANE_START_RECEVING_SKP_OS_SAME_T): When Not all active lanes receiving SKP OS starting at same cycle time in SKPOS state 0x28 (_2_BLK_TIMEOUT_SKP_OS_SKPOS_STATE): When a 2-Block timeout occurs for SKP OS in SKPOS state

Bit	Attr	Reset Value	Description
			0x29 (CONSECUTIVE_OS_WITHIN_DATA_IN_SKPOS_STATE): When Receiving consecutive OS Blocks within a Data Stream in SKPOS state 0x2a (PHYSTATUS_ERR_IN_SKPOS_STATE): When Phy status error was detected in SKPOS state 0x2b (NOT_ALL_LANE_START_RECEVING_EIOS_SAME_T): When Not all active lanes receiving EIOS starting at same cycle time in EIOS state 0x2c (AT_LEAST_1_SYM_IS_NOT_EIOS_FROM_4_SYM): When At least one Symbol from the first 4 Symbols is not EIOS Symbol in EIOS state (CX_NB=2 only) 0x2d (NOT_ALL_LANE_START_RECEVING_EIEOS_SAME_T): When Not all active lanes receiving EIEOS starting at same cycle time in EIEOS state 0x2e (NOT_16_EIEOS_SYM_RECEIVED): When Not full 16 eieos symbols are received in EIEOS state Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_STATUS_PM_REG
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	LATCHED_NFTS Latched N_FTS. Indicates the value of N_FTS in the received TS Ordered Sets from the Link Partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:13	RO	0x0	L1SUB_STATE L1Sub State. Indicates internal state machine of L1Sub state. Note: This register field is sticky. Values: 0x0 (S_L1_U): S_L1_U : idle state 0x1 (S_L1_0): S_L1_0 : wait for aux_clk_active 0x2 (S_L1_0_WAIT4_ACK): S_L1_0_WAIT4_ACK : wait for pclkack 0x3 (S_L1_0_WAIT4_CLKREQ): S_L1_0_WAIT4_CLKREQ : wait for clkreq 0x4 (S_L1_N_ENTRY): S_L1_N_ENTRY : check clkreq_in_n is de-asserted for t_power_off time (only for L1.2, reduces to one cycle for L1.1) 0x5 (S_L1_N): S_L1_N : L1 substate, turn off txcommonmode circuits (L1.2 only) and rx electrical idle detection circuits 0x6 (S_L1_N_EXIT): S_L1_N_EXIT : locally/remotely initiated exit, assert pclkreq, wait for pclkack 0x7 (S_L1_N_ABORT): S_L1_N_ABORT : wait for pclkack when aborting an attempt to enter L1_N Value After Reset: 0x0 Testable: writeAsRead Volatile: true
12	RW	0x0	PME_RESEND_FLAG PME Re-send flag. When the DUT sends a PM_PME message TLP, the DUT sets PME_Status bit. If host software does not clear PME_Status bit for 100ms(+50%/-5%), the DUT resends the PM_PME Message. This bit indicates that a PM_PME was resent. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:8	RO	0x0	INTERNAL_PM_SSTATE Internal PM State(Slave). Indicates internal state machine of Power Management Slave controller. Note: This register field is sticky. Values: 0x0 (S_IDLE): S_IDLE 0x1 (S_RESPOND_NAK): S_RESPOND_NAK 0x2 (S_BLOCK_TLP): S_BLOCK_TLP 0x3 (S_WAIT_LAST_TLP_ACK): S_WAIT_LAST_TLP_ACK 0x4 (S_WAIT_EIDLE): S_WAIT_EIDLE 0x5 (S_LINK_ENTR_L1): S_LINK_ENTR_L1 0x6 (S_L1): S_L1 0x7 (S_L1_EXIT): S_L1_EXIT 0x8 (S_L23RDY): S_L23RDY 0x9 (S_LINK_ENTR_L23): S_LINK_ENTR_L23 0xa (S_L23RDY_WAIT4ALIVE): S_L23RDY_WAIT4ALIVE 0xb (S_ACK_WAIT4IDLE): S_ACK_WAIT4IDLE 0xc (S_WAIT_LAST_PMDLLP): S_WAIT_LAST_PMDLLP Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RO	0x00	INTERNAL_PM_MSTATE Internal PM State(Master). Indicates internal state machine of Power Management Master controller. Note: This register field is sticky. Values: 0x0 (IDLE): IDLE 0x1 (L0): L0 0x2 (L0S): L0S 0x3 (ENTER_L0S): ENTER_L0S 0x4 (EXIT_L0S): L0S_EXIT 0x5 (WAIT_PMCSR_CPL_SENT): WAIT_PMCSR_CPL_SENT 0x8 (L1): L1 0x9 (L1_BLOCK_TLP): L1_BLOCK_TLP 0xa (L1_WAIT_LAST_TLP_ACK): L1_WAIT_LAST_TLP_ACK 0xb (L1_WAIT_PMDLLP_ACK): L1_WAIT_PMDLLP_ACK 0xc (L1_LINK_ENTR_L1): L1_LINK_ENTR_L1 0xd (L1_EXIT): L1_EXIT 0xf (PREP_4L1): PREP_4L1 0x10 (L23_BLOCK_TLP): L23_BLOCK_TLP 0x11 (L23_WAIT_LAST_TLP_ACK): L23_WAIT_LAST_TLP_ACK 0x12 (L23_WAIT_PMDLLP_ACK): L23_WAIT_PMDLLP_ACK 0x13 (L23_ENTR_L23): L23_ENTR_L23 0x14 (L23RDY): L23RDY 0x15 (PREP_4L23): PREP_4L23 0x16 (L23RDY_WAIT4ALIVE): L23RDY_WAIT4ALIVE 0x17 (L0S_BLOCK_TLP): L0S_BLOCK_TLP 0x18 (WAIT_LAST_PMDLLP): WAIT_LAST_PMDLLP 0x19 (WAIT_DSTATE_UPDATE): WAIT_DSTATE_UPDATE Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_STATUS_L2_REG
Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	FC_INIT2 FC_INIT2. Indicates the controller is in FC_INIT2(VC0) state. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
26	RO	0x0	FC_INIT1 FC_INIT1. Indicates the controller is in FC_INIT1(VC0) state. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
25:24	RO	0x0	DLCMSM DLCMSM. Indicates the current DLCMSM. Note: This register field is sticky. Values: 0x0 (DL_INACTIVE): DL_INACTIVE 0x1 (DL_FC_INIT): DL_FC_INIT 0x3 (DL_ACTIVE): DL_ACTIVE Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:12	RO	0xfff	RX_ACK_SEQ_NO Tx Ack Sequence Number. Indicates ACKD_SEQ which is updated by receiving ACK/NAK DLLP. Note: This register field is sticky. Value After Reset: 0xfff Testable: writeAsRead Volatile: true
11:0	RO	0x000	TX_TLP_SEQ_NO Tx Tlp Sequence Number. Indicates next transmit sequence number for transmit TLP. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_STATUS_L3FC_REG
Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	CREDIT_DATA1 Credit Data1. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. Rx: Credit Allocated Value Tx: Credit Limit Value. This value is valid when DLCMSM=0x3(DL_ACTIVE). Note: This register field is sticky. Value After Reset: 0x0 Testable: untestable Volatile: true
19:8	RO	0x000	CREDIT_DATA0 Credit Data0. Current FC credit data selected by the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields. Rx: Credit Received Value Tx: Credit Consumed Value Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved
6	RW	0x0	CREDIT_SEL_HD Credit Select(HeaderData). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_TLP_TYPE viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (HEADER_CREDIT): Header Credit 0x1 (DATA_CREDIT): Data Credit Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
5:4	RW	0x0	CREDIT_SEL_TLP_TYPE Credit Select(TLP Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_CREDIT_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (POSTED): Posted 0x1 (NON_POSTED): Non-Posted 0x2 (COMPLETION): Completion Value After Reset: 0x0 Testable: writeAsRead
3	RW	0x0	CREDIT_SEL_CREDIT_TYPE Credit Select(Credit Type). This field in conjunction with the CREDIT_SEL_VC, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (RX): Rx 0x1 (TX): Tx Value After Reset: 0x0 Testable: writeAsRead
2:0	RW	0x0	CREDIT_SEL_VC Credit Select(VC). This field in conjunction with the CREDIT_SEL_CREDIT_TYPE, CREDIT_SEL_TLP_TYPE, and CREDIT_SEL_HD viewport-select fields determines that data that is returned by the CREDIT_DATA0 and CREDIT_DATA1 data fields. Note: This register field is sticky. Values: 0x0 (MIN_VAL): VC0 0x7 (MAX_VAL): VC7 Value After Reset: 0x0

USP_PCIE_RAS_DES_SD_STATUS_L3_REG

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	MFTLP_STATUS Malformed TLP Status. Indicates malformed TLP has occurred. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6:0	RO	0x00	MFTLP_POINTER First Malformed TLP Error Pointer. Indicates the element of the received first malformed TLP. This pointer is validated by MFTLP_STATUS. All encodings other than the defined encodings are reserved. Note: This register field is sticky. Values: 0x1 (ATMC_OP_ALIGN): AtomicOp address alignment 0x2 (ATMC_OP_OPERAND): AtomicOp operand 0x3 (ATMC_OP_BYTE_EN): AtomicOp byte enable 0x4 (TLP_LENGTH_MISMATCH): TLP length miss match 0x5 (MAX_PAYLOAD_SIZE): Max payload size 0x6 (TLP_WITHOUT_TC0): Message TLP without TC0 0x7 (INVALID_TC): Invalid TC 0x8 (UNXPCTD_ROUTE_BIT_MSG_TLP): Unexpected route bit in Message TLP 0x9 (UNXPCTD_CRS_STATUS_CMPL_TLP): Unexpected CRS status in Completion TLP 0xa (BYTE_ENABLE): Byte enable 0xb (MEM_ADDR_4KB_BOUNDARY): Memory Address 4KB boundary 0xc (TLP_PREFIX_RULES): TLP prefix rules 0xd (TRANSLATION_RULES): Translation request rules 0xe (INVALID_TLP_TYPE): Invalid TLP type 0xf (CMPL_RULES): Completion rules 0x7f (APPLICATION): Application Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_EQ_CONTROL1_REG
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	FOM_TARGET FOM Target. Indicates figure of merit target criteria value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2). This field is only valid when GEN3_EQ_FB_MODE is 0001b(Figure Of Merit). Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	FOM_TARGET_ENABLE FOM Target Enable. Enables the FOM_TARGET fields. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
22:18	RO	0x00	reserved
17:16	RW	0x0	EVAL_INTERVAL_TIME Eval Interval Time. Indicates interval time of RxEqEval assertion. This field is used for EQ Master(DSP in EQ Phase3/USP in EQ Phase2). Note: This register field is sticky. Values: 0x0 (_500NS): 500ns 0x1 (_1US): 1us 0x2 (_2US): 2us 0x3 (_4US): 4us Value After Reset: 0x0 Testable: writeAsRead
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	EXT_EQ_TIMEOUT Extends EQ Phase2/3 Timeout. This field is used when the LTSSM is in Recovery.EQ2/3. When this field is set, the value of EQ2/3 timeout is extended. Note: This register field is sticky. Values: 0x0 (_24MS_OR_32MS): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] 24ms (default) or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] 32ms (default) 0x1 (_48MS_OR_56MS): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] 48ms (x2) or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] 56ms (32ms+24ms) 0x2 (_240MS_OR_248MS): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] 240ms (x10) or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] 248ms (32ms +9*24ms) 0x3 (NO_TIMEOUT): [EQ Master(DSP in EQ Phase3/USP in EQ Phase2)] No timeout or [EQ Slave(DSP in EQ Phase2/USP in EQ Phase3)] No timeout Value After Reset: 0x0 Testable: writeAsRead
7:5	RO	0x0	reserved
4	RW	0x0	EQ_RATE_SEL EQ Status Rate Select. Setting this field in conjunction with the EQ_LANE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky. Values: 0x0 (_8GT): 8.0GT/s Speed (include ESM data rate) 0x1 (_16GT): 16.0GT/s Speed (include ESM data rate) 0x2 (_32GT): 32.0GT/s Speed Value After Reset: 0x0 Testable: writeAsRea

Bit	Attr	Reset Value	Description
3:0	RW	0x0	EQ_LANE_SEL EQ Status Lane Select. Setting this field in conjunction with the EQ_RATE_SEL field determines the per-lane Silicon Debug EQ Status data returned by the SD_EQ_CONTROL[2/3] and SD_EQ_STATUS[1/2/3] viewport registers. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Lane0 0xf (MAX_VAL): Lane15 Value After Reset: 0x0 Testable: writeAsRead

USP_PCIE_RAS_DES_SD_EQ_CONTROL2_REG
Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	FORCE_LOCAL_TX_PRESET_ENABLE Force Local Transmitter Preset Enable. Enables the FORCE_LOCAL_TX_PRESET field. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
29	RW	0x0	FORCE_LOCAL_RX_HINT_ENABLE Force Local Receiver Preset Hint Enable. Enables the FORCE_LOCAL_RX_HINT field. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
28	RW	0x0	FORCE_LOCAL_TX_COEF_ENABLE Force Local Transmitter Coefficient Enable. Enables the following fields: FORCE_LOCAL_TX_PRE_CURSOR FORCE_LOCAL_TX_CURSOR FORCE_LOCAL_TX_POST_CURSOR Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
27:24	RW	0x0	FORCE_LOCAL_TX_PRESET Force Local Transmitter Preset. Indicates initial preset value of USP in EQ Slave(EQ Phase2) instead of receiving EQ TS2. If select rate in the EQ_RATE_SEL field is 32.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved
20:18	RW	0x0	FORCE_LOCAL_RX_HINT Force Local Receiver Preset Hint. Indicates the RxPresetHint value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of received or set value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17:12	RW	0x00	FORCE_LOCAL_TX_POST_CURSOR Force Local Transmitter Post-Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:6	RW	0x00	FORCE_LOCAL_TX_CURSOR Force Local Transmitter Cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RW	0x00	FORCE_LOCAL_TX_PRE_CURSOR Force Local Transmitter Pre-cursor. Indicates the coefficient value of EQ Slave(DSP in EQ Phase2/USP in EQ Phase3), instead of the value instructed from link partner. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_EQ_CONTROL3_REG

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	FORCE_REMOTE_TX_COEF_ENABLE Force Remote Transmitter Coefficient Enable. Enables the following fields: FORCE_REMOTE_TX_PRE_CURSOR FORCE_REMOTE_TX_CURSOR FORCE_REMOTE_TX_POST_CURSOR This function can only be used when GEN3_EQ_FB_MODE = 0000b(Direction Change) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
27:18	RO	0x000	reserved

Bit	Attr	Reset Value	Description
17:12	RW	0x00	FORCE_REMOTE_TX_POST_CURSOR Force Remote Transmitter Post-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:6	RW	0x00	FORCE_REMOTE_TX_CURSOR Force Remote Transmitter Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RW	0x00	FORCE_REMOTE_TX_PRE_CURSOR Force Remote Transmitter Pre-Cursor. Indicates the coefficient value of EQ Master(DSP in EQ Phase3/USP in EQ Phase2), instead of the value instructed from local phy in dirchange mode. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_EQ_STATUS1_REG

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RO	0x0	EQ_REJECT_EVENT EQ Reject Event. Indicates that the controller receives two consecutive TS1 OS w/Reject=1b during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
6	RO	0x0	EQ_RULEC_VIOLATION EQ Rule C Violation. Indicates that coefficients rule C violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rule C correspond to the rules c) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5	RO	0x0	EQ_RULEB_VIOLATION EQ Rule B Violation. Indicates that coefficients rule B violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules B correspond to the rules b) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
4	RO	0x0	EQ_RULEA_VIOLATION EQ Rule A Violation. Indicates that coefficients rule A violation is detected in the values provided by PHY using direction change method during EQ Master phase(DSP in EQ Phase3/USP in EQ Phase2). The coefficients rules A correspond to the rules a) from section "Rules for Transmitter Coefficents" in the PCI Express Base Specification. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3	RO	0x0	reserved
2:1	RO	0x0	EQ_CONVERGENCE_INFO EQ Convergence Info. Indicates equalization convergence information. This bit is automatically cleared when the controller starts EQ Master phase again. Note: This register field is sticky. Values: 0x0 (EQ_NOT_ATTEMPTED): Equalization is not attempted 0x1 (EQ_SUCCESSFUL): Equalization finished successfully 0x2 (EQ_UNSUCCESSFUL): Equalization finished unsuccessfully 0x3 (RSVD): Reserved Value After Reset: 0x0 Testable: writeAsRead Volatile: true
0	RO	0x0	EQ_SEQUENCE EQ Sequence. Indicates that the controller is starting the equalization sequence. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_EQ_STATUS2_REG
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EQ_LOCAL_FOM_VALUE EQ Local Figure of Merit. Indicates Local maximum Figure of Merit value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved
20:18	RO	0x0	EQ_LOCAL_RX_HINT EQ Local Receiver Preset Hint. Indicates Local Receiver Preset Hint value. If select rate in the EQ_RATE_SEL field is other than 8.0GT/s Speed, this feature is not available. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17:12	RO	0x00	EQ_LOCAL_POST_CURSOR EQ Local Post-Cursor. Indicates Local post cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:6	RO	0x00	EQ_LOCAL_CURSOR EQ Local Cursor. Indicates Local cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
5:0	RO	0x00	EQ_LOCAL_PRE_CURSOR EQ Local Pre-Cursor. Indicates Local pre cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_RAS_DES_SD_EQ_STATUS3_REG

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	EQ_REMOTE_FS EQ Remote FS. Indicates Remote FS value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:18	RO	0x00	EQ_REMOTE_LF EQ Remote LF. Indicates Remote LF value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
17:12	RO	0x00	EQ_REMOTE_POST_CURSOR EQ Remote Post-Cursor. Indicates Remote post cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:6	RO	0x00	EQ_REMOTE_CURSOR EQ Remote Cursor. Indicates Remote cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RO	0x00	EQ_REMOTE_PRE_CURSOR EQ Remote Pre-Cursor. Indicates Remote pre cursor coefficient value. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

11.4.4.27 USP_PCIE_VSECDMA Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_VSECDMA_EXT_CAP_HDR_OFF	0x0000	W	0x0001000B	PCIe Extended Capability ID, Capability Version, and Next Capability Offset Register
USP_PCIE_VSECDMA_VENDOR_SPECIFIC_HDR_OFF	0x0004	W	0x01800006	Vendor Specific Header Register
USP_PCIE_VSECDMA_DEVICE_INFORMATION_OFF	0x0008	W	0x00A80401	DMA and related AXI Bridge Implementation Information
USP_PCIE_VSECDMA_NUM_CHAN_OFF	0x000C	W	0x00020002	Number of Implemented Channels Register
USP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_LOW_OFF	0x0010	W	0x00000000	DMA Register Map Start Address Offset Low Register
USP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_HIGH_OFF	0x0014	W	0x00000000	DMA Register Map Start Address Offset High Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.28 USP_PCIE_VSECDMA Detail Registers Description

USP_PCIE_VSECDMA_EXT_CAP_HDR_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead
19:16	RW	0x1	CAP Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. A version of the specification that changes the Extended Capability in a way that is not otherwise identifiable (that is, through a new Capability field) is permitted to increment this field. All such changes to the Capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as Functions reporting any such Capability Version numbers will contain a Capability structure that is compatible with that piece of software. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15:0	RW	0x000b	ID PCI Express Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Value After Reset: 0xb Testable: writeAsRead

USP_PCIE_VSECDMA_VENDOR_SPECIFIC_HDR_OFF
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:20	RO	0x018	VSEC_LENGTH VSEC Length. This field indicates the number of bytes in the entire VSEC structure, including the Vendor-Specific Extended Capability Header, the Vendor-Specific Header, and the vendor-specific registers. Value After Reset: 0x18
19:16	RO	0x0	VSEC_REV VSEC Rev. This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field. Value After Reset: 0x0
15:0	RO	0x0006	VSEC_ID VSEC ID. This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field. Value After Reset: 0x6

USP_PCIE_VSECDMA_DEVICE_INFORMATION_OFF
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	MASTER_PAGE_BOUNDARY_POINTER_WIDTH This field provides address page boundary information. It reports the value of CC_MSTR_PAGE_BOUNDARY_PW configuration parameter. Value After Reset: 0xd

Bit	Attr	Reset Value	Description
25:23	RO	0x1	MASTER_BURST_LENGTH Reports the CC_MSTR_BURST_LEN configuration parameter. Values: 0x0 (MSTR_BRSTLEN_8): 8 bits 0x1 (MSTR_BRSTLEN_16): 16 bits 0x2 (MSTR_BRSTLEN_32): 32 bits 0x3 (MSTR_BRSTLEN_64): 64 bits 0x4 (MSTR_BRSTLEN_128): 128 bits 0x5 (MSTR_BRSTLEN_256): 256 bits Value After Reset: 0x1
22:20	RO	0x2	MASTER_BUS_WIDTH This field provides information regarding the AXI master data bus width. It reports the value of MASTER_BUS_DATA_WIDTH configuration parameter. Values: 0x0 (MSTR_BUSWD_32): 32 bits 0x1 (MSTR_BUSWD_64): 64 bits 0x2 (MSTR_BUSWD_128): 128 bits 0x3 (MSTR_BUSWD_256): 256 bits 0x4 (MSTR_BUSWD_512): 512 bits Value After Reset: 0x2
19	RO	0x1	AXI This field provides information about AXI interface usage. It reports the value of AXI_POPULATED configuration parameter. Value After Reset: 0x1
18:16	RO	0x0	CHANNEL_SEPARATION If the MAP_FORMAT is set to HDMA_NATIVE, this field specifies the read write channel address separation. Other values are reserved. Values: 0x0 (CHSEP_256): 256 separated 0x1 (CHSEP_512): 512 separated 0x2 (CHSEP_1K): 1k separated 0x3 (CHSEP_2K): 2k separated 0x4 (CHSEP_4K): 4k separated 0x5 (CHSEP_8K): 8k separated 0x6 (CHSEP_16K): 16k separated 0x7 (CHSEP_32K): 32k separated Value After Reset: 0x0
15:11	RO	0x00	PFN Physical Function Number. This field provides information regarding the DMA register and physical function mapping. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
10:8	RO	0x4	BARN Bar Number. This field provides information regarding the DMA register and BAR number mapping. Value After Reset: 0x4
7:3	RO	0x00	reserved
2:0	RO	0x1	MAP_FORMAT Defines the register map format and features to be one of the following values: Other values are reserved. Values: 0x0 (EDMA_LEGACY_PL): Legacy DMA register map accessed by the port-logic registers 0x1 (EDMA_LEGACY_UNROLL): Legacy DMA register map, mapped to a PF/BAR 0x5 (HDMA_COMPATIBILITY_MODE): HDMA compatibility mode (CC_LEGACY_DMA_MAP =1) register map, mapped to a PF/BAR 0x7 (HDMA_NATIVE): HDMA native (CC_LEGACY_DMA_MAP =0) register map, mapped to a PF/BAR Value After Reset: 0x1

USP_PCIE_VSECDMA_NUM_CHAN_OFF
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x002	NUM_DMA_RD_CHAN This field provides information regarding the number of implemented read channels. It reports the value of CC_NUM_DMA_RD_CHAN parameter. Value After Reset: 0x2
15:10	RO	0x00	reserved
9:0	RO	0x002	NUM_DMA_WR_CHAN This field provides information regarding the number of implemented write channels. It reports the value of CC_NUM_DMA_WR_CHAN parameter. Value After Reset: 0x2

USP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_LOW_OFF
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	UNROLL_ADDR_OFFSET_LOW BAR address offset, 32-bit LSB. Value After Reset: 0x0

USP_PCIE_VSECDMA_UNROLL_ADDR_OFFSET_HIGH_OFF
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	UNROLL_ADDR_OFFSET_HIGH BAR address offset, 32-bit MSB. Value After Reset: 0x0

11.4.4.29 USP_PCIE_RESBAR Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_RESBAR_CAP_HDR_REG	0x0000	W	0x00010015	Resizable BAR Capability Header
USP_PCIE_RESBAR_CAP_REG_0_REG	0x0004	W	0x00007FF0	Resizable BAR0 Capability Register
USP_PCIE_RESBAR_CTRL_REG_0_REG	0x0008	W	0x00000AC0	Resizable BAR0 Control Register
USP_PCIE_RESBAR_CAP_REG_1_REG	0x000C	W	0x00007FF0	Resizable BAR1 Capability Register
USP_PCIE_RESBAR_CTRL_REG_1_REG	0x0010	W	0x00000A01	Resizable BAR1 Control Register
USP_PCIE_RESBAR_CAP_REG_2_REG	0x0014	W	0x00003FF0	Resizable BAR2 Capability Register
USP_PCIE_RESBAR_CTRL_REG_2_REG	0x0018	W	0x00000902	Resizable BAR2 Control Register
USP_PCIE_RESBAR_CAP_REG_3_REG	0x001C	W	0x00001FF0	Resizable BAR3 Capability Register
USP_PCIE_RESBAR_CTRL_REG_3_REG	0x0020	W	0x00000003	Resizable BAR3 Control Register
USP_PCIE_RESBAR_CAP_REG_4_REG	0x0024	W	0x00000010	Resizable BAR4 Capability Register
USP_PCIE_RESBAR_CTRL_REG_4_REG	0x0028	W	0x00000004	Resizable BAR4 Capability Register
USP_PCIE_RESBAR_CAP_REG_5_REG	0x002C	W	0x00000010	Resizable BAR5 Capability Register
USP_PCIE_RESBAR_CTRL_REG_5_REG	0x0030	W	0x00000005	Resizable BAR5 Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.30 USP_PCIE_RESBAR Detail Registers Description

USP_PCIE_RESBAR_CAP_HDR_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	RESBAR_CAP_NEXT_OFFSET Next Capability Offset. This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xfff (MAX_VAL): Max value Value After Reset: 0x0 Testable: unconstrained
19:16	RW	0x1	RESBAR_CAP_VERSION Capability Version. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This bit depends on the version of the specification. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x1 Testable: unconstrained

Bit	Attr	Reset Value	Description
15:0	RW	0x0015	RESBAR_EXT_CAP_ID Resizable BAR Extended Capability ID. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Resizable BAR Capability is 0015h. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xffff (MAX_VAL): Max value Value After Reset: 0x15 Testable: unconstrained

USP_PCIE_RESBAR_CAP_REG_0_REG
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CAP_REG_0_128TB Up to 128TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 128 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
30	RW	0x0	RESBAR_CAP_REG_0_64TB Up to 64TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 64 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 TB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CAP_REG_0_32TB Up to 32TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 32 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 TB. Value After Reset: 0x0 Testable: writeAsRead
28	RW	0x0	RESBAR_CAP_REG_0_16TB Up to 16TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 16 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
27	RW	0x0	RESBAR_CAP_REG_0_8TB Up to 8TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 8 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 TB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CAP_REG_0_4TB Up to 4TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 4 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 TB. Value After Reset: 0x0 Testable: writeAsRead
25	RW	0x0	RESBAR_CAP_REG_0_2TB Up to 2TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 2 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
24	RW	0x0	RESBAR_CAP_REG_0_1TB Up to 1TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 1 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1TB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CAP_REG_0_512GB Up to 512GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 512 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 GB. Value After Reset: 0x0 Testable: writeAsRead
22	RW	0x0	RESBAR_CAP_REG_0_256GB Up to 256GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 256 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21	RW	0x0	RESBAR_CAP_REG_0_128GB Up to 128GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 128 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 GB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CAP_REG_0_64GB Up to 64GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 64 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 GB. Value After Reset: 0x0 Testable: writeAsRead
19	RW	0x0	RESBAR_CAP_REG_0_32GB Up to 32GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 32 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
18	RW	0x0	RESBAR_CAP_REG_0_16GB Up to 16GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 16 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 GB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CAP_REG_0_8GB Up to 8GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 8 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 GB. Value After Reset: 0x0 Testable: writeAsRead
16	RW	0x0	RESBAR_CAP_REG_0_4GB Up to 4GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 4 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15	RW	0x0	RESBAR_CAP_REG_0_2GB Up to 2GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 2 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 GB. Value After Reset: 0x0 Testable: writeAsRead
14	RW	0x1	RESBAR_CAP_REG_0_1GB Up to 1GB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 1 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 GB. Value After Reset: 0x1 Testable: writeAsRead
13	RW	0x1	RESBAR_CAP_REG_0_512MB Up to 512MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 512 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
12	RW	0x1	RESBAR_CAP_REG_0_256MB Up to 256MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 256 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 MB. Value After Reset: 0x1 Testable: writeAsRead
11	RW	0x1	RESBAR_CAP_REG_0_128MB Up to 128MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 128 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 MB. Value After Reset: 0x1 Testable: writeAsRead
10	RW	0x1	RESBAR_CAP_REG_0_64MB Up to 64MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 64 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
9	RW	0x1	RESBAR_CAP_REG_0_32MB Up to 32MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 32 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 MB. Value After Reset: 0x1 Testable: writeAsRead
8	RW	0x1	RESBAR_CAP_REG_0_16MB Up to 16MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 16 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 MB. Value After Reset: 0x1 Testable: writeAsRead
7	RW	0x1	RESBAR_CAP_REG_0_8MB Up to 8MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 8 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
6	RW	0x1	RESBAR_CAP_REG_0_4MB Up to 4MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 4 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 MB. Value After Reset: 0x1 Testable: writeAsRead
5	RW	0x1	RESBAR_CAP_REG_0_2MB Up to 2MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 2 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 MB. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	RESBAR_CAP_REG_0_1MB Up to 1MB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 1 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 MB. Value After Reset: 0x1 Testable: writeAsRead
3:0	RO	0x0	reserved

USP_PCIE_RESBAR_CTRL_REG_0_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CTRL_REG_0_8EB Up to 8EB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 8 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 EB. Value After Reset: 0x0 Testable: writeAsRead
30	RW	0x0	RESBAR_CTRL_REG_0_4EB Up to 4EB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 4 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 EB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CTRL_REG_0_2EB Up to 2EB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 2 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 EB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
28	RW	0x0	RESBAR_CTRL_REG_0_1EB Up to 1EB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 1 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 EB. Value After Reset: 0x0 Testable: writeAsRead
27	RW	0x0	RESBAR_CTRL_REG_0_512PB Up to 512PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 512 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 PB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CTRL_REG_0_256PB Up to 256PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 256 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
25	RW	0x0	RESBAR_CTRL_REG_0_128PB Up to 128PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 128 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 PB. Value After Reset: 0x0 Testable: writeAsRead
24	RW	0x0	RESBAR_CTRL_REG_0_64PB Up to 64PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 64 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 PB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CTRL_REG_0_32PB Up to 32PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 32 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
22	RW	0x0	RESBAR_CTRL_REG_0_16PB Up to 16PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 16 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 PB. Value After Reset: 0x0 Testable: writeAsRead
21	RW	0x0	RESBAR_CTRL_REG_0_8PB Up to 8PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 8 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 PB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CTRL_REG_0_4PB Up to 4PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 4 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
19	RW	0x0	RESBAR_CTRL_REG_0_2PB Up to 2PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 2 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 PB. Value After Reset: 0x0 Testable: writeAsRead
18	RW	0x0	RESBAR_CTRL_REG_0_1PB Up to 1PB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 1 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 PB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CTRL_REG_0_512TB Up to 512TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 512 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
16	RW	0x0	RESBAR_CTRL_REG_0_256TB Up to 256TB BAR Supported. When Set, indicates that the Function supports operating with the BAR0 sized to 256 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 TB. Value After Reset: 0x0 Testable: writeAsRead
15:14	RO	0x0	reserved
13:8	RW	0x0a	RESBAR_CTRL_REG_BAR_SIZE BAR0 Size. The default value of this field is equal to the default size of the address space that the BAR0 resource is requesting via the BAR?s read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (MIN_VAL): 1MB(2^20 bytes) 0x2b (MAX_VAL): 8EB(2^63 bytes) Value After Reset: 0xa Testable: writeAsRead
7:5	RO	0x6	RESBAR_CTRL_REG_NUM_BARS Number of Resizeable BARs. This field indicates the total number of resizable BARs in the capability structure for the Function. The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR0 Control register (0) (at offset 008h), and is RsvdP for all others. Note: This register field is sticky. Values: 0x1 (BAR1): one resizable BAR for the function 0x2 (BAR2): two resizable BARs for the function. 0x3 (BAR3): three resizable BARs for the function. 0x4 (BAR4): four resizable BARs for the function. 0x5 (BAR5): five resizable BARs for the function. 0x6 (BAR6): six resizable BARs for the function. Value After Reset: 0x6
4:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x0	RESBAR_CTRL_REG_IDX_0 BAR Index. This encoded value points to the beginning of the BAR0. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size. Note: This register field is sticky. Values: 0x0 (BAR_10h): BAR located at offset 10h. 0x1 (BAR_14h): BAR located at offset 14h. 0x2 (BAR_18h): BAR located at offset 18h. 0x3 (BAR_1Ch): BAR located at offset 1Ch. 0x4 (BAR_20h): BAR located at offset 20h. 0x5 (BAR_24h): BAR located at offset 24h. Value After Reset: 0x0

USP_PCIE_RESBAR_CAP_REG_1_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CAP_REG_1_128TB Up to 128TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 128 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
30	RW	0x0	RESBAR_CAP_REG_1_64TB Up to 64TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 64 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 TB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CAP_REG_1_32TB Up to 32TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 32 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 TB. Value After Reset: 0x0 Testable: writeAsRead
28	RW	0x0	RESBAR_CAP_REG_1_16TB Up to 16TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 16 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
27	RW	0x0	RESBAR_CAP_REG_1_8TB Up to 8TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 8 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 TB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CAP_REG_1_4TB Up to 4TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 4 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 TB. Value After Reset: 0x0 Testable: writeAsRead
25	RW	0x0	RESBAR_CAP_REG_1_2TB Up to 2TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 2 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
24	RW	0x0	RESBAR_CAP_REG_1_1TB Up to 1TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 1 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1TB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CAP_REG_1_512GB Up to 512GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 512 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 GB. Value After Reset: 0x0 Testable: writeAsRead
22	RW	0x0	RESBAR_CAP_REG_1_256GB Up to 256GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 256 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21	RW	0x0	RESBAR_CAP_REG_1_128GB Up to 128GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1sized to 128 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 GB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CAP_REG_1_64GB Up to 64GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 64 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 GB. Value After Reset: 0x0 Testable: writeAsRead
19	RW	0x0	RESBAR_CAP_REG_1_32GB Up to 32GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 32 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
18	RW	0x0	RESBAR_CAP_REG_1_16GB Up to 16GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 16 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 GB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CAP_REG_1_8GB Up to 8GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 8 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 GB. Value After Reset: 0x0 Testable: writeAsRead
16	RW	0x0	RESBAR_CAP_REG_1_4GB Up to 4GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 4 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15	RW	0x0	RESBAR_CAP_REG_1_2GB Up to 2GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 2 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 GB. Value After Reset: 0x0 Testable: writeAsRead
14	RW	0x1	RESBAR_CAP_REG_1_1GB Up to 1GB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 1 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 GB. Value After Reset: 0x1 Testable: writeAsRead
13	RW	0x1	RESBAR_CAP_REG_1_512MB Up to 512MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 512 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
12	RW	0x1	RESBAR_CAP_REG_1_256MB Up to 256MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 256 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 MB. Value After Reset: 0x1 Testable: writeAsRead
11	RW	0x1	RESBAR_CAP_REG_1_128MB Up to 128MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 128 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 MB. Value After Reset: 0x1 Testable: writeAsRead
10	RW	0x1	RESBAR_CAP_REG_1_64MB Up to 64MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 64 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
9	RW	0x1	RESBAR_CAP_REG_1_32MB Up to 32MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 32 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 MB. Value After Reset: 0x1 Testable: writeAsRead
8	RW	0x1	RESBAR_CAP_REG_1_16MB Up to 16MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 16 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 MB. Value After Reset: 0x1 Testable: writeAsRead
7	RW	0x1	RESBAR_CAP_REG_1_8MB Up to 8MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 8 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
6	RW	0x1	RESBAR_CAP_REG_1_4MB Up to 4MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 4 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 MB. Value After Reset: 0x1 Testable: writeAsRead
5	RW	0x1	RESBAR_CAP_REG_1_2MB Up to 2MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 2 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 MB. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	RESBAR_CAP_REG_1_1MB Up to 1MB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 1 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 MB. Value After Reset: 0x1 Testable: writeAsRead
3:0	RO	0x0	reserved

USP_PCIE_RESBAR_CTRL_REG_1_REG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CTRL_REG_1_8EB Up to 8EB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 8 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 EB. Value After Reset: 0x0 Testable: writeAsRead
30	RW	0x0	RESBAR_CTRL_REG_1_4EB Up to 4EB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 4 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 EB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CTRL_REG_1_2EB Up to 2EB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 2 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 EB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
28	RW	0x0	RESBAR_CTRL_REG_1_1EB Up to 1EB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 1 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 EB. Value After Reset: 0x0 Testable: writeAsRead
27	RW	0x0	RESBAR_CTRL_REG_1_512PB Up to 512PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 512 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 PB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CTRL_REG_1_256PB Up to 256PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 256 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
25	RW	0x0	RESBAR_CTRL_REG_1_128PB Up to 128PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 128 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 PB. Value After Reset: 0x0 Testable: writeAsRead
24	RW	0x0	RESBAR_CTRL_REG_1_64PB Up to 64PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 64 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 PB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CTRL_REG_1_32PB Up to 32PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 32 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
22	RW	0x0	RESBAR_CTRL_REG_1_16PB Up to 16PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 16 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 PB. Value After Reset: 0x0 Testable: writeAsRead
21	RW	0x0	RESBAR_CTRL_REG_1_8PB Up to 8PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 8 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 PB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CTRL_REG_1_4PB Up to 4PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 4 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
19	RW	0x0	RESBAR_CTRL_REG_1_2PB Up to 2PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 2 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 PB. Value After Reset: 0x0 Testable: writeAsRead
18	RW	0x0	RESBAR_CTRL_REG_1_1PB Up to 1PB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 1 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 PB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CTRL_REG_1_512TB Up to 512TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 512 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
16	RW	0x0	RESBAR_CTRL_REG_1_256TB Up to 256TB BAR Supported. When Set, indicates that the Function supports operating with the BAR1 sized to 256 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 TB. Value After Reset: 0x0 Testable: writeAsRead
15:14	RO	0x0	reserved
13:8	RW	0x0a	RESBAR_CTRL_REG_BAR_SIZE BAR1 Size. The default value of this field is equal to the default size of the address space that the BAR1 resource is requesting via the BAR?s read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (MIN_VAL): 1MB(2^20 bytes) 0x2b (MAX_VAL): 8EB(2^63 bytes) Value After Reset: 0xa Testable: writeAsRead
7:5	RO	0x0	RESBAR_CTRL_REG_NUM_BARS Number of Resizeable BARs. This field indicates the total number of resizable BARs in the capability structure for the Function. The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR1 Control register (0) (at offset 008h), and is RsvdP for all others. Note: This register field is sticky. Values: 0x1 (BAR1): one resizable BAR for the function 0x2 (BAR2): two resizable BARs for the function. 0x3 (BAR3): three resizable BARs for the function. 0x4 (BAR4): four resizable BARs for the function. 0x5 (BAR5): five resizable BARs for the function. 0x6 (BAR6): six resizable BARs for the function. Value After Reset: 0x0
4:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x1	RESBAR_CTRL_REG_IDX_1 BAR Index. This encoded value points to the beginning of the BAR1. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size. Note: This register field is sticky. Values: 0x0 (BAR_10h): BAR located at offset 10h. 0x1 (BAR_14h): BAR located at offset 14h. 0x2 (BAR_18h): BAR located at offset 18h. 0x3 (BAR_1Ch): BAR located at offset 1Ch. 0x4 (BAR_20h): BAR located at offset 20h. 0x5 (BAR_24h): BAR located at offset 24h. Value After Reset: 0x1

USP_PCIE_RESBAR_CAP_REG_2_REG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CAP_REG_2_128TB Up to 128TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 128 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
30	RW	0x0	RESBAR_CAP_REG_2_64TB Up to 64TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 64 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 TB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CAP_REG_2_32TB Up to 32TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 32 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 TB. Value After Reset: 0x0 Testable: writeAsRead
28	RW	0x0	RESBAR_CAP_REG_2_16TB Up to 16TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 16 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
27	RW	0x0	RESBAR_CAP_REG_2_8TB Up to 8TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 8 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 TB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CAP_REG_2_4TB Up to 4TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 4 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 TB. Value After Reset: 0x0 Testable: writeAsRead
25	RW	0x0	RESBAR_CAP_REG_2_2TB Up to 2TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 2 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
24	RW	0x0	RESBAR_CAP_REG_2_1TB Up to 1TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 1 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1TB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CAP_REG_2_512GB Up to 512GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 512 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 GB. Value After Reset: 0x0 Testable: writeAsRead
22	RW	0x0	RESBAR_CAP_REG_2_256GB Up to 256GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 256 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21	RW	0x0	RESBAR_CAP_REG_2_128GB Up to 128GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 128 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 GB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CAP_REG_2_64GB Up to 64GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 64 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 GB. Value After Reset: 0x0 Testable: writeAsRead
19	RW	0x0	RESBAR_CAP_REG_2_32GB Up to 32GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 32 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
18	RW	0x0	RESBAR_CAP_REG_2_16GB Up to 16GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 16 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 GB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CAP_REG_2_8GB Up to 8GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 8 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 GB. Value After Reset: 0x0 Testable: writeAsRead
16	RW	0x0	RESBAR_CAP_REG_2_4GB Up to 4GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 4 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15	RW	0x0	RESBAR_CAP_REG_2_2GB Up to 2GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 2 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 GB. Value After Reset: 0x0 Testable: writeAsRead
14	RW	0x0	RESBAR_CAP_REG_2_1GB Up to 1GB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 1 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 GB. Value After Reset: 0x0 Testable: writeAsRead
13	RW	0x1	RESBAR_CAP_REG_2_512MB Up to 512MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 512 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
12	RW	0x1	RESBAR_CAP_REG_2_256MB Up to 256MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 256 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 MB. Value After Reset: 0x1 Testable: writeAsRead
11	RW	0x1	RESBAR_CAP_REG_2_128MB Up to 128MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 128 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 MB. Value After Reset: 0x1 Testable: writeAsRead
10	RW	0x1	RESBAR_CAP_REG_2_64MB Up to 64MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 64 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
9	RW	0x1	RESBAR_CAP_REG_2_32MB Up to 32MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 32 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 MB. Value After Reset: 0x1 Testable: writeAsRead
8	RW	0x1	RESBAR_CAP_REG_2_16MB Up to 16MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 16 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 MB. Value After Reset: 0x1 Testable: writeAsRead
7	RW	0x1	RESBAR_CAP_REG_2_8MB Up to 8MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 8 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
6	RW	0x1	RESBAR_CAP_REG_2_4MB Up to 4MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 4 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 MB. Value After Reset: 0x1 Testable: writeAsRead
5	RW	0x1	RESBAR_CAP_REG_2_2MB Up to 2MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 2 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 MB. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	RESBAR_CAP_REG_2_1MB Up to 1MB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 1 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 MB. Value After Reset: 0x1 Testable: writeAsRead
3:0	RO	0x0	reserved

USP_PCIE_RESBAR_CTRL_REG_2_REG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CTRL_REG_2_8EB Up to 8EB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 8 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 EB. Value After Reset: 0x0 Testable: writeAsRead
30	RW	0x0	RESBAR_CTRL_REG_2_4EB Up to 4EB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 4 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 EB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CTRL_REG_2_2EB Up to 2EB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 2 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 EB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
28	RW	0x0	RESBAR_CTRL_REG_2_1EB Up to 1EB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 1 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 EB. Value After Reset: 0x0 Testable: writeAsRead
27	RW	0x0	RESBAR_CTRL_REG_2_512PB Up to 512PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 512 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 PB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CTRL_REG_2_256PB Up to 256PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 256 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
25	RW	0x0	RESBAR_CTRL_REG_2_128PB Up to 128PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 128 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 PB. Value After Reset: 0x0 Testable: writeAsRead
24	RW	0x0	RESBAR_CTRL_REG_2_64PB Up to 64PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 64 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 PB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CTRL_REG_2_32PB Up to 32PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 32 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
22	RW	0x0	RESBAR_CTRL_REG_2_16PB Up to 16PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 16 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 PB. Value After Reset: 0x0 Testable: writeAsRead
21	RW	0x0	RESBAR_CTRL_REG_2_8PB Up to 8PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 8 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 PB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CTRL_REG_2_4PB Up to 4PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 4 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
19	RW	0x0	RESBAR_CTRL_REG_2_2PB Up to 2PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 2 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 PB. Value After Reset: 0x0 Testable: writeAsRead
18	RW	0x0	RESBAR_CTRL_REG_2_1PB Up to 1PB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 1 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 PB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CTRL_REG_2_512TB Up to 512TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 512 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
16	RW	0x0	RESBAR_CTRL_REG_2_256TB Up to 256TB BAR Supported. When Set, indicates that the Function supports operating with the BAR2 sized to 256 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 TB. Value After Reset: 0x0 Testable: writeAsRead
15:14	RO	0x0	reserved
13:8	RW	0x09	RESBAR_CTRL_REG_BAR_SIZE BAR2 Size. The default value of this field is equal to the default size of the address space that the BAR2 resource is requesting via the BAR?s read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (MIN_VAL): 1MB(2^20 bytes) 0x2b (MAX_VAL): 8EB(2^63 bytes) Value After Reset: 0x9 Testable: writeAsRead
7:5	RO	0x0	RESBAR_CTRL_REG_NUM_BARS Number of Resizeable BARs. This field indicates the total number of resizable BARs in the capability structure for the Function. The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR2 Control register (0) (at offset 008h), and is RsvdP for all others. Note: This register field is sticky. Values: 0x1 (BAR1): one resizable BAR for the function 0x2 (BAR2): two resizable BARs for the function. 0x3 (BAR3): three resizable BARs for the function. 0x4 (BAR4): four resizable BARs for the function. 0x5 (BAR5): five resizable BARs for the function. 0x6 (BAR6): six resizable BARs for the function. Value After Reset: 0x0
4:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x2	RESBAR_CTRL_REG_IDX_2 BAR Index. This encoded value points to the beginning of the BAR2. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size. Note: This register field is sticky. Values: 0x0 (BAR_10h): BAR located at offset 10h. 0x1 (BAR_14h): BAR located at offset 14h. 0x2 (BAR_18h): BAR located at offset 18h. 0x3 (BAR_1Ch): BAR located at offset 1Ch. 0x4 (BAR_20h): BAR located at offset 20h. 0x5 (BAR_24h): BAR located at offset 24h. Value After Reset: 0x2

USP_PCIE_RESBAR_CAP_REG_3_REG

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CAP_REG_3_128TB Up to 128TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 128 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
30	RW	0x0	RESBAR_CAP_REG_3_64TB Up to 64TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 64 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 TB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CAP_REG_3_32TB Up to 32TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 32 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 TB. Value After Reset: 0x0 Testable: writeAsRead
28	RW	0x0	RESBAR_CAP_REG_3_16TB Up to 16TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 16 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
27	RW	0x0	RESBAR_CAP_REG_3_8TB Up to 8TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 8 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 TB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CAP_REG_3_4TB Up to 4TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 4 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 TB. Value After Reset: 0x0 Testable: writeAsRead
25	RW	0x0	RESBAR_CAP_REG_3_2TB Up to 2TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 2 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
24	RW	0x0	RESBAR_CAP_REG_3_1TB Up to 1TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 1 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1TB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CAP_REG_3_512GB Up to 512GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 512 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 GB. Value After Reset: 0x0 Testable: writeAsRead
22	RW	0x0	RESBAR_CAP_REG_3_256GB Up to 256GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 256 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21	RW	0x0	RESBAR_CAP_REG_3_128GB Up to 128GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 128 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 GB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CAP_REG_3_64GB Up to 64GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 64 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 GB. Value After Reset: 0x0 Testable: writeAsRead
19	RW	0x0	RESBAR_CAP_REG_3_32GB Up to 32GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 32 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
18	RW	0x0	RESBAR_CAP_REG_3_16GB Up to 16GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 16 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 GB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CAP_REG_3_8GB Up to 8GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 8 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 GB. Value After Reset: 0x0 Testable: writeAsRead
16	RW	0x0	RESBAR_CAP_REG_3_4GB Up to 4GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 4 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15	RW	0x0	RESBAR_CAP_REG_3_2GB Up to 2GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 2 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 GB. Value After Reset: 0x0 Testable: writeAsRead
14	RW	0x0	RESBAR_CAP_REG_3_1GB Up to 1GB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 1 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 GB. Value After Reset: 0x0 Testable: writeAsRead
13	RW	0x0	RESBAR_CAP_REG_3_512MB Up to 512MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 512 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
12	RW	0x1	RESBAR_CAP_REG_3_256MB Up to 256MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 256 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 MB. Value After Reset: 0x1 Testable: writeAsRead
11	RW	0x1	RESBAR_CAP_REG_3_128MB Up to 128MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 128 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 MB. Value After Reset: 0x1 Testable: writeAsRead
10	RW	0x1	RESBAR_CAP_REG_3_64MB Up to 64MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 64 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
9	RW	0x1	RESBAR_CAP_REG_3_32MB Up to 32MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 32 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 MB. Value After Reset: 0x1 Testable: writeAsRead
8	RW	0x1	RESBAR_CAP_REG_3_16MB Up to 16MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 16 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 MB. Value After Reset: 0x1 Testable: writeAsRead
7	RW	0x1	RESBAR_CAP_REG_3_8MB Up to 8MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 8 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
6	RW	0x1	RESBAR_CAP_REG_3_4MB Up to 4MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 4 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 MB. Value After Reset: 0x1 Testable: writeAsRead
5	RW	0x1	RESBAR_CAP_REG_3_2MB Up to 2MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 2 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 MB. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	RESBAR_CAP_REG_3_1MB Up to 1MB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 1 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 MB. Value After Reset: 0x1 Testable: writeAsRead
3:0	RO	0x0	reserved

USP_PCIE_RESBAR_CTRL_REG_3_REG

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CTRL_REG_3_8EB Up to 8EB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 8 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 EB. Value After Reset: 0x0 Testable: writeAsRead
30	RW	0x0	RESBAR_CTRL_REG_3_4EB Up to 4EB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 4 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 EB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CTRL_REG_3_2EB Up to 2EB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 2 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 EB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
28	RW	0x0	RESBAR_CTRL_REG_3_1EB Up to 1EB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 1 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 EB. Value After Reset: 0x0 Testable: writeAsRead
27	RW	0x0	RESBAR_CTRL_REG_3_512PB Up to 512PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 512 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 PB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CTRL_REG_3_256PB Up to 256PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 256 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
25	RW	0x0	RESBAR_CTRL_REG_3_128PB Up to 128PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 128 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 PB. Value After Reset: 0x0 Testable: writeAsRead
24	RW	0x0	RESBAR_CTRL_REG_3_64PB Up to 64PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 64 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 PB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CTRL_REG_3_32PB Up to 32PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 32 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
22	RW	0x0	RESBAR_CTRL_REG_3_16PB Up to 16PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 16 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 PB. Value After Reset: 0x0 Testable: writeAsRead
21	RW	0x0	RESBAR_CTRL_REG_3_8PB Up to 8PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 8 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 PB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CTRL_REG_3_4PB Up to 4PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 4 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
19	RW	0x0	RESBAR_CTRL_REG_3_2PB Up to 2PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 2 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 PB. Value After Reset: 0x0 Testable: writeAsRead
18	RW	0x0	RESBAR_CTRL_REG_3_1PB Up to 1PB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 1 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 PB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CTRL_REG_3_512TB Up to 512TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 512 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
16	RW	0x0	RESBAR_CTRL_REG_3_256TB Up to 256TB BAR Supported. When Set, indicates that the Function supports operating with the BAR3 sized to 256 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 TB. Value After Reset: 0x0 Testable: writeAsRead
15:14	RO	0x0	reserved
13:8	RW	0x00	RESBAR_CTRL_REG_BAR_SIZE BAR3 Size. The default value of this field is equal to the default size of the address space that the BAR3 resource is requesting via the BAR?s read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (MIN_VAL): 1MB(2^20 bytes) 0x2b (MAX_VAL): 8EB(2^63 bytes) Value After Reset: 0x9 Testable: writeAsRead
7:5	RO	0x0	RESBAR_CTRL_REG_NUM_BARS Number of Resizeable BARs. This field indicates the total number of resizable BARs in the capability structure for the Function. The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR3 Control register (0) (at offset 008h), and is RsvdP for all others. Note: This register field is sticky. Values: 0x1 (BAR1): one resizable BAR for the function 0x2 (BAR2): two resizable BARs for the function. 0x3 (BAR3): three resizable BARs for the function. 0x4 (BAR4): four resizable BARs for the function. 0x5 (BAR5): five resizable BARs for the function. 0x6 (BAR6): six resizable BARs for the function. Value After Reset: 0x0
4:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x3	RESBAR_CTRL_REG_IDX_3 BAR Index. This encoded value points to the beginning of the BAR3. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size. Note: This register field is sticky. Values: 0x0 (BAR_10h): BAR located at offset 10h. 0x1 (BAR_14h): BAR located at offset 14h. 0x2 (BAR_18h): BAR located at offset 18h. 0x3 (BAR_1Ch): BAR located at offset 1Ch. 0x4 (BAR_20h): BAR located at offset 20h. 0x5 (BAR_24h): BAR located at offset 24h. Value After Reset: 0x3

USP_PCIE_RESBAR_CAP_REG_4_REG

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CAP_REG_4_128TB Up to 128TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 128 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
30	RW	0x0	RESBAR_CAP_REG_4_64TB Up to 64TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 64 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 TB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CAP_REG_4_32TB Up to 32TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 32 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 TB. Value After Reset: 0x0 Testable: writeAsRead
28	RW	0x0	RESBAR_CAP_REG_4_16TB Up to 16TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 16 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
27	RW	0x0	RESBAR_CAP_REG_4_8TB Up to 8TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 8 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 TB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CAP_REG_4_4TB Up to 4TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 4 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 TB. Value After Reset: 0x0 Testable: writeAsRead
25	RW	0x0	RESBAR_CAP_REG_4_2TB Up to 2TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 2 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
24	RW	0x0	RESBAR_CAP_REG_4_1TB Up to 1TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 1 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1TB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CAP_REG_4_512GB Up to 512GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 512 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 GB. Value After Reset: 0x0 Testable: writeAsRead
22	RW	0x0	RESBAR_CAP_REG_4_256GB Up to 256GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 256 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21	RW	0x0	RESBAR_CAP_REG_4_128GB Up to 128GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 128 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 GB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CAP_REG_4_64GB Up to 64GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 64 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 GB. Value After Reset: 0x0 Testable: writeAsRead
19	RW	0x0	RESBAR_CAP_REG_4_32GB Up to 32GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 32 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
18	RW	0x0	RESBAR_CAP_REG_4_16GB Up to 16GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 16 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 GB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CAP_REG_4_8GB Up to 8GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 8 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 GB. Value After Reset: 0x0 Testable: writeAsRead
16	RW	0x0	RESBAR_CAP_REG_4_4GB Up to 4GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 4 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15	RW	0x0	RESBAR_CAP_REG_4_2GB Up to 2GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 2 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 GB. Value After Reset: 0x0 Testable: writeAsRead
14	RW	0x0	RESBAR_CAP_REG_4_1GB Up to 1GB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 1 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 GB. Value After Reset: 0x0 Testable: writeAsRead
13	RW	0x0	RESBAR_CAP_REG_4_512MB Up to 512MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 512 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 MB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
12	RW	0x0	RESBAR_CAP_REG_4_256MB Up to 256MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 256 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 MB. Value After Reset: 0x0 Testable: writeAsRead
11	RW	0x0	RESBAR_CAP_REG_4_128MB Up to 128MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 128 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 MB. Value After Reset: 0x1 Testable: writeAsRead
10	RW	0x0	RESBAR_CAP_REG_4_64MB Up to 64MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 64 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
9	RW	0x0	RESBAR_CAP_REG_4_32MB Up to 32MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 32 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 MB. Value After Reset: 0x1 Testable: writeAsRead
8	RW	0x0	RESBAR_CAP_REG_4_16MB Up to 16MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 16 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 MB. Value After Reset: 0x1 Testable: writeAsRead
7	RW	0x0	RESBAR_CAP_REG_4_8MB Up to 8MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 8 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
6	RW	0x0	RESBAR_CAP_REG_4_4MB Up to 4MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 4 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 MB. Value After Reset: 0x1 Testable: writeAsRead
5	RW	0x0	RESBAR_CAP_REG_4_2MB Up to 2MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 2 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 MB. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	RESBAR_CAP_REG_4_1MB Up to 1MB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 1 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 MB. Value After Reset: 0x1 Testable: writeAsRead
3:0	RO	0x0	reserved

USP_PCIE_RESBAR_CTRL_REG_4_REG

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CTRL_REG_4_8EB Up to 8EB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 8 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 EB. Value After Reset: 0x0 Testable: writeAsRead
30	RW	0x0	RESBAR_CTRL_REG_4_4EB Up to 4EB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 4 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 EB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CTRL_REG_4_2EB Up to 2EB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 2 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 EB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
28	RW	0x0	RESBAR_CTRL_REG_4_1EB Up to 1EB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 1 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 EB. Value After Reset: 0x0 Testable: writeAsRead
27	RW	0x0	RESBAR_CTRL_REG_4_512PB Up to 512PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 512 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 PB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CTRL_REG_4_256PB Up to 256PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 256 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
25	RW	0x0	RESBAR_CTRL_REG_4_128PB Up to 128PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 128 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 PB. Value After Reset: 0x0 Testable: writeAsRead
24	RW	0x0	RESBAR_CTRL_REG_4_64PB Up to 64PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 64 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 PB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CTRL_REG_4_32PB Up to 32PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 32 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
22	RW	0x0	RESBAR_CTRL_REG_4_16PB Up to 16PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 16 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 PB. Value After Reset: 0x0 Testable: writeAsRead
21	RW	0x0	RESBAR_CTRL_REG_4_8PB Up to 8PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 8 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 PB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CTRL_REG_4_4PB Up to 4PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 4 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
19	RW	0x0	RESBAR_CTRL_REG_4_2PB Up to 2PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 2 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 PB. Value After Reset: 0x0 Testable: writeAsRead
18	RW	0x0	RESBAR_CTRL_REG_4_1PB Up to 1PB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 1 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 PB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CTRL_REG_4_512TB Up to 512TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 512 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
16	RW	0x0	RESBAR_CTRL_REG_4_256TB Up to 256TB BAR Supported. When Set, indicates that the Function supports operating with the BAR4 sized to 256 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 TB. Value After Reset: 0x0 Testable: writeAsRead
15:14	RO	0x0	reserved
13:8	RW	0x00	RESBAR_CTRL_REG_BAR_SIZE BAR4 Size. The default value of this field is equal to the default size of the address space that the BAR4 resource is requesting via the BAR?s read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (MIN_VAL): 1MB(2^20 bytes) 0x2b (MAX_VAL): 8EB(2^63 bytes) Value After Reset: 0x7 Testable: writeAsRead
7:5	RO	0x0	RESBAR_CTRL_REG_NUM_BARS Number of Resizeable BARs. This field indicates the total number of resizable BARs in the capability structure for the Function. The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR4 Control register (0) (at offset 008h), and is RsvdP for all others. Note: This register field is sticky. Values: 0x1 (BAR1): one resizable BAR for the function 0x2 (BAR2): two resizable BARs for the function. 0x3 (BAR3): three resizable BARs for the function. 0x4 (BAR4): four resizable BARs for the function. 0x5 (BAR5): five resizable BARs for the function. 0x6 (BAR6): six resizable BARs for the function. Value After Reset: 0x0
4:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x4	RESBAR_CTRL_REG_IDX_4 BAR Index. This encoded value points to the beginning of the BAR4. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size. Note: This register field is sticky. Values: 0x0 (BAR_10h): BAR located at offset 10h. 0x1 (BAR_14h): BAR located at offset 14h. 0x2 (BAR_18h): BAR located at offset 18h. 0x3 (BAR_1Ch): BAR located at offset 1Ch. 0x4 (BAR_20h): BAR located at offset 20h. 0x5 (BAR_24h): BAR located at offset 24h. Value After Reset: 0x4

USP_PCIE_RESBAR_CAP_REG_5_REG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CAP_REG_5_128TB Up to 128TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 128 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
30	RW	0x0	RESBAR_CAP_REG_5_64TB Up to 64TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 64 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 TB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CAP_REG_5_32TB Up to 32TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 32 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 TB. Value After Reset: 0x0 Testable: writeAsRead
28	RW	0x0	RESBAR_CAP_REG_5_16TB Up to 16TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 16 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
27	RW	0x0	RESBAR_CAP_REG_5_8TB Up to 8TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 8 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 TB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CAP_REG_5_4TB Up to 4TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 4 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 TB. Value After Reset: 0x0 Testable: writeAsRead
25	RW	0x0	RESBAR_CAP_REG_5_2TB Up to 2TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 2 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
24	RW	0x0	RESBAR_CAP_REG_5_1TB Up to 1TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 1 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1TB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CAP_REG_5_512GB Up to 512GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 512 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 GB. Value After Reset: 0x0 Testable: writeAsRead
22	RW	0x0	RESBAR_CAP_REG_5_256GB Up to 256GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 256 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
21	RW	0x0	RESBAR_CAP_REG_5_128GB Up to 128GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 128 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 GB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CAP_REG_5_64GB Up to 64GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 64 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 GB. Value After Reset: 0x0 Testable: writeAsRead
19	RW	0x0	RESBAR_CAP_REG_5_32GB Up to 32GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 32 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
18	RW	0x0	RESBAR_CAP_REG_5_16GB Up to 16GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 16 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 GB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CAP_REG_5_8GB Up to 8GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 8 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 GB. Value After Reset: 0x0 Testable: writeAsRead
16	RW	0x0	RESBAR_CAP_REG_5_4GB Up to 4GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 4 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 GB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
15	RW	0x0	RESBAR_CAP_REG_5_2GB Up to 2GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 2 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 GB. Value After Reset: 0x0 Testable: writeAsRead
14	RW	0x0	RESBAR_CAP_REG_5_1GB Up to 1GB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 1 GB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 GB. Value After Reset: 0x0 Testable: writeAsRead
13	RW	0x0	RESBAR_CAP_REG_5_512MB Up to 512MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 512 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 MB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
12	RW	0x0	RESBAR_CAP_REG_5_256MB Up to 256MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 256 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 MB. Value After Reset: 0x0 Testable: writeAsRead
11	RW	0x0	RESBAR_CAP_REG_5_128MB Up to 128MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 128 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 MB. Value After Reset: 0x1 Testable: writeAsRead
10	RW	0x0	RESBAR_CAP_REG_5_64MB Up to 64MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 64 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
9	RW	0x0	RESBAR_CAP_REG_5_32MB Up to 32MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 32 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 MB. Value After Reset: 0x1 Testable: writeAsRead
8	RW	0x0	RESBAR_CAP_REG_5_16MB Up to 16MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 16 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 MB. Value After Reset: 0x1 Testable: writeAsRead
7	RW	0x0	RESBAR_CAP_REG_5_8MB Up to 8MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 8 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 MB. Value After Reset: 0x1 Testable: writeAsRead

Bit	Attr	Reset Value	Description
6	RW	0x0	RESBAR_CAP_REG_5_4MB Up to 4MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 4 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 MB. Value After Reset: 0x1 Testable: writeAsRead
5	RW	0x0	RESBAR_CAP_REG_5_2MB Up to 2MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 2 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 MB. Value After Reset: 0x1 Testable: writeAsRead
4	RW	0x1	RESBAR_CAP_REG_5_1MB Up to 1MB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 1 MB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 MB. Value After Reset: 0x1 Testable: writeAsRead
3:0	RO	0x0	reserved

USP_PCIE_RESBAR_CTRL_REG_5_REG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31	RW	0x0	RESBAR_CTRL_REG_5_8EB Up to 8EB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 8 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 EB. Value After Reset: 0x0 Testable: writeAsRead
30	RW	0x0	RESBAR_CTRL_REG_5_4EB Up to 4EB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 4 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 EB. Value After Reset: 0x0 Testable: writeAsRead
29	RW	0x0	RESBAR_CTRL_REG_5_2EB Up to 2EB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 2 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 EB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
28	RW	0x0	RESBAR_CTRL_REG_5_1EB Up to 1EB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 1 EB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 EB. Value After Reset: 0x0 Testable: writeAsRead
27	RW	0x0	RESBAR_CTRL_REG_5_512PB Up to 512PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 512 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 PB. Value After Reset: 0x0 Testable: writeAsRead
26	RW	0x0	RESBAR_CTRL_REG_5_256PB Up to 256PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 256 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
25	RW	0x0	RESBAR_CTRL_REG_5_128PB Up to 128PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 128 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 128 PB. Value After Reset: 0x0 Testable: writeAsRead
24	RW	0x0	RESBAR_CTRL_REG_5_64PB Up to 64PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 64 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 64 PB. Value After Reset: 0x0 Testable: writeAsRead
23	RW	0x0	RESBAR_CTRL_REG_5_32PB Up to 32PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 32 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 32 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
22	RW	0x0	RESBAR_CTRL_REG_5_16PB Up to 16PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 16 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 16 PB. Value After Reset: 0x0 Testable: writeAsRead
21	RW	0x0	RESBAR_CTRL_REG_5_8PB Up to 8PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 8 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 8 PB. Value After Reset: 0x0 Testable: writeAsRead
20	RW	0x0	RESBAR_CTRL_REG_5_4PB Up to 4PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 4 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 4 PB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
19	RW	0x0	RESBAR_CTRL_REG_5_2PB Up to 2PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 2 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 2 PB. Value After Reset: 0x0 Testable: writeAsRead
18	RW	0x0	RESBAR_CTRL_REG_5_1PB Up to 1PB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 1 PB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 1 PB. Value After Reset: 0x0 Testable: writeAsRead
17	RW	0x0	RESBAR_CTRL_REG_5_512TB Up to 512TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 512 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 512 TB. Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
16	RW	0x0	RESBAR_CTRL_REG_5_256TB Up to 256TB BAR Supported. When Set, indicates that the Function supports operating with the BAR5 sized to 256 TB. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: if (DBI_RO_WR_EN == 1) then R/W(sticky) else R(sticky) Note: This register field is sticky. Values: 0x1 (SET): If Set, function supports operating with BAR sized to 256 TB. Value After Reset: 0x0 Testable: writeAsRead
15:14	RO	0x0	reserved
13:8	RW	0x00	RESBAR_CTRL_REG_BAR_SIZE BAR5 Size. The default value of this field is equal to the default size of the address space that the BAR5 resource is requesting via the BAR?s read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (MIN_VAL): 1MB(2^20 bytes) 0x2b (MAX_VAL): 8EB(2^63 bytes) Value After Reset: 0x7 Testable: writeAsRead
7:5	RO	0x0	RESBAR_CTRL_REG_NUM_BARS Number of Resizeable BARs. This field indicates the total number of resizable BARs in the capability structure for the Function. The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR5 Control register (0) (at offset 008h), and is RsvdP for all others. Note: This register field is sticky. Values: 0x1 (BAR1): one resizable BAR for the function 0x2 (BAR2): two resizable BARs for the function. 0x3 (BAR3): three resizable BARs for the function. 0x4 (BAR4): four resizable BARs for the function. 0x5 (BAR5): five resizable BARs for the function. 0x6 (BAR6): six resizable BARs for the function. Value After Reset: 0x0
4:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x5	RESBAR_CTRL_REG_IDX_5 BAR Index. This encoded value points to the beginning of the BAR5. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size. Note: This register field is sticky. Values: 0x0 (BAR_10h): BAR located at offset 10h. 0x1 (BAR_14h): BAR located at offset 14h. 0x2 (BAR_18h): BAR located at offset 18h. 0x3 (BAR_1Ch): BAR located at offset 1Ch. 0x4 (BAR_20h): BAR located at offset 20h. 0x5 (BAR_24h): BAR located at offset 24h. Value After Reset: 0x5

11.4.4.31 USP_PCIE_PL Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_PL_ACK_LATENCY_TIMER_OFF	0x0000	W	0x0C23040B	Ack Latency Timer and Replay Timer Register
USP_PCIE_PL_VENDOR_SPEC_DLLP_OFF	0x0004	W	0xFFFFFFFF	Vendor Specific DLLP Register
USP_PCIE_PL_PORT_FORCE_OFF	0x0008	W	0x00800004	Port Force Link Register
USP_PCIE_PL_ACK_F_ASPM_CTRL_OFF	0x000C	W	0x1BD2D200	Ack Frequency and L0-L1 ASPM Control Register
USP_PCIE_PL_PORT_LINK_CTRL_OFF	0x0010	W	0x00030120	Port Link Control Register
USP_PCIE_PL_LANE_SKEW_OFF	0x0014	W	0x08000000	Lane Skew Register
USP_PCIE_PL_TIMER_CTRL_MAX_FUNC_NUM_OFF	0x0018	W	0x00000000	Timer Control and Max Function Number Register
USP_PCIE_PL_SYMBOL_TIMER_FILTER_1_OFF	0x001C	W	0x00000140	Symbol Timer Register and Filter Mask 1 Register
USP_PCIE_PL_FILTER_MASK_2_OFF	0x0020	W	0x00000000	Filter Mask 2 Register
USP_PCIE_PL_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF	0x0024	W	0x00000001	AMBA Multiple Outbound Decomposed NP SubRequests Control Register
USP_PCIE_PL_PL_DEBUG0_OFF	0x0028	W	0x00000000	Debug Register 0
USP_PCIE_PL_PL_DEBUG1_OFF	0x002C	W	0x00000000	Debug Register 1
USP_PCIE_PL_TX_P_FC_CREDIT_STATUS_OFF	0x0030	W	0x00000000	Transmit Posted FC Credit Status
USP_PCIE_PL_TX_NP_FC_CREDIT_STATUS_OFF	0x0034	W	0x00000000	Transmit Non-Posted FC Credit Status
USP_PCIE_PL_TX_CPL_FC_CREDIT_STATUS_OFF	0x0038	W	0x00000000	Transmit Completion FC Credit Status

Name	Offset	Size	Reset Value	Description
USP_PCIE_PL_QUEUE_STATUS_OFF	0x003C	W	0x00000000	Queue Status
USP_PCIE_PL_VC_TX_ARBI_1_OFF	0x0040	W	0x0000000F	VC Transmit Arbitration Register 1
USP_PCIE_PL_VC_TX_ARBI_2_OFF	0x0044	W	0x00000000	VC Transmit Arbitration Register 2
USP_PCIE_PL_VC0_P_RX_Q_CTRL_OFF	0x0048	W	0x45227110	Segmented-Buffer VC0 Posted Receive Queue Control
USP_PCIE_PL_VC0_NP_RX_Q_CTRL_OFF	0x004C	W	0x0505C017	Segmented-Buffer VC0 Non-Posted Receive Queue Control
USP_PCIE_PL_VC0_CPL_RX_Q_CTRL_OFF	0x0050	W	0x05000000	Segmented-Buffer VC0 Completion Receive Queue Control
USP_PCIE_PL_GEN2_CTRL_OFF	0x010C	W	0x000102D2	Link Width and Speed Change Control Register
USP_PCIE_PL_PHY_STATUS_OFF	0x0110	W	0x00000000	PHY Status Register
USP_PCIE_PL_PHY_CONTROL_OFF	0x0114	W	0x00000001	PHY Control Register
USP_PCIE_PL_TRGT_MAP_CTRL_OFF	0x011C	W	0x00000047	Programmable Target Map Control Register
USP_PCIE_PL_CLOCK_GATING_CTRL_OFF	0x018C	W	0x00000003	RADM clock gating enable control register
USP_PCIE_PL_GEN3_RELATED_OFF	0x0190	W	0x00000000	Gen3 Control Register
USP_PCIE_PL_GEN3_EQ_CONTROL_OFF	0x01A8	W	0x04059F61	Gen3 EQ Control Register
USP_PCIE_PL_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF	0x01AC	W	0x00000040	Gen3 EQ Direction Change Feedback Mode Control Register
USP_PCIE_PL_ORDER_RULE_CTRL_OFF	0x01B4	W	0x00000000	Order Rule Control Register
USP_PCIE_PL_PIPE_LOOPBACK_CONTROL_OFF	0x01B8	W	0x0000000F	PIPE Loopback Control Register
USP_PCIE_PL_MISC_CONTROL_1_OFF	0x01BC	W	0x00037F40	DBI Read-Only Write Enable Register
USP_PCIE_PL_MULTI_LANE_CONTROL_OFF	0x01C0	W	0x00000080	UpConfigure Multi-lane Control Register
USP_PCIE_PL_PHY_INTEROP_CTRL_OFF	0x01C4	W	0x0001E044	PHY Interoperability Control Register
USP_PCIE_PL_TRGT_CPL_LUT_DELETE_ENTRY_OFF	0x01C8	W	0x00000000	TRGT_CPL_LUT Delete Entry Control Register
USP_PCIE_PL_LINK_FLUSH_CONTROL_OFF	0x01CC	W	0x00000000	Link Reset Request Flush Control Register
USP_PCIE_PL_AMBA_ERROR_RESPONSE_DEFAULT_OFF	0x01D0	W	0x00009C00	AXI Bridge Slave Error Response Register
USP_PCIE_PL_AMBA_LINK_TIMEOUT_OFF	0x01D4	W	0x00000032	Link Down AXI Bridge Slave Timeout Register
USP_PCIE_PL_AMBA_ORDERING_CTRL_OFF	0x01D8	W	0x00000000	AMBA Ordering Control
USP_PCIE_PL_COHERENCY_CONTROL_1_OFF	0x01E0	W	0x00000000	ACE Cache Coherency Control Register 1

Name	Offset	Size	Reset Value	Description
USP_PCIE_PL_COHERENCY_CONTROL_2_OFF	0x01E4	W	0x00000000	ACE Cache Coherency Control Register 2
USP_PCIE_PL_COHERENCY_CONTROL_3_OFF	0x01E8	W	0x00000000	ACE Cache Coherency Control Register 3
USP_PCIE_PL_AXI_MSTR_MSG_ADDR_LOW_OFF	0x01F0	W	0x00000000	Lower 32-bits of the Programmable AXI Address
USP_PCIE_PL_AXI_MSTR_MSG_ADDR_HIGH_OFF	0x01F4	W	0x00000000	Upper 32-bits of the Programmable AXI Address
USP_PCIE_PL_PCIE_VERSION_NUMBER_OFF	0x01F8	W	0x3536302A	PCIe Controller IIP Release Version Number
USP_PCIE_PL_PCIE_VERSION_TYPE_OFF	0x01FC	W	0x6C703035	PCIe Controller IIP Release Version Type
USP_PCIE_PL_MSIX_ADDRESS_MATCH_LOW_OFF	0x0240	W	0x00000000	MSI-X Address Match Low Register
USP_PCIE_PL_MSIX_ADDRESS_MATCH_HIGH_OFF	0x0244	W	0x00000000	MSI-X Address Match High Register
USP_PCIE_PL_MSIX_DOORBELL_OFF	0x0248	W	0x00000000	MSI-X Doorbell Register
USP_PCIE_PL_MSIX_RAM_CTRL_OFF	0x024C	W	0x00000000	MSI-X RAM Power Mode and Debug Control Register
USP_PCIE_PL_DTIM_CTRL0_OFF	0x03B0	W	0x001FFFFF	DTI Master Control Register 0
USP_PCIE_PL_DTIM_CTRL1_OFF	0x03B4	W	0x00000000	DTI Master Control Register 1
USP_PCIE_PL_DTIM_CTRL2_OFF	0x03B8	W	0x00000000	DTI Master Control Register 2
USP_PCIE_PL_DTIM_CTRL3_OFF	0x03BC	W	0x00004210	DTI Master Control Register 3
USP_PCIE_PL_DTIM_CTRL4_OFF	0x03C0	W	0x00000000	DTI Master Control Register 4
USP_PCIE_PL_DTIM_CTRL5_OFF	0x03C4	W	0x00000000	DTI Master Control Register 5
USP_PCIE_PL_DTIM_INT_STATUS_OFF	0x03CC	W	0x00000000	DTI Master Interrupt Status Register
USP_PCIE_PL_DTIM_INT_EN_OFF	0x03D0	W	0x00000000	DTI Master Interrupt Enable Register
USP_PCIE_PL_DTIM_INT_CLR_OFF	0x03D4	W	0x00000000	DTI Master Interrupt Clear Register
USP_PCIE_PL_DTIM_INT_MSK_OFF	0x03D8	W	0x00000000	DTI Master Interrupt Mask Register
USP_PCIE_PL_DTIM_MSI_ADDR_UPR_OFF	0x03DC	W	0x00000000	DTI Master MSI Upper Address Register
USP_PCIE_PL_DTIM_MSI_ADDR_LWR_OFF	0x03E0	W	0x00000000	DTI Master MSI Lower Address Register
USP_PCIE_PL_DTIM_MSI_DATA_OFF	0x03E4	W	0x00000000	DTI Master MSI Data Register
USP_PCIE_PL_DTIM_ERR_LOG0_OFF	0x03E8	W	0x00000000	DTI Master Error Logging Register 0
USP_PCIE_PL_DTIM_ERR_LOG1_OFF	0x03EC	W	0x00000000	DTI Master Error Logging Register 1
USP_PCIE_PL_DTIM_ERR_LOG2_OFF	0x03F0	W	0x00000000	DTI Master Error Logging Register 2

Name	Offset	Size	Reset Value	Description
USP_PCIE_PL_DTIM_DIAG_OFF	0x03FC	W	0x00000010	DTI Master Debug Diagnostic Register
USP_PCIE_PL_PL_APP_BUS_DEV_NUM_STATUS_OFF	0x0410	W	0x00000000	Application Driven bus and Device Number Register
USP_PCIE_PL_PCIPM_TRAFFIC_CTRL_OFF	0x041C	W	0x00000000	TLP Traffic during Non-D0 State Control Register
USP_PCIE_PL_PL_LTR_LATENCY_OFF	0x0430	W	0x00000000	LTR Latency Register
USP_PCIE_PL_AUX_CLK_FREQ_OFF	0x0440	W	0x00000018	Auxiliary Clock Frequency Control Register
USP_PCIE_PL_L1_SUBSTATES_OFF	0x0444	W	0x000000D2	L1 Substates Timing Register
USP_PCIE_PL_POWERDOWN_CTRL_STATUS_OFF	0x0448	W	0x00000020	Powerdown Control and Status Register
USP_PCIE_PL_PIPE_RELATED_OFF	0x0490	W	0x00000000	PIPE Related Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.32 USP_PCIE_PL Detail Registers Description

USP_PCIE_PL_ACK_LATENCY_TIMER_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0c23	REPLAY_TIME_LIMIT Replay Timer Limit. The replay timer expires when it reaches this limit. The controller initiates a replay upon reception of a NAK or when the replay timer expires. For more details, see "Transmit Replay" in the Databook. You can modify the effective timer limit through the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-4, 3-5, and 3-6 of the PCI Express Base Specification. If there is a change in the payload size or link speed, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. Value After Reset: 0xc23 Testable: untestable Volatile: true

Bit	Attr	Reset Value	Description
15:0	RW	0x040b	ROUND_TRIP_LATENCY_TIME_LIMIT Ack Latency Timer Limit. The Ack latency timer expires when it reaches this limit. For more details, see "ACK/NAK Scheduling" in the Databook. You can modify the effective timer limit through the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-7, 3-8, and 3-9 of the PCI Express Base Specification. The limit must reflect the round trip latency from requester to completer. If there is a change in the payload size or link width, the controller overrides any value that you have written to this register field, and resets the field back to the specification-defined value. The controller does not change the value in the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. Value After Reset: 0x40b Testable: untestable Volatile: true

USP_PCIE_PL_VENDOR_SPEC_DLLP_OFF
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	VENDOR_SPEC_DLLP Vendor Specific DLLP Register. You can use this register to send a specific PCI Express DLLP. Your application can write 8-bit DLLP Type and 24-bit Payload data into this register, and set the VENDOR_SPECIFIC_DLLP_REQ field of the PORT_LINK_CTRL_OFF, to send the DLLP. Bits[7:0]: DLLP Type Bits[31:8]: Vendor Defined Payload (24 bits) Note: This register field is sticky. Values: 0x0 (ZERO): Zero value 0xffffffff (MAX): Max value Value After Reset: 0xffffffff

USP_PCIE_PL_PORT_FORCE_OFF
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x1	DO_DESKEW_FOR_SRIS Use the transitions from TS2 to Logical Idle Symbol, SKP OS to Logical Idle Symbol, EIEOS to Logical Idle Symbol, and FTS Sequence to SKP OS to do deskew instead of using received SKP OS or TS1 to TS2 transition if DO_DESKEW_FOR_SRIS is set to '1'. Note: This register field is sticky. Value After Reset: 0x1
22	RW	0x0	SUPPORT_PART_LANES_RXEI_EXIT Support LTSSM transition from Polling.Active to Polling.Config based on Rx 8 TSs on any lanes which are Rx EI exit too from base spec after 24ms timeout. This prevents some lanes detected but not Rx EI exit and LTSSM cannot move to Polling.Config. You must set the parameter CX_AUTO_LANE_FLIP_CTRL_EN true for the auto lanes reversal. Note: This register field is sticky. Values: 0x1 (SUPPORT): Any lanes receives 8 consecutive TS OSs, LTSSM moves from Polling.Active to Polling.Config. If all lanes do not receive 8 consecutive TS OSs and any predetermined lanes are still on Rx ElecIdle, LTSSM moves from Polling.Active to Polling.Compliance. 0x0 (UNSUPPORT): Any lanes receives 8 consecutive TS OS and all predetermined lanes have Rx ElecIdle exit, LTSSM moves from Polling.Active to Polling.Config. This is legacy mode from Base Spec. Any predetermined lanes are still on Rx ElecIdle, LTSSM moves from Polling.Active to Polling.Compliance. Value After Reset: 0x0
21:16	RW	0x00	LINK_STATE Forced LTSSM State. The LTSSM state that the controller is forced to when you set the FORCE_EN bit (Force Link). LTSSM state encoding is defined by the lts_state variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15	WO	0x0	FORCE_EN Force Link. The controller supports a testing and debug capability to allow your software to force the LTSSM state machine into a specific state, and to force the controller to transmit a specific Link Command. Asserting this bit triggers the following actions: Forces the LTSSM to the state specified by the Forced LTSSM State field. Forces the controller to transmit the command specified by the Forced Link Command field. This is a self-clearing register field. Reading from this register field always returns a '0'. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0 Testable: writeAsRead Volatile: true
14:12	RO	0x0	reserved
11:8	RW	0x0	FORCED_LTSSM Forced Link Command. The link command that the controller is forced to transmit when you set FORCE_EN bit (Force Link). Link command encoding is defined by the ltssm_cmd variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky. Value After Reset: 0x0
7:0	RW	0x04	LINK_NUM Link Number. Not used for endpoint. Note: This register field is sticky. Value After Reset: 0x4

USP_PCIE_PL_ACK_F_ASPM_CTRL_OFF

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30	RW	0x0	ENTER_ASPM ASPM L1 Entry Control. Note: This register field is sticky. Values: 0x1 (IDLE_TO_L1): Controller enters ASPM L1 after a period in which it has been idle. 0x0 (L0S_TO_L1): Controller enters ASPM L1 only after idle period during which both receive and transmit are in L0s. Value After Reset: 0x0
29:27	RW	0x3	L1_ENTRANCE_LATENCY L1 Entrance Latency. Note: Programming this timer with a value greater that 32us has no effect unless extended sync is used, or all of the credits are infinite. Note: This register field is sticky. Values: 0x0 (_1_US): 1 us 0x1 (_2_US): 2 us 0x2 (_4_US): 4 us 0x3 (_8_US): 8 us 0x4 (_16_US): 16 us 0x5 (_32_US): 32 us 0x6 (_64_US): 64Us 0x7 (_64US_): 64 us Value After Reset: 0x3
26:24	RW	0x3	L0S_ENTRANCE_LATENCY L0s Entrance Latency. Note: This register field is sticky. Values: 0x0 (_1_US): 1 us 0x1 (_2_US): 2 us 0x2 (_3_US): 3 us 0x3 (_4_US): 4 us 0x4 (_5_US): 5 us 0x5 (_6_US): 6 us 0x6 (_7_US): 7 US 0x7 (_7US_): 7 us Value After Reset: 0x3

Bit	Attr	Reset Value	Description
23:16	RO	0xd2	COMMON_CLK_N_FTS Common Clock N_FTS. This is the N_FTS when common clock is used. The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. This field is only writable (sticky) when all of the following configuration parameter equations are true: CX_NFTS !=CX_COMM_NFTS DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY Note: The access attributes of this field are as follows: Wire: R Dbi: R Values: 0x0 (ZERO): The controller does not support a value of zero; a value of zero can cause the LTSSM to go into the recovery state when exiting from L0s. 0xff (MAX_VAL): The maximum number of FTS ordered-sets that a component can request is 255. Value After Reset: 0xd2
15:8	RW	0xd2	ACK_N_FTS The number of Fast Training Sequence(N_FTS) ordered sets to be transmitted when transitioning from L0s to L0. Note: This register field is sticky. Values: 0x0 (ZERO): The controller does not support a value of zero; a value of zero can cause the LTSSM to go into the recovery state when exiting from L0s. 0xff (MAX_VAL): The maximum number of FTS ordered-sets that a component can request is 255. Value After Reset: 0xd2

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ACK_FREQ Ack Frequency. The controller accumulates the number of pending ACKs specified here (up to 255) before scheduling an ACK DLLP. 0: Indicates that this Ack Frequency Counter feature is turned off. The controller generates a low-priority ACK request for every TLP that it receives. The controller waits until the ACK Latency Timer expires, then converts the current low-priority ACK request to a high-priority ACK request and schedules the DLLP for transmission to the remote link partner. 1-255: Indicates that the controller will schedule a high-priority ACK after receiving this number of TLPs. It might schedule the ACK before receiving this number of TLPs if the ACK Latency Timer expires, but never later. For a typical system, you do not have to modify the default setting. For more details, see "ACK/NAK Scheduling" in the Databook. Note: This register field is sticky. Values: 0x0 (MIN_VAL): The value '0' indicates that this Ack Frequency Counter feature is turned off. 0xff (MAX_VAL): Any value between 1 and 255 indicates that the controller will schedule a high-priority ACK after receiving the specified number of TLPs. Value After Reset: 0x0

USP_PCIE_PL_PORT_LINK_CTRL_OFF
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	TRANSMIT_LANE_REVERSALE_ENABLE TRANSMIT_LANE_REVERSALE_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
26	RW	0x0	EXTENDED_SYNCH EXTENDED_SYNCH is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
25	RW	0x0	CORRUPT_LCRC_ENABLE CORRUPT_LCRC_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
24	RW	0x0	BEACON_ENABLE BEACON_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
23:22	RO	0x0	reserved
21:16	RW	0x03	LINK_CAPABLE Link Mode Enable. Sets the number of lanes in the link that you want to connect to the link partner. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Predetermined Number of Lanes" field of the "Link Width and Speed Change Control Register". For more information, see "How to Tie Off Unused Lanes". For information on upsizing and downsizing the link width, see "Link Establishment". Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (X1): x1 0x3 (X2): x2 0x7 (X4): x4 0xf (X8): x8 0x1f (X16): x16 0x3f (X32): x32 (not supported) Value After Reset: 0x7 Testable: unconstrained
15:12	RO	0x0	reserved
11:8	RW	0x1	LINK_RATE LINK_RATE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
7	RW	0x0	FAST_LINK_MODE Fast Link Mode. Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation. Forces the LTSSM training (link initialization) to use shorter time-outs and to link up faster. The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. Fast Link Mode can also be activated by setting the diag_ctrl_bus[2] pin to '1'. For more details, see the "Fast Link Simulation Mode" section in the "Integrating the Controller with the PHY or Application RTL or Verification IP" chapter of the User Guide. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
6	RW	0x0	LINK_DISABLE LINK_DISABLE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
5	RW	0x1	DLL_LINK_EN DLL Link Enable. Note: This register field is sticky. Values: 0x1 (ENABLE): Enables link initialization. 0x0 (DISABLE): The controller does not transmit InitFC DLLPs and does not establish a link. Value After Reset: 0x1
4	RO	0x0	reserved
3	RW	0x0	RESET_ASSERT Reset Assert. Triggers a recovery and forces the LTSSM to the hot reset state (downstream port only). Note: This register field is sticky. Values: 0x1 (SET): Set 0x0 (CLEAR): Clear Value After Reset: 0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	LOOPBACK_ENABLE Loopback Enable. Turns on loopback. For more details, see "Loopback" in the Databook. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
1	RW	0x0	SCRAMBLE_DISABLE Scramble Disable. Turns off data scrambling. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
0	W1C	0x0	VENDOR_SPECIFIC_DLLP_REQ Vendor Specific DLLP Request. Reading from this self-clearing register field always returns a '0'. Values: 0x1 (SET): When software writes a '1' to this bit, the controller transmits the DLLP contained in the VENDOR_SPEC_DLLP field of VENDOR_SPEC_DLLP_OFF 0x0 (CLEAR): This is a self clearing register Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_LANE_SKEW_OFF
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	DISABLE_LANE_TO_LANE_DESKEW Disable Lane-to-Lane Deskew. Causes the controller to disable the internal Lane-to-Lane deskew logic. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
30:27	RW	0x1	IMPLEMENT_NUM_LANES Implementation-specific Number of Lanes. Set the implementation-specific number of lanes. The number of lanes to be used when in Loopback Master. The number of lanes programmed must be equal to or less than the valid number of lanes set in LINK_CAPABLE field. You must configure this field before initiating Loopback by writing in the LOOPBACK_ENABLE field. The controller will transition from Loopback.Entry to Loopback.Active after receiving two consecutive TS1 Ordered Sets with the Loopback bit asserted on the implementation specific number of lanes configured in this field. Note: This register field is sticky. Values: 0x0 (_1_LANE): 1 lane 0x1 (_2_LANE): 2 lanes 0x3 (_4_LANE): 4 lanes 0x7 (_8_LANE): 8 lanes 0xf (_16_LANE): 16 lanes Value After Reset: 0x3
26	RW	0x0	ELASTIC_BUFFER_MODE Selects Elasticity Buffer operating mode: Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (HALF_FULL): Nominal Half Full Buffer mode 0x1 (EMPTY): Nominal Empty Buffer Mode Value After Reset: 0x1

Bit	Attr	Reset Value	Description
25	RW	0x0	ACK_NAK_DISABLE Ack/Nak Disable. Prevents the controller from sending ACK and NAK DLLPs. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
24	RW	0x0	FLOW_CTRL_DISABLE Flow Control Disable. Prevents the controller from sending FC DLLPs. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
23:0	RW	0x000000	INSERT_LANE_SKEW INSERT_LANE_SKEW is an internally reserved field. Do not use. Note: This register field is sticky. Values: 0x0 (MIN): Zero value 0xff (MAX): Max value Value After Reset: 0x0

USP_PCIE_PL_TIMER_CTRL_MAX_FUNC_NUM_OFF
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x0	FAST_LINK_SCALING_FACTOR Fast Link Timer Scaling Factor. Sets the scaling factor of LTSSM timer when FAST_LINK_MODE field in PORT_LINK_CTRL_OFF is set to '1'. Default is set by the hidden configuration parameter DEFAULT_FAST_LINK_SCALING_FACTOR which defaults to '0'. Note: This register field is sticky. Values: 0x0 (SF_1024): Scaling Factor is 1024 (1ms is 1us). When the LTSSM is in Config or L12 Entry State, 1ms timer is 2us, 2ms timer is 4us and 3ms timer is 6us. 0x1 (SF_256): Scaling Factor is 256 (1ms is 4us) 0x2 (SF_64): Scaling Factor is 64 (1ms is 16us) 0x3 (SF_16): Scaling Factor is 16 (1ms is 64us) Value After Reset: 0x2

Bit	Attr	Reset Value	Description
28:24	RW	0x00	UPDATE_FREQ_TIMER UPDATE_FREQ_TIMER is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
23:19	RW	0x00	TIMER_MOD_ACK_NAK Ack Latency Timer Modifier. Increases the timer value for the Ack latency timer in increments of 64 clock cycles. A value of '0' represents no modification to the timer value. For more details, see the ROUND_TRIP_LATENCY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. Note: This register field is sticky. Value After Reset: 0x0
18:14	RW	0x00	TIMER_MOD_REPLAY_TIMER Replay Timer Limit Modifier. Increases the time-out value for the replay timer in increments of 64 clock cycles at Gen1 or Gen2 speed, and in increments of 256 clock cycles at Gen3 speed. A value of '0' represents no modification to the timer limit. For more details, see the REPLAY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. At Gen3 speed, the controller automatically changes the value of this field to DEFAULT_GEN3_REPLAY_ADJ. Note: This register field is sticky. Value After Reset: 0xa Testable: writeAsRead Reset Mask: 0x0 Volatile: true
13:8	RO	0x00	reserved
7:0	RW	0x00	MAX_FUNC_NUM Maximum function number that can be used in a request. Configuration requests targeted at function numbers above this value are returned with UR (unsupported request). Note: This register field is sticky. Values: 0x0 (MIN): Zero value 0xff (MAX): Max value Value After Reset: 0x0

USP_PCIE_PL_SYMBOL_TIMER_FILTER_1_OFF
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RW	0x0	CX_FLT_MASK_RC_CFG_DISCARD CX_FLT_MASK_RC_CFG_DISCARD 0: For RADM RC filter to not allow CFG transaction being received 1: For RADM RC filter to allow CFG transaction being received
30	RW	0x0	CX_FLT_MASK_RC_IO_DISCARD CX_FLT_MASK_RC_IO_DISCARD 0: For RADM RC filter to not allow IO transaction being received 1: For RADM RC filter to allow IO transaction being received
29	RW	0x0	CX_FLT_MASK_MSG_DROP CX_FLT_MASK_MSG_DROP 0: Drop MSG TLP (except for Vendor MSG). Send decoded message on the SII. 1: Do not Drop MSG (except for Vendor MSG). Send message TLPs to your application on TRGT1 and send decoded message on the SII. The default for this bit is the inverse of FLT_DROP_MSG. That is, if FLT_DROP_MSG =1, then the default of this bit is '0' (drop message TLPs). This bit only controls message TLPs other than Vendor MSGs. Vendor MSGs are controlled by Filter Mask Register 2, bits [1:0]. The controller never passes ATS Invalidate messages to the SII interface regardless of this filter rule setting. The controller passes all ATS Invalidate messages to TRGT1 (or AXI bridge master), as they are too big for the SII.
28	RW	0x0	CX_FLT_MASK_CPL_ECRC_DISCARD CX_FLT_MASK_CPL_ECRC_DISCARD Only used when completion queue is advertised with infinite credits and is in store-and-forward mode. 0: Discard completions with ECRC errors 1: Allow completions with ECRC errors to be passed up Reserved field for SW.
27	RW	0x0	CX_FLT_MASK_ECRC_DISCARD CX_FLT_MASK_ECRC_DISCARD 0: Discard TLPs with ECRC errors 1: Allow TLPs with ECRC errors to be passed up
26	RW	0x0	CX_FLT_MASK_CPL_LEN_MATCH CX_FLT_MASK_CPL_LEN_MATCH 0: Enforce length match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err 1: Mask length match for completions
25	RW	0x0	CX_FLT_MASK_CPL_ATTR_MATCH CX_FLT_MASK_CPL_ATTR_MATCH 0: Enforce attribute match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask attribute match for completions

Bit	Attr	Reset Value	Description
24	RW	0x0	CX_FLT_MASK_CPL_TC_MATCH CX_FLT_MASK_CPL_TC_MATCH 0: Enforce Traffic Class match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Traffic Class match for completions
23	RW	0x0	CX_FLT_MASK_CPL_FUNC_MATCH CX_FLT_MASK_CPL_FUNC_MATCH 0: Enforce function match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask function match for completions
22	RW	0x0	CX_FLT_MASK_CPL_REQID_MATCH CX_FLT_MASK_CPL_REQID_MATCH 0: Enforce Req. Id match for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Req. Id match for completions
21	RW	0x0	CX_FLT_MASK_CPL_TAGERR_MATCH CX_FLT_MASK_CPL_TAGERR_MATCH 0: Enforce Tag Error Rules for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Tag Error Rules for completions
20	RW	0x0	CX_FLT_MASK_LOCKED_RD_AS_UR CX_FLT_MASK_LOCKED_RD_AS_UR 0: Treat locked Read TLPs as UR for EP; Supported for RC 1: Treat locked Read TLPs as Supported for EP; UR for RC
19	RW	0x0	CX_FLT_MASK_CFG_TYPE1_REQ_AS_UR CX_FLT_MASK_CFG_TYPE1_REQ_AS_UR 0: Treat CFG type1 TLPs as UR for EP; Supported for RC 1: Treat CFG type1 TLPs as Supported for EP; UR for RC When CX_SRIOV_ENABLE is set then this bit is set to allow the filter to process Type 1 Config requests if the EP consumes more than one bus number.
18	RW	0x0	CX_FLT_MASK_UR_OUTSIDE_BAR CX_FLT_MASK_UR_OUTSIDE_BAR 0: Treat out-of-bar TLPs as UR 1: Do not treat out-of-bar TLPs as UR
17	RW	0x0	CX_FLT_MASK_UR_POIS CX_FLT_MASK_UR_POIS 0: Treat poisoned request TLPs as UR 1: Do not treat poisoned request TLPs as UR The native controller always passes poisoned completions to your application except when you are using the DMA read channel.

Bit	Attr	Reset Value	Description
16	RW	0x0	CX_FLT_MASK_UR_FUNC_MISMATCH CX_FLT_MASK_UR_FUNC_MISMATCH 0: Treat Function MisMatched TLPs as UR 1: Do not treat Function MisMatched TLPs as UR Note: This register field is sticky. Value After Reset: 0x0
15	RW	0x0	DISABLE_FC_WD_TIMER Disable FC Watchdog Timer. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
14:11	RW	0x0	EIDLE_TIMER EIDLE_TIMER is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
10:0	RW	0x140	SKP_INT_VAL SKP Interval Value. The number of symbol times to wait between transmitting SKP ordered sets. The controller waits the number of symbol times in this register plus 1, between transmitting SKP ordered sets. Your application must program this register accordingly. For example, if 1536 were programmed into this register (in a 250 MHz controller), then the controller actually transmits SKP ordered sets once every 1537 symbol times. The value programmed to this register is actually clock ticks and not symbol times. In a 125 MHz controller, programming the value programmed to this register should be scaled down by a factor of 2 (because one clock tick =two symbol times in this case). Note: This value is not used at Gen3 speed; the skip interval is hardcoded to 370 blocks. Note: This register field is sticky. Value After Reset: 0x140

USP_PCIE_PL_FILTER_MASK_2_OFF

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	CX_FLT_MASK_CPL_IN_LUT_CHECK CX_FLT_MASK_CPL_IN_LUT_CHECK 0: Disable masking of checking if the tag of CPL is registered in LUT 1: Enable masking of checking if the tag of CPL is registered in LUT
8	RW	0x0	CX_FLT_MASK_POIS_ERROR_REPORTING CX_FLT_MASK_POIS_ERROR_REPORTING 0: Disable masking of error reporting for Poisoned TLPs 1: Enable masking of error reporting for Poisoned TLPs
7	RW	0x0	CX_FLT_MASK_PRS_DROP CX_FLT_MASK_PRS_DROP 0: Allow PRS message to pass through 1: Drop PRS Messages silently This bit is ignored when the CX_FLT_MASK_MSG_DROP bit in the MASK_RADM_1 field of the SYMBOL_TIMER_FILTER_1_OFF register is set to '1'.
6	RW	0x0	CX_FLT_UNMASK_TD CX_FLT_UNMASK_TD 0: Disable unmask TD bit if CX_STRIP_ECRC_ENABLE 1: Enable unmask TD bit if CX_STRIP_ECRC_ENABLE
5	RW	0x0	CX_FLT_UNMASK_UR_POIS_TRGT0 CX_FLT_UNMASK_UR_POIS_TRGT0 0: Disable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination 1: Enable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination
4	RW	0x0	CX_FLT_MASK_LN_VENMSG1_DROP CX_FLT_MASK_LN_VENMSG1_DROP 0: Allow LN message to pass through 1: Drop LN Messages silently
3	RW	0x0	CX_FLT_MASK_HANDLE_FLUSH CX_FLT_MASK_HANDLE_FLUSH 0: Disable controller Filter to handle flush request 1: Enable controller Filter to handle flush request
2	RW	0x0	CX_FLT_MASK_DABORT_4UCPL CX_FLT_MASK_DABORT_4UCPL 0: Enable DLLP abort for unexpected completion 1: Do not enable DLLP abort for unexpected completion
1	RW	0x0	CX_FLT_MASK_VENMSG1_DROP CX_FLT_MASK_VENMSG1_DROP 0: Vendor MSG Type 1 dropped silently 1: Vendor MSG Type 1 not dropped

Bit	Attr	Reset Value	Description
0	RW	0x0	CX_FLT_MASK_VENMSG0_DROP CX_FLT_MASK_VENMSG0_DROP 0: Vendor MSG Type 0 dropped with UR error reporting 1: Vendor MSG Type 0 not dropped

USP_PCIE_PL_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	OB_RD_SPLIT_BURST_EN Enable AMBA Multiple Outbound Decomposed NP SubRequests. You should not clear this register unless your application master is requesting an amount of read data greater than Max_Read_Request_Size, and the remote device (or switch) is reordering completions that have different tags. For more details, see "AXI Bridge Ordering" in the AXI chapter of the Databook. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (DISABLE): This bit when set to '0' disables the possibility of having multiple outstanding non-posted requests that were derived from decomposition of an outbound AMBA request. 0x1 (ENABLE): Enable Value After Reset: 0x1

USP_PCIE_PL_PL_DEBUG0_OFF
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DEB_REG_0 The value on cxpl_debug_info[31:0]. Values: 0x0 (ZERO): Zero value. 0xffffffff (MAX): Max value. Value After Reset: 0x0 Testable: untestable Reset Mask: 0x0 Volatile: true

USP_PCIE_PL_PL_DEBUG1_OFF
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DEB_REG_1 The value on cxpl_debug_info[63:32]. Values: 0x0 (ZERO): Zero value. 0xffffffff (MAX): Max value. Value After Reset: 0x0 Testable: untestable Reset Mask: 0x0 Volatile: true

USP_PCIE_PL_TX_P_FC_CREDIT_STATUS_OFF

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_P_HEADER_FC_CREDIT Transmit Posted Header FC Credits. The posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_P_DATA_FC_CREDIT Transmit Posted Data FC Credits. The posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

USP_PCIE_PL_TX_NP_FC_CREDIT_STATUS_OFF

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_NP_HEADER_FC_CREDIT Transmit Non-Posted Header FC Credits. The non-posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_NP_DATA_FC_CREDIT Transmit Non-Posted Data FC Credits. The non-posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised non-posted credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_TX_CPL_FC_CREDIT_STATUS_OFF
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_CPL_HEADER_FC_CREDIT Transmit Completion Header FC Credits. The Completion Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_CPL_DATA_FC_CREDIT Transmit Completion Data FC Credits. The Completion Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data Scaled Flow Control: [4'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [4'b0, 12'hFFF, 16'hFFFF]. No Scaling: [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF]. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_QUEUE_STATUS_OFF
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	TIMER_MOD_FLOW_CONTROL_EN FC Latency Timer Override Enable. Note: This register field is sticky. Values: 0x1 (SET): When this bit is set, the value from the "FC Latency Timer Override Value" field in this register will override the FC latency timer value that the controller calculates according to the PCIe specification. 0x0 (CLEAR): Clear Value After Reset: 0x0
30:29	RO	0x0	reserved
28:16	RW	0x0000	TIMER_MOD_FLOW_CONTROL FC Latency Timer Override Value. When you set the "FC Latency Timer Override Enable" in this register, the value in this field will override the FC latency timer value that the controller calculates according to the PCIe specification. For more details, see "Flow Control" in the Databook. Note: This register field is sticky. Value After Reset: 0x0
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RO	0x0	RX_SERIALIZATION_Q_NON_EMPTY Receive Serialization Queue Not Empty. Values: 0x1 (SET): Indicates there is data in the serialization queue. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true
12:4	RO	0x000	reserved
3	W1C	0x0	RX_QUEUE_OVERFLOW Receive Credit Queue Overflow. Values: 0x1 (SET): Indicates insufficient buffer space available to write to the P/NP/CPL credit queue. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RO	0x0	RX_QUEUE_NON_EMPTY Receive Credit Queue Not Empty. Values: 0x1 (SET): Indicates there is data in one or more of the receive buffers. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	RO	0x0	TX_RETRY_BUFFER_NE Transmit Retry Buffer Not Empty. Values: 0x1 (SET): Indicates that there is data in the transmit retry buffer. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RO	0x0	RX_TLP_FC_CREDIT_NON_RETURN Received TLP FC Credits Not Returned. Values: 0x1 (SET): Indicates that the controller has received a TLP but has not yet sent an UpdateFC DLLP indicating that the credits for that TLP have been restored by the receiver at the other end of the link. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_VC_TX_ARBI_1_OFF
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	WRR_WEIGHT_VC_3 WRR Weight for VC3. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0
23:16	RW	0x00	WRR_WEIGHT_VC_2 WRR Weight for VC2. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0
15:8	RO	0x00	WRR_WEIGHT_VC_1 WRR Weight for VC1. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0
7:0	RO	0x0f	WRR_WEIGHT_VC_0 WRR Weight for VC0. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0xf

USP_PCIE_PL_VC_TX_ARBI_2_OFF
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	WRR_WEIGHT_VC_7 WRR Weight for VC7. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0
23:16	RW	0x00	WRR_WEIGHT_VC_6 WRR Weight for VC6. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0
15:8	RW	0x00	WRR_WEIGHT_VC_5 WRR Weight for VC5. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0
7:0	RW	0x00	WRR_WEIGHT_VC_4 WRR Weight for VC4. Note: The access attributes of this field are as follows: Wire: R Dbi: R Value After Reset: 0x0

USP_PCIE_PL_VC0_P_RX_Q_CTRL_OFF
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RW	0x0	VC_ORDERING_RX_Q VC Ordering for Receive Queues. Determines the VC ordering rule for the receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky. Values: 0x1 (STRICT_ORDERING): Strict ordering, higher numbered VCs have higher priority 0x0 (ROUND_ROBIN): Round robin Value After Reset: 0x0

Bit	Attr	Reset Value	Description
30	RW	0x1	TLP_TYPE_ORDERING_VC0 TLP Type Ordering for VC0. Determines the TLP type ordering rule for VC0 receive queues, used only in the segmented-buffer configuration: Note: This register field is sticky. Values: 0x1 (PCIE_ORDERING_RULE): PCIe ordering rules (recommended) 0x0 (STRICT_ORDERING): Strict ordering: posted, completion, then non-posted Value After Reset: 0x1
29:28	RO	0x0	reserved
27:26	RW	0x1	VC0_P_DATA_SCALE VC0 Scale Posted Data Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
25:24	RW	0x1	VC0_P_HDR_SCALE VC0 Scale Posted Header Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
23:22	RO	0x0	reserved
21	RW	0x1	VC0_P_TLP_Q_MODE Reserved. Note: This register field is sticky. Value After Reset: 0x1
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:12	RO	0x27	VC0_P_HEADER_CREDIT VC0 Posted Header Credits. The number of initial posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xff (MAX_VAL): Max value Value After Reset: 0x5c
11:0	RO	0x110	VC0_P_DATA_CREDIT VC0 Posted Data Credits. The number of initial posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xfff (MAX_VAL): Max value Value After Reset: 0x110

USP_PCIE_PL_VC0_NP_RX_Q_CTRL_OFF

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x1	VC0_NP_DATA_SCALE VC0 Scale Non-Posted Data Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1

Bit	Attr	Reset Value	Description
25:24	RW	0x1	VC0_NP_HDR_SCALE VC0 Scale Non-Posted Header Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
23	RO	0x0	reserved
22:21	RW	0x0	VC0_NP_TLP_Q_MODE Reserved. Note: This register field is sticky. Value After Reset: 0x1
20	RO	0x0	reserved
19:12	RO	0x5c	VC0_NP_HEADER_CREDIT VC0 Non-Posted Header Credits. The number of initial non-posted header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xff (MAX_VAL): Max value Value After Reset: 0x5c
11:0	RO	0x017	VC0_NP_DATA_CREDIT VC0 Non-Posted Data Credits. The number of initial non-posted data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xfff (MAX_VAL): Max value Value After Reset: 0x17

USP_PCIE_PL_VC0_CPL_RX_Q_CTRL_OFF
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x1	VC0_CPL_DATA_SCALE VC0 Scale CPL Data Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
25:24	RW	0x1	VC0_CPL_HDR_SCALE VC0 Scale CPL Header Credits. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3 (MAX_VAL): Max value Value After Reset: 0x1
23	RO	0x0	reserved
22:21	RW	0x0	VC0_CPL_TLP_Q_MODE Reserved. Note: This register field is sticky. Value After Reset: 0x1
20	RO	0x0	reserved
19:12	RO	0x00	VC0_CPL_HEADER_CREDIT VC0 Completion Header Credits. The number of initial Completion header credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xff (MAX_VAL): Max value Value After Reset: 0x0

Bit	Attr	Reset Value	Description
11:0	RO	0x000	VC0_CPL_DATA_CREDIT VC0 Completion Data Credits. The number of initial Completion data credits for VC0, used only in the segmented-buffer configuration. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xfff (MAX_VAL): Max value Value After Reset: 0x0

USP_PCIE_PL_GEN2_CTRL_OFF

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	FORCE_LANE_FLIP Enable to force the LANE_UNDER_TEST physical lane flips to logical lane 0. All the other physical lanes are turned off. The LINK_CAPABLE register must be set to 1 and only x1 link can be formed if the FORCE_LANE_FLIP register is set to 1. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
29:25	RO	0x00	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	LANE_UNDER_TEST The Lane Under Test is the lane for Forced Lane Flip or for Loopback Eq. Only one lane is configured each time. The default of this field is the CX_DEFAULT_LANE_UNDER_TEST configuration parameter. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero 0x1 (MAX_VAL): CX_NL Value After Reset: 0x0
23	RW	0x0	SELECTABLE_DEEMPH_BIT_MUX The selectable deemphasis bit (Symbol 4 bit 6) of the transmitted TS2 Ordered Sets for DSP in Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP. Note: This register field is sticky. Values: 0x0 (FROM_LINK_CTRL_2_REG): The value from the Selectable De-emphasis field in the Link Control 2 register 0x1 (REQUESTED_BY_USP): The value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP Value After Reset: 0x0
22	RW	0x0	SELECT_DEEMPH_VAR_MUX The select_deemphasis variable for DSP on entry to Recovery.RcvrCfg state is muxed between the Selectable De-emphasis field in the Link Control 2 register and the value requested by the Upstream Port in the eight consecutive TS1 Ordered Sets it received. Note: This register field is sticky. Values: 0x0 (REQUESTED_BY_USP): The value requested by USP in Recovery.RcvrLock state through Tx TS1s from USP 0x1 (FROM_LINK_CTRL_2_REG): The value from the Selectable De-emphasis field in the Link Control 2 register Value After Reset: 0x0

Bit	Attr	Reset Value	Description
21	RW	0x0	GEN1_EI_INFERENCE Electrical Idle Inference Mode at Gen1 Rate. Programmable mode to determine inferred electrical idle (EI) in Recovery.Speed or Loopback.Active (as slave) state at Gen1 speed by looking for a '1' value on RxElecIdle instead of looking for a '0' on RxValid. If the PHY fails to deassert the RxValid signal in Recovery.Speed or Loopback.Active (because of corrupted EIOS for example), then EI cannot be inferred successfully in the controller by just detecting the condition RxValid=0. Note: This register field is sticky. Values: 0x0 (RXELECIDLE_TO_INFER): Use RxElecIdle signal to infer Electrical Idle 0x1 (RXVALID_TO_INFER): Use RxValid signal to infer Electrical Idle Value After Reset: 0x0
20	RW	0x0	SEL_DEEMPHASIS Used to set the de-emphasis level for upstream ports. This bit selects the level of de-emphasis the link operates at. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (N_6DB): -6 dB 0x1 (N_3_5DB): -3.5 dB Value After Reset: 0x0
19	RW	0x0	CONFIG_TX_COMP_RX Config Tx Compliance Receive Bit. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (SET): When set to 1, signals LTSSM to transmit TS ordered sets with the compliance receive bit assert (equal to '1'). 0x0 (CLEAR): Clear Value After Reset: 0x0

Bit	Attr	Reset Value	Description
18	RW	0x0	CONFIG_PHY_TX_CHANGE Config PHY Tx Swing. Controls the PHY transmitter voltage swing level. The controller drives the mac_phy_txswing output from this register bit field. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (FULL_SWING): Full Swing 0x1 (LOW_SWING): Low Swing Value After Reset: 0x0
17	RW	0x0	DIRECT_SPEED_CHANGE Directed Speed Change. When the speed change occurs, the controller will clear the contents of this field; and a read to this field by your software will return a '0'. To manually initiate the speed change: Write to LINK_CONTROL2_LINK_STATUS2_REG.PCIE_CAP_TARGET_LINK_SPEED in the local device Deassert this field Assert this field If you set the default of this field using the DEFAULT_GEN2_SPEED_CHANGE configuration parameter to '1', then the speed change is initiated automatically after link up, and the controller clears the contents of this field. If you want to prevent this automatic speed change, then write a lower speed value to the Target Link Speed field of the Link Control 2 register (LINK_CONTROL2_LINK_STATUS2_OFF.PCIE_CAP_TARGET_LINK_SPEED) through the DBI before link up. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Values: 0x1 (SET): Writing '1' to this field instructs the LTSSM to initiate a speed change to Gen2 or Gen3 after the link is initialized at Gen1 speed. 0x0 (CLEAR): Clear Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
16	RW	0x1	AUTO_LANE_FLIP_CTRL_EN Enable Auto flipping of the lanes. You must set the CX_AUTO_LANE_FLIP_CTRL_EN configuration parameter to include the hardware for this feature in the controller. For more details, see the 'Lane Reversal' appendix in the Databook. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x1 Testable: unconstrained
15:13	RW	0x0	PRE_DET_LANE Predetermined Lane for Auto Flip. This field defines which physical lane is connected to logical Lane0 by the flip operation performed in Detect. This field is used to restrict the receiver detect procedure to a particular lane when the default detect and polling procedure performed on all lanes cannot be successful. A notable example of when it is useful to program this field to a value different from the default, is when a lane is asymmetrically broken, that is, it is detected in Detect LTSSM state but it cannot exit Electrical Idle in Polling LTSSM state. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x0 (LANE0): Connect logical Lane0 to physical lane 0 or CX_NL-1 or CX_NL/2-1 or CX_NL/4-1 or CX_NL/8-1, depending on which lane is detected 0x1 (LANE1): Connect logical Lane0 to physical lane 1 0x2 (LANE3): Connect logical Lane0 to physical lane 3 0x3 (LANE7): connect logical lane0 to physical lane 7 0x4 (LANE15): Connect logical Lane0 to physical lane 15 Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
12:8	RW	0x02	NUM_OF_LANES Predetermined Number of Lanes. Defines the number of lanes which are connected and not bad. Used to limit the effective link width to ignore 'broken" or "unused" lanes that detect a receiver. Indicates the number of lanes to check for exit from Electrical Idle in Polling.Active and L2.Idle. It is possible that the LTSSM might detect a receiver on a bad or broken lane during the Detect Substate. However, it is also possible that such a lane might also fail to exit Electrical Idle and therefore prevent a valid link from being configured. This value is referred to as the "Predetermined Number of Lanes" in section 4.2.6.2.1 of the PCI Express Base Specification. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Link Mode Enable" field of PORT_LINK_CTRL_OFF. The value in this register is normally the same as the encoded value in PORT_LINK_CTRL_OFF. If you find that one of your used lanes is bad then you must reduce the value in this register. For more information, see "How to Tie Off Unused Lanes" in the Databook. For information on upsizing and downsizing the link width, see "Link Establishment" in the Databook. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (_1_LANE): 1 lane 0x2 (_2_LANE): 2 lanes 0x3 (_3_LANE): 3 lanes Value After Reset: 0x4 Testable: unconstrained
7:0	RW	0xd2	FAST_TRAINING_SEQ Sets the Number of Fast Training Sequences (N_FTS) that the controller advertises as its N_FTS during Gen2 or Gen3 link training. This value is used to inform the link partner about the PHY's ability to recover synchronization after a low power state. The number should be provided by the PHY vendor. Do not set N_FTS to zero; doing so can cause the LTSSM to go into the recovery state when exiting from L0s. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0xd2

USP_PCIE_PL_PHY_STATUS_OFF
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PHY_STATUS PHY Status. Data received directly from the phy_cfg_status bus. These is a GPIO register reflecting the values on the static phy_cfg_status input signals. The usage is left completely to the user and does not in any way influence controller functionality. You can use it for any static sideband status signalling requirements that you have for your PHY. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true

USP_PCIE_PL_PHY_CONTROL_OFF

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000001	PHY_CONTROL PHY Control. Data sent directly to the cfg_phy_control bus. This is a GPIO register driving the values on the static cfg_phy_control output signals, and does not in any way influence controller functionality. It can be used for any static sideband control signaling requirements that you have for your PHY. Usage of this register and the associated GPIO bus is RESERVED when the controller is connected to a Synopsys PHY. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x1

USP_PCIE_PL_TRGT_MAP_CTRL_OFF

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	TARGET_MAP_INDEX The number of the PF Function on which the Target Values are set. This register does not respect the Byte Enable setting, any write will affect all register bits. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:7	RO	0x000	reserved
6	RW	0x1	TARGET_MAP_ROM Target Value for the ROM page of the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
5:0	RW	0x07	TARGET_MAP_PF Target Values for each BAR on the PF Function selected by the index number. This register does not respect the Byte Enable setting, any write will affect all register bits. Value After Reset: 0x2f Testable: writeAsRead Volatile: true

USP_PCIE_PL_CLOCK_GATING_CTRL_OFF
Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x1	AXI_CLK_GATING_EN AXI Clock Gating Enable. This register enables the AXI Bridge to autonomously enable and disable the AXI Master clock, the AXI Slave clock and the AXI DBI slave clock. The DWC_pcie_clk_rst.v module provides the gated clock, mstr_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, mstr_aclk_active, is asserted. For the AXI Slave this module provides the gated clock, slv_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, slv_aclk_active, is asserted. If the AXI DBI Slave is enabled (DBI_4SLAVE_POPULATED=1) the module provides the gated clock, dbi_axi_aclk_gated, to the AXI Bridge and is enabled when the controllers clock enable signal, dbi_aclk_active, is asserted. The controller de-asserts the clock enable signals when the respective AXI Master/Slave interfaces are idle. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable (default) Value After Reset: 0x1
0	RW	0x1	RADM_CLK_GATING_EN RADM Clock Gating Enable. This register, if set, enables the RADM to autonomously enable and disable its clock. The DWC_pcie_clk_rst.v module provides the gated clock, radm_clk_g, to the RADM and is enabled when the controllers clock enable signal, en_radm_clk_g, is asserted. The RADM clock is a gated version of the controller clock, core_clk. The controller de-asserts en_radm_clk_g when there is no Rx traffic, Rx queues and pre/post-queue pipelines are empty, RADM completion LUT is empty, and there are no FLR actions pending. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable (default) Value After Reset: 0x1

USP_PCIE_PL_GEN3_RELATED_OFF
Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	GEN3_EQ_INVREQ_EVAL_DIFF_DISABLE Eq InvalidRequest and RxEqEval Different Time Assertion Disable. Disable the assertion of Eq InvalidRequest and RxEqEval at different time. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
22:19	RO	0x0	reserved
18	RW	0x0	GEN3_DC_BALANCE_DISABLE DC Balance Disable. Disable DC Balance feature. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0
17	RW	0x0	GEN3_DLLP_XMT_DELAY_DISABLE DLLP Transmission Delay Disable. Disable delay transmission of DLLPs before equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
16	RW	0x0	GEN3_EQUALIZATION_DISABLE Equalization Disable. Disable equalization feature. This bit cannot be changed once the LTSSM starts link training. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	RXEQ_RGRDLESS_RXTS When set to '1', the controller as Gen3 EQ master asserts RxEqEval to instruct the PHY to do Rx adaptation and evaluation after a 500ns timeout from a new preset request. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: Wire: see description Dbi: see description Note: This register field is sticky. Values: 0x0 (ASSERT_1US): mac_phy_rxeqeval asserts after 1us and 2 TS1 received from remote partner. 0x1 (ASSERT_500NS): mac_phy_rxeqeval asserts after 500ns regardless of TS's received or not. Value After Reset: 0x1 Testable: writeAsRead
12	RW	0x0	RXEQ_PH01_EN Rx Equalization Phase 0/Phase 1 Hold Enable. When this bit is set the upstream port holds phase 0 (the downstream port holds phase 1) for 10ms. Holding phase 0 or phase 1 can be used to allow sufficient time for Rx Equalization to be performed by the PHY. This bit is used during Virtex-7 Gen3 equalization. The programmable bits [RXEQ_PH01_EN, EQ_PHASE_2_3] can be used to obtain the following variations of the equalization procedure: Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: Wire: see description Dbi: see description Note: This register field is sticky. Values: 0x0 (TX_EQ_23): Tx equalization only in phase 2/3 0x1 (NO_TX_EQ_NO_RX_EQ): No Tx equalization Value After Reset: 0x0 Testable: writeAsRead

Bit	Attr	Reset Value	Description
11	RW	0x0	EQ_REDO Equalization Redo Disable. Disable autonomous mechanism for requesting to redo the equalization process. The received presets or coefficients mismatch in Recovery.RcvrLock after Recovery EQ phases causes the EQ redo requests. If the EQ redo is infinite or you do not want eq requests and redo, setting this bit to 1 will stop the EQ requests and EQ redo so that the link can go ahead to L0 state for packet trasmissions. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0 Testable: unconstrained
10	RW	0x0	EQ_EIEOS_CNT Equalization EIEOS Count Reset Disable. Disable requesting reset of EIEOS count during equalization. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Values: 0x1 (DISABLE): Disable Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
9	RW	0x0	EQ_PHASE_2_3 Equalization Phase 2 and Phase 3 Disable. This applies to downstream ports only. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: The access attributes of this field are as follows: Wire: see description Dbi: see description Note: This register field is sticky. Values: 0x1 (TX_EQ_23_RX_EQ_PH01): No Rx equalization 0x0 (NO_TX_EQ_RX_EQ_PH01): Rx equalization in phase 0/1 Value After Reset: 0x0 Testable: writeAsRead
8	RW	0x0	DISABLE_SCRAMBLER_GEN_3 Disable Scrambler for Gen3 and Gen4 Data Rate. The Gen3 and Gen4 scrambler/descrambler within the controller needs to be disabled when the scrambling function is implemented outside of the controller (for example within the PHY). Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x0
7:2	RO	0x00	reserved
1	RW	0x0	NO_SEED_VALUE_CHANGE If this bit is set to 1, the seed value of LFSR for scrambler at Gen3 rate does not change after LinkUp = 1. This bit takes effect only when CX_AUTO_LANE_FLIP_CTRL_EN is supported. This feature requires both sides of the link support it. Note: this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky. Values: 0x1 (NO_CHANGE): Not Change Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	GEN3_ZRXDC_NONCOMPL Gen3 Receiver Impedance ZRX-DC Not Compliant. Receivers that operate at 8.0 GT/s with an impedance other than the range defined by the ZRX-DC parameter for 2.5 GT/s (40-60 Ohms) must meet additional behavior requirements in the following LTSSM states: Polling, Rx_L0s, L1, L2, and Disabled. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shared for Gen3 and Gen4/Gen5 data rates. Note: This register field is sticky. Values: 0x0 (RCVR_COMPLIES): The receiver complies with the ZRX-DC parameter for 2.5 GT/s when operating at 8 GT/s or higher. 0x1 (RCVR_NOT_COMPLIES): The receiver does not comply with the ZRX-DC parameter for 2.5 GT/s when operating at 8 GT/s or higher. Value After Reset: 0x1

USP_PCIE_PL_GEN3_EQ_CONTROL_OFF

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x1	GEN3_REQ_SEND_CONSEC_EIEOS_FOR_PSET_MAP Request controller to send back-to-back EIEOS in Recovery.RcvrLock state until presets to coefficients mapping is complete. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky. Values: 0x0 (DO_NOT_REQ): Do not request 0x1 (REQ): Request Value After Reset: 0x1 Testable: writeAsRead Volatile: true
25	RW	0x0	GEN3_EQ_PSET_REQ_AS_COEF GEN3_EQ_PSET_REQ_AS_COEF is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
24	RW	0x0	GEN3_EQ_FOM_INC_INITIAL_EVAL Include Initial FOM. Include or not the FOM feedback from the initial preset evaluation performed in the EQ Master, when finding the highest FOM among all preset evaluations. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (DO_NOT_INCLUDE): Do not include 0x1 (INCLUDE): Include Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:8	RW	0x059f	GEN3_EQ_PSET_REQ_VEC Preset Request Vector. Requesting of Presets during the initial part of the EQ Master Phase. Encoding scheme is as follows: Bit [15:0] =0x0: No preset is requested and evaluated in EQ Master Phase. Bit [i] =1: "Preset=i" is requested and evaluated in EQ Master Phase. 0000000000000000: No preset be requested and evaluated in EQ Master Phase 000000xxxxxxxxx1: Preset 0 is requested and evaluated in EQ Master Phase 000000xxxxxxxx1x: Preset 1 is requested and evaluated in EQ Master Phase 000000xxxxxxx1xx: Preset 2 is requested and evaluated in EQ Master Phase 000000xxxxxx1xxx: Preset 3 is requested and evaluated in EQ Master Phase 000000xxxxx1xxxx: Preset 4 is requested and evaluated in EQ Master Phase 000000xxxx1xxxxx: Preset 5 is requested and evaluated in EQ Master Phase 000000xxx1xxxxxx: Preset 6 is requested and evaluated in EQ Master Phase 000000xx1xxxxxxx: Preset 7 is requested and evaluated in EQ Master Phase 000000x1xxxxxxxx: Preset 8 is requested and evaluated in EQ Master Phase 00000x1xxxxxxxxx: Preset 9 is requested and evaluated in EQ Master Phase 000001xxxxxxxxxx: Preset 10 is requested and evaluated in EQ Master Phase All other encodings: Reserved Note: You must contact your PHY vendor to ensure 24 ms timeout does not occur in presets requests in EQ master phase, that is, you must set a proper value to the GEN3_EQ_PSET_REQ_VEC register so that the EQ tunning for Figure of Merit in the EQ master phase completes before 24 ms timeout. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Value After Reset: 0x59f Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x1	GEN3_LOWER_RATE_EQ_REDO_ENABLE Support EQ redo and lower rate change. Note: Gen3 and Gen4 share the same register bit and have the same feature. Note: This register field is sticky. Values: 0x0 (NO_SUP): Not supported 0x1 (SUP): Supported Value After Reset: 0x1 Testable: writeAsRead Volatile: true
5	RW	0x1	GEN3_EQ_EVAL_2MS_DISABLE Phase2_3 2 ms Timeout Disable. Determine behavior in Phase2 for USP (Phase3 if DSP) when the PHY does not respond within 2ms to the assertion of RxEqEval. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (ABORT_CURRENT_EVA): Abort the current evaluation, stop any attempt to modify the remote transmitter settings, Phase2 is terminated by the 24ms timeout 0x1 (IGNORE_2MS_TIMEOUT): Ignore the 2ms timeout and continue as normal. This is used to support PHYs that require more than 2ms to respond to the assertion of RxEqEval. Value After Reset: 0x1 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
4	RW	0x0	GEN3_EQ_PHASE23_EXIT_MODE Behavior After 24 ms Timeout (when optimal settings are not found). For a USP: Determine next LTSSM state from Phase2 after 24ms Timeout 0: Recovery.Speed 1: Recovery.Equalization.Phase3 When optimal settings are not found then: Equalization Phase 2 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 Equalization Phase 2 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 Equalization Phase 2 Complete status bit is set in the "Link Status Register 2" For a DSP: Determine next LTSSM state from Phase3 after 24ms Timeout 0: Recovery.Speed 1: Recovery.Equalization.RcvrLock When optimal settings are not found then: Equalization Phase 3 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 Equalization Phase 3 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 Equalization Phase 3 Complete status bit is set in the "Link Status Register 2" Note: GEN3_EQ_PHASE23_EXIT_MODE = 1 affects Direction Change feed back mode. EQ requests for Figure Of Merit mode complete before 24 ms timeout. Please see GEN3_EQ_PSET_REQ_VEC Register for more. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (RCVRY_SPEED): Recovery.Speed 0x1 (RCVRY_EQ): USP: Recovery.Equalization.Phase3; DSP: Recovery.Equalization.RcvrLock Value After Reset: 0x1

Bit	Attr	Reset Value	Description
3:0	RW	0x1	GEN3_EQ_FB_MODE Feedback Mode. Other values are reserved. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is a shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (DIR_CHG): Direction Change 0x1 (FOM): Figure Of Merit Value After Reset: 0x1 Testable: writeAsRead Volatile: true

USP_PCIE_PL_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF
Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:14	RW	0x0	GEN3_EQ_FMDC_MAX_POST_CUSROR_DELTA Convergence Window Aperture for C+1. Post-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x0 Testable: unconstrained

Bit	Attr	Reset Value	Description
13:10	RW	0x0	GEN3_EQ_FMDC_MAX_PRE_CUSROR_DELTA Convergence Window Aperture for C-1. Pre-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x0 Testable: unconstrained
9:5	RW	0x02	GEN3_EQ_FMDC_N_EVALS Convergence Window Depth. Number of consecutive evaluations considered in Phase 2/3 when determining if optimal coefficients have been found. Allowed range: 0,1,2,..16 up to a maximum of CX_GEN3_EQ_COEFQ_DEPTH. When set to 0, EQ Master is performed without sending any requests to the remote partner in Phase 2 for USP and Phase 3 for DSP. Therefore, the remote partner will not change its transmitter coefficients and will move to the next state. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x1f (MAX_VAL): Maximum of CX_GEN3_EQ_COEFQ_DEPTH Value After Reset: 0x2 Testable: unconstrained

Bit	Attr	Reset Value	Description
4:0	RW	0x00	GEN3_EQ_FMDC_T_MIN_PHASE23 Minimum Time (in ms) To Remain in EQ Master Phase. The LTSSM stays in EQ Master phase for at least this amount of time, before starting to check for convergence of the coefficients. Allowed values 0,1,...,24. Note: When CX_GEN4_SPEED/CX_GEN5_SPEED, this register is shadow register for Gen3 and Gen4/Gen5 data rate. If RATE_SHADOW_SEL==00b, this register is for Gen3 data rate. If RATE_SHADOW_SEL==01b, this register is for Gen4 data rate. If RATE_SHADOW_SEL==10b, this register is for Gen5 data rate. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x18 (MAX_VAL): Max value Value After Reset: 0x0 Testable: unconstrained

USP_PCIE_PL_ORDER_RULE_CTRL_OFF
Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CPL_PASS_P Completion Passing Posted Ordering Rule Control. Determines if CPL can pass halted P queue. Values: 0x0 (CPL_CAN_NOT_PASS): CPL can not pass P (recommended) 0x1 (CPL_CAN_PASS): CPL can pass P Value After Reset: 0x0
7:0	RW	0x00	NP_PASS_P Non-Posted Passing Posted Ordering Rule Control. Determines if NP can pass halted P queue. Values: 0x0 (NP_CAN_NOT_PASS): NP can not pass P (recommended). 0x1 (NP_CAN_PASS): NP can pass P Value After Reset: 0x0

USP_PCIE_PL_PIPE_LOOPBACK_CONTROL_OFF
Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	PIPE_LOOPBACK PIPE Loopback Enable. Indicates RMMI Loopback if M-PCIe. Note: This register field is sticky. Value After Reset: 0x0
30:27	RO	0x0	reserved
26:24	RW	0x0	RXSTATUS_VALUE RXSTATUS_VALUE is an internally reserved field. Do not use. Value After Reset: 0x0 Testable: writeAsRead Reset Mask: 0x0 Volatile: true
23:22	RO	0x0	reserved
21:16	RW	0x00	RXSTATUS_LANE RXSTATUS_LANE is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
15:0	RW	0x000f	LPBK_RXVALID LPBK_RXVALID is an internally reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0xf

USP_PCIE_PL_MISC_CONTROL_1_OFF
Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	PORT_LOGIC_WR_DISABLE Disable port logic register write from wire side. Note: The access attributes of this field are as follows: Wire: R (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
21	RW	0x0	P2P_ERR_RPT_CTRL Determines whether to enable Peer to Peer (P2P) error reporting. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable P2P error reporting 0x1 (ENABLE): Enable P2P error reporting Value After Reset: 0x0
20	RW	0x0	P2P_TRACK_CPL_TO_REG Determines whether to track completion of transmitted Non-Posted TLPs in P2P mode. Note: This register field is sticky. Values: 0x0 (DO_NOT_TRACk): Do not track completion 0x1 (TRACK): Track completion Value After Reset: 0x0
19:18	RW	0x0	TARGET_ABOVE_CONFIG_LIMIT_REG Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of this field. This field can have the following values: Note: This register field is sticky. Values: 0x1 (ELBI): ELBI 0x2 (TRGT1): TRGT1 Value After Reset: 0x1
17:8	RW	0x37f	CONFIG_LIMIT_REG Configuration requests are directed either to CDM or ELBI/RTRGT1 based on the value of this field. Configuration requests with an address less CONFIG_LIMIT_REG are directed to the CDM Configuration requests with an address greater than CONFIG_LIMIT_REG are directed to either ELBI or TRGT1 interface based on the setting of TARGET_ABOVE_CONFIG_LIMIT_REG field. Your application must set a proper value for this field based on your extended configuration registers. For more details, see the "CDM/ELBI Register Space Access Through CFG Request" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Value After Reset: 0x37f

Bit	Attr	Reset Value	Description
7	RW	0x0	CFG_TLP_BYPASS_EN_REG Setting of this field defines how to decide the destination of Configuration requests. Note: When app_req_retry_en is asserted, the setting of this field is ignored. Note: This register field is sticky. Values: 0x1 (ONE): Configuration TLPs are routed according to the setting of TARGET_ABOVE_CONFIG_LIMIT_REG, regardless the value of CONFIG_LIMIT_REG. 0x0 (ZERO): Configuration TLPs are routed according to the setting of TARGET_ABOVE_CONFIG_LIMIT_REG, depending on the setting of CONFIG_LIMIT_REG. Refer to the definition of CONFIG_LIMIT_REG for details. Value After Reset: 0x0
6	RW	0x1	CPLQ_MNG_EN This field enables the Completion Queue Management feature. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x1
5	RW	0x0	ARI_DEVICE_NUMBER When ARI is enabled, this field enables use of the device ID. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
4	RW	0x0	DISABLE_AUTO_LTR_CLR_MSG Disable the autonomous generation of LTR clear message in upstream port. This field can have the following values: For more details, see "Latency Tolerance Reporting (LTR) Message Generation [EP Mode]" in "Message Generation" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (ALLOW): Allow the autonomous generation of LTR clear message. 0x1 (DISABLE): Disable the autonomous generation of LTR clear message. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
3	RW	0x0	SIMPLIFIED_REPLAY_TIMER Enables Simplified Replay Timer (Gen4). For more details, see "Transmit Replay" in "Transmit TLP Processing" section in the "Controller Operations" chapter of the Databook. Simplified Replay Timer can have the following Values: A value from 24,000 to 31,000 Symbol Times when Extended Synch is 0b. A value from 80,000 to 100,000 Symbol Times when Extended Synch is 1b. The Simplified Replay Timer value must not be changed while the link is in use. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
2	RW	0x0	UR_CA_MASK_4_TRGT1 When this field is set to '1', the controller suppresses error logging, error message generation, and CPL generation for non-posted requests TLPs (with UR filtering status) forwarded to your application (that is, when DEFAULT_TARGET =1). For more details, see "Advanced Error Handling For Received TLPs" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set Value After Reset: 0x0
1	RW	0x0	DEFAULT_TARGET Default target for an IO or MEM request with UR/CA/CRS received. Based on the value of this field the controller either drops or forwards these requests to your application. For more details, see "ECRC Handling" and "Request TLP Routing Rules" in "Receive Routing" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (DROP_IO_MEM_REQ): The controller drops all incoming I/O or MEM requests (after corresponding error reporting). A completion with UR status is generated for non-posted requests. 0x1 (FWD_IO_MEM_UR_CA_CRS): The controller forwards all incoming I/O or MEM requests with UR/CA/CRS status to your application. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	DBI_RO_WR_EN Write to RO Registers Using DBI. For more details, see "Writing to Read-Only Registers" in "Register Module, LBC, and DBI" section in the "Controller Operations" chapter of the Databook. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Your application can write to some RO and HwInit register fields through the DBI when you set this field to '1'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_MULTI_LANE_CONTROL_OFF

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	UPCONFIGURE_SUPPORT Upconfigure Support. The controller sends this value as the Link Upconfigure Capability in TS2 Ordered Sets in Configuration.Complete state. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Note: This register field is sticky. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
6	RW	0x0	DIRECT_LINK_WIDTH_CHANGE Directed Link Width Change. If the upconfigure_capable variable is '1' and the PCIE_CAP_HW_AUTO_WIDTH_DISABLE bit in LINK_CONTROL_LINK_STATUS_REG is '0', the controller starts upconfigure or autonomous width downsizing (to the TARGET_LINK_WIDTH value) in the Configuration state. If TARGET_LINK_WIDTH value is 0x0, the controller does not start upconfigure or autonomous width downsizing in the Configuration state. The controller self-clears this field when the controller accepts this request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (CLEAR): Clear 0x1 (SET): The controller always moves to Configuration state through Recovery state when this bit is set to '1'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
5:0	RW	0x00	TARGET_LINK_WIDTH Target Link Width. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (NOT_START): Controller does not start upconfigure or autonomous width downsizing in the Configuration state. 0x1 (X1): x1 0x2 (X2): x2 0x4 (X4): x4 0x8 (X8): x8 0x10 (X16): x16 0x20 (X32): x32 Value After Reset: 0x0

USP_PCIE_PL_PHY_INTEROP_CTRL_OFF

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17:12	RW	0x1e	PHY_RST_TIMER Decide how many aux clock cycles the PHY reset lasts (0 to 63 aux clock cycles). Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0x3f (MAX_VAL): Max value Value After Reset: 0x1e
11	RO	0x0	reserved
10	RW	0x0	L1_CLK_SEL L1 Clock control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: This register field is sticky. Values: 0x1 (NO_REQ): Controller does not request aux_clk switch and core_clk gating in L1. 0x0 (CAN_REQ): Controller requests aux_clk switch and core_clk gating in L1. Value After Reset: 0x0
9	RW	0x0	L1_NOWAIT_P1 L1 entry control bit. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky. Values: 0x1 (NO_WAIT_FOR_ACK): Controller does not wait for PHY to acknowledge transition to P1 before entering L1. 0x0 (WAIT_FOR_ACK): Controller waits for the PHY to acknowledge transition to P1 before entering L1. Value After Reset: 0x1

Bit	Attr	Reset Value	Description
8	RW	0x0	L1SUB_EXIT_MODE L1 Exit Control Using phy_mac_pclkack_n. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. If PCLK as PHY input is selected, you should not write to this field and change the default value since PCLK as PHY input doesn't support any value other than the default. Note: This register field is sticky. Values: 0x1 (NO_WAIT_FOR_PCLKACK): Controller exits L1 without waiting for the PHY to assert phy_mac_pclkack_n. 0x0 (WAIT_FOR_PCLKACK): Controller waits for the PHY to assert phy_mac_pclkack_n before exiting L1. Value After Reset: 0x0
7	RO	0x0	reserved
6:0	RW	0x44	RXSTANDBY_CONTROL Rxstandby Control. Bits 0..5 determine if the controller asserts the RxStandby signal (mac_phy_rxstandby) in the indicated condition. Bit 6 enables the controller to perform the RxStandby/RxStandbyStatus handshake. This field is reserved for internal use. You should not write to this field and change the default unless specifically instructed by Synopsys support. [0]: Rx EIOS and subsequent T TX-IDLE-MIN [1]: Rate Change [2]: Inactive lane for upconfigure/downconfigure [3]: PowerDown=P1orP2 [4]: RxL0s.Idle [5]: EI Infer in L0 [6]: Execute RxStandby/RxStandbyStatus Handshake Note: This register field is sticky. Value After Reset: 0x44

USP_PCIE_PL_TRGT_CPL_LUT_DELETE_ENTRY_OFF
Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31	RW	0x0	DELETE_EN This is a one-shot bit. This is a self-clearing register field. Reading from this register field always returns a '0'. Values: 0x0 (CLEAR): Clear 0x1 (SET): A '1' write to this bit triggers the deletion of the target completion LUT entry that is specified in the LOOK_UP_ID field. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:0	RW	0x00000000	LOOK_UP_ID This number selects one entry to delete of the TRGT_CPL_LUT. Value After Reset: 0x0

USP_PCIE_PL_LINK_FLUSH_CONTROL_OFF

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	AUTO_FLUSH_EN Enables automatic flushing of pending requests before sending the reset request to the application logic to reset the PCIe controller and the AXI Bridge. The flushing process is initiated if any of the following events occur: Hot reset request. A downstream port (DSP) can "hot reset" an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. Warm (Soft) reset request. Generated when exiting from D3 to D0 and cfg_pm_no_soft_rst=0. Link down reset request. A high to low transition on smlh_req_rst_not indicates the link has gone down and the controller is requesting a reset. If you disable automatic flushing, your application is responsible for resetting the PCIe controller and the AXI Bridge. For more details see "Warm and Hot Resets" section in the Architecture chapter of the Databook. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x1

USP_PCIE_PL_AMBA_ERROR_RESPONSE_DEFAULT_OFF

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:10	RW	0x27	AMBA_ERROR_RESPONSE_MAP AXI Slave Response Error Map. Allows you to selectively map the errors received from the PCIe completion (for non-posted requests) to the AXI slave responses, slv_rresp or slv_bresp. The recommended setting is SLVERR. CRS is always mapped to OKAY. [0] 0: UR (unsupported request) -> DECERR 1: UR (unsupported request) -> SLVERR [1] 0: CRS (configuration retry status) -> DECERR 1: CRS (configuration retry status) -> SLVERR [2] 0: CA (completer abort) -> DECERR 1: CA (completer abort) -> SLVERR [3]: RESERVED (0x0) [4]: RESERVED (0x0) [5] 0: Completion Timeout -> DECERR 1: Completion Timeout -> SLVERR. The AXI bridge internally drops (processes internally but not passed to your application) a completion that has been marked by the Rx filter as UC or MLF, and does not pass its status directly down to the slave interface. It waits for a timeout and then signals "Completion Timeout" to the slave interface. The controller sets the AXI slave read databus to 0xFFFF for all error responses. Note: This register field is sticky. Value After Reset: 0x27
9:5	RO	0x00	reserved
4:3	RW	0x0	AMBA_ERROR_RESPONSE_CRS CRS Slave Error Response Mapping. Determines the AXI slave response for CRS completions. For more details see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky. Values: 0x0 (OK_): OKAY 0x1 (OK_CRS_CMPL): OKAY with all FFFF_FFFF data for all CRS completions 0x2 (OK_READ_REQ): OKAY with FFFF_0001 data for CRS completions to vendor ID read requests, OKAY with FFFF_FFFF data for all other CRS completions 0x3 (SLVERR_DECERR): SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Value After Reset: 0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	AMBA_ERROR_RESPONSE_VENDORID Vendor ID Non-existent Slave Error Response Mapping. Determines the AXI slave response for errors on reads to non-existent Vendor ID register. For more details see "Error Handling" in the AXI chapter of the Databook. Note: This register field is sticky. Values: 0x0 (_OK_): OKAY (with FFFF data). 0x1 (_ERR_): SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Value After Reset: 0x0
1	RO	0x0	reserved
0	RW	0x0	AMBA_ERROR_RESPONSE_GLOBAL Global Slave Error Response Mapping. Determines the AXI slave response for all error scenarios on non-posted requests. For more details see "Error Handling" in the AXI chapter of the Databook. The error response mapping is not applicable to Non-existent Vendor ID register reads. Note: This register field is sticky. Values: 0x0 (OK_): OKAY (with FFFF data for non-posted requests) 0x1 (ERR_): SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Value After Reset: 0x0

USP_PCIE_PL_AMBA_LINK_TIMEOUT_OFF

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	LINK_TIMEOUT_ENABLE_DEFAULT Disable Flush. Note: This register field is sticky. Values: 0x0 (ENABLE): Enable 0x1 (DISABLE): You can disable the flush feature by setting this field to '1'. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x32	LINK_TIMEOUT_PERIOD_DEFAULT Timeout Value (ms). The timer will timeout and then flush the bridge TX request queues after this amount of time. The timer counts when there are pending outbound AXI slave interface requests and the PCIe TX link is not transmitting any of these requests. The timer is clocked by core_clk. Note: This register field is sticky. Value After Reset: 0x32

USP_PCIE_PL_AMBA_ORDERING_CTRL_OFF
Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	AX_MSTR_ZEROLREAD_FW AXI Master Zero Length Read Forward to the application. The DW PCIe controller AXI bridge is able to terminate in order with the Posted transactions the zero length read, implementing the PCIe express flush semantics of the Posted transactions. Values: 0x0 (_0_LN_RD_TERMINATE): The zero length Read is terminated at the DW PCIe AXI bridge master 0x1 (_0_LN_RD_FWD): The zero length Read is forward to the application. Value After Reset: 0x0
6:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:3	RW	0x0	AX_MSTR_ORDR_P_EVENT_SEL AXI Master Posted Ordering Event Selector. This field selects how the master interface determines when a P write is completed when enforcing the PCIe ordering rule, "NP must not pass P" at the AXI Master Interface. The AXI protocol does not support ordering between channels. Therefore, NP reads can pass P on your AXI bus fabric. This can result in an ordering violation when the read overtakes a P that is going to the same address. Therefore, the bridge master does not issue any NP requests until all outstanding P writes reach their destination. It does this by waiting for the all of the write responses on the B channel. This can affect the performance of the master read channel. For scenarios where the interconnect serializes the AXI master "AW", "W" and "AR" channels,you can increase the performance by reducing the need to wait until the complete Posted transaction has effectively reached the application slave. Note: This setting will not affect: MSI interrupt catcher and P data ordering. This is always driven by the B'last event. DMA read engine TLP ordering. This is always driven by the B'last event. NP write transactions which are always serialized with P write transactions. Values: 0x0 (B): B'last event: wait for the all of the write responses on the B channel thereby ensuring that the complete Posted transaction has effectively reached the application slave (default). 0x1 (AW): AW'last event: wait until the complete Posted transaction has left the AXI address channel at the bridge master. 0x2 (W): W'last event: wait until the complete Posted transaction has left the AXI data channel at the bridge master. 0x3 (RSVD): Reserved Value After Reset: 0x0
2	RO	0x0	reserved
1	RW	0x0	AX_SNP_EN AXI Serialize Non-Posted Requests Enable. This field enables the AXI Bridge to serialize same ID Non-Posted Read/Write Requests on the wire. Serialization implies one outstanding same ID NP Read or Write on the wire and used to avoid AXI RAR and WAW hazards at the remote link partner. For more details, see the "Optional Serialization of AXI Slave Non-posted Requests" section in the AXI chapter of the Databook. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0
0	RO	0x0	reserved

USP_PCIE_PL_COHERENCY_CONTROL_1_OFF
Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_LOW_ADDR Boundary Lower Address For Memory Type. Bits [31:0] of dword-aligned address of the boundary for Memory type. The two lower address LSBs are '00'. Addresses up to but not including this value are in the lower address space region; addresses equal or greater than this value are in the upper address space region. Note: This register field is sticky. Value After Reset: 0x0
1	RO	0x0	reserved
0	RW	0x0	CFG_MEMTYPE_VALUE Sets the memory type for the lower and upper parts of the address space: Note: This register field is sticky. Values: 0x0 (LOWER_PREPH): lower = Peripheral; upper = Memory 0x1 (LOWER_MEM): lower = Memory type; upper = Peripheral Value After Reset: 0x

USP_PCIE_PL_COHERENCY_CONTROL_2_OFF
Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_HIGH_ADDR Boundary Upper Address For Memory Type. Bits [63:32] of the 64-bit dword-aligned address of the boundary for Memory type. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_COHERENCY_CONTROL_3_OFF
Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	CFG_MSTR_AWCACHE_VALUE Master Write CACHE Signal Value. Value of the individual bits in mstr_awcache when CFG_MSTR_AWCACHE_MODE is '1'. Note: Not applicable to message requests; for message requests the value of mstr_awcache is always '0000'. Note: This register field is sticky. Value After Reset: 0x0
26:23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:19	RW	0x0	CFG_MSTR_ARCACHE_VALUE Master Read CACHE Signal Value. Value of the individual bits in mstr_arcache when CFG_MSTR_ARCACHE_MODE is '1'. Note: This register field is sticky. Value After Reset: 0x0
18:15	RO	0x0	reserved
14:11	RW	0x0	CFG_MSTR_AWCACHE_MODE Master Write CACHE Signal Behavior. Defines how the individual bits in mstr_awcache are controlled. Note: for message requests the value of mstr_awcache is always "0000" regardless of the value of this bit. Note: This register field is sticky. Values: 0x0 (SET_BY_AXI_MASTER): set automatically by the AXI master 0x1 (SET_BY_FIELD): set by the value of the corresponding bit of the CFG_MSTR_AWCACHE_VALUE field Value After Reset: 0x0
10:7	RO	0x0	reserved
6:3	RW	0x0	CFG_MSTR_ARCACHE_MODE Master Read CACHE Signal Behavior. Defines how the individual bits in mstr_arcache are controlled. Note: This register field is sticky. Values: 0x0 (SET_BY_AXI_MASTER): set automatically by the AXI master 0x1 (SET_BY_FIELD): set by the value of the corresponding bit of the CFG_MSTR_ARCACHE_VALUE field Value After Reset: 0x0
2:0	RO	0x0	reserved

USP_PCIE_PL_AXI_MSTR_MSG_ADDR_LOW_OFF

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	CFG_AXIMSTR_MSG_ADDR_LOW Lower 20-bits of the programmable AXI address for Messages. Note: This register field is sticky. Value After Reset: 0x0
11:0	RO	0x000	CFG_AXIMSTR_MSG_ADDR_LOW_RESERVED Reserved for future use. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_AXI_MSTR_MSG_ADDR_HIGH_OFF
Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_AXIMSTR_MSG_ADDR_HIGH Upper 32 bits of the programmable AXI address for Messages. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_PCIE_VERSION_NUMBER_OFF
Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3536302a	VERSION_NUMBER Version Number. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x3536302a

USP_PCIE_PL_PCIE_VERSION_TYPE_OFF
Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x6c703035	VERSION_TYPE Version Type. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x6c703035

USP_PCIE_PL_MSIX_ADDRESS_MATCH_LOW_OFF
Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	MSIX_ADDRESS_MATCH_LOW MSI-X Address Match Low Address. Note: This register field is sticky. Value After Reset: 0x0
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	MSIX_ADDRESS_MATCH_EN MSI-X Match Enable. Enable the MSI-X Address Match feature when the AXI bridge is present. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable Value After Reset: 0x0

USP_PCIE_PL_MSIX_ADDRESS_MATCH_HIGH_OFF
Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSIX_ADDRESS_MATCH_HIGH MSI-X Address Match High Address. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Zero value 0xffffffff (MAX_VAL): Max value Value After Reset: 0x0

USP_PCIE_PL_MSIX_DOORBELL_OFF
Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	WO	0x00	MSIX_DOORBELL_PF MSIX Doorbell Physical Function. This register determines the Physical Function for the MSI-X transaction. Value After Reset: 0x0
23:16	WO	0x00	MSIX_DOORBELL_VF MSIX Doorbell Virtual Function. This register determines the Virtual Function for the MSI-X transaction. Value After Reset: 0x0
15	WO	0x0	MSIX_DOORBELL_VF_ACTIVE MSIX Doorbell Virtual Function Active. This register determines whether a Virtual Function is used to generate the MSI-X transaction. Value After Reset: 0x0
14:12	WO	0x0	MSIX_DOORBELL_TC MSIX Doorbell Traffic Class. This register determines which traffic class to generate the MSI-X transaction with. Value After Reset: 0x0
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	WO	0x000	MSIX_DOORBELL_VECTOR MSI-X Doorbell Vector. This register determines which vector to generate the MSI-X transaction for. Value After Reset: 0x0

USP_PCIE_PL_MSIX_RAM_CTRL_OFF

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	MSIX_RAM_CTRL_DBG_PBA MSIX PBA RAM Debug Mode. You can also use the dbg_pba input to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable. Use this bit to activate the debug mode and allow direct read/write access to the PBA. Value After Reset: 0x0
24	RW	0x0	MSIX_RAM_CTRL_DBG_TABLE MSIX Table RAM Debug Mode. You can also use the dbg_table input to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. Note: This register field is sticky. Values: 0x0 (DISABLE): Disable 0x1 (ENABLE): Enable. Use this bit to activate the debug mode and allow direct read/write access to the Table. Value After Reset: 0x0
23:17	RO	0x00	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	MSIX_RAM_CTRL_BYPASS MSIX RAM Control Bypass. It is up to the application to ensure the RAMs are in the proper power state before trying to access them. Moreover, the application needs to observe all timing requirements of the RAM low power signals before trying to use the MSIX functionality. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): The bypass field, when set, disables the internal generation of low power signals for both RAMs. Value After Reset: 0x0
15:10	RO	0x00	reserved
9	RW	0x0	MSIX_RAM_CTRL_PBA_SD MSIX PBA RAM Shut Down. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_pba_sd output to signal your external logic to place the MSIX PBA RAM in Shut Down low-power mode. Value After Reset: 0x0
8	RW	0x0	MSIX_RAM_CTRL_PBA_DS MSIX PBA RAM Deep Sleep. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_pba_ds output to signal your external logic to place the MSIX PBA RAM in Deep Sleep low-power mode. Value After Reset: 0x0
7:2	RO	0x00	reserved
1	RW	0x0	MSIX_RAM_CTRL_TABLE_SD MSIX Table RAM Shut Down. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_table_sd output to signal your external logic to place the MSIX Table RAM in Shut Down low-power mode. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	MSIX_RAM_CTRL_TABLE_DS MSIX Table RAM Deep Sleep. Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): Set this bit to drive the cfg_msix_table_ds output to signal your external logic to place the MSIX Table RAM in Deep Sleep low-power mode. Value After Reset: 0x0

USP_PCIE_PL_DTIM_CTRL0_OFF

Address: Operational Base + offset (0x03B0)

Bit	Attr	Reset Value	Description
31	RW	0x0	DTIM_CTRL0_IREQ_SW_FLUSH_EN Invalidate Request Software Flush Enable. If set enables software to flush pending DTI-ATS invalidate requests from the invalidate request queue. Software forces the flush by writing to the DTIM_CTRL1.INV_REQ_FLUSH_SID register. The flushing mechansim enables software to remove invalidate requests from the request queue in response to a UR from an Endpoint function. Prior to removing unsupported invalidate requests software should disable the hardware invalidate request timer (DTIM_CTRL0.IREQ_TMR_EN=0). To continue monitoring outstanding invalidate requests enable the timer once again. The timer restarts from its programmed timeout value (DTIM_CTRL5.IREQ_TMR_TRGT_TO). Note: Software initiated flushing does not result in a sync or timeout error. Note: This register field is sticky. Value After Reset: 0x0
30	RW	0x0	DTIM_CTRL0_IREQ_TMR_EN Invalidate Request Timer Enable. If set enables the DTIM to flush timed out DTI-ATS invalidate requests from the invalidate request queue. The invalidate request timer times each invalidation request sent on the wire. If disabled the responsibilty to flush the request is passed to software. Software writes to the DTIM_CTRL1.INV_REQ_FLUSH_SID register field to flush all pending requests associated with the particular Stream ID (SID). Subsequent received PCIe invalidate completions, associated with the particular SID, are treated as unexpected completions (completion received but no request pending). Timed out invalidate requests result in a sync error response to an outstanding sync request. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
29	RW	0x0	DTIM_CTRL0_IREQ_BYTE_ORDER Invalidate Request Byte Order. In normal operation PCIe data bytes are transmitted in little endian format, that is, PCIe data byte 0 is the first byte transmitted on the wire. The format of the DTI-ATS untranslated address and the PCIe untranslated address embedded in the two DWORD data field of the invalidate request message is defined in big endian format, that is, PCIe byte 0 contains the most significant byte of the address, byte 7. To align the DTI-ATS data byte order to PCIe data byte order the bytes are reversed. To be robust against misinterpretation of the byte order software can reverse the bytes by setting this bit. Note: This register field is sticky. Values: 0x0 (LITTLE_ENDIAN): DTI-ATS Invalidate Request data bytes are transmitted in little endian format. 0x1 (BIG_ENDIAN): DTI-ATS Invalidate Request data bytes are transmitted in big endian format. Value After Reset: 0x0
28	RW	0x0	DTIM_CTRL0_TRESP_BYTE_ORDER Translation Response Byte Order. In normal operation PCIe data bytes are transmitted in little endian format, that is, PCIe data byte 0 is the first byte transmitted on the wire. The format of the DTI-ATS translated address and the PCIe translated address embedded in the two DWORD data field of the translation completion is defined in big endian format, that is, PCIe byte 0 contains the most significant byte of the address, byte 7. To align the DTI-ATS data byte order to PCIe data byte order the bytes are reversed. To be robust against misinterpretation of the byte order software can reverse the bytes by setting this bit. Note: This register field is sticky. Values: 0x0 (LITTLE_ENDIAN): DTI-ATS Translation Response data bytes are transmitted in little endian format. 0x1 (BIG_ENDIAN): DTI-ATS Translation Response data bytes are transmitted in big endian format. Value After Reset: 0x0
27:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x1f	DTIM_CTRL0_TOK_TRANS_REQ Number of Translation Request Tokens Requested. Its default value is configured by the visible parameter, CC_DTIM_NUM_TRANS_TOKENS_REQUESTED. Software can overide this value at initialization time. The number of tokens requested is equal to TOK_TRANS_REQ + 1 (1 to 256). Note: This register field is sticky. Value After Reset: 0x1f
15:0	RW	0xffff	DTIM_CTRL0_ROOT_PORT_ID Root Port ID. Its default value is configured by the visible parameter, CC_ROOT_PORT_ID. Software can overide this value at initialization time. Note: This register field is sticky. Value After Reset: 0xffff

USP_PCIE_PL_DTIM_CTRL1_OFF

Address: Operational Base + offset (0x03B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	DTIM_CTRL1_FLUSH_IREQ_GLOB Flush Invalidate Requests Global. Flushes all outstanding DTI-ATS invalidate requests. The flush is triggered when a 32-bit write to the DTIM_CTRL1 register is performed and FLUSH_IREQ_GLOB =1. Forcing the errored sync ack avoids deadlocking the SMMU in scenarios where the Endpoint function fails to complete the outstanding invalidate requests. In normal operation invalidate requests are flushed by hardware when the per Stream ID invalidate request timer expires. This field is primarily a test feature enabling software to force the sync ack to a pending sync request without having to wait for hardware to time out and flush all prior invalidate requests. Flushing outstanding DTI-ATS invalidate requests does not result in a timeout or a sync error (sync ack with its ERROR =1) if a sync request is outstanding. PCIe invalidate completions received after the flush sequence is complete are discarded and treated as unexpected completions (completion received but no request pending). If enabled, software is notified if unexpected completions are received. This field is valid if DTIM_CTRL0.FLUSH_CTRL_SW_EN is set. Note: This register field is sticky. Value After Reset: 0x0
30:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	DTIM_CTRL1_FLUSH_IREQ_SID Flush Invalidate Request Stream ID. Flushes all pending DTI-ATS invalidate requests, associated with a particuar Stream ID (SID/BDF), from the invalidate request queue. The flush is triggered when a 32-bit write to the DTIM_CTRL1 register is performed and FLUSH_IREQ_GLOB=0. FLUSH_IREQ_SID specifies the flushed Stream ID. This flushing mechanism enables software to remove invalidate requests from the request queue in response to a ERR_NONFATAL message from an Endpoint function. Software flushing of invalidate requests prior to a hardware invalidate request timeout does not result in a timeout error or a sync error (sync ack with its ERROR=1) if a sync request is outstanding. PCIe invalidate completions received with the flushed Stream ID are discarded and treated as unexpected completions (completion received but no request pending). If enabled, software is notified if unexpected completions are received. This field is valid if DTIM_CTRL0.FLUSH_CTRL_SW_EN is set. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_CTRL2_OFF

Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	DTIM_CTRL2_CONDIS_REQ Connect/Disconnect Request. Software initiates disconnection of the DTI-ATS interface when all ATC's have been invalidated and disabled and all outststanding page/translation requests have completed. The "Request Connect" and "Force Acknowledge" commands are used for debug purposes only. Note: This register field is sticky. Values: 0x0 (NOT_CARE): Don't care 0x1 (REQ_DISCONNECT): Request Disconnect 0x2 (REQ_CONNECT): Request Connect 0x3 (FORCE_ACK): Force Acknowledge Value After Reset: 0x0

USP_PCIE_PL_DTIM_CTRL3_OFF

Address: Operational Base + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x4	DTIM_CTRL3_TREQ_WEIGHT AXI4 Master #0 Translation Request Priority Weighting. This value sets the priority of the DTI-ATS translation request messages being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x4
11	RO	0x0	reserved
10:8	RW	0x2	DTIM_CTRL3_PREQ_WEIGHT AXI4 Master #0 Page Request Priority Weighting. This value sets the priority of the DTI-ATS page request messages being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x2
7	RO	0x0	reserved
6:4	RW	0x1	DTIM_CTRL3_SREQ_WEIGHT DTI-ATS Sync Request Priority Weighting. This value sets the priority of the DTI-ATS sync acknowledge message being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x1
3	RO	0x0	reserved
2:0	RW	0x0	DTIM_CTRL3_IACK_WEIGHT DTI-ATS Invalidation Ack Priority Weighting. This value sets the priority of the DTI-ATS invalidate acknowledge message being transmitted from the DTI Master to the DTI Slave. The higher the value the lower the priority. If the priority value is the same as other requests being transmitted from the DTI Master to the DTI Slave then the" fairness among equals" arbitration scheme applies when requests are valid in the same cycle. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_CTRL4_OFF
Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	DTIM_CTRL4_TREQ_QOS_VC0 Translation Request Quality of Service Level VC0. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_CTRL5_OFF
Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DTIM_CTRL5_IREQ_TMR_TRGT_TO Invalidate Request Timeout Value (msec). The target timeout value is set to IREQ_TRGT_TO + 1. For example, programming this field to 15 sets the target timeout value to 16msec. The minimum target timeout value is 2msec. That is, IREQ_TRGT_TO must be greater than 0. The maximum target timeout value is 65536 msec. The target timeout value is the guaranteed minimum timeout value and must be set to an even number of msec. The timeout range is set at the target timeout value -0%, +50%. For example, if the target timeout value is set to 16msec then the timeout range is set at 16msec to 24msec. - This field is valid if DTIM_CTRL0.IREQ_TMR_EN is set. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_INT_STATUS_OFF
Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	DTIM_INT_STATUS_ERR_TRESP_OAS Translation Response Output Address Size Mismatch Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected a DTI-ATS translation response output address size mismatch error. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_TRESP_OAS_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
8	RO	0x0	DTIM_INT_STATUS_ERR_TRESP_UID Translation Response Unexpected ID Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected an unexpected DTI-ATS translation response. The translation response translation ID can not be associated with an outstanding DTI-ATS translation request. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_TRESP_UID_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:5	RO	0x0	reserved
4	RO	0x0	DTIM_INT_STATUS_ERR_ICPL_UC Invalidate Completion Unexpected Completion Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected an unexpected PCIe invalidate completion error. The PCIe invalidate completion tag can not be associated with an outstanding DTI-ATS invalidate request. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_ICPL_UC_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved
1	RO	0x0	DTIM_INT_STATUS_ERR_IREQ_OPERTN Invalidate Request Operation Code Error. Indicates that the Distributed Translation Interface Master (DTIM) has detected an illegal DTI-ATS invalidate request operation code. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_OPERTN_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RO	0x0	DTIM_INT_STATUS_ERR_IREQ_TO Invalidate Request Timeout Error. Indicates that the Distributed Translation Interface Master (DTIM) has timed out one or more DTI-ATS invalidate requests. The Endpoint Translation Cache (ATC) has not returned one or more invalidate completions within an expected timeframe. The outstanding invalidate completion(s) are not expected to be received at this point in time. This is a level interrupt. It is set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_TO_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_DTIM_INT_EN_OFF

Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	DTIM_INT_EN_ERR_TRESP_OAS_INT_EN Translation Response Output Address Size Mismatch Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	DTIM_INT_EN_ERR_TRESP_UID_INT_EN Translation Response Unexpected ID Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0
7:5	RO	0x0	reserved
4	RW	0x0	DTIM_INT_EN_ERR_ICPL_UC_INT_EN Invalidate Completion Unexpected Completion Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0
3:2	RO	0x0	reserved
1	RW	0x0	DTIM_INT_EN_ERR_IREQ_OPERTN_INT_EN Invalidate Request Operation Code Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	DTIM_INT_EN_ERR_IREQ_TO_INT_EN Invalidate Request Timeout Error Interrupt Enable. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_INT_CLR_OFF
Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	WO	0x0	DTIM_INT_CLR_ERR_TRESP_OAS_INT_CLR Translation Response Output Address Size Mismatch Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_TRESP_OAS. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
8	WO	0x0	DTIM_INT_CLR_ERR_TRESP_UID_INT_CLR Translation Response Unexpected ID Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_TRESP_UID. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:5	RO	0x0	reserved
4	WO	0x0	DTIM_INT_CLR_ERR_ICPL_UC_INT_CLR Invalidate Completion Unexpected Completion Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_ICPL_UC. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved
1	WO	0x0	DTIM_INT_CLR_ERR_IREQ_OPERTN_INT_CLR Invalidate Request Operation Code Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_IREQ_OPERTN. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	WO	0x0	DTIM_INT_CLR_ERR_IREQ_TO_INT_CLR Invalidate Request Timeout Error Interrupt Clear. A write to this register automatically clears the interrupt status bit, DTIM_INT_STATUS.ERR_IREQ_TO. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_DTIM_INT_MSK_OFF
Address: Operational Base + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	DTIM_INT_MSK_ERR_TRESP_OAS_INT_MSK Translation Response Output Address Size Mismatch Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	DTIM_INT_MSK_ERR_TRESP_UID_INT_MSK Translation Response Unexpected ID Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
7:5	RO	0x0	reserved
4	RW	0x0	DTIM_INT_MSK_ERR_ICPL_UC_INT_MSK Invalidate Completion Unexpected Completion Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
3:2	RO	0x0	reserved
1	RW	0x0	DTIM_INT_MSK_ERR_IREQ_OPERTN_INT_MSK Invalidate Request Operation Code Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0
0	RW	0x0	DTIM_INT_MSK_ERR_IREQ_TO_INT_MSK Invalidate Request Timeout Error Interrupt Mask. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_MSI_ADDR_UPR_OFF
Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DTIM_MSI_ADDR_UPR_MSI_ADDR MSI Target Address [63:32]. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_MSI_ADDR_LWR_OFF
Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	DTIM_MSI_ADDR_LWR_MSI_ADDR MSI Data. Note: This register field is sticky. Value After Reset: 0x0
1:0	RO	0x0	reserved

USP_PCIE_PL_DTIM_MSI_DATA_OFF
Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DTIM_MSI_DATA_MSI_DATA MSI Data. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_PL_DTIM_ERR_LOG0_OFF
Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DTIM_ERR_LOG0_ERR_IREQ_OPCODE Invalidate Request Illegal Op Code. This field contains the DTI-ATS Invalidate Request "Operation" field and is set when an illegal invalidate request opcode is detected by the DTI Master. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_OPERTN_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RO	0x00	DTIM_ERR_LOG0_ERR_IREQ_TO_ITAG Invalidate Request Timeout ITAG. This field contains the itag associated with the first timed out DTI-ATS invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_TO_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:0	RO	0x0000	DTIM_ERR_LOG0_ERR_IREQ_TO_SID_LWR Invalidate Request Timeout Target SID/BDF. This field contains the target Stream/Device ID associated with the first timed out DTI-ATS invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_IREQ_TO_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_DTIM_ERR_LOG1_OFF
Address: Operational Base + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RO	0x00	DTIM_ERR_LOG1_ERR_ICPL_UC_ITAG Unexpected Invalidate Completion ITAG. This field contains the PCIe invalidate completion itag associated with the first unexpected completion. A completion is unexpected if a completion is received from the Endpoint with a corresponding outstanding PCIe invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_ICPL_UC_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	DTIM_ERR_LOG1_ERR_ICPL_UC_REQ_ID Unexpected Invalidate Completion Requester ID. This field contains the PCIe invalidate completion Requester ID associated with the first unexpected completion. A completion is unexpected if a completion is received from the Endpoint with a corresponding outstanding PCIe invalidate request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_ICPL_UC_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_DTIM_ERR_LOG2_OFF
Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	DTIM_ERR_LOG2_ERR_TRESP_UR_TID Unexpected Translation Response ID. This field contains the DTI-ATS translation response translation ID associated with the first unexpeted translation response. A translation response is unexpected when a response is received without a corresponding outstanding translation request. These bits are set by hardware and cleared by software (DTIM_INT_CLR.ERR_TRESP_UID_INT_CLR=1) Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_DTIM_DIAG_OFF
Address: Operational Base + offset (0x03FC)

Bit	Attr	Reset Value	Description
31	RO	0x0	DTIM_DIAG_SUP_PRI Indicates of DTI-ATS Page Request/Responses are supported by the SMMU. The field corresponds to the SUP_PRI field of the DTI_ATS_CONDIS_ACK message. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:25	RO	0x00	reserved

Bit	Attr	Reset Value	Description
24	RO	0x0	DTIM_DIAG_VERSION Acknowledged DTI-ATS Protocol Version. The field corresponds to the VERSION field of the DTI_ATS_CONDIS_ACK message. 0000: DTI-ATSv1 Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23:20	RO	0x0	DTIM_DIAG_OAS Maximum address size permitted for translated addresses. The field corresponds to the OAS field of the DTI_ATS_CONDIS_ACK message. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
19:16	RO	0x0	reserved
15:8	RO	0x00	DTIM_DIAG_TOK_TREQ_GNT This field indicates the number of pre-allocated tokens for translation requests that have been granted by the SMMU. The number of translation tokens granted is equal to the value of this field plus one. The field corresponds to the TOK_TRANS_GNT field of the DTI_ATS_CONDIS_ACK message. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RO	0x0	DTIM_DIAG_IREQ_FLUSH_SID_LWR_Q_EMPTY Invalidation Request Flush SID Lower Queue Empty Flag. If set, this bit indicates that all outstanding invalidate requests associated with the flushed Endpoint function, DTIM_CTRL1.IREQ_FLUSH_SID_LWR, have been flushed from the invalidate request queue. The flag is set when the software initiated flush sequence completes. If subsequent in-flight invalidate requests are received post the flush sequence then this flag will be cleared. Further flushing of the invalidate request queue is required in this case. Note: It is expected the SMMU stops sending invalidate requests to the DTIM prior to triggering the flush sequence. At some point all in-flight invalidate requests associated with the Endpoint function will be flushed. Value After Reset: 0x1 Testable: writeAsRead Volatile: true
5	RO	0x0	DTIM_DIAG_IREQ_FLUSH_DONE Invalidate Request Flush Done. Invalidate Request Flush Done. If set this bit indicates that the software initiated invalidate request queue flush sequence has completed. The flag is initially cleared by hardware when the flush sequence is initially triggerred by a write to the DTIM_CTRL1 register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	RO	0x1	DTIM_DIAG_IREQ_ORDRQ_EMPTY Invalidation Request Order Q Empty Flag. If set this bit indicates the DTI-ATS invalidate request queue is empty, that is, all invalidate requests have received a completion or invalidate request have not be sent to the DTIM or sent to the DTIM but discarded (broadcast DTI-ATS invalidate requests). Value After Reset: 0x1 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RO	0x0	DTIM_DIAG_CONDIS_STATE Connect/Disconnect FSM state. The field corresponds to the current state of the Connect/Disconnect FSM. The following encoding applies: Other value are reserved. Values: 0x0 (DISCONNECTED): DISCONNECTED 0x1 (REQ_CONNECT): REQ_CONNECT 0x2 (CONNECTED): CONNECTED 0x3 (REQ_DISCONNECT): REQ_DISCONNED Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_PL_APP_BUS_DEV_NUM_STATUS_OFF

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	RC_DSW_BUS_NUM This field reflects the value of bus number driven on app_bus_num input signal by your application. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7:3	RO	0x00	RC_DSW_DEV_NUM This field reflects the value of device number driven on app_device_num input signal by your application. Note: This register field is sticky. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2:0	RO	0x0	reserved

USP_PCIE_PL_PCIPM_TRAFFIC_CTRL_OFF

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	PCIPM_NEW_TLP_CLIENT2_BLOCKED This field indicates that all TLPs transmitted by Client 2 interface are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x0
2	RW	0x0	PCIPM_NEW_TLP_CLIENT1_BLOCKED This field indicates that all TLPs transmitted by Client 1 interface are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x0
1	RW	0x0	PCIPM_NEW_TLP_CLIENT0_BLOCKED This field indicates that all TLPs transmitted by Client 0 interface are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x0
0	RW	0x0	PCIPM_VDM_TRAFFIC_BLOCKED This field indicates that VDM Message TLPs are blocked during non-D0 states. Note: This register field is sticky. Value After Reset: 0x

USP_PCIE_PL_PL_LTR_LATENCY_OFF

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31	RW	0x0	NO_SNOOP_LATENCY_REQUIRE No Snoop Latency Requirement. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W Value After Reset: 0x0
30:29	RO	0x0	reserved
28:26	RW	0x0	NO_SNOOP_LATENCY_SCALE No Snoop Latency Scale. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
25:16	RW	0x000	NO_SNOOP_LATENCY_VALUE No Snoop Latency Value. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W Value After Reset: 0x0
15	RW	0x0	SNOOP_LATENCY_REQUIRE Snoop Latency Requirement. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W Value After Reset: 0x0
14:13	RO	0x0	reserved
12:10	RW	0x0	SNOOP_LATENCY_SCALE Snoop Latency Scale. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W Value After Reset: 0x0
9:0	RW	0x000	SNOOP_LATENCY_VALUE Snoop Latency Value. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W Value After Reset: 0x0

USP_PCIE_PL_AUX_CLK_FREQ_OFF

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x018	AUX_CLK_FREQ The aux_clk frequency in MHz. This value is used to provide a 1 us reference for counting time during low-power states with aux_clk when the PHY has removed the pipe_clk. Frequencies lower than 1 MHz are possible but with a loss of accuracy in the time counted. If the actual frequency (f) of aux_clk does not exactly match the programmed frequency (f_prog), then there is an error in the time counted by the controller that can be expressed in percentage as: err% = (f_prog/f-1)*100. For example if f=2.5 MHz and f_prog=3 MHz, then err% =(3/2.5-1)*100 =20%, meaning that the time counted by the controller on aux_clk will be 20% greater than the time in us programmed in the corresponding time register (for example T_POWER_ON). Note: This register field is sticky. Value After Reset: 0x18

USP_PCIE_PL_L1_SUBSTATES_OFF
Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	L1SUB_LOW_POWER_CLOCK_SWITCH_MODE If the bit is set to 1'b1 the controller will delay the switching of aux_clk to the slow platform clock until it detects that the link partner has de-asserted CLKREQ#. Note: This register field is sticky. Values: 0x0 (CLEAR): The reference clock may be gated off when CLKREQ# is de-asserted. 0x1 (SET): The reference clock shall be kept running regardless of the CLKREQ# setting. Value After Reset: 0x0
7:6	RW	0x3	L1SUB_T_PCLKACK Max delay (in 1us units) between a MAC request to remove the clock on mac_phy_pclkreq_n and a PHY response on phy_mac_pclkack_n. If the PHY does not respond within this time the request is aborted. Range is 1..4 Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x3 (MAX_VAL): Max value Value After Reset: 0x3

Bit	Attr	Reset Value	Description
5:2	RW	0x4	L1SUB_T_L1_2 Duration (in 1us units) of L1.2. Range is 1..16. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0xf (MAX_VAL): Max value Value After Reset: 0x4
1:0	RW	0x2	L1SUB_T_POWER_OFF Duration (in 1us units) of L1.2.Entry. Range is 1..4. Note: This register field is sticky. Values: 0x0 (MIN_VAL): Min value 0x3 (MAX_VAL): Max value Value After Reset: 0x2

USP_PCIE_PL_POWERDOWN_CTRL_STATUS_OFF

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	POWERDOWN_PHY_POWERDOWN This field represents the Powerdown value that has been acknowledged by the PHY. It is updated with the value of Powerdown driven by the controller, when the PHY has returned the Phystatus acknowledgment for the Powerdown transition. Value After Reset: 0x2 Testable: writeAsRead Volatile: true
7:4	RW	0x2	POWERDOWN_MAC_POWERDOWN This field represents the Powerdown value driven by the controller to the PHY. Value After Reset: 0x2 Testable: writeAsRead Volatile: true
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	POWERDOWN_VMAIN_ACK Set this bit to 1 if you do not want to perform the handshake with the power-switch after PERST# assertion. By default the controller will perform the handshake with the power-switch if L1 power gating is enabled Note: This register field is sticky. Values: 0x0 (CLEAR): Clear 0x1 (SET): If you do not want to perform the handshake with the power-switch after PERST# assertion. Value After Reset: 0x0
0	WO	0x0	POWERDOWN_FORCE This field is a one shot field. This field could be used for debug purposes in event that the P2 Powerdown transition does not complete. It will allow the controller to proceed with the transition to the P1 Powerdown state. This field always reads back as 1'b0. Values: 0x0 (CLEAR): Clear 0x1 (SET): Writing a value of 1 to this field causes the controller to complete the P2 Powerdown handshake regardless of whether the PHY has returned Phystatus. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_PL_PIPE_RELATED_OFF
Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	PIPE_GARBAGE_DATA_MODE PIPE Garbage Data Mode. RxValid is deasserted a valid RxStartBlock is received at 128b/130b encoding a valid COM symbol is received at 8b/10b encoding Note: This register field is sticky. Values: 0x0 (COMPLIANT_MODE): PIPE Spec compliant mode: The MAC discards any symbols received after the electrical idle ordered-set until RxValid is deasserted. 0x1 (PHY_SUP_MODE): Special PHY Support mode: The MAC discards any symbols received after the electrical idle ordered-set until when any of the following three conditions are true: Value After Reset: 0x0
7:0	RO	0x00	reserved

11.4.4.33 USP_TYPE0_HDR_DBI2 Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_TYPE0_HDR_DBI2_BAR0_MASK_REG	0x0010	W	0xFFFFFFFF	BAR0 Mask Register
USP_PCIE_TYPE0_HDR_DBI2_BAR1_MASK_REG	0x0014	W	0xFFFFFFFF	BAR1 Mask Register
USP_PCIE_TYPE0_HDR_DBI2_BAR2_MASK_REG	0x0018	W	0xFFFFFFFF	BAR2 Mask Register
USP_PCIE_TYPE0_HDR_DBI2_BAR3_MASK_REG	0x001C	W	0xFFFFFFFF	BAR3 Mask Register
USP_PCIE_TYPE0_HDR_DBI2_BAR4_MASK_REG	0x0020	W	0xFFFFFFFF	BAR4 Mask Register
USP_PCIE_TYPE0_HDR_DBI2_BAR5_MASK_REG	0x0024	W	0xFFFFFFFF	BAR5 Mask Register
USP_PCIE_TYPE0_HDR_DBI2_EXP_ROM_BAR_MASK_REG	0x0030	W	0x0001FFFF	Expansion ROM BAR Mask Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.34 USP_TYPE0_HDR_DBI2 Detail Registers Description

USP_PCIE_TYPE0_HDR_DBI2_BAR0_MASK_REG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	WO	0x7fffffff	PCI_TYPE0_BAR0_MASK BAR0 Mask. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: W (sticky) Note: This register field is sticky. Value After Reset: 0x7fffffff Testable: untestable
0	WO	0x1	PCI_TYPE0_BAR0_ENABLED BAR0 Mask Enabled. Note: This register field is sticky. Value After Reset: 0x1 Testable: untestable

USP_PCIE_TYPE0_HDR_DBI2_BAR1_MASK_REG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	WO	0x7fffffff	PCI_TYPE0_BAR1_MASK BAR1 Mask. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: W (sticky) Note: This register field is sticky. Value After Reset: 0x7fffffff Testable: untestable
0	WO	0x1	PCI_TYPE0_BAR1_ENABLED BAR1 Mask Enabled. Note: This register field is sticky. Value After Reset: 0x1 Testable: untestable

USP_PCIE_TYPE0_HDR_DBI2_BAR2_MASK_REG
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	WO	0x7fffffff	PCI_TYPE0_BAR2_MASK BAR2 Mask. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: W (sticky) Note: This register field is sticky. Value After Reset: 0x7fffffff Testable: untestable
0	WO	0x1	PCI_TYPE0_BAR2_ENABLED BAR2 Mask Enabled. Note: This register field is sticky. Value After Reset: 0x1 Testable: untestable

USP_PCIE_TYPE0_HDR_DBI2_BAR3_MASK_REG
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:1	WO	0x7fffffff	PCI_TYPE0_BAR3_MASK BAR3 Mask. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: W (sticky) Note: This register field is sticky. Value After Reset: 0x7fffffff Testable: untestable
0	WO	0x1	PCI_TYPE0_BAR3_ENABLED BAR3 Mask Enabled. Note: This register field is sticky. Value After Reset: 0x1 Testable: untestable

USP_PCIE_TYPE0_HDR_DBI2_BAR4_MASK_REG
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	WO	0x7fffffff	PCI_TYPE0_BAR4_MASK BAR4 Mask. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: W (sticky) Note: This register field is sticky. Value After Reset: 0x7fffffff Testable: untestable
0	WO	0x1	PCI_TYPE0_BAR4_ENABLED BAR4 Mask Enabled. Note: This register field is sticky. Value After Reset: 0x1 Testable: untestable

USP_PCIE_TYPE0_HDR_DBI2_BAR5_MASK_REG
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	WO	0x7fffffff	PCI_TYPE0_BAR5_MASK BAR5 Mask. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: W (sticky) Note: This register field is sticky. Value After Reset: 0x7fffffff Testable: untestable
0	WO	0x1	PCI_TYPE0_BAR5_ENABLED BAR5 Mask Enabled. Note: This register field is sticky. Value After Reset: 0x1 Testable: untestable

USP_PCIE_TYPE0_HDR_DBI2_EXP_ROM_BAR_MASK_REG
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	WO	0x0000ffff	ROM_MASK Expansion ROM Mask. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if ROM_BAR_ENABLED && ROM_MASK_WRITABLE then W Note: This register field is sticky. Value After Reset: 0xffff Testable: untestable
0	WO	0x1	ROM_BAR_ENABLED Expansion ROM Bar Mask Register Enabled. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if ROM_MASK_WRITABLE then W Note: This register field is sticky. Value After Reset: 0x1 Testable: untestable

11.4.4.35 USP_PCIE_MSIX_CAP_DBI2 Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_MSIX_CAP_DBI2_PCI_MSIX_CAP_ID_NEXT_CTRL_REG	0x0000	W	0x007F0000	MSI-X Capability ID, Next Pointer, Control Registers
USP_PCIE_MSIX_CAP_DBI2_MSIX_TABLE_OFFSET_REG	0x0004	W	0x00000000	MSI-X Table Offset and BIR Register
USP_PCIE_MSIX_CAP_DBI2_MSIX_PBA_OFFSET_REG	0x0008	W	0x00000800	MSI-X PBA Offset and BIR Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.36 USP_PCIE_MSIX_CAP_DBI2 Detail Registers Description

USP_PCIE_MSIX_CAP_DBI2_PCI_MSIX_CAP_ID_NEXT_CTRL_REG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x07f	PCI_MSIX_TABLE_SIZE MSI-X Table Size in the shadow register. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1) then R/W else R Note: This register field is sticky. Value After Reset: 0x7f Testable: untestable Volatile: true
15:0	RO	0x0000	reserved

USP_PCIE_MSIX_CAP_DBI2_MSIX_TABLE_OFFSET_REG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	PCI_MSIX_TABLE_OFFSET MSI-X Table Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: untestable Volatile: true
2:0	RW	0x0	PCI_MSIX_BIR MSI-X Table BAR Indicator Register Field. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI , is used to map the Function's MSI-X Table into Memory Space. All encodings other than the defined encodings are reserved. For a 64-bit Base Address Register , the Table BIR indicates the lower DWORD. For Functions with Type 1 Configuration Space headers, BIR values 2 through 5 are also Reserved. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Values: 0x0 (BAR_10): Base Address Register 10h 0x1 (BAR_14): Base Address Register 14h 0x2 (BAR_18): Base Address Register 18h 0x3 (BAR_1C): Base Address Register 1Ch 0x4 (BAR_20): Base Address Register 20h 0x5 (BAR_24): Base Address Register 24h Value After Reset: 0x0 Testable: untestable Volatile: true

USP_PCIE_MSIX_CAP_DBI2_MSIX_PBA_OFFSET_REG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000100	PCI_MSIX_PBA_OFFSET MSI-X PBA Offset. Used as an offset from the address contained by one of the Function's Base Address Registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Value After Reset: 0x100 Testable: untestable Volatile: true
2:0	RW	0x0	PCI_MSIX_PBA_BIR MSI-X PBA BIR. This field indicates which one of a Function's Base Address Registers , located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BEI, is used to map the Function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the Table BIR . Note: The access attributes of this field are as follows: Wire: No access Dbi: No access Dbi2: if (DBI_RO_WR_EN == 1 && MSIX_CAP_ENABLE=1) then R/W else R Note: This register field is sticky. Value After Reset: 0x0 Testable: untestable Volatile: true

11.4.4.37 USP_PCIE_IATU Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_IATU_REGION_CTRL_1_OFF_OUTBOUND_i	0x0000	W	0x00000000	iATU Region Control 1 Register (for i = 0; i <= 15)
USP_PCIE_IATU_REGION_CTRL_2_OFF_OUTBOUND_i	0x0004	W	0x00000000	iATU Region Control 2 Register (for i = 0; i <= 15)

Name	Offset	Size	Reset Value	Description
USP_PCIE_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_i	0x0008	W	0x00000000	iATU Lower Base Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_i	0x000C	W	0x00000000	iATU Upper Base Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_LIMIT_ADDR_OFF_OUTBOUND_i	0x0010	W	0x0000FFF0	iATU Limit Address Registe (for i = 0; i <= 15)
USP_PCIE_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i	0x0014	W	0x00000000	iATU Lower Target Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_i	0x0018	W	0x00000000	iATU Upper Target Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_i	0x0020	W	0x00000000	iATU Upper Limit Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_REGION_CTRL_1_OFF_INBOUND_i	0x0100	W	0x00000000	iATU Region Control 1 Register (for i = 0; i <= 15)
USP_PCIE_IATU_REGION_CTRL_2_OFF_INBOUND_i	0x0104	W	0x00000000	iATU Region Control 2 Register (for i = 0; i <= 15)
USP_PCIE_IATU_LWR_BASE_ADDR_OFF_INBOUND_i	0x0108	W	0x00000000	iATU Lower Base Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_UPPER_BASE_ADDR_OFF_INBOUND_i	0x010C	W	0x00000000	iATU Upper Base Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_LIMIT_ADDR_OFF_INBOUND_i	0x0110	W	0x0000FFF0	iATU Limit Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_LWR_TARGET_ADDR_OFF_INBOUND_i	0x0114	W	0x00000000	iATU Lower Target Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_i	0x0118	W	0x00000000	iATU Upper Target Address Register (for i = 0; i <= 15)
USP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_i	0x0120	W	0x00000000	iATU Upper Limit Address Register (for i = 0; i <= 15)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.38 USP_PCIE_IATU Detail Registers Description

USP_PCIE_IATU_REGION_CTRL_1_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

Bit	Attr	Reset Value	Description
22:20	RW	0x0	CTRL_1_FUNC_NUM Function Number. When the address of an outbound TLP is matched to this region and the FUNC_BYPASS field in the "iATU Region Control 2 Register" is '0', then the function number used in generating the function part of the requester ID (RID) field of the TLP is taken from this 5-bit register. The value in this register must be 0x0 unless multifunction operation in the controller is enabled (CX_NFUNC > 1). When you are using the AXI Bridge, then this field is swapped before AXI decomposition occurs so that the correct "Max_Read_Request_Size" and "Max_Payload_Size" values are used. Note: This register field is sticky. Value After Reset: 0x0
19:18	RO	0x0	reserved
17:16	RW	0x0	AT AT. When the address of an outbound TLP is matched to this region, then the AT field of the TLP is changed to the value in this register. Only valid when the ATS_ENABLE configuration parameter is '1'. Note: This register field is sticky. Value After Reset: 0x0
15:14	RO	0x0	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky. Values: 0x1 (ENABLE): Maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE 0x0 (DISABLE): Maximum ATU Region size is 4 GB (default) Value After Reset: 0x0
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	TD This is a reserved field. Do not use. Note: This register field is sticky. Value After Reset: 0x0
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky. Value After Reset: 0x0
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_REGION_CTRL_2_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky. Value After Reset: 0x0
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0

Bit	Attr	Reset Value	Description
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky. Value After Reset: 0x0
27	RW	0x0	DMA_BYPASS DMA Bypass Mode. Allows request TLPs which are initiated by the DMA controller to pass through the iATU untranslated. Note: This field is reserved for the SW product. You must set it to '0'. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
26:24	RO	0x0	reserved
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. Encodings are as above. Note: This register field is sticky. Values: 0x1 (FILL_BYTES): LWR_TARGET_RW in the iATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i register is used to fill bytes 8-to-11 (for 3 DWORD header) or bytes 12-to-15 (for 4 DWORD header) of the translated TLP header. 0x0 (FORM_ADDR): LWR_TARGET_RW in the iATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i register forms the new address of the translated region. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. Encoding are define as above. Note: This register field is sticky. Values: 0x1 (NO_SUPPORT_FOR_DATA_TLP): Fmt[1] =0 so that only TLP type without data is sent. For example, a Msg instead of MsgD will be sent. 0x0 (SUPPORT_DATA_TLP): Fmt[1] =0/1 so that TLPs with or without data can be sent. Value After Reset: 0x0
21	RO	0x0	reserved
20	RW	0x0	SNP TLP Header Fields Translation Bypass. In this mode header fields of the translated TLP is taken from your application transmit interface or, if AMBA is configured, from the AMBA sideband bus (slv_awmisc_info) and not from the corresponding fields of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i or IATU_REGION_CTRL_2_OFF_OUTBOUND_i registers. The header fields are TC PH TH ST AT Attr (IDO, RO and NS). Note: This register field is sticky. Value After Reset: 0x0
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Region Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
18:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note (CX_TPH_ENABLE=1): TAG substitution for MWr will not occur because this field (byte 6) in the TLP header is the ST field. ST substitution can still take place using the MSG_CODE field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky. Value After Reset: 0x0
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Memory TLPs: (ST: Steering Tag). When the ST field of an outbound TLP is matched to this region, and the translated TLP TYPE field targets memory space; then the ST field of the TLP is changed to the value in this register. Only Valid when the CX_TPH_ENABLE configuration parameter is 1. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_LWR_BASE_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky. Value After Reset: 0x0
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE) Value After Reset: 0x0

USP_PCIE_IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_LIMIT_ADDR_OFF_OUTBOUND_i
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky. Value After Reset: 0x0
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller. Note: This register field is sticky. Value After Reset: 0xfff

Bit	Attr	Reset Value	Description
3:0	RO	0x0	CBUF_INCR Circular Buffer. Note: This register field is sticky. Value After Reset: 0xf

USP_PCIE_IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1'. These bits are always '0'. Value After Reset: 0x0
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_OUTBOUND_i is '1' Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_REGION_CTRL_1_OFF_INBOUND_i

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Function Number. MEM-I/O: When the Address and BAR matching logic in the controller indicate that a MEM-I/O transaction matches a BAR in the function corresponding to this value, then address translation proceeds. This check is only performed if the "Function Number Match Enable" bit of the "iATU Region Control 2 Register" is set. CFG0/CFG1: When the destination function number as specified in the routing ID of the TLP header matches the function, then address translation proceeds. This check is only performed if the "Function Number Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
19:18	RO	0x0	reserved
17:16	RW	0x0	AT When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "AT Match Enable" bit of the "iATU Region Control 2 Register" is set. Only valid when the ATS_ENABLE configuration parameter is '1'. Note: This register field is sticky. Value After Reset: 0x0
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky. Values: 0x1 (ENABLE): Maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE 0x0 (DISABLE): Maximum ATU Region size is 4 GB (default) Value After Reset: 0x0
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Region Control 2 Register" is set. Note: This register field is sticky. Value After Reset: 0x0
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_REGION_CTRL_2_OFF_INBOUND_i
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. -1: BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: -0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. -1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: -0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. -1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header. - If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN = 1 AND MSG_TYPE_MATCH_MODE =1, then Match Mode is ignored. Note: This register field is sticky. Values: 0x0 (ZERO): The interpretation is dependent on TLP type, that is, MEM/IO, CFG0, or MSG/MSGD TLPs. 0x1 (ONE): The interpretation is dependent on TLP type, that is, MEM/IO, CFG0, or MSG/MSGD TLPs. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
29	RW	0x0	INVERT_MODE Invert Mode Enable. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). When set all regions of that type must use address match mode. Note: This register field is sticky. Values: 0x1 (ENABLE): Invert Mode Enable 0x0 (DISABLE): Invert Mode Disable Value After Reset: 0x0
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Enable. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky. Values: 0x1 (ENABLE): CFG Shift Enable 0x0 (DISABLE): CFG Shift Disable Value After Reset: 0x0
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Enable. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. MWr, MRd, and MRdLk TLPs are seen as identical The Routing field of Msg/MsgD TLPs is ignored FetchAdd, Swap, and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Region Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. Note: This register field is sticky. Values: 0x1 (ENABLE): Fuzzy Type Match Enable 0x0 (DISABLE): Fuzzy Type Match Disable Value After Reset: 0x0
26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. Note: This register field is sticky. Values: 0x0 (NORMAL_RADM): Normal RADM filter response is used. 0x1 (UNSUP_REQ): Unsupported request (UR) 0x2 (COMPL_ABORT): Completer abort (CA) 0x3 (NOT_USED): Not used / undefined / reserved Value After Reset: 0x0
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
22	RO	0x0	reserved
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Region Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Region Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky. Values: 0x1 (ENABLE): Message Code Match Enable (for Msg TLPS) or ST Match Enable (for Mem TLPs) 0x0 (DISABLE): Virtual Function Number Match Disable Value After Reset: 0x0
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19	RW	0x0	FUNC_NUM_MATCH_EN Function Number Match Enable. Ensures that a successful Function Number TLP field comparison match (see Function Number field of the "iATU Region Control 1 Register") occurs (in MEM-I/O and CFG0/CFG1 transactions) for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): Function Number Match Enable 0x0 (DISABLE): Function Number Match Disable Value After Reset: 0x0
18	RO	0x0	reserved
17	RW	0x0	AT_MATCH_EN AT Match Enable. Ensures that a successful AT TLP field comparison match (see AT field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Only valid when the ATS_ENABLE configuration parameter is '1'. Note: This register field is sticky. Values: 0x1 (ENABLE): AT Match Enable 0x0 (DISABLE): AT Match Disable Value After Reset: 0x0
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): ATTR Match Enable 0x0 (DISABLE): ATTR Match Disable Value After Reset: 0x0
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): TD Match Enable 0x0 (DISABLE): TD Match Disable Value After Reset: 0x0

Bit	Attr	Reset Value	Description
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Region Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky. Values: 0x1 (ENABLE): TC Match Enable 0x0 (DISABLE): TC Match Disable Value After Reset: 0x0
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the IATU_REGION_CTRL_1_VIEWPORT_OFF_INBOUND_i register (TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0
12:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	BAR_NUM BAR Number. When the BAR number of an inbound MEM or IO TLP " that is matched by the normal internal BAR address matching mechanism " is the same as this field, address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Match Mode" bit of the "iATU Region Control 2 Register" is set. IO translation would require either 00100b or 00101b in the inbound TLP TYPE; the BAR Number set in the range 000b - 101b and that BAR configured as an IO BAR. Note: This register field is sticky. Values: 0x0 (BAR0): BAR0 0x1 (BAR1): BAR1 0x2 (BAR2): BAR2 0x3 (BAR3): BAR3 0x4 (BAR4): BAR4 0x5 (BAR5): BAR5 0x6 (ROM): ROM 0x7 (RSVD): reserved Value After Reset: 0x0
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Region Control 2 Register" is set. Memory TLPs: (ST: Steering Tag). When the ST field of an inbound TLP is matched to this value, then address translation proceeds. This check is only performed if the "ST Match Enable" bit of the "iATU Region Control 2 Register" is set. The setting is independent of the setting of the TH field. Only Valid when the CX_TPH_ENABLE configuration parameter is '1'. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_LWR_BASE_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky. Value After Reset: 0x0
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE) Value After Reset: 0x0

USP_PCIE_IATU_UPPER_BASE_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_LIMIT_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms the upper bits of the limit address for the circular buffer. Note: This register field is sticky. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:4	RO	0xfff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. When SINGLE_ADDR_LOC_TRANS_EN = 1, MSG_TYPE_MATCH_MODE = 1, and CBUF_INCR > 0 then this field forms lower bits of the limit address for the circular buffer. A write to this location is ignored by the PCIe controller. Note: This register field is sticky. Value After Reset: 0xfff
3:0	RW	0x0	CBUF_INCR Circular Buffer Increment. When CX_ATU_SLOC_CBUF = 0, then this field is Read-only and forms the lowest bits of the end address of the address region to be translated. When CX_ATU_SLOC_CBUF = 1, then this field is R/W and forms the upper bits of the Circular Buffer Increment size (CBUF_INCR) field for Single Location Address translation. The increment value (in bytes) is decoded as follows: 0000b: 0 (Default; legacy Single Address Location mode) 0001b: 4 0010b: 8 0011b: 16 0100b: 32 0101b: 64 0110b: 128 0111b: 256 1000b: 512 1001b: 1024 1010b: 2048 1011b: 4096 1100b: 8192 1101b: rsvd. 1110b: rsvd. 1111b: rsvd. Note: A write to any bit in the CBUF_INCR field resets the circular buffer pointer ? that is, the next matched received Message will be translated to the start address of the Circular Buffer. This field must be written to AFTER the target and limit registers have been updated. Note: The access attributes of this field are as follows: Wire: No access. Dbi: R (sticky) Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_LWR_TARGET_ADDR_OFF_INBOUND_i
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky. Value After Reset: 0x0
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. Field size depends on log2(BAR_MASK+1) in BAR match mode. Value After Reset: 0x0

USP_PCIE_IATU_UPPER_TARGET_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky. Value After Reset: 0x0

USP_PCIE_IATU_UPPR_LIMIT_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	UPPR_LIMIT_ADDR_HW Forms MSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1'. These bits are always '0'. Value After Reset: 0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	UPPR_LIMIT_ADDR_RW Forms the LSB's of the Upper Limit part of the region "end address" to be translated. Only applies to 64-bit systems and when the INCREASE_REGION_SIZE field in IATU_REGION_CTRL_1_OFF_INBOUND_i is '1' Note: This register field is sticky. Value After Reset: 0x0

11.4.4.39 USP_PCIE_DMA Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_DMA_CTRL_DATA_ARB_PRIOR_OFF	0x0000	W	0x00000688	DMA Arbitration Scheme for TRGT1 Interface
USP_PCIE_DMA_CTRL_OFF	0x0008	W	0x00020002	DMA Number of Channels Register
USP_PCIE_DMA_WRITE_ENGINE_EN_OFF	0x000C	W	0x00000000	DMA Write Engine Enable Register
USP_PCIE_DMA_WRITE_DOORBELL_OFF	0x0010	W	0x00000000	DMA Write Doorbell Register
USP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF	0x0018	W	0x00008421	DMA Write Engine Channel Arbitration Weight Low Register
USP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF	0x001C	W	0x00000000	DMA Write Engine Channel Arbitration Weight High Register
USP_PCIE_DMA_READ_ENGINE_EN_OFF	0x002C	W	0x00000000	DMA Read Engine Enable Register
USP_PCIE_DMA_READ_DOORBELL_OFF	0x0030	W	0x00000000	DMA Read Doorbell Register
USP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF	0x0038	W	0x00008421	DMA Read Engine Channel Arbitration Weight Low Register
USP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF	0x003C	W	0x00008421	DMA Read Engine Channel Arbitration Weight High Register
USP_PCIE_DMA_WRITE_INT_STATUS_OFF	0x004C	W	0x00000000	DMA Write Interrupt Status Register
USP_PCIE_DMA_WRITE_INT_MASK_OFF	0x0054	W	0x00030003	DMA Write Interrupt Mask Register
USP_PCIE_DMA_WRITE_INT_CLEAR_OFF	0x0058	W	0x00000000	DMA Write Interrupt Clear Register
USP_PCIE_DMA_WRITE_ERR_STATUS_OFF	0x005C	W	0x00000000	DMA Write Error Status Register
USP_PCIE_DMA_WRITE_DONE_IMWR_LOW_OFF	0x0060	W	0x00000000	DMA Write Done IMWr Address Low Register
USP_PCIE_DMA_WRITE_DONE_IMWR_HIGH_OFF	0x0064	W	0x00000000	DMA Write Done IMWr Interrupt Address High Register
USP_PCIE_DMA_WRITE_ABORT_IMWR_LOW_OFF	0x0068	W	0x00000000	DMA Write Abort IMWr Address Low Register
USP_PCIE_DMA_WRITE_ABORT_IMWR_HIGH_OFF	0x006C	W	0x00000000	DMA Write Abort IMWr Address High Register

Name	Offset	Size	Reset Value	Description
USP_PCIE_DMA_WRITE_CH01_IMWR_DATA_OFF	0x0070	W	0x00000000	DMA Write Channel 1 and 0 IMWr Data Register
USP_PCIE_DMA_WRITE_CH23_IMWR_DATA_OFF	0x0074	W	0x00000000	DMA Write Channel 3 and 2 IMWr Data Register
USP_PCIE_DMA_WRITE_CH45_IMWR_DATA_OFF	0x0078	W	0x00000000	DMA Write Channel 5 and 4 IMWr Data Register
USP_PCIE_DMA_WRITE_CH67_IMWR_DATA_OFF	0x007C	W	0x00000000	DMA Write Channel 7 and 6 IMWr Data Register
USP_PCIE_DMA_WRITE_LINKED_LIST_ERR_EN_OFF	0x0090	W	0x00000000	DMA Write Linked List Error Enable Register
USP_PCIE_DMA_READ_INT_STATUS_OFF	0x00A0	W	0x00000000	DMA Read Interrupt Status Register
USP_PCIE_DMA_READ_INT_MASK_OFF	0x00A8	W	0x00030003	DMA Read Interrupt Mask Register
USP_PCIE_DMA_READ_INT_CLEAR_OFF	0x00AC	W	0x00000000	DMA Read Interrupt Clear Register
USP_PCIE_DMA_READ_ERR_STATUS_LOW_OFF	0x00B4	W	0x00000000	DMA Read Error Status Low Register
USP_PCIE_DMA_READ_ERR_STATUS_HIGH_OFF	0x00B8	W	0x00000000	DMA Read Error Status High Register
USP_PCIE_DMA_READ_LINKED_LIST_ERR_EN_OFF	0x00C4	W	0x00000000	DMA Read Linked List Error Enable Register
USP_PCIE_DMA_READ_DONE_IMWR_LOW_OFF	0x00CC	W	0x00000000	DMA Read Done IMWr Address Low Register
USP_PCIE_DMA_READ_DONE_IMWR_HIGH_OFF	0x00D0	W	0x00000000	DMA Read Done IMWr Address High Register
USP_PCIE_DMA_READ_ABORT_IMWR_LOW_OFF	0x00D4	W	0x00000000	DMA Read Abort IMWr Address Low Register
USP_PCIE_DMA_READ_ABORT_IMWR_HIGH_OFF	0x00D8	W	0x00000000	DMA Read Abort IMWr Address High Register
USP_PCIE_DMA_READ_CH01_IMWR_DATA_OFF	0x00DC	W	0x00000000	DMA Read Channel 1 and 0 IMWr Data Register
USP_PCIE_DMA_READ_CH23_IMWR_DATA_OFF	0x00E0	W	0x00000000	DMA Read Channel 3 and 2 IMWr Data Register
USP_PCIE_DMA_READ_CH45_IMWR_DATA_OFF	0x00E4	W	0x00000000	DMA Read Channel 5 and 4 IMWr Data Register
USP_PCIE_DMA_READ_CH67_IMWR_DATA_OFF	0x00E8	W	0x00000000	DMA Read Channel 7 and 6 IMWr Data Register
USP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_LOW_OFF	0x0108	W	0x00000000	DMA Write Engine Handshake Counter Channel 0/1/2/3 Register
USP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF	0x010C	W	0x00000000	DMA Write Engine Handshake Counter Channel 4/5/6/7 Register
USP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF	0x0118	W	0x00000000	DMA Read Engine Handshake Counter Channel 0/1/2/3 Register
USP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF	0x011C	W	0x00000000	DMA Read Engine Handshake Counter Channel 4/5/6/7 Register
USP_PCIE_DMA_WRITE_CHi_PWR_EN_OFF	0x0128	W	0x00000000	DMA Write Channel 0 Power Enable Register (for i = 0; i <= 7)

Name	Offset	Size	Reset Value	Description
USP_PCIE_DMA_READ_CHi_PWR_EN_OFF	0x0168	W	0x00000000	DMA Read Channel 0 Power Enable Register (for i = 0; i <= 7)
USP_PCIE_DMA_CH_CONTROL1_OFF_WRCH_i	0x0200	W	0x00000000	DMA Write Channel Control 1 Register (for i = 0; i <= 1)
USP_PCIE_DMA_TRANSFER_SIZE_OFF_WRCH_i	0x0208	W	0x00000000	DMA Write Transfer Size Register
USP_PCIE_DMA_SAR_LOW_OFF_WRCH_i	0x020C	W	0x00000000	DMA Write SAR Low Register
USP_PCIE_DMA_SAR_HIGH_OFF_WRCH_i	0x0210	W	0x00000000	DMA Write SAR High Register (for i = 0; i <= 1)
USP_PCIE_DMA_DAR_LOW_OFF_WRCH_i	0x0214	W	0x00000000	DMA Write DAR Low Register (for i = 0; i <= 1)
USP_PCIE_DMA_DAR_HIGH_OFF_WRCH_i	0x0218	W	0x00000000	DMA Write DAR High Register (for i = 0; i <= 1)
USP_PCIE_DMA_LLP_LOW_OFF_WRCH_i	0x021C	W	0x00000000	DMA Write Linked List Pointer Low Register (for i = 0; i <= 1)
USP_PCIE_DMA_LLP_HIGH_OFF_WRCH_i	0x0220	W	0x00000000	DMA Write Linked List Pointer High Register (for i = 0; i <= 1)
USP_PCIE_DMA_CH_CONTROL1_OFF_RDCH_i	0x0300	W	0x00000000	DMA Read Channel Control 1 Register (for i = 0; i <= 1)
USP_PCIE_DMA_TRANSFER_SIZE_OFF_RDCH_i	0x0308	W	0x00000000	DMA Read Transfer Size Register (for i = 0; i <= 1)
USP_PCIE_DMA_SAR_LOW_OFF_RDCH_i	0x030C	W	0x00000000	DMA Read SAR Low Register (for i = 0; i <= 1)
USP_PCIE_DMA_SAR_HIGH_OFF_RDCH_i	0x0310	W	0x00000000	DMA Read SAR High Register (for i = 0; i <= 1)
USP_PCIE_DMA_DAR_LOW_OFF_RDCH_i	0x0314	W	0x00000000	DMA Read DAR Low Register (for i = 0; i <= 1)
USP_PCIE_DMA_DAR_HIGH_OFF_RDCH_i	0x0318	W	0x00000000	DMA Read DAR High Register (for i = 0; i <= 1)
USP_PCIE_DMA_LLP_LOW_OFF_RDCH_i	0x031C	W	0x00000000	DMA Read Linked List Pointer Low Register (for i = 0; i <= 1)
USP_PCIE_DMA_LLP_HIGH_OFF_RDCH_i	0x0320	W	0x00000000	DMA Read Linked List Pointer High Register (for i = 0; i <= 1)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.40 USP_PCIE_DMA Detail Registers Description

USP_PCIE_DMA_CTRL_DATA_ARB_PRIOR_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	VERSION Reports the version of Register Map of eDMA. Value After Reset: 0x0
11:9	RW	0x3	RDBUFF_TRGT_WEIGHT DMA Read Channel MWr Requests. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x3

Bit	Attr	Reset Value	Description
8:6	RW	0x2	RD_CTRL_TRGT_WEIGHT DMA Read Channel MRd Requests (for LL element/descriptor access). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x2
5:3	RW	0x1	WR_CTRL_TRGT_WEIGHT DMA Write Channel MRd Requests (for DMA data requests and LL element/descriptor access). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
2:0	RW	0x0	RTRGT1_WEIGHT Non-DMA Rx Requests. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_CTRL_OFF
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	DIS_C2W_CACHE_RD Disable DMA Read Channel's "completion to memory write" context cache pre-fetch function. Note: For internal debugging only. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
24	RW	0x0	DIS_C2W_CACHE_WR Disable DMA Write Channel's "completion to memory write" context cache pre-fetch function. Note: For internal debugging only. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RO	0x2	NUM_DMA_RD_CHAN Number of Read Channels. You can read this register to determine the number of read channels configured. Value After Reset: 0x2
15:4	RO	0x000	reserved
3:0	RO	0x2	NUM_DMA_WR_CHAN Number of Write Channels. You can read this register to determine the number of write channels configured. Value After Reset: 0x2

USP_PCIE_DMA_WRITE_ENGINE_EN_OFF
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH7 Enable Handshake for DMA Write Engine Channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
22	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH6 Enable Handshake for DMA Write Engine Channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
21	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH5 Enable Handshake for DMA Write Engine Channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
20	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH4 Enable Handshake for DMA Write Engine Channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
19	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH3 Enable Handshake for DMA Write Engine Channel 3. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
18	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH2 Enable Handshake for DMA Write Engine Channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
17	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH1 Enable Handshake for DMA Write Engine Channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
16	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH0 Enable Handshake for DMA Write Engine Channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	DMA_WRITE_ENGINE DMA Write Engine Enable. For normal operation, you must initially set this bit to '1', before any other software setup action. You do not need to toggle or rewrite to this bit during normal operation. You should set this bit to '0' when you want to "Soft Reset" the DMA controller write logic. There are three possible reasons for resetting the DMA controller write logic: The "Abort Interrupt Status" bit is set in the DMA Write Interrupt Status Register (DMA_WRITE_INT_STATUS_OFF), and any of the bits in the DMA Write Error Status Register (DMA_WRITE_ERR_STATUS_OFF) are set. Resetting the DMA controller write logic re-initializes the control logic, ensuring that the next DMA write transfer is executed successfully. You have executed the procedure outlined in "Stop Bit", after which, the "Abort Interrupt Status" bit is set and the Channel Status(CS) field of the DMA Write Channel Control 1 Register (DMA_CH_CONTROL1_OFF_WRCH_i) is set to "Stopped". Resetting the DMA controller write logic re-initializes the control logic ensuring that the next DMA write transfer is executed successfully. During software development, when you incorrectly program the DMA write engine. To "Soft Reset" the DMA controller write logic, you must: De-assert the DMA write engine enable bit. Wait for the DMA to complete any in-progress TLP transfer, by waiting until a read on the DMA write engine enable bit returns a '0'. Assert the DMA write engine enable bit. This "Soft Reset" does not clear the DMA configuration registers. The DMA write transfer does not start until you write to the DMA Write Doorbell Register (DMA_WRITE_DOORBELL_OFF). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable (Soft Reset) Value After Reset: 0x0 Testable: untestable Volatile: true

USP_PCIE_DMA_WRITE_DOORBELL_OFF
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	WR_STOP Stop. Set in conjunction with the Doorbell Number field. The DMA write channel stops issuing requests, sets the channel status to "Stopped", and asserts the "Abort" interrupt if it is enabled. Before setting the Stop bit, you must read the channel Status field (CS) of the DMA Write Channel Control 1 Register (DMA_CH_CONTROL1_OFF_WRCH_0) to ensure that the write channel is "Running" (transferring data). For more information, see "Stopping the DMA Transfer (Software Stop)". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:3	RO	0x0000000	reserved
2:0	RW	0x0	WR_DOORBELL_NUM Doorbell Number. You must write the channel number to this register to start the DMA write transfer for that channel. The DMA detects a write to this register field even if the value of this field does not change. You do not need to toggle or write any other value to this register to start a new transfer. The range of this field is 0x0 to 0x7, where 0x0 corresponds to channel 0. Note: A write to this field triggers the controller to exit L1 substates. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

USP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x01	WRITE_CHANNEL3_WEIGHT Channel 3 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
14:10	RW	0x01	WRITE_CHANNEL2_WEIGHT Channel 2 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
9:5	RW	0x01	WRITE_CHANNEL1_WEIGHT Channel 1 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
4:0	RW	0x01	WRITE_CHANNEL0_WEIGHT Channel 0 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1

USP_PCIE_DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x00	WRITE_CHANNEL7_WEIGHT Channel 7 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
14:10	RW	0x00	WRITE_CHANNEL6_WEIGHT Channel 6 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
9:5	RW	0x00	WRITE_CHANNEL5_WEIGHT Channel 5 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
4:0	RW	0x00	WRITE_CHANNEL4_WEIGHT Channel 4 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1

USP_PCIE_DMA_READ_ENGINE_EN_OFF

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH7 Enable Handshake for DMA Read Engine Channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
22	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH6 Enable Handshake for DMA Read Engine Channel 6. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
21	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH5 Enable Handshake for DMA Read Engine Channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
20	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH4 Enable Handshake for DMA Read Engine Channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
19	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH3 Enable Handshake for DMA Read Engine Channel 3. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
18	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH2 Enable Handshake for DMA Read Engine Channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
17	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH1 Enable Handshake for DMA Read Engine Channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
16	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH0 Enable Handshake for DMA Read Engine Channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:1	RO	0x0000	reserved
0	RW	0x0	DMA_READ_ENGINE DMA Read Engine Enable. 1: Enable 0: Disable (Soft Reset) For normal operation, you must initially set this bit to "1", before any other software setup actions. You do not need to toggle or rewrite to this bit during normal operation. You should set this field to "0" when you want to "Soft Reset" the DMA controller read logic. There are three possible reasons for resetting the DMA controller read logic: The "Abort Interrupt Status" bit is set (in the "DMA Read Interrupt Status Register" (DMA_READ_INT_STATUS_OFF), and any of the bits in the "DMA Read Error Status Low Register" (DMA_READ_ERR_STATUS_LOW_OFF) is set. Resetting the DMA controller read logic re-initializes the control logic, ensuring that the next DMA read transfer is executed successfully. You have executed the procedure outlined in "Stop Bit", after which, the "Abort Interrupt Status" bit is set and the channel Status field (CS) of the DMA read "DMA Channel Control 1 Register " (DMA_CH_CONTROL1_OFF_WRCH_0) is set to "Stopped". Resetting the DMA controller read logic re-initializes the control logic ensuring that the next DMA read transfer is executed successfully. During software development, when you incorrectly program the DMA read engine. To "Soft Reset" the DMA controller read logic, you must: De-assert the DMA read engine enable bit. Wait for the DMA to complete any in-progress TLP transfer, by waiting until a read on the DMA read engine enable bit returns a "0". Assert the DMA read engine enable bit. This "Soft Reset" does not clear the DMA configuration registers. The DMA read transfer does not start until you write to the "DMA Read Doorbell Register" (DMA_READ_DOORBELL_OFF). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

USP_PCIE_DMA_READ_DOORBELL_OFF
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31	RW	0x0	RD_STOP Stop. Set in conjunction with the Doorbell Number field. The DMA read channel stops issuing requests, sets the channel status to "Stopped", and asserts the "Abort" interrupt if it is enabled. Before setting the Stop bit, you must read the channel Status field (CS) of the DMA Channel Control 1 Register (DMA_CH_CONTROL1_OFF_RDCH_i) to ensure that the read channel is "Running" (transferring data). For more information, see "Stopping the DMA Transfer (Software Stop)". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
30:3	RO	0x0000000	reserved
2:0	RW	0x0	RD_DOORBELL_NUM Doorbell Number. You must write 0x0 to this register to start the DMA read transfer for that channel. The DMA detects a write to this register field even if the value of this field does not change. The range of this field is 0x0 to 0x7, where 0x0 corresponds to channel 0. Note: A write to this field triggers the controller to exit L1 substates. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x01	READ_CHANNEL3_WEIGHT Channel 3 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
14:10	RW	0x01	READ_CHANNEL2_WEIGHT Channel 2 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
9:5	RW	0x01	READ_CHANNEL1_WEIGHT Channel 1 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
4:0	RW	0x01	READ_CHANNEL0_WEIGHT Channel 0 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1

USP_PCIE_DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:15	RW	0x01	READ_CHANNEL7_WEIGHT Channel 7 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
14:10	RW	0x01	READ_CHANNEL6_WEIGHT Channel 6 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
9:5	RW	0x01	READ_CHANNEL5_WEIGHT Channel 5 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1
4:0	RW	0x01	READ_CHANNEL4_WEIGHT Channel 4 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x1

USP_PCIE_DMA_WRITE_INT_STATUS_OFF

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	WR_ABORT_INT_STATUS Abort Interrupt Status. The DMA write channel has detected an error, or you manually stopped the transfer as described in "Error Handling Assistance by Remote Software". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA write interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved
7:0	RW	0x00	WR_DONE_INT_STATUS Done Interrupt Status. The DMA write channel has successfully completed the DMA transfer. For more details, see "Interrupts and Error Handling". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA write interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

USP_PCIE_DMA_WRITE_INT_MASK_OFF
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x3	WR_ABORT_INT_MASK Abort Interrupt Mask. Prevents the Abort interrupt status field in the DMA write interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x3
15:2	RO	0x0000	reserved
1:0	RW	0x3	WR_DONE_INT_MASK Done Interrupt Mask. Prevents the Done interrupt status field in the DMA write interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x3

USP_PCIE_DMA_WRITE_INT_CLEAR_OFF

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	WR_ABORT_INT_CLEAR Abort Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Abort interrupt status field of the DMA write interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1:0	WO	0x0	WR_DONE_INT_CLEAR Done Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Done interrupt status field of the DMA write interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_WRITE_ERR_STATUS_OFF

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	LINKLIST_ELEMENT_FETCH_ERR_DETECT Linked List Element Fetch Error Detected. The DMA write channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while reading a linked list element from local memory. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Write Interrupt Clear Register (DMA_WRITE_INT_CLEAR_OFF) to clear this error bit. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	APP_READ_ERR_DETECT Application Read Error Detected. The DMA write channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while reading data from it. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Write Interrupt Clear Register (DMA_WRITE_INT_CLEAR_OFF) to clear this error bit. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_WRITE_DONE_IMWR_LOW_OFF
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_DONE_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Done IMWr TLP. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_DONE_IMWR_HIGH_OFF
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_DONE_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Done IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_ABORT_IMWR_LOW_OFF
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_ABORT_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP it generates. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_ABORT_IMWR_HIGH_OFF
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_WRITE_ABORT_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Abort IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_CH01_IMWR_DATA_OFF
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_1_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	WR_CHANNEL_0_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_CH23_IMWR_DATA_OFF
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_3_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 3. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	WR_CHANNEL_2_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_CH45_IMWR_DATA_OFF
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_5_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	WR_CHANNEL_4_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_CH67_IMWR_DATA_OFF
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_7_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	WR_CHANNEL_6_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 6. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_LINKED_LIST_ERR_EN_OFF

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	WR_CHANNEL_LLLAIE Write Channel LL Local Abort Interrupt Enable (LLLAIE). You enable the write channel local abort interrupt through this bit. The LIE and RIE bits in the LL element enable the write channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:2	RO	0x0000	reserved
1:0	RW	0x0	WR_CHANNEL_LLRAIE Write Channel LL Remote Abort Interrupt Enable (LLRAIE). You enable the write channel remote abort interrupt through this bit. The LIE and RIE bits in the LL element enable the write channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_INT_STATUS_OFF

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	RD_ABORT_INT_STATUS Abort Interrupt Status. The DMA read channel has detected an error, or you manually stopped the transfer as described in "Stopping the DMA Transfer (Software Stop)". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. You can read the DMA Read Error Status Low Register (DMA_READ_ERR_STATUS_LOW_OFF) and DMA Read Error Status High Register (DMA_READ_ERR_STATUS_HIGH_OFF) to determine the source of the error. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA read interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved
7:0	RW	0x00	RD_DONE_INT_STATUS Done Interrupt Status. The DMA read channel has successfully completed the DMA read transfer. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA read interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_READ_INT_MASK_OFF

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x3	RD_ABORT_INT_MASK Abort Interrupt Mask. Prevents the Abort interrupt status field in the DMA read interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x3
15:2	RO	0x0000	reserved
1:0	RW	0x3	RD_DONE_INT_MASK Done Interrupt Mask. Prevents the Done interrupt status field in the DMA read interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x3

USP_PCIE_DMA_READ_INT_CLEAR_OFF

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	WO	0x00	RD_ABORT_INT_CLEAR Abort Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Abort interrupt status field of the DMA read interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	WO	0x00	RD_DONE_INT_CLEAR Done Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Done interrupt status field of the DMA read interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a '0'. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_READ_ERR_STATUS_LOW_OFF

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	LINK_LIST_ELEMENT_FETCH_ERR_DETECT Linked List Element Fetch Error Detected. The DMA read channel has received an error response from the AXI bus while reading a linked list element from local memory. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this clears all bits in this register, and also the DMA Read Error Status High register (DMA_READ_ERR_STATUS_HIGH_OFF). Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	APP_WR_ERR_DETECT Application Write Error Detected. The DMA read channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while writing data to it. This error is fatal. You must restart the transfer from the beginning, as the channel context is corrupted, and the transfer is not rolled back. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this clears all bits in this register, and also the DMA Read Error Status High register (DMA_READ_ERR_STATUS_HIGH_OFF). Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_READ_ERR_STATUS_HIGH_OFF

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DATA_POISIONING Data Poisoning. The DMA read channel has detected data poisoning in the completion from the remote device (in response to the MRd request). The DMA read channel will drop the completion and then be halted. The CX_FLT_MASK_UR_POIS filter rule does not affect this behavior. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23:16	RO	0x00	CPL_TIMEOUT Completion Time Out. The DMA read channel has timed-out while waiting for the remote device to respond to the MRd request, or a malformed CplD has been received. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling" . Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true
15:8	RO	0x00	CPL_ABORT Completer Abort. The DMA read channel has received a PCIe completer abort completion status from the remote device in response to the MRd request. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
7:0	RO	0x00	UNSUPPORTED_REQ Unsupported Request. The DMA read channel has received a PCIe unsupported request completion status from the remote device in response to the MRd request. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For more details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the DMA Read Interrupt Clear Register (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register. Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_READ_LINKED_LIST_ERR_EN_OFF
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	RD_CHANNEL_LLLAIE Read Channel LL Local Abort Interrupt Enable (LLLAIE). You enable the read channel Local Abort interrupt through this bit. The LIE and RIE bits in the LL element enable the read channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:1	RO	0x0000	reserved
0	RW	0x0	RD_CHANNEL_LLRAIE Read Channel LL Remote Abort Interrupt Enable (LLRAIE). You enable the read channel Remote Abort interrupt through this bit. The LIE and RIE bits in the LL element enable the read channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_DONE_IMWR_LOW_OFF
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_DONE_LOW_REG The DMA uses this field to generate bits [63:32] of the address field for the Done IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_DONE_IMWR_HIGH_OFF
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_DONE_HIGH_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_ABORT_IMWR_LOW_OFF
Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_ABORT_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP. Bits [1:0] must be '00' as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_ABORT_IMWR_HIGH_OFF
Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_ABORT_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Abort IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_CH01_IMWR_DATA_OFF
Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_1_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	RD_CHANNEL_0_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_CH23_IMWR_DATA_OFF
Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_3_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x
15:0	RW	0x0000	RD_CHANNEL_2_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x

USP_PCIE_DMA_READ_CH45_IMWR_DATA_OFF
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_5_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	RD_CHANNEL_4_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_READ_CH67_IMWR_DATA_OFF

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_7_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0
15:0	RW	0x0000	RD_CHANNEL_6_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 6. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0

USP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_LOW_OFF

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH3 DMA handshake counter for DMA Write Engine Channel 3. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH2 DMA handshake counter for DMA Write Engine Channel 2. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH1 DMA handshake counter for DMA Write Engine Channel 1. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH0 DMA handshake counter for DMA Write Engine Channel 0. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

USP_PCIE_DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH7 DMA handshake counter for DMA Write Engine Channel 7. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH6 DMA handshake counter for DMA Write Engine Channel 6. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH5 DMA handshake counter for DMA Write Engine Channel 5. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH4 DMA handshake counter for DMA Write Engine Channel 4. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

USP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH3 DMA handshake counter for DMA Read Engine Channel 3. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH2 DMA handshake counter for DMA Read Engine Channel 2. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH1 DMA handshake counter for DMA Read Engine Channel 1. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH0 DMA handshake counter for DMA Read Engine Channel 0. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

USP_PCIE_DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF
Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH7 DMA handshake counter for DMA Read Engine Channel 7. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH6 DMA handshake counter for DMA Read Engine Channel 6. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH5 DMA handshake counter for DMA Read Engine Channel 5. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH4 DMA handshake counter for DMA Read Engine Channel 4. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero. Value After Reset: 0x0

USP_PCIE_DMA_WRITE_CHi_PWR_EN_OFF
Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_WRITE_CH0_PWR_EN DMA Write Channel 0 Power enable/disable. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0

USP_PCIE_DMA_READ_CHi_PWR_EN_OFF
Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_READ_CH0_PWR_EN DMA Read Channel 0 Power enable/disable. Values: 0x1 (ENABLE): Enable 0x0 (DISABLE): Disable Value After Reset: 0x0

USP_PCIE_DMA_CH_CONTROL1_OFF_WRCH_i
Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	DMA_AT Address Translation TLP Header Bit (AT). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
29:27	RW	0x0	DMA_TC Traffic Class TLP Header Bit (TC). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
26	RO	0x0	reserved
25	RW	0x0	DMA_RO Relaxed Ordering TLP Header Bit (RO). DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
24	RW	0x0	DMA_NS_SRC Source No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MRd (SAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
23	RW	0x0	DMA_NS_DST Destination No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MWr (DAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
22	RW	0x0	DMA_MEM_TYPE Master AXI ACE-Lite Cache Coherency Control. This field sets the DMA channel memory type of the address space of the data transfer as follows: For more details, see "ACE-Lite Features and Limitations" section of the Databook. Irrespective of the value of this field, Linked list descriptor requests have this attribute set to 0x1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (PERIPHERAL): peripheral type 0x1 (MEM_TYPE): memory type Value After Reset: 0x0 Testable: writeAsRead Volatile: true
21:17	RO	0x00	reserved
16:12	RW	0x00	DMA_FUNC_NUM Function Number (FN). The controller uses this field when generating the requester ID for the MRd/MWr DMA TLP. When you have enabled SR-IOV, then this field is ignored if you have set the VFE field in the "DMA Write Channel Control 2 Register" (DMA_CH_CONTROL2_OFF_WRCH_0). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	LLE Linked List Enable (LLE). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x1 (ENABLE): Enable linked list operation 0x0 (DISABLE): Disable linked list operation Value After Reset: 0x0 Testable: writeAsRead Volatile: true
8	RW	0x0	CCS Consumer Cycle State (CCS). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". You must initialize this bit. The DMA updates this bit during linked list operation. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RO	0x0	CS Channel Status (CS). The channel status bits identify the current operational state of the DMA channel. The operation state encoding for each DMA channel is a s follows: Values: 0x0 (RESERVED): Reserved 0x1 (RUNNING): This channel is active and transferring data 0x2 (HALTED): An error condition has been detected, and the DMA has stopped this channel 0x3 (STOPPED): The DMA has transferred all data for this channel, or you have prematurely stopped this channel by writing to the Stop field of the DMA Write Doorbell Register (DMA_WRITE_DOORBELL_OFF) or DMA Read Doorbell Register (DMA_READ_DOORBELL_OFF) Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	RW	0x0	RIE Remote Interrupt Enable (RIE). You must set this bit to enable the generation of the Done or Abort Remote interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the RIE of the LL element. The RIE bit in a LL element only enables the Done interrupt. In non-LL mode, the RIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	LIE Local Interrupt Enable (LIE). You must set this bit to enable the generation of the Done or Abort Local interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the LIE of the LL element. The LIE bit in a LL element only enables the Done interrupt. In non-LL mode, the LIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RW	0x0	LLP Load Link Pointer (LLP). Used in linked list mode only. Indicates that this linked list element is a link element, and its LL element pointer dwords are pointing to the next (non-contiguous) element. The DMA loads this field with the LLP of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	RW	0x0	TCB Toggle Cycle Bit (TCB). Indicates to the DMA to toggle its interpretation of the CB. Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the TCB of the linked list element. this field is not defined in a data LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	CB Cycle Bit (CB). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the CB of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_TRANSFER_SIZE_OFF_WRCH_i
Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_TRANSFER_SIZE DMA Transfer Size. You program this register with the size of the DMA transfer. The maximum DMA transfer size is 4Gbytes. The minimum transfer size is one byte (0x1). This field is automatically decremented by the DMA as the DMA write channel transfer progresses. This field indicates the number bytes remaining to be transferred. When all bytes are successfully transferred the current transfer size is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element. You can read this register to monitor the transfer progress, however in some scenarios this register is updated after a delay. For example, when less than 3 channels are doorbelled, this register is updated only after a descriptor finishes(linked list mode), or the transfer ends (non-linked list mode). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_SAR_LOW_OFF_WRCH_i
Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_LOW Source Address Register (lower 32 bits). Indicates the next address to be read from. The DMA increments the SAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The SAR is the address of the remote memory. DMA Write: The SAR is the address of the local memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_SAR_HIGH_OFF_WRCH_i
Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_HIGH Source Address Register (higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_DAR_LOW_OFF_WRCH_i
Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_LOW Destination Address Register (lower 32 bits). Indicates the next address to be written to. The DMA increments the DAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The DAR is the address of the local memory. DMA Write: The DAR is the address of the remote memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_DAR_HIGH_OFF_WRCH_i
Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_HIGH Destination Address Register (Higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: tru

USP_PCIE_DMA_LLP_LOW_OFF_WRCH_i
Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_LOW Lower bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list after the previous element is consumed. When the current element is a data element; this field is incremented by 6 DWORDS. When the current element is a link element; this field is overwritten by the LL Element Pointer of the element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_LLP_HIGH_OFF_WRCH_i
Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_HIGH Higher 32 bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list as elements are consumed. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_CH_CONTROL1_OFF_RDCH_i
Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	DMA_AT Address Translation TLP Header Bit (AT). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
29:27	RW	0x0	DMA_TC Traffic Class TLP Header Bit (TC). The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
26	RO	0x0	reserved
25	RW	0x0	DMA_RO Relaxed Ordering TLP Header Bit (RO) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
24	RW	0x0	DMA_NS_SRC Source No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MRd (SAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
23	RW	0x0	DMA_NS_DST Destination No Snoop TLP Header Bit. The DMA uses this TLP header field when generating MWr (DAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
22	RW	0x0	DMA_MEM_TYPE Master AXI ACE-Lite Cache Coherency Control. This field sets the DMA channel memory type of the address space of the data transfer as follows: For more details, see "ACE-Lite Features and Limitations" section of the Databook. Irrespective of the value of this field, Linked list descriptor requests have this attribute set to 0x1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x0 (PERIPHERAL): peripheral 0x1 (MEM_TYPE): main memory Value After Reset: 0x0 Testable: writeAsRead Volatile: true
21:17	RO	0x00	reserved

Bit	Attr	Reset Value	Description
16:12	RW	0x00	DMA_FUNC_NUM Function Number (FN). The controller uses this field when generating the requester ID for the MRd/MWr DMA TLP. When you have enabled SR-IOV, then this field is ignored if you have set the VFE field in the DMA Read Channel Control 2 Register (DMA_CH_CONTROL2_OFF_RDCH_0). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
11:10	RO	0x0	reserved
9	RW	0x0	LLE Linked List Enable (LLE). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Values: 0x1 (ENABLE): Enable linked list operation 0x0 (DISABLE): Disable linked list operation Value After Reset: 0x0 Testable: writeAsRead Volatile: true
8	RW	0x0	CCS Consumer Cycle State (CCS). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". You must initialize this bit. The DMA updates this bit during linked list operation. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RO	0x0	CS Channel Status (CS). The channel status bits identify the current operational state of the DMA channel. The operation state encoding for each DMA channel is a s follows: Values: 0x0 (RSVD): Reserved 0x1 (RUN): Running. This channel is active and transferring data. 0x2 (HALT): Halted. An error condition has been detected, and the DMA has stopped this channel. 0x3 (STOP): Stopped. The DMA has transferred all data for this channel, or you have prematurely stopped this channel by writing to the Stop field of the DMA Read Doorbell Register (DMA_WRITE_DOORBELL_OFF) or DMA Read Doorbell Register (DMA_READ_DOORBELL_OFF). Value After Reset: 0x0 Testable: writeAsRead Volatile: true
4	RW	0x0	RIE Remote Interrupt Enable (RIE). You must set this bit to enable the generation of the Done or Abort Remote interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the RIE of the LL element. The RIE bit in a LL element only enables the Done interrupt. In non-LL mode, the RIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
3	RW	0x0	LIE Local Interrupt Enable (LIE). You must set this bit to enable the generation of the Done or Abort Local interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the LIE of the LL element. The LIE bit in a LL element only enables the Done interrupt. In non-LL mode, the LIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
2	RW	0x0	LLP Load Link Pointer (LLP). Used in linked list mode only. Indicates that this linked list element is a link element, and its LL element pointer dwords are pointing to the next (non-contiguous) element. The DMA loads this field with the LLP of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true
1	RW	0x0	TCB Toggle Cycle Bit (TCB). Indicates to the DMA to toggle its interpretation of the CB. Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the TCB of the linked list element. This field is not defined in a data LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

Bit	Attr	Reset Value	Description
0	RW	0x0	CB Cycle Bit (CB). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the CB of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_TRANSFER_SIZE_OFF_RDCH_i
Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_TRANSFER_SIZE DMA Transfer Size. You program this register with the size of the DMA transfer. The maximum DMA transfer size is 4Gbytes. The minimum transfer size is one byte (0x1). This field is automatically decremented by the DMA as the DMA read channel transfer progresses. This field indicates the number bytes remaining to be transferred. When all bytes are successfully transferred the current transfer size is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element. You can read this register to monitor the transfer progress, however in some scenarios this register is updated after a delay. For example, when less than 3 channels are doorbelled, this register is updated only after a descriptor finishes(linked list mode), or the transfer ends (non-linked list mode). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_SAR_LOW_OFF_RDCH_i
Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_LOW Source Address Register (Lower 32 bits). Indicates the next address to be read from. The DMA increments the SAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The SAR is the address of the remote memory. DMA Read: The SAR is the address of the local memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_SAR_HIGH_OFF_RDCH_i
Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_HIGH Source Address Register (higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_DAR_LOW_OFF_RDCH_i
Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_LOW Destination Address Register (Lower 32 bits). Indicates the next address to be written to. The DMA increments the DAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The DAR is the address of the local memory. DMA Read: The DAR is the address of the remote memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_DAR_HIGH_OFF_RDCH_i
Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_HIGH Destination Address Register (higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_LLP_LOW_OFF_RDCH_i
Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_LOW Lower bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list after the previous element is consumed. When the current element is a data element; this field is incremented by 6 DWORDS. When the current element is a link element; this field is overwritten by the LL Element Pointer of the element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

USP_PCIE_DMA_LLP_HIGH_OFF_RDCH_i
Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_HIGH Higher 32 bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list as elements are consumed. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W Value After Reset: 0x0 Testable: writeAsRead Volatile: true

11.4.4.41 USP_PCIE_ELBI Registers Summary

Name	Offset	Size	Reset Value	Description
USP_PCIE_ELBI_APP_ELBI_INT_GEN0	0x0E00	W	0x00000000	ELBI Interface Application Interrupt Generate Register 0
USP_PCIE_ELBI_APP_ELBI_INT_GEN1	0x0E04	W	0x00000000	ELBI Interface Application Interrupt Generate Register 1
USP_PCIE_ELBI_APP_ELBI_INTMSK0	0x0E08	W	0x00000000	ELBI Interface Application Interrupt Mask Register 0
USP_PCIE_ELBI_APP_ELBI_INTMSK1	0x0E0C	W	0x00000000	ELBI Interface Application Interrupt Mask Register 1
USP_PCIE_ELBI_APP_ELBI_USER4	0x0E10	W	0x00000000	ELBI Interface Application User Register 4

Name	Offset	Size	Reset Value	Description
USP_PCIE_ELBI_APP_ELBI_USER5	0x0E14	W	0x00000000	ELBI Interface Application User Register 5
USP_PCIE_ELBI_APP_ELBI_USER6	0x0E18	W	0x00000000	ELBI Interface Application User Register 6
USP_PCIE_ELBI_APP_ELBI_INTSTS	0x0E1C	W	0x00000000	ELBI Interface Application Interrupt Status Register
USP_PCIE_ELBI_APP_ELBI_USER8	0x0E20	W	0x00000000	ELBI Interface Application User Register 8
USP_PCIE_ELBI_APP_ELBI_USER9	0x0E24	W	0x00000000	ELBI Interface Application User Register 9
USP_PCIE_ELBI_APP_ELBI_USER10	0x0E28	W	0x00000000	ELBI Interface Application User Register 10
USP_PCIE_ELBI_APP_ELBI_USER11	0x0E2C	W	0x00000000	ELBI Interface Application User Register 11
USP_PCIE_ELBI_APP_ELBI_USER12	0x0E30	W	0x00000000	ELBI Interface Application User Register 12
USP_PCIE_ELBI_APP_ELBI_USER13	0x0E34	W	0x00000000	ELBI Interface Application User Register 13
USP_PCIE_ELBI_APP_ELBI_USER14	0x0E38	W	0x00000000	ELBI Interface Application User Register 14
USP_PCIE_ELBI_APP_ELBI_USER15	0x0E3C	W	0x00000000	ELBI Interface Application User Register 15

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.4.42 USP_PCIE_ELBI Detail Registers Description

USP_PCIE_ELBI_APP_ELBI_INT_GEN0

Address: Operational Base + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	elbi_app_int_0 Interrupt Status Generation These registers can be set "1" by wire access to generate interrupt to local CPU through ep_elbi_app_int.

USP_PCIE_ELBI_APP_ELBI_INT_GEN1

Address: Operational Base + offset (0x0E04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	elbi_app_int_1 Interrupt Status Generation These registers can be set "1" by wire access to generate interrupt to local CPU through ep_elbi_app_int.

USP_PCIE_ELBI_APP_ELBI_INTMSK0

Address: Operational Base + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	elbi_app_intmsk Interrupt Status Generation These registers can be set "1" by wire access to generate interrupt to local CPU through ep_elbi_app_int.

USP_PCIE_ELBI_APP_ELBI_INTMSK1

Address: Operational Base + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	elbi_app_intmsk Interrupt Status Generation These registers can be set "1" by wire access to generate interrupt to local CPU through ep_elbi_app_int.

USP_PCIE_ELBI_APP_ELBI_USER4

Address: Operational Base + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER5

Address: Operational Base + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER6

Address: Operational Base + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_INTSTS

Address: Operational Base + offset (0x0E1C)

Bit	Attr	Reset Value	Description
31:16	W1C	0x0000	elbi_app_intsts_1 Interrupt Status 1 1'b0: No interrupt 1'b1: Interrupt Write "1" to clear each status bit
15:0	W1C	0x0000	elbi_app_intsts_0 Interrupt Status 0 1'b0: No interrupt 1'b1: Interrupt Write "1" to clear each status bit

USP_PCIE_ELBI_APP_ELBI_USER8

Address: Operational Base + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER9
Address: Operational Base + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER10
Address: Operational Base + offset (0x0E28)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER11
Address: Operational Base + offset (0x0E2C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER12
Address: Operational Base + offset (0x0E30)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER13
Address: Operational Base + offset (0x0E34)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER14
Address: Operational Base + offset (0x0E38)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

USP_PCIE_ELBI_APP_ELBI_USER15
Address: Operational Base + offset (0x0E3C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	app_data Application User Define Information.

11.5 Interface Description

Table 11-10 PCIe IO Usage Model

Signal name	Direction	IO Attribute
BUTTON_RSTN	I	pull down
WAKEN	I/O	Open Drain, pull up
PERSTN	I/O	pull down
CLKREQN	I/O	Open Drain, pull up

Table 11-11 PCIe3_4L G3 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_button_rst_n	I		PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d	BUS_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'h4
pcie_perst_n	I	M0	I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d	BUS_IOC_GPIO0D_IOMUX_SEL_L[3:0] = 4'hc
		M1	BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDOUT_M0/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d	BUS_IOC_GPIO4B_IOMUX_SEL_H[11:8] = 4'h4
		M2	CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[11:8] = 4'h4
		M3	PDM1_SDI3_M1/PCIE30X4_PERSTN_M3/UART4_RX_M2/SPI0_MOSI_M2/GPIO1_B2_d	BUS_IOC_GPIO1B_IOMUX_SEL_L[11:8] = 4'h4
pcie_wake_in/out	I/O	M0	I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d	BUS_IOC_GPIO0C_IOMUX_SEL_H[15:12] = 4'hc
		M1	BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d	BUS_IOC_GPIO4B_IOMUX_SEL_H[7:4] = 4'h4
		M2	CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4] = 4'h4
		M3	PDM1_SDI2_M1/PCIE30X4_WAKEN_M3/SPI0_MISO_M2/GPIO1_B1_d	BUS_IOC_GPIO1B_IOMUX_SEL_L[7:4] = 4'h4
pcie_clkreq_in/out_n	I/O	M0	I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u	BUS_IOC_GPIO0C_IOMUX_SEL_H[11:8] = 4'hc
		M1	CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u	BUS_IOC_GPIO4B_IOMUX_SEL_H[3:0] = 4'h4
		M2	CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0] = 4'h4
		M3	PDM1_SDI1_M1/PCIE30X4_CLKREQN_M3/SPI2_CS1_M0/GPIO1_B0_u	BUS_IOC_GPIO1B_IOMUX_SEL_L[3:0] = 4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 11-12 PCIe3_2L RC G3 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_button_rst_n	I		GMAC1_PPSCLK/PCIE30X2_BUTTON_RSTN/UART7_RX_M1/SPI1_CLK_M1/GPIO3_C1_d	BUS_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'h4
pcie_perst_n	I	M0	I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u	BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0] = 4'hc
		M1	CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_	BUS_IOC_GPIO4B_IOMUX_SEL_L[3:0] = 4'h4

Module Pin	Dir	Group	Pin Name	IOMUX Setting
			B0_d	
		M2	HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d	BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h4
		M3	MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u	BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12] = 4'h4
pcie_wake_in/out	I/O	M0	I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 4'hc
		M1	CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7_d	BUS_IOC_GPIO4A_IOMUX_SEL_H[15:12] = 4'h4
		M2	CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d	BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 4'h4
		M3	MIPI_CAMERA1_CLK_M0/SPDIF0_TX_M0/PCIE30X2_WAKEN_M3/HDMI_RX_HPDOUT_M2/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6_d	BUS_IOC_GPIO1B_IOMUX_SEL_H[11:8] = 4'h4
pcie_clkreq_in/out_n	I/O	M0	I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[7:4] = 4'hc
		M1	CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d	BUS_IOC_GPIO4A_IOMUX_SEL_H[11:8] = 4'h4
		M2	CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d	BUS_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h4
		M3	MIPI_CAMERA4_CLK_M0/PCIE30X2_CLKREQN_M3/HDMI_RX_SDA_M2/I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7_u	BUS_IOC_GPIO1D_IOMUX_SEL_H[15:12] = 4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 11-13 PCIe3_1L0 RC G3 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_button_rst_n	I		MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u	BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4] = 4'h4
pcie_perst_n	I	M0	I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5_u	BUS_IOC_GPIO0C_IOMUX_SEL_H[7:4] = 4'hc
		M1	CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d	GPIO4A_IOMUX_SEL_H[7:4] = 4'h4
		M2	PDM1_CLK0_M1/PCIE30X1_0_PERSTN_M2/UART7_RX_M2/SPI0_CS0_M2/GPIO1_B4_u	BUS_IOC_GPIO1B_IOMUX_SEL_H[3:0] = 4'h4
pcie_wake_in/out	I/O	M0	PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4_d	BUS_IOC_GPIO0C_IOMUX_SEL_H[3:0] = 4'hc
		M1	CIF_D4/BT1120_D4	BUS_IOC_GPIO4A_IOMUX_

Module Pin	Dir	Group	Pin Name	IOMUX Setting
			/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4_d	SEL_H[3:0] = 4'h4
		M2	PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED_M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3_d	BUS_IOC_GPIO1B_IOMUX_SEL_L[15:12] = 4'h4
pcie_clkreq_in/out_n	I/O	M0	PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d	BUS_IOC_GPIO0C_IOMUX_SEL_L[3:0] = 4'hc
		M1	CIF_D3/BT1120_D3/I2S1_SCLK_M0/PCIE30X1_0_CLKREQN_M1/UART0_TX_M2/GPIO4_A3_d	BUS_IOC_GPIO4A_IOMUX_SEL_L[15:12] = 4'h4
		M2	PCIE30X1_0_CLKREQN_M2/UART7_TX_M2/SPI0_CS1_M2/GPIO1_B5_u	BUS_IOC_GPIO1B_IOMUX_SEL_H[7:4] = 4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 11-14 PCIe3_1L1 RC G3 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_button_rst_n	I		CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u	BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8] = 4'h4
pcie_perst_n	I	M0	I2S1_LRCK__M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d	BUS_IOC_GPIO0B_IOMUX_SEL_H[15:12] = 4'hc
		M1	CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/SPI0_CLK_M1/GPIO4_A2_d	BUS_IOC_GPIO4A_IOMUX_SEL_L[11:8] = 4'h4
		M2	PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SPI2_CS0_M0/GPIO1_A7_u	BUS_IOC_GPIO1A_IOMUX_SEL_H[15:12] = 4'h4
pcie_wake_in/out	I/O	M0	I2S1_SCLK_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6_d	BUS_IOC_GPIO0B_IOMUX_SEL_H[11:8] = 4'hc
		M1	CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1_d	BUS_IOC_GPIO4A_IOMUX_SEL_L[7:4] = 4'h4
		M2	PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1_d	BUS_IOC_GPIO1A_IOMUX_SEL_L[7:4] = 4'h4
pcie_clkreq_in/out_n	I/O	M0	I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5_d	BUS_IOC_GPIO0B_IOMUX_SEL_H[7:4] = 4'hc
		M1	CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0_d	BUS_IOC_GPIO4A_IOMUX_SEL_L[3:0] = 4'h4
		M2	PCIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/I2C2_SDA_M4/UART6_RX_M1/SPI4_MISO_M2/GPIO1_A0_d	BUS_IOC_GPIO1A_IOMUX_SEL_L[3:0] = 4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 11-15 PCIe3_1L2 RC G3 Interface Description

Module Pin	Dir	Group	Pin Name	IOMUX Setting
pcie_button_rst_n	I		CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u	BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12] = 4'h4
pcie_perst_n	I	M0	CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d	BUS_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'h4
		M1	BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDM	BUS_IOC_GPIO4C_IOMUX_

Module Pin	Dir	Group	Pin Name	IOMUX Setting
			I_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d	SEL_L[7:4] = 4'h4
pcie_wake_in/out	I/O	M0	CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u	BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0] = 4'h4
		M1	BT1120_D14/PCIE20X1_2_WAKEN_M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0_u	BUS_IOC_GPIO4C_IOMUX_SEL_L[3:0] = 4'h4
pcie_clkreq_in/out_n	I/O	M0	CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[15:12] = 4'h4
		M1	BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7_u	BUS_IOC_GPIO4B_IOMUX_SEL_H[15:12] = 4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

11.6 Application Notes

11.6.1 Clock and Reset

11.6.1.1 Clock Overview

The PCIe module uses multiple clock domains, it consists of system bus clocks (APB and AXI), Core function clock, PIPE interface clock, Power management clock, and PCIe PHY reference clock.

Table 11-16 Clock Overview

Clock Name	Note
pclk/core_clk/pipe_clk	PIPE and Core clock from PHY PLL generated
mstr_aclk	AXI master clock
slv_aclk	AXI slave clock
dbi_aclk	DBI AXI slave clock
aux_clk	Low power clock(24MHz)
apb_clk	APB slave clock for Client

The system bus clock is generated from SOC main PLL internally, please refer to the relative CRU for details. System bus clock gating is handled automatically by PCIe controller

Core function clock is derived from the PIPE interface clock output from the PCIe PHY. In specific low power state, core function clock is gated and switch to Power management clock automatically. After power up, if the PHY is not ready(phystatus is not de-assert), accessing the core through AXI slave will be held until it is ready.

The PHY TX PLL generates PIPE interface clock from the platform reference clock. The PCIe link Training and transaction is completely dependent upon availability of this clock. Application should not initiate transactions before ensuring that the PHY PLL is locked.

The Power management clock which should be fixed with 24MHz driven by crystal input clock. The PCIe controller uses this clock for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value of 24MHz to count real time.

Many PCIe connections, especially backplane connections, require a synchronous reference clock between the two link partners. To achieve this a common clock source, referred to as REFCLK in the PCI Express Card Electromechanical Specification, should be used by both ends of the PCIe link.

11.6.1.2 PCIe PHY Reference Clock

The PHY usually use the external dedicated 100M differential clock as reference clock, the clock should be compatible with the CEM specification.

For low BOM cost usage, In RC mode, PCIe PHY can use internal single-ended clock which can be configured to 24Mhz(Combo PHY), 25Mhz(Combo PHY), 100Mhz(Combo PHY and PCIe 3.0 PHY). Meanwhile, in Combo PHY mode, PCIe PHY can provide differential clock output for system application. The source of differential clock output can be select from internal single-ended clock or PHY TX PLL.

The PCIe 3.0 PHY can use internal SoC 100M reference by setting the ref_use_pad to "0". To get better SI, the unused should be gated.

11.6.1.3 Reset Overview

11.6.1.3.1 Power-On Reset

The power-on reset is used as Cold reset of the PCIe. The entire module is reset when power-on reset is asserted and also generate a phy_rst_n to reset the PHY link. After de-assertion of the power-on reset, the PCIe PHY and PCIe Core function reset keeps until the software release. Software should finish PCIe PHY initialization before de-asserting the power-on reset. The power-on reset is controlled by CRU, the power-on reset is keep asserted until the software de-assert the reset request.

11.6.1.3.2 System reset

The PCIe Controller has the following distinct resets, all of these are configurable through software driver. This section describes the function of each of the reset inputs.

- button_rst_n: Button reset from board if related IO has been used. Please refer to Interface Description section for more information. This reset has an equal functionality with power-on reset.
- perst_n: This reset works as Warm Reset of PCIe if related IO has been used. Please refer to Interface Description section for more information.
- core_rst_n: This is the main reset for the PCIe Controller. It resets all the logic in the core running in the CORE_CLK(partial of PCLK) domain, except for the PMC module. It keeps reset with power-up reset by default. It also should be asserted when Hot Reset or link down reset occurs, but Application software can delay core_rst_n been asserted until system is ready to do core reset. This delayed reset operation will be discussed in next section.
- AXI Reset: All three AXI interface has its own reset input: mstr_aresetn, slv_aresetn, dbi_resetn. Each resets all logic in the specific AXI clock domain. Typically, these resets are be asserted whenever core_rst_n is asserted. Application software shall have the knowledge of choosing an appropriate time to drive this reset in order to avoid times when a transaction is in flight.
- non_sticky_rst_n: Resets all non-sticky bit registers in the configuration register space.
- sticky_rst_n : Resets all sticky bit registers in the configuration register space.
- pwr_rst_n: Resets the PMC module and resets all registers in the PM clock domain, including sticky bits. It is the power-on reset.
- phy_rst_n: output reset signal to reset the PCIe PHY. This reset asserted along with Cold Reset, Warm Reset, Hot Reset.

11.6.1.3.3 Hot Reset and Link-Down Reset

A downstream port (DSP) can hot reset an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. Eventually, the DSP and USP assert link_req_rst_not to request external logic to reset them. Alternatively, during normal operation, the link might fail and go down. After this link-down event, the controller requests the reset module to hot-reset the controller. There is no difference in the handling of a link-down reset or a hot reset.

Hot Reset or Link-down reset cannot be activated before no transaction is appending on system bus. Application software must confirm that system bus is in IDLE state then let the reset operation go on.

To prevent your application from hanging when the controller is reset, the controller must cleanly terminate all transactions that are still in-progress. In AXI configurations with a segmented-buffer Rx queue architecture, the controller automatically executes this process before asserting link_req_rst_not. To disable automatic flushing, set the AUTO_FLUSH_EN field in LINK_FLUSH_CONTROL_OFF to '0'.

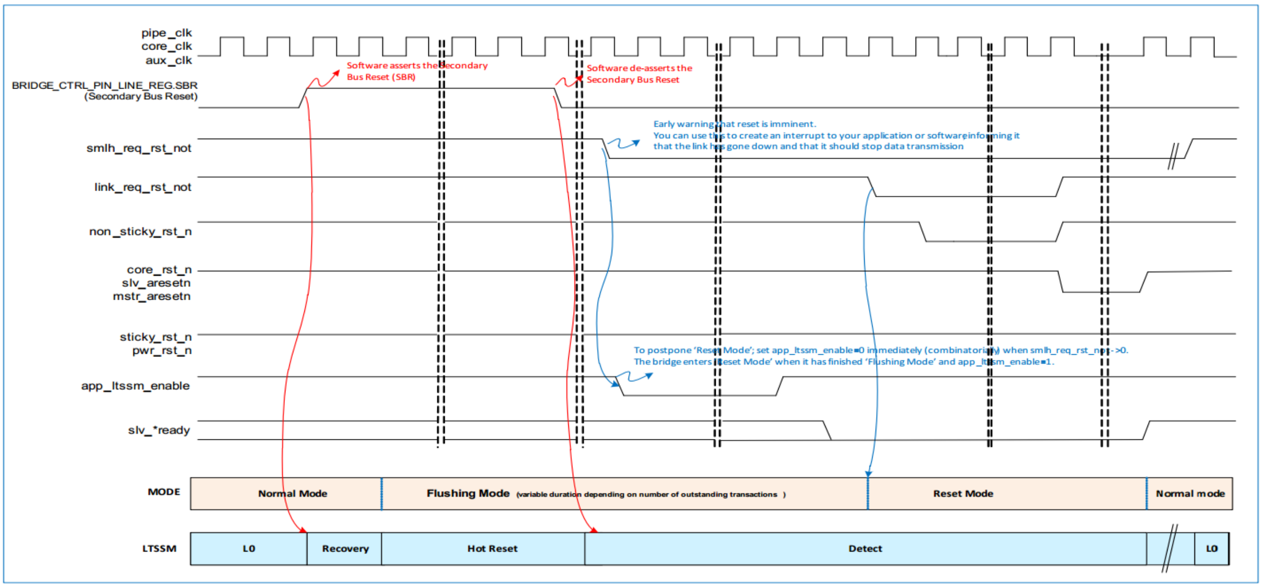

Fig. 11-5 Delaying the PCIe Hot Reset

Figure above illustrates the timing of handling Hot Reset. When Hot Reset or Link-down reset occurs, controller will assert smlh_req_rst_not as an early warning. This warning is an interrupt bit in Client Register group(link_req_rst_not_int). If you want to delay the reset of the controller so that it continues to accept and terminate slave requests, or to read out some register status through the DBI, you must set app_ltssm_enable =0 immediately (combinatorially) after smlh_req_rst_not ->0, as shown in above, this can be achieved by enable the app_dly1_en, app_ltssm_enable will be de-asserted immediately to disable the LTSSM. Then the Hot Reset process is holding on, software then should set the PCIe BIU in IDLE state. This delay will be end-up by asserting app_dly1_done.

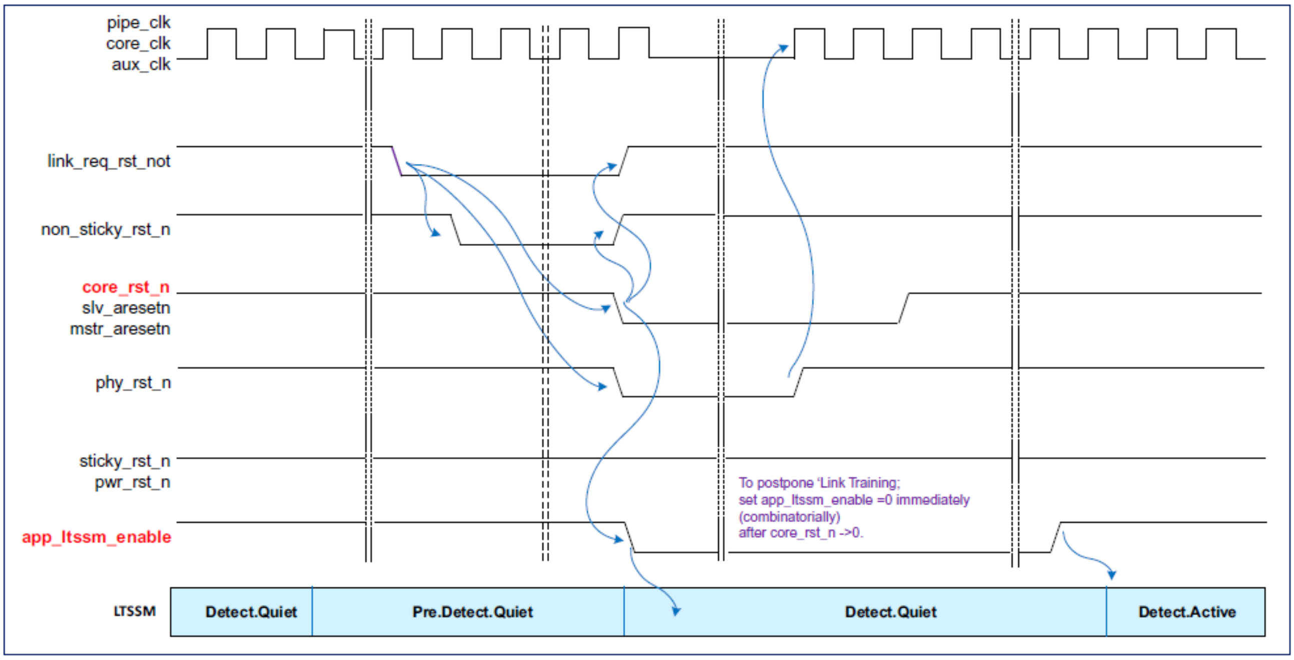

Fig. 11-6 Delaying the Link Training After Hot Reset

If you want to delay link re-establishment (after reset) so that you can reprogram some registers through DBI, you must set app_ltssm_enable =0 immediately after core_rst_n as shown in above. This can be achieved by enable the app_dly2_en, and end-up the delay by assert app_dly2_done.
To be compatible with old version client design, the app_ltssm_enable_enhance is a new

way to control the glue behavior of the app_ltssm_enable. It's advised set app_ltssm_enable_enhance to "1" when the version >= 0x50600. The mechanisms of delaying the Hot reset are available only in app_ltssm_enable_enhance mode.

11.6.2 Initialization

11.6.2.1 Initialization Sequence for RC Mode

The initialization sequence for RC mode is as follows:

1. Configure the IO for CLKREQ# and WAKE# signals. Configure the optional signals button_rst_n and perst_n if they are used. Please refer to section Interface Description for details.
2. De-assert the PCIe 3.0 PHY PMA output clamp(pcie30_clamp_n) if PCIe 3.0 PHY used.
3. If want to change the default pcie30_phy_mode or other critical configurations that need to be followed by phy_reset, please assert pcie30_phy_resetn
4. Configure the CRU registers to provide appropriate reference clock to PCIe PHY if internal reference used. Check all the CRU control registers, such as PLL/DIV/CKG(clock gating), to make sure the reference and other clock is working normally. Please refer to CRU Chapter for more information.
5. Configure Combo PIPE PHY or PCIe 3.0 PHY General Register File, to set PHY working mode, control the unused PIPE signals and initialize the PHY, the source of the reference or output the differential reference clock.
6. De-assert the PCIe 3.0 pcie30_phy_resetn if necessary
7. Sometimes, it is also necessary to configure the PHY internal register to adjust some analog trim.
8. De-assert the power-up reset of PCIe Controller. Delay some time or wait PLL lock if the PLL lock flag is accessible.
9. Set the app_ltssm_enable_enhance to enable enhance control mode of app_ltssm_enable
10. Initialize the device_type as Root Complex. You can program Client and controller registers before Link training start if necessary. Link training can be initialed by setting ltssm_enable bit in register PCIE_CLIENT_GENERAL_CON to 1. Link training success will set phy_link_up_int to 1. And if data flow initialization success, dll_link_up_int interrupt status bit will be set to 1. These two bits can be polled in LTSSM_STATUS or GENERAL_DEBUG_INFO, besides, it can be informed by interrupt optionally. The controller tries to linkup at maximum Link width/speed, if you want to resize or change speed, please refer to internal application document about speed changing and lane resizing. It is strongly recommended that set direct_speed_change bit to 1 in PL_GEN2_CTRL_OFF before link training.
11. Software emulation and initialization.
12. Writes to Bus Master Enable (BME), Memory Space Enable (MSE), then application can start application traffic generation.

11.6.2.2 Initialization Sequence for EP Mode

The initialization sequence for EP mode is similar with Root Complex, except:

- Normally, perst_n is input for EP device if it is used.
- The reference clock of PHY is normally provided by mother board.
- The device_type to EP mode.
- EP doesn't do emulation.

11.6.2.3 SRIS Mode

Software can enable support for the Separate Refclk with Independent Spread Spectrum Clocking (SRIS) feature as defined by the PCI Express Base Specification, Revision 5.0, Version 1.0, by setting CX_SRIS_SUPPORT =1. This also populates the app_sris_mode input pin. When CX_SRIS_SUPPORT =1 and app_sris_mode =1, then L0s is not supported and must not be advertised in the ASPM Support Capability Registers.

The SRIS mode is only support when controller interfaces with PCIe 3.0 PHY that supports SRIS. Software should initialize the controller and PHY by setting below registers before power-up the PHY.

- app_sris_mode in Client.
- Set rxX_sris_mode_en to “1”, and rxX_cmn_refclk_mode to “0” in PCIe 3.0 PHY GRF

11.6.2.4 Tie Off Unused Lanes

N/A
It is automatically implemented by hardware.

11.6.3 Address Translation

The controller uses the internal Address Translation Unit(iATU) to implement a local address translation scheme that replaces the TLP address and TLP header fields in the current TLP request header.

The iAUT has several inbound Address Translation regions and several outbound Address Translation regions. The minimum size of an Address Translation Region is 64k and the maximum size of an Address Translation Region is 4G.

11.6.3.1 Outbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The ATU also supports type translation. Without address translation, your application address is passed unmodified to the TLPs directly through the Tx application interface. You can program the iATU to implement your own outbound address translation scheme. The outbound features are as follows:

- Address Match mode operation for MEM and I/O, CFG, and MSG TLPs. No translation for completions.
- Supports type translation through TLP type header field replacement for MEM or I/O types to MSG/CFG types.
- Programmable TLP header field replacement. Including TYPE, TC, AT, ATTR, MSG-Code, TH, PH, ST.
- Multiple (up to 16) address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- Configuration Shift mode. Optimizes the memory footprint of CFG accesses destined for the Rx application interface in a multifunction device.
- Response code which defines the completion status to return for accesses matching a region.
- Supports regions from 64 KB to 4 GB in size.
- Payload Inhibit marks all TLPs as having no payload data.
- Header Substitution replaces bytes 8 to 11 (for 3 DWORD header) or bytes 12 to 15 (for 4 DWORD header), inclusive, of the outbound TLP header.
- Tag Substitution of the outbound TLP tag field.
- Function number bypass mode to allow function number information to be supplied from your application transmit interface while translating the address and other attributes of the TLP.
- DMA bypass mode to allow TLPs which are initiated by the embedded DMA engine, to pass through the iATU untranslated.

11.6.3.2 Outbound Basic Operation

The address field of each request MEM and I/O TLP is checked to see if it falls into any of the enabled address regions defined by the Start and End addresses as defined in Figure below. When an address match is found, then the TLP address field is modified as follows:

Translated Address = Original Address - Base Address + Target Address

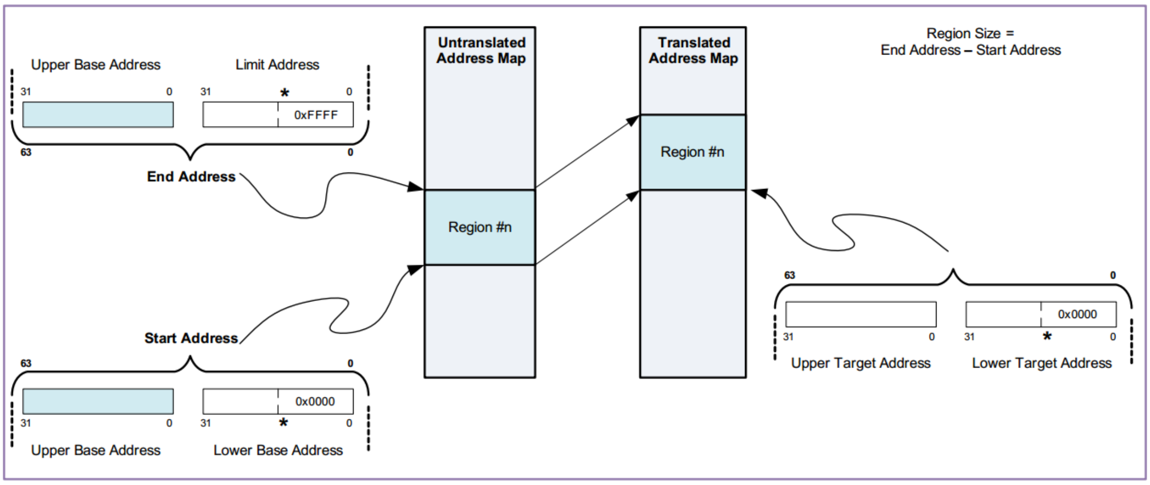

Fig. 11-7 PCIe Hot Reset Control Structure

The TYPE, TC, AT, TH, PH, ST, Function Number, and ATTR header fields are replaced with the corresponding fields in the IATU_REGION_CTRL_1_OFF_OUTBOUND_0 register. When your application address field matches more than one of the CX_ATU_NUM_OUTBOUND_REGIONS address regions, then the first (from lowest number 0) enabled region to be matched is used. For details on what happens when there is no address match, see "No Address Match Result". This operational mode (called Address Match Mode) is always used for outbound translation.

The minimum size of an address translation region is 64KB. So, the lower 16 bits of the Base, Limit, and Target registers are zero and all address regions are aligned on 64 KB boundaries.

11.6.3.3 Outbound Detailed Operation

11.6.3.3.1 RID BDF Number Replacement

When there is a successful address match on an outbound TLP, then the function number used in generating the function part of the requester ID field of the TLP is taken from the 3-bit Function Number field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_iregister. The value in this field must be 0x0 unless multifunction operation in the controller is enabled. To override this behavior, use the "Function Number Translation Bypass Feature" described later.

11.6.3.3.2 iATU Outbound MSG Handling

The iATU supports TYPE translation/conversion of MEM and I/O TLPs to Msg/MsgD TLPs. This supports applications that are unable to directly generate Msg/MsgD TLPs. When there is a successful address match on an outbound MEM TLP, and the translated TLP type field is MSG (that is, the type field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i register is 10xxx), then the message code field of the TLP is set to the value in the Message Code field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.A Memory Write with an effective length of '0' is converted to Msg and all other MWr TLPs are converted to MsgD.

11.6.3.3.3 MEM-CFG Type Translation

The iATU supports translation of I/O and MEM TLPs to CFG TLPs. This is useful for applications that are unable to generate CFG TLPs. The 16-bit BDF is located at bits [31:16] of the translated address where:

Translated Address = Original Address - Base Address + Target Address

As an example:

Original Address[31:16] = {13h0,function_no[2:0]}
Base Address[31:16] = 16h0
Target Address[31:16] = {bus_no[7:0],device_no[4:0],3h0}

then:

Translated Address[31:16] = BDF ={bus_no[7:0], device_no[4:0], function_no[2:0]}

To handle eight functions (as the previous example indicates), you should use a 19-bit wide region size. For CFG transactions created directly by your application (asopposed to the iATU), you must ensure that the BDF field does not match any programmed iATU address region or else unintentional type translation could occur.

11.6.3.3.4 CFG Shift Feature

This feature is enabled by setting the CFG_SHIFT_MODE field the IATU_REGION_CTRL_2_OFF_OUTBOUND_0 register. The iATU uses bits [27:12] of the original address to form bits [31:16] (BDF location) of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space.

11.6.3.3.5 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeros in the upper 32 bits of the translated address. Otherwise, it sets it to four DWORDs when it detects a 64-bit address (that is, when there is a '1' in the upper 32 bits of the translated address). When the original address and the translated address are of different format, the iATU ensures that the TLP header size matches the translated address format.

11.6.3.3.6 Invert Feature

In normal operation an address match on an outbound TLP occurs when the untranslated address is in the region bounded by the base address and limit address. When the invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the base address and limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.

11.6.3.3.7 DMA Bypass Feature

When you do not want the iATU to translate outbound requests that are generated by the DMA, you must implement one of the following approaches:

- Ensure that the combination of DMA channel address programming and iATU control register programming causes no translation of DMA traffic to be done in the iATU.
- Activate the DMA bypass mode to allow request TLPs which are initiated by the embedded DMA controller to pass through the iATU untranslated. You can activate the DMA bypass mode by setting the DMA Bypass field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_i register to 1.

11.6.3.3.8 Function Number Translation Bypass Feature

In this mode the function number of the translated TLP is taken from your application transmit interface and not from the Function Number field of the REGION_CTRL_1_OFF_OUTBOUND_i register. You can activate the function number bypass mode by setting the Function Number Translation Bypass Enable field in the IATU_REGION_CTRL_2_OFF_OUTBOUND_i to '1'.

11.6.3.3.9 General Bypass

Application can program PCIE_CLIENT_AXI_SLV_ATU_BYPASS register to do general ATU bypassing. Note that you should make sure that there is no transfer pending before you program this register.

11.6.3.3.10 Header Substitution (Tx)

When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. The expected usage scenario is for Vendor Defined Msg/MsgD and ATS transactions over the AXI bridge which is normally inefficient requiring a very large iATU region. Enabled using the HEADER_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

11.6.3.3.11 Tag Substitution (Tx)

When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Enabled using the TAG_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

Your application must not attempt to perform TAG substitution for outgoing non-posted TLPs.

Note: If the iATU is programmed to allow a TLP to be matched to more than one iATU outbound regions, the Function Number Translation Bypass field of the

IATU_REGION_CTRL_2_OFF_OUTBOUND_i register should be same for every region where that TLP can be matched.

11.6.3.4 Outbound Programming Example

Define Outbound Region 1 as:
64 KB I/O region from 0x80000000_d000000to 0x80000000_d000ffff, to be mapped to 0x00010000in the PCIe I/O space.

1. Setup the Region Base and Limit Address Registers.
   Write 0xd0000000to Address {0x208} to set the Lower Base Address.
   Write 0x80000000to Address {0x20C} to set the Upper Base Address.
   Write 0xd000ffff to Address {0x210} to set the Limit Address.
2. Setup the Target Address Registers.
   Write 0x00010000to Address {0x214} to set the Lower Target Address.
   Write 0x00000000to Address {0x218} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
   Write 0x00000002to Address {0x200} to define the type of the region to be I/O.
4. Enable the region.
   Write 0x80000000to Address {0x204} to enable the region.

11.6.3.5 Inbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The iATU supports type translation. Without address translation, your application address is passed from the TLPs directly through the AXI application interface. You can program the iATU to implement your own inbound address translation scheme without external logic.

- Programmable Match mode operation for MEM, I/O, CFG, and MSG TLPs. No translation for completions.
- Selectable BAR Match mode operation for I/O and MEM TLPs:
  - TLPs destined for the internal CDM (or ELBI) in an upstream port are not translated.
  - TLPs that are not error-free (ECRC, malformed and so on) are not translated.
- Programmable TLP header field matching:
  - TYPE/TD/TC/AT/ATTR/MSG-Code/TH/PH/ST
  - Function Number
- Multiple address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- ECAM Configuration Shift mode to allow a 256 MB CFG1 space to be located anywhere in the 64-bit address space.
- Supports regions from 64 KB to 4 GB in size.
- Single Address Location to allow all TLPs to be translated to a single address location.
- Msg Type Match Mode to allow matching of any TLP of type Message.

11.6.3.6 Inbound Basic Operation

11.6.3.6.1 Overview

The following translation rules and limitations apply:

- When there is no match, then the address is untranslated. In addition
- TLPs destined for the internal registers in an upstream port are not translated.
- TLPs that are not error-free (ECRC, malformed and so on) are not translated.
- Address translation of all TLP types (MEM, I/O, CFG, and MSG) except completion is supported in Address Match mode. In BAR Match mode, only translation of I/O and MEM is supported.

The setting of the MATCH_MODE field in IATU_REGION_CTRL_2_OFF_INBOUND_0 determines how iATU inbound matching is done for each TLP type.

Table 11-17 Determination of Match Mode

TLP Type	MATCH_MODE =0	MATCH_MODE =1
MEM or I/O	Address Match Mode	BAR Match Mode
CFG0	Routing ID Match Mode	Accept Mode
MSG/MSGD	Address Match Mode	Vendor ID Match Mode

11.6.3.6.2 I/O and MEM Match Modes

Inbound address translation for I/O and MEM TLPs operates in one of two matching modes as determined by the "Inbound Match Mode" field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register.

Address Match Mode:

The operation is similar to "Outbound Basic Operation (Address Match Mode)". The address field of each request TLP is checked to see if it falls into any of the enabled address regions. When an address match is found then the TLP address field is modified as follows:

Address = Address - Base Address + Target Address

BAR Match Mode:

Looking for an address match is a two-step process.

1. The standard internal PCI Express BAR Matching Mechanism checks if the address field of any MEM and I/O request TLP falls into any address region defined by the enabled BAR addresses and masks.
2. When a matched BAR is found, then the iATU compares the BAR ID to the BAR Number field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register for all enabled regions. Figure below provides more details on inbound translation in BAR Match Mode.

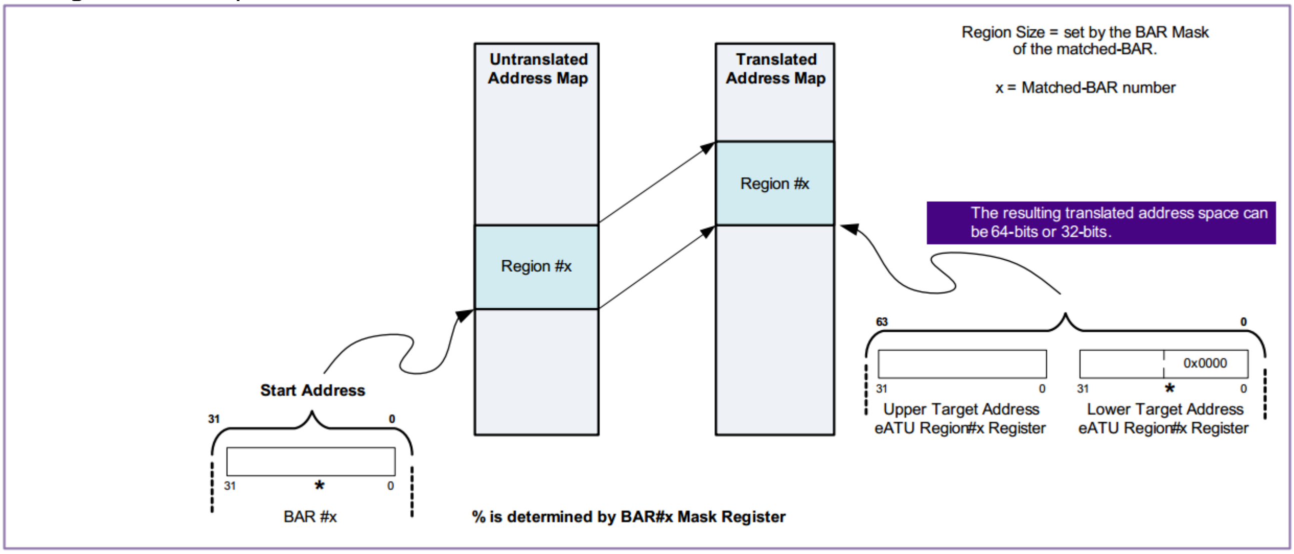

Fig. 11-8 Inbound BAR Match Mode

11.6.3.7 Inbound Detailed Operation

11.6.3.7.1 Single Address Location

When enabled and region address is matched, the TLPs can be translated to a single address location as determined by the target address register of the iATU region. This feature can be enabled using the SINGLE_ADDR_LOC_TRANS_EN field in IATU_REGION_CTRL_2_OFF_INBOUND_i. This feature is useful for translating messages on AXI bridge.

11.6.3.7.2 CFG Handling (Upstream Port)

The controller normally routes CFG TLPs (to the internal CDM or ELBI) without translation. The iATU only translates CFG0 TLPs that the controller has routed to the TRGT1. Inbound address translation for CFG0 TLPs operates in one of two matching modes as determined by the Inbound CFG0 Match Mode field in the IATU_REGION_CTRL_2_OFF_INBOUND_i register.

Accept Mode

The controller always accepts CFG0 TLPs even when the CFG bus number does not match the current bus number of the device. This mode follows that behavior. The routing ID of received CFG0 TLPs are ignored when determining a match.

Routing ID Match Mode

The operation is similar to “Outbound Basic Operation (Address Match Mode)”. The routing ID of the inbound CFG0 TLP must fall within the Base and Limit of the defined iATU region for matching to proceed. The iATU interprets the routing ID (Bytes1 8-11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM and I/O transactions.

CFG Shift Feature

Inbound CFG transactions routed to the Rx application interface can exist anywhere in address space, because the PCIe controller filter processes the routing ID (BDF) as bits [31:16] of an address. This BDF changes according on the PCIe bus topology. A compressor feature (CFG Shift Feature) can be enabled by setting the CFG Shift bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Bits [15:12] of the third DWORD1 of CFG TLPs are reserved. The compressor feature uses this fact to reduce the memory requirement. This shifts/maps the BDF (bits [31:16] of the third header DWORD, which would be matched against the Base and Limit addresses) of the incoming CfgRd0/CfgWr0 down to bits [27:12] of the translated address.

11.6.3.7.3 Optional Matching Fields

In address and BAR match modes, a successful address/BAR match can be optionally gated by successful matching of the following programmable TLP header fields (per region):

- TYPE/TD/TC/AT/ATTR/TH/PH/ST
- MSG Code (MSG TLPs only)
- Function number (MEM, I/O, or CFG TLPs only)
- Virtual function number (MEM or I/O TLPs only)

For each of the previous fields in the IATU_REGION_CTRL_1_OFF_INBOUND_i register, there is an associated Match Enable bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Address translation only proceeds when compares on all enabled field are successful.

11.6.3.7.4 Response Code Feature

When the Response Code field of the IATU_REGION_CTRL_REG_2_INBOUND_i register is set to a value other than 00, the controller uses it to determine the completion status field of completion TLPs sent in response to successfully match non-posted TLPs. This can be set to unsupported request (UR) or completer abort (CA). When the error response field is set to 2b00, then the normal receive filter response for this TLP is used.

11.6.3.7.5 Inbound MSG Handling

Inbound message (Msg/MsgD) transactions can use one of two matching modes:

Address Match Mode

The third and fourth header DWORDs are treated as an address and are compared against the iATU Region Base and Limit Address registers. For vendor defined messages this allows specific messages to be filtered into memory at the target address. The Upper Base address should be set to BDF and Vendor ID. The Lower Base address can be used as a filter for specific messages.

Vendor ID Match Mode

This mode is relevant for ID-routed vendor defined messages. The iATU ignores the routing ID (BDF) in bits [31:16] of the third DWORD of the TLP header1 but compares it against the vendor ID in bits [15:0] of the third DWORD of the TLP header (bytes1 10 and 11). This

allows vendor defined messages to be filtered against specific vendor IDs without needing to know the BDF number which might vary depending on the PCI topology. Bits [15:0] of the Region Upper Base register should be programmed with the required vendor ID as follows:
Region Upper Base [15:8] =byte 10
Region Upper Base [7:0] =byte 11
The lower base and limit register should be programmed to translate TLPs based on vendor-specific information in the fourth DWORD of the TLP header.

11.6.3.7.6 Msg Type Match Mode

Inbound message (Msg/MsgD) transactions can also use Msg Type Matching mode. When this mode is enabled and Single Address Location is enabled, the iATU matches Msg TLP Type field with TYPE field of IATU_REGION_CTRL_1_OFF_INBOUND_i register.

If Fuzzy Type Match Mode is also enabled, then any Msg received will be matched (that is, Msg Type's sub-field r[2:0], which specifies the Message routing mechanism, is ignored). The Message should be consumed by your application before the next message arrives as all messages go to the same address.

If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is set for any region, then you must ensure that the same TLP cannot be matched in any other region where SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is not set. If this happens radm_trgt1_hdr_uppr_bytes could have incorrect data.

11.6.3.7.7 Fuzzy Type Match Mode

When enabled, the iATU relaxes the matching of the TLP type field against the expected type field so that:

- CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1.
- MWr, MRd and MRdLk TLPs are seen as identical.
- The routing field of MsgD TLPs is ignored.
- Atomic Ops TLPs-FetchAdd, Swap, and CAS are seen as identical.

For example, CFG0 in the type of field in the IATU_REGION_CTRL_1_OFF_INBOUND_i register matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. To enable this feature, set the Fuzzy Type Match Mode bit of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

11.6.3.7.8 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeroed in the upper 32 bits of the translated address. Otherwise, it sets it to four DWORDs when it detects a 64-bit address (when there is a 1 in the upper 32 bits of the translated address). When the original address and the translated address are of a different format then the iATU ensures that the TLP header size matches the translated address format.

11.6.3.7.9 Invert Feature

Normally an address match on an inbound TLP occurs when the untranslated address is in the region bounded by the Base address and Limit address. When the Invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the Base address and Limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

11.6.3.8 Inbound Programming Example

You must not update the iATU registers while operations are in progress on the AXI bridge slave interface.

Example 1:

Define Inbound Region 2 as: MEM region matching BAR4 (BAR match mode) mapping to 0x8000_0000_2000_0000 in your application memory space
1. Setup the Target Address Registers.
   Write 0x20000000 to Address {0x508} to set the Lower Target Address.
   Write 0x80000000 to Address {0x50C} to set the Upper Target Address.
2. Configure the region through the Region Control 1 Register.

Write 0x00000000 to Address {0x500} to define the type of the region to be MEM.
3. Enable the region for BAR Match Mode.
Write 0xC0000400 to Address {0x504} to enable the region for BAR match mode for BAR#4.

Example 2:

MEM region matching TLPs with addresses in the range 0x00010000 to 0x0005ffff mapped to 0x2000_0000 - 0x2004_ffff in your application memory space.
1. Setup the Region Base and Limit Address Registers.
Write 0x00010000 to Address {0x108} to set the Lower Base Address.
Write 0x00000000 to Address {0x10C} to set the Upper Base Address.
Write 0x0005ffff to Address {0x110} to set the Limit Address
2. Setup the Target Address Registers.
Write 0x20000000 to Address {0x114} to set the Lower Target Address.
Write 0x10000000 to Address {0x118} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
Write 0x00000000 to Address {0x100} to define the type of the region to be MEM.
4. Enable the region.
Write 0x80000000 to Address {0x104} to enable the region in address match mode

11.6.4 PCIe Embedded DMA

11.6.4.1 PCIe DMA Overview

The RC system CPU, or the EP application CPU, can off load the transfer ring of large blocks of data to the embedded DMA controller, leaving the CPU free to perform other tasks. The DMA is configured to have 2 read channels and 2 write channels. It can simultaneously perform the following types of memory transactions:

DMA write
Transfer (copy) of a block of data from local memory to remote memory.
DMA read
Transfer (copy) of a block of data from remote memory to local memory.

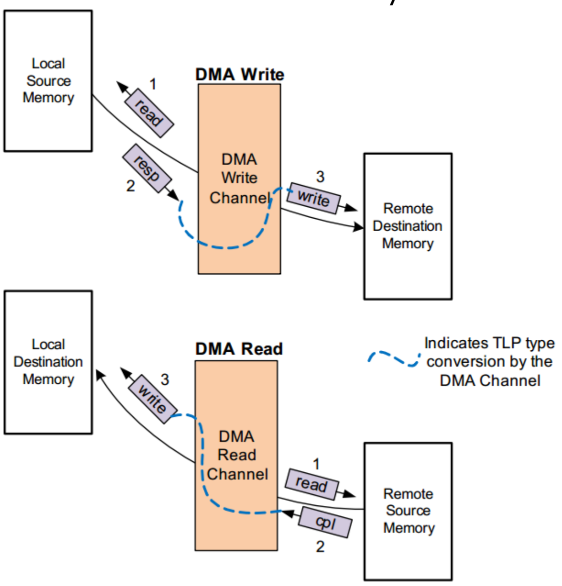

Fig. 11-9 System Level View of PCIe Embedded DMA

Therefore, the DMA supports full duplex operation, processing read and write transfers at the same time, and in parallel with normal (non-DMA) traffic. Upon completion of a DMA transfer or an error, the DMA optionally interrupts the local CPU or sends an interrupt MWr (IMWr) to the remote CPU. The DMA is highly configurable, and you can program it using the local DBI or over the PCIe wire.

In linked list mode, the DMA fetches the transfer control information (called channel context) for each transfer (block), from a list of DMA elements that have constructed in local memory.

11.6.4.2 Interrupts and Error Handling

The DMA generates two interrupts, read channel interrupt and write channel interrupt. Each of them can be caused by one of the two reasons:

Done: The DMA successfully completes the transfer.

Abort: The DMA fails to complete the transfer, or an error occurs during the transfer.

The interrupts are signaled to the software on your CPU, using one or both of the following mechanisms:

- Locally through the edma_rd_int or edma_wr_int field of PCIE_CLIENT_INTR_STATUS_MISC register.
- Remotely using a posted memory write (IMWr), which can be interpreted as an MSI or MSIX when directed toward the RC.

For remote interrupt, there are two programmable IMWr addresses per channel, one each for the done and abort interrupts. For MSI, you must program all IMWRr address registers with the same MSI address, as PCIe only supports a single MSI address per function.

A single IMWr data register is used for both types of interrupts, so you must read DMA_READ_INT_STATUS_OFF(or DMA_WRITE_INT_STATUS_OFF) to identify the interrupt type.

The interrupt handling mechanism is different for linked list (LL) mode (than non LL mode), and there are also some differences between the read and write channels.

11.6.4.2.1 Non Linked List Mode Interrupt Handling

You enable the local and remote interrupts through the local and remote interrupt enable (LIE and RIE) bits: DMA_CH_CONTROL1_OFF_WRCH_0.lie and DMA_CH_CONTROL1_OFF_WRCH_0.rie.

In the write channel, there is only one error condition that results in an abort interrupt. For more details, see “Linked List Mode” on next section. You mask, clear, and read the status of each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below:

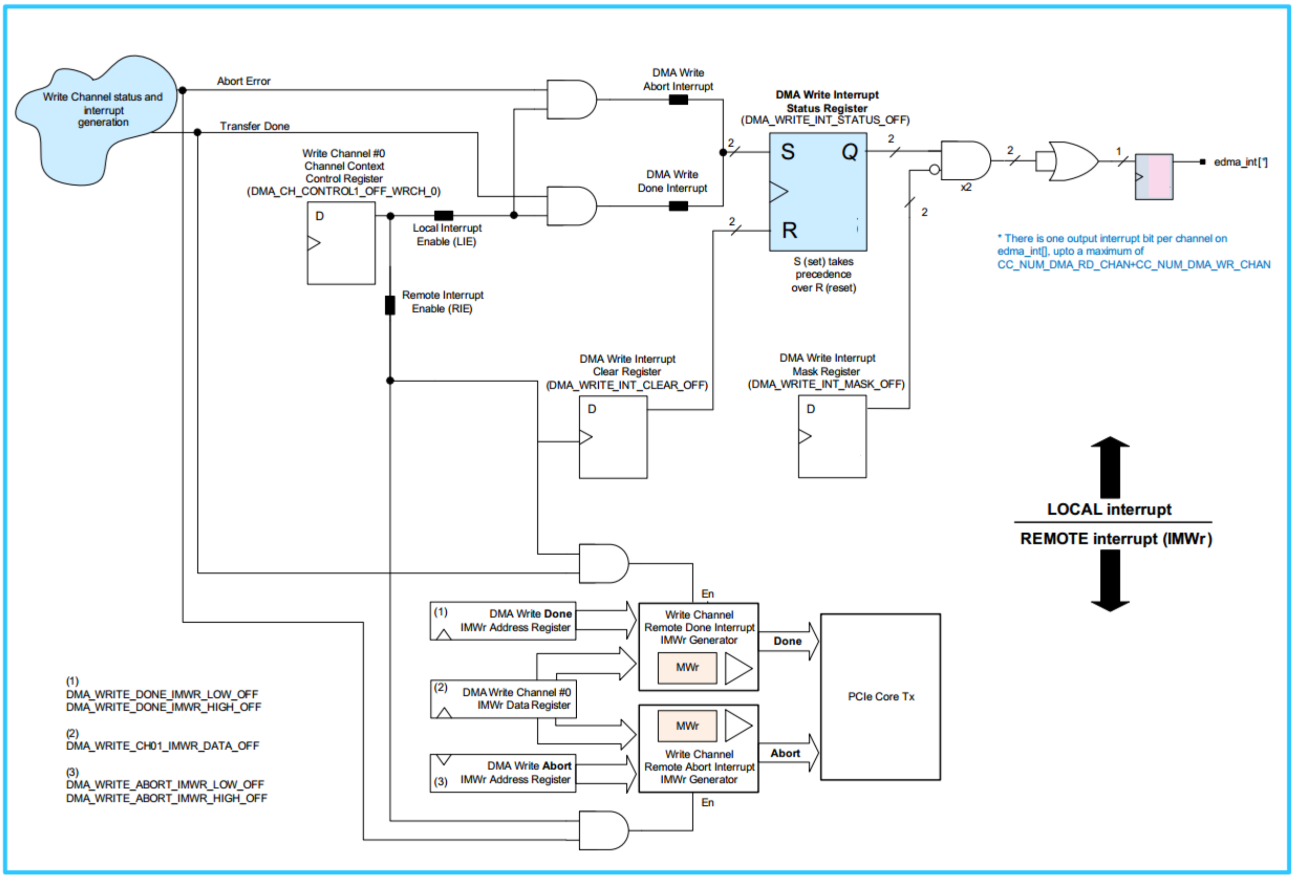

Fig. 11-10 Write Interrupt Generation - Non Linked List Mode

In the read channel, there are five error conditions that results in an abort interrupt. For more details, see “Linked List Mode” on next section. You mask and clear each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below. However, you can read the status of each of the five abort errors (that contribute to the abort interrupt) through DMA_READ_ERR_STATUS_LOW_OFF and DMA_READ_ERR_STATUS_HIGH_OFF.

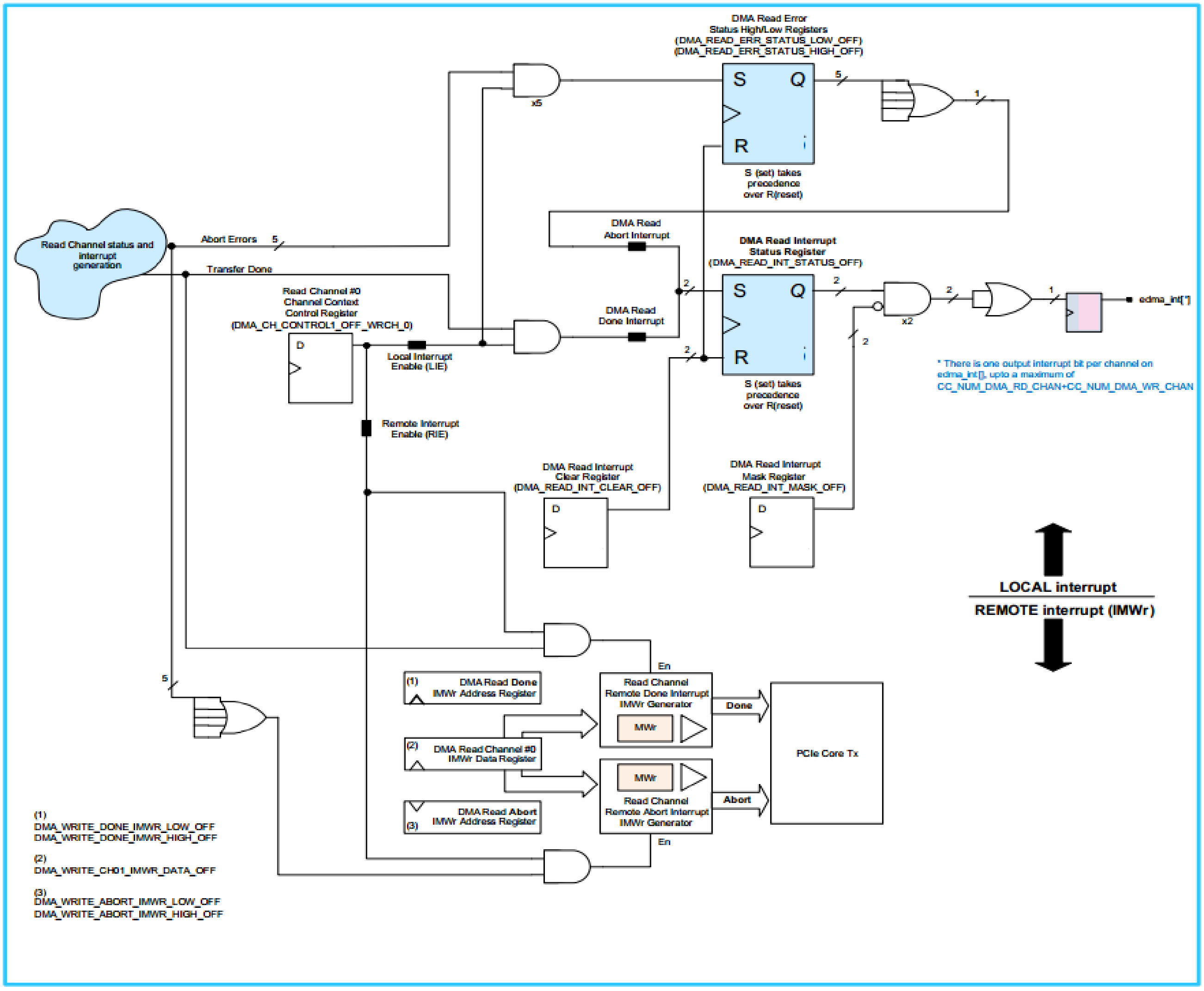

Fig. 11-11 Read Interrupt Generation - Non Linked List Mode

11.6.4.2.2 Linked List Mode Interrupt Handling

The LIE and RIE bits in the LL element enable the channel done interrupts (local and remote). The LLLAIE and LLRAIE bits of the DMA_WRITE_LINKED_LIST_ERR_EN_OFF and DMA_READ_LINKED_LIST_ERR_EN_OFF registers enable the channel abort interrupts (local and remote). In the write channel, there are two error conditions that results in an abort interrupt. For more details, see "Linked List Mode" on next section. You mask and clear each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below. You can read the status of each of the two abort errors (that contribute to the abort interrupt) through the DMA_WRITE_ERR_STATUS_OFF register.

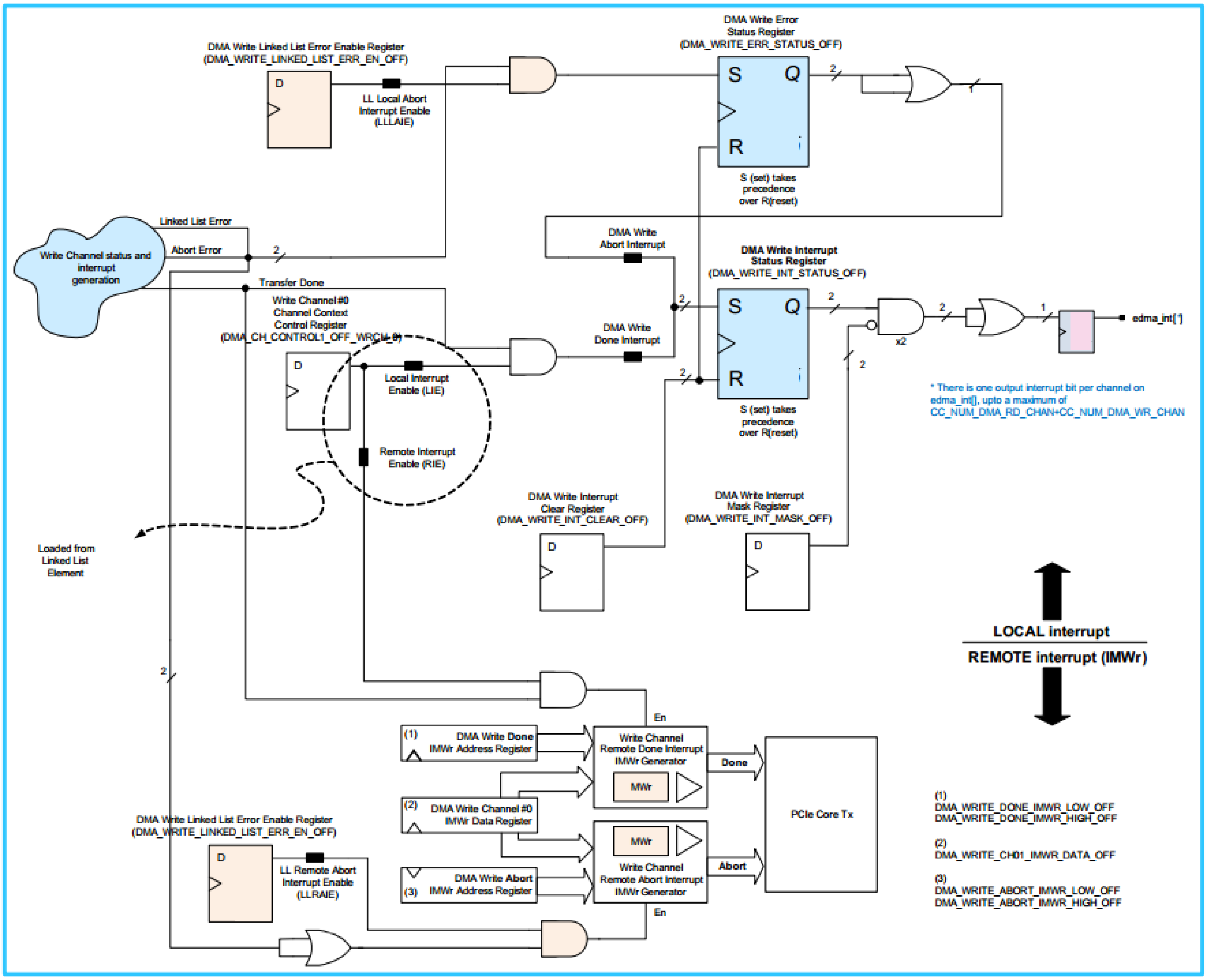

Fig. 11-12 Write Interrupt Generation - Linked List Mode

In the read channel, there are six error conditions that results in an abort interrupt. For more details, see "Linked List Mode" on next section. You mask and clear each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below. You can read the status of each of the six abort errors (that contribute to the abort interrupt) through the DMA_READ_ERR_STATUS_LOW_OFF and DMA_READ_ERR_STATUS_HIGH_OFF registers.

In non-linked list mode, LIE acts as a global switch. However, when in linked list mode, LIE is just local to the current linked list element and the global switch is LLLAIE.

If the DMA driver is running on the host and the interrupt service routine is reading local interrupts to determine if the transfer is successful, then you must set LIE and RIE in the same element and you should mask or ignore the local interrupt pin. Setting RIE and LIE in element A followed by RIE (only) in element B is not a verified usage scenario.

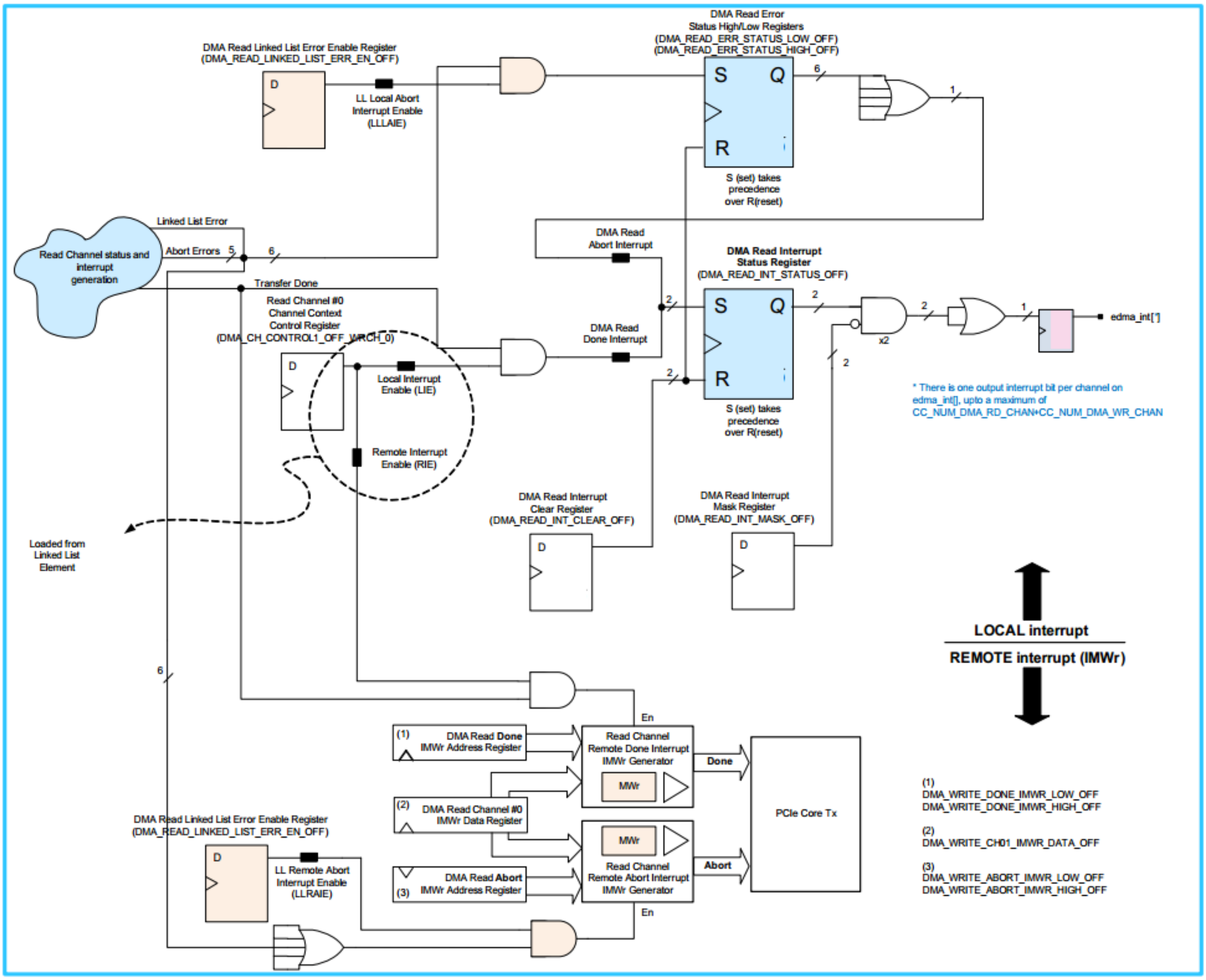

Fig. 11-13 Read Interrupt Generation - Linked List Mode

11.6.4.3 Linked List Mode

The DMA provides a linked list (LL) mode to efficiently move data from source to destination with minimal intervention from the local CPU. This mode provides an alternative to programming the DMA multiple times to transfer multiple blocks of data. The programming information (address, size, and so on) for each block of memory is pre-programmed by your software into a LL element (also known as a descriptor) in local memory. Each element (called a data element) in the LL structure (called a transfer list) can transfer up to 4 GB of data.

You enable LL operation for a channel, by setting the LLE field of the DMA_CH_CONTROL1_OFF_[WRCH|RDCH]_0 register to 1. Your application must produce the LL element structure in local memory as shown in figure below. Normally, all of the elements are contiguous (one after the other) in memory, and each element has six DWORDs containing the information about the block of data to be transferred. You program the channel context registers (DMA_LLP_LOW_OFF_WRCH_0 and DMA_LLP_HIGH_OFF_WRCH_0) with the location of where you have placed the LL element structure in local memory.

When you start the DMA transfer (by writing to the DMA Write Doorbell Register DMA_WRITE_DOORBELL_OFF or DMA Read Doorbell Register DMA_READ_DOORBELL_OFF), the DMA reads (consumes) each element from local memory, and loads the information (SAR, DAR, size, and so on) from that element into the channel context registers in the DMA. These channel context registers determine the operation of the channel that the DMA controller is currently servicing. The DMA then proceeds to transfer the block of data (as defined by the element), and when it is finished, reads the next element from local memory.

Normally, all of the elements are contiguous (one after the other) in memory, with the starting address defined in the channel context DMA Linked List Pointer Low Register DMA_LLP_LOW_OFF_WRCH_0.

When you want to jump in local memory to another element list (or recycle the consumed elements), then you set the LLP bit in the element (for example, link element #N-1 in figure below), specify the location of the next element structure using the LL Element Pointer DWORDs, and, set TCB to 1 (for recycling) or to 0 (to jump to another list).

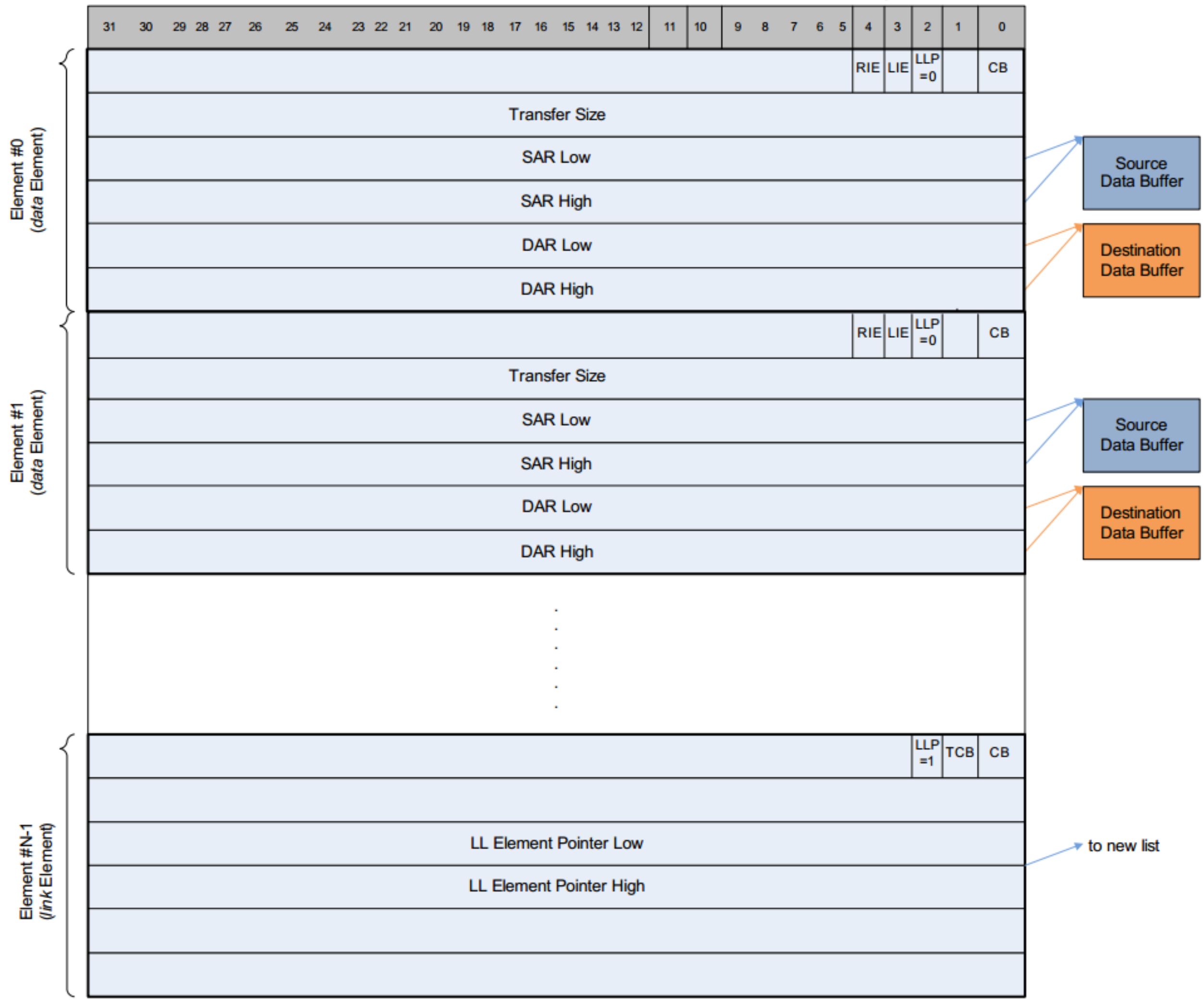

Fig. 11-14 Linked List Element/Descriptor Structure in Local Memory

11.6.4.3.1 LL Element and Channel Context Registers

Notice the similarity between a data element and the DMA Channel Context registers for each channel. Each element has six DWORDs as in Figure 9-6. There are eight channel context registers (DWORDs) for a channel. The DMA loads the six element DWORDs into the following channel context:

- CB, LLP, LIE, and RIE fields of the DMA Channel Control 1 register
- DMA Transfer Size
- DMA SAR Low and DMA SAR High
- DMA DAR Low and DMA DAR High

The definitions of the element DWORD bit fields are the same as the DMA Channel Context registers described in the register section, with the exception of the LIE and RIE bits. The LIE and RIE bits in a LL element, only enable the done interrupt. In non-LL mode, the RIE and LIE bits (in the channel context registers) enable the done and abort interrupts.

11.6.4.4 Flow Control

11.6.4.4.1 Overview

This optional feature is available only for those channels which are configured to operate in linked list (LL) mode. It enables your application to flow control the DMA controller by using

PCIE_CLIENT_DMA_HSHAKE_TOGG register, that is, your application determines when data block transfer starts.
In normal mode, as soon as the DMA is doorbelled, the DMA reads the LL descriptor, and starts the data block transfer. When this feature is enabled, the DMA reads the descriptor, but starts the data transfer only when your application logic toggles the [w|r]dxfer_go_togg field in PCIE_CLIENT_DMA_HSHAKE_TOGG register.

The DMA handshake mechanism can be turned on or off per channel using DMA_[WRITE/READ]_ENGINE_EN_OFF register. The handshake mechanism cannot be enabled/disabled when the channel status isactive, that is, when DMA_CH_CONTROL1_OFF_[WR|RD]CH_i.CS =01.

11.6.4.4.2 DMA Handshake Operation

The handshake between the DMA and your application is done using [w|r]dxfer_go_togg and [w|r]dxfer_done_togg. In case of a DMA Write, your application should toggle the wdxfer_go_togg signal to indicate data block availability. In case of a DMA Read, your application should toggle the rdxfer_go_togg signal to indicate that your application hardware is ready to receive a data block.

To keep a track of [w|r]dxfer_go_togg signal toggles, the DMA implements a 5-bit handshake counter for each write/read channel. When your application toggles [w|r]dxfer_go_togg signal, the handshake counter is incremented. The handshake counter value is taken into account by the DMA before performing the data transfer for each descriptor. The data transfer happens only when the handshake counter value is non-zero. When the data transfer is complete, the DMA decrements the handshake counter, and toggles [w|r]dxfer_done_togg signal to indicate completion of data transfer to your application.

The handshake counter is 5-bit wide, so only 32 outstanding [w|r]dxfer_go_toggrequests can be handled by the DMA for each channel. The DMA does not implement an overflow protection or overflow error indication mechanism for the handshake counter. It is the responsibility of your application to keep the number of [w|r]dxfer_go_togg toggles under check.

One example of the DMA operation when the handshake feature is enabled for a write channel is as follows:

1. The CPU doorbells channel 0.
2. The DMA resets the handshake counter for channel 0.
3. The DMA reads LL element 0 descriptor. After the DMA receives descriptor read completions, the DMA checks the value of the handshake counter.
   If handshake counter =0, DMA waits until handshake counter >0 before transferring the data block.
   If handshake counter >0, DMA transfers the data block immediately.
4. After the data transfer is complete, the DMA Decrements the handshake counter, and Toggles wdxfer_done_togg.
5. Steps 3-4 are repeated for all the remaining elements of the linked list.

11.6.4.5 Using the DMA

11.6.4.5.1 Source and Destination Address Registers

The DMA channel context SAR and DAR registers (DMA_SAR_LOW_OFF_WRCH_0, DMA_SAR_HIGH_OFF_WRCH_0 etc.) provide support for remote-to-local, and local-to-remote PCIe address mapping. You program the start of the local and remote data buffers using these registers, and the DMA increments the SAR and DAR as the DMA transfer progresses. For a write transfer, the SAR is the address of the local memory, and the DAR is the address of the remote memory, as shown in figure below.

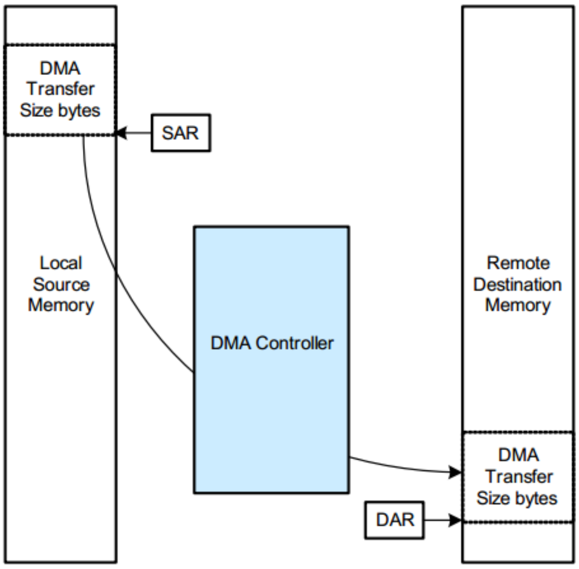

Fig. 11-15 Write Transfer: SAR and DAR for Write Channel

For a read transfer, the SAR is the address of the remote memory, and the DAR is the address of the local memory, as shown in Figure below.

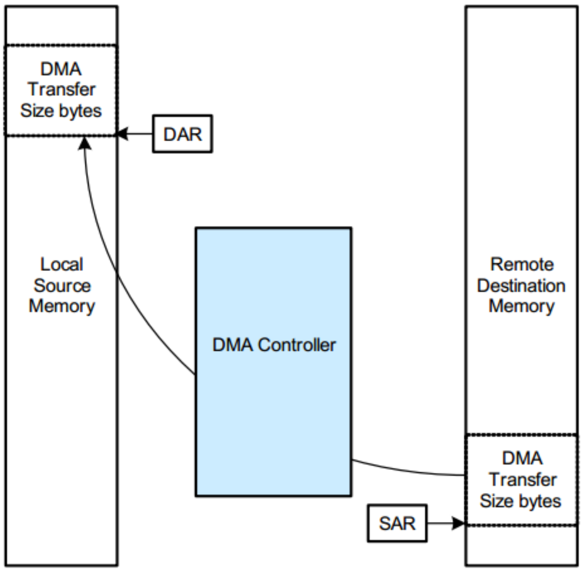

Fig. 11-16 Read Transfer: SAR and DAR for Write Channel

11.6.4.5.2 DMA Transfer Size Registers

You program the DMA transfer size using the DMA Transfer Size Register (DMA_TRANSFER_SIZE_OFF_WRCH_0 or DMA_TRANSFER_SIZE_OFF_RDCH_0). The maximum DMA transfer size is 4GB, and the minimum transfer size is one byte (0x1). The DMA decrements the value in this register as the DMA transfer progresses. When all bytes are successfully transferred, the value in this register is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element.

You can read this register to monitor the transfer progress. However, in some scenarios there is a delay before the controller updates this register. For example, when less than three channels are door belled, this register is only updated after a descriptor finishes (LL mode), or the transfer ends (non-LL mode).

11.6.4.5.3 Starting The DMA Transfer

After you program the DMA controller registers (including writing to the DMA Read Engine Enable or DMA Write Engine Enable register), you start a DMA transfer by writing zero to the Doorbell Number field of the DMA_WRITE_DOORBELL_OFF or DMA_READ_DOORBELL_OFF. You can program and start both a read and a write transfer at the same time. The DMA supports full duplex operation, processing read and write transfers at the same time and in parallel with normal (non-DMA) traffic.

11.6.4.5.4 Detecting the End of The DMA Transfer

11.6.4.5.4.1 Detecting End of Transfer without Errors

The normal end of a DMA transfer is detected by any of the following methods:
- Local interrupt asserted.
- Remote interrupt (IMWr) received.
- Channel status field of the Channel Control 1 register is Stopped, and the DMA Transfer Size register is 0x0.
- Polling of the DMA Write Interrupt Status Register (DMA_WRITE_INT_STATUS_OFF) or DMA Read Interrupt Status Register (DMA_READ_INT_STATUS_OFF).

11.6.4.5.4.2 Detecting End of Transfer with Errors

The abnormal end of a DMA transfer is detected by any of the following methods:
- Local interrupt (pin) asserted.
- Remote interrupt (IMWr) received.
- Polling of the DMA Write Interrupt Status Register (DMA_WRITE_INT_STATUS_OFF) or DMA Read Interrupt Status Register (DMA_READ_INT_STATUS_OFF).
- Channel Status field of the Channel Control 1 register is Halted. When the DMA controller detects an error, it forces the DMA to stop issuing requests for the channel. It also sets the channel status field of the Channel Control 1 register to Halted, generates an abort interrupt (if enabled), and sends an abort IMWr (if enabled). The DMA Transfer Size register indicates the remaining number bytes to be transferred, except when there is an AXI write error during a DMA read transfer.
- Channel Status field of the Channel Control 1 register is Stopped, and the DMA Transfer Size register is not 0x0. You have prematurely stopped this channel as described in "Stopping the DMA Transfer (Software Stop)"on next section

11.6.4.5.5 Stopping the DMA Transfer (Software Stop)

You can manually abort (stop) the DMA transfer by writing the channel number to the Doorbell Number field and writing 1 to the Stop field in DMA_[WRITE|READ]_DOORBELL_OFF. This causes the DMA to:
- Place the channel in a Stopped state. The channel Status field in DMA_CH_CONTROL1_OFF_WRCH_0 is Stopped and the value in DMA_TRANSFER_SIZE_OFF_WRCH_0 will not be 0x0.
- Wait for all outstanding pending transactions.
- Assert the abort interrupt (if it is enabled) in DMA_WRITE_INT_STATUS_OFF.

You might also do this as part of a function level reset (FLR). FLR does not directly affect the DMA transfer so you must manually stop the DMA transfer before initiating an FLR.

11.6.4.6 Programming Examples

This section provides two programming and operation example flows.

11.6.4.6.1 Non-LL Write Transfer

In this example, the IMWr generation is disabled, as the local CPU initiates the DMA transfer. The local CPU is interrupted using the pcie_sys_int interrupt. The SAR is the address of the local memory, and the DAR is the address of the remote memory. Write DMA Transfer is from 0xBEEF_BEE0 to 0xCAFE_CAF0. Table below provides the programming details for this example transfer. The transfer size is 1MB.

Table 11-18 Write DMA Transfer Example

Address 0x380000+	NAME	Value
0x00C	DMA Write Engine Enable You must not write 0 to this register. Even temporarily writing 0 to this register resets the DMA logic.	0x1
0x054	DMA Write Interrupt Mask	0x0
0x200	DMA Channel Control 1 register ■ Local Interrupt Enable (LIE) =1 ■ Remote Interrupt Enable (RIE) =0	0x04000008

Address 0x380000+	NAME	Value
	■ AT, RO, NS, TC, Function Number =0	
0x208	DMA Transfer Size	0x00100000
0x20C	DMA SAR Low	0xBEEF_BEE0
0x210	DMA SAR High	0x0000_0000
0x214	DMA DAR Low	0xCAFE_CAF0
0x218	DMA DAR High	0x0000_0000
0x010	DMA Write Doorbell	0x0

11.6.4.6.2 Non-LL Read Transfer

In this example, the local interrupt generation is disabled, as the remote CPU initiates the DMA transfer. The remote CPU is interrupted using an IMWr. The SAR is the address of the remote memory, and the DAR is the address of the local memory. Read DMA Transfer from 0xBEEF_BEE0 to 0xCAFE_CAF0. Table below provides the programming details for this example transfer. The transfer size is 1MB.

Table 11-19 Read DMA Transfer Example

Address 0x380000+	NAME	Value
0x02C	DMA Read Engine Enable You must not write 0 to this register. Even temporarily writing 0 to this register resets the DMA logic.	0x1
0x0CC/0x0D0	DMA Read Done IMWr Address Low and high	IMWr Address #1
0x0D4/0x0D8	DMA Read Abort IMWr Address Low and High	IMWr Address #2
0x0DC	DMA Read Channel 0 IMWr Data	IMWr Data
0x200	DMA Channel Control 1 register ■ Local Interrupt Enable (LIE) =0 ■ Remote Interrupt Enable (RIE) =1 ■ AT, RO, NS, TC, Function Number =0	0x04000010
0x208	DMA Transfer Size	0x00100000
0x20C	DMA SAR Low	0xBEEF_BEE0
0x210	DMA SAR High	0x0000_0000
0x214	DMA DAR Low	0xCAFE_CAF0
0x218	DMA DAR High	0x0000_0000
0x030	DMA Read Doorbell	0x0

11.6.5 PCIe Message Handling

This section describes the processing of messages through the controller. For a proper understanding of messages, you should be familiar with Section 2.2.8, “Message Request Rules” of the PCI Express Base Specification, Revision 3.0.

11.6.5.1 Message Generation

These are three methods to generate PCIe Messages:

- Specific MSG interface
  You can use PCIE_CLIENT_MSG_GEN_CON register to generate messages such as:
  - Vendor-Defined Message
  - Legacy PCI Interrupt Message
  - PME_Turn_Off message
  - Unlock message
  - LTR Message
  - OBFF Message

  Refer to register description for more details.
- AXI bridge

In this method, you should program the PCIE_CLIENT_AXI_SLV_AWMISC_HDR PCIE_CLIENT_AXI_SLV_AWMISC_HDR3 and PCIE_CLIENT_AXI_SLV_AWMISC_HDR4 registers to set these parameters:
slv_awmisc_info [4:0] =MSG
slv_awmisc_info [20:13] = message code
slv_awmisc_tag [5:0] = tag
slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
Then you can send zero length memory write (slv_awstrb=0) to generate the message. You must not program registers mentioned above when there are normal transfers pending on AXI slave interface. And should set these registers in normal value when you want to send MWr TLP. This method is not recommended because of these limitations.

- AXI bridge and iATU

Program related client register fields as follows:
slv_awmisc_info[4:0] =MEM
slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
Then iATU needs to be configured to to translate MWr to Msg TLPs. Refer to "Address Translation" for more details. This method is not recommended because that it needs additional iATU resources.

11.6.5.2 Message Reception

PCIe controller use pcie_msg_int interrupt to indicate the reception of PCIe Message. Application can poll to PCIE_CLIENT_INTR_STATUS_MSG_RX register to check the status of Message reception. Refer to register information for details.

11.6.6 PCIe Power Management

11.6.6.1 Overview

The controller supports two categories of PM operations to control the device state (D-state) and link state. For a proper understanding of PCIe Power management you should be familiar with Section 5, "Power Management" of the PCI Express Base Specification, Revision 3.0.

Software PCI Compatible PM (PCI-PM)

- D-state PM of Function. The host software can direct the function to enter any of the D1, D2, or D3 low-power states. It does this by writing to the Power Management Control and Status Register (PMCSR) in the PCI-PM capability structure.
- D-state PM of Link. Link states are not visible to PCI-PM legacy compatible software and are derived from the power management D-states of the components connected to that link. The action of changing the D-state in the PMCSR indirectly causes a change in the link power state. The L1 state is entered whenever all functions of a USP on a link are programmed to a non-D0 state. The entry into L2 and L3 states is initiated by the DSP.

PCIe PM Mechanisms

- Active State PM (ASPM).When the USP is in L0 and detects idleness on the link for a specific amount of time, it automatically transitions the link to the L0s or L1 (optional) power state.
- L1 Substates. This is an optional PCIe feature that enables components on a link to further reduce idle power consumption while the link is in L1, including almost complete removal of power for the high speed PHY circuits.

11.6.6.2 L0s Operation

L0s is a low-power state enabled by ASPM. ASPM controls entry into L0s for the transmitter. The remote device controls entry into L0s for the receiver.

11.6.6.2.1 L0s Entry

All of these conditions must be met:

- ASPM L0s is enabled through the ASPM Control field in the Link Control register.
- L0s entry conditions as defined in Section 5.4.1.1.1, "Entry into the L0s State" of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L0S_ENTRANCE_LATENCY field in ACK_F_ASPM_CTRL_OFF).

- No higher stage of power-down requested.

11.6.6.2.2 L0s Exit

Any of these conditions can be met:

- A DLLP or TLP is pending to be sent.
- L1 entry conditions as defined in Section 5.4.1.2.1, “Entry into the L1 State” of the PCI Express Base Specification, Revision 3.0, are satisfied.
- PCIe link partner requests to enter into link recovery.

11.6.6.3 L1 Operation (Non-substates)

The following topic will be discussed in this section: L1 (ASPM/PM) Entry and Exit Conditions and L1 Clock PM (L1 with REFCLK removal/PLL Off) Entry and Exit Conditions.

11.6.6.3.1 L1 (ASPM/PM) Entry

L1 is a low-power state enabled either by ASPM (L1-ASPM) or by the software changing the D-state (L1-PM). The L1 state is a bi-directional link low-power state and both link partners must negotiate to go to this state.

The L1-ASPM entry negotiation handshake uses PM_Active_State_Request_L1 DLLPs, PM_Request_Ack DLLPs, and PM_Active_State_Nak MSG TLPs. Refer to PCIe Basic Specification for more information.

There are three scenarios that cause the controller to enter L1 under ASPM conditions.

Scenario 1: L1 Idle Timeout In L0s

All of these conditions must be met in the USP:

- ASPM L1 and L0s are enabled through the ASPM Control field in the Link Control register.
- The ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to ‘0’ and the link state is L0s for both link partners, or the ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to ‘1’.
- L1 entry conditions as defined in Section 5.4.1.2.1, “Entry into the L1 State” of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power-down requested.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller
- There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
- There are no pending DMA transfers.

Scenario 2: L1 Idle Timeout In L0

All of these conditions must be met in the USP:

- ASPM L1 is enabled and L0s is not enabled through the ASPM Control field in the Link Control register.
- Link state is L0.
- L1 entry conditions as defined in Section 5.4.1.2.1, “Entry into the L1 State” of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
- No higher stage of power down-requested.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller.
- There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
- There are no pending DMA transfers.

Scenario 3: Application Controlled (USP only)

All of these conditions must be met in the USP:

- ASPM L1 is enabled through the ASPM Control field in the Link Control register.
- Your application writes 1 to the app_req_entr_l1 field in PCIE_CLIENT_POWER_CON register.
- Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
- There are no in-progress transactions in the controller.

- There are no pending requests at the AXI slave interface, that is, slv_a*validmust be 0.
- There are no pending DMA transfers.

L1-PM Entry

The power management state of a link is determined bythe D-state of theUSP.When you change the device state of the USP to D1, D2, or D3hot by writing to the PMCSR, the controller must initiate a link state transition to L1.

An USP application asserting the app_xfer_pending field does not prevent L1-PM entry, but will cause immediate exit from L1-PM.

11.6.6.3.2 L1-PM/L1-ASPM Exit

Any of these conditions are met:

- A DLLP or TLP is pending to be sent.
- Your application asserts the app_req_exit_l1 field.
- Link partner is requesting exit from L1.
- Your application asserts the app_xfer_pending field.
- Your application asserts the app_pm_xmt_pme field.

When the USP is programmed with capability to support PME; it sends a PME message to the RC which calls the PM software to transition the USP to the D0 state. Therefore, you should only use app_pm_xmt_pme for L1-PM exit.

- PM software (RC) requests a higher stage of power-down by writing to the PMCSR in the USP.
- Your application (USP) requests transmission of VDM, MSI/MSIX, or LTR message. Legacy interrupt is not included.
- Your application (DSP) requests transmission of Unlock message.
- Your application is requesting to send traffic by asserting or slv_a*valid.
- Your application doorbells a DMA read or write channel, or DMA controller is requesting data.
- Your application (DSP) initiates link disable, or link retrain (by setting PCIE_CAP_LINK_DISABLE or PCIE_CAP_RETRAIN_LINK field in LINK_CONTROL_LINK_STATUS_REG to 1).
- Your application (DSP) initiates hot reset by either:
  - setting RESET_ASSERT field in PORT_LINK_CTRL_OFF to 1, or
  - setting SBR field in BRIDGE_CTRL_INT_PIN_INT_LINE_REG to 1, or
  - toggling app_init_rst field in PCIE_CLIENT_GENERAL_CON.
- Your application requests a speed change (by setting DIRECT_SPEED_CHANGE field in GEN2_CTRL_OFF to 1).
- Your application requests link width change (by setting DIRECT_LINK_WIDTH_CHANGE field in MULTI_LANE_CONTROL_OFF is set to 1).

11.6.6.3.3 L1 Clock PM

For an USP, host software uses the Enable Clock Power Management bit in the Link Control register to enable this feature. For a DSP, this register bit is hard coded to ‘0’ and cannot be used to control this behavior. Your application can use the app_clk_pm_en input to dynamically control whether to execute L1 with or without Clock PM.

- The Support Clock Power Management bit in the Link Capabilities register must be set. For downstream ports it is hardcoded to 0, for upstream ports it can be accessed through the DBI.
- The Enable Clock Power Management bit in the Link Control register must be set.
- You must set the app_clk_pm_en field to 1. The controller only samples app_clk_pm_en when L1 is entered.

L1 with Clock PM and L1 substates work orthogonal to each other. L1 with Clock PM uses the mac_phy_pclkreq_n[0]signaling, and L1 substates uses the mac_phy_pclkreq_n[1]signaling. However, L1 substates takes precedence over Clock PM within the cores PM state machine.

11.6.6.4 L1 Substate

The L1 substates are applicable in both the ASPM and PCI-PM L1 link states. L1 substates management utilizes a per-link sideband signal called CLKREQ#.

- During L1 substates it is assumed that core_clk is turned off and that aux_clk is active. It is required that your application switches aux_clk to a low frequency free running clock on entry into L1.

- The controller uses aux_clk for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value in the range 1...1000MHz to count real time. Frequencies lower than 1 MHz are possible, but with a loss of accuracy in the time counted.
- When the electrical idle detection circuitry is disabled, it is assumed that the PHY holds the signal phy_mac_rxelecidle to 1.

After the link has entered L1 through the normal L1 negotiation, the USP can initiate the sequence for entering the target L1 substate (L1.1 or L1.2) by tri-stating its CLKREQ# output buffer. The entry sequence can only proceed if the DSP is also tri-stating its CLKREQ# output buffer, resulting in the bidirectional CLKREQ# signal being pulled up to 1. Otherwise CLKREQ# will remain asserted at 0 and the link state will stay in L1. The exit sequence can be initiated by either port by asserting CLKREQ# to 0. For each port there are two cases to consider, the first where the exit is initiated locally, the second where the exit is initiated remotely. L1 substates management utilizes a per-link sideband signal called CLKREQ#.

11.6.6.4.1 L1 Substates Software Control

When the controller enters L1, the target L1 substate depends on several programming bits:

- PM Control/Status Register
  - USP: The current D-state
  - DSP: The DLLP type that was used by USP to request L1
- L1 Substates Control 1 Register
  - ASPM PM L1.1 Enabled
  - ASPM PM L1.2 Enabled
  - PCI PM L1.1 Enabled
  - PCI PM L1.2 Enabled

After the USP controller enters L1, it uses the D-state of the device to determine if L1 was entered in ASPM mode or PCI-PM mode.

After the DSP controller enters L1, it uses the USPs DLLPL1 request type to determine if L1 was entered in ASPM mode or PCI-PM mode. The next tables shows the target L1 substate as a function of the relevant programming bits.

Table 11-20 Target L1 Substate as a Function of Software Controls (USP)

D-State	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
!D0	-	-	-	0	0	L1
!D0	-	-	-	1	0	L1.1
!D0	-	-	-	-	1	L1.2
D0	0	0	-	-	-	L1
D0	1	0	-	-	-	L1.1
D0	0	1	0	-	-	L1
D0	1	1	0	-	-	L1.1
D0	-	1	1	-	-	L1.2

Table 11-21 Target L1 Substate as a Function of Software Controls (DSP)

DLLP Receive	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
PM_Enter_L1	-	-	-	0	0	L1
	-	-	-	1	0	L1.1
	-	-	-	-	1	L1.2
PM_	0	0	-	-	-	L1

DLLP Receive	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
Active_State_Request_L1	1	0	-	-	-	L1.1
	0	1	0	-	-	L1
	1	1	0	-	-	L1.1
	-	1	1	-	-	L1.2

The Reported LTR is the maximum of the snoop/no snoop latency values embedded in LTR messages transmitted by the upstream ports or received by the downstream port. The controller stores these values in the port logic LTR Latency Register (LTR_LATENCY_OFF). When the requirement bit in the message is 0, the latency value is considered infinite (that is, the check with the threshold always pass).

11.6.6.4.2 L1 Substates Entry and Exit

PCIe link entered L1 substate automatically if related enable bit is set and LTSSM already in L1 state, refer to section L1 Substates Software Control for details.

L1 substates Exit can be triggered locally or Remotely. For locally initiated exit, refer to section L1-PM/L1-ASPM Exit. Remotely initiated exit begins when CLKREQ# is asserted by remote PCIe partner.

11.6.6.5 L2 and L3 Power Down Entry and Exit

L2/L3 entry is initiated after the RC calls power management software to initiate the removal of power and clocks. USPs of devices in D0, D1, D2, and D3hot must respond to the receipt of a PME_Turn_Off MSG TLP by transmitting a PME_TO_Ack MSG TLP. The device must then request a link transition to L2/L3_Ready. L2/L3_Ready is a bi-directional link power down state. If your application is not ready to be shut down, it must keep the app_ready_entr_l23 field de-asserted.

L2/L3 Entry

All of these conditions must be met:

- PME_Turn_Off/PME_TO_Ack handshake has been completed.
- Your USP application is ready to be turned off; app_ready_entr_l23=1.
- After sending the PME_TO_Ack, the USP initiates the L2/L3 Ready transition protocol by sending the PM_Enter_L23 DLLP. The RC responds with the PM_Request_Ack.

L2/L3 Exit

Any of these conditions can be met:

- When the USP is programmed with capability to support PME, your application can assert the apps_pm_xmt_pme field to request the controller to wake up. The USP then sends a PM_PME MSG TLP to the RC which calls the PM software to transition the USP out of the D3 state.
- Device is programmed with capability to support PME and your application requests the controller to wake up by triggering a native hot-plug event.
- Link partner is requesting exit from L2/L3.

11.6.6.6 Dynamic Power Allocation (DPA)

The DPA capability enables software to actively manage and optimize function power usage when in the D0 state. DPA is not applicable to power states D1-D3.
For details on how your application interacts with the controller, see the description of the dpa_sub_upd_int field in PCIE_CLIENT_INTR_STATUS_MISC register.

11.6.7 PCIe Interrupt

The PCIe provides several types of interrupts to system interrupt controller. They can be divided into MSI/MSI-X, PCIe Error interrupt, PCIe Message Receive interrupt, PCIe Legacy interrupt, PCIe System interrupt and PCIe Power Management Interrupt etc. When operating as RC, the PCIe is capable of handling both MSI/MSI-X and legacy interrupts. This is because when operating as RC it should be able to service both PCIe end points as well as legacy endpoints. It is capable of generating MSI or Legacy interrupt if the PCIe is configured as EP. Notes that PCIe EP component can't generate both Legacy and MSI/MSI-X interrupt. It is either one or the other. The interrupt type an EP generates is configured during configuration time.

Interrupt status and mask bits are located in client register group, some interrupts are handled by client register directly, but some interrupts are generated by events deep into controller and software should clear the root cause to serve the interrupt events. For more information, refer to the register description.

The pcie_edma_wr/rd_int is more efficient than service by pcie_sys_int, it is available depends on Chip ID.

Table 11-22 PCIe Interrupt Table

System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
pcie_sys_int	PCIe System Interrupt	phy_link_up_int	RC & EP
		dll_link_up_int	RC & EP
		link_req_rst_not_int	RC & EP
		hp_pme_int	RC
		hp_int	RC
		hp_msi	RC
		link_auto_bw_int	RC
		link_auto_bw_msi	RC
		bw_mgt_int	RC
		bw_mgt_msi	RC
		edma_wr_int	RC & EP
		edma_rd_int	RC & EP
		dpa_sub_upd_int	EP
		rbar_update_int	EP
		link_eq_req_int	RC & EP
		ep_elbi_app_int	EP
pcie_legacy_int	PCIe Legacy interrupt	rx_inta_int	RC
		rx_intb_int	RC
		rx_intc_int	RC
		rx_intd_int	RC
		tx_inta_int	EP
		tx_intb_int	EP
		tx_intc_int	EP
		tx_intd_int	EP
pcie_msg_rx_int	PCIe message received interrupt	ven_msg_int	RC & EP
		unlock_msg_int	EP
		ltr_msg_int	RC
		cfg_pme_int	RC
		cfg_pme_msi_int	RC
		pm_pme_int	RC
		pm_to_ack_int	RC
		pm_turnoff_int	EP
		obff_idle_int	EP
		obff_obff_int	EP
		obff_cpu_active_int	EP
pcie_err_int	PCIe Error interrupt	aer_rc_err_int	RC
		aer_rc_err_msi	RC
		rx_cpl_timeout_int	RC & EP
		tx_cpl_timeout_int	RC & EP
		cor_err_sent_int	EP
		nf_err_sent_int	EP
		f_err_sent_int	EP

System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
		cor_err_rx_int	RC
		nf_err_rx_int	RC
		f_err_rx_int	RC
		radm_qoverflow_int	RC & EP
pcie_pmc_int	PCIe Power Management interrupt	linkst_in_l1sub_int	RC & EP
		linkst_in_l1_int	RC & EP
		linkst_in_l2_int	RC & EP
		linkst_in_l0s_int	RC & EP
		linkst_out_l1sub_int	RC & EP
		linkst_out_l1_int	RC & EP
		linkst_out_l2_int	RC & EP
		linkst_out_l0s_int	RC & EP
		pm_dstate_update_int	EP
pcie_dtim_int	DTIM Interrupt	N/A	RC
pcie_edma_wr_int[1:0]	eDMA Write Interrupt	N/A	RC & EP
pcie_edma_rd_int[1:0]	eDMA Read Interrupt	N/A	RC & EP
GIC LPI	MSI/MSI-X	message signaled interrupt	RC service and EP initiate

11.7 Appendix

11.7.1 LTSSM Code

S_DETECT_QUIET	6'h00
S_DETECT_ACT	6'h01
S_POLL_ACTIVE	6'h02
S_POLL_COMPLIANCE	6'h03
S_POLL_CONFIG	6'h04
S_PRE_DETECT_QUIET	6'h05
S_DETECT_WAIT	6'h06
S_CFG_LINKWD_START	6'h07
S_CFG_LINKWD_ACEPT	6'h08
S_CFG_LANENUM_WAIT	6'h09
S_CFG_LANENUM_ACEPT	6'h0A
S_CFG_COMPLETE	6'h0B
S_CFG_IDLE	6'h0C
S_RCVRY_LOCK	6'h0D
S_RCVRY_SPEED	6'h0E
S_RCVRY_RCVRCFG	6'h0F
S_RCVRY_IDLE	6'h10
S_RCVRY_EQ0	6'h20
S_RCVRY_EQ1	6'h21
S_RCVRY_EQ2	6'h22
S_RCVRY_EQ3	6'h23
S_L0	6'h11
S_L0S	6'h12
S_L123_SEND_EIDLE	6'h13
S_L1_IDLE	6'h14
S_L2_IDLE	6'h15
S_L2_WAKE	6'h16
S_DISABLED_ENTRY	6'h17
S_DISABLED_IDLE	6'h18

S_DISABLED	6'h19
S_LPBK_ENTRY	6'h1A
S_LPBK_ACTIVE	6'h1B
S_LPBK_EXIT	6'h1C
S_LPBK_EXIT_TIMEOUT	6'h1D
S_HOT_RESET_ENTRY	6'h1E
S_HOT_RESET	6'h1F

Chapter 12 USB2.0 Host & PHY

12.1 Overview

USB2.0 host subsystem include two USB2.0 host controller and USB2.0 PHY. The two host are same. USB2.0 host controller supports fully USB2.0 functions with one EHCI host controller and one OHCI host controller, and each host controller has one USB port. OHCI host controller only supports full-speed and low-speed mode and is used for full-speed devices and low-speed devices. EHCI only supports high-speed mode and is used for high-speed devices. OHCI host controller and EHCI host controller shares the same USB port, EHCI host controller will auto select the owner (OHCI or EHCI) of this USB port depending on the speed mode of attached devices, when selecting OHCI as owner, OHCI host controller will serve for the attached device; when selecting EHCI as owner, EHCI host controller will serve for the attached device.

USB2.0 host supports the following features:

- Compatible Specifications
  - Universal Serial Bus Specification, Revision 2.0
  - Enhanced host Controller Interface Specification (EHCI), Revision 1.0
  - Open host Controller Interface Specification (OHCI), Revision 1.0a
- Support High-speed (480Mbps), Full-speed (12Mbps) and Low-speed (1.5Mbps)

12.2 Block Diagram

USB2.0 host subsystem include two USB2.0 host controller and USB2.0 PHY.

USB2.0 host Controller comprises with:

- EHCI host Controller: Perform High-speed transactions
- OHCI host Controller: Perform full/low-speed transactions
- Port Routing Control: Select EHCI host Controller or OHCI host Controller

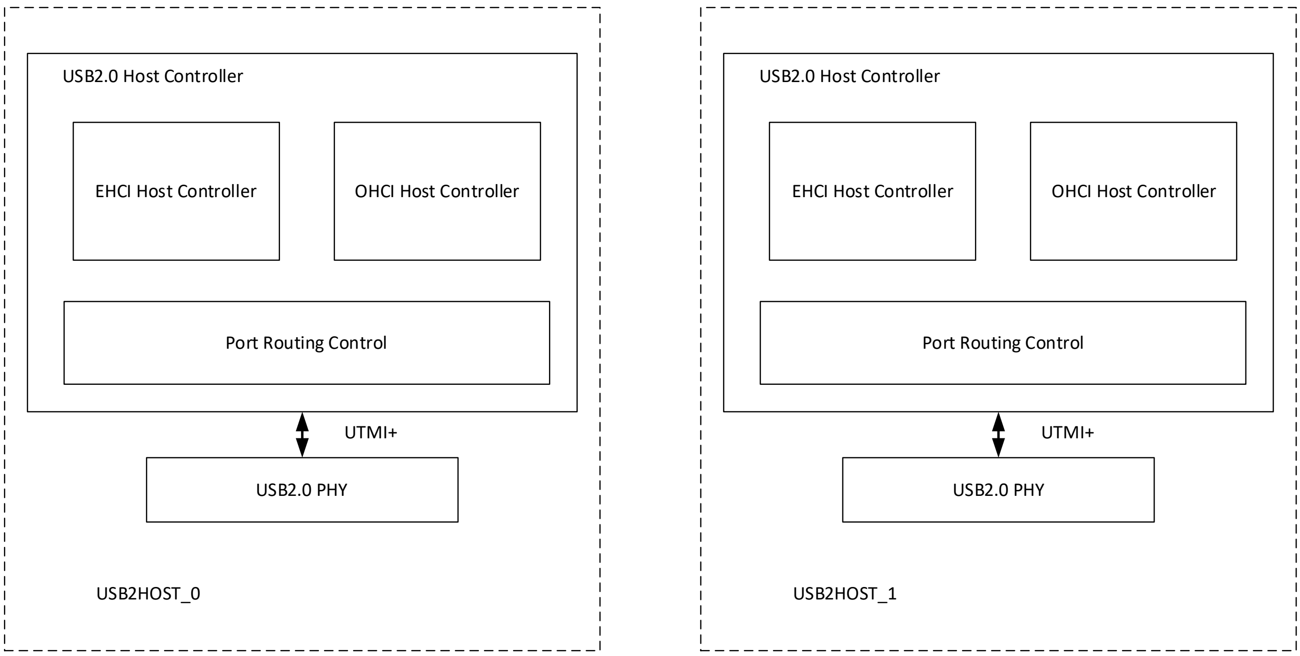

Fig. 12-1 USB2.0 Host Block Diagram

12.3 Function Description

12.3.1 EHCI Host Controller

It performs descriptors and data read or write from or to system memory and packs or unpack USB transactions from or to UTMI+ interface defined in EHCI specification for high-speed data transmission.

12.3.2 OHCI Host Controller

It performs descriptors and data read/write from/to system memory and packs or un-pack USB transactions from or to UTMI+ interface defined in OHCI specification for full-speed or low-speed data transmission.

12.3.3 Port Routing Control

As part of logic in the EHCI host controller, it is used to auto-select EHCI or OHCI host controller to serve the attached device depending on the speed of the attached device.

12.4 Register Description

12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 12-1 USB2.0 Host Controller Address Mapping

Base Address	Device
0xFC800000~0xFC87FFFF	USB2HOST_0 controller
0xFC880000~0xFC8FFFFF	USB2HOST_1 controller
USB2.0 Host Controller Address Mapping	
Offset Address Range	**Register Type**
0x00000 ~ 0x3ffff	EHCI
0x40000 ~ 0x7ffff	OHCI

EHCI and OHCI register definitions, please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

12.5 Interface Description

Table 12-2 USB2.0 PHY Interface Description

Pad Name	Direction	Descriptions
USB20_HOST0_DM	I/O	USB D- Signal
USB20_HOST0_DP	I/O	USB D+ Signal
USB20_HOST0_REXT	I/O	USB2.0 PHY Transmitter Resistor Tune Pin
USB20_HOST1_DM	I/O	USB D- Signal
USB20_HOST1_DP	I/O	USB D+ Signal
USB20_HOST1_REXT	I/O	USB2.0 PHY Transmitter Resistor Tune Pin

12.6 Application Notes

12.6.1 Host Charge Detect Sequence

The USB2.0 PHY supports battery charger detection to enable device draw increased current from VBUS for charging and/or powering up from dedicated charging ports or charging downstream ports.

The related signals with GRF is following:

Table 12-3 USB2PHY Battery Charging GRF Description

GRF	Description
USB2PHY_GRF_CON2[5]	CHRGSEL: This signal selects whether the Battery Charger circuit sets voltage sourcing on the DP line and sensing on the DM line or voltage sourcing on DM and sensing on DP.
USB2PHY_GRF_CON2[6]	VDATDETENB: This signal activates the Battery Charger comparator and enables detection of the DP and DM lines according to the Battery Charging specification.
USB2PHY_GRF_CON2[7]	VDATSRCENB: This signal activates the voltage sourcing on the DP or DM line.
USB2PHY_GRF_STATUS0[0]	CHGDET: This signal is the battery charge detection (VDAT_REF) comparator output.
USB2PHY_GRF_STATUS0[1]	FSVPLUS: This signal is the DP FS/LS single ended receiver output, which is also the VLGC output.
USB2PHY_GRF_STATUS0[2]	FSVMINUS: This signal is the DM FS/LS single ended receiver output, which is also the VLGC output.
USB2PHY_GRF_STATUS0[11]	OTGSESSVLD0: This signal is the VBUS session valid detection and can be used by a portable device to detect the VBUS voltage from the host or charger port.

Table 1-6 lists the detection flow.

Table 12-4 USB2PHY Battery Charging Operations

Mode of Operation	Inputs			Outputs			
	CHRGSEL	VDATDETENB	VDATSRCENB	OTGSESSVLD	CHGDET	FSVPUS	FSVMINUS
Battery charging is disabled	X	0	0	X	0	X	X
PHY is operating as a host CDP with no PD detected.	1	1	0	X	0	0	X
PHY is operating as a host CDP that detects an attached PD, which supports the BC specification.	1	1	1	X	1	0	X
PHY is operating as a host CDP that detects a connect from the PD D+ pullup.	1	1	0	X	X	1	0

12.6.2 Program Flow

Please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

Chapter 13 USB3 Controller

13.1 Overview

USB3 sub-system include three USB3.0 controller and some PHYs. Two of the USB3.0 controller (marked as USB3OTG_0 and USB3OTG_1) in PD_USB can act as static host, static device, USB2.0/3.0 OTG A device or B device basing on the status of input ID from USB2.0 PHY. The two controllers respectively connect to one USB3.0 PHY and one USB2.0 PHY. They can perform data transmission between host and device as host or device for Super-Speed/High-Speed/Full-Speed/Low-Speed. The other one (marked as USB3OTG_2) in PD_PHP only support USB3.0 Host and only connect to one USB3.0 PHY and be used for Super-Speed.
USB3.0 sub-system supports the following features:

- General Features
  1. Compatible Specification
     - Universal Serial Bus 3.0 Specification, Revision 1.0
     - Universal Serial Bus Specification, Revision 2.0 (exclude USB3OTG_2)
     - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  2. Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  3. Simultaneous IN and OUT transfer for USB3.0, up to 8Gbps bandwidth
  4. Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  5. LPM protocol in USB 2.0 (exclude USB3OTG_2) and U0, U1, U2, and U3 states for USB 3.0
  6. Dynamic FIFO memory allocation for endpoints
  7. Keep-Alive feature in LS mode and (micro-)SOFs in HS/FS modes (exclude USB3OTG_2)
  8. Low MIPS requirement
     - Driver involved only in setting up transfers and high-level error recovery
     - Hardware handles data packing and routing to a specific pipe
- Application Interface Features
  1. AHB Slave interface
  2. AXI Master interface
     - Programmable burst lengths up to 16
     - Handle fixed burst address alignment
     - Programmable number of outstanding read/write requests up to 16
     - Concurrent read/write to get best performance of USB3.0 duplex operation
- USB3.0 Device Features
  1. Up to 10 IN endpoints, including control endpoint 0
  2. Up to 6 OUT endpoints, including control endpoint 0
  3. Up to 16 endpoint transfer resources, each one for each endpoint
  4. Flexible endpoint configuration for multiple applications/USB set-configuration modes
  5. Hardware handles ERDY and burst
  6. Stream-based bulk endpoints with controller automatically initiating data movement
  7. Isochronous endpoints with isochronous data in data buffers
  8. Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB Class-Specific Device Features
  1. Stream support for UASP application
  2. Gathering of scattered packet to support Ethernet Over USB
  3. Scheduling of multiple Ethernet packets without interrupt
  4. Variable FIFO buffer allocation for each endpoint
  5. For isochronous applications, scheduling of variable-length payloads for each microframe
  6. Microframe precise scheduling for isochronous applications
  7. Configurable endpoint type selection and dynamic FIFO allocation to facilitate multi-function/composite device implementation. During set-config or alternate-setting, device resources are reconfigured to meet the configuration or alternate setting

requirements.

- USB 3.0 xHCI Host Features
  1. Support up to 64 devices
  2. Support 1 interrupter
  3. Support 1 USB2.0 port (exclude USB3OTG_2) and 1 Super-Speed port
  4. Support standard or open-source xHCI and class driver
- USB 3.0 Dual-Role Device (DRD) Features
  1. Static Device Operation
  2. Static Host Operation
  3. USB3.0/USB2.0 OTG A device and B device basing on ID, USB3OTG_2 only support USB3.0
  4. Not Support USB3.0/USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)
- Miscellaneous Features
  5. USB2.0 PHY support Battery Charge detection
  6. USB3OTG_0 and USB3OTG_1 support USB Type-C and DP Alt Mode (DP should refer to DP TX Controller section)
  7. USB3OTG_2 PHY combos with PCIE and SATA, this could refer to Multi-PHY section

13.2 Block Diagram

USB3OTG_0 and USB3OTG_1 comprises with:

- Bus Interface: Register Interface/Data and Descriptors DMA management
- SS/HS/FS/LS MAC: USB part logic
- USB2.0 PHY: UTMI+ interface USB2.0 PHY
- USBDP PHY: USB3.0 and DP combo

Note: For detail about USBDP PHY, please refer to USBDP PHY section.

USB3OTG_2 comprises with:

- Bus Interface: Register Interface/Data and Descriptors DMA management
- SS/HS/FS/LS MAC: USB2.0 part logic not used
- USB3/PCIE/SATA Combo PHY

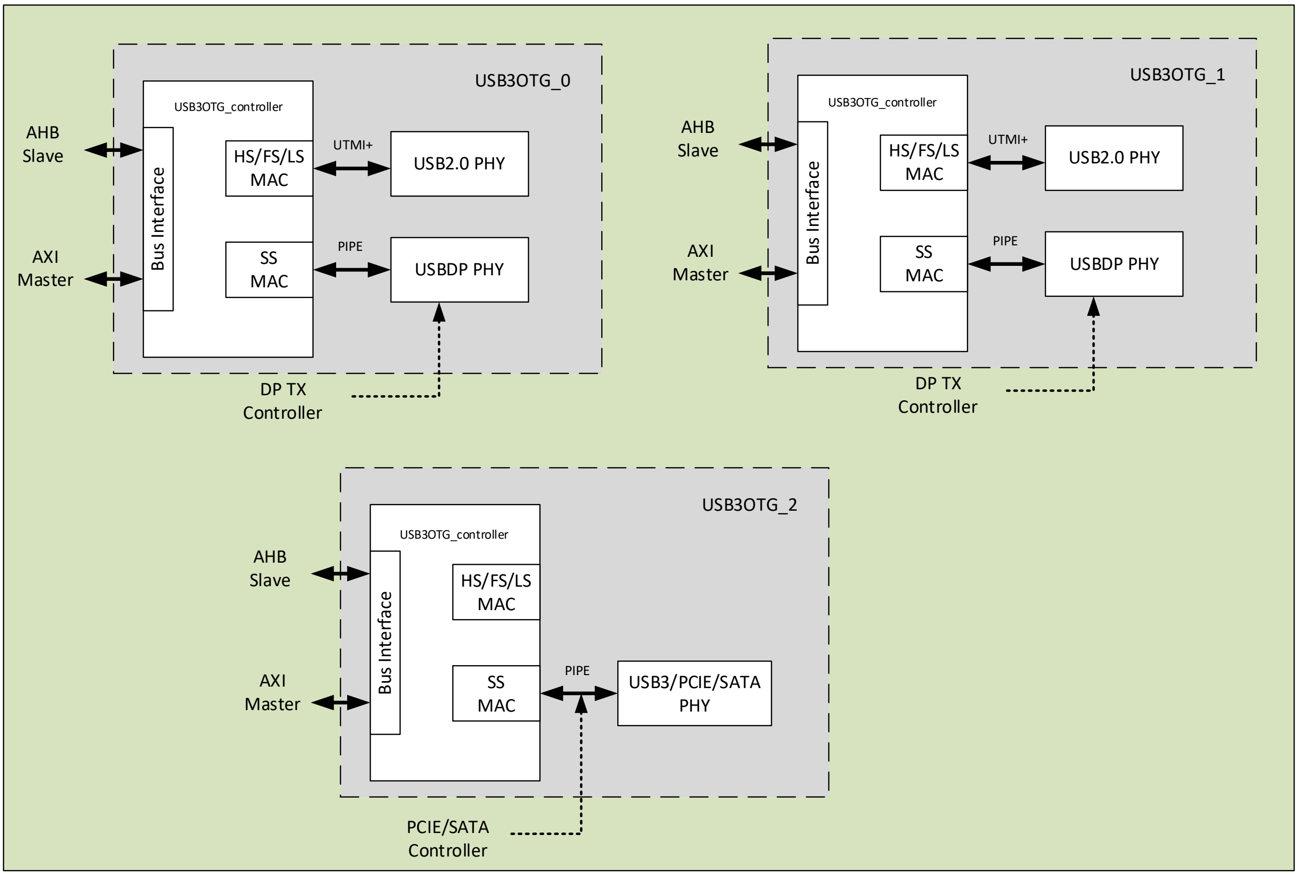

Fig. 13-1 USB3 Block Diagram

13.3 Function Description

As USB3OTG_0 or USB3OTG_1, it can act as static xHCI host controller, static device controller, USB3.0/2.0 OTG A device or B device basing on ID of USB2.0 PHY. As device controller, it can work on either USB2.0 speed or Super-Speed basing on speed of host attached to, and process USB transactions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface of USBDP PHY. As host controller, it can work on USB2.0 speed, Super-Speed or both basing on speed or type of attached device, and process USB transactions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface of USBDP PHY.
For USB3OTG_2, it only works in Super-Speed mode and process USB transactions described in the descriptors (read back from external memory by AXI master) to/from Pipe Interface of USB3/SATA/PCIE combo PHY.

13.4 Register Description

13.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 13-1 USB3 Address Mapping

Base Address	Device
0xFC000000~0xFC3FFFFF	USB3OTG_0 controller
0xFC4000000~xFC7FFFFF	USB3OTG_1 controller
0xFCD00000~0xFD0FFFFF	USB3OTG_2 controller
USB3.0 Controller Address Mapping	
Offset Address Range	**Register Type**
0x00000 ~ 0x07FFF	xHCI Registers, see xHCI spec.
0x0C100 ~ 0x0C6FF	Global Registers
0x0C700 ~ 0x0CBFF	Device Controller Registers

0x0CC00 ~ 0x0CFFF	Unused/Reserved
0x40000 ~ 0x7FFFF	Internal RAM0 – Debug Access (256KB)
0x80000 ~ 0xBFFFF	Internal RAM1 – Debug Access (256KB)
0xC0000 ~ 0xFFFFF	Internal RAM2 – Debug Access (256KB)

13.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
USB3OTG_GSBUSCFG0	0xC100	W	0x00000001	Global SoC Bus Configuration Register 0
USB3OTG_GSBUSCFG1	0xC104	W	0x00000300	Global SoC Bus Configuration Register 1
USB3OTG_GTXTHRCFG	0xC108	W	0x00000000	Global Tx Threshold Control Register
USB3OTG_GRXTHRCFG	0xC10C	W	0x00000000	Global Rx Threshold Control Register
USB3OTG_GCTL	0xC110	W	0x13512004	Global Core Control Register
USB3OTG_GSTS	0xC118	W	0x7E800000	Global Status Register
USB3OTG_GUCTL1	0xC11C	W	0x0004018A	Global User Control Register 1
USB3OTG_GSNPSID	0xC120	W	0x5533300A	Global SNPS ID Register
USB3OTG_GGPIO	0xC124	W	0x00000000	Global General Purpose Input/Output Register
USB3OTG_GUID	0xC128	W	0x20190520	Global User ID Register
USB3OTG_GUCTL	0xC12C	W	0x02008010	Global User Control Register
USB3OTG_GBUSERRADDRLO	0xC130	W	0x00000000	Global SoC Bus Error Address Register - Low
USB3OTG_GBUSERRADDRHI	0xC134	W	0x00000000	Global SoC Bus Error Address Register - High
USB3OTG_GPRTBIMAPLO	0xC138	W	0x00000000	Global SS Port to Bus Instance Mapping Register
USB3OTG_GHWPARAMS0	0xC140	W	0x2020400A	Global Hardware Parameters Register 0
USB3OTG_GHWPARAMS1	0xC144	W	0x0120C93B	Global Hardware Parameters Register 1
USB3OTG_GHWPARAMS2	0xC148	W	0x20190520	Global Hardware Parameters Register 2
USB3OTG_GHWPARAMS3	0xC14C	W	0x069CD084	Global Hardware Parameters Register 3
USB3OTG_GHWPARAMS4	0xC150	W	0x47822010	Global Hardware Parameters Register 4
USB3OTG_GHWPARAMS5	0xC154	W	0x04204018	Global Hardware Parameters Register 5
USB3OTG_GHWPARAMS6	0xC158	W	0x09D78020	Global Hardware Parameters Register 6
USB3OTG_GHWPARAMS7	0xC15C	W	0x00000000	Global Hardware Parameters Register 7
USB3OTG_GDBGFIFOSPACE	0xC160	W	0x000A0000	Global Debug Queue/FIFO Space Available Register
USB3OTG_GDBGLNMCC	0xC168	W	0x00000000	Global Debug LNMCC Register
USB3OTG_GDBGBMU	0xC16C	W	0x00000000	Global Debug BMU Register
USB3OTG_GDBGLSPMUX	0xC170	W	0x003F0000	Global Debug LSP MUX Register - Device
USB3OTG_GDBGLSP	0xC174	W	0x00000000	Global Debug LSP Register
USB3OTG_GDBGEPINFO0	0xC178	W	0x00000000	Global Debug Endpoint Information Register 0

Name	Offset	Size	Reset Value	Description
USB3OTG_GDBGEPINFO1	0xC17C	W	0x00800000	Global Debug Endpoint Information Register 1
USB3OTG_GPRTBIMAP_HSLO	0xC180	W	0x00000000	Global High-Speed Port to Bus Instance Mapping Register - Low
USB3OTG_GPRTBIMAP_FSLO	0xC188	W	0x00000000	Global Full-Speed Port to Bus Instance Mapping Register - Low
USB3OTG_GUSB2PHYCFG0	0xC200	W	0x40102400	Global USB2 PHY Configuration Register 0
USB3OTG_GUSB3PIPECTL0	0xC2C0	W	0x00000000	Global PIPE PHY Configuration Register 0
USB3OTG_GTXFIFOSIZn	0xC300	W	0x00000042	Global Transmit FIFO Size Register n, offset (0xc300 + 4*n), n=0~6
USB3OTG_GRXFIFOSIZn	0xC380	W	0x03340185	Global Receive FIFO Size Register n
USB3OTG_GEVNTADRLO0	0xC400	W	0x00000000	Global Event Buffer Address (Low) Register 0
USB3OTG_GEVNTADRHI0	0xC404	W	0x00000000	Global Event Buffer Address (High) Register 0
USB3OTG_GEVNTSIZ0	0xC408	W	0x00000000	Global Event Buffer Size Register 0
USB3OTG_GEVNTCOUNT0	0xC40C	W	0x00000000	Global Event Buffer Count Register 0
USB3OTG_GHWPARAMS8	0xC600	W	0x0000047C	Global Hardware Parameters Register 8
USB3OTG_GTXFIFOPRIDEV	0xC610	W	0x00000000	Global Device TX FIFO DMA Priority Register
USB3OTG_GTXFIFOPRIHST	0xC618	W	0x00000000	Global Host TX FIFO DMA Priority Register
USB3OTG_GRXFIFOPRIHST	0xC61C	W	0x00000000	Global Host RX FIFO DMA Priority Register
USB3OTG_GFIFOPRIDBC	0xC620	W	0x00000000	Global Host Debug Capability DMA Priority Register
USB3OTG_GDMAHLRATIO	0xC624	W	0x00000000	Global Host FIFO DMA High-Low Priority Ratio Register
USB3OTG_GFLADJ	0xC630	W	0x00000000	Global Frame Length Adjustment Register
USB3OTG_DCFG	0xC700	W	0x00080000	Device Configuration Register
USB3OTG_DCTL	0xC704	W	0x00F00000	Device Control Register
USB3OTG_DEVTEN	0xC708	W	0x00000000	Device Event Enable Register
USB3OTG_DSTS	0xC70C	W	0x00520000	Device Status Register
USB3OTG_DGCMDPAR	0xC710	W	0x00000000	Device Generic Command Parameter Register
USB3OTG_DGCMD	0xC714	W	0x00000000	Device Generic Command Register
USB3OTG_DALEPENA	0xC720	W	0x00000000	Device Active USB Endpoint Enable Register
USB3OTG_DEPnCMDPAR2	0xC800	W	0x00000000	Device Physical Endpoint-n Command Parameter 2 Register, offset (0xc800 + 4*n), n=0~12
USB3OTG_DEPnCMDPAR1	0xC804	W	0x00000000	Device Physical Endpoint-n Command Parameter 1 Register, offset (0xc804 + 4*n), n=0~12

Name	Offset	Size	Reset Value	Description
USB3OTG_DEPnCMDPAR0	0xC808	W	0x00000000	Device Physical Endpoint-n Command Parameter 0 Register, offset (0xc808 + 4*n), n=0~12
USB3OTG_DEPnCMD	0xC80C	W	0x00000000	Device Physical Endpoint-n Command Register, offset (0xc80c + 4*n), n=0~12

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.3 Detail Registers Description

USB3OTG_GSBUSCFG0

Address: Operational Base + offset (0xC100)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	datrdreqinfo AXI-cache for Data Read (DatRdReqInfo).
27:24	RW	0x0	desrdreqinfo AXI-cache for Descriptor Read (DesRdReqInfo).
23:20	RW	0x0	datwrreqinfo AXI-cache for Data Write (DatWrReqInfo).
19:16	RW	0x0	deswrreqinfo AXI-cache for Descriptor Write (DesWrReqInfo).
15:12	RO	0x0	reserved
11	RW	0x0	datbigend This bit controls the endian mode for data accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
10	RW	0x0	desbigend This bit controls the endian mode for descriptor accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
9:8	RO	0x0	reserved
7	RW	0x0	incr256brstena If software set this bit to 1, the AXI master uses INCR to do the 256-beat burst.
6	RW	0x0	incr128brstena If software set this bit to 1, the AXI master uses INCR to do the 128-beat burst.
5	RW	0x0	incr64brstena If software set this bit to 1, AXI master uses INCR to do the 64-beat burst.
4	RW	0x0	incr32brstena If software set this bit to 1, the AXI master uses INCR to do the 32-beat burst.
3	RW	0x0	incr16brstena If software set this bit to 1, the AXI master uses INCR to do the 16-beat burst.
2	RW	0x0	incr8brstena If software set this bit to 1, the AXI master uses INCR to do the 8-beat burst.
1	RW	0x0	incr4brstena When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers.

Bit	Attr	Reset Value	Description
0	RW	0x1	incrbrstena This bit determines the set of burst lengths the master interface uses. It works in conjunction with the GSBUSCFG0[7:1] enables (INCR256/128/64/32/16/8/4). 0: INCRX burst mode ARLEN/AWLEN do not use INCR. They use only the following burst lengths: 4 (if GSBUSCFG0.INCR4BrstEna = 1); 8 (if GSBUSCFG0.INCR8BrstEna = 1); 16 (if GSBUSCFG0.INCR16BrstEna = 1); 32 (if GSBUSCFG0.INCR32BrstEna = 1); 64 (if GSBUSCFG0.INCR64BrstEna = 1); 128 (if GSBUSCFG0.INCR128BrstEna = 1); 256 (if GSBUSCFG0.INCR256BrstEna = 1); 1: INCR (undefined length) burst mode; ARLEN/AWLEN uses any length less than or equal to the largest-enabled burst length of INCR4/8/16/32/64/128/256. For cache line-aligned applications, this bit is typically set to 0 to ensure that the master interface uses only power-of-2 burst lengths (as enabled via GSBUSCFG0[7:0]).

USB3OTG_GSBUSCFG1

Address: Operational Base + offset (0xC104)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	en1kpage 1K Page Boundary Enable. By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	RW	0x3	pipe_trans_limit AXI Pipelined Transfers Burst Request Limit. The field controls the number of outstanding pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 4’h0: 1 request 4’h1: 2 requests 4’h2: 3 requests 4’h3: 4 requests ... 4’hF: 16 requests
7:0	RO	0x00	reserved

USB3OTG_GTXTHRCFG

Address: Operational Base + offset (0xC108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29	RO	0x0	USBTxPktCntSel This field enables/disables the USB transmission multi-packet thresholding: 1'b0: USB transmission multi-packet thresholding is disabled; the core can only start transmission on the USB after the entire packet has been fetched into the corresponding TXFIFO. 1'b1: USB transmission multi-packet thresholding is enabled. The core can only start transmission on the USB after USB Transmit Packet Count amounts of packets for the USB transaction (burst) are already in the corresponding TXFIFO. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	RO	0x0	reserved
27:24	RW	0x0	USBTxPktCnt This field specifies the number of packets that must be in the TXFIFO before the core can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15. Note: This field must be less than or equal to the USB Maximum TX Burst Size field.
23:16	RW	0x00	USBMaxTxBurstSize When USBTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the core can do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. You can program a smaller value to this field to limit the TX burst size that the core can execute. Host mode: It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints. Device mode: This value is not used in device mode, but users need to program a value when using the TX threshold feature to make sure that the value programmed in USBTxPktCnt is less than this value. Valid values are from 1 to 16.
15:0	RO	0x0000	reserved

USB3OTG_GRXTHRCFG

Address: Operational Base + offset (0xC10C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	usb_rx_pkt_cntsel USB ReceivePacket Count Enable. This field enables/disables the USB reception multi-packet thresholding: 1'b0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. 1'b1: Not applied. If you are using external buffer control (EBC) feature, disable this mode by setting USBRxPktCntSel to 0.
28:13	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	resvl_socout_spc Space reserved in rx fifo for ISOC OUT. In host mode, this field is not applicable and must be programmed to 0. In device mode, this value represents the amount of space to be reserved for ISOC OUT packets. The value to be programmed should be chosen so as to ensure that non ISOC packets are not completely dropped, If no space needs to be reserved for ISOC OUT packets, program this field to 0. This field is valid only in device mode. The maximum configurable depth of rx fifo is 8192. Therefore, this field is 13 bits wide. For HS/FS, the space reservation is the actual value.

USB3OTG_GCTL

Address: Operational Base + offset (0xC110)

Bit	Attr	Reset Value	Description
31:19	RW	0x026a	pwrdnscale Not applied.
18	RW	0x0	masterfiltbypass Master Filter Bypass When this bit is set to 1'b1, all the filters are bypassed. The double synchronizers to mac clk preceding the filters are also bypassed. For enabling the filters, this bit must be 1'b0.
17	RW	0x0	bypassetaddr Bypass SetAddress in Device Mode. When BYPSSETADDR bit is set, the device core uses the value in the DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, you can use this feature to avoid sending an actual SET ADDRESS control transfer on the USB, and make the device core respond to a new address. Note: You can set this bit for simulation purposes only. In the actual hardware, this bit must be set to 1'b0.
16	RW	0x1	u2rstecn Device controller on USB 2.0 reset checks for receiver termination eight times per attempt if this bit is set to zero, or only once per attempt if the bit is set to one. Note: This bit is applicable only in device mode.
15:14	RW	0x0	frmscldwn This field scales down device view of a SOF/USOF duration. For HS mode: Value of 2'h3 implements interval to be 15.625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be 125us For FS mode, the scale-down value is multiplied by 8. This field also scales down the MaxPacketSize of the IN and OUT bulk endpoint to allow more traffic during simulation. It can only be changed from a non-zero value during simulation. 2'h0: 1024 bytes 2'h1: 512 bytes 2'h2: 256 bytes 2'h3: 128 bytes

Bit	Attr	Reset Value	Description
13:12	RW	0x2	prtcapdir PRTCAPDIR: Port Capability Direction (PrtCapDir) 2'b01: for Host configurations 2'b10: for Device configurations SW should base on IDDIG input to set usb controller as an OTG 2.0 device with A-device or B-device.
11	RW	0x0	coresoftreset Core Soft Reset (CoreSoftReset) 1'b0: No soft reset; 1'b1: Soft reset to core Clears the interrupts and all the CSRs except the following registers: GCTL; GUCTL; GSTS; GSNPSID; GGPIO; GUID; GUSB2PHYCFGn registers; GUSB3PIPECTLn registers; DCFG; DCTL; DEVTEN; DSTS.
10	RW	0x0	sofitpsync Not applied.
9	RW	0x0	u1u2_timescale Not applied.
8	RW	0x0	debugattach Debug Attach. Not applied.
7:6	RW	0x0	ramclksel RAM Clock Select (RAMClkSel) 2'b00: bus clock 2'b01: pipe clock (Only used in device mode) 2'b10: In device mode, pipe/2 clock. In Host mode, controller switches ram_clk between pipe/2 clock, mac2_clk and bus_clk based on the status of the U2 ports 2'b11: In device mode, selects mac2_clk as ram_clk (when 8-bit UTMI or ULPI used. Not supported in 16-bit UTMI mode); In Host mode, controller switches ram_clk between pipe_clk, mac2_clk and bus_clk based on the status of the U2 ports. In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00.
5:4	RW	0x0	scaledown Scale-Down Mode (ScaleDown) When Scale-Down mode is enabled for simulation, the core uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes: 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include Speed enumeration, HNP/SRP, and Host mode suspend and resume 2'b10: Enables scale-down of Device mode suspend and resume timing values only. 2'b11: Enables bit 0 and bit 1 scale-down timing values.
3	RW	0x0	disscramble Disable Scrambling (DisScramble) Transmit request to Link Partner on next transition to Recovery or Polling.

Bit	Attr	Reset Value	Description
2	RW	0x1	u2exit_lfps If this bit is: 1'b0: the link treats 248ns LFPS as a valid U2 exit. 1'b1: the link waits for 8us of LFPS before it detects a valid U2 exit. This bit is added to improve interoperability with a third part host controller. This host controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the device can stay in U2 while ignoring this glitch from the host controller.
1	RO	0x0	gbl_hibernation_en This bit enables hibernation at the global level. If hibernation is not enabled through this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	RW	0x0	dsblclkgtng Disable Clock Gating. This bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset.

USB3OTG_GSTS

Address: Operational Base + offset (0xC118)

Bit	Attr	Reset Value	Description
31:20	RO	0x7e8	cbelt Current BELT Value. In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:12	RO	0x00	reserved
11	RO	0x0	SSIC_IP Not applied.
10	RO	0x0	OTG_IP OTG Interrupt Pending. This field indicates that there is a pending interrupt pertaining to OTG in OEVT register.
9	RO	0x0	bc_ip Battery Charger Interrupt Pending This field indicates that there is a pending interrupt pertaining to BC in BCEVT register.
8	RO	0x0	adp_ip ADP Interrupt Pending. This field indicates that there is a pending interrupt pertaining to ADP in ADPEVT register.
7	RO	0x0	host_ip Host Interrupt Pending. This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.

Bit	Attr	Reset Value	Description
6	RO	0x0	device_ip Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.
5	W1C	0x0	csr_timeout When this bit is 1'b1, it indicates that the software performed a write or read to a core register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: h1FFFF).
4	W1C	0x0	buserraddrvld us Error Address Valid Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	RO	0x0	reserved
1:0	RO	0x0	curmod Current Mode of Operation.

USB3OTG_GUCTL1

Address: Operational Base + offset (0xC11C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	filter_se0_fsls_eop 1'b0: Default behaviour, no change in Linestate check for SE0 detection in FS/LS. 1'b1: Feature enabled, FS/LS SE0 is filtered for 2 clocks for detecting EOP. This bit is applicable for FS/LS operation. If this feature is enabled, then SE0 on the Linestate is validated for 2 consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode: FS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the core will ignore single SE0 glitch on the Linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS. Host mode: FS/LS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the core will ignore single SE0 glitch on the Linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if the Linestate has SE0 glitches during transmission. This bit is quasi-static, i.e., should not be changed during device operation.

Bit	Attr	Reset Value	Description
28	RW	0x0	tx_ipgap_linecheck_dis 1'b0: Default behavior, no change in Linestate check. 1'b1: Feature enable, 2.0 MAC disables Linestate check during HS transmit. This bit is applicable for HS operation of u2mac. If this feature is enabled, then the 2.0 mac operating in HS ignores the UTMI/ULPI Linestate during the transmit of a token (during token-to-token and token-to-data IPGAP). When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the Linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the core will ignore the Linestate after TX and wait for a fixed clocks (40 bit times equivalent) after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap between (tkn to tkn/data) is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if the LineState will not reflect the expected line state (J) during transmission. This bit is quasi-static, i.e., should not be changed during device operation.
27	RW	0x0	dev_trb_out_spr_ind 1'b0: Default behavior, no change in TRB status dword. 1'b1: Feature enable, OUT TRB status indicates Short Packet. This bit is applicable for device mode only (and ignored in host mode). If the device application (SW/HW) wants to know if a short packet was received for an OUT in the TRB status itself, then this feature can be enabled, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the trbstatus, RSVD, SPR,PCM1, bufsize dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, i.e., should not be changed during device operation.
26	RW	0x0	dve_force_20clk_for_30clk Not applied.
25	RW	0x0	p3_in_u2 Not applied.

Bit	Attr	Reset Value	Description
24	RW	0x0	dev_l1_exit_by_hw 1'b0: Default behavior, disables device L1 hardware exit logic. 1'b1: Feature enabled This bit is applicable for device mode (2.0) only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wkp signaling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This HW remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control When control transfers are in progress, the LPM will be rejected (NYET response). Only after control transfers are completed (either with ACK/STALL), LPM will be accepted For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests thru L1. This bit is quasi-static, i.e., should not be changed during device operation.
23:21	RW	0x0	ip_gap_add_on This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC.
20	RW	0x0	dev_lsp_tail_lock_dis 1'b0: Default behaviour, enables device lsp lock logic for tail TRB update. 1'b1: Fix disabled This is a bug fix for STAR 9000716195 that affects the CSP mode for OUT endpoints in device mode. The issue is that tail TRB index is not synchronized with the cache Scratchpad bytecount update. If the fast-forward request comes in-between the bytecount update on a newly fetched TRB and the tail-index write update in TPF, the RDP works on an incorrect tail index and misses the byte count decrement for the newly fetched TRB in the fast-forwarding process. This fix needs to be present all the times.
19	RW	0x0	nak_per_enh_fs 1'b1: Enables performance enhancement for FS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other Full Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your FullSpeed application. Setting this bit will only control, and is only required for Full Speed transfers.

Bit	Attr	Reset Value	Description
18	RW	0x1	nak_per_enh_hs 1'b1: Enables performance enhancement for HS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other High Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your HighSpeed application. Setting this bit will only control, and is only required for High Speed transfers.
17	RW	0x0	parkmode_disbale_ss Not applied.
16	RW	0x0	parkmode_disable_hs This bit is used only in host mode. When this bit is set to 1 all HS bus instances park mode are disabled. To improve performance in park mode, the xHCI scheduler queues in three requests of 4 packets each for High Speed asynchronous endpoints in a micro-frame. But if a device is slow and if it NAKs more than 3 times, then it is rescheduled only in the next micro-frame. This could decrease the performance of a slow device even further. In a few High Speed devices (such as Sandisk Cruzer Blade 4GB VID: 1921, PID: 21863 and Flex Drive VID: 3744, PID: 8552) when an IN request is sent within 900ns of the ACK of the previous packet, these devices send a NAK. When connected to these devices, if required, the software can disable the park mode if you see performance drop in your system. When park mode is disabled, pipelining of multiple packet is disabled and instead one packet at a time is requested by the scheduler. This allows up to 12 NAKs in a micro-frame and improves performance of these slow devices.
15	RW	0x0	parkmod_disavale_fsls This bit is used only in host mode, and is for debug purpose only. When this bit is set to 1 all FS/LS bus instances in park mode disabled.
14:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x1	l1_susp_thrld_en_for_host This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals (see LPM Interface Signals table in the Databook) as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: The HIRD/BESL value used is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: The HIRD/BESL value used is less than the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0.
7:4	RW	0x8	l1_susp_thrld_for_host This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit.
3	RW	0x1	hc_errata_enable Not applied.
2	RW	0x0	hc_parchk_disable Host Parameter Check Disable. When this bit is set to 0 (by default), the xHC checks that the input slot/EP context fields comply to the xHCI Specification. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating PARAMETER ERROR. When the bit is set to 1, the xHC does not perform parameter checks and does not generate PARAMETER ERROR completion code.
1	RW	0x1	ovrld_l1_susp_com If this bit is set, the utmi_l1_suspend_com_n is overloaded with the utmi_sleep_n signal. This bit is usually set if the PHY stops the port clock during L1 sleep condition.
0	RW	0x0	loa_filter_en If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables. Note: This bit is valid only in host mode.

USB3OTG_GSNPSID

Address: Operational Base + offset (0xC120)

Bit	Attr	Reset Value	Description
31:0	RO	0x5533300a	snpsid SNPSID[31:16] indicates Core Identification Number. 0x5533 is ASCII for U3 (DWC_usb3). SNPSID[15:0] indicates the release number. Current Release is 3.00a. Software uses this register to configure release-specific features in the driver.

USB3OTG_GGPIO

Address: Operational Base + offset (0xC124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	gpo General Purpose Output This field's value is driven out on the gp_out[15:0] core output port.
15:0	RO	0x0000	gpi General Purpose Input This field's read value reflects the gp_in[15:0] core input value.

USB3OTG_GUID

Address: Operational Base + offset (0xC128)

Bit	Attr	Reset Value	Description
31:0	RW	0x20190520	userid Application-programmable ID field.

USB3OTG_GUCTL

Address: Operational Base + offset (0xC12C)

Bit	Attr	Reset Value	Description
31:22	RW	0x008	refclkper This field indicates in terms of nano seconds the period of ref_clk. The default value of this register is set to 'h8 (8ns/125 MHz). This field needs to be updated during power-on initialization, if GCTL.SOFITPSYNC or GFLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. The programmable maximum value is 62ns, and the minimum value is 8ns. You must use a reference clock with a period that is an integer multiple, so that ITP can meet the jitter margin of 32ns. The allowable ref_clk frequencies whose period is not integer multiples are 16/17/19.2/24/39.7MHz. This field must not be set to 0 at any time. If you never plan to use this feature, then set this field to 'h8, the default value.
21	RW	0x0	no_extr_di No Extra Delay Between SOF and the First. Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host must wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. 1'b1: Host doesn't wait after a SOF before it sends the first USB packet.
20:18	RO	0x0	reserved
17	RW	0x0	sprs_ctrl_trans_en Sparse Control Transaction Enable. Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames.

Bit	Attr	Reset Value	Description
16	RW	0x0	res_bw_hs_esp Reserving 85% Bandwidth for HS Periodic EPs. By default, HC reserves 80% of the bandwidth for periodic EPs. If this bit is set, the bandwidth is relaxed to 85% to accommodate two high speed, high bandwidth ISOC EPs. USB 2.0 required 80% bandwidth allocated for ISOC traffic. If two High-bandwidth ISOC devices (HD Webcams) are connected, and if each requires 1024-bytes X 3 packets per Micro-Frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 payload per Micro-Frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
15	RW	0x1	cm_dev_addr Compliance Mode for Device Address. When this bit is 1'b1, Slot ID may have different value than Device Address if max_slot_enabled < 128. 1'b1: Increment Device Address on each Address Device command. 1'b0: Device Address is equal to Slot ID. The xHCI compliance requires this bit to be set to 1. The 0 mode is for debug purpose only. This allows you to easily identify a device connected to a port in the Lecroy or Eliisys trace during hardware debug. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
14	RW	0x0	usb_host_in_auto_retry_en Host IN Auto Retry. 1'b0: Auto Retry Disabled 1'b1: Auto Retry Enabled Note: This bit is also applicable to the device mode.
13	RW	0x0	en_overlap_chk Not applied.

Bit	Attr	Reset Value	Description
12	RW	0x0	ext_cap_suppt_en External Extended Capability Support Enable When set, this field enables extended capabilities to be implemented outside the core. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in Debug Capability returns 16. A read to the first DWORD of the last internal extended capability (the "xHCI Supported Protocol Capability for USB 3.0" when the Debug Capability is not enabled) returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability (for example, at address N+16 where N is the address of this DWORD). If enabled, an external address decoder that snoops the xHC slave interface must be implemented. If it sees an access to N+16 or greater, the slave access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer' field. This indicates there are no more capabilities.
11	RW	0x0	insrt_extr_fsbodi Insert Extra Delay Between FS Bulk OUT. Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. Note: Setting this bit to one will reduce the Bulk OUT transfer performance for most of the FS devices.
10:9	RW	0x0	dtct Device Timeout Coarse Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The core first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: 2'b00: 0 usec -> use DTFT value instead 2'b01: 500 usec 2'b10: 1.5 msec 2'b11: 6.5 msec

Bit	Attr	Reset Value	Description
8:0	RW	0x010	ctft Device Timeout Fine Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For the DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. The minimum value of DTFT is 2. For example, if the mac3_clk is 125 MHz clk (8 ns period), this is calculated as follows: (DTFT value) * 256 * (8 ns) Quick Reference: if DTFT = 0x2, 2*256*8 = 4usec timeout if DTFT = 0x5, 5*256*8 = 10usec timeout if DTFT = 0xA, 10*256*8 = 20usec timeout if DTFT = 0x10, 16*256*8 = 32usec timeout if DTFT = 0x19, 25*256*8 = 51usec timeout if DTFT = 0x31, 49*256*8 = 100usec timeout if DTFT = 0x62, 98*256*8 = 200usec timeout

USB3OTG_GBUSERRADDRLO

Address: Operational Base + offset (0xC130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	buserraddr Bus Address - Low. This register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

USB3OTG_GBUSERRADDRHI

Address: Operational Base + offset (0xC134)

Bit	Attr	Reset Value	Description
31:0	RU	0x00000000	buserraddr Bus Address - High. This register contains the higher 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

USB3OTG_GPRTBIMAPLO

Address: Operational Base + offset (0xC138)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	BINUM1 SS USB Instance Number for Port 1 Application-programmable ID field.

USB3OTG_GHWPARAMS0

Address: Operational Base + offset (0xC140)

Bit	Attr	Reset Value	Description
31:0	RO	0x2020400a	ghwparams0 Global Hardware Parameters Register 0.

USB3OTG_GHWPARAMS1
Address: Operational Base + offset (0xC144)

Bit	Attr	Reset Value	Description
31:0	RO	0x0120c93b	ghwparams1 Global Hardware Parameters Register 1.

USB3OTG_GHWPARAMS2
Address: Operational Base + offset (0xC148)

Bit	Attr	Reset Value	Description
31:0	RO	0x20190520	ghwparams2 Global Hardware Parameters Register 2.

USB3OTG_GHWPARAMS3
Address: Operational Base + offset (0xC14C)

Bit	Attr	Reset Value	Description
31:0	RO	0x069cd084	ghwparams3 Global Hardware Parameters Register 3.

USB3OTG_GHWPARAMS4
Address: Operational Base + offset (0xC150)

Bit	Attr	Reset Value	Description
31:0	RO	0x47822010	ghwparams4 Global Hardware Parameters Register 4.

USB3OTG_GHWPARAMS5
Address: Operational Base + offset (0xC154)

Bit	Attr	Reset Value	Description
31:0	RO	0x04204018	ghwparams5 Global Hardware Parameters Register 5.

USB3OTG_GHWPARAMS6
Address: Operational Base + offset (0xC158)

Bit	Attr	Reset Value	Description
31:0	RO	0x09d78020	ghwparams6 Global Hardware Parameters Register 6.

USB3OTG_GHWPARAMS7
Address: Operational Base + offset (0xC15C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ghwparams7 Global Hardware Parameters Register 7.

USB3OTG_GDBGFIFOSPACE
Address: Operational Base + offset (0xC160)

Bit	Attr	Reset Value	Description
31:16	RO	0x000a	space_available Space Available.
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8:0	RW	0x000	fifo_queue_select FIFO/Queue Select (or) Port-Select. FIFO/Queue Select[8:5] indicates the FIFO/Queue Type. FIFO/Queue Select[4:0] indicates the FIFO/Queue Number. Port-Select[3:0] selects the port-number when accessing GDBGLTSSM register.

USB3OTG_GDBGLNMCC

Address: Operational Base + offset (0xC168)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	lnmcc_berc This field indicates the bit error rate information for the port selected in the GDBGFIFOSPACE.PortSelect field. This field is for debug purposes only.

USB3OTG_GDBGBMU

Address: Operational Base + offset (0xC16C)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	bmu_bcu BMU_BCU Debug information.
7:4	RO	0x0	bmu_dcu BMU_DCU Debug information.
3:0	RO	0x0	bmu_ccu BMU_CCU Debug information.

USB3OTG_GDBGLSPMUX

Address: Operational Base + offset (0xC170)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x3f	logic_analyzer_trace Logic Analyzer Trace Port MUX Select. Currently only bits[21:16] are used. A value of 6'h3F drives "0"s on the logic_analyzer_trace signal. If you plan to OR (instead using a mux) this signal with other trace signals in your system to generate a common trace signal, you can use this feature.
15	RW	0x0	endbc Enable debugging of Debug capability LSP in Host mode. Use HostSelect to select DbC LSP debug information presented in the GDBGLSP register.
14	RO	0x0	Reserved
13:8	RW	0x00	hostselect Host LSP Select. Selects the LSP debug information presented in the GDBGLSP register in host mode.
7:4	RW	0x0	devselect Device LSP Select. Selects the LSP debug information presented in the GDBGLSP register in device mode. Or bit[7:4] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	epselect Device Endpoint Select. Selects the Endpoint debug information presented in the GDBGEPINFO registers in device mode. Or bit[3:0] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.

USB3OTG_GDBGLSP
Address: Operational Base + offset (0xC174)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lspdebug LSP Debug Information.

USB3OTG_GDBGEPINFO0
Address: Operational Base + offset (0xC178)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	epdebug Endpoint Debug Information Low 32-bit.

USB3OTG_GDBGEPINFO1
Address: Operational Base + offset (0xC17C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00800000	epdebug Endpoint Debug Information High 32-bit.

USB3OTG_GPRTBIMAP_HSLO
Address: Operational Base + offset (0xC180)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 HS USB Instance Number for Port 1. Application-programmable ID field.

USB3OTG_GPRTBIMAP_FSLO
Address: Operational Base + offset (0xC188)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 FS USB Instance Number for Port 1. Application-programmable ID field.

USB3OTG_GUSB2PHYCFG0
Address: Operational Base + offset (0xC200)

Bit	Attr	Reset Value	Description
31	RW	0x0	physoftrst UTMI PHY Soft Reset. Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl. Reset register, and the core automatically writes to this register when the core is reset (vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset).

Bit	Attr	Reset Value	Description
30	RW	0x1	u2_freeclk_exists Specifies whether your USB 2.0 PHY provides a free-running PHY clock, which is active when the clock control input is active. If your USB 2.0 PHY provides a free-running PHY clock, it must be connected to the utmi_clk[0] input. The remaining utmi_clk[n] must be connected to the respective port clocks. The core uses the Port-0 clock for generating the internal mac2 clock. 1'b0: USB 2.0 free clock does not exist 1'b1: USB 2.0 free clock exists Note: When the core is configured as device-only, do not set this bit to 1.
29:25	RO	0x00	reserved
24:22	RW	0x0	lstrd LS Turnaround Time. This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h0 (2 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the Open LS mouse requires 3 bit times of inter-packet gap to work correctly.
21:19	RW	0x2	lsipd LS Inter-Packet Time. This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h2 (3 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly.
18:14	RO	0x00	reserved

Bit	Attr	Reset Value	Description
13:10	RW	0x9	usbtrdim USB 2.0 Turnaround Time. Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). The following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+/ULPI. If SoC bus clock is less than 60 MHz, and USB turnaround time is not critical, this field can be set to a larger value. Note: This field is valid only in device mode.
9	RW	0x0	xcvrdly Transceiver Delay. Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal (for HS) and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay (of approximately 2.5 us) is introduced from the time when the Transceiver Select is set to 2'b00 (HS) to the time the TxValid is driven to 0 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: If you enable the hibernation feature when the device core comes out of power-off, you must re-initialize this bit with the appropriate value because the core does not save and restore this bit value during hibernation. This bit is valid only in device mode.
8	RW	0x0	enblslpm Enable utmi_sleep_n and utmi_l1_suspend_n. The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is not transferred to the external PHY. 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is transferred to the external PHY. Note: This bit must be set high for Port0 if SNPS PHY is used. In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
7	RO	0x0	physel USB 2.0 High-Speed PHY or USB 1.1 Full-Speed. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY. 1'b1: USB 1.1 full-speed serial transceiver.

Bit	Attr	Reset Value	Description
6	RW	0x0	suspendusb20 Suspend USB2.0 HS/FS/LS PHY. When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the core initialization completes. For all other configurations, this bit can be set to 1 during core configuration. Note: In host mode, on reset, this bit is set to 1. Software can override this bit after reset. In device mode, before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. If you issue a command without disabling this bit when the device is in L2 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
5	RO	0x0	reserved
4	RO	0x0	ulpi_utmi_sel ULPI or UTMI+ Select. 1'b0: UTMI+ Interface 1'b1: ULPI Interface
3	RW	0x0	phyif If UTMI+ is selected, the application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. 1'b0: 8 bits 1'b1: 16 bits
2:0	RW	0x0	tout_cal HS/FS Timeout Calibration. The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor; this factor is added to the high-speed/full-speed interpacket timeout duration in the core to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times

USB3OTG_GUSB3PIPECTL0

Address: Operational Base + offset (0xC2C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHYSoftRst USB3 PHY Soft Reset After setting this bit to 1, the software needs to clear this bit.

Bit	Attr	Reset Value	Description
30	RW	0x0	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.0 cable. This bit enables placing the SS port link into a compliance state. By default, this bit must be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows: 1. Disconnect any plugged in devices. 2. Perform USBCMD.HCRST or power-on-chip reset. 3. Set PORTSC.PP=0. 4. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence (toggle the set GUSB3PIPECTL. HstPrtCmpl): 1. Set GUSB3PIPECTL.HstPrtCmpl=0. 2. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state perform USBCMD.HCRST or power-on-chip reset.
29	RW	0x0	U2SSInactP3ok 1’b0: During link state U2/SS.Inactive, put PHY in P2 (Default) 1’b1: During link state U2/SS.Inactive, put PHY in P3
28	RW	0x0	DisRxDetP3 Disabled receiver detection in P3 1’b0: If PHY is in P3 and Core needs to perform receiver detection, The core performs receiver detection in P3. (Default) 1’b1: If PHY is in P3 and Core needs to perform receiver detection, The core changes the PHY power state to P2 and then performs receiver detection. After receiver detection, the cores changes PHY power state to P3.
27	RW	0x0	Ux_exit_in_Px 1’b0: The core does U1/U2/U3 exit in PHY power state P0 (default behavior). 1’b1: The core does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively.
26	RW	0x0	ping_enhancement_en Ping Enhancement Enable When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for the downstream port only.
25	RW	0x0	u1u2exitfail_to_recov U1U2exitfail to Recovery When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake.

Bit	Attr	Reset Value	Description
24	RW	0x0	request_p1p2p3 Always Request P1/P2/P3 for U1/U2/U3 When set, the core always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit (remotely initiated, or locally initiated) happens, the core does not request P1/P2/P3 power state change.
23	RW	0x0	StartRxDetU3RxDet Start Receiver Detection in U3/Rx.Detect (StartRxdetU3RxDet) If DWC_USB3_GUSB3PIPECTL_INIT[22] is set, and the link is in either U3 or Rx.Detect state, the core starts receiver detection on the rising edge of this bit. This can only be used for Downstream ports. This bit must be set to '0' for Upstream ports. This feature must not be enabled for normal operation.
22	RW	0x0	DisRxDetU3RxDet Disable Receiver Detection in U3/Rx.Det When set, the core does not handle receiver detection in either U3 or Rx.Detect states. DWC_USB3_GUSB3PIPECTL_INIT[23] must be used to start receiver detection manually. This bit can only be used for the downstream port. This bit must be set to 0 for Upstream ports. This feature must not be enabled for normal operation. If you have to use this feature, contact SNPS.
21:19	RW	0x0	DelayP1P2P3 Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality.
18	RW	0x0	DELAYP1TRANS DELAYP1TRANS Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit must be set to '1' for SNPS PHY. It is also used by third-party SS PHY.
17	RW	0x0	SUSPENDENABLE Suspend USB3.0 SS PHY (Suspend_en) When set, and if Suspend conditions are valid, the USB 3.0 PHY enters Suspend mode. Application needs to set it to '1' after the core initialization is completed.
16:15	RW	0x0	DATWIDTH 2'b00: 32 bits 2'b01: 16 bits 2'b10: 8 bits One clock after reset, these bits receive the value seen on the pipe3_DataBusWidth.

Bit	Attr	Reset Value	Description
14	RW	0x0	AbortRxDetInU2 Abort Rx Detect in U2 (AbortRxDetInU2) When set, and the link state is U2, then the core will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for the downstream port only.
13	RW	0x0	SkipRxDet Skip Rx Detect: When set, the core skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
12	RW	0x0	LFPSP0Algn LFPS P0 Align When set: 1. The core deasserts LFPS transmission on the clock edge that it requests PHY power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. 2. The core requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. Currently, this bit is only used in USB 3.0 HUB with SNPS PHY. For other USB 3.0 Host, Device, and DRD cores, this bit is not required.
11	RW	0x0	P3P2TranOK P3 P2 Transitions OK (P3P2TranOK) When set, the core transitions directly from PHY power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 Specification. According to the PIPE3 Specification, any direct transition between P3 and P2 is illegal.
10	RW	0x0	P3ExSigP2 P3 Exit Signal in P2 When this bit is set, the core always changes the PHY power state to P2, before attempting a U3 exit handshake. This bit is used only for some non-SNPS PHYs that cannot do LFPS in P3.
9	RW	0x0	LFPSFILTER LFPS Filter When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted.

Bit	Attr	Reset Value	Description
8	RW	0x0	RX_DETECT_to_Polling_L RX_DETECT to Polling.LFPS Control 1'b0 (Default): Enables a 400us delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. 1'b1: Disables the 400us delay to start Polling LFPS after RX_DETECT. During controller certification with third party PHY it is observed that the PHY is not able to meet the Tx AC common mode voltage active (VTX-CM-ACPP_ACTIVE <100mv) if the link starts polling within 80us from the time rx.detect is performed. To meet this VTX-CM-ACPP_ACTIVE specification, the polling must be delayed further. If the PHY does not have issue then they can set this bit to 1 which allows polling to start within 80us.
7	RO	0x0	reserved
6	RW	0x0	TX_SWING Tx Swing (TxSwing) Refer to the PIPE3 specification.
5:3	RW	0x0	TX_MARGIN Tx Margin[2:0] (TxMargin) Refer to Table 5-3 of the PIPE3 Specification.
2:1	RW	0x0	TX_DE_EPPHASIS Tx Deemphasis The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode.
0	RW	0x0	ELASTIC_BUFFER_MODE Elastic Buffer Mode (ElasticBufferMode) (Refer to Table 5-3 of the PIPE3 specification.)

USB3OTG_GTXFIFOSIZn

Address: Operational Base + offset (0xC300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	txfstaddr_n Transmit FIFOn RAM Start Address. This field contains the memory start address for TxFIFOn in 64-bit words.
15:0	RW	0x0042	txfdep_n TxFIFO Depth. This field contains the depth of TxFIFOn in 64-bit words. Minimum value: 32; Maximum value: 32,768.

USB3OTG_GRXFIFOSIZn

Address: Operational Base + offset (0xC380)

Bit	Attr	Reset Value	Description
31:16	RW	0x0334	rxfstaddr_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.
15:0	RW	0x0185	rxfdep_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.

USB3OTG_GEVNTADRLO0

Address: Operational Base + offset (0xC400)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrlo Event Buffer Address. Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

USB3OTG_GEVNTADRHI0

Address: Operational Base + offset (0xC404)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrhi Event Buffer Address. Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

USB3OTG_GEVNTSIZ0

Address: Operational Base + offset (0xC408)

Bit	Attr	Reset Value	Description
31	RW	0x0	evntintrptmask Event Interrupt Mask. When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued.
30:16	RO	0x0000	reserved
15:0	RW	0x0000	eventsiz Event Buffer Size in bytes. Holds the size of the Event Buffer in bytes; must be a multiple of four. This is programmed by software once during initialization. The minimum size of the event buffer is 32 bytes.

USB3OTG_GEVNTCOUNT0

Address: Operational Base + offset (0xC40C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	evntcount Event Count. When read, returns the number of valid events in the Event Buffer (in bytes). When written, hardware decrements the count by the value written. The interrupt line remains high when count is not 0.

USB3OTG_GHWPARAMS8

Address: Operational Base + offset (0xC600)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000047c	ghwparams8_32_0 ghwparams8

USB3OTG_GTXFIFOPRIDEV

Address: Operational Base + offset (0xC610)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	gtxfifopridev Device TxFIFO priority. This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. High-priority TXFIFOs are granted access using round-robin arbitration 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the core is configured to operate in the device mode. The register size corresponds to the number of Device IN endpoints.

USB3OTG_GTXFIFOPRIHST

Address: Operational Base + offset (0xC618)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	gtxfifoprihst Host TxFIFO priority. This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). 2. The TX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

USB3OTG_GRXFIFOPRIHST
Address: Operational Base + offset (0xC61C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	grxfifoprihst Host RxFIFO priority This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). 2. The RX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

USB3OTG_GFIFOPRIDBC
Address: Operational Base + offset (0xC620)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	gfifopridbc Host DbC DMA priority. This register specifies the relative priority of the RXFIFOs and TXFIFOs associated with the DbC mode. It overrides the priority assigned in the corresponding indexes of the Host RXFIFO and TXFIFO DMA priority registers, when the DbC mode is enabled.

USB3OTG_GDMAHLRATIO
Address: Operational Base + offset (0xC624)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:8	RW	0x0000	hstrxfifo Host RXFIFO DMA High-Low Priority.
7:5	RO	0x0	reserved
4:0	RW	0x00	hsttxfifo Host TXFIFO DMA High-Low Priority.

USB3OTG_GFLADJ
Address: Operational Base + offset (0xC630)

Bit	Attr	Reset Value	Description
31	RW	0x0	gfladj_refclk_240mhzdecr_pls1 This field indicates that the decrement value that the controller applies for each ref_clk must be GFLADJ_REFCLK_240MHZ_DECR and GFLADJ_REFCLK_240MHZ_DECR +1 alternatively on each ref_clk. Set this bit to a 1 only if GFLADJ_REFCLK_LPM_SEL is set to 1 and the fractional component of 240/ref_frequency is greater than or equal to 0.5. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = (240/24) = 10 3. GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 0
30:24	RW	0x00	gfladj_refclk_240mhz_decr This field indicates the decrement value that the controller applies for each ref_clk in order to derive a frame timer in terms of a 240-MHz clock. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1. The value is derived as follows: GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/24 = 10
23	RW	0x0	gfladj_refclk_lpm_sel This bit enables the functionality of running SOF counters on the ref_clk. This bit must not be set to 1 if GCTL.SOFITPSYNC bit is set to 1. Similarly, if GFLADJ_REFCLK_LPM_SEL set to 1, GCTL.SOFITPSYNC must not be set to 1. Note that the ref_clk frequencies supported in this mode are 16/17/19.2/20/24/39.7/40 MHz. The utmi_clk[0] signal of the core must be connected to the FREECLK of the PHY. Note: If you set this bit to 1, the GUSB2PHYCFG.U2_FREECLK_EXISTS bit must be set to 0.
22	RO	0x0	reserved
21:8	RW	0x0000	gfladj_refclk_fladj This field indicates the frame length adjustment to be applied when SOF counter is running on the ref_clk. SOF interval when GLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1 or GCTL.SOFITPSYNC is set to 1. The value is derived as follows: FLADJ_REF_CLK_FLADJ=((125000/ref_clk_period_integer) - (125000/ref_clk_period)) * ref_clk_period where: 1. The ref_clk_period_integer is the integer value of the ref_clk period got by truncating the decimal (fractional) value that is programmed in the GUCTL.REF_CLK_PERIOD field. 2. The ref_clk_period is the ref_clk period including the fractional value. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GLADJ_REFCLK_FLADJ = ((125000/41) - (125000/41.6666)) * 41.6666 = 2032 (ignoring the fractional value).

Bit	Attr	Reset Value	Description
7	RW	0x0	gfladj_30mhz_sdbnd_sel This field selects whether to use the input signal fladj_30mhz_reg or the GFLADJ.GFLADJ_30MHZ to adjust the frame length for the SOF. When this bit is set to: 1'b1: the controller uses the register field GFLADJ.GFLADJ_30MHZ value 1'b0: the controller uses the input signal fladj_30mhz_reg value.
6	RO	0x0	reserved
5:0	RW	0x00	gfadj_30mhz This field indicates the value that is used for frame length adjustment instead of considering from the sideband input signal fladj_30mhz_reg. This enables post-silicon frame length adjustment in case the input signal fladj_30mhz_reg is connected to a wrong value or is not valid. For details on how to set this value, refer to section 5.2.4, "Frame Length Adjustment Register (FLADJ)," of the xHCI Specification.

USB3OTG_DCFG
Address: Operational Base + offset (0xC700)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	ignstrmpp This bit only affects stream-capable bulk endpoints. Not applied.
22	RW	0x0	lpmcap LPM Capable. Not applied.
21:17	RW	0x04	nump Number of Receive Buffers. Not applied.
16:12	RW	0x00	intrnum Interrupt number. Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts (see DEVT) are generated.
11:10	RO	0x0	reserved
9:3	RW	0x00	devaddr Device Address. The application must perform the following: 1. Program this field after every SetAddress request. 2. Reset this field to zero after USB reset.
2:0	RW	0x0	devspd Device Speed. Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 3'b000: High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 3'b001: Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)

USB3OTG_DCTL
Address: Operational Base + offset (0xC704)

Bit	Attr	Reset Value	Description
31	RW	0x0	run_stop The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1. After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2. The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared is specified in the Note below. If the software attempts a connect after the soft disconnect or detects a disconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stop bit. 3. When the USB is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller. Note: The following is the minimum duration under various conditions for which the soft disconnect (SftDiscon) bit must be set for the USB host to detect a device disconnect: 10ms: For high-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions); For full-speed/low-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions). To accommodate clock jitter, it is recommended that the application add extra delay to the specified minimum duration.

Bit	Attr	Reset Value	Description
30	R/W SC	0x0	csftrst Core Soft Reset. Reset all clock domains as follows: 1. This bit clears the interrupts and all the CSRs except GSTS, GSNPSID, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. 2. All module state machines (except the SoC Bus Slave Unit) are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. 3. Any transactions on the SoC bus Master are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the core. This is a self-clearing bit; the core clears this bit after all necessary logic is reset in the core, which may take several clocks depending on the core's current state. Once this bit is cleared, the software must wait at least 3 PHY clocks before accessing the PHY domain (synchronization delay). Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation.
29	RO	0x0	reserved
28:24	RW	0x00	hirdthres HIRD Threshold. The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: 1. HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] 2. HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: 1. If the HIRD value is less than HIRD_Thres[3:0] or 2. HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation.

Bit	Attr	Reset Value	Description
23:20	RW	0xf	lpm_nyet_thres LPM NYET Threshold Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. DCFG.LPMCap is 1'b0 - The core always responds with Timeout (that is, no response). DCFG.LPMCap is 1'b1 - The core responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: 1. There are no PID or CRC5 errors in both the EXT token and the LPM token (if not true, inactivity results in a timeout ERROR). 2. No data is pending in the Transmit FIFO and OUT endpoints not in flow controlled state (else NYET). 3. The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0].
19	RW	0x0	keep_connect When 1, this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to 0. The device core disconnects from the host when DCTL.RunStop is set to 0. This bit indicates whether to preserve this behavior (0), or if the core must not disconnect when RunStop is set to 0 (1).
18	RW	0x0	l1_hibernation_en When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core does not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	RW	0x0	crs Controller Restore State. This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to 1, the controller immediately sets DSTS.RSS to 1. When the controller has finished the restore process, it sets DSTS.RSS to 0. Note: When read, this field always returns 0.
16	RW	0x0	css Controller Save State. This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to 1, the controller immediately sets DSTS.SSS to 1. When the controller has finished the save process, it sets DSTS.SSS to 0. Note: When read, this field always returns 0.
15:13	RO	0x0	reserved
12	RW	0x0	initu2ena Not applied.
11	RW	0x0	acceptu2ena Not applied.
10	RW	0x0	initu1ena Not applied.
9	RW	0x0	acceptu1ena Not applied.

Bit	Attr	Reset Value	Description
8:5	RW	0x0	ulstchngreq Software writes this field to issue a USB state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. In HS/FS/LS mode: Value: Requested USB state transition 8: Remote wakeup request Others: Reserved The Remote wakeup request must be issued 2us after the device goes into suspend state (DSTS[21:18] is 3). Note: After coming out of hibernation, software must write 8 (Recovery) into this field to confirm exit from the suspended state.
4:1	RW	0x0	tstctl Test Control. 4'b000: Test mode disabled 4'b001: Test_J mode 4'b010: Test_K mode 4'b011: Test_SE0_NAK mode 4'b100: Test_Packet mode 4'b101: Test_Force_Enable Others: Reserved
0	RO	0x0	reserved

USB3OTG_DEVTEN

Address: Operational Base + offset (0xC708)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	vendevtstrcvden Vendor Device Test LMP Received Event. 1'b0: Disable this event 1'b1: Enable this event
11:10	RO	0x0	reserved
9	RW	0x0	errticerrevten Erratic Error Event Enable. 1'b0: Disable this event 1'b1: Enable this event
8	RO	0x0	reserved
7	RW	0x0	softevten Start of (u)frame Event Enable. 1'b0: Disable this event 1'b1: Enable this event
6	RW	0x0	u3l2l1_susp_en U3/L2-L1 Suspend Event Enable. 1'b0: Disable this event 1'b1: Enable this event

Bit	Attr	Reset Value	Description
5	RW	0x0	hibernation_req_evt_en Hibernation Request Event Enable. 1'b0: Disable this event 1'b1: Enable this event
4	RW	0x0	wkupevten Resume/Remote Wakeup Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event
3	RW	0x0	ulstcngen USB State Change Event Enable. 1'b0: Disable this event 1'b1: Enable this event
2	RW	0x0	connectdoneevten Connection Done Event Enable. 1'b0: Disable this event 1'b1: Enable this event
1	RW	0x0	usbrstevten USB Reset Event Enable. 1'b0: Disable this event 1'b1: Enable this event
0	RW	0x0	disconnevten Disconnect Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event

USB3OTG_DSTS

Address: Operational Base + offset (0xC70C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	dcnrd Device Controller Not Ready. The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to 1 and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt.
28:26	RO	0x0	reserved
25	RW	0x0	rss Restore State Status. This bit is similar to the USBSTS.RSS in host mode. When the controller finishes the restore process, it completes the command by setting DSTS.RSS to 0.
24	RO	0x0	sss Save State Status. This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to 0.

Bit	Attr	Reset Value	Description
23	RO	0x0	coreidle Core Idle. The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero. Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the core and does not hold a static value.
22	RO	0x1	devctrlhlt Device Controller Halted. This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to 0, the core is idle and the lower layer finishes the disconnect process. When Halted=1, the core does not generate Device events. Note: The core does not set this bit to 1 if GEVNTCOUNTn has some valid value. Software needs to acknowledge the events that are generated (by writing to GEVNTCOUNTn) while it is waiting for this bit to be set to 1.
21:18	RO	0x4	usblnkst USB/Link State In SS mode: LTSSM State 4'h0: U0 4'h1: U1 4'h2: U2 4'h3: U3 4'h5: RX_DET 4'h6: SS_INACT 4'h7: POLL 4'h8: RECOV 4'h9: HRESET 4'ha: CMPLY 4'hb: LPBK 4'hf: Resume/Reset In HS/FS/LS mode: 4'h0: On state 4'h2: Sleep (L1) state 4'h3: Suspend (L2) state 4'h4: Disconnected state (Default state) 4'h5: Early Suspend state (valid only when Hibernation is disabled, GCTL[1].GblHibernationEn = 0) 4'he: Reset (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) 4'hf: Resume (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) The link state Resume/Reset indicates that the core received a resume or USB reset request from the host while the link was in hibernation. Software must write 8 (Recovery) to the DCTL.ULStChngReq field to acknowledge the resume/reset request. When Hibernation is enabled, GCTL[1].GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL[31].Run/Stop set to 1 and DSTS[29].DCNRD = 0.
17	RO	0x1	rx_fifo_empty Rx Fifo Empty.

Bit	Attr	Reset Value	Description
16:3	RO	0x0000	reserved
2:0	RU	0x0	connectspd Connected Speed. Indicates the speed at which the DWC_usb3 core has come up after speed detection through a chirp sequence. 3'b000: High-speed (PHY clock is running at 30 or 60 MHz) 3'b001: Full-speed (PHY clock is running at 30 or 60 MHz)

USB3OTG_DGCMDPAR

Address: Operational Base + offset (0xC710)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the device command parameter. This must be programmed before or along with the device command. The available device commands are listed in DGCMD register.

USB3OTG_DGCMD

Address: Operational Base + offset (0xC714)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	cmdstatus Command Status: 1'b1: CmdErr: Indicates that the device controller encountered an error while processing the command. 1'b0: Indicates command success
11:10	RO	0x0	reserved
9	R/W SC	0x0	cmdact Command Active. The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:0	RW	0x00	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 8'h0: Reserved 8'h1: Set Endpoint Configuration - 64 or 96-bit Parameter 8'h2: Set Endpoint Transfer Resource Configuration - 32-bit Parameter 8'h3: Get Endpoint State - No Parameter Needed 8'h4: Clear Stall (see Set Stall) - No Parameter Needed 8'h5: Start Transfer - 64-bit Parameter 8'h6: Update Transfer - No Parameter Needed 8'h7: End Transfer - No Parameter Needed 8'h8 Start New Configuration - No Parameter Needed

USB3OTG_DALEPENA

Address: Operational Base + offset (0xC720)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbactep USB Active Endpoints. This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0~15 and OUT endpoints 0~15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN ... The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints (resources) after USBReset. Hardware clears these bits for all endpoints (other than EP0-OUT and EP0-IN) after detecting a USB reset event. After receiving SetConfiguration and SetInterface requests, the application must program endpoint registers accordingly and set these bits.

USB3OTG_DEPnCMDPAR2

Address: Operational Base + offset (0xC800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

USB3OTG_DEPnCMDPAR1

Address: Operational Base + offset (0xC804)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command.

USB3OTG_DEPnCMDPAR0

Address: Operational Base + offset (0xC808)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 0. It must be programmed before issuing the command.

USB3OTG_DEPnCMD

Address: Operational Base + offset (0xC80C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	commandparam Command Parameters or Event Parameters when this register is written: For Start Transfer command: The 16-bit StreamID assigned to this transfer. For Start Transfer command applied to an isochronous endpoint: StartMicroFramNum, Indicates the (micro) frame number to which the first TRB applies. For Update Transfer, End Transfer, and Start New Configuration commands: [22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. Event Parameters (EventParam), when this register is read.
15:12	RW	0x0	cmdstatus Command Completion Status. The information is in the same format as bits 15:12 of the Endpoint Command Complete event.
11	RW	0x0	hipri_forcerm HighPriority: Only valid for Start Transfer command. ForceRM: Only valid for End Transfer command. ClearPendIN: Only valid for Clear Stall command. Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.
10	RW	0x0	cmdact Command Active. Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	RO	0x0	reserved
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 4'h0: Reserved 4'h1: Set Endpoint Configuration 64 or 96-bit Parameter 4'h2: Set Endpoint Transfer Resource Configuration - 32-bitparameter 4'h3: Get Endpoint State - No Parameter Needed 4'h4: Set Stall - No Parameter Needed 4'h5: Clear Stall (see Set Stall) - No Parameter Needed 4'h6: Start Transfer - 64-bit Parameter 4'h7: Update Transfer - No Parameter Needed 4'h8: End Transfer - No Parameter Needed 4'h9: Start New Configuration - No Parameter Needed

13.5 Interface Description

Table 13-2 USB3OTG_0 Interface Description

Pad Name	Direction	Descriptions
TYPEC0_SBU2/DP0_AUXN	I/O	USBDP PHY AUX differential serial data line
TYPEC0_SBU1/DP0_AUXP	I/O	
TYPEC0_SSRX1N/DP0_TX0N	I/O	Received Differential Data for USB3.0
TYPEC0_SSRX1P/DP0_TX0P	I/O	
TYPEC0_SSTX1N/DP0_TX1N	I/O	Transmitted Different Data for USB3.0
TYPEC0_SSTX1P/DP0_TX1P	I/O	
TYPEC0_SSRX2N/DP0_TX2N	I/O	Received Differential Data for USB3.0
TYPEC0_SSRX2P/DP0_TX2P	I/O	
TYPEC0_SSTX2N/DP0_TX3N	I/O	Transmitted Different Data for USB3.0
TYPEC0_SSTX2P/DP0_TX3P	I/O	
TYPEC0_DP0_REXT	I/O	USBDP PHY External Reference Resistor
TYPEC0_USB20_OTG_DM	I/O	USB D- Signal
TYPEC0_USB20_OTG_DP	I/O	USB D+ Signal
TYPEC0_USB20_OTG_ID	I/O	USB2.0 PHY Mini-Receptacle Identifier
TYPEC0_USB20_OTG0_REXT	I/O	USB2.0 PHY Transmitter Resistor Tune Pin
TYPEC0_USB20_VBUSDET	I/O	USB2.0 PHY VBUS

Table 13-3 USB3OTG_1 Interface Description

Pad Name	Direction	Descriptions
TYPEC1_SBU2/DP1_AUXN	I/O	USBDP PHY AUX differential serial data line
TYPEC1_SBU1/DP1_AUXP	I/O	
TYPEC1_SSRX1N/DP1_TX0N	I/O	Received Differential Data for USB3.0
TYPEC1_SSRX1P/DP1_TX0P	I/O	
TYPEC1_SSTX1N/DP1_TX1N	I/O	Transmitted Different Data for USB3.0
TYPEC1_SSTX1P/DP1_TX1P	I/O	
TYPEC1_SSRX2N/DP1_TX2N	I/O	Received Differential Data for USB3.0
TYPEC1_SSRX2P/DP1_TX2P	I/O	
TYPEC1_SSTX2N/DP1_TX3N	I/O	Transmitted Different Data for USB3.0
TYPEC1_SSTX2P/DP1_TX3P	I/O	
TYPEC1_DP0_REXT	I/O	USBDP PHY External Reference Resistor
TYPEC1_USB20_OTG_DM	I/O	USB D- Signal
TYPEC1_USB20_OTG_DP	I/O	USB D+ Signal
TYPEC1_USB20_OTG_ID	I/O	USB2.0 PHY Mini-Receptacle Identifier
TYPEC1_USB20_OTG0_REXT	I/O	USB2.0 PHY Transmitter Resistor Tune Pin
TYPEC1_USB20_VBUSDET	I/O	USB2.0 PHY VBUS

Table 13-4 USB3OTG_2 Interface Description

Pad Name	Direction	Descriptions
PCIE20_2_RXN/SATA30_2_RXN/USB30_SSRXN	I/O	Received Differential Data for USB3.0
PCIE20_2_RXP/SATA30_2_RXP/USB30_SSRXP	I/O	
PCIE20_2_TXN/SATA30_2_TXN/USB30_SSTXN	I/O	Transmitted Different Data for USB3.0
PCIE20_2_TXP/SATA30_2_TXP/USB30_SSTXP	I/O	

13.6 Application Notes

13.6.1 Some Settings About USB3OTG_0 and USB3OTG_1

- **USB3 mode initial sequence**

In this application USBDP PHY will use 24Mhz reference clock, some initial sequence should be set and USB mode should be configured before working. Please refer to USBDP PHY section.

- **Power Down Mode**

When no transfer happened, PD_USB can be power down in application. At this time the PowerDown signal to USBDP PHY PIPE interface will be clamped to 3'b3. But there is also a MUX near USBDP PHY which could choose form GRF. Also, RxTermination, TxElecIdle and TxDetectRxLoopbx can also be control by GRF, this could be found in USBDPGRF_CON3 in GRF section.
If USB and DP not be used, USBDPPHY could also be power down, and before power down, USBDPGRF_CON2[15] will use to clamp the PHY output signal.

- **PhyStatus in PIPE Interface for USB2 only**

If only USB2 is used and USBDP PHY initial sequence not correctly processes, the PIPE interface signal PhyStatus may be set to 1'b1, USB3OTG0/1_CON1[3:2] can be set to control PhyStatus.

13.6.2 USB3OTG_2 mode setting

In USB3OTG_2 subsystem, PHY is combo with PCIE and SATA, so you must set some GRF to set USB mode.

- Set PIPE_PHY_GRF_PIPE_CON0[3:2] to 1'b1 to select USB mode.
- Set PIPE_PHY_GRF_PIPE_CON2[12] and [15] to 1'b0. This will select TxElecidle and TxCompliance form controller.
- Set PIPE_PHY_GRF_PIPE_CON3[14:13] to 2'b01 to select pipe to USB3 controller.

13.6.3 Battery Charging Application

The USB2.0 PHY supports battery charger detection to enable device draw increased current from VBUS for charging and/or powering up from dedicated charging ports or charging downstream ports.
The related signals with GRF are following:

Table 13-5 USB2PHY Battery Charging GRF Description

GRF	Description
USB2PHYGRF_CON2[5]	CHRGSEL: This signal selects whether the Battery Charger circuit sets voltage sourcing on the DP line and sensing on the DM line or voltage sourcing on DM and sensing on DP.
USB2PHYGRF_CON2[6]	VDATDETENB: This signal activates the Battery Charger comparator and enables detection of the DP and DM lines according to the Battery Charging specification.
USB2PHYGRF_CON2[7]	VDATSRCENB: This signal activates the voltage sourcing on the DP or DM line.
USB2PHYGRF_STATUS0[0]	CHGDET: This signal is the battery charge detection (VDAT_REF) comparator output.
USB2PHYGRF_STATUS0[1]	FSVPLUS: This signal is the DP FS/LS single ended receiver output, which is also the VLGC output.

GRF	Description
USB2PHYGRF_STATUS0[2]	FSVMINUS: This signal is the DM FS/LS single ended receiver output, which is also the VLGC output.
USB2PHYGRF_STATUS0[11]	OTGSESSVLD0: This signal is the VBUS session valid detection and can be used by a portable device to detect the VBUS voltage from the host or charger port.

Table 1-6 lists the detection flow.

Table 13-6 USB2PHY Battery Charging Operations

Mode of Operation	Inputs			Outputs			
	CHRGSEL	VDATDETENB	VDATSRCENB	OTGSESSVLD	CHGDET	FSVPUS	FSVMINUS
Battery charging is disabled	X	0	0	X	0	X	X
PHY is operating as a portable device (PD) and is not attached to host nor charger port.	X	0	0	0	X	X	X
PHY is operating as a PD using the Dead Battery Provision (DBP) - Unconfigured Clause, while attached to a standard downstream port (SDP).	0	1	1	1	0	X	0
PHY is operating as a PD using the DBP - Unconfigured Clause, while attached to a special port (such as a PS2 or proprietary charger) that pulls D+/D– high.	0	1	1	1	1	X	1
PHY is operating as a PD using the DBP - Unconfigured Clause, while attached to a charging downstream port (CDP) or a dedicated charging port (DCP).	0	1	1	1	1	X	0
PHY is operating as a PD that is performing Primary Detection while attached to an SDP.	1	1	1	1	0	X	0
PHY is operating as a PD that is performing Primary Detection while attached to a special port (such as a PS2 or proprietary charger) that pulls D+/D– high.	0	1	1	1	1	X	1
PHY is operating as a PD that is performing Primary Detection while attached to a CDP or DCP.	0	1	1	1	1	X	0
PHY is operating as a PD that is performing Secondary Detection while attached to a CDP.	1	1	1	1	0	X	X
PHY is operating as a PD that is performing Secondary Detection while attached to a DCP.	1	1	1	1	1	X	X
PHY is operating as a host CDP with no PD detected.	1	1	0	X	0	0	X
PHY is operating as a host CDP that detects an attached PD, which supports the BC specification.	1	1	1	X	1	0	X
PHY is operating as a host CDP that detects a connect from the PD D+ pullup.	1	1	0	X	X	1	0

13.6.4 OTG Programming Model

When detect ID change event (see USB2PHY_GRF) or VBUS change event (see USB2PHY_GRF) after disconnect, it means a USB3/2 OTG A device or B device may connect, then check status of ID (see USB2PHY_GRF). If ID==0, it will work as A device, then follow host programming flow; if ID==1, it will work as B device, then it follows device

programming flow.
Note: USB3.0 OTG doesn’t support host/device mode swapping through HNP and RSP.

Chapter 14 USBDP COMBO PHY

14.1 Overview

This chapter describes an overview of USBDP Combo PHY. USBDP Combo PHY is a PMA hardmacro to support USB and DP interface. USB's PCS and DP Link must be used along with USBDP Combo PHY for successful operation.

14.2 Features

The supported features in USBDP Combo PHY are:

- USB Specification 3.0 and DP Specification 1.4 compliant
- 5Gb/s Serializer/Deserializer for USB
- 1.62 Gb/s, 2.7 Gb/s, 5.4 Gb/s and 8.1 Gb/s Serializer for DP
- USB Type-C and DP Alt Mode supported

14.3 Function Description

14.3.1 Block Diagram

Fig.1-1 illustrates a block diagram of USBDP Combo PHY. USBDP Combo PHY comprises one Common, two lanes of transceiver, two lanes of transmitter, one AUX channel for DP, and PMA digital.

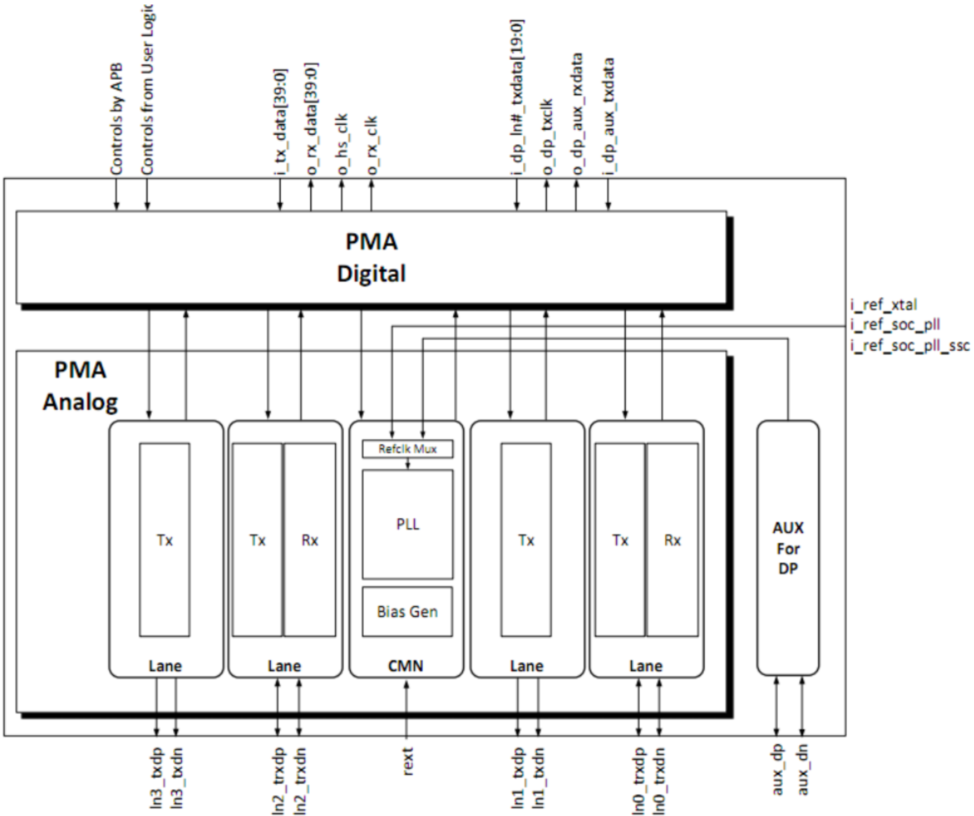

Fig. 14-1 USBDP Combo PHY Block Diagram

The following sections describe the various blocks and their functionalities. DPTX uses a 32 bit internal data path for the main link.

14.3.2 Function Overview

USBDP Combo PHY is used for Universal Serial Bus (USB) and DisplayPort (DP) applications. The transceiver in the core performs these functions:

- Serializes the 8b/10b encoded data for transmission for USB Gen1 and DP RBR/HBR/HBR2/HBR3 operations
- De-serializes the received code groups Input data coming is registered once before it goes through a 3-stage pipeline. The 3-stage pipeline is required to capture the three colors components in various input video formats.

When transmitting the data, the transceiver performs these functions:

- Accepts four 10-bit 8b/10b encoded transmit characters for USB Gen1
- Attaches and serializes the data to the TXP/TXN differential outputs to a maximum value of 5.0 Gb/s for USB. Accepts two 10-bit 8b/10b encoded transmit characters for DP

- Attaches and serializes the data to the TXP/TXN differential outputs to a maximum value of 8.1 Gb/s for DP

When receiving the data, the transceiver performs these functions:

- Samples the received serial data on the RXP/RXN differential inputs
- De-serializes it into four 10-bit (or 8-bit) received characters

14.3.3 PMA Analog

USBDP Combo PHY comprises of a PMA analog and PMA digital. The PMA consists of:

- One CMN block
- One AUX block for DP
- Two lanes including TX (lane1/3)
- Two lanes including TX and RX (lane0/2)
- One SSC ROPLL for DP
- One SSC LCPLL for USB

To support display alter mode, lane0 and lane2 work as TX in DP mode and as RX in USB mode. TX and RX are sharing bump in lane0 and lane2.
In the DP transmitter side, the PMA analog executes these actions:

- PMA Analog receives parallel data from PMA digital
- The data is serialized and transmitted through ln0/2_trxdp/n and ln1/3_txdp/n pads by hybrid-mode driver
- The TX driver characteristics, such as amplitude and 2-tap FIR filter, are user-controllable

In the USB transmitter side, the PMA analog executes these actions:

- PMA Analog receives parallel data from PMA digital
- The data is serialized and transmitted through ln1/3_txdp/n pads by hybrid-mode driver
- The TX driver characteristics, such as amplitude and 3-tap FIR filter, are either pre-settable or user-controllable

In the USB receiver side, the PMA analog executes these actions:

- The data is received through ln0/2_trxdp/n pads with 50Ω termination resistance
- Distortion on received signal due to channel loss is compensated by Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE)
- Clock and Data Recovery (CDR) generates frequency- and phase-aligned clock and equalized signal is deserialized to parallel data which is delivered to the PMA digital

14.3.4 CMN

The CMN consists of a band-gap reference (BGR), bias generator and PLL.
The BGR circuit generates high-accuracy reference voltage of 820mV across PVT variation. A bias generator makes two kinds of current, external- and internal-resistor (RMRES)-referred current, and these currents are distributed to each block in CMN and lanes. The external resistor-referred (REXT) current is generated using an8.2KΩ resistor which is connected between the rext pad and ground outside the chip. On the other hand, the internal resistor-referred current is generated using internally integrated replica resistor to compensate resistance error across PVT variation.
The PLL in the CMN synthesizes high-speed clock, which is used for TX serializer and RX CDR lock, from a reference clock.
The following are the main features of the PLL:

- Wide-range LC VCO from 8GHz to 10GHz
- Wide-range RO VCO from 4GHz to 8.1GHz
- Pre-defined or programmable divider setting for each USBDP Type-C specification
- Spread spectrum clocking (SSC) with sigma-delta modulated fractional divider
- Automatic Frequency Calibrated (AFC) oscillator setting for the desired frequency of operation
- Programmable charge pump current and loop filter resistance allowing for wide range of programmable loop bandwidth and peaking

14.3.5 AUX

The AUX is 1Mbps half-duplex bidirectional channel used for link management and device control. The AUX block does not support upstream detection feature.

14.4 Register Description

14.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 14-1 USB3 Address Mapping

Base Address	Device
0xFED70000~0xFED7FFFF	USBDPPHY 0
0xFED80000~0xFED8FFFF	USBDPPHY 1
USB3.0 Controller Address Mapping	
Offset Address Range	**Register Type**
0x8000 ~ 0xFFFF	USBDPPHY PMA

14.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
USBDPPHY_CMM_REG0024	0x0090	W	0x00000060	USBDPPHY CMN configure register
USBDPPHY_CMM_REG0025	0x0094	W	0x00000060	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004A	0x0128	W	0x0000003C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004B	0x012C	W	0x000000F4	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004C	0x0130	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG004D	0x0134	W	0x000000F4	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0057	0x015C	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0058	0x0160	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0059	0x0164	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005A	0x0168	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005D	0x0174	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005E	0x0178	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG005F	0x017C	W	0x00000034	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0060	0x0180	W	0x0000004E	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0063	0x018C	W	0x00000041	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0064	0x0190	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0065	0x0194	W	0x00000005	USBDPPHY CMN configure register
USBDPPHY_CMN_REG006B	0x01AC	W	0x0000002C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG006C	0x01B0	W	0x0000002C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG006D	0x01B4	W	0x0000002C	USBDPPHY CMN configure register

Name	Offset	Size	Reset Value	Description
USBDPPHY_CMN_REG006E	0x01B8	W	0x0000002C	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0072	0x01C8	W	0x00000008	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0073	0x01CC	W	0x00000008	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0074	0x01D0	W	0x00000008	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0075	0x01D4	W	0x00000008	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0076	0x01D8	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0077	0x01DC	W	0x00000005	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0078	0x01E0	W	0x0000002D	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0079	0x01E4	W	0x0000000A	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007C	0x01F0	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007D	0x01F4	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007E	0x01F8	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG007F	0x01FC	W	0x00000007	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0082	0x0208	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0083	0x020C	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0084	0x0210	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0085	0x0214	W	0x00000016	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0089	0x0224	W	0x00000010	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FC	0x03F0	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FD	0x03F4	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FE	0x03F8	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00FF	0x03FC	W	0x00000019	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0101	0x0404	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0102	0x0408	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0103	0x040C	W	0x0000000F	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0104	0x0410	W	0x0000003C	USBDPPHY CMN configure register

Name	Offset	Size	Reset Value	Description
USBDPPHY_TRSV_REG028F	0x0A3C	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0291	0x0A44	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0292	0x0A48	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0293	0x0A4C	W	0x000000F9	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0295	0x0A54	W	0x000000CF	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0297	0x0A5C	W	0x000000CF	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0299	0x0A64	W	0x0000009B	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG068F	0x1A3C	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0691	0x1A44	W	0x000000C0	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0692	0x1A48	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0693	0x1A4C	W	0x000000F9	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0695	0x1A54	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0697	0x1A5C	W	0x000000CF	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0699	0x1A64	W	0x0000009B	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG00A3	0x028C	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG0215	0x0854	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0415	0x1054	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0815	0x1054	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG00E3	0x038C	W	0x00000002	USBDPPHY CMN configure register
USBDPPHY_CMN_REG00D5	0x0354	W	0x00000000	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG02E1	0x0B84	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG06E1	0x1B84	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0204	0x0810	W	0x0000000F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0404	0x1010	W	0x0000000F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0604	0x1810	W	0x0000000F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0804	0x2010	W	0x0000000F	USBDPPHY TRSV configure register

Name	Offset	Size	Reset Value	Description
USBDPPHY_TRSV_REG0205	0x0814	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0405	0x1014	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0605	0x1814	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0805	0x2014	W	0x00000000	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0206	0x0818	W	0x00000001	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0406	0x1018	W	0x00000001	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0606	0x1818	W	0x00000001	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0806	0x2018	W	0x00000001	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0207	0x081C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0407	0x101C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0607	0x181C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0807	0x201C	W	0x000000E7	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG020C	0x0830	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0217	0x085C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG040C	0x1030	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0417	0x105C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG060C	0x1830	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0617	0x185C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG080C	0x2030	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0817	0x205C	W	0x00000080	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG008A	0x0228	W	0x00000038	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0041	0x0104	W	0x00000077	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0092	0x0248	W	0x00000077	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG021E	0x0878	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG061E	0x1878	W	0x00000004	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0226	0x0898	W	0x00000077	USBDPPHY TRSV configure register

Name	Offset	Size	Reset Value	Description
USBDPPHY_TRSV_REG0626	0x189C	W	0x00000077	USBDPPHY TRSV configure register
USBDPPHY_CMN_REG0015	0x0054	W	0x00000001	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0038	0x00E0	W	0x00000038	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0018	0x0060	W	0x00000024	USBDPPHY CMN configure register
USBDPPHY_CMN_REG0019	0x0064	W	0x000000FF	USBDPPHY CMN configure register
USBDPPHY_CMN_REG001C	0x0070	W	0x00000006	USBDPPHY CMN configure register
USBDPPHY_CMN_REG008D	0x0234	W	0x00000068	USBDPPHY CMN configure register
USBDPPHY_TRSV_REG02BD	0x0AF4	W	0x00000018	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG06BD	0x1AF4	W	0x00000018	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0267	0x099C	W	0x00000008	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0667	0x199C	W	0x00000008	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0269	0x09A4	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG026A	0x09A8	W	0x00000022	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0669	0x19A4	W	0x00000007	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG066A	0x19A8	W	0x00000022	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG026E	0x09B8	W	0x0000004E	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG066E	0x19B8	W	0x0000004E	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0279	0x09E4	W	0x00000002	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0679	0x09E8	W	0x00000002	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG028D	0x0A34	W	0x00000010	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG068D	0x1A34	W	0x00000010	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG02A6	0x0A98	W	0x0000004F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG06A6	0x1A98	W	0x0000004F	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG030C	0x0C30	W	0x00000006	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG0312	0x0C48	W	0x00000003	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG070C	0x1C3C	W	0x00000006	USBDPPHY TRSV configure register

Name	Offset	Size	Reset Value	Description
USBDPPHY_TRSV_REG0712	0x1C48	W	0x00000003	USBDPPHY TRSV configure register
USBDPPHY_TRSV_REG06BC	0x1AF0	W	0x0000001D	USBDPPHY TRSV configure register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3 Detail Registers Description

USBDPPHY_CMM_REG0024

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	ana_lcpll_pms_mdiv PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMM_REG0025

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	ana_lcpll_pms_mdiv PLL main divider setting for AFC counter. Divider value = Setting code.

USBDPPHY_CMN_REG004A

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x7	ropll_ana_cpi_ctrl_coarse PLL integral path charge-pump current contorl. 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101: 1.5625uA 3'b110: 20833uA 3'b111: 3.125uA
2:0	RW	0x4	ropll_ana_cpi_ctrl_fine PLL integral path charge-pump current contorl. 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101: 1.5625uA 3'b110: 20833uA 3'b111: 3.125uA

USBDPPHY_CMN_REG004B

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0xf	ropll_ana_cpp_ctrl_coarse PLL proportional path charge-pump current contorl. 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110: 200uA 3'b111: 300uA
3:0	RW	0x4	ropll_ana_cpp_ctrl_fine PLL proportional path charge-pump current contorl. 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110: 200uA 3'b111: 300uA

USBDPPHY_CMN_REG004C

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x1	ropll_ana_lpf_c_sel_coarse PLL loop filter capacitor control. 3'b000: 0pF 3'b001: 1pF 3'b010: 2pF 3'b011: 3pF 3'b100: 4pF 3'b101: 5pF 3'b110: 6pF 3'b111: 7pF
2:0	RW	0x7	ropll_ana_lpf_c_sel_fine PLL loop filter capacitor control. 3'b000: 0pF 3'b001: 1pF 3'b010: 2pF 3'b011: 3pF 3'b100: 4pF 3'b101: 5pF 3'b110: 6pF 3'b111: 7pF

USBDPPHY_CMN_REG004D

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0xf	ropll_ana_lpf_r_sel_coarse PLL loop filter resistor control. 4'b0000: 2K 4'b0001: 4K 4'b0010:6K ~ 4'b1111: 32K
3:0	RW	0x4	ropll_ana_lpf_r_sel_fine PLL loop filter resistor control. 4'b0000: 2K 4'b0001: 4K 4'b0010:6K 4'b1111: 32K

USBDPPHY_CMN_REG0057

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_rbr PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG0058

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_hbr PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG0059

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_hbr2 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005A

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_hbr3 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005D

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_afc_rbr PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005E

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_afc_hbr PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG005F

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x34	ropll_pms_mdiv_afc_hbr2 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG0060

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_pms_mdiv_afc_hbr3 PLL main divider setting. Divider value = Setting code.

USBDPPHY_CMN_REG0063

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ropll_pms_sdiv_rbr PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8
3:0	RW	0x1	ropll_pms_sdiv_hbr PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8

USBDPPHY_CMN_REG0064

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ropll_pms_sdiv_hbr3 PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8
3:0	RW	0x0	ropll_pms_sdiv_hbr2 PLL post divider setting (N-1, except /7). 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8

USBDPPHY_CMN_REG0065
Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ana_ropll_iqdiv_bypass VCO clock bypass IQ divider enable.
6	RW	0x0	ovrd_ropll_pms_iqdiv_rstn Override enable flag for ropll_pms_iqdiv_rstn
5	RW	0x0	ropll_pms_iqdiv_rstn IQ divider resetn.
4:3	RW	0x0	ana_ropll_ref_bypass_clk_sel PLL Bypass clock selection. 2'b00: XO 2'b01: IO 2'b10: PIXEL or LC_OUT_CLK 2'b11: System PLL clock
2	RW	0x1	ana_ropll_ref_chopper_clk_en Chopper clk enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ovrd_ropll_ref_chopper_clk_div_rstn Override enable flag for ropll_ref_chopper_clk_div_rstn.
0	RW	0x1	ropll_ref_chopper_clk_div_rstn Chopper clk divider reset. 1'b0: Reset. 1'b1: Released.

USBDPPHY_CMN_REG006B
Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x2c	ropll_sdm_denominator_rbr Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG006C
Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	ropll_sdm_denominator_hbr Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG006D
Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	ropll_sdm_denominator_hbr2 Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG006E
Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	ropll_sdm_denominator_hbr3 Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signedi_pll_sdm_k-i_pll_ssc_fm_deviation-i_pll_ssc_fm_freq-1|

USBDPPHY_CMN_REG0072
Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_rbr Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0073
Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_hbr Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0074
Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_hbr2 Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0075

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	ropll_sdm_numerator_hbr3 Numerator of SDM with i_pll_sdm_k_sign (-255~255).

USBDPPHY_CMN_REG0076

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_ropll_sdm_ph_num_sel PLL PI input clock phase number . 1'b0: 8-phase, 1'b1: 4-phase
4:3	RW	0x0	ana_ropll_sdm_pi_step PLL phase interpolstor step. 3'b00: 1-step (16-phase) 3'b01: 2-step (8-phase) 3'b1x: 0.5-step
2:0	RW	0x0	ropll_sdc_n_sp PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

USBDPPHY_CMN_REG0077

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x0	ropll_sdc_n_ssp PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1). 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8
2:0	RW	0x5	ropll_sdc_n_rbr PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1). 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

USBDPPHY_CMN_REG0078

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:3	RW	0x5	ropll_sdc_n_hbr PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8
2:0	RW	0x5	ropll_sdc_n_hbr2 PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

USBDPPHY_CMN_REG0079

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:1	RW	0x5	ropll_sdc_n_hbr3 PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8
0	RW	0x0	ana_ropll_sdc_n2 PLL SDC divide-ratio selection. 1'b0: No additional /2 1'b1: Additional /2

USBDPPHY_CMN_REG007C

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	ropll_sdc_numerator_rbr Numerator of SDC (Max 65).

USBDPPHY_CMN_REG007D

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	ropll_sdc_numerator_hbr Numerator of SDC (Max 65).

USBDPPHY_CMN_REG007E

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x07	ropll_sdc_numerator_hbr2 Numerator of SDC (Max 65).

USBDPPHY_CMN_REG007F
Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x07	ropll_sdc_numerator_hbr3 Numerator of SDC (Max 65).

USBDPPHY_CMN_REG0082
Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_rbr Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0083
Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_hbr Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0084
Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_hbr2 Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0085
Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x16	ropll_sdc_denominator_hbr3 Denominator of SDC (Max 65).

USBDPPHY_CMN_REG0089
Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	ana_ropll_ssc_clk_div_sel PLL SSC clock divide ratio. 4'b0000: N/A 4'b0001: /1 4'b0010: /2 ~ 4'b1111: /15
3	RW	0x0	ovrd_ropll_cd_clk_en Override enable flag for ropll_cd_clk_en
2	RW	0x0	ropll_cd_clk_en CD enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	ovrd_ropll_cd_tx_ser_rstn Override enable flag for ropll_cd_tx_ser_rstn.

Bit	Attr	Reset Value	Description
0	RW	0x0	ropll_cd_tx_ser_rstn TX_SER resetn.

USBDPPHY_CMN_REG00FC
Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_rbr PLL SSC modulation deviation.

USBDPPHY_CMN_REG00FD
Address: Operational Base + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_hbr PLL SSC modulation deviation.

USBDPPHY_CMN_REG00FE
Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_hbr2 PLL SSC modulation deviation.

USBDPPHY_CMN_REG00FF
Address: Operational Base + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x19	ana_ropll_ssc_fm_deviation_hbr3 PLL SSC modulation deviation.

USBDPPHY_CMN_REG0101
Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0f	ana_ropll_ssc_fm_freq_rbr PLL SSC modulation frequency.

USBDPPHY_CMN_REG0102
Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0f	ana_ropll_ssc_fm_freq_hbr PLL SSC modulation frequency.

USBDPPHY_CMN_REG0103
Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0f	ana_ropll_ssc_fm_freq_hbr2 PLL SSC modulation frequency.

USBDPPHY_CMN_REG0104
Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:2	RW	0x0f	ana_ropll_ssc_fm_freq_hbr3 PLL SSC modulation frequency.
1	RW	0x0	lcpll_lock_done_delay_bypass Lock_done_flag_delay_bypass.
0	RW	0x0	ropll_lock_done_delay_bypass Lock_done_flag_delay_bypass.

USBDPPHY_TRSV_REG028F

Address: Operational Base + offset (0x0A3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln0_rx_cdr_pms_m_sp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0291

Address: Operational Base + offset (0x0A44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln0_rx_cdr_pms_m_ssp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0292

Address: Operational Base + offset (0x0A48)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln0_rx_cdr_pms_m_rbr_8 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0293

Address: Operational Base + offset (0x0A4C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xf9	ln0_rx_cdr_pms_m_rbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0295

Address: Operational Base + offset (0x0A54)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xcf	ln0_rx_cdr_pms_m_hbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0297

Address: Operational Base + offset (0x0A5C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xcf	ln0_rx_cdr_pms_m_hbr2_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0299
Address: Operational Base + offset (0x0A64)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x9b	ln0_rx_cdr_pms_m_hbr3_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG068F
Address: Operational Base + offset (0x1A3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln2_rx_cdr_pms_m_sp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0691
Address: Operational Base + offset (0x1A44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xc0	ln2_rx_cdr_pms_m_ssp_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0692
Address: Operational Base + offset (0x1A48)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln2_rx_cdr_pms_m_rbr_8 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0693
Address: Operational Base + offset (0x1A4C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xf9	ln2_rx_cdr_pms_m_rbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0695
Address: Operational Base + offset (0x1A54)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln2_rx_cdr_pms_m_hbr_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0697
Address: Operational Base + offset (0x1A5C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xcf	ln2_rx_cdr_pms_m_hbr2_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_TRSV_REG0699

Address: Operational Base + offset (0x1A64)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x9b	ln2_rx_cdr_pms_m_hbr3_7_0 CDR AFC target value. The ratio of VCO frequency over reference clock frequency.

USBDPPHY_CMN_REG00A3

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	dp_tx_link_bw DP bandwidth 2'b00: RBR (1.62Gbps) 2'b01: HBR (2.7Gbps) 2'b10: HBR2(5.4Gbps) 2'b11: HBR3(8.1Gbps)
4:3	RO	0x0	reserved
2	RW	0x0	dp_tx_lane_swap_en DP lane swap enable. 1'b0: Lane0/1/2/3_TxData mapping to Lane0/1/2/3_TXDP/N. 1'b1: Lane0/1/2/3_TxData mapping to Lane2/3/0/1_TXDP/N.
1	RW	0x0	dp_tx_data_inv DP TX data polarity inversion enable.
0	RW	0x0	dp_tx_data_swap DP TX data bit order swap enable (MSB <-> LSB).

USBDPPHY_TRSV_REG0215

Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln0_tx_ser_rate_sel_hbr TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
6	RW	0x0	ln0_tx_ser_rate_sel_hbr2 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
5	RW	0x0	ln0_tx_ser_rate_sel_hbr3 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ovrd_ln0_tx_ser_clk_rstn Override enable flag for ln0_tx_ser_clk_rstn

Bit	Attr	Reset Value	Description
3	RW	0x0	ln0_tx_ser_clk_rstn TX serializer clock-path resetn. 1'b0: Reset 1'b1: Released
2	RW	0x0	ln0_ana_tx_cdr_clk_mon_en TX serializer clock selection: If default=0 then MUX will always toggle with PLL clk and 1mA power waste. CDR clock is turned off in RX therefore power will not burn. 1'b0: PLL clock 1'b1: CDR clock
1	RO	0x0	reserved
0	RW	0x0	ln0_ana_tx_lane_rstn_sel Mux select to choose lane RSTN (ser_clk_rstn) or CMN RSTN (ser_tx_clk_rstn) which resets the CMN RSTN (ser_tx_clk_rstn) which resets the divider, 1'b0: CMN RSTN 1'b1: LINE RSTN

USBDPPHY_TRSV_REG0415

Address: Operational Base + offset (0x1054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln1_tx_ser_rate_sel_hbr TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
6	RW	0x0	ln1_tx_ser_rate_sel_hbr2 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
5	RW	0x0	ln1_tx_ser_rate_sel_hbr3 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ovrd_ln1_tx_ser_clk_rstn Override enable flag for ln1_tx_ser_clk_rstn
3	RW	0x0	ln1_tx_ser_clk_rstn TX serializer clock-path resetn. 1'b0: Reset 1'b1: Released
2	RW	0x1	ln1_ana_tx_cdr_clk_mon_en TX serializer clock selection: If default=0 then MUX will always toggle with PLL clk and 1mA power waste. CDR clock is turned off in RX therefore power will not burn 1'b0: PLL clock 1'b1: CDR clock
1	RO	0x0	reserved
0	RW	0x0	ln1_ana_tx_lane_rstn_sel Mux select to choose lane RSTN (ser_clk_rstn) or CMN RSTN (ser_tx_clk_rstn) which resets the divider (/5/10/20). 1'b0: CMN RSTN 1'b1: LANE RSTN

USBDPPHY_TRSV_REG0815

Address: Operational Base + offset (0x1054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln3_tx_ser_rate_sel_hbr TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
6	RW	0x0	ln3_tx_ser_rate_sel_hbr2 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
5	RW	0x0	ln3_tx_ser_rate_sel_hbr3 TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ovrd_ln3_tx_ser_clk_rstn Override enable flag for ln1_tx_ser_clk_rstn
3	RW	0x0	ln3_tx_ser_clk_rstn TX serializer clock-path resetn. 1'b0: Reset 1'b1: Released
2	RW	0x1	ln3_ana_tx_cdr_clk_mon_en TX serializer clock selection: If default=0 then MUX will always toggle with PLL clk and 1mA power waste. CDR clock is turned off in RX therefore power will not burn 1'b0: PLL clock 1'b1: CDR clock
1	RO	0x0	reserved
0	RW	0x0	ln3_ana_tx_lane_rstn_sel Mux select to choose lane RSTN (ser_clk_rstn) or CMN RSTN (ser_tx_clk_rstn) which resets the divider (/5/10/20). 1'b0: CMN RSTN 1'b1: LANE RSTN

USBDPPHY_CMN_REG00E3

Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	dp_init_rstn DP initial reset.
2	RW	0x0	dp_cmn_rstn DP PLL reset.
1	RW	0x1	cdr_watchdog_en CDR lock watchdog enable. If CDR lock wasn't occured, toggle cdr_en signal to restart CDR.
0	RW	0x0	cdr_watchdog_mask_cdr_en Disable cdr_en toggle when CDR restart by watchdog.

USBDPPHY_CMN_REG00D5

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RO	0x0	ana_lcpll_mon_gm_code LC VCO GM code monitor.
1	RO	0x0	ana_ropll_lock_done PLL Lock Done.
0	RO	0x0	ana_ropll_afc_done PLL AFC Done.

USBDPPHY_TRSV_REG02E1
Address: Operational Base + offset (0x0B84)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	ln0_mon_rx_cdr_afc_done Monitoring SFR.
2	RO	0x0	ln0_mon_rx_cdr_cal_done Monitoring SFR.
1	RO	0x0	ln0_mon_rx_cdr_fld_pll_mode_done Monitoring SFR.
0	RO	0x0	ln0_mon_rx_cdr_lock_done Monitoring SFR.

USBDPPHY_TRSV_REG06E1
Address: Operational Base + offset (0x1B84)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ln2_mon_rx_cdr_afc_done Monitoring SFR.
2	RO	0x0	ln2_mon_rx_cdr_cal_done Monitoring SFR.
1	RO	0x0	ln2_mon_rx_cdr_fld_pll_mode_done Monitoring SFR.
0	RO	0x0	ln2_mon_rx_cdr_done Monitoring SFR.

USBDPPHY_TRSV_REG0204
Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln0_tx_drv_lvl_ctrl Override enable flag for ln0_tx_drv_lvl_ctrl
4:0	RW	0x0f	ln0_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0404
Address: Operational Base + offset (0x1010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln1_tx_drv_lvl_ctrl Override enable flag for ln1_tx_drv_lvl_ctrl

Bit	Attr	Reset Value	Description
4:0	RW	0x0f	ln1_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0604

Address: Operational Base + offset (0x1810)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln2_tx_drv_lvl_ctrl Override enable flag for ln2_tx_drv_lvl_ctrl
4:0	RW	0x0f	ln2_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0804

Address: Operational Base + offset (0x2010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_ln3_tx_drv_lvl_ctrl Override enable flag for ln3_tx_drv_lvl_ctrl
4:0	RW	0x0f	ln3_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ~ 5'b00000: min main-tap level (min swing) Others: N/A

USBDPPHY_TRSV_REG0205

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln0_tx_drv_lvl_ctrl Override enable flag for ln0_tx_drv_post_lvl_ctrl
3:0	RW	0x0	ln0_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0405

Address: Operational Base + offset (0x1014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln1_tx_drv_lvl_ctrl Override enable flag for ln1_tx_drv_post_lvl_ctrl

Bit	Attr	Reset Value	Description
3:0	RW	0x0	ln1_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0605
Address: Operational Base + offset (0x1814)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln2_tx_drv_lvl_ctrl Override enable flag for ln2_tx_drv_post_lvl_ctrl
3:0	RW	0x0	ln2_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0805
Address: Operational Base + offset (0x2014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_ln3_tx_drv_lvl_ctrl Override enable flag for ln3_tx_drv_post_lvl_ctrl
3:0	RW	0x0	ln3_tx_drv_post_lvl_ctrl TX driver de-emphasis level (TX_DE_EMP<14:0>) 3'b0000: min de-emphasis level ~ 3'b1110: max de-emphasis level Others: N/A

USBDPPHY_TRSV_REG0206
Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_ln0_tx_drv_pre_lvl_ctrl Override enable flag for ln0_tx_drv_pre_lvl_ctrl
5:2	RW	0x0	ln0_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln0_tx_drv_idrv_en Override enable flag for ln0_tx_drv_idrv_en
0	RW	0x1	ln0_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0406
Address: Operational Base + offset (0x1018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_ln1_tx_drv_pre_lvl_ctrl Override enable flag for ln1_tx_drv_pre_lvl_ctrl
5:2	RW	0x0	ln1_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln1_tx_drv_idrv_en Override enable flag for ln1_tx_drv_idrv_en
0	RW	0x1	ln1_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0606

Address: Operational Base + offset (0x1818)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_ln2_tx_drv_pre_lvl_ctrl Override enable flag for ln2_tx_drv_pre_lvl_ctrl
5:2	RW	0x0	ln2_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln2_tx_drv_idrv_en Override enable flag for ln2_tx_drv_idrv_en
0	RW	0x1	ln2_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0806

Address: Operational Base + offset (0x2018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_ln3_tx_drv_pre_lvl_ctrl Override enable flag for ln3_tx_drv_pre_lvl_ctrl
5:2	RW	0x0	ln3_tx_drv_pre_lvl_ctrl TX driver pre-shoot level (TX_PRE_EMP<9:0>) 4'b0000: min pre-shoot boosting ~ 4'b1001: max pre-shoot boosting Others: N/A
1	RW	0x0	ovrd_ln3_tx_drv_idrv_en Override enable flag for ln3_tx_drv_idrv_en
0	RW	0x1	ln3_tx_drv_idrv_en TX current-driver enable 1'b0: Disable 1'b1: Enable

USBDPPHY_TRSV_REG0207

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln0_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln0_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org
3:2	RW	0x1	ln0_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln0_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln0_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG0407

Address: Operational Base + offset (0x101C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln1_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln1_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org
3:2	RW	0x1	ln1_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln1_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln1_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG0607

Address: Operational Base + offset (0x181C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln2_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln2_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org
3:2	RW	0x1	ln2_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln2_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln2_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG0807

Address: Operational Base + offset (0x201C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x7	ln3_ana_tx_drv_idrv_iup_ctrl TX current driver pmos current control. 3'b000: Min 3'b111: Max
4	RW	0x0	ln3_ana_tx_drv_beacon_idrv_delay_sel Retain idrv settling time margin @beacon entry. 1'b0: Select delay (default) 1'b1: Org
3:2	RW	0x1	ln3_ana_tx_drv_beacon_idrv_delay_ctrl i_tx_drv_beacon_delay_ctrl<1:0> 3'b00: 2UI delay 3'b01: 3UI delay (default) 3'b10: 4UI delay 3'b11: 5UI delay
1	RW	0x1	ln3_ana_tx_drv_accdrv_en Enable of Cap. Peaking block. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ln3_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b1: polarity change, data P/N is switched (enhancement) 1'b0: polarity non-change (deenhancement)

USBDPPHY_TRSV_REG020C

Address: Operational Base + offset (0x0830)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ln0_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln0_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0217

Address: Operational Base + offset (0x085C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln0_tx_ser_vreg_en Override enable flag for ln0_tx_ser_vreg_en
6	RW	0x0	ln0_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln0_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln0_tx_ser_vreg_lpf_bypass Override enable flag for ln0_tx_ser_vreg_lpf_bypass.
3	RW	0x0	ln0_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln0_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_TRSV_REG040C

Address: Operational Base + offset (0x1030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ln1_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln1_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0417

Address: Operational Base + offset (0x105C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln1_tx_ser_vreg_en Override enable flag for ln1_tx_ser_vreg_en
6	RW	0x0	ln1_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln1_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln1_tx_ser_vreg_lpf_bypass Override enable flag for ln1_tx_ser_vreg_lpf_bypass.
3	RW	0x0	ln1_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln1_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_TRSV_REG060C

Address: Operational Base + offset (0x1830)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ln2_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln2_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0617

Address: Operational Base + offset (0x185C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln2_tx_ser_vreg_en Override enable flag for ln2_tx_ser_vreg_en
6	RW	0x0	ln2_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln2_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln2_tx_ser_vreg_lpf_bypass Override enable flag for ln2_tx_ser_vreg_lpf_bypass.
3	RW	0x0	ln2_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln2_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_TRSV_REG080C

Address: Operational Base + offset (0x2030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ln3_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x7	ln3_tx_jeq_even_ctrl_sp TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on

USBDPPHY_TRSV_REG0817
Address: Operational Base + offset (0x205C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ovrd_ln3_tx_ser_vreg_en Override enable flag for ln3_tx_ser_vreg_en
6	RW	0x0	ln3_tx_ser_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
5	RW	0x0	ln3_ana_tx_ser_vreg_bypass Force Bypass Regulator: 1'b0: Regulator mode 1'b1: Bypass Regulator and VDD is connected to Regulator node using pass gate
4	RW	0x0	ovrd_ln3_tx_ser_vreg_lpf_bypass Override enable flag for ln3_tx_ser_vreg_lpf_bypass.
3	RW	0x0	ln3_tx_ser_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
2:0	RW	0x0	ln3_ana_tx_ser_vreg Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref=: 3'b000:0.749 3'b001:0.776 3'b010:0.804 3'b011:0.831 3'b100:0.859(default), 3'b101:0.886 3'b110:0.914 3'b111:0.941

USBDPPHY_CMN_REG008A
Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	ana_ropll_cd_hsclk_inv CD output clock polarity inversion 1'b0: No swap 1'b1: P/N swap
5	RW	0x1	ana_ropll_cd_hsclk_west_en CD driver nmos strength control N/A
4	RW	0x1	ana_ropll_cd_hsclk_east_en CD driver pmos strength control N/A
3	RW	0x1	ovrd_ropll_cd_vreg_en Override enable flag for ropll_cd_vreg_en
2	RW	0x0	ropll_cd_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
1	RW	0x0	ovrd_ropll_cd_vreg_lpf_bypass Override enable flag for ropll_cd_vreg_lpf_bypass
0	RW	0x0	ropll_cd_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)

USBDPPHY_CMN_REG0041
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x77	ana_lcpll_reserved USBDP [7]: i_pll_cd_div2_en_west (default: 0) [6]: i_pll_cd_rstn_sel_west (default: 1) [5:4]: i_pll_cd_hsclk_west_ctrl<1:0> (default: 3) [3]: i_pll_cd_div2_en_east (default: 0) [2]: i_pll_cd_rstn_sel_east (default: 0) [1:0]: i_pll_cd_hsclk_east_ctrl<1:0> (default: 3)

USBDPPHY_CMN_REG0092
Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x77	ana_ropll_reserved USBDP [7]: i_pll_cd_div2_en_west (default: 0) [6]: i_pll_cd_rstn_sel_west (default: 1) [5:4]: i_pll_cd_hsclk_west_ctrl<1:0> (default: 3) [3]: i_pll_cd_div2_en_east (default: 0) [2]: i_pll_cd_rstn_sel_east (default: 0) [1:0]: i_pll_cd_hsclk_east_ctrl<1:0> (default: 3)

USBDPPHY_TRSV_REG021E
Address: Operational Base + offset (0x0878)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x04	ln0_ana_tx_reserved Reserved port USBDP Lane0,2 [0]: Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en [1]: Driver input P data @ force mode [2]: Driver input N data @ force mode USBDP Lane 1,3 [0]: Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en

USBDPPHY_TRSV_REG061E

Address: Operational Base + offset (0x1878)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	ln2_ana_tx_reserved Reserved port USBDP Lane0,2 [0]: Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en [1]: Driver input P data @ force mode [2]: Driver input N data @ force mode USBDP Lane 1,3 [0]: Driver input data force sel 1'b0: Data force @ driver off state 1'b1: Data force @ srlb_en

USBDPPHY_TRSV_REG0226

Address: Operational Base + offset (0x0898)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x7	ln0_rx_cdr_mdiv_sel_pll_sp CDR IQ (main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1
3:0	RW	0x7	ln0_rx_cdr_mdiv_sel_pll_ssp CDR IQ (main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1

USBDPPHY_TRSV_REG0626

Address: Operational Base + offset (0x189C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x7	ln2_rx_cdr_mdiv_sel_pll_sp CDR IQ (main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1
3:0	RW	0x7	ln2_rx_cdr_mdiv_sel_pll_ssp CDR IQ (main) divider rate control 4'b1111: div16 4'b0111: div8 4'b0011: div4 4'b0001: div2 4'b0000: div1

USBDPPHY_CMN_REG0015

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x0	ana_lcpll_avc_cnt_wait_num Number of reference clock cycle to wait VCO clock during AFC
1	RW	0x0	ana_lcpll_avc_en AVC Enable
0	RW	0x1	ana_lcpll_avc_force_en AVC Force Enable

USBDPPHY_CMN_REG0038

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ana_lcpll_cd_hsclk_inv CD output clock polarity inversion 1'b0: No swap 1'b1: P/N swap
5	RW	0x1	ana_lcpll_cd_hsclk_west_en CD driver enable to WEST Side clocks
4	RW	0x1	ana_lcpll_cd_hsclk_east_en CD driver enable to EAST Side clocks
3	RW	0x1	ovrd_lcpll_cd_vreg_en Override enable flag for lcpll_cd_vreg_en
2	RW	0x0	lcpll_cd_vreg_en Controls Regulator Enable: 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)
1	RW	0x0	ovrd_lcpll_cd_vreg_lpf_pass Override enable flag for lcpll_cd_vreg_lpf_bypass
0	RW	0x0	lcpll_cd_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)

USBDPPHY_CMN_REG0018

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x4	lcpll_ana_cpi_ctrl_coarse PLL integral path charge-pump current control 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101:1.5625uA 3'b110: 20833uA 3'b111: 3.125uA
2:0	RW	0x4	lcpll_ana_cpi_ctrl_fine PLL integral path charge-pump current control 3'b0xx: half current (not used) 3'b100: 1.25uA 3'b101:1.5625uA 3'b110: 20833uA 3'b111: 3.125uA

USBDPPHY_CMN_REG0019

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0xf	lcpll_ana_cpp_ctrl_coarse PLL proportional path charge-pump current control 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110:200uA 3'b111:300uA
3:0	RW	0xf	lcpll_ana_cpp_ctrl_fine PLL proportional path charge-pump current control 3'b000: 66.7uA 3'b001: 75uA 3'b010: 85.7uA 3'b011: 100uA 3'b100: 120uA 3'b101: 150uA 3'b110:200uA 3'b111:300uA

USBDPPHY_CMN_REG001C

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	lcpll_ana_lpf_c_sel_fine PLL loop filter capacitor control 3'b000: 0pF 3'b001: 1pF 3'b010: 2pF 3'b011: 3pF 3'b100: 4pF 3'b101: 5pF 3'b110: 6pF 3'b111: 7pF

Bit	Attr	Reset Value	Description
3:0	RW	0x6	lcpll_ana_lpf_r_sel_coarse PLL loop filter resistor control 4'b0000: 2K 4'b0001: 4K 4'b0010:6K ~ 4'b1111: 32K

USBDPPHY_CMN_REG008D
Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ropll_beacon_lfps_out_en Override enable flag for ropll_beacon_lfps_out_en
6	RW	0x1	ropll_beacon_lfps_out_en TX beacon clock enable 1'b0: Disable 1'b1: Enable
5	RW	0x1	ana_ropll_misc_clk_sync_en PLL miscellaneous clock synchronization enable If enabled, PLL misc clock output is self-synchronized so that clock shape is not affected by LFPS/beacon enable timing. 1'b0: Disable (async) 1'b1: Enable (sync)
4:3	RW	0x1	ana_ropll_misc_clk_sel PLL low-frequency clock output source selection 2'b00: Reference clock 2'b01: Config clock from SoC 2'b10: Internal oscillator clock 2'b11: Divided PLL clock
2	RW	0x0	ana_ropll_ref_clk_mon_en PLL reference clock monitor enable 1'b0: Disable 1'b: Enable
1	RW	0x0	ovrd_ropll_misc_osc_rstn Override enable flag for ropll_misc_osc_rstn
0	RW	0x0	ropll_misc_osc_rstn Self osc reset

USBDPPHY_TRSV_REG02BD
Address: Operational Base + offset (0x0AF4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln0_ovrd_rx_rcal_rstn Override enable flag for ln0_rx_rcal_rstn
6	RW	0x0	ln0_rx_rcal_rstn Signal override
5:4	RW	0x1	ln0_rx_rcal_opt_code 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code + i_sfr_rcal_code 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code
3:0	RW	0x8	ln0_rx_rterm_ctrl Offset to tune_code at opt_code = 2 or 3

USBDPPHY_TRSV_REG06BD
Address: Operational Base + offset (0x1AF4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln2_ovrd_rx_rcal_rstn Override enable flag for ln0_rx_rcal_rstn
6	RW	0x0	ln2_rx_rcal_rstn Signal override
5:4	RW	0x1	ln2_rx_rcal_opt_code 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code + i_sfr_rcal_code 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code
3:0	RW	0x8	ln2_rx_rterm_ctrl Offset to tune_code at opt_code = 2 or 3

USBDPPHY_TRSV_REG0267
Address: Operational Base + offset (0x099C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	ln0_rx_dfe_vga_rl_ctrl_hbr2 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm
4:2	RW	0x2	ln0_rx_dfe_vga_rl_ctrl_hbr3 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm
1:0	RW	0x0	ln0_ana_rx_dfe_vga_pbias_ctrl_reserved VGA default current control 2'b00: 1.2mA 2'b01: 1.6mA 2'b10: 2.0mA 2'b11: 2.4mA

USBDPPHY_TRSV_REG0667
Address: Operational Base + offset (0x199C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	ln2_rx_dfe_vga_rl_ctrl_hbr2 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm
4:2	RW	0x2	ln2_rx_dfe_vga_rl_ctrl_hbr3 VGA R output value control 3'b000: 600ohm ... 3'b111: 75ohm

Bit	Attr	Reset Value	Description
1:0	RW	0x0	ln2_ana_rx_dfe_vga_pbias_ctrl_reserved VGA default current control 2'b00: 1.2mA 2'b01: 1.6mA 2'b10: 2.0mA 2'b11: 2.4mA

USBDPPHY_TRSV_REG0269
Address: Operational Base + offset (0x09A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln0_ana_rx_rterm_ofsn_ctrl Offset code for RX RTERM N node
5	RW	0x0	ln0_ana_rx_rterm_ofsp_ctrl Offset code for RX RTERM P node 1'b0: No offset added 1'b1: +1 offset code added
4	RW	0x0	ln0_ana_rx_rterm_path_ctrl RX term sw ctrl 1'b0: Rtern sw ctrl by"offset_cal_enable" 1'b1: Ctrl by "offset_cal_enable" && "rterm_en" --> for DP tx mode
3:0	RW	0x7	reserved

USBDPPHY_TRSV_REG026A
Address: Operational Base + offset (0x09A8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x1	ln0_ana_rx_rterm_incm_vcm_ctrl_reserved reserved
4	RW	0x0	ovrd_ln0_rx_rterm_cm_pulldn_reserved Override enable flag for ln0_rx_rterm_cm_pulldn_reserved
3	RW	0x0	ln0_rx_rterm_cm_pulldn_reserved reserved
2	RW	0x0	ovrd_ln0_rx_rterm_vcm_en_reserved Override enable flag for ln0_rx_rterm_vcm_en_reserved
1	RW	0x1	ln0_rx_rterm_vcm_en_reserved reserved
0	RW	0x0	ln0_ana_rx_sq_vref_820m_lpf_bypass_reserved reserved

USBDPPHY_TRSV_REG0669
Address: Operational Base + offset (0x19A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln2_ana_rx_rterm_ofsn_ctrl Offset code for RX RTERM N node
5	RW	0x0	ln2_ana_rx_rterm_ofsp_ctrl Offset code for RX RTERM P node 1'b0: No offset added 1'b1: +1 offset code added

Bit	Attr	Reset Value	Description
4	RW	0x0	ln2_ana_rx_rterm_path_ctrl RX term sw ctrl 1'b0: Rtern sw ctrl by"offset_cal_enable" 1'b1: Ctrl by "offset_cal_enable" && "rterm_en" --> for DP tx mode
3:0	RW	0x7	reserved

USBDPPHY_TRSV_REG066A
Address: Operational Base + offset (0x19A8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x1	ln2_ana_rx_rterm_incm_vcm_ctrl_reserved reserved
4	RW	0x0	ovrd_ln2_rx_rterm_cm_pulldn_reserved Override enable flag for ln2_rx_rterm_cm_pulldn_reserved
3	RW	0x0	ln2_rx_rterm_cm_pulldn_reserved reserved
2	RW	0x0	ovrd_ln2_rx_rterm_vcm_en_reserved Override enable flag for ln2_rx_rterm_vcm_en_reserved
1	RW	0x1	ln2_rx_rterm_vcm_en_reserved reserved
0	RW	0x0	ln2_ana_rx_sq_vref_820m_lpf_bypass_reserved reserved

USBDPPHY_TRSV_REG026E
Address: Operational Base + offset (0x09B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ln0_ana_rx_sqhs_th_ctrl_reserved reserved
3	RW	0x1	ln0_ana_rx_sqhs_filter_en SQHS loss detector enable
2:1	RW	0x3	ln0_ana_rx_sqhs_bw_ctrl Not used
0	RO	0x0	reserved

USBDPPHY_TRSV_REG066E
Address: Operational Base + offset (0x19B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ln2_ana_rx_sqhs_th_ctrl_reserved reserved
3	RW	0x1	ln2_ana_rx_sqhs_filter_en SQHS loss detector enable
2:1	RW	0x3	ln2_ana_rx_sqhs_bw_ctrl Not used
0	RW	0x0	ln2_ana_rx_sqhs_vref_supply_sel Selection of supply voltage of reference voltage for threshold calibration of HS SQ 1'b0: VREG 1'b1: VDD

USBDPPHY_TRSV_REG0279
Address: Operational Base + offset (0x09E4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x02	ln0_rx_sslms_c1_init_reserved reserved

USBDPPHY_TRSV_REG0679

Address: Operational Base + offset (0x09E8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x02	ln2_rx_sslms_c1_init_reserved reserved

USBDPPHY_TRSV_REG028D

Address: Operational Base + offset (0x0A34)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	ln0_rx_sslms_rstn RX DFE force Reset 1'b0: Reset 1'b1: Use lane reset
3	RW	0x0	ln0_ovrd_rx_sslms_adap_en_reserved Override enable flag for ln0_rx_sslms_adap_en_reserved
2	RW	0x0	ln0_rx_sslms_adap_en_reserved reserved
1	RW	0x0	ln0_ovrd_rx_sslms_adap_hold_reserved Override enable flag for override enable flag for ln0_rx_sslms_adap_hold_reserved
0	RW	0x0	ln0_rx_sslms_adap_hold_reserved reserved

USBDPPHY_TRSV_REG068D

Address: Operational Base + offset (0x1A34)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	ln2_rx_sslms_rstn RX DFE force Reset 1'b0: Reset 1'b1: Use lane reset
3	RW	0x0	ln2_ovrd_rx_sslms_adap_en_reserved Override enable flag for ln2_rx_sslms_adap_en_reserved
2	RW	0x0	ln2_rx_sslms_adap_en_reserved reserved
1	RW	0x0	ln2_ovrd_rx_sslms_adap_hold_reserved Override enable flag for override enable flag for ln2_rx_sslms_adap_hold_reserved
0	RW	0x0	ln2_rx_sslms_adap_hold_reserved reserved

USBDPPHY_TRSV_REG02A6

Address: Operational Base + offset (0x0A98)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x4	ln0_rx_cdr_fbb_fine_ctrl_sp RX CDR FBB code in PLL Low-BW of CK and Data mode 4'b0000: Min FBB code ~ 4'b1111: Max FBB code
3:0	RW	0xf	ln0_rx_cdr_fbb_pll_bw_diff_sp RX CDR FBB offset from FBB-calibrated code in PLL mode 4'b0000: No offset 4'b0001: +1 4'b0010: +2 ~ 4'b1111: Max FBB code

USBDPPHY_TRSV_REG06A6
Address: Operational Base + offset (0x1A98)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	ln2_rx_cdr_fbb_fine_ctrl_sp RX CDR FBB code in PLL Low-BW of CK and Data mode 4'b0000: Min FBB code ~ 4'b1111: Max FBB code
3:0	RW	0xf	ln2_rx_cdr_fbb_pll_bw_diff_sp RX CDR FBB offset from FBB-calibrated code in PLL mode 4'b0000: No offset 4'b0001: +1 4'b0010: +2 ~ 4'b1111: Max FBB code

USBDPPHY_TRSV_REG030C
Address: Operational Base + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x06	ln0_rx_sslms_hf_init_rate_ssp RX DFE SSLMS init value

USBDPPHY_TRSV_REG0312
Address: Operational Base + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x03	ln0_rx_sslms_mf_init_rate_ssp RX DFE SSLMS init value

USBDPPHY_TRSV_REG070C
Address: Operational Base + offset (0x1C3C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x06	ln2_rx_sslms_hf_init_rate_ssp RX DFE SSLMS init value

USBDPPHY_TRSV_REG0712
Address: Operational Base + offset (0x1C48)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x03	ln2_rx_sslms_mf_init_rate_ssp RX DFE SSLMS init value

USBDPPHY_TRSV_REG06BC
Address: Operational Base + offset (0x1AF0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln2_rxd_polarity On normal path, Rx data polarity inversion
6:5	RW	0x0	ln2_rx_sigval_lpf_bypass Low pass filter for removing sigval falling glitchs. 1'b0: Filter enable 1'b1: Filter bypass
4:2	RW	0x7	ln2_tg_rx_sigval_lpf_delay_time N/A
1	RW	0x0	ln2_rx_ctle_eq_mf_man_sel N/A
0	RW	0x1	ln2_rx_ctle_eq_hf_man_sel N/A

14.5 Application Notes

14.5.1 Signal Controlled by GRF and CRU

There are two USBDP PHY (USBDPPHY 0 and USBDPPHY 1) in system. The signals need to be controlled by CRU or GRF are list below:

USBDPPHY 0:
i_rx_lfps_en: USB3PHY0_GRF_CON1[14]
i_init_rstn: CRU_SOFTRST_CON02[8]
i_apb_presetn: CRU_SOFTRST_CON72[2]
i_pcs_apb_presetn: CRU_SOFTRST_CON02[11]
i_cmn_rstn: CRU_SOFTRST_CON02[9]
i_lane_rstn: CRU_SOFTRST_CON02[10]

USBDPPHY 1:
i_rx_lfps_en: USB3PHY1_GRF_CON1[14]
i_init_rstn: CRU_SOFTRST_CON02[15]
i_apb_presetn: CRU_SOFTRST_CON72[4]
i_pcs_apb_presetn: CRU_SOFTRST_CON03[2]
i_cmn_rstn: CRU_SOFTRST_CON03[0]
i_lane_rstn: CRU_SOFTRST_CON03[1]

14.5.2 Power Sequence Guide

14.5.2.1 Power-Up Sequence

Sequential power-up of 1.8V and 0.85V must be provided to USBDP Combo PHY for proper SerDes operation. Supply voltage of 0.85V must be ramped up first, and supply voltage of 1.8V must be started ramping up after 0.85V supply is completely settled down. Signals i_init_rstn and i_apb_presetn must be asserted after power is fully turned on. Following the release of i_init_rstn, you can access some registers through APB if need and the primary inputs i_cmn_rstn should be set low until the APB programming is finished from initial. After the APB is programmed, the i_cmn_rstn should be released. The signal i_cmn_rstn=0 will cause the PMA's COMMON to turn on. And, the primary input i_lane_rstn will be controlled by Link sub-controller and will be reset in abnormal situation like link-down.
PLL locks within 60us after i_cmn_rstn is asserted and o_pll_lock_done goes to high when the PLL achieves lock. Fig.1-2 illustrates the timing restrictions for RESET signals and the typical timing information for the related output signals.

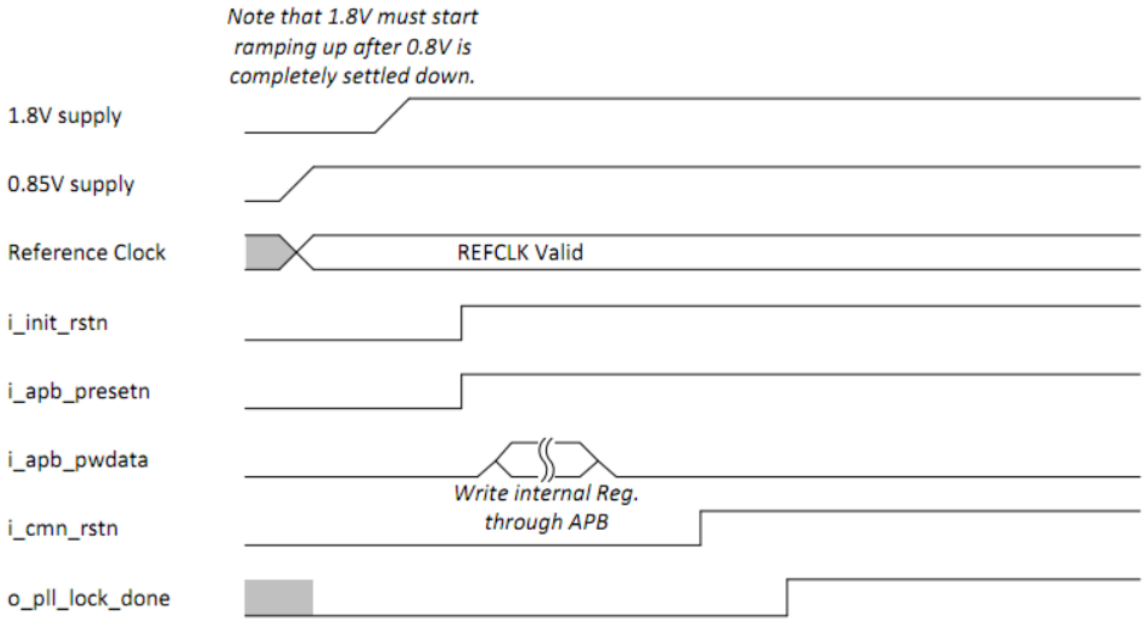

Fig. 14-2 USBDP PHY Power Up Sequence

14.5.2.2 Power-Down Sequence

During power-down (Turning-off supply voltage), supply voltage of 0.85V must start ramping down after supply voltage of 1.8V is completely discharge.

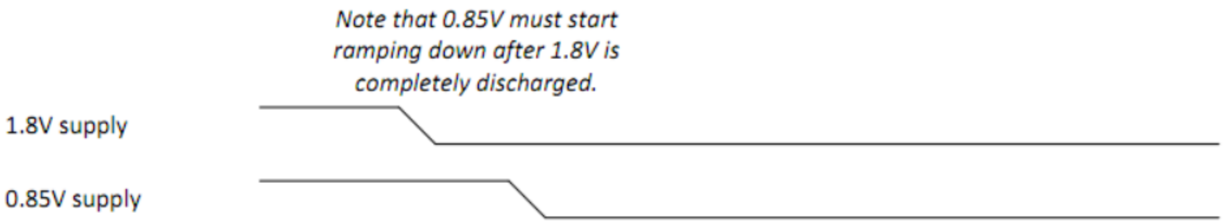

Fig. 14-3 USBDP PHY Power Down Sequence

14.5.3 PHY Initialization Guide

14.5.3.1 USBDP APB Reset Sequence

The USBDP PHY has USB part and DP part. And both parts share the APB Reset. The APB Reset sequence is needed to initialize the USBDP PHY.

Please de-assert USBDP PHY APB Reset when the USBDP PHY is needed to re-initialize like POR (Power-On-Reset, Alt-mode configuration changing).

Please do not de-assert i_apb_presetn when only USB part or DP part initialized.

14.5.3.2 USB LANE0/1, DP LANE2/3 Setting Sequence

When USBDP PHY works, some initial setting should be applicated. The following shows the initialization sequence.

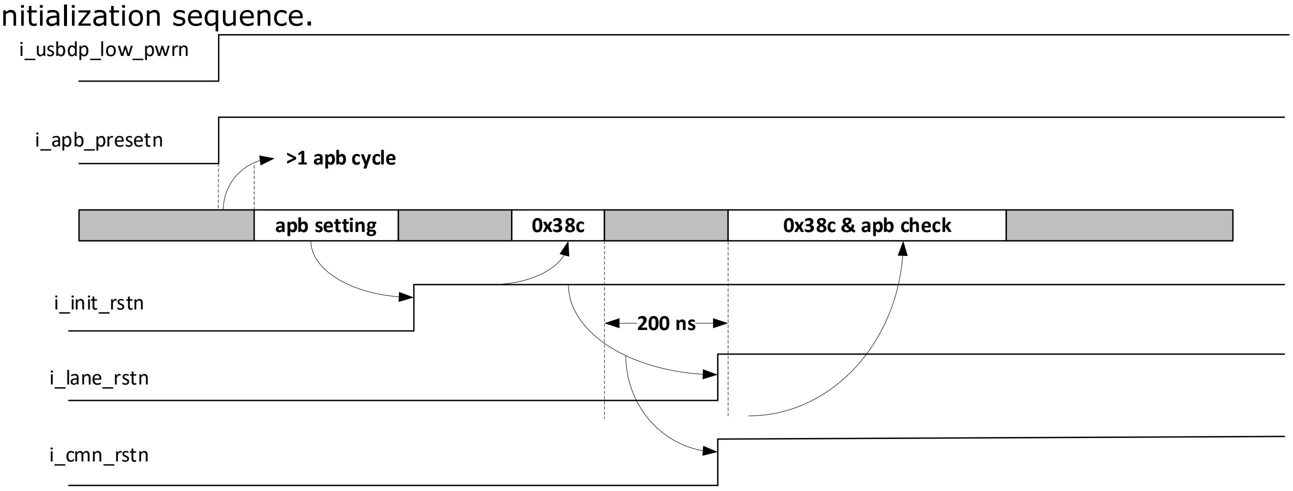

Fig. 14-4 USBDP PHY Power Down Sequence

Table 14-2 PHY Initialization Sequence

Port / SFR Address	Write value			Read value
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
rext	1	1	1	
i_usbdp_low_pwrn	0	0	0	
i_apb_presetn	0	0	0	
WAIT 1 APB_CLK				
i_usbdp_low_pwrn	1	1	1	
i_apb_presetn	1	1	1	
i_lcpll_ref_clk_sel	0	0	0	
i_ropll_ref_clk_Sel	0	0	0	
i_init_rstn	0	0	0	
i_lane_rstn	0	0	0	
i_cmn_rstn	0	0	0	
24M reference clk:	**24M reference clk:**			
0x0090	0x68			
0x0094	0x68			
0x0128	0x24			
0x012c	0x44			
0x0130	0x3f			
0x0134	0x44			
0x015c	0xa9			
0x0160	0x71			
0x0164	0x71			
0x0168	0xa9			
0x0174	0xa9			
0x0178	0x71			
0x017c	0x71			
0x0180	0xa9			
0x018c	0x41			
0x0190	0x00			
0x0194	0x05			
0x01ac	0x2a			
0x01b0	0x17			
0x01b4	0x17			
0x01b8	0x2a			
0x01c8	0x04			
0x01cc	0x08			
0x01d0	0x08			
0x01d4	0x04			
0x01d8	0x20			
0x01dc	0x01			
0x01e0	0x09			
0x01e4	0x03			
0x01f0	0x29			
0x01f4	0x02			
0x01f8	0x02			
0x01fc	0x29			
0x0208	0x2a			
0x020c	0x17			
0x0210	0x17			
0x0214	0x2a			
0x0224	0x20			
0x03f0	0x0d			

Port / SFR Address	Write value			Read value
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
0x03f4	0x09			
0x03f8	0x09			
0x03fc	0x0d			
0x0404	0x0e			
0x0408	0x14			
0x040c	0x14			
0x0410	0x3b			
0x0a3c	0xd0			
0x0a44	0xd0			
0x0a48	0x01			
0x0a4c	0x0d			
0x0a54	0xe0			
0x0a5c	0xe0			
0x0a64	0xa8			
0x1a3c	0xd0			
0x1a44	0xd0			
0x1a48	0x01			
0x1a4c	0x0d			
0x1a54	0xe0			
0x1a5c	0xe0			
0x1a64	0xa8			
0x0E38	0x05			
26M reference clk:	**26M reference clk:**			
0x0830	0x07			
0x085c	0x80			
0x1030	0x07			
0x105c	0x80			
0x1830	0x07			
0x185c	0x80			
0x2030	0x07			
0x205c	0x80			
0x0228	0x38			
0x0104	0x44			
0x0248	0x44			
0x038C	0x02			
0x0878	0x04			
0x1878	0x04			
0x0898	0x77			
0x1898	0x77			
0x0054	0x01			
0x00e0	0x38			
0x0060	0x24			
0x0064	0x77			
0x0070	0x76			
0x0234	0xE8			
0x0AF4	0x15			
0x1AF4	0x15			
0x081C	0xE5			
0x181C	0xE5			
0x099C	0x48			
0x199C	0x48			
0x09A4	0x07			

Port / SFR Address	Write value			Read value
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
0x09A8 0x19A4 0x19A8 0x09B8 0x19B8 0x09E4 0x19E4 0x0A34 0x1A34 0x0A98 0x1A98 0x0c30 0x0C48 0x1C30 0x1C48 0x028C 0x0AF0 0x1AF0 0x0E38	0x22 0x07 0x22 0x3E 0x3E 0x02 0x02 0x1E 0x1E 0x2F 0x2F 0x0E 0x06 0x0E 0x06 0x18 0x00 0x00 0x05			
0x028C	0x14 // RBR 0x34 // HBR 0x54 // HBR2 0x74 // HBR3	0x10 // RBR 0x30 // HBR 0x50 // HBR2 0x70 // HBR3	0x10 // RBR 0x30 // HBR 0x50 // HBR2 0x70 // HBR3	
0x0854 (RBR, HBR) 0x1054 (RBR, HBR)	0x04 0x04	0x06 0x06	0x06 0x06	
0x1854 (RBR, HBR) 0x2054 (RBR, HBR)	0x06 0x06	0x04 0x04	0x06 0x06	
0x0854 (HBR2, HBR3) 0x1054 (HBR2, HBR3)	0x04 0x04	0x04 0x04	0x04 0x04	
0x1854 (HBR2, HBR3) 0x2054 (HBR2, HBR3)	0x04 0x04	0x04 0x04	0x04 0x04	
i_init_rstn (when USB used)	1	1	0	
0x038C (when DP used)	0x0A	0x0A	0x0A	
WAIT 200ns				
i_lane_rstn (when USB used)	1	1	0	
i_cmn_rstn (when USB used)	1	1	0	
0x038C (when DP used)	0x0E	0x0E	0x0E	
0x0350 (Check when USB used)			SKIP	0b_11XX_XXXX
0x0354 (Check when DP used)				0b_XXXX_XX11

Port / SFR Address	Write value			Read value
	USB RX0 TX1 DP TX2 TX3	DP TX0 TX1 USB RX2 TX3	DP TX0/TX1/TX2/TX3	
0x0B84 (Check when USB used)		SKIP	SKIP	0b_XXXX_XXX1
0x1B84 (Check when USB used)	SKIP		SKIP	0b_XXXX_XXX1

14.5.4 SFR Setting for Transmitter

14.5.4.1 Amplitude

Tx amplitude is defined as a differential swing of low-frequency (DC) signal, which is less dependent on off-chip environment, at ln[N]_txdp, ln[N]_txdn, ln[N]_trxdp and ln[N]_trxdn as shown in Fig.1-4. Tx driver amplitude is controlled by two tuning parameters; voltage-mode and current-mode driver amplitude control, respectively.

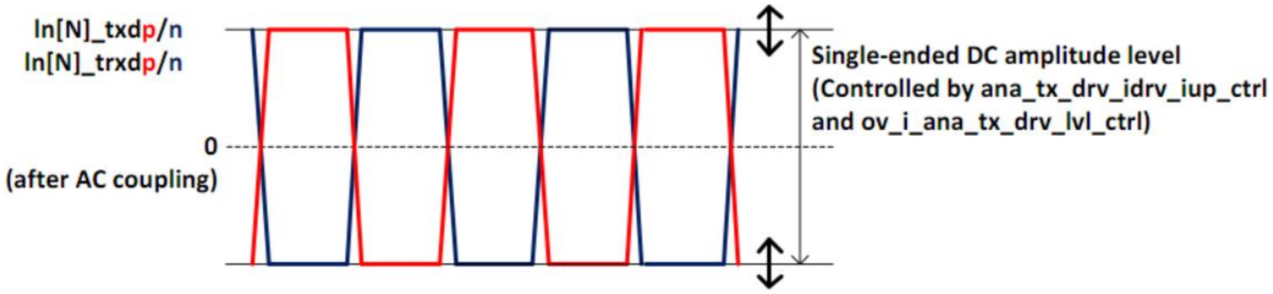

Fig. 14-5 TX DC Amplitude Control

The amplitude of voltage-mode driver can be controlled by either PCS or PMA SFR setting. As shown in Table1-3, SFR fields for control consist of override enable and input bits. When override enable is set to high, all following input bits for override are directly applied to Tx voltage mode driver circuit. Due to its own characteristic of voltage-mode driver, the maximum single-ended amplitude of the driver cannot exceed the supply voltage level, VDD (Assuming well-matched Tx impedance). Note that the register field for voltage-mode driver swing control is separated into four rate-specific registers and one matched register value is automatically applied according to the data rate under operation. A current-mode driver is implemented to achieve higher voltage swing beyond the limit of voltage-mode drive. In order to activate the current-mode driver, ln_tx_drv_idrv_en must be set to high and ana_tx_drv_idrv_iup_ctrl must be set When the current-mode driver is enabled, extra higher swing can be achieved over VDD.

Table 14-3 Amplitude Control of Voltage-Mode Driver

Name	Address	Code	Description
Override enable for TX Amplitude Contorl	0x0810 0x1010 0x1810 0x2010 Bit[5]	0x1	Override enable for tx_drv_idrv_en
TX Differential Output (TXDP/TXDN) Amplitude Control ln0/1/2/3_tx_drv_lvl_ctrl	0x0810 0x1010 0x1810 0x2010 Bit[4:0]	0xa	1200mV (Max)
		0x0	400 mV
TX Differential Output (TXDP/TXDN)	0x0818 0x1018	0x10	Disable current driver

Name	Address	Code	Description
Amplitude Control ln0/1/2/3_tx_drv_idrv_en	0x1818 0x2018 Bit[0]	0x11	enable current driver
TX Differential Output (TXDP/TXDN) Amplitude Control ln0/1/2/3_ana_tx_drv_idrv_iup_ctrl	0x081C 0x101C 0x181C 0x201C Bit[7:5]	0x0	1200mV (Max)
		0x7	850mV (Min)

14.5.4.2 Equalization

USBDP Combo PHY has 3 tap FIR filter in Tx. De-emphasis function is implemented to reduce the swing of driver when there is no transition (bit change) between current and previous data bit as shown in Fig.1-5.

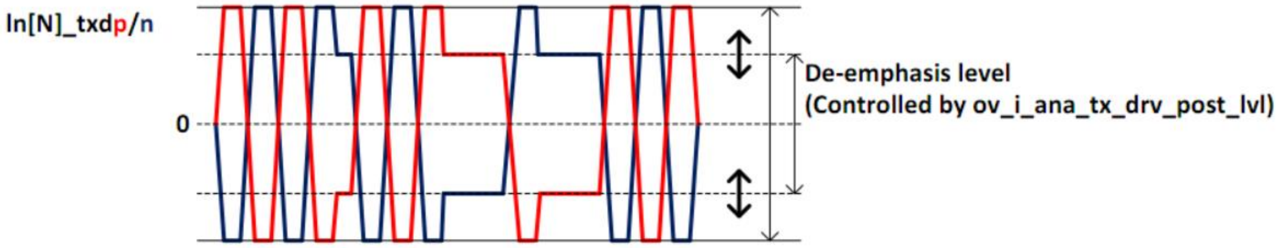

Fig. 14-6 TX De-emphasis Level Control

Table 14-4 SFR Setting for De-emphasis Level Control

Name	Address	Code	Description
TX De-Emphasis Level Control ln0/1/2/3_tx_drv_post_lvl_ctrl	0x0814 0x1014 0x1814 0x2014 Bit[4:0]	00000	-0.5 dB
		00100	– 1.5 dB.
		0100	– 2.8 dB.
		01000	– 4.2 dB.

Preshoot function is implemented to reduce the swing of driver when there is no transition (bit change) between current and next data bit as shown in Fig.1-6

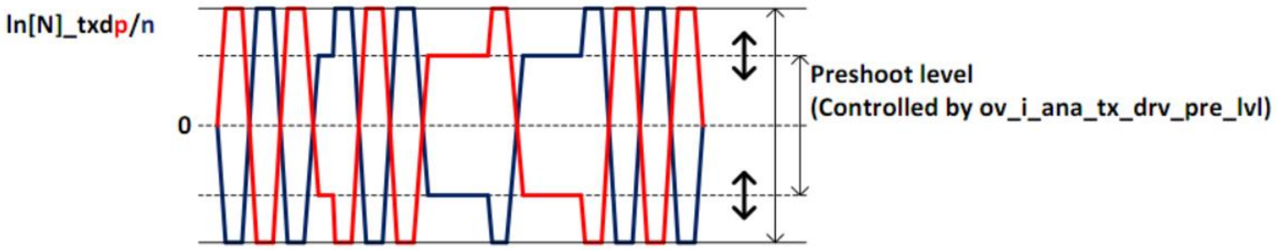

Fig. 14-7 TX Preshoot Level Control

Table 14-5 SFR Setting for Preshoot Level Control

Name	Address	Code	Description
TX Pre-shoot Level Control ln0/1/2/3_tx_drv_pre_lvl_ctrl	0x0818 0x1018 0x1818 0x2018 Bit[5:2]	0000	0 dB Recommend to use over 5 Gbps speed
		0110	– 1.6 dB. Recommend to use over 10 Gbps speed.
		1001	– 6.9 dB. Not recommend to use because main amplitude level is also aggressively

Name	Address	Code	Description
			reduced.

14.5.4.3 Slew Rate

Slew rate of Tx waveform is able to be controlled by SFR shown in Table 1-6. In order to enable slew-rate control, ana_tx_drv_accdrv_en bit must be set to high. Polarity of slew-rate control is controlled by ana_tx_drv_accdrv_pol_sel_* for each data rate. Tx driver has faster slew rate when this bit is set to high, while slower rate when set to low. Amount of slew rate control is determined by ana_tx_drv_accdrv_ctrl_* for each data rate. Higher value makes Tx driver to have faster slope when ana_tx_drv_accdrv_pol_sel_* is set to high, while higher value makes Tx driver to have slower slope when ana_tx_drv_accdrv_pol_sel_* is set to low.

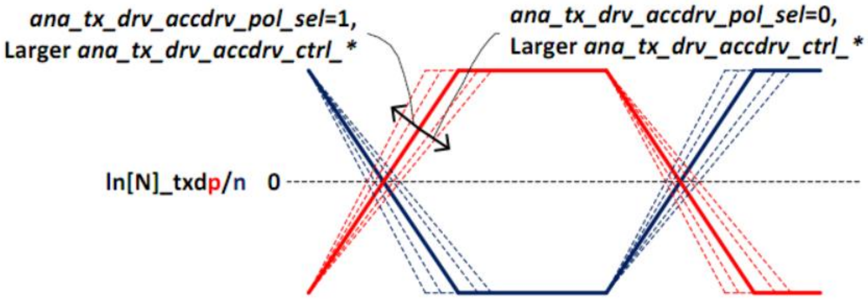

Fig. 14-8 TX Slew-Rate Control

Table 14-6 SFR Setting for Slew Rate Level Control

Name	Address	Code	Description
accdrv_en ln0/1/2/3_ana_tx_drv_accdrv_en	0x081C 0x101C 0x181C 0x201C Bit[1]	0x0	TX AC-coupled driver enable for slew rate control Disable
		0x1	TX AC-coupled driver enable for slew rate control Enable
accdrv_pol_sel ln0/1/2/3_ana_tx_drv_accdrv_pol_sel	0x081C 0x101C 0x181C 0x201C Bit[0]	0x1	Faster slew rate
		0x0	Slower slew rate
drv_accdrv_ctrl ln0/1/2/3_ana_tx_ drv_accdrv_ctrl	0x0820 0x1020 0x1820 0x2020 Bit[5:3]	0x7	TX AC-coupled driver Max Strength
		0x0	TX AC-coupled driver Min Strength

Chapter 15 SATA Host

15.1 Overview

SATA Host implements the Serial Advanced Technology Attachment (SATA) storage interface for physical storage devices.
SATA Host supports the following features:

- Include 3 ports, and each port can connect up to 5 devices using PM switching
- SATA 1.5Gb/s, SATA 3.0Gb/s, SATA 6.0Gb/s speeds
- eSATA
- Compliant with Serial ATA 3.3 specifications
- Compliant with AHCI Revision 1.3.1
- OOB signaling detection and generation
- Digital support of Mechanical presence switch and cold presence detect
- Activity LED support
- Digital support of device hot-plugging
- Output port to indicate speed that is negotiated after COMRESET for power optimization
- Memory Data Protection (ECC) and Error Correction (ECC)
- Memory Data Protection Diagnostic Error Injection
- SATA 1.5Gb/s, SATA 3.0Gb/s, and SATA 6.0Gb/s speed negotiation
- Asynchronous signal recovery, including retry polling
- Power management features including automatic partial-to-slumber transition
- BIST loopback modes
- Hardware-assisted Native Command Queuing for up to 32 entries
- Port Multiplier with FIS-based switching
- Disabling RX and TX Data clocks during power down modes
- Any sector sizes
- AXI interface used for configuration only support single
- AXI interface used to fetch data from memory

15.2 Block Diagram

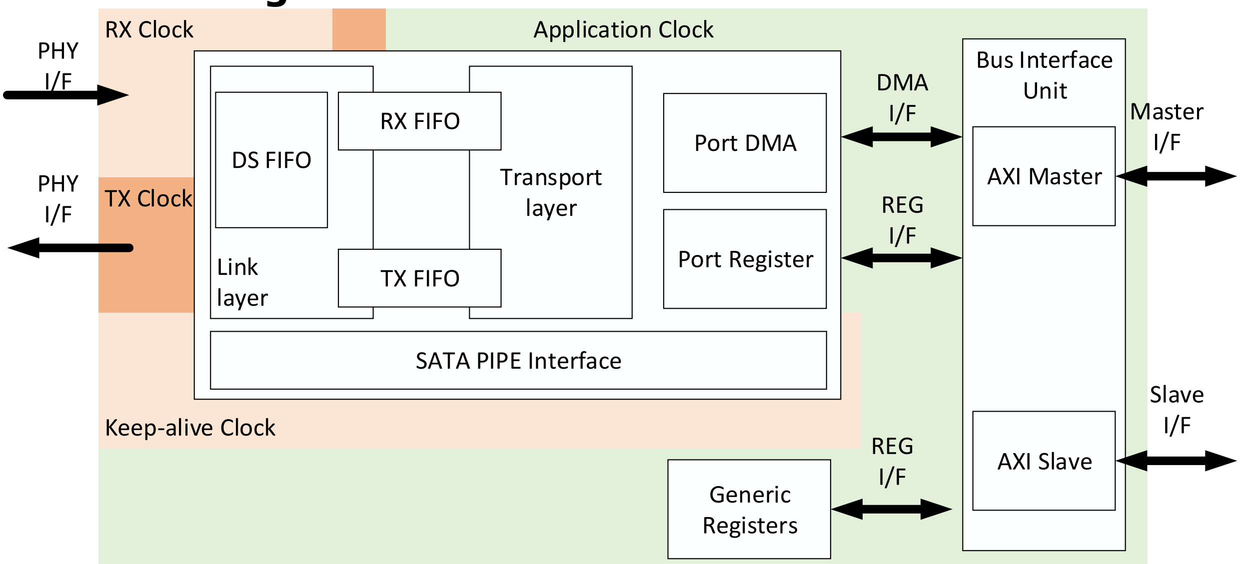

Fig. 15-1 SATA host Architecture

15.3 Function Description

15.3.1 Bus Interface Unit (BIU)

The Bus Interface Unit provides two interfaces:
AXI Master - This interface enables the SATA AHCI DMA engine to read and write to an AXI slave connected to AXI BIU.
AXI Slave - This interface enables an AXI master to read and write through the AXI BIU to the SATA AHCI registers.

15.3.2 Generic Registers (GCSR)

This module implements all global registers and provides the following functions:
- Generic configuration and control
- Global interrupt support
- BIST operation

15.3.3 Port Registers (PCSR)

The port registers module implements all Port-specific registers:
- Command list and FIS Based address
- Interrupt status/ enable
- Port command / status
- Task file data/signature /serial ATA
- DMA status/control

15.3.4 Port DMA(PDMA)

This module performs the following functions:
- Monitors commands posted by system software using the CI register
- Control data transfer between the Transport layer FIFOs and system memory using Physical Region Descriptor Table (PRDT)
- Transfers non-Data FISes received from the device to system memory using Received FIS Structure

Most of the communication between the PDMA and software is done using two system memory descriptors that are constructed by software prior to initiating the transfer: FIS descriptor, which contains FISes received from that device; and the command list, which contains a list of 1 to 32 commands available for Port to execute and the pointers for data transfers. Some additional communication is done by registers located in the GCSR and PCSR modules.
System memory structures are described in the SATA AHCI specification and are not repeated in this document.
The PDMA module operates in the application clock(aclk) domain.

15.3.5 Port Transport layer

The transport layer block provides FIS reception and transmission functions of the SATA transport layer. It operates in two clock domains: transmit and application. During reception, the transport layer receives a new FIS from the link layer through the RX FIFO, decodes the FIS type, and instructs the PDMA to route the FIS payload data to the appropriate location in system memory. During transmission, the transport layer instructs the PDMA to construct the appropriate FIS, and then passes it to the link layer through the TX FIFO. The transport layer block receives all the PHY/Link errors from the link layer, detects transport errors and passes them to the PCSR for setting the corresponding error bits.
The transport layer processes one FIS at time on the transmit side, meaning only one FIS is allowed in the TX FIFO at a time. On the receive side, RX FIFO can potentially contain more than one FIS at a time. For example, when the device transmits several DMA data FISes back-to-back with minimal delay, the RX FIFO still has the previous Data FIS while the next FIS is being received. The transport layer also contains a small internal eight-DWORD RX FIFO1 that is used for non-data FISes and FIS "End Status."

15.3.6 Port Link layer

This module optional OOB signaling, system initialization, speed negotiation, frame negotiation and arbitration, envelope framing/de-framing, CRC calculating, insertion and checking, flow control, frame acknowledgement and status reporting, data scrambling/de-scrambling for EMI reduction, repeat primitive data transmission and reception handling, ALIGN primitive detection, dropping and data alignment and power management.

15.4 Register Description

15.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

15.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SATA_CAP	0x0000	W	0x6737FF80	This register indicates basic capabilities of the SATA Host to the software.
SATA_GHC	0x0004	W	0x80000000	This register controls various global actions of the SATA Host.
SATA_IS	0x0008	W	0x00000000	This register indicates which of the ports within the SATA Host have an interrupt pending and require service
SATA_PI	0x000C	W	0x00000000	This register indicates which ports are exposed by the SATA Host and are available for the software to use. It is loaded by the BIOS.
SATA_VS	0x0010	W	0x00010300	This register indicates the major and minor version of the AHCI specification that the SATA Host implementation supports. The SATA Host supports version 1.3.0
SATA_CCC_CTL	0x0014	W	0x00010108	This register is used to configure the command completion coalescing (CCC) feature for the SATA Host.
SATA_CCC_PORTS	0x0018	W	0x00000000	This register specifies the ports that are coalesced as part of the command completion coalescing (CCC) feature.
SATA_CAP2	0x0024	W	0x00000000	This register indicates capabilities of the SATA Host to the software.
SATA_BISTAFR	0x00A0	W	0x00000000	This register contains the pattern definition and data pattern fields of the received BIST Activate FIS.
SATA_BISTCR	0x00A4	W	0x00000000	This register is used in BIST initiator modes and for general PHY/Link control. It is loaded by the host software prior to sending BIST Activate FIS to the device.
SATA_BISTFCTR	0x00A8	W	0x00000000	This register contains the received BIST FIS count in the loopback initiator Far-end Retimed, Far-end Analog and Near-end Analog modes.
SATA_BISTSR	0x00AC	W	0x00FFFFFF	This register contains errors detected in the received BIST FIS in the loopback initiator Far-end Retimed, Far-end Analog and Near-end Analog modes. It is updated each time a new BIST FIS is received.

Name	Offset	Size	Reset Value	Description
SATA_BISTDECR	0x00B0	W	0xFFFFF000	This register contains the number of DWORD errors detected in the received BIST frame in the loopback initiator Far-end Retimed, Far-end Analog and Near-end Analog modes. It is updated each time a new BIST frame is received.
SATA_MEMEDFBSERRDATA	0x00B4	W	0x00000000	This is read-only per-port FBS RAM Data Ecc/Parity error location (address) and syndrome register.
SATA_MEMEDADDRERRINJ	0x00B8	W	0x00000000	This per-port register controls the ECC/Parity error injection functionality. Single-bit and double-bit pseudo-random errors can be injected in each of the three memory interfaces (RX FIFO RAM, TX FIFO RAM, FBS RAM). The register allows for just one memory element to be injected with an error or for continuous error injection in each memory element.
SATA_OOBR	0x00BC	W	0x00000000	This register controls the Link layer OOB detection counters. The default values, MIN_COMWAKE, MAX_COMWAKE, MIN_COMINIT and MAX_COMINIT are calculated based on the RXOOB_CLK_FREQ parameter and loaded on power-up or asynchronous SATA Host reset.
SATA_MEMEDTXFERRDATAU	0x00C0	W	0x00000000	When the TX FIFO RAM Data parity error syndrome width excess the range of the register MEMEDTXFERRDATA.mem_txf_err_synd, extra bits are logged in this register. If the upper syndrome bits are not enough for filling all the bits of this register, redundancy bits filled with 0.
SATA_DIAGNR3	0x00C4	W	0x00000000	DIAGNR3
SATA_TIMER1MS	0x00E0	W	0x00000000	This register is used to generate a 1-ms tick for the command completion coalescing (CCC) or DevSleep logic, based on the AMBA bus clock frequency.
SATA_MEMDPCR	0x00E4	W	0x00000000	This register is used to control the various options associated with the Data protection (ECC/Parity) and Address protection (Parity) functionality.

Name	Offset	Size	Reset Value	Description
SATA_TESTR	0x00F4	W	0x00000000	This register is used to put the SATA Host slave interface into a test mode and to select a Port for BIST operation.
SATA_VERSION	0x00F8	W	0x00000000	This 32-bit read-only register contains hard-coded hexadecimal SATA Host component version value.
SATA_IDR	0x00FC	W	0x00000000	This register contains a hard-coded hexadecimal SATA Host identification value, as determined by the configuration parameter External User Core ID Port.
SATA_P0CLB	0x0100	W	0x00000000	Port Command List Base Address Register
SATA_P0FB	0x0108	W	0x00000000	Port FIS Base Address Register
SATA_P0IS	0x0110	W	0x00000000	Port Interrupt Status Register.
SATA_P0IE	0x0114	W	0x00000000	Port Interrupt Enable Register.
SATA_P0CMD	0x0118	W	0x00000000	Port Command Register. This register contains bits controlling various Port functions.
SATA_P0TFD	0x0120	W	0x00000000	Port Task File Data Register. This register contains Error and Status registers updated every time a new Register FIS, PIO Setup FIS, or Set Device Bits FIS is received from the device.
SATA_P0SIG	0x0124	W	0x00000000	Port Signature Register
SATA_P0SSTS	0x0128	W	0x00000000	Port Serial ATA Status (SStatus) Register. This 32-bit register conveys the current state of the interface and host. The Port updates it continuously and asynchronously. When the Port transmits a COMRESET to the device, this register is updated to its reset values (such as, Global reset, Port reset, or device disconnect ('PHY Ready' negation)).
SATA_P0SCTL	0x012C	W	0x00000000	Port Serial ATA Control Register. This 32-bit read-write register is used by the software to control SATA interface capabilities. Writes to this register result in an action being taken by the Port PHY interface. Reads from the register return the last value written to it. Reset on Global reset.
SATA_P0SERR	0x0130	W	0x00000000	Port Serial ATA Error Register. This 32-bit register represents all the detected interface errors accumulated since the last time it was cleared.

Name	Offset	Size	Reset Value	Description
SATA_P0SACT	0x0134	W	0x00000000	Port Serial ATA Active Register
SATA_P0CI	0x0138	W	0x00000000	Port Command Issue Register
SATA_P0SNTF	0x013C	W	0x00000000	Port Serial ATA Notification Register. This register is used to determine when asynchronous notification events have occurred for directly connected devices and devices connected to a Port Multiplier.
SATA_P0FBS	0x0140	W	0x00000000	Port FIS-Based Switching Control Register. This register is used to control and obtain status for Port Multiplier FIS-based switching.
SATA_P0DMACR	0x0170	W	0x00000000	Port DMA Control Register. This register contains bits for controlling the Port DMA engine. The software can change the fields of this register only when P0CMD.ST=0. This register is reset to its default value on power-up (system reset) only.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

15.4.3 Detail Registers Description

SATA_CAP

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	s64a Supports 64-bit addressable data structures by utilizing P0FBU and P0CLBU registers.
30	RO	0x1	sncq Supports SATA native command queuing by handing DMA Setup FIS natively.
29	RO	0x1	ssntf Supports P0SNTF (SNotification) register and its associated functionality.
28	RW	0x0	smps This bit is set by the system firmware/BIOS when platform supports mechanical presence for hot plug operation.
27	RW	0x0	sss This bit is set by the system firmware/BIOS to indicate platform support for staggered devices' spin-up. SATA Host supports this feature through the P0CMD.SUD bit functionality.
26	RO	0x1	salp Supports auto-generating Link Layer requests to the PARTIAL or SLUMBER power management states when there are no commands to process.
25	RO	0x1	sal Supports activity indication using signal P0_act_led.
24	RO	0x1	sclo Supports the P0CMA.CLO bit functionality for Port Multiplier devices' enumeration.

Bit	Attr	Reset Value	Description
23:20	RO	0x3	iss Supports SATA 1.5Gb/s, SATA 3Gb/s, SATA 6Gb/s interface speeds.
19	RO	0x0	snzo This feature is not supported.
18	RO	0x1	sam Supports AHCI mode only and does not supports legacy, task-file based register interface.
17	RO	0x1	spm Supports command-based switching Port Multiplier on any of its ports.
16	RO	0x1	fbss FIS-Based Switching supported.
15	RO	0x1	pmd Supports multiple DRQ block data transfer for the PIO command protocol.
14	RO	0x1	ssc Supports transitions to the interface SLUMBER power management state.
13	RO	0x1	psc Supports transitions to the interface PARTIAL power management state.
12:8	RO	0x1f	ncs Supports 32 command slots per Port.
7	RO	0x1	cccs Command Completion Coalescing Supported
6	RO	0x0	ems SATA Host does not support enclosure management.
5	RO	0x0	sxs The options for this field are: 1'h0: Indicates that the SATA Host has no ports that have a signal only connector externally accessible; 1'h1: Indicates that the SATA Host has one or more ports that has a signal only connector (power is not part of that connector) that is externally accessible. When this bit is set to 1, the software can refer to the P0CMD.ESP bit to determine whether a specific Port has its signal connector externally accessible.
4:0	RO	0x00	np Indicating the numbers of ports supported by the SATA Host.

SATA_GHC

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x1	ae This bit is always set since SATA Host supports only AHCI mode as indicated by the CAP.SAM=1.
30:2	RO	0x00000000	reserved
1	RW	0x0	ie This global bit enables interrupts from the SATA Host. When cleared, all interrupt sources from all the ports are disabled. When set, interrupts are enabled and ant SATA Host interrupt event caused interrupt assertion.

Bit	Attr	Reset Value	Description
0	WO	0x0	hr When set by the software, this bit causes an internal Global reset of the SATA Host. All state machines that relate to data transfers and queuing return to and idle state, and all the ports are re-initialized by sending COMRESET when staggered spin-up is not supported. When staggered spin-up is supported, then the software must spin-up each port after this reset has complete.

SATA_IS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	ips When set, this bit indicates that the corresponding Ports or Command Completion Coalescing logic has an interrupt pending. The software can use this information to determine which ports require service after an interrupt. The bits of this field are set by the ports that have interrupt events pending in the P0IS bits and enabled by the P0IE or CCC interrupt is generated. Set bits are cleared by the software writing 1 to all bits to clear.

SATA_PI

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pi This register is bit significant. 1'h0: The Port is not available for the software to use; 1'h1: The corresponding Port is available for the software to use.

SATA_VS

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	mjr Indicates that the major AHCI version is 1.
15:0	RO	0x0300	mnr Indicates that the minor AHCI version is 30 or 31.

SATA_CCC_CTL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	tv This field specifies the CCC time-out value in 1ms intervals. The software loads this value prior to enabling CCC.
15:8	RW	0x01	cc This field specifies the number of command completions that are necessary to cause a CCC interrupt. The value 8'h00 for this field disables CCC interrupts being generated based on the number of commands completed. In this case, CCC interrupts are only generated based on the timer.
7:3	RO	0x01	intr_int This field specifies the interrupt used by the ccc feature, using the number of ports configured for the core.
2:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	en The options for this field are: 1'h0: CCC feature is disabled and no CCC interrupts are generated; 1'h1: CCC feature is enabled and CCC interrupts may be generated based on the time-out or command completion conditions.

SATA_CCC_PORTS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	prt This field is bit significant. Each bit corresponds to a particular Port, where bit 0 corresponds to Port0.The options for this field are: 1'h0: The corresponding Port is not part of the CCC feature. 1'h1: The corresponding Port is part of the CCC feature. Bits set in this register must also have the corresponding bit set in the PI (Ports Implemented Register).

SATA_CAP2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	deso SATA Host supports DevSleep entrance from any Link state (active, Partial, or Slumber).
4	RO	0x0	sadm SATA Host supports hardware assertion of the P0_phy_devslp output after the idle timer expires.
3	RO	0x0	sds SATA Host supports hardware assertion of the P0_phy_devslp output after the idle timer expires.
2	RO	0x0	apst Automatic Partial to Slumber Transitions
1	RO	0x0	nvmp SATA Host does not support NVMHCI.
0	RO	0x0	bph SATA Host does not support BOH.

SATA_BISTAFR

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	ncp Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for Far-end transmit only mode (BISTAFR.PD=0xC0 or 0xE0): 8'h4A: High frequency test pattern (HFTP); 8'h78: Mid frequency test pattern (MFTP); 8'h7E: Low frequency test pattern (LFTP); 8'h7F: Simultaneous switching outputs pattern (SSOP); 8'hAB: Low frequency spectral component pattern (LFSCP); 8'hB5: High transition density pattern (HTDP); 8'hF1: Low transition density pattern (LTDP). When none of these values is decoded, the Lone bit pattern (LBP) is transmitted by default.
7:0	RO	0x00	pd Indicates the pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. It is used to put the SATA Host in one of the following BIST modes: 8'h08: Far-end Analog (when PHY supports this mode); 8'h10: Far-end Retimed; 8'hC0: Far-end Transmit only; 8'hE0: Far-end Transmit only with scrambler bypassed. All other values should not be used by the device, otherwise, the FIS is negatively acknowledged with R_ERRp. For Far-end Transmit only modes BISTAFR.NCP field contains the required data pattern.

SATA_BISTCR

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	old_phy_ready Old phy_ready
24	RO	0x0	late_phy_ready When set, this bit changes monitoring of phy_ready to be the "OR" of phy_ready or phy_rx_data_vld so that a "late arriving", or even "never asserting" phy_ready. This requires that phy_rx_data_vld does not become valid until after the PHY has locked onto post OOB incoming ALIGNs, and the ALIGNs are valid from the PHY. This will not work if phy_rx_data_vld is asserted during OOB data bursts. This behavior is intended for PHYs that assert phy_ready late, but will also work if phy_ready never asserts or is not present.
23:21	RO	0x0	reserved
20	WO	0x0	ferlb When set, this bit is used to put the SATA Host Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0.
19	RO	0x0	reserved
18	WO	0x0	txo This bit is used to initiate transmission of one of the non-compliant patterns defined by the BISTCR.PATTERN value when the device is disconnected.

Bit	Attr	Reset Value	Description
17	WO	0x0	cntclr This bit clears BIST error count registers. This field is one-shot type and reads returns 0. 1'h1: Clear BISTFCTR, BISTSR, and BISTDECR registers.
16	WO	0x0	nearlb This bit places the Port PHY into Near-end Analog loopback mode. This field is one-shot type and reads returns 0. 1'h0: Near-end Analog loopback disabled; 1'h1: Near-end Analog loopback request. BISTCR.PATTERN field contains the appropriate pattern. This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode.
15	RW	0x0	llb When set, masks out phy_sig_det from the OOB Detector in BIST Loopback Mode, and the only way to exit BIST Loopback mode is to clear the register bit (requires access to the Device AMBA register interface), then issue COMRESET or receive COMINIT as normal. Alternately, a power on reset will automatically clear the BIST Loopback Mode register bit.
14	RO	0x0	qphyinit When set, this bit enables quick PHY initialization feature. The Link does not require any ALIGNs to transition from OOB to normal operation.
13	RW	0x0	errlossen This bit is cleared until it is set via programming.
12	RW	0x0	sdfe This bit is cleared until it is set via programming. It is not affected by a Global reset or COMRESET.
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	llc This field controls the Port Link Layer functions: scrambler, de-scrambler, and repeat primitive drop. Note the different meanings for normal and BIST modes of operation: Bit 8 - SCRAM The options for this field are: 1'h0: Scrambler disabled in normal mode, enabled in BIST mode; 1'h1: Scrambler enabled in normal mode, disabled in BIST mode. Bit 9 - DESCRAM The options for this field are: 1'h0: Descrambler disabled in normal mode, enabled in BIST mode; 1'h1: Descrambler enabled in normal mode, disabled in BIST mode. Bit 10 - RPD The options for this field are: 1'h0: Repeat primitive drop function disabled in normal mode, NA in BIST mode; 1'h1: Repeat primitive drop function enabled in normal mode, NA in BIST mode. The SCRAM bit is cleared (enabled) by the Port when the Port enters a responder far-end transmit BIST mode with scrambling enabled (BISTAFR.PD=0xC0). In normal mode, the functions scrambler, descrambler, or RPD can be changed only during Port reset (P0SCTL.DET=0x1)
7	RO	0x0	reserved
6	RW	0x0	erren This bit is used to allow or filter (disable) PHY internal errors outside the FIS boundary to set corresponding P0SERR bits. The options for this field are: 1'h0: Filter errors outside the FIS, allow errors inside the FIS; 1'h1: Allow errors outside or inside the FIS.
5	RW	0x0	flip This bit is used to change disparity of the current test pattern to the opposite every time its state is changed by the software.
4	RW	0x0	pv This bit is used to select either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP patterns. The options for this field are: 1'h0: Short pattern version; 1'h1: Long pattern version.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	pattern This field defines one of the following SATA-compliant patterns for Far-end Retimed/Far-end Analog/Near-end Analog initiator modes, or non-compliant patterns for Transmit-only responder mode when initiated by the software writing to the BISTCR.TXO bit. The options for this field are: 4'h0: Simultaneous switching outputs pattern (SSOP); 4'h1: High transition density pattern (HTDP); 4'h2: Low transition density pattern (LTDP); 4'h3: Low frequency spectral component pattern (LFSCP); 4'h4: Composite pattern (COMP); 4'h5: Lone bit pattern (LBP); 4'h6: Mid frequency test pattern (MFTP); 4'h7: High frequency test pattern (HFTP); 4'h8: Low frequency test pattern (LFTP). All other values are reserved and should not be used. If the value is none of the listed previously, Composite pattern (COMP) is transmitted by default.

SATA_BISTFCTR

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	count Received BIST FIS Count

SATA_BISTSR

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0xff	brsterr This field contains the burst error count. It is accumulated each time a burst error condition is detected: DWORD error is detected in the received frame and 1.5 seconds (27,000 frames) passed since the previous burst error was detected.
15:0	RO	0xffff	framerr This field contains the frame error count. It is accumulated (new value is added to the old value) each time a new BIST frame with a CRC error is received.

SATA_BISTDECR

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RO	0xfffff000	dwerr This field contains the DWORD error count. It is accumulated (new value is added to the old value) each time a new BIST frame is received.

SATA_MEMEDFBSERRDATA

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	mem_fbs_err_synd This field logs the error syndrome of the RAM Data Ecc/Parity error, if the syndrome with excess the range of the filed MEMEDFBSERRDATA.mem_fbs_err_synd, extra bits is logged in another register MEMEDFBSERRDATAU.mem_fbs_err_synd_u.
11:0	RO	0x000	mem_fbs_err_addr This filed logs the error location (the address of which the RAM data Ecc/Parity error detected)

SATA_MEMEDADDRERRINJ

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	ued Indicates a single bit uncorrected, or multiple bit error was detected. Cleared by writing '1' to this field.
16	RW	0x0	ced Indicates a single bit error was corrected. Cleared by writing '1' to this field.
15:5	RO	0x000	reserved
4	RW	0x0	oneB_2B When MEM_DP_TYPE=1 (Parity), only single-bit error injection is allowed in Parity mode and hence the value programmed in this bit is 'don't care'.
3	RW	0x0	cont Selects 'one-shot' (0) or 'continuous' (1) errors
2:1	RW	0x0	mem_sel 2'h0: All three memory interfaces; 2'h1: RX FIFO Memory; 2'h2: TX FIFO Memory; 2'h3: FBS RAM.
0	RW	0x0	err_inj_valid The values in the rest of the fields of this register are valid only when this bit is set to 1.

SATA_OOBR

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31	RW	0x0	we The options for this field are: 1'h0: OOBR bits [30:0] are read-only; 1'h1: OOBR bits [30:0] can be written. This bit is cleared when COMRESET is detected.
30:24	RW	0x00	cwMin This field is RW when WE=1 and RO when WE=0.
23:16	RW	0x00	cwMax This field is RW when WE=1 and RO when WE=0.
15:8	RW	0x00	ciMin This field is RW when WE=1 and RO when WE=0.
7:0	RW	0x00	ciMax This field is RW when WE=1 and RO when WE=0.

SATA_MEMEDTXFERRDATAU

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mem_txf_err_synd_u When the TX FIFO RAM Data parity error syndrome width excess the range of the register MEMEDTXFERRDATA.mem_tx_err_synd, extra bits is logged in this field.

SATA_DIAGNR3
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fbcsw_cnt FIS-based context switching counter

SATA_TIMER1MS
Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	timv This field contains the following value for the internal timer to generate 1-ms tick: Famba*1000, where Famba = AMBA clock frequency in MHz. The options for this field are: RW when CCC_CTL.EN=0 and CCC_SUPPORT = Include RO when CCC_CTL.EN=1 and CCC_SUPPORT = Include RW when CCC_SUPPORT=Exclude and DEVSLP_SUPPORT=Include

SATA_MEMDPCR
Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	mem_par_even This value is derived from the MEM_PAR_EVEN parameter. The options for this field are as follows: 1'h0: Generate odd type of parity for data (if parity type protection selected) and address; 1'h1: Generate even type of parity for data (if parity type protection selected) and address.
8	RW	0x0	mem_err_inj_loc The options for this field are as follows: 1'h0: Inject error on data bits; 1'h1: Inject error on data check bits.
7	RW	0x0	mem_ed_log_clr_en 1'h0: All error detection and correction logging registers are cleared by Global or COMRESET. 1'h1: All error detection and correction logging registers are cleared only when MEMDPCR.EM_ED_LOG_CLR is set.
6	WO	0x0	mem_ed_log_clr This field clears all error detection and correction logging registers when written. This bit clears itself one cycle after written.
5	RW	0x0	mem_ed_log_dis This field disables error detection and correction logging when set.
4	RW	0x0	mem_ed_ce_en This field enables correctable error detection interrupt (INFS). (For diagnostic purposes only)

Bit	Attr	Reset Value	Description
3	RW	0x0	mem_ed_pdmaf_dis This field disables PDMA from entering a fatal error state when an incorrect error is detected. (For diagnostic purposes only)
2	RW	0x0	mem_ed_ifs_dis This field disables setting the IFS interrupt register bit (interface fatal error status interrupt) when an incorrect error is detected when MEM_DP_TYPE selects ECC, or a Parity error is detected when MEM_DP_TYPE selects Parity.
1	RW	0x0	mem_ec_dis When set, disables the single error correcting features everywhere, and all errors are reported as incorrect. This field has no effect when MEM_DP_TYPE = Parity or when MEM_DP_EN = 0.
0	RW	0x0	mem_ed_dis All ECC/Parity error detection, correction, interrupt generation and Fatal error state transitions are disabled when this bit is set to 1. This field has no effect when the hardware parameter MEM_DP_EN = 0.

SATA_TESTR

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	bsel This field is used to select a bank for BIST or Data Protection operation or Address Protection operation. The options for this field are: 2'h0: BIST registers selected 2'h1: Data Protection registers selected 2'h2: Address Protection registers selected 2'h3: Reserved
23:19	RO	0x00	reserved
18:16	RW	0x0	psel This field is used to select a Port for BIST operation. The options for this field are: 3'h0: Port0 is selected; 3'h1: Port1 is selected; 3'h2: Port2 is selected; 3'h3: Port3 is selected; 3'h4: Port4 is selected; 3'h5: Port5 is selected; 3'h6: Port6 is selected; 3'h7: Port7 is selected.
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	test_if This bit is used to put the SATA Host slave interface into the test mode. The options for this field are: 1'h0: Normal mode: the read back value of some registers is a function of the SATA Host state and does not match the value written; 1'h1: Test mode: the read back value of the registers matches the value written. Normal operation is disabled. The following registers can be accessed in this mode: GHC register IE bit BISTAFR register NCP and PD bits become read-write BISTCR register LLC, ERREN, FLIP, PV, PATTERN BISTFCTR, BISTSR, BISTDECR become read-write P0CLB/CLBU, P0FB/FBU registers P0IS register RW1C and UFS bits become read-write P0IE register RW bits (CPDE is RO if DEV_CP_DET = Exclude, DMPE bit is RO if DEV_MP_SWITCH = Exclude) P0CMD register ASP, ALPE, DLAE, ATAPI, PMA bits P0TFD, P0SIG registers become read-write P0SCTL register RW bits [9:8], [5:4], and [2:0] (Bits [2:0] cannot be written with the 3'b001 value if P0CMD.SUD=0) P0SERR register RW1C bits become read-write bits P0SACT, P0CI, P0SNTF registers become read-write P0DMACR register P0PHYCR register P0PHYSR register becomes read-write GPSR register becomes read-write

SATA_VERSION

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	version SATA Host hard-coded hexadecimal version value.

SATA_IDR

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	id Hard-coded hexadecimal identification value.

SATA_P0CLB

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	clb Indicates the 32-bit base physical address for the command list for this Port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1-KB-aligned as indicated by bits [9:0] being read only.
9:0	RO	0x000	reserved

SATA_P0FB

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	fb Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256byte-aligned as indicated by bits [7:0] being read only.
7:0	RO	0x00	reserved

SATA_P0IS

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31	RW	0x0	cpds This bit is set when the P0_cp_det input changes its state due to the insertion or removal of the device. This bit is only valid when the Port supports cold presence detect as indicated by the P0CMD.CPD set to 1.
30	RW	0x0	tfes This bit is set whenever the P0TFD.STS register is updated by the device and the error bit [0] is set.
29	RW	0x0	hbfs This bit is set when SATA Host AMBA Master detects an ERROR response from the slave. Port DMA transitions to a fatal state until the software clears P0CMD.ST bit or resets the interface by way of Port or Global reset.
28	RW	0x0	hbds This bit is always cleared to 0.
27	RW	0x0	ifs This bit is set when any of the following conditions are detected: SYNC escape is received from the device during non-Data or Data FIS transmission or reception (P0SERR.DIAG_S and ERR_P are set); One or more of the following errors are detected during Data FIS transfer: Protocol (P0SERR.ERR_P) CRC (P0SERR.DIAG_C) Handshake (P0SERR.DIAG_H) PHY Not Ready (P0SERR.ERR_C) Unknown FIS is received with good CRC, but the length exceeds 64 bytes; PRD table byte count is zero; DMA Setup FIS is received with a TAG corresponding to inactive (P0SACT bit is cleared) command slot; RAM address protection error detected (when hardware configuration parameter MEM_AP_SUPPORT is set to Include, and the MEM_AP_ERRFB_EN is set to Include, and the MEMDPCR.MEM_ADDR_ED_IFS_DIS register bit is set to 0); and/or Uncorrected error detected (when hardware configuration parameter MEM_DP_SUPPORT is set to Include, and the MEMDPCR.MEM_ED_IFS_DIS register bit is set to 0). Port DMA transitions to a fatal state until the software clears PCMD.ST bit or resets the interface by way of Port or Global reset.

Bit	Attr	Reset Value	Description
26	RW	0x0	infs This bit is set when any of the following conditions are detected: One or more of the following errors are detected during non-data FIS transfer: Protocol (P0SERR.ERR_P) CRC (P0SERR.DIAG_C) Handshake (P0SERR.DIAG_H) PHY Not Ready (P0SERR.ERR_C) Command list underflow during read operation (such as, DMA read) when the software builds command table that has more total bytes than the transaction given to the device Corrected error detected (when hardware configuration parameter MEM_DP_SUPPORT is set to Include, MEM_DP_TYPE is set to ECC, and the MEMDPCR.MEM_ED_CE_EN register bit is set to 1) In both cases Port operation continues normally. When error is detected during non-data FIS transmission, this FIS is retransmitted continuously until it succeeds, or until the software times out and resets the interface.
25	RO	0x0	reserved
24	RW	0x0	ofs This bit is set when command list overflow is detected during read or write operation when the software builds command table that has fever total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears P0CMD.ST bit or resets the interface by way of Port or Global reset.
23	RW	0x0	ipms Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier.
22	RW	0x0	prcs This bit reflects the state of the P0SERR.DIAG_N bit. When set to 1, indicates the internal P0_phy_ready signal changed state. To clear this bit, the software must clear the P0SERR.DIAG_N bit to 0.
21:8	RO	0x0000	reserved
7	RW	0x0	dmps This bit is set when the P0_mp_switch input changes its state as a result of a mechanical switch attached to this Port opening or closing. This bit is valid only when both CAP.SMPS and P0CMD.MPSP are set.
6	RO	0x0	pcs This bit reflects the state of the P0SERR.DIAG_X bit: 1'h0: No change in Current Connect Status; 1'h1: Change in Current Connect Status. This bit is cleared only when P0SERR.DIAG_X is cleared.
5	RW	0x0	dps A PRD with the I bit set has transferred all of its data.

Bit	Attr	Reset Value	Description
4	RO	0x0	ufs When set to 1, indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by the software clearing the P0SERR.DIAG_F bit to 0.
3	RW	0x0	sdbs A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
2	RW	0x0	dss A DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
1	RW	0x0	pss A PIO Setup FIS has been received with the 'I' bit set, it has been copied into system memory, and the data related to that FIS has been transferred.
0	RW	0x0	dhrs A Device-to-Host Register FIS has been received with the 'I' bit set, and has been copied into system memory.

SATA_P0IE
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31	RW	0x0	cpde When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.CPDS=1
30	RW	0x0	tfee when the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.TFES=1
29	RW	0x0	hbfe When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.HBFS=1
28	RW	0x0	hbde When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.HBDS=1
27	RW	0x0	ife When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.IFS=1

Bit	Attr	Reset Value	Description
26	RW	0x0	infe When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.INFS=1
25	RO	0x0	reserved
24	RW	0x0	ofe When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.OFS=1
23	RW	0x0	ipme When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.IPMS=1
22	RW	0x0	prce When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.PRCS=1
21:8	RO	0x0000	reserved
7	RW	0x0	dmpe When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.DMPS=1
6	RO	0x0	pce When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.PCS=1
5	RW	0x0	dpe When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.DPS=1
4	RO	0x0	ufe When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.UFS=1

Bit	Attr	Reset Value	Description
3	RW	0x0	sdbe When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.SDBS=1
2	RW	0x0	dse When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.DSS=1
1	RW	0x0	pse When the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.PSS=1
0	RW	0x0	dhre Dependencies: when the following conditions are true, the interrupt output signal is asserted: This bit=1 GHC.IE=1 P0IS.DHRS=1

SATA_P0CMD
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	icc This field is used to control power management states of the interface. When the Link layer is currently in the L_IDLE state or L_NoCommPower state, writes to this field cause the Port to initiate a transition to the interface power management state requested. When the Link layer is not currently in the L_IDLE state or L_NoCommPower, writes to this field have no effect. 4'h1: Active. This causes the Port to request a transition of the interface into the active state; 4'h2: Partial. This causes the Port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state; 4'h6: Slumber. This causes the Port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state; Else: Reserved.

Bit	Attr	Reset Value	Description
27	RW	0x0	asp The options for this field are: When set to 1, and P0CMD.ALPE=1, the Port aggressively enters the SLUMBER state when one of the following conditions is true: The Port clears the P0CI and the P0SACT register is cleared. The Port clears the P0SACT register and P0CI is cleared. When cleared to 0, and P0CMD.ALPE=1, the Port aggressively enters the PARTIAL state when one of the following conditions is true: The Port clears the P0CI register and the P0SACT register is cleared. The Port clears the P0SACT register and P0CI is cleared.
26	RW	0x0	alpe When set to 1, the Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of the P0CMD.ASP bit. When cleared to 0, aggressive power management state transition is disabled.
25	RW	0x0	dlae When set to 1, P0CMD.ATAPI=1, and commands are active, the Port asserts P0_act_led output.
24	RW	0x0	atapi This bit is used by the Port to control whether to assert P0_act_led output when commands are active. The options for this field are: 1'h0: Non-ATAPI device; 1'h1: ATAPI device.
23	RW	0x0	apste When this bit is set and the SATA Host Link layer negotiates Partial power management state with the device, it transitions into the Slumber state directly, regardless whether it was host software-, Port (aggressive)-, or device-initiated.
22	RW	0x0	fbscp When set to 1, indicates that this Port supports Port Multiplier FIS-based switching. When cleared to 0, indicates that this Port does not support FIS-based switching.
21	RW	0x0	esp When set to 1, indicates that this Port's signal only connector is externally accessible. When set to 1, CAP.SXS is also set to 1. When cleared to 0, indicates that this Port's signal only connector is not externally accessible.
20	RW	0x0	cpd The options for this field are: 1'h0: Platform does not support cold presence detection on this Port; 1'h1: Platform supports cold presence detection on this Port. When this bit is set to 1, P0CMD.HPCP must also be set to 1.
19	RW	0x0	mpsp To enable the SATA Host mechanical presence detection feature. The options for this field are: 1'h0: Indicates the platform does not support a mechanical presence switch attached to this Port. When this bit is set to 1, P0CMD.HPCP should also be set to 1; 1'h1: Indicates the platform supports a mechanical presence switch attached to this Port.

Bit	Attr	Reset Value	Description
18	RW	0x0	hpcp The options for this field are: 1'h0: Indicates that this Port's signal and power connectors are not externally accessible; 1'h1: Indicates that this Port's signal and power connectors are externally accessible via a joint signal-power connector for blind mate device hot plug.
17	RO	0x0	pma The software is responsible for detecting whether a Port Multiplier is present; the SATA Host Port does not auto-detect the presence of a Port Multiplier. The options for this field are: 1'h0: A Port Multiplier is not attached to this Port; 1'h1: A Port Multiplier is attached to this Port.
16	RO	0x0	cps This bit reports whether a device is currently detected on this Port as indicated by the P0_cp_det input state. The options for this field are: 1'h0: No device attached to this Port; 1'h1: Device is attached to this Port.
15	RO	0x0	cr When this bit is set to '1', the command list DMA engine for this Port is running.
14	RO	0x0	fr When set to '1', the FIS Receive DMA engine for the Port is running.
13	RO	0x0	mpss The software must use this bit only when both CAP.SMPS and P0CMD.MPSP are set. This bit reports the state of a mechanical presence switch attached to this Port as indicated by the P0_mp_switch input state. The options for this field are: 1'h0: Switch is closed; 1'h1: Switch is open. When CAP.SMPS=0 then this bit is cleared to 0.
12:8	RW	0x00	ccs This field is set to the command slot value of the command that is currently being issued by the Port. When P0CMD.ST transitions from 1 to 0, this field is cleared again to 5'h0. After P0CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P0CMD.CCS+1.
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	fre When set to 1, the Port may post received FISes into the FIS receive area pointed to by P0FB. When cleared, received FISes are not accepted by the Port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. The software must not set this bit until P0FB has been programmed with a valid pointer to the FIS receive area. When the software wishes to move the base, this bit must first be cleared, and the software must wait for the P0CMD.FR bit to be cleared.
3	RW	0x0	clo Setting this bit to 1 cause P0TFD.STS.BSY and P0TFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the P0TFD.STS register. This bit is cleared to 0 when P0TFD.STS.BSY and P0TFD.STS.DRQ have been cleared to 0. A write to this register with a value of '0' has no effect. This bit should only be set to 1 immediately prior to setting P0CMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and results in indeterminate behaviors.
2	RW	0x0	pod This bit is read/write when cold presence detection is supported on this Port as indicated by P0CMD.CPD=1. This bit is read-only 1 when cold presence detection is not supported and P0CMD.CPD=0. When set, the Port asserts the P0_cp_pod output pin so that it may be used to provide power to a cold-presence detectable Port.
1	RW	0x0	sud This bit is read/write when staggered spin-up is supported as indicated by the CAP.SSS=1. This bit is read-only 1 when staggered spin-up is not supported and CAP.SSS=0. On an edge detect from 0 to 1, the Port starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface.
0	RW	0x0	st When set to 1, the Port processes the command list. When cleared, the Port does not process the command list. Whenever this bit is changed from a 0 to a 1, the Port starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the P0CI register is cleared by the Port upon transition into an idle state.

SATA_P0TFD

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	err This field contains the latest copy of the task file error register.

Bit	Attr	Reset Value	Description
7:0	RO	0x00	sts This field contains the latest copy of the task file status register. The bits that affect SATA Host operation are: Bit [7] BSY: Indicates the interface is busy; Bits [6:4] cs: Command specific; Bit [3] DRQ: Indicates a data transfer is requested; Bits [2:1] cs: Command specific; Bit [0] ERR: Indicates an error during the transfer.

SATA_P0SIG

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sig This field contains the signature received from a device on the first D2H Register FIS. The bit order as follows: Bits [31:24]: LBA High (Cylinder High) Register; Bits [23:16]: LBA Mid (Cylinder Low) Register; Bits [15:8]: LBA Low (Sector Number) Register; Bits [7:0]: Sector Count Register. This field is updated once after a reset sequence (cause by asynchronous, port, or soft reset). Reset on Global or Port reset.

SATA_P0SSTS

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x0	ipm Indicates the current interface state. The options for this field are: 4'h0: Device not present or communication not established; 4'h1: Interface in Active state; 4'h2: Interface in Partial power management state; 4'h6: Interface in Slumber power management state; 4'h8: Interface in DevSleep power management state.
7:4	RO	0x0	spd Indicates the negotiated interface communication speed. The options for this field are: 4'h0: Device not present or communication not established; 4'h1: 1.5 Gb/s communication rate negotiated; 4'h2: 3.0 Gb/s communication rate negotiated; 4'h3: 6.0 Gb/s communication rate negotiated.
3:0	RO	0x0	det Indicates the interface device detection and PHY state. The options for this field are: 4'h0: No device detected and PHY communication not established; 4'h1: Device presence detected but PHY communication not established (COMINIT is detected); 4'h3: Device presence detected and PHY communication established ('PHY Ready' is detected); 4'h4: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved.

SATA_P0SCTL

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	ipm This field indicates which power states the Port PHY interface is allowed to transition to. When an interface power management state is disabled, the Port does not initiate that state and any request from the device to enter that state is rejected via PMNAKp. The options for this field are: 2'h0: No interface power management state restrictions; 2'h1: Transitions to the Partial state disabled; 2'h2: Transitions to the Slumber state disabled; 2'h3: Transitions to both Partial and Slumber states disabled.
7:6	RO	0x0	reserved
5:4	RW	0x0	spd This field indicates the highest allowable speed of the Port PHY interface. The options for this field are: 2'h0: No speed negotiation restrictions 2'h1: Limit speed negotiation to SATA 1.5 Gb/s communication rate 2'h2: Limit speed negotiation to SATA 3.0 Gb/s communication rate 2'h3: Limit speed negotiation to a rate not greater than SATA 6.0 Gb/s communication rate.
3	RO	0x0	reserved
2:0	RW	0x0	det Controls the Port's device detection and interface initialization. The options for this field are: 3'h0: No device detection or initialization action requested 3'h1: Perform interface initialization sequence to establish communication. This results in the interface being reset and communication re initialized. The SATA Host asserts the corresponding P0_phy_reset(_n) output when DET=0x1. It negates P0_phy_reset(_n) and sends COMRESET OOB sequence when DET=0x0. 3'h4: Disable the Serial ATA interface and put the Port PHY in offline mode.

SATA_P0SERR

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	diag_x This bit is set to 1 when PHY COMINIT signal is detected. This bit is reflected in the P0IS.PCS bit.
25	RW	0x0	diag_f This bit indicates that one or more FISes were received by the Transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64 bytes.
24	RW	0x0	diag_t This bit indicates that a Transport Layer protocol violation was detected since the last time this bit was cleared.

Bit	Attr	Reset Value	Description
23	RW	0x0	diag_s This bit indicates that one or more Link state machine error conditions was encountered. One of the conditions that cause this bit to be set is device doing SYNC escape during FIS transmission.
22	RW	0x0	diag_h This bit indicates that one or more R_ERRp was received in response to frame transmission. Such errors may be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	RW	0x0	diag_c This bit indicates that one or more CRC errors were detected by the Link layer during FIS reception.
20	RO	0x0	diag_d This bit is always cleared to 0 since it is not used by the AHCI specification.
19	RW	0x0	diag_b This bit indicates errors were detected by 10b/8b decoder.
18	RW	0x0	diag_w This bit is set when PHY COMWAKE signal is detected.
17	RW	0x0	diag_i This bit is set when the PHY detects some internal error as indicated by the assertion of the P0_phy_rx_err input.
16	RW	0x0	diag_n This bit indicates that the PHY Ready signal changed state. This bit is reflected in the P0IS.PRCS bit.
15:12	RO	0x0	reserved
11	RW	0x0	err_e This bit is set to 1 when one or more AMBA bus ERROR responses are detected on the master interface.
10	RW	0x0	err_p This bit is set to 1 when any of the following conditions are detected. Transport state transition error (DIAG_T) Link sequence error (DIAG_S) RX FIFO overflow Link bad end error (WTRM instead of EOF is received).
9	RW	0x0	err_c This bit is set to 1 when PHY Ready signal is negated due to the loss of communication with the device or problems with interface, but not after transition from active to Partial or Slumber power management state.
8	RW	0x0	err_t This bit is set when any of the following P0SERR register bits are set during Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake) ERR_C ('PHY Ready' negation)
7:2	RO	0x00	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	err_m This bit is set to 1 when the PHY Ready condition is asserted under the following conditions: At any time except when there is a transition from power-down mode to Active state After interface initialization (after power on or COMRESET)
0	RW	0x0	err_i This bit is set when any of the following P0SERR register bits is set during non-Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake)

SATA_P0SACT

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ds This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Software sets this field prior to issuing a native queued command for a particular command slot. Prior to writing P0CI[TAG] to 1, the software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. This field is cleared to 0 when: The software writes P0CMD.ST from a 1 to a 0. The device sends a Set Device Bits FIS to the Port. The Port clears bits in this field that are set in the SActive field of the Set Device Bits FIS. The Port clears only bits that correspond to native queued commands that have completed successfully. This field is not cleared by the following: Port reset (COMRESET). Software reset.

SATA_P0CI

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ci This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by the software to indicate to the Port that a command has been built in system memory for a command slot and may be sent to the device. When the Port receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by the software when P0CMD.ST is set to 1.

SATA_P0SNTF

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	pmn This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the SATA Host Port with the Notification bit set: PM Port 0 sets bit 0. PM Port 1 sets bit 1. ... PM Port 15 sets bit 15. Individual bits are cleared by the software writing 1s to the corresponding bit positions. This field is reset on Global reset, but it is not reset by Port reset (COMRESET) or software reset.

SATA_P0FBS

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	dwe This field is set by the SATA Host core to the value of the Port Multiplier port number of the device that experienced a fatal error condition. This field is only valid when P0FBS.SDE=1.
15:12	RW	0x0	ado This field is hard-wired to the FBS_PMPN_MAX value.
11:8	RW	0x0	dev Software sets this field to the Port Multiplier port value of the next command to issue. This field enables the SATA Host core to know the port the command to be issues to without fetching the command header. Software should not issue commands to multiple Port Multiplier ports on the same write of the P0CI register. This bit is reset on Global reset.
7:3	RO	0x00	reserved
2	RW	0x0	sde When this field is set to 1 and a fatal error condition has occurred, the SATA Host core believes the error is localized to one device such that software's first error recovery step should be to utilize the P0FBS.DEC functionality. When cleared to 0 and a fatal error condition has occurred, the error applies to the entire Port. To clear the error, software should clear P0CMD.ST to 0. This bit is cleared on P0FBS.DEC being set to 1 or on P0CMD.ST being cleared to 0. This bit is reset on Global reset.
1	RW	0x0	dec When set to 1 by software, the SATA Host core clears the device-specific error condition. It flushes any commands outstanding for the device that experienced the error, including clearing P0CI and P0SACT bits for that device to 0. The SATA Host core clears this bit to 0 when it completes error recovery actions. When software writes a 0 to this bit, there is no effect. Software should only set this bit to 1 if P0FBS.EN=1 and P0FBS.SDE=1. This bit is reset on Global reset.

Bit	Attr	Reset Value	Description
0	RW	0x0	en 1'h0: FIS-based switching is not being used (command-based switching is used instead). Software should only change the value of this bit when P0CMD.ST=0; 1'h1: A Port Multiplier is attached and the SATA Host uses FIS-based switching to communicate with it. This bit is reset on Global reset.

SATA_P0DMACR

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	rxts This field defines the Port DMA transaction size in FIFO words for receive (system bus write, device read) operation. The options for this field are: 4'h0: 1 4'h1: 2 4'h2: 4 4'h3: 8 4'h4: 16 4'h5: 32 4'h6: 64 4'h7: 128 4'h8: 256 4'h9: 512 4'hA: 1024 All other values are reserved and should not be used. This field is read-write when P0CMD.ST=0 and read-only when P0CMD.ST=1.
3:0	RW	0x0	txts This field defines the DMA transaction size in FIFO words for transmit (system bus read, device write) operation. The options for this field are: 4'h0: 1 4'h1: 2 4'h2: 4 4'h3: 8 4'h4: 16 4'h5: 32 4'h6: 64 4'h7: 128 4'h8: 256 4'h9: 512 4'hA: 1024 All other values are reserved and should not be used. This field is read-write when P0CMD.ST=0 and read-only when P0CMD.ST=1.

15.5 Interface Description

Table 1- 1 SATA host interface description

Module Pin	Dir	Pad Name	IOMUX Setting
SATA0_CPDET	I	I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u	SYS_GRF_SOC_CON7[1:0]=2’b00 BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4’hd
SATA1_CPDET	I	I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u	SYS_GRF_SOC_CON7[1:0]=2’b01 BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4’hd
SATA2_CPDET	I	I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u	SYS_GRF_SOC_CON7[1:0]=2’b10 BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4’hd
SATA0_MPSWITCH	I	I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u	SYS_GRF_SOC_CON7[1:0]=2’b00 BUS_IOC_GPIO0D_IOMUX_SEL_H[7:4]=4’hd
SATA1_MPSWITCH	I	I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u	SYS_GRF_SOC_CON7[1:0]=2’b01 BUS_IOC_GPIO0D_IOMUX_SEL_H[7:4]=4’hd
SATA2_MPSWITCH	I	I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u	SYS_GRF_SOC_CON7[1:0]=2’b10 BUS_IOC_GPIO0D_IOMUX_SEL_H[7:4]=4’hd
SATA0_CPPOD	O	I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u	SYS_GRF_SOC_CON7[1:0]=2’b00 BUS_IOC_GPIO0C_IOMUX_SEL_H[11:8]=4’hd
SATA1_CPPOD	O	I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u	SYS_GRF_SOC_CON7[1:0]=2’b01 BUS_IOC_GPIO0C_IOMUX_SEL_H[11:8]=4’hd

Module Pin	Dir	Pad Name	IOMUX Setting
SATA2_CPPOD	O	I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u	SYS_GRF_SOC_CON7[1:0]=2'b10 BUS_IOC_GPIO0C_IOMUX_SEL_H[11:8]=4'hd
SATA0_ACTLED	O	BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDOUT_M0/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d	BUS_IOC_GPIO4B_IOMUX_SEL_H[11:8]=4'h6
SATA0_ACTLED	O	PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED_M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3_d	BUS_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h6
SATA1_ACTLED	O	BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d	BUS_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'h6
SATA1_ACTLED	O	PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1_d	BUS_IOC_GPIO1A_IOMUX_SEL_L[7:4]=4'h6
SATA2_ACTLED	O	MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u	BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'h6
SATA2_ACTLED	O	MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u	BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12]=6'h6

15.6 Application Notes

15.6.1 Data transfer

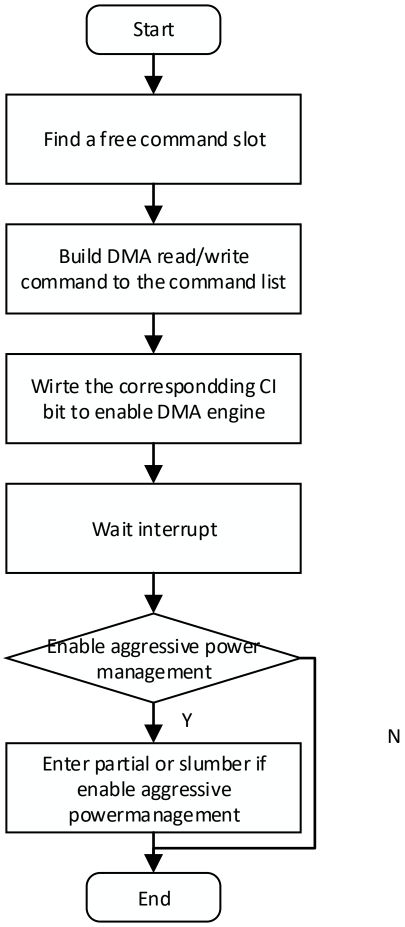

Fig. 1- 1 Data transfer flow

15.6.2 Port multiple support

When a port is connected to a Port Multiplier, software must first enumerate it by issuing software reset to Port 0xF (control Port) on the Port Multiplier. When the signature returned corresponds to a Port Multiplier, then a Port Multiplier is attached. When the signature returned corresponds to another device type, then a Port Multiplier is not attached.

The SATA host provides command list override feature via CMD.CLO to help software reliably enumerate the Port Multiplier:

- software ensures that CMD.ST bit is 0;
- software constructs the two register FISes required for a software reset in the command list, where the PM port field value in the register FIS is set to 0xF;
- software set CMD.CLO to 1 to force the BSY and DRQ bits in the TFD register to be cleared;
- software sets CMD.ST bit to 1 and set appropriate CI bits in order to begin execution of the software reset command.

15.6.3 Interrupt

The SATA host uses two-tiered interrupt structure.

First tier (GIS register)

The first tier is identified by the GIS and GHC registers. GHC.IE bit enables interrupts for the entire host: when it is cleared, interrupt output is not asserted regardless of any bits set in the GIS register. GHC.IE bit acts as a mask and does not affect the setting of any interrupt status bits.

Second tier (PIS registers)

The second tier is identified in each port through the PIS (status) and PIE (interrupt enable) register. The PIS register has various interrupt bits that can be individually enabled or disabled by setting the corresponding bit in the PIE. The status bit in the PIS is always set regardless of the setting of the corresponding PIE bit.

15.6.4 reset condition

System reset
System bus resets SATA host by asserting aresetn=0. It is usually initiated on power-up or during system bus failure. All components of the host are initialized, including ports, Generic registers, BIU.
Global reset
Software may globally reset host by setting GHC.HR to 1. When software sets the GHC.HR bit to 1, the host performs an internal reset action, then clears this bit to 0 when the reset is complete. A software writes of 0 to GHC.HR has no affect.
Port reset (COMRESET)
Software causes a Port reset by writing 1h to the SCTL.DET field to invoke COMRESET on the interface and start a re-establishment of the PHY Layer communication. Software should wait at least 1ms before clearing SCTL.DET to 0h. After clearing SCTL.DET to 0h, software should wait for communication to be re-established as indicated by 0 of SSTS.DET being set to 1. Then software should write all ones to SERR register to clear any bits that were set as part of the Port reset.
Software reset
Software builds two H2D register FISes in the command list. The first register FIS has the SRST bit set to 1 in the control field of the register FIS, the “C” bit is cleared to “0” in the register FIS, and the command table has the CH[R] (reset) and CH[C] (clear BSY ON R_OK) bits set to “1”. The CH[R] bit causes the Port to perform a SYNC escape when necessary to put the device into an idle condition before sending the software reset. The CH[C] bit needs to be set for the first register FIS to clear the BSY bit and proceed to issue the next register FIS since the device does not send a response to the first register FIS in a software reset sequence. The second register FIS has SRST=”0” in the control field of the register FIS, the “C” bit is cleared to “0” in the register FIS, and the command tables has the CH[R] and CH[C] bits cleared to “0”. When issuing a software reset sequence, there should not be other commands in the command list. Before issuing the software reset, software must clear CMD.ST, wait for the Port to be idle, and then re-set CMD.ST. TFD.STS.BSY and TFD.STS.DRQ must be cleared prior to issuing the reset. When TFD.STS.BSY or TFD.STS.DRQ is still set based on the failed command, then a Port reset should be attempted or command list override should be used.

15.6.5 Staggered spin-up

The CMD.SUD bit is used to manipulate the PHY behavior. SCTL.DET and CMD.SUD must be set correctly in order to avoid illegal combinations of the two values. Table 1-1 describes interaction between the CMD.SUD and SCTL.DET bits.

Table 15-1 CMD.SUD and SCTL.DET interaction

SCTL.DET	CMD.SUD	Mode	Behavior
0	0		Interface is in a reduced power state. When COMINIT is received then SERR.DIAG_X is set and no response is sent to the device COMWAVE is ignored. The application must place the Port into this state only when no device is detected as connected to this Port. In this mode, the Port forces the PHY into a low power state without requesting a SLUMBER transition on the link.
0	0->1		Port sends COMRESET, begins initialization sequence.
0	1		Normal operating state when the Port is performing data transfer.
1	0	Illegal	This combination is prohibited in hardware, i.e. CMD.SUD can’t be cleared when SCTL/DET=1, and SCTL.DET can’t be set to 1 when CMD.SUD=0.
1	1	Reset	Port continuously transmits COMRESET and does not listen for COMINIT. When COMINIT is received in this state, the SERR.DIAG_X bit is set.

SCTL.DET	CMD.SUD	Mode	Behavior
1->0	1	Initialize	Port stops sending COMRESET, being initialization sequence
4	N/A	Off	Port PHY is off.

Software must only clear CMD.SUD when it believes that no device is attached. In listen mode, the Port PHY enters a reduced power state, equivalent to the SLUMBER power management state. The Port PHY enters this state without negotiating a transition to SLUMBER on the link, as asking for a transition to SLUMBER when no device is attached fails, and therefore the PHY remains in a high power state. To avoid this software should ensure that SSTS.DET=0x0 indicating that no device is present before clearing CMD.SUD.

15.6.6 Activity LED

The CAP.SAL=1 indicates that the activity LED feature is enabled to software.
Act_led outputs is used to drive an external LED based upon activity of the Port:

- 1 - LED On
- 0 - LED Off

The port drives the LED active if:

- (CI!=0 or SACT!=0) and CMD.ATAPI = 0
- (CI!=0 or SACT!=0) and CMD.ATAPI = 1 and CMD.DLAE = 1

The Port drives the LED off when CI and SACT are both cleared to 0.

15.6.7 Asynchronous notification

The SATA host supports asynchronous notification feature as indicated by the CAP.SSNT=1. This feature allows an ATAPI device to send a signal to the host when media is inserted or removed and avoid polling the device for media changes. The signal sent to the host is Set Device Bits FIS with the "I" and "N" bits set to "1".
To use asynchronous notification, software should set the IS.SDBS bit to enable interrupt notification on a Set Device Bits FIS. When accesses to the ATAPI device are idle, software should place the device in a low power state. When the device has media change, it signals this to the host with a Set Device Bits FIS. In response to receiving a IS.SDBS interrupt on an idle Port, the software should interrogate the device to determine the cause of the interrupt.
The first DWORD of any FIS received by the host contains a 4-bit Port Multiplier field. The PM port field indicates which Port behind the Port Multiplier issued the FIS to the host. When a set device bits FIS is received by the host and "N" bit is set, the bit position in the SNTF register corresponding to the PM Port field is set. The host sets the IS.SDBS to "1" when the "I" bit is set in the set device bits FIS. This causes an interrupt to be generated when that interrupt is enabled.

15.6.8 BIST operation

1.6.8.1 Loopback responder

Software must ensure that the CMD.ST bit is set, the Port is in idle state, and there are no outstanding commands by checking CI and SACT registers are both cleared, TFD.STS register BSY, DRQ and ERR bits are all cleared.
The host enters one of the BIST loopback responder modes when a corresponding BIST Activate FIS is successfully received from the device and is supported by the host. SSTS.DET field return 4h when read. Since BIST registers' locations are shared between all the active ports, software must first select the Port for BIST operation by writing the Port number to the TESTR.PSEL field before accessing BISTAFR.
The following loopback responder modes are supported by the host:

- Far-end Retimed
  - The Port receives BIST activate FIS with pattern definition field=0x10 from the RX FIFO and stores it in the BIST AFR.PD field
  - All the data received from the device in the form of a SATA-compliant pattern is retimed in the Link Layer and transmitted back to the device.
  - Alternately, this mode can be initiated with device disconnected from the Port PHY

when software writes BISTCR.FERLB=1. After the device is connected to the host, the device must transmit the number of ALIGNs required for the PHY to sync.

- Far-end Analog
  - The Port receives BIST active FIS with pattern definition field =0x08 from the RX FIFO and stores it in the BISTAFR.PD field
  - The Port asserts phy_farafelb signal to the PHY to put it to the Far-end analog loopback mode. The PHY receives and retransmits the raw data without retiming
- Far-end Transmit only
  - The Port receives BIST activate FIS with pattern definition field = 0xC0(scrambling is enabled) or 0xE0 (scrambling is bypassed) from the RX FIFO and stores it in the BISTAFR.PD field. The second DWORD of the BIST activate FIS least significant byte is stored in the BISTAFR.NCP field.
  - The Port transmits corresponding a SATA non-compliant test pattern to the device based on the BISTAFR.NCP value:
    - 0xF1: Low transition density pattern (LTDP)
    - 0xB5: High transition density pattern (HTDP)
    - 0xAB: Low frequency spectral component pattern (LFSCP)
    - 0x7F: Simultaneous switching outputs pattern (SSOP)
    - 0x78: Mid frequency test pattern (MFTP)
    - 0x4A: High frequency test pattern (HFTP)
    - 0x7E: Low frequency test pattern (LFTP)

  If none of the previous pattern is decoded, the Lone bit pattern (LBP) is transmitted by default.
  - Alternately, this mode can be initiated with the device disconnected from the Port PHY when software writes a one to BISTCR.TXO bit. Host transmits non-compliant BIST pattern defined by the value in the BISTCR.PATTERN field.

Loopback responder BIST modes can be exited either when the device signals COMINIT OOB condition, or when the software initiates Port reset.

1.6.8.2 Loopback initiator

The software first selects the Port for BIST operation by writing the Port number to the TESTR.PSEL field, then the required pattern by writing to the BISTCR.PATTERN field.

The software builds a BIST FIS with the required mode in the commands list and sets CTBAz[B]. Once a BIST command is placed into the list, software is not allowed to build any more commands until it clears CMD.ST. After the Port successfully transmits this FIS, it enters this mode and generates/receives the compliant test pattern selected by the BISTCR.PATTERN field.

SSTS.DET return 4h when read. BISTCR and BISTFCTR registers are updated with error/FIS count information for each received BIST FIS.

The following BIST initiator modes can be requested by the software:

- Far-end Retimed
  - The host software writes the BISTCR.PATTERN field to select one of the SATA-defined compliant patterns:
    - 0x0: Simultaneous switching outputs pattern (SSOP)
    - 0x1: High transition density pattern (HTDP)
    - 0x2: Low transition density pattern (LTDP)
    - 0x3: Low frequency spectral component pattern (LFSCP)
    - 0x4: Composite pattern (COMP)
    - 0x5: Lone bit pattern (LBP)
    - 0x6: Mid frequency test pattern (MFTP)
    - 0x7: High frequency test pattern (HFTP)
    - 0x8: Low frequency test pattern (LFTP)
  - The software prepares BIST Activate FIS with bits [23:16] = 8’h10 of the first DWORD in the command list. The Port sends this BIST Activate FIS to the device.
  - After successful transmission of the BIST Activate FIS the Port generates the requested compliant pattern in the form of BIST frames continuously and checks for errors on the receive side.

- BISTCTR register is updated with received BIST frame count and BISTSR - with frame /burst error count. SERR register is updated with CRC, disparity and 10B8B errors for each frame. BISTFCTR, BISTSR, and BISTDECR registers can be cleared by writing 1 to the BISTCR.CNTCLR bit.
- To change the pattern, the software issues a Port Reset, write to the BISTCR.PATTERN field to select a new pattern and re-issues the command by setting the CI bit.

- Far-end Analog
  - The software prepares BIST Activate FIS with bits [23:16] = 8’h8 of the first DWORD in the command list. The Port sends this BIST Activate FIS to the device.
  - The operation proceeds as described in the Far-end retimed test above.

- Near-end Analog
  - This mode can be initiated either in the PARTIAL power management mode or with the device disconnected from the Port PHY. The software issues a PARTIAL power state request to the device via CMD.ICC field and sets the BISTCR.NEALB bit. The BISTCR.PATTERN field selects the required BIST pattern.
  - The Port asserts phy_nearfelb to the PHY. The PHY loops the data from its transmitter to its receiver and ignores any data coming from the device.

- Far-end Transmit only
  - The software prepares BIST Activate FIS in the command list with the second and third DWORDs containing the required pattern, and the first DWORD - with the Pattern definition value corresponding to the required mode - Bit 23 is set, bits 20,19,17 cleared and bits 22,21 and 18 are used to enable the following options:
    - Bit 22 is set - Bypass ALIGN
    - Bit 21 is set - Bypass scrambling
    - Bit 18 is set - primitive bit
  - The Port sends this BIST Activate FIS to the device.
  - After the device acknowledges the reception of this FIS with R_OKp, the Port disables the PHY receiver and transmitter.

Loopback initiator BIST modes can be terminated either by the device when it signals COMINIT OOB condition (except the near-end analog mode), or when the software initiates Port reset.

15.6.9 command completion coalescing

A command completion coalescing (CCC) feature is used to reduce the interrupt and command completion overhead in a heavily-loaded system. The host generates an interrupt to allow software to process completed commands when either of these conditions is true:

- A software-specified number of commands have completed
- A software-specified time-out has expired

This feature applies to all ports selected to be in the CCC set by software via the CCC_PORTS register.

CCC logic used specific register TIMERIMS to generate 1ms interval based on the application clock frequency. Software must load this register with the required value before enabling the CCC feature:

Fappclk*1000, where Fappclk = aclk frequency, in MHz.

Additional Command completion coalescing details and examples can be found in the AHCI specification.

Chapter 16 Multiple Protocol PHY Subsystem

16.1 Overview

The subsystem contains two types of PHY. One is dedicated for PCIe 3.0 protocol with aggregation and bifurcation feature. The other one is a combo of multiple protocol including the PCIe, SATA, USB and QSGMII.

16.1.1 Combo PIPE PHY Overview

The Combo PHY supports physical layer of multiple protocol including USB3.0 Super Speed (5GT/s), PCIe Gen1/Gen2(2.5GT/s and 5GT/s), SATA Gen1/Gen2/Gen3 (1.5GT/3GT/6GT) and QSGMII(1.25GT/5GT). QSGMII mode is not used in current chip.

The key features of the Combo PIPE PHY core include:

- Compatible with PCIe/USB3/SATA/QSGMII base Specification
- Fully compatible with PIPE 4.3 interface specification
- Data rate configurable to 1.25G/1.5G/2.5G/3G/5G/6G for different application
- Support 16-bit or 32-bit parallel interface when encode/decode enabled
- Support 20-bit parallel interface when encode/decode bypassed
- Support flexible reference clock frequency
- Support 100MHz differential reference clock input or output (optional with SSC) in PCIe Mode
- Support Spread-Spectrum clock (SSC) generation and receiving from -5000ppm to 0ppm
- Support programmable transmit amplitude and De-emphasis
- Support TX detect RX function in PCIE and USB3.0 Mode
- Support Beacon signal generation and detection in PCIE Mode
- Support Low Frequency Periodic Signaling (LFPS) generation and detection in USB3.0 Mode
- Support COMWAKE, COMINIT and COMRESET (OOB) generation and detection in SATA Mode
- Support L1 sub-state power management
- Support RX low latency mode in SATA operation mode
- Support Loopback BERT and Multiple Pattern BIST Mode

16.1.2 PCIe 3.0 PHY Overview

The PHY provides the following features:

- Standard PIPE 4 interface to upper layers of protocol stack (MAC layer and above)
- PCIe: 8b/10b (Gen 1/2) and 128b/130b (Gen3) encoding and decoding
- Translation of PIPE 4 power states (P0, P1, and so on) into the appropriate PHY controls, including any PHY-specific intermediate state sequencing
- Clock-rate compensation via SKP ordered sets and an elasticity buffer
- Each PCS lane can be independently configured to operate as follows:
  - PCIe (1.1, 2.1, and 3.0) modes
- PIPE4.3- or PIPE4.2-compliant PCIe 1.1, 2.1, or 3.0 controllers
  - Highly customizable physical medium attachment (PMA) configuration PCIe data rates: 2.5 Gbps (PCIe 1.1), 5 Gbps (PCIe 2.1), 8 Gbps (PCIe 3.0)
  - Single, dual and quad channel macros configurations lanes Extensive PMA debug capability through read/write and read-only registers in PCS
  - Register-based control of all PCS-to-PMA signals
  - Adaptive and configurable RX continuous time linear equalizer (CTLE) and decision feedback equalizer (DFE)
  - Programmable TX equalization
- PCIe 3.0 aggregation and bifurcation up to x4 PHY configuration
- Supports PCIe L1-substate power managements
- Built-in Self-Test (BIST) features for production; at-speed testing on any digital tester

- Advanced, built-in diagnostics including on-chip sampling scope
- Visibility and controllability of hard macro functions through programmable registers in the design:
  - Overrides on all ASIC side functional control inputs for easy debug
  - Access register space through a parallel interface
  - Access register space through a JTAG port
- Configurable PCS with extensive debug options:
  - Independent TX and RX control per lane
  - Configurable TX and RX power modes
  - Pseudo-random bit sequence (PRBS) generation and checker (PRBS31, PRBS23, PRBS16, PRBS15, PRBS11, PRBS9, PRBS7)
  - Programmable 10-bit pattern generation with error injection capability

16.2 Block Diagram

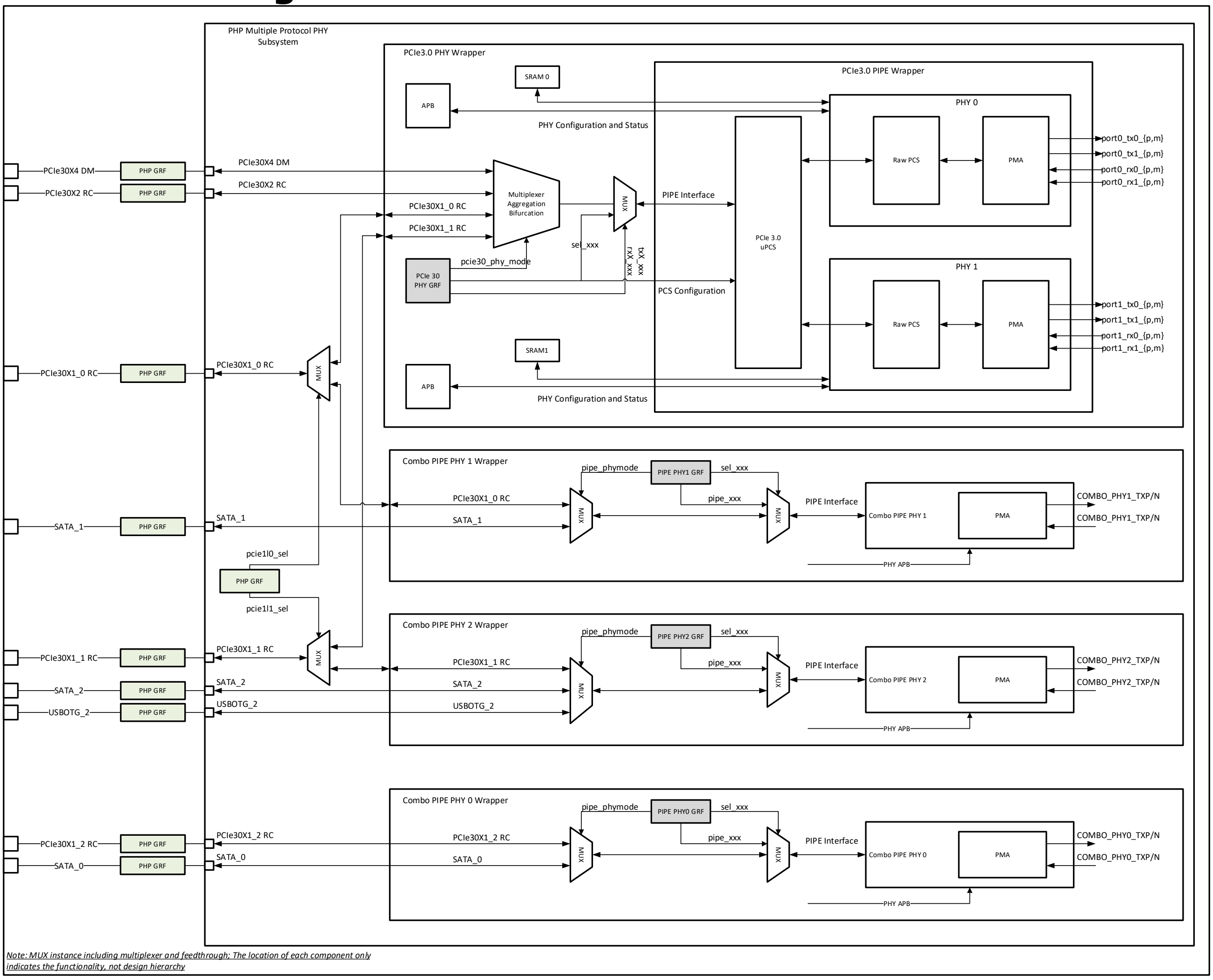

Fig. 16-1 Diagram of Multiple Protocol PHY Subsystem Architecture

There are three Combo protocol PHYs illustrated above. The pipe_phymode is used to select the target protocol controller. The PIPE PHYn GRF module is used to generate common control signals and override some PIPE interface signal in specific cases, PIPE interface bus is connected with the selected protocol controller by default. The PHY APB can config the PHY internal register to adjust the trims of CDR, PLL, etc. Please refer to PIPE PHY GRF and for detail description.

The PCIe 3.0 PHY is consist of two PHY Marco and interfacing with a X4 uPCS. PHY0 and PHY1 can be aggregated as one X4 Link, and both can be bifurcated into two X1 Link. Each PHY has individual PHY configuration and status space, the PCIe 30 PHY GRF is used to control the multiplexers and PCS configuration, it is also used override some PIPE interface signal in some specific scenarios. APB is in charge of accessing the internal control register and status of each PHY. Two external SRAM 0/1 are included for the purpose of updating the IP firmware, it can be updated by APB bus access. The aggregation and bifurcation of the PHYs are controlled by pcie30_phy_mode.

The multiplex function table is listed in section Subsystem Protocol Link Mapping.

16.2.1 Combo PHY Function Description

16.2.1.1 Block Diagram and Description

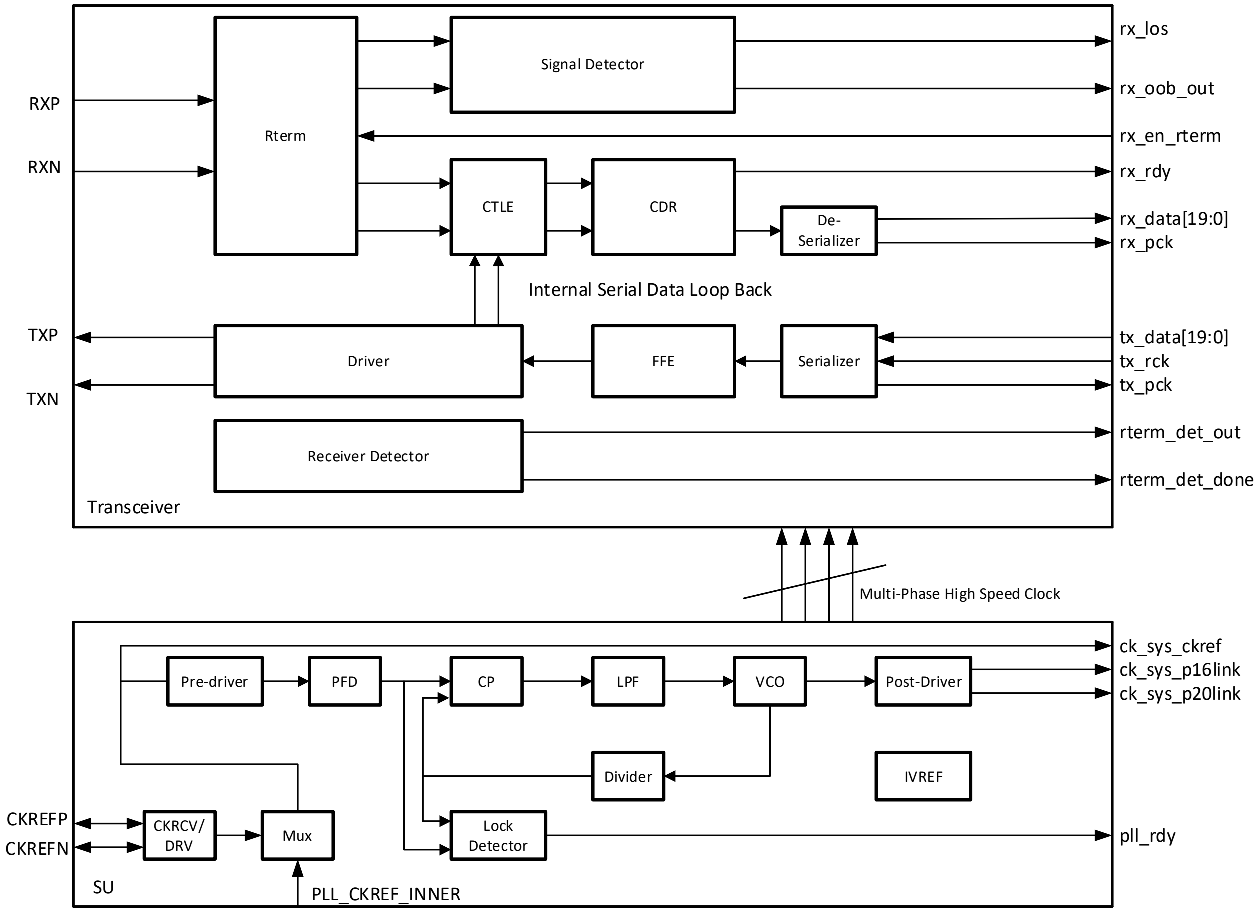

Fig. 16-2 PMA Block Diagram of Multi-PHY

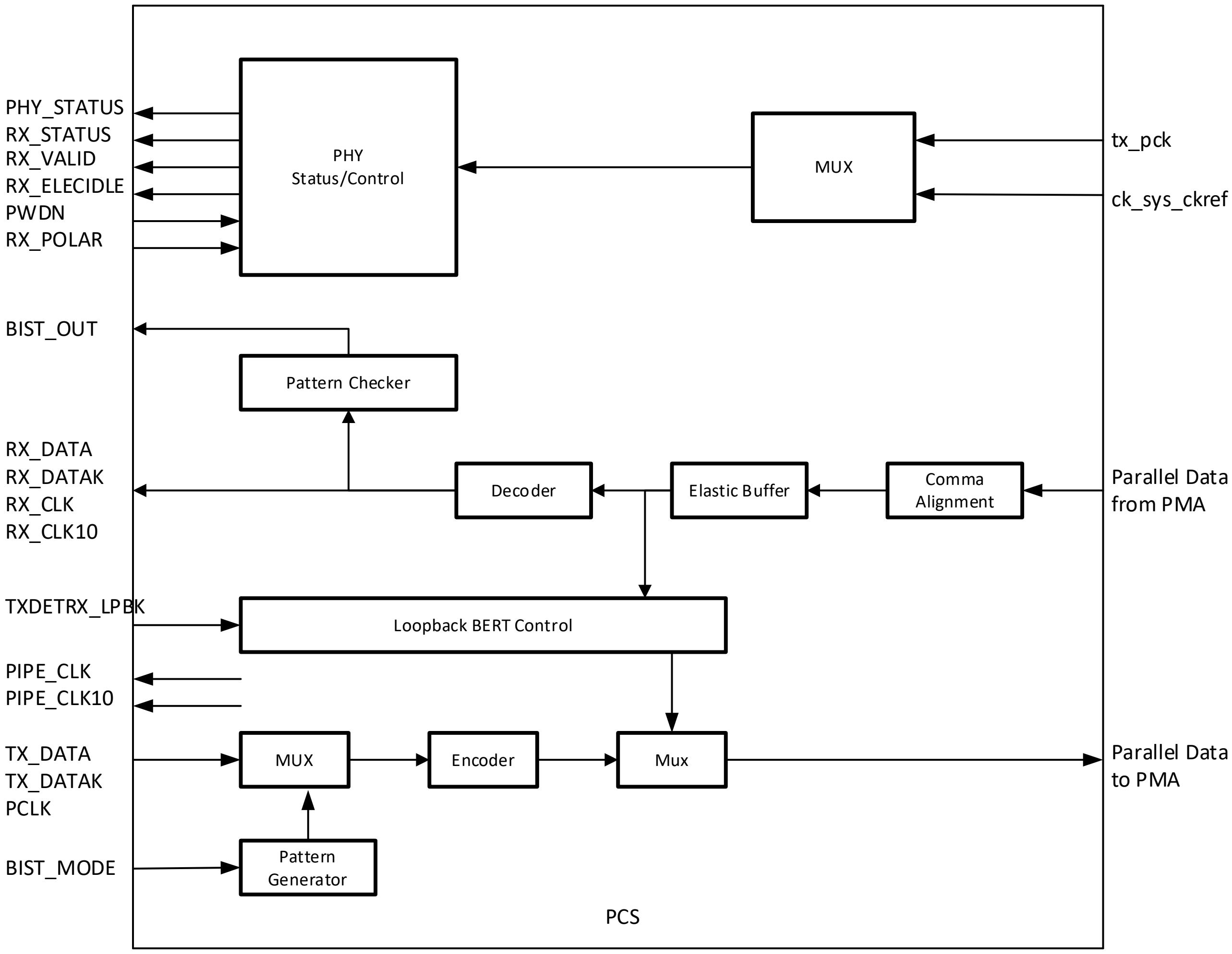

Fig. 16-3 PCS Block Diagram of Multi-PHY

Combo PIPE PHY includes two major blocks, PMA and PCS. PMA is an analog macro to perform serial to parallel and parallel to serial conversion. PMA includes three blocks, Transmitter, Receiver and SU(includes PLL, IVREF, etc.). PCS is a digital synthesis macro to perform PHY coding sub-layer function like 8bit/10bit code and decode, elastic buffer, comma alignment and BERT loopback, it also includes a register interface to access internal control registers with APB interface.

16.2.1.2 SHARED UNIT (SU)

PLL takes reference clock input from CKREFP/N and PLL_CKREF_INNER, to generate a high-speed clock for data transmission and clock data recovery. The high-speed clock generated by PLL could be SSC (spectrum spread clock) modulated if SSC mode is turned on. When SSC is enabled, the PHY is transmitting spread-spectrum serial data with frequency offset in 31.5KHz periodically.

IVREF includes a voltage and current reference generator, which comprises a Bandgap Reference and a Voltage Regulator. Reference voltage and current are generated for internal circuit usage. IVREF block is always on as long as IP power up, it will consume ~170uA static current all the time.

CKDRV is an input/output differential clock buffer, when it is used as input, it can receive a wide range differential reference clock. When used as output, CKDRV can drive a 100MHz differential clock for PCIE host application.

16.2.1.3 TRANSMITTER (TX)

The Serializer block converts parallel data from PHY PCS to high-speed serial data by using high speed clock generated by PLL. A feed forward equalizer (FFE) is implemented to compensate channel ISI.

Driver will convert the serial data to differential signal on TXP/TXM, also the driver will transmit Beacon Signal (PCIE2.0), OOB(SATA) or LFPS(USB3.0) signaling. The differential output amplitude and Deemphasis level can be programmed via setting PIPE3 control pins TX_SWING, TX_DEEMPH[2:0] and TX_MARGIN[2:0].

The receiver detector will be used to detect the far-end receiver present or not.

16.2.1.4 RECEIVER (RX)

The CTLE (Continuous Time Linear Equalizer) is used to compensate channel loss and cancel ISI of the input signals by boosting high frequency gain. The CTLE can be set to adaptive mode or manual setting mode.

The CDR (Clock and Data Recover) tracks input data stream and generate recovered clock for data de-serializer. De-Serializer converts incoming serial bit stream recovered by CDR into a synchronized parallel data bus and forward it to PHY PCS block.

The Signal Detector detects OOB/LFPS on the RX input pair.

16.2.1.5 PCS

PCS module is a pure digital synthesis module, it works as an interface between PMA and MAC, it accomplishes functions including comma alignment, 8bit/10bit code/decode, elastic buffer, power control and IP testing. This module also includes an APB interface for accessing PHY control registers. PCS is fully compatible with the PIPE3 interface of “PHY interface for PCI express and USB3.0 architecture by intel”.

16.2.2 PCIe 3.0 PHY Function Description

16.2.2.1 uPCS Transmit and Receive Datapath

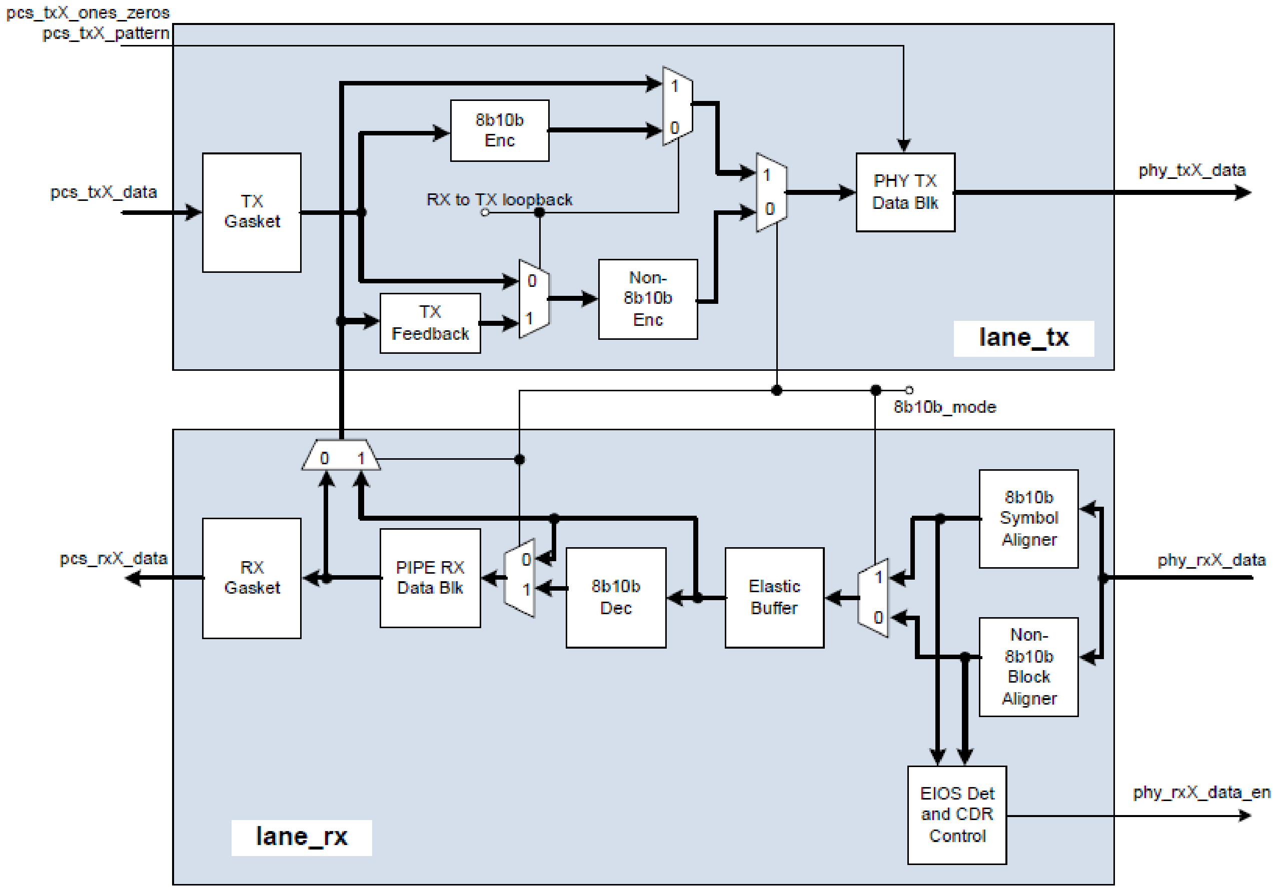

Fig. 16-4 Transmit and Receive Datapath

The pcs_txX_data transmit data and controls are converted from the PIPE interface clock to the internal pcs_clk in the TX gasket. The fixed data-path-width data at the output of the TX gasket is encoded as follows:

- 8b10b-encoded for 8b10b protocols
- 128b-130b-encoded for PCIe Gen3

To support RX-to-TX loopback mode as specified in the PIPE specification, the RX recovered data is multiplexed into the TX Datapath. Note that for 8b10b mode, the non-decoded 8b10b received data is sent to the transmitter. For non-8b10b data, the received data is decoded first; that is, the header is extracted from the data, then looped back into the TX Datapath, where it is encoded before being transmitted to the PHY. The encoded TX data goes through override logic where fixed patterns are inserted into the TX data-stream controller by the pcs_txX_ones_zeros and pcs_txX_pattern[1:0] PIPE signals.

Data received from the PHY is processed to find symbol alignment for 8b10b data and block alignment for non-8b10b data. The aligned data is monitored for EIOS ordered sets (PCIe) to detect end-of-packets and to infer entry into electrical idle condition. After detecting EIOSs, the Consumer PCIe 3.0 PCS de-asserts phy_rxX_data_en to the PHY lane, causing the lane CDR to stop monitoring input data transitions and to switch to reference clock tracking mode. The aligned data is passed to the elastic buffer, where compensation for frequency drift is performed by adding or removing SKP (PCIe) ordered sets. The frequency-compensated data is 8b10b-decoded for 8b10b data, then passed through the PIPE RX processing block where data and status signals are cycle-aligned. The RX data and status signals pass through the RX gasket that maps the internal fixed-width data to variable interface widths supported by the PIPE interface.

16.2.2.2 Physical Medium Attachment (PMA)

Each PMA comprises a full duplex transceiver for each lane. On the transmit (TX) side, the PMA receives parallel data from the relevant lane of the PCS. The data is serialized and sent to the TX driver, which is a high-speed, hybrid-mode (voltage and current), differential-output driver. TX driver characteristics, such as amplitude, 3-tap feed-forward equalization, and termination, are user controllable. The TX driver output is sent to a pair of external pads.

On the receive (RX) side, the PMA receives differential serial data from a pair of external pads. Receiver characteristics, such as equalization and termination, are user controllable. A continuous-time linear equalizer (CTLE) is first used to compensate for channel loss. A decision feedback equalizer (DFE) is also implemented after the CTLE to further equalize the signal for high-speed data rates. A clock and data recovery (CDR) circuit is implemented, which recovers the clock from the data. A dedicated VCO is implemented as the source of the recovering clock. The CDR loop adjusts the VCO clock frequency and phase until the frequency matches incoming data and the phase is aligned with incoming data. This recovered clock is used to retime received data and send it to the de-serializer, which produces parallel data and a parallel data clock for the relevant PCS lane.

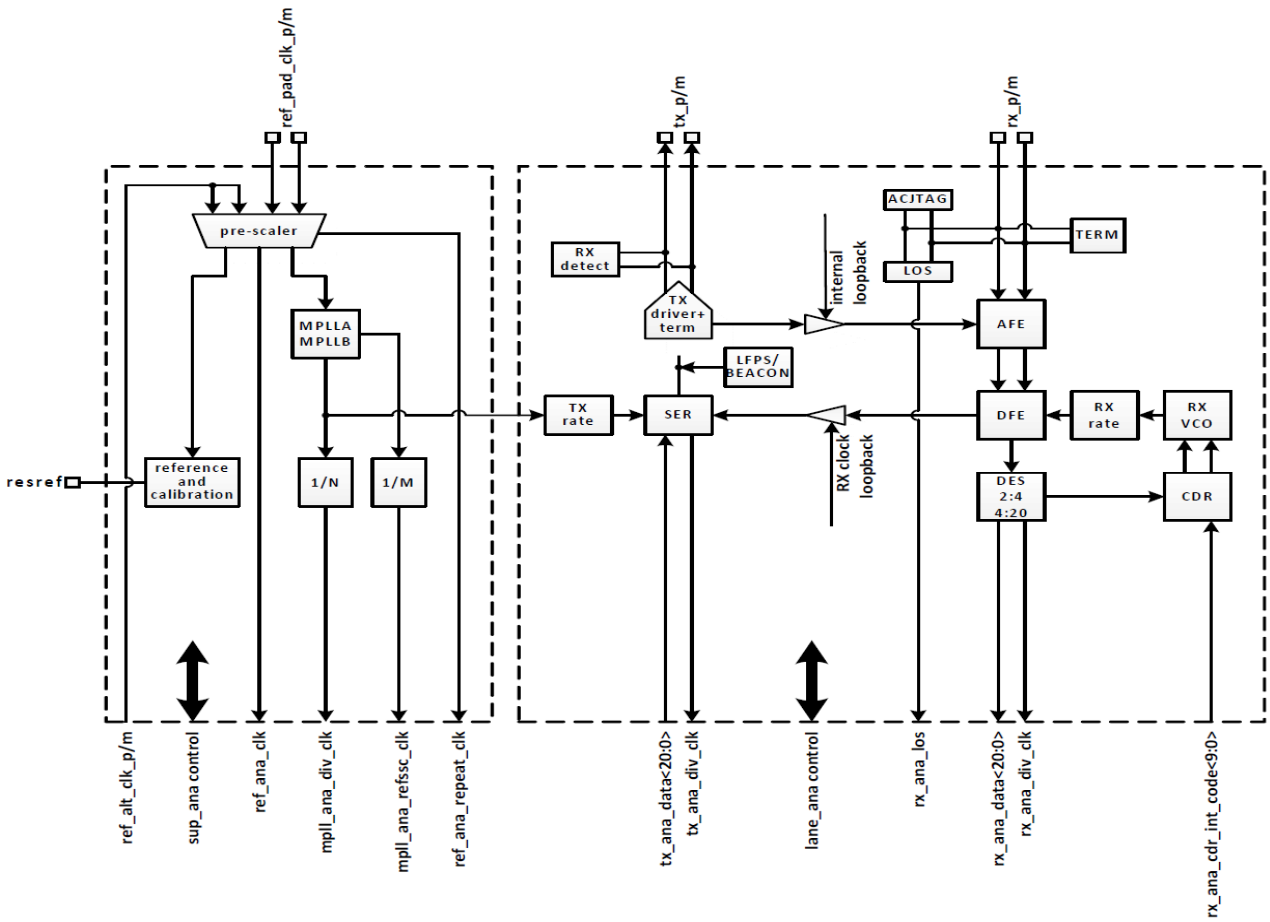

Fig. 16-5 PMA Analog Architecture(Single Lane)

16.2.2.3 Raw PCS

The PMA PCS features listed below:

- Power-up calibration algorithms for the PMA analog front-end, for example, RX AFE

offset cancellation, RX slicer calibration, MPLL calibrations, and RX VCO calibrations
- Controls for the adaptation routines in the PMA for modes when adaptation is enabled
- MPLL power-up and power-down control based upon txX_pstate and txX_mpllb_sel inputs
- JTAG Tap controller for serial register access
- Register access arbitration between JTAG/CR Parallel access, and the internal power-up and adaptation routines

The selection between JTAG and CR Parallel interfaces is controlled using primary input cr_para_sel, which means that both of these interfaces cannot operate simultaneously. A round-robin arbitration mechanism exists to provide equal priority to different sources requesting access to the shared internal register bus. These sources include multiple internal state machines as well as external register access interfaces (JTAG/CR-Parallel).

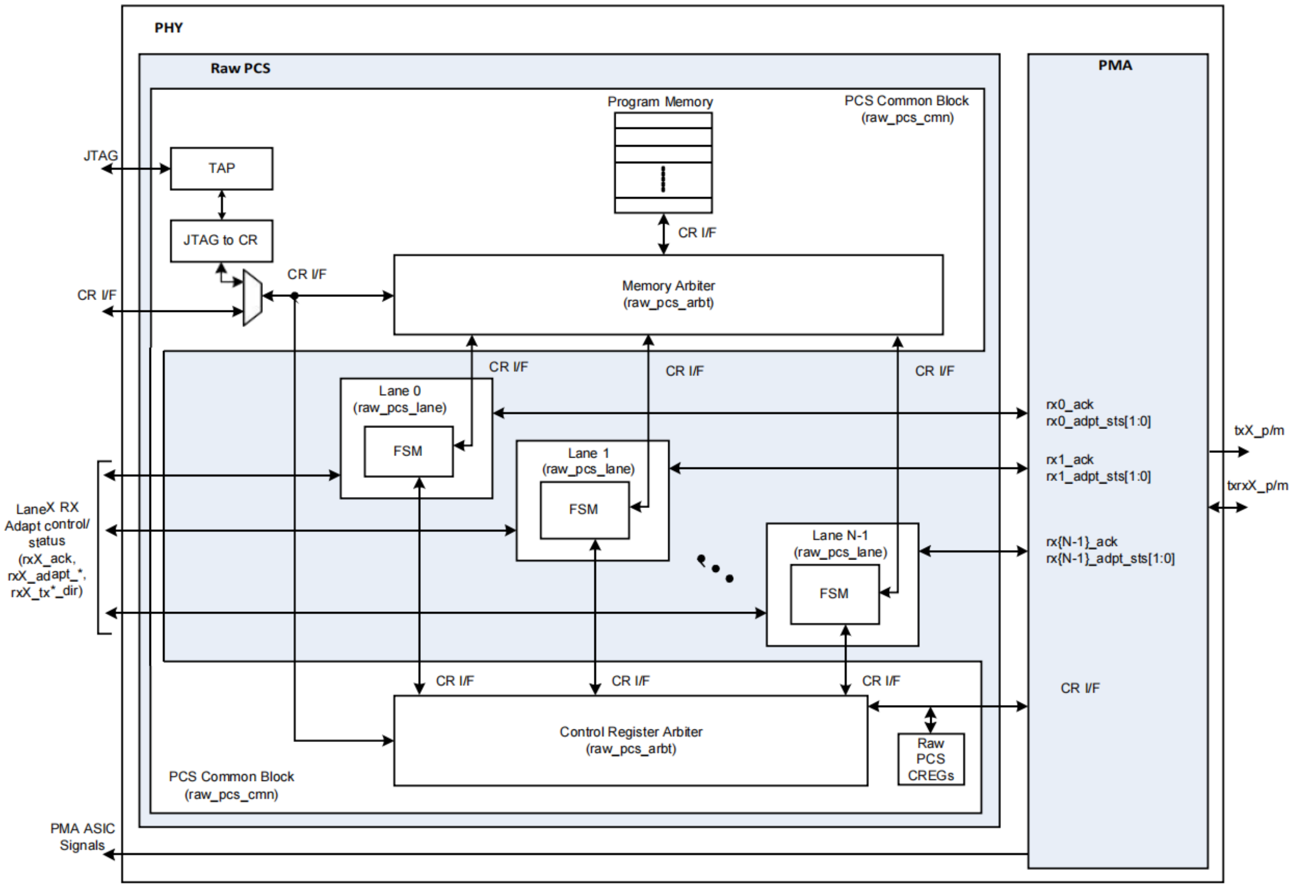

Fig. 16-6 PMA Analog Architecture(Single Lane)

Each lane module (raw_pcs_lane) contains finite state machines (FSMs) to execute the power-up calibration and run-time adaptation algorithms. The algorithms are stored in a register bank located in a common module (raw_pcs_cmn). The design includes two register access arbiters. The Memory arbiter is used for accessing the register bank whereas the Control Register Arbiter is used to access all other registers in the PMA PCS and the PMA. This mechanism provides efficient use of the registers and state machines within each lane where each lane can independently execute a different portion of the algorithm while reducing the register access bottleneck.

All control registers in the PMA PCS and PMA can be externally accessed using JTAG or CR Parallel Interfaces, with only one interface at any given time.

16.3 Register Description

16.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 16-1 Combo PHY Address Mapping Table

Name	Address Base	Size
Combo PIPE PHY0	0xFEE00000	0x10000(64KB)
Combo PIPE PHY1	0xFEE10000	0x10000(64KB)
Combo PIPE PHY2	0xFEE20000	0x10000(64KB)
Combo PIPE PHY0 GRF	0xFD5BC000	0x4000(16KB)
Combo PIPE PHY1 GRF	0xFD5C0000	0x4000(16KB)
Combo PIPE PHY2 GRF	0xFD5C4000	0x4000(16KB)

Table 16-2 PCIe 3.0 PHY Address Mapping Table

Name	Address Base	Size
PCIe 3.0 PHY 0	0xFEE80000	0x40000(256KB)
PCIe 3.0 PHY 1	0xFEEC0000	0x40000(256KB)
PCIe 3.0 PHY GRF	0xFD5B8000	0x4000(16KB)

Note: The offset of the each PCIe 3.0 PHY's SRAM begins at 0x18000(Base 0xFEE80000/0xFEEC0000), ends up at 0x1BFFC.

16.3.2 Combo PIPE PHY Registers Summary

Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_000	0x0000	W	0x00000000	Combo PHY Register 0
COMBO_PIPE_PHY_REG_001	0x0004	W	0x00000080	Combo PHY Register 1
COMBO_PIPE_PHY_REG_002	0x0008	W	0x000000FF	Combo PHY Register 2
COMBO_PIPE_PHY_REG_003	0x000C	W	0x00000000	Combo PHY Register 3
COMBO_PIPE_PHY_REG_004	0x0010	W	0x00000000	Combo PHY Register 4
COMBO_PIPE_PHY_REG_005	0x0014	W	0x00000000	Combo PHY Register 5
COMBO_PIPE_PHY_REG_006	0x0018	W	0x00000088	Combo PHY Register 6
COMBO_PIPE_PHY_REG_007	0x001C	W	0x00000008	Combo PHY Register 7
COMBO_PIPE_PHY_REG_008	0x0020	W	0x00000060	Combo PHY Register 8
COMBO_PIPE_PHY_REG_009	0x0024	W	0x00000009	Combo PHY Register 9
COMBO_PIPE_PHY_REG_010	0x0028	W	0x00000093	Combo PHY Register 10
COMBO_PIPE_PHY_REG_011	0x002C	W	0x00000002	Combo PHY Register 11
COMBO_PIPE_PHY_REG_012	0x0030	W	0x00000008	Combo PHY Register 12
COMBO_PIPE_PHY_REG_013	0x0034	W	0x00000059	Combo PHY Register 13

Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_014	0x0038	W	0x00000040	Combo PHY Register 14
COMBO_PIPE_PHY_REG_015	0x003C	W	0x00000063	Combo PHY Register 15
COMBO_PIPE_PHY_REG_016	0x0040	W	0x00000000	Combo PHY Register 16
COMBO_PIPE_PHY_REG_017	0x0044	W	0x00000032	Combo PHY Register 17
COMBO_PIPE_PHY_REG_018	0x0048	W	0x0000009B	Combo PHY Register 18
COMBO_PIPE_PHY_REG_019	0x004C	W	0x00000047	Combo PHY Register 19
COMBO_PIPE_PHY_REG_020	0x0050	W	0x0000000B	Combo PHY Register 20
COMBO_PIPE_PHY_REG_021	0x0054	W	0x00000041	Combo PHY Register 21
COMBO_PIPE_PHY_REG_022	0x0058	W	0x0000002C	Combo PHY Register 22
COMBO_PIPE_PHY_REG_023	0x005C	W	0x00000030	Combo PHY Register 23
COMBO_PIPE_PHY_REG_024	0x0060	W	0x00000000	Combo PHY Register 24
COMBO_PIPE_PHY_REG_025	0x0064	W	0x00000000	Combo PHY Register 25
COMBO_PIPE_PHY_REG_026	0x0068	W	0x00000014	Combo PHY Register 26
COMBO_PIPE_PHY_REG_027	0x006C	W	0x00000000	Combo PHY Register 27
COMBO_PIPE_PHY_REG_028	0x0070	W	0x00000005	Combo PHY Register 28
COMBO_PIPE_PHY_REG_029	0x0074	W	0x00000040	Combo PHY Register 29
COMBO_PIPE_PHY_REG_030	0x0078	W	0x00000000	Combo PHY Register 30
COMBO_PIPE_PHY_REG_031	0x007C	W	0x00000010	Combo PHY Register 31
COMBO_PIPE_PHY_REG_032	0x0080	W	0x00000000	Combo PHY Register 32
COMBO_PIPE_PHY_REG_033	0x0084	W	0x00000000	Combo PHY Register 33
COMBO_PIPE_PHY_REG_034	0x0088	W	0x00000000	Combo PHY Register 34
COMBO_PIPE_PHY_REG_035	0x008C	W	0x00000000	Combo PHY Register 35
COMBO_PIPE_PHY_REG_036	0x0090	W	0x00000000	Combo PHY Register 36
COMBO_PIPE_PHY_REG_037	0x0094	W	0x00000000	Combo PHY Register 37
COMBO_PIPE_PHY_REG_038	0x0098	W	0x00000000	Combo PHY Register 38
COMBO_PIPE_PHY_REG_039	0x009C	W	0x00000000	Combo PHY Register 39

Name	Offset	Size	Reset Value	Description
COMBO_PIPE_PHY_REG_040	0x00A0	W	0x00000000	Combo PHY Register 40
COMBO_PIPE_PHY_REG_041	0x00A4	W	0x00000000	Combo PHY Register 41
COMBO_PIPE_PHY_REG_042	0x00A8	W	0x00000000	Combo PHY Register 42
COMBO_PIPE_PHY_REG_043	0x00AC	W	0x00000000	Combo PHY Register 43
COMBO_PIPE_PHY_REG_044	0x00B0	W	0x00000000	Combo PHY Register 44
COMBO_PIPE_PHY_REG_045	0x00B4	W	0x00000000	Combo PHY Register 45
COMBO_PIPE_PHY_REG_046	0x00B8	W	0x00000000	Combo PHY Register 46
COMBO_PIPE_PHY_REG_047	0x00BC	W	0x00000000	Combo PHY Register 47
COMBO_PIPE_PHY_REG_048	0x00C0	W	0x00000000	Combo PHY Register 48
COMBO_PIPE_PHY_REG_049	0x00C4	W	0x00000000	Combo PHY Register 49

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

16.3.3 Combo PIPE PHY Detail Registers Description

COMBO_PIPE_PHY_REG_000

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	clk_out_sel Select which internal clock connect to output test_clk 1'b0: TXPLL clock/4 1'b1: RXCDR clock/4
6	RW	0x0	inv_txpll_clk 1'b1: Invert the PLL clock from PHY to PCS in PCS
5	RW	0x0	inv_rxcdr_clk 1'b1: Invert the CDR clock from PHY to PCS in PCS
4:0	RO	0x00	reserved

COMBO_PIPE_PHY_REG_001

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x2	pwdn_ctrl_l [0]: If 1, PHY block power controlled by pwon** signals instead of PIPE signals [1]: Enable IVREF in PMA when pwdn_ctrl[0]=1
5:1	RO	0x00	reserved
0	RW	0x0	custom_specific Used to select which of operation2 or operation3 L1 SSTM the PHY interface would act as

COMBO_PIPE_PHY_REG_002

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xff	pwdn_ctrl_h [2]: Enable PWON_TX_BUF to power on TX driver in PMA pwdn_ctrl[0]=1 [3]: Enable PWON_TXPLL to power on PLL in PMA pwdn_ctrl[0]=1 [4]: Enable PWON_IDLE_DET to power on PCIE EIDLE detect driver in PMA pwdn_ctrl[0]=1 [5]: Enable PWON_LFPS_DET to power on USB LFPS detect in PMA pwdn_ctr[0]=1 [6]: Enable PWON_RX_BUF to power on RX CTLE in PMA pwdn_ctrl[0]=1 [7]: Enable PWON_CDR to power on RX CDR in PMA pwdn_ctrl[0]=1 [8]: Enable PWON_OOB_DET to power on SATA OOB detect in PMA pwdn_ctr[0]=1 [9]: Enable PWON_HS_DET to power on SATA high speed data detect in PMA pwdn_ctrl[0]=1

COMBO_PIPE_PHY_REG_003

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	rx_rterm_vcom RX vcom voltage select signal 2'b00: GND 2'b01, 2'b10: Floating 2'b11: 320mV
5:3	RW	0x0	tx_rate bit[2]: PMA tx_rate source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: tx_rate control
2:0	RW	0x0	rx_rate bit[2]: PMA rx_rate source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: rx_rate control

COMBO_PIPE_PHY_REG_004

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RO	0x0	bist_mode IP bist mode control
2:0	RO	0x0	reserved

COMBO_PIPE_PHY_REG_005

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pll_ckref_div PLL input clock divider, valid when su_trim[14]=1 2'b00: 1 2'b01: 1/2 2'b10: 1/3 2'b11: 1/4

Bit	Attr	Reset Value	Description
5:3	RW	0x0	rate bit[2]: PMA PLL rate source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: PLL rate control
2:0	RW	0x0	phy_mode bit[2]: PMA phy_mode source selects. 1'b0: Source from PIPE 1'b1: Source from APB bit[1:0]: Phy model control.

COMBO_PIPE_PHY_REG_006
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x8	tx_rterm TX output resister adjust signal by step about 1ohm 4'h0: 60 4'h8: 50 4'hf: 44 Others: Reserved
3:0	RW	0x8	rx_rterm RX input resister adjust signal by step about 1ohm 4'h0: 60 4'h8: 50 4'hf: 43.5 Others: Reserved

COMBO_PIPE_PHY_REG_007
Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	byps_cdr_en 1'b0: CDR recovered clock will be operation while PLL is locked and CDR is operation, and rx_cdr_trim[7] only can be set to 1'b0 using reference clock for rx_rdy generation. 1'b1: CDR recovered clock will be operation while PLL is locked, and rx_cdr_trim[7] can be set to 1'b1 using recovered clock for rx_rdy generation.
6	RW	0x0	tx_swing Tx_swing control.
5	RW	0x0	near_end_lpk_enable PHY Near end loop back enable in BIST mode.
4	RW	0x0	ssc_en In U3 and SATA mode, this bit= 1, set SSC on. In PCIE mode, this bit=0 set SSC off.
3:0	RW	0x8	tx_swing_com TX boost level adjust signal 3'b000: Minimum 3'b111: Maximum

COMBO_PIPE_PHY_REG_008
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	byps_cdr_fl_en 1'b0: rx_rdy is pulse signal to indicate CDR start to clock and data recovered from input serial data. 1'b1: rx_rdy is not controlled by PMA/PCS interface signal "cdr_fl_en".
6	RW	0x1	byps_cpath_limit 1'b0: CDR CPATH will be reset while CDR CPATH is overflow. 1'b1: CDR CPATH will be locked to MAX frequency offset while CDR CPATH is overflow.
5	RW	0x1	byps_capth_overflow 1'b0: CDR CPATH is controlled by CDR CPATH overflow. 1'b1: CDR CPATH is not controlled by CDR CPATH overflow.
4	RW	0x0	byps_fgain_adpt 1'b0: CDR CPATH gain is X2 while CDR recover frequency while rx_cdr_trim[6]=0. 1'b1: CDR CPATH gain is X1 while CDR recover frequency while rx_cdr_trim[6]=0.
3	RW	0x0	byps_pwon_rx_buf 1'b0: CTLE and LOS detector is controlled by PWDN[1:0]. 1'b1: CTLE and LOS detector is operation while reference clock and RX termination is present.
2	RW	0x0	byps_pown_rx_cdr 1'b0: CDR is controlled by PWDN[1:0]. 1'b1: CDR is operation after PLL is locked while reference clock and RX termination is present.
1	RW	0x0	byps_pwon_tx_buf 1'b0: TX Driver is controlled by PWDN[1:0]. 1'b1: TX Driver is operation after PLL is locked while reference clock is present, and TX detect RX is finished.
0	RW	0x0	byps_resetn 1'b0: PMA is reset by RSTN. 1'b1: PMA is not controlled by RSTN.

COMBO_PIPE_PHY_REG_009

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	byps_rterm_en 1'b0: RX termination is controlled by RTERM_EN. 1'b1: RX termination is present all the way.
6	RW	0x0	byps_rx_cdr_idle 1'b0: CDR is reset if EIDLE is detected by LOS Detect module. 1'b1: CDR is not controlled by LOS Detect module.
5	RW	0x0	byps_rx_rdy_pulse 1'b0: rx_rdy is pulse signal. 1'b1: rx_rdy is step signal while byps_cdr_fl_en=1.
4	RW	0x0	byps_tx_eidle_en 1'b0: TX EIDLE is controlled by PMA/PCS interface signal "tx_eidle_en" (SATA Mode) or "tx_lfps_beacon_en"(PCIE/USB Mode). 1'b1: TX EIDLE is disable.

Bit	Attr	Reset Value	Description
3:0	RW	0x9	ssc_ppm PLL SCC ppm adjust signal by step 500ppm. 4'h0: 0ppm 4'h1: 500ppm 4'h8: 4000ppm 4'hf: 7500ppm

COMBO_PIPE_PHY_REG_010

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x93	su_trim_bank0 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_011

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x02	su_trim_bank1 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_012

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x08	su_trim_bank2 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_013

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x59	su_trim_bank3 SU adjust signal [2:0]: PLL KVCO adjust 3'b000: Min 3'b111: Max [3]: PLL force lock [24:23], [6:4]: PLL charge pump current adjusts 5'b00000: Min 5'b11111: Max [10:7]: PLL LPF R1 adjust 3'b000: Max 3'b111: Min [11]: bypass PLL power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [21:20]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [22]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid, CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, step:50 mV 4'h0: 100 mV ..... 4'hf: 860 mV [29]: CKDRV input clock select signal, 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [31:30]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow

COMBO_PIPE_PHY_REG_014

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x1	ssc_cnt_l PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, This signal should be set to its default value unless the user want to change the 31.5KHz SSC modulation frequency. When the pll_ckref_inner is 24MHz, this signal should be set to its default value unless the user want to change the 32.8KHz SSC modulation frequency.
5:2	RW	0x0	test_sel select the digital test signal. 4'h0: Input Reference Clock 4'h1: PLL Loopback Clock 4'h2: PLL Locked 4'h3: RX PCL enable 4'h4: RX CDR enable 4'h5: RX CTLE enable 4'h6: CDR overflow 4'h7: RX ready 4'h8: RX LFPS idle detect 4'h9: RX PCIE idle detect 4'ha: RX SATA idle detect 4'hb: RX super speed detect 4'hc: Iddq_en 4'hd: Rterm detect Others: Reserved
1	RW	0x0	rx_tseq USB Mode When asserted, it is used to instruct USB3.0 PHY to bypass normal operation and do a receiver equalization training. Please refer to PIPE3 interface and USB3.0 base spec for more detail information.
0	RW	0x0	en_adpt Adaptive Continuous Time Linear Equalizer (CTLE) enable signal 1'b0: Disable adaptive CTLE 1'b1: Enable adaptive CTLE

COMBO_PIPE_PHY_REG_015

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x63	ssc_cnt_h PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, This signal should be set to its default value unless the user want to change the 31.5KHz SSC modulation frequency. When the pll_ckref_inner is 24MHz, this signal should be set to its default value unless the user want to change the 32.8KHz SSC modulation frequency.

COMBO_PIPE_PHY_REG_016

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	pll_div_l PLL loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction.

COMBO_PIPE_PHY_REG_017
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	frez_apt_eq 1'b0: The adaptive equalizer will be always working when the adaptive equalizer function is enabled. 1'b1: The adaptive equalizer will freeze at its final result when equalizer training pattern transmission is done. This signal is used in USB3.1 mode, when equalizer training pattern transmission is done, IP user can stop adaptive equalization and freeze the result.
6:0	RW	0x32	pll_div_h PLL loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction.

COMBO_PIPE_PHY_REG_018
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	cdr_valid_sel cdr data valid counter delay in pcs select.
5:3	RW	0x0	rx_afe_trim Receiver 2nd stage equalizer res control, used to adjust pole-zero of RX eq.
2:0	RW	0x3	rx_afe_ctrim Receiver 1st stage equalizer cap control, used to adjust pole-zero of RX EQ.

COMBO_PIPE_PHY_REG_019
Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	com_det_once Disable Look for the comma location multiple times 1'b0: 5 times 1'b1: 2 times
6	RW	0x1	sata_vlaid_sel SATA mode rx_valid source selects
5	RW	0x0	beacon_timeout_sel PCIe beacon timeout select
4	RW	0x0	rx_polar RX output polarity set 1'b0: No invert RX output data polarity 1'b1: Invert RX output data polarity
3:0	RW	0x7	rx_afe_rtrim Receiver 1st stage equalizer res control, used to adjust pole-zero of RX eq.

COMBO_PIPE_PHY_REG_020
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x0B	rx_sqdet_trim_l RX squelch adjust [2:0]: squelch input filler bandwidth adjusts 3'b000: Max bandwidth 3'b111: Min bandwidth [4:3]: squelch delay adjusts 2'b00: Max delay 2'b11: Min delay [6:5]: amp bias adjusts 2'b00: Max ibias 2'b11: Min ibias [8:7]: squelch detect vth adjust 2'b00: Min vth 2'b11: Max vth

COMBO_PIPE_PHY_REG_021
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	rx_adpt_eq_trim [2:0]: adaptive equalizer detection threshold control [3]: adaptive equalizer gain control
3:0	RW	0x1	rx_sqdet_trim_h [9]: bypass rx_superspeed 1'b1: rx_superspeed=1 [10]: rx_superspeed function selects 1'b0: ~los output 1'b1: ~los output | squelch output [11]: rx_pcie_idle function selects 1'b0: ~ squelch output 1'b1: los output

COMBO_PIPE_PHY_REG_022
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	rx_adpt_eq_trim_h [6:4]: adaptive equalizer bandwidth control [8:7]: adaptive output refresh bandwidth control [9]: bypass the adaptive Cj function [10]: test mode selects [11]: Reserved

COMBO_PIPE_PHY_REG_023
Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x3	rx_cdr_trim_l [3]: CDR gain adjust 1'b0: 1/4([4]=1), 1/8([4]=0) 1'b1: 1/8 [2:0]: The slew rate control for PI 3'b000: Fast slew rate 3'b111: Slow slew rate
3:0	RW	0x0	rx_los_trim RX los detect adjust [1:0]: Low vth adjust [2]: Reserved [3]: Enable signal of Los eidle reseting CDR or not 1'b0: Los eidle not reset CDR 1'b1: Los eidle reset CDR

COMBO_PIPE_PHY_REG_024

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	rx_cdr_trim_h [4]: CDR gain adjust 1'b0: 1/8 1'b1: 1/4 when rx_cdr_trim[3]=1 [5]: CDR phase path gain adjust 1'b0: x1 1'b1: x2 [6]: CDR cpath bandwidth gain adjusts 1'b0: Low bandwidth 1'b1: High bandwidth [7]: rx_rdy counter clock select 1'b0: Ref clock 1'b1: CDR recovery clock [9:8]: rx_rdy delay time select 2'b00: 1.28us 2'b01: 0.64us 2'b10: 2.56us 2'b11: 5.12us [11:10]: Reserved

COMBO_PIPE_PHY_REG_025

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	tx_trim_l TX adjust [3:0]: TX FFE adjust valid when tx_trim[4]=1 [4]: Manual mode enable [5]: Force rterm detect ready 1'b1: Force rtern_det_out=1 [6]: Force eidle 1'b1: txp/txm is eidle [7]: hi-z idle enable [8]: tx_pck invert enable [9]: MSB enable [10]: Bypass low resister eidle mode 1'b0: Eidle has not hi-z mode 1'b1: Eidle has hi-z mode [11]: Bypass 0.6kohm charge resister 1'b0: 0.6kohm resister 1'b1: 1kohm resister [13:12]: Rterm detect vth adjust 2'b00: Max vth 2'b11: Min vth [14]: Bypass signal of gate_tx_pck

COMBO_PIPE_PHY_REG_026

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x14	tx_trim_h TX adjust [3:0]: TX FFE adjust valid when tx_trim[4]=1 [4]: Manual mode enable [5]: Force rterm detect ready 1'b1: Force rtern_det_out=1 [6]: Force eidle 1'b1: txp/txm is eidle [7]: hi-z idle enable [8]: tx_pck invert enable [9]: MSB enable [10]: Bypass low resister eidle mode 1'b0: Eidle has not hi-z mode 1'b1: Eidle has hi-z mode [11]: Bypass 0.6kohm charge resister 1'b0: 0.6kohm resister 1'b1: 1kohm resister [13:12]: Rterm detect vth adjust 2'b00: Max vth 2'b11: Min vth [14]: Bypass signal of gate_tx_pck

COMBO_PIPE_PHY_REG_027

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	rx_trim [0]: rx_pck invert enable [1]: RX MSB enable [3:2]: PLL LPF C1 adjust signal 2'b00: 20pf 2'b01: 40pf 2;b10: 65pf 2'b11: 85pf [5:4]: PLL loop's divider factor(pre-divider) adjust signal 2'b00, 2'b01: 1 2'b10: 2 2'b11: 4 [6]: PLL LPF R1 fine-adjust signal 1'b0: Disable(2.5kohm by step) 1'b1: Enable(1.25kohm by step) [7]: Reserved

COMBO_PIPE_PHY_REG_028

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	tx_margin Tx margin control
4:0	RW	0x05	rterm_det_trim [1:0]: rterm detect pre-charge time adjust 2'b00: 512us 2'b11: 4096us [3:2]: rterm detect post-charge time adjust 2'b00: 8us 2'b11: 64us [4]: Reserved

COMBO_PIPE_PHY_REG_029

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	unused_name1_bank0 Bit[3]: gate_tx_pck_sel length select Bit[2]: Reserved Bit[1]: Bypass idle det in PCIe P1.1 and P1.2 Bit[0]: SATA align detect logic output select
3	RW	0x0	bist_out_sel Reserved
2:0	RW	0x0	tx_deemph Tx_deemph control

COMBO_PIPE_PHY_REG_030

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	testo_sel pcs internal signal to testo io select

COMBO_PIPE_PHY_REG_031

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	register_bank0 [0]: bypass the mode of pd_ck100m controlling CKDRV 1'b0: CKDRV is on only in PCIE mode 1'b1: CKDRV is controlled by ckref_src[1:0] [2:1]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow [3]: 50ohm termination disable signal in CKREP/N TX mode 1'b0: Not disable 1'b1: Disable mode [5:4]: Select signal of SSC direction 2'b00: Up spread spectrum 2'b01: Down spread spectrum 2'b10: Illegal 2'b11: Intermediate spread spectrum [7:6]: SSC offset compensation 2'b00: 0ppm 2'b01: +500ppm 2'b10, 2'b11: -500ppm [8]: pll_rdy delay control when rate change 1'b0: Delay 3*TX_PCK relative to the falling edge of gate_tx_pck 1'b1: Delay about 20us relative to the falling edge of gate_tx_pck [9]: Select pll_lock to TX/RX 1'b0: pll_lock_txrx is same to pll_lock_pcs 1'b1: pll_lock_txrx is not controled by gate_tx_pck [12:10]: PLL KVCO fine tuning signals [13]: PLL control SSC module period [15:14]: Reserved

COMBO_PIPE_PHY_REG_032

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	register_bank1 [0]: bypass the mode of pd_ck100m controlling CKDRV 1'b0: CKDRV is on only in PCIE mode 1'b1: CKDRV is controlled by ckref_src[1:0] [2:1]: CKDRV output slew rate adjusts 2'b00: Fast 2'b11: Slow [3]: 50ohm termination disable signal in CKREP/N TX mode 1'b0: Not disable 1'b1: Disable mode [5:4]: Select signal of SSC direction 2'b00: Up spread spectrum 2'b01: Down spread spectrum 2'b10: Illegal 2'b11: Intermediate spread spectrum [7:6]: SSC offset compensation 2'b00: 0ppm 2'b01: +500ppm 2'b10, 2'b11: -500ppm [8]: pll_rdy delay control when rate change 1'b0: Delay 3*TX_PCK relative to the falling edge of gate_tx_pck 1'b1: Delay about 20us relative to the falling edge of gate_tx_pck [9]: Select pll_lock to TX/RX 1'b0: pll_lock_txrx is same to pll_lock_pcs 1'b1: pll_lock_txrx is not controled by gate_tx_pck [12:10]: PLL KVCO fine tuning signals [13]: PLL control SSC module period [15:14]: Reserved

COMBO_PIPE_PHY_REG_033

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	COMMA_DET Comma detect
5	RO	0x0	COMMA_RECEIVED Comma received
4	RO	0x0	CDR_DATA_VALID CDR data valid
3	RO	0x0	RX_SUPERSPEED RX super speed
2	RO	0x0	DET_FINISH_PUSE Detection finish
1	RO	0x0	SKP_REMOVED SKP removed
0	RO	0x0	SKP_INSERTED SKP inserted

COMBO_PIPE_PHY_REG_034

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	EB_OF Ebuffer overflow

Bit	Attr	Reset Value	Description
6	RO	0x0	EB_UF Ebuffer underflow
5:4	RO	0x0	DISPARITY_ERR Dsiparity error
3:2	RO	0x0	INVALID_CODE Invalid code
1:0	RO	0x0	BRST_SYM BRST_SYM

COMBO_PIPE_PHY_REG_035
Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	NO_ERR NO_ERR
6	RO	0x0	BIST_RESULT BIST result
5	RO	0x0	TEST_DONE Test done
4	RO	0x0	RX_ELECIDLE_O RX electrical idle
3	RO	0x0	BIST_DONE BIST done
2	RO	0x0	BIST_TIMEOUT BIST timeout
1	RO	0x0	DET_FINSH Detect finish
0	RO	0x0	DET_RESULT Detect result

COMBO_PIPE_PHY_REG_036
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	ERR_CNT Error count

COMBO_PIPE_PHY_REG_037
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RO	0x00	MAX_JITTER Max jitter
1	RO	0x0	CDR_FL_EN CDR_FL_EN
0	RO	0x0	CDR_FREQ_LK CDR frequency lock

COMBO_PIPE_PHY_REG_038
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	USB3_MODE USB3_MODE

Bit	Attr	Reset Value	Description
5	RO	0x0	SATA_MODE SATA_MODE
4	RO	0x0	PCIE_MODE PCIE_MODE
3	RO	0x0	BEACON_LFPS BEACON_LFPS
2	RO	0x0	TX_DET_RX_0 TX_DET_RX_0
1	RO	0x0	GAT_PLL_CLK GAT_PLL_CLK
0	RO	0x0	SS_MODULE SS_MODULE

COMBO_PIPE_PHY_REG_039
Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	RATE_1_O RATE_1_O
6	RO	0x0	RATE_0_O RATE_0_O
5	RO	0x0	RATE_TX_1 RATE_TX_1
4	RO	0x0	RATE_TX_0 RATE_TX_0
3	RO	0x0	RATE_RX_1 RATE_RX_1
2	RO	0x0	RATE_RX_0 RATE_RX_0
1	RO	0x0	PWON_PLL_O PWON_PLL_O
0	RO	0x0	TXPLL_LOCK TX PLL lock

COMBO_PIPE_PHY_REG_040
Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	PWON_IREF PWON_IREF
6	RO	0x0	PWON_LFPS_DET PWON_LFPS_DET
5	RO	0x0	PWON_IDLE_DET PWON_IDLE_DET
4	RO	0x0	PWON_OOB_DET PWON_OOB_DET
3	RO	0x0	PWON_HS_DET PWON_HS_DET
2	RO	0x0	PWON_RX_BUS PWON_TX_BUF
1	RO	0x0	PWON_TX_BUF PWON_TX_BUF
0	RO	0x0	PWON_CDR_O PWON_CDR_O

COMBO_PIPE_PHY_REG_041
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	RX_DETECEED RX_DETECEED
5	RO	0x0	RX_LFPS_I RX_LFPS_I
4	RO	0x0	RX_SUPERSPEED RX_SUPERSPEED
3	RO	0x0	RX_SATA_IDLE RX_SATA_IDLE
2	RO	0x0	RX_PCIE_IDLE RX_PCIE_IDLE
1	RO	0x0	RX_ELECIDLE RX_ELECIDLE
0	RO	0x0	RX_VALID RX_VALID

COMBO_PIPE_PHY_REG_042
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RO	0x0	REFCK_DET_OUT REFCK_DET_OUT
5	RO	0x0	RTERM_DET_OUT RTERM_DET_OUT
4	RO	0x0	RX_ADPE_EQ_FL RX_ADPE_EQ_FL
3:0	RO	0x0	RX_ADPT_EQ_TRIM RX_ADPT_EQ_TRIM

COMBO_PIPE_PHY_REG_043
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RO	0x0	BERC_SYM BERC_SYM
4	RO	0x0	LP_RX_EN LP_RX_EN
3	RO	0x0	LP_SLAVE_EN LP_SLAVE_EN
2:0	RO	0x0	RX_ADPT_EQ_CTRIM RX_ADPT_EQ_CTRIM

COMBO_PIPE_PHY_REG_044
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	RX_DEBUG_R RX_DEBUG_R

COMBO_PIPE_PHY_REG_045
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	UNUSED_DEBUG RX_DEBUG_R

COMBO_PIPE_PHY_REG_046

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	unused_name1_bank1 bit[5]: phy clk_src source selects 1'b0: Source from APB 1'b1: Source from SOC bit[4:3]: phy clk_src control bit[2]: IP BIST_MODE source selects 1'b0: Source from APB 1'b1: Source from SOC bit[1:0]: rx_supperspeed delay selects: 2'b00: Delay 2 reference clock cycles 2'b01: Delay 6 reference clock cycles 2'b10: Delay 8 reference clock cycles 2'b11: Delay 10 reference clock cycles

COMBO_PIPE_PHY_REG_047

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	unused_name1_bank2 bit[7]: bypass PHY power down in p1.2 with PCIe mode 1'b0: Disable 1'b1: Enable bit[6]: mac_interface module data valid input source selects 1'b0: CDR lock from PMA 1'b1: Data valid generation by cdr_ctrl module bit[5]: PMA tx_deemph control source selects 1'b0: Source from PCS 1'b1: From APB config bit[4]: PMA tx_margin control source selects 1'b0: Source from PCS 1'b1: From APB config bit[3]: PMA tx_swing control source selects 1'b0: Source from PCS 1'b1: From APB config bit[2]: Reserved bit[1]: RX_STANDY_O output selects 1'b0: rx_standby_o active when rx_standby assert 1'b1: rx_standby_o normal output when rx_standby dis-assert bit[0]: Bypass com_det module sata_mode input when PHY in general serdes model 1'b0: Not SATA mode 1'b1: SATA mode

COMBO_PIPE_PHY_REG_048

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	register_bank2 Reserved

COMBO_PIPE_PHY_REG_049

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	register_bank3 Reserved

16.3.4 PCIe 3.0 PHY Registers Summary

N/A

16.3.5 PCIe 3.0 PHY Detail Registers Description

N/A

16.4 Interface Description

Table 16-3 PCIe 3.0 Analog IO Port 0 Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
ref_pad_clk_m	I	PCIE30_PORT0_REF_CLKN	N/A
ref_pad_clk_p	I	PCIE30_PORT0_REF_CLKP	N/A
resref	I/O	PCIE30_PORT0_RESREF	N/A
rx0_m	I	PCIE30_PORT0_RX0N	N/A
rx0_p	I	PCIE30_PORT0RX0P	N/A
rx1_m	I	PCIE30_PORT0_RX1N	N/A
rx1_p	I	PCIE30_PORT0_RX1P	N/A
tx0_m	O	PCIE30_PORT0_TX0N	N/A
tx0_p	O	PCIE30_PORT0_TX0P	N/A
tx1_m	O	PCIE30_PORT0_TX1N	N/A
tx1_p	O	PCIE30_PORT0_TX1P	N/A
vp/vptxX/vpdig	I/O	PCIE30_PORT0_AVDD0V75	N/A
vph	I/O	PCIE30_PORT0_AVDD1V8	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Table 16-4 PCIe 3.0 Analog IO Port 1 Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
ref_pad_clk_m	I	PCIE30_PORT1_REF_CLKN	N/A
ref_pad_clk_p	I	PCIE30_PORT1_REF_CLKP	N/A
resref	I/O	PCIE30_PORT1_RESREF	N/A
rx0_m	I	PCIE30_PORT1_RX0N	N/A
rx0_p	I	PCIE30_PORT1_RX0P	N/A
rx1_m	I	PCIE30_PORT1_RX1N	N/A
rx1_p	I	PCIE30_PORT1_RX1P	N/A
tx0_m	O	PCIE30_PORT1_TX0N	N/A
tx0_p	O	PCIE30_PORT1_TX0P	N/A
tx1_m	O	PCIE30_PORT1_TX1N	N/A

Module Pin	Dir	Pin Name	IOMUX Setting
tx1_p	O	PCIE30_PORT1_TX1P	N/A
vp/vptxX/vpdig	I/O	PCIE30_PORT1_AVDD0V75	N/A
vph	I/O	PCIE30_PORT1_AVDD1V8	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Table 16-5 Combo PIPE PHY 0 Analog IO Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
AVDH	I/O	PCIE20_SATA30_0_AVDD_1V8	N/A
AVDL	I/O	PCIE20_SATA30_0_AVDD_0V85	N/A
CKREFN	I/O	PCIE20_0_REFCLKN	N/A
CKREFP	I/O	PCIE20_0_REFCLKP	N/A
RXN	I	PCIE20_0_RXN/SATA30_0_RXN	N/A
RXP	I	PCIE20_0_RXP/SATA30_0_RXP	N/A
TXN	O	PCIE20_0_TXN/SATA30_0_TXN	N/A
TXP	O	PCIE20_0_TXP/SATA30_0_TXP	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Table 16-6 Combo PIPE PHY 1 Analog IO Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
AVDH	I/O	PCIE20_SATA30_1_AVDD_1V8	N/A
AVDL	I/O	PCIE20_SATA30_1_AVDD_0V85	N/A
CKREFN	I/O	PCIE20_1_REFCLKN	N/A
CKREFP	I/O	PCIE20_1_REFCLKP	N/A
RXN	I	PCIE20_1_RXN/SATA30_1_RXN	N/A
RXP	I	PCIE20_1_RXP/SATA30_1_RXP	N/A
TXN	O	PCIE20_1_TXN/SATA30_1_TXN	N/A
TXP	O	PCIE20_1_TXP/SATA30_1_TXP	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Table 16-7 Combo PIPE PHY 2 Analog IO Interface Description

Module Pin	Dir	Pin Name	IOMUX Setting
AVDH	I/O	PCIE20_SATA30_USB30_2_AVDD_1V8	N/A
AVDL	I/O	PCIE20_SATA30_USB30_2_AVDD_0V85	N/A
CKREFN	I/O	PCIE20_2_REFCLKN	N/A
CKREFP	I/O	PCIE20_2_REFCLKP	N/A
RXN	I	PCIE20_2_RXN/SATA30_2_RXN/USB30_SSRXN	N/A
RXP	I	PCIE20_2_RXP/SATA30_2_RXP/USB30_SSRXP	N/A
TXN	O	PCIE20_2_TXN/SATA30_2_TXN/USB30_SSTXN	N/A
TXP	O	PCIE20_2_TXP/SATA30_2_TXP/USB30_SSTXP	N/A

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

16.5 Application Notes

16.5.1 Subsystem Protocol Link Mapping

Table 16-8 Protocol Link Mapping

Controller Name	Physical Link Option	PCIe Link	REF CLKP/N	Digital GPIO	pcie30_phy_mode[2:0]					Note	
					3’b1xx	3’b000	3’b011	3’b001	3’b010		
					Config 1	Config 2	Config 3	Config 4	Config 5		
PCIE30X4 DM	PCIE30_PORT0_LANE0 PCIE30_PORT0_LANE1 PCIE30_PORT1_LANE0(2)⑥ PCIE30_PORT1_LANE1(3)⑥	X4G3	PCIE30_PORT0_REF_CLKP/N PCIE30_PORT1_REF_CLKP/N	PCIE30X4_*	√③	×	×	×	×	N/A	
	PCIE30_PORT0_LANE0 PCIE30_PORT0_LANE1	X2G3④	PCIE30_PORT0_REF_CLKP/N		O②	√	×	×	√		
	PCIE30_PORT0_LANE0	X1G3④	PCIE30_PORT0_REF_CLKP/N		O②	O②	√	√	O②		
PCIE30X2 RC	PCIE30_PORT1_LANE0 PCIE30_PORT1_LANE1	X2G3	PCIE30_PORT1_REF_CLKP/N	PCIE30X2_*	×	√	×	√	×		
	PCIE30_PORT1_LANE0	X1G3	PCIE30_PORT1_REF_CLKP/N		×	O②	√	O②	√		
PCIE30X1_0 RC	PCIE30_PORT0_LANE1	X1G3	PCIE30_PORT0_REF_CLKP/N	PCIE30X1_0_*	×	×	√	√	×	3’b1xx	{pcie_1ln_sel,pipe_phymode}⑤
	COMBO_PHY_1_LANE0	X1G2	PCIE20_1_REFCLKP/N		√①	√①	√①	√①	√①	3’b000	
SATA30_1	COMBO_PHY_1_LANE0		N/A	TBD	√①	√①	√①	√①	√①	3’bx10	
PCIE30X1_1 RC	PCIE30_PORT1_LANE1	X1G3	PCIE30_PORT1_REF_CLKP/N	PCIE30X1_1_*	×	×	√	×	√	3’b1xx	
	COMBO_PHY_2_LANE0	X1G2	PCIE20_2_REFCLKP/N		√①	√①	√①	√①	√①	3’b000	
SATA30_2	COMBO_PHY_2_LANE0		N/A	TBD	√①	√①	√①	√①	√①	3’bx10	
USB30OTG_2	COMBO_PHY_2_LANE0		N/A	N/A	√①	√①	√①	√①	√①	3’bx01	
PCIE30X1_2 RC	COMBO_PHY_0_LANE0	X1G2	PCIE20_0_REFCLKP/N	PCIE30X1_2_*	√①	√①	√①	√①	√①	3’bx00	
SATA30_0	COMBO_PHY_0_LANE0		N/A	TBD	√①	√①	√①	√①	√①	3’bx10	

Note：

①：The pcie_30_phy_mode is ignored by the tagged Configuration, it is only decided by {pcie_1ln_sel,pipe_phymode}.

②: The tagged link is down width of an upper link width.

③: In this configuration, if the link width down to X2 or X1, both of the reference clocks still need to be driven and should be from the same clock generator.

*④: If this link is active and regarded as Endpoint function, then this *PORT0* can’t be bifurcated.*

⑤: The pcie_1ln_sel stands for pcie_1l0_sel and pcie_1l1_sel located in PD PHP GRF, and for COMBO PHY 0, the pcie_1l2_sel is reserved. The pcie_1ln_sel is only valid in PCIe scenario.

⑥: In X4 link, the PORT 1 Lane0 aka Lane2, and PORT 1 Lane1 aka Lane3

Table 16-9 Name Mapping of Controller

Controller Number	Name	Aka
0	PCIe30X4 DM	PCIe3_4L
1	PCIe30X2 RC	PCIe3_2L
2	PCIe30X1_0 RC	PCIe3_1L0
3	PCIe30X1_1 RC	PCIe3_1L1
4	PCIe30X1_2 RC	PCIe3_1L2

Table 16-10 Link IO Name Mapping

PHY IO Name	PCIe	PCIe IO	SATA IO	USBOTG IO
COMBO_PHY_0_LANE0	1L2	PCIE20_0_{TX,RX}P/N	SATA30_0_{TX,RX}P/N	
COMBO_PHY_1_LANE0	1L0	PCIE20_1_{TX,RX}P/N	SATA30_1_{TX,RX}P/N	
COMBO_PHY_2_LANE0	1L1	PCIE20_2_{TX,RX}P/N	SATA30_2_{TX,RX}P/N	USB30_SS{TX,RX}P/N

16.5.2 Combo PHY Application Note

16.5.2.1 Operation Mode Support

The following mode are supported for IP operation, IP configuration other than this list are not supported

Table 16-11 PHY operation mode

PHY_MODE	RATE	BUS_WIDTH	PHY Operation Mode
00	00	00	PCIe Gen1, 32bit, PCLK=62.5M
		01	N/A
	01	00	PCIe Gen2, 32bit, PCLK=125M
		01	N/A

PHY_MODE	RATE	BUS_WIDTH	PHY Operation Mode
01	00	00	USB3.0, 32bit, PCLK=125M
01	00	01	N/A
10	00	00	N/A
		01	SATA Gen1, 16bit, PCLK=75M
	01	00	N/A
		01	SATA Gen2, 16bit, PCLK=150M
	10	00	N/A
		01	SATA Gen3, 16bit, PCLK=300M

- PHY_MODE is configured by PIPE_PHY_GRF_PIPE_CON0.pipe_phymode
- RATE is controlled by protocol controller or can be configured PIPE_PHY_GRF_PIPE_CON0.pipe_rate when override is enabled
- BUS_WIDTH is controlled by protocol controller or can be configured PIPE_PHY_GRF_PIPE_CON0.pipe_databuswidth when override is enabled

16.5.2.2 Power Down Mode

Power down control signals to individual analog modules are generated based on PWDN[1:0] setting from PIPE inputs as shown in below table. An override function is provided for debug purpose, see Multi-PHY register list. (√ – active; ╳– power down)

Table 16-12 PCIE power down mode

PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
0000	--	√	√	√	√
0001	0(illegal)	√	√	√	√
	1	╳	√	√	√
0010	0(illegal)	√	╳	╳	√
	1	╳	╳	╳	√
0011	0	√	╳	╳	╳
	1	╳	╳	╳	╳
1---	0(illegal)	√	╳	╳	╳
	1	╳	╳	╳	╳

In PCIe mode, power for IVREF and PCIe idle detector are always on, while power for LFPS, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of Rx buffer is off when RX_STANDBY is high.

Note: If TX_ELECIDLE(pipe_txelecidle) and TX_COMPLIANCE(pipe_txcompliance) is both asserted, all powers are off.

Table 16-13 USB3 power down mode

PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
0000	--	√	√	√	√
0001	0	√	√	╳	√
	1	√	√	╳	√
0010	0	√	√	╳	√
	1	√	√	╳	√
0011	0	√	√	╳	╳
	1	╳	√	╳	╳

In USB3.0 mode, power for IVREF and LFPS detector are always on, while power for PCIe idle, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of LFPS detector and power of Rx buffer are turned off if termination is not on.

Table 16-14 SATA power down mode

PWDN[3:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
0000	--	√	√	√	√
0001	0(illegal)	√	×	√	√
	1	×	×	√	√
0011	0(illegal)	√	×	×	√
	1	×	×	×	√
0101	0(illegal)	√	×	√	√
	1	×	×	√	√
0111	0(illegal)	√	×	×	×
	1	×	×	×	×

In SATA mode, power for IVREF and 1.5G SATA idle detector are always on, while power for LFPS and PCIE idle detectors are always off, and power of Rx buffer is off when RX_STANDBY is high.

The PWDN is controlled by protocol controller default, it also can be controlled by PIPE_PHY_GRF_PIPE_CON0.pipe_powerdown when override is enabled.

16.5.2.3 Reference Clock

Combo PIPE PHY's reference clock source can be selected from either PLL_CKREF_INNER or CKREFP/CKREFN, according to the status CKREF_SRC[1:0] after the PHY de-asserted reset.

The differential pair CKREFP/N can be configured as either reference clock input or reference clock output, according to CKREF_SRC[1]

Configure the register signal su_trim[29] to select reference clock(ckref) or 100MHz clock (ck100m_pcie) from PLL to drive to CKREFP/N

The CKREF_SRC is controlled by PIPE_PHY_GRF_PIPE_CON3.phy_clk_ref_src, and the PIPE_PHY_GRF_PIPE_CON3.phy_clk_sel is used to set the frequency of the selected reference clock.

The PLL_CKREF_INNER is derived by SoC internal CRU, refers to CRU for detail configurations to generate the appropriate reference clock.

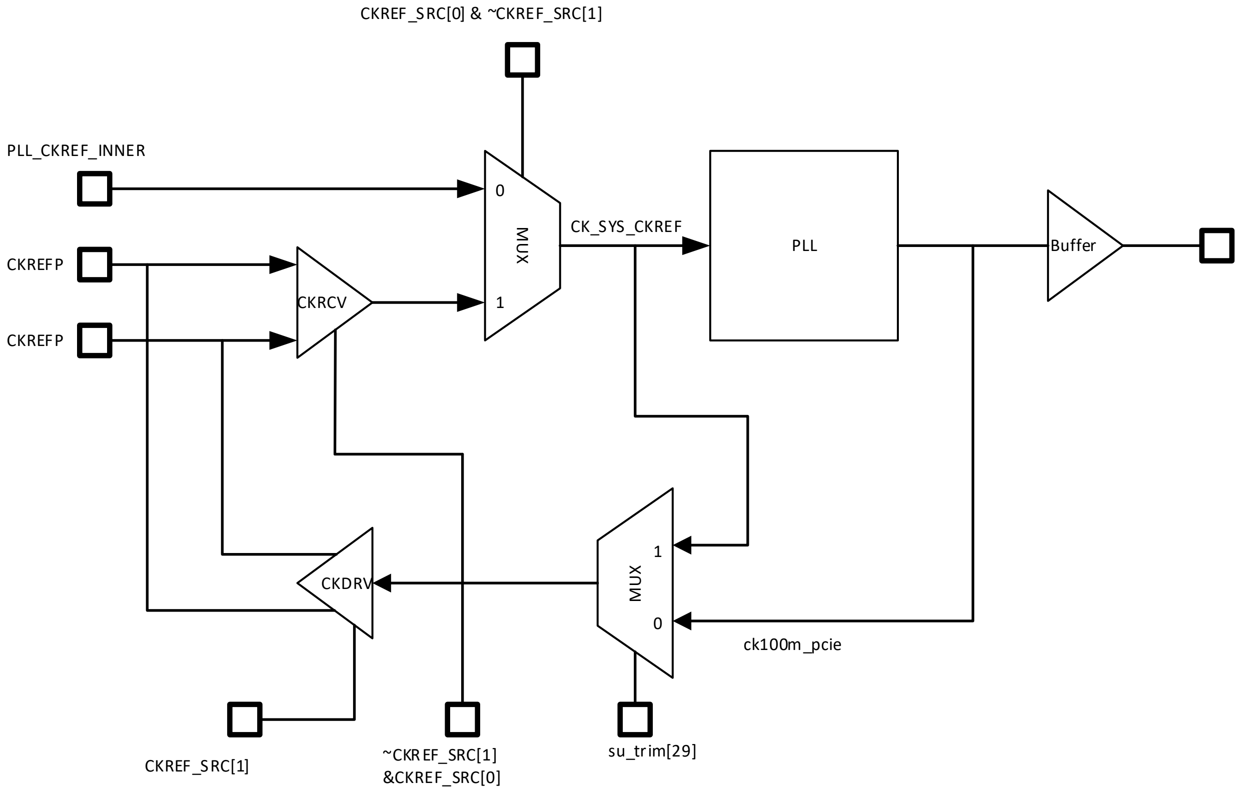

Fig. 16-7 Reference Clock Structure of Combo PIPE PHY

16.5.3 PCIe 3.0 PHY Application Note

16.5.3.1 Aggregation and Bifurcation

The PCIe 3.0 PCS can be connected to up to 2 PHYs, so that the number of lanes on the PCIe 3.0 PCS equals the cumulative number of lanes on the PHYs. This feature is referred to as PHY aggregation.

The PCIe 3.0 PCS lanes can be configured to operate as one or more links with each link configured to operate at a different rate (pipe_laneX_rate) and in a different protocol (pipe_laneX_protocol), provided the PHY supports such a bifurcation configuration. Each PCIe 3.0 PCS lane can be independently configured to be part of a particular link using the pipe_laneX_phy_src_sel input.

In current design subsystem, aggregation and bifurcation is automatically implemented by configuring the pcie30_phy_mode, it is no necessary do other configuration by default.

The pipe_laneX_phy_src_sel changed depends on the pcie30_phy_mode, so any changes to pcie30_phy_mode must be followed by phy_reset (PHPTOPSOFTRST_CON00.resetn_pcie30_phy) assertion.

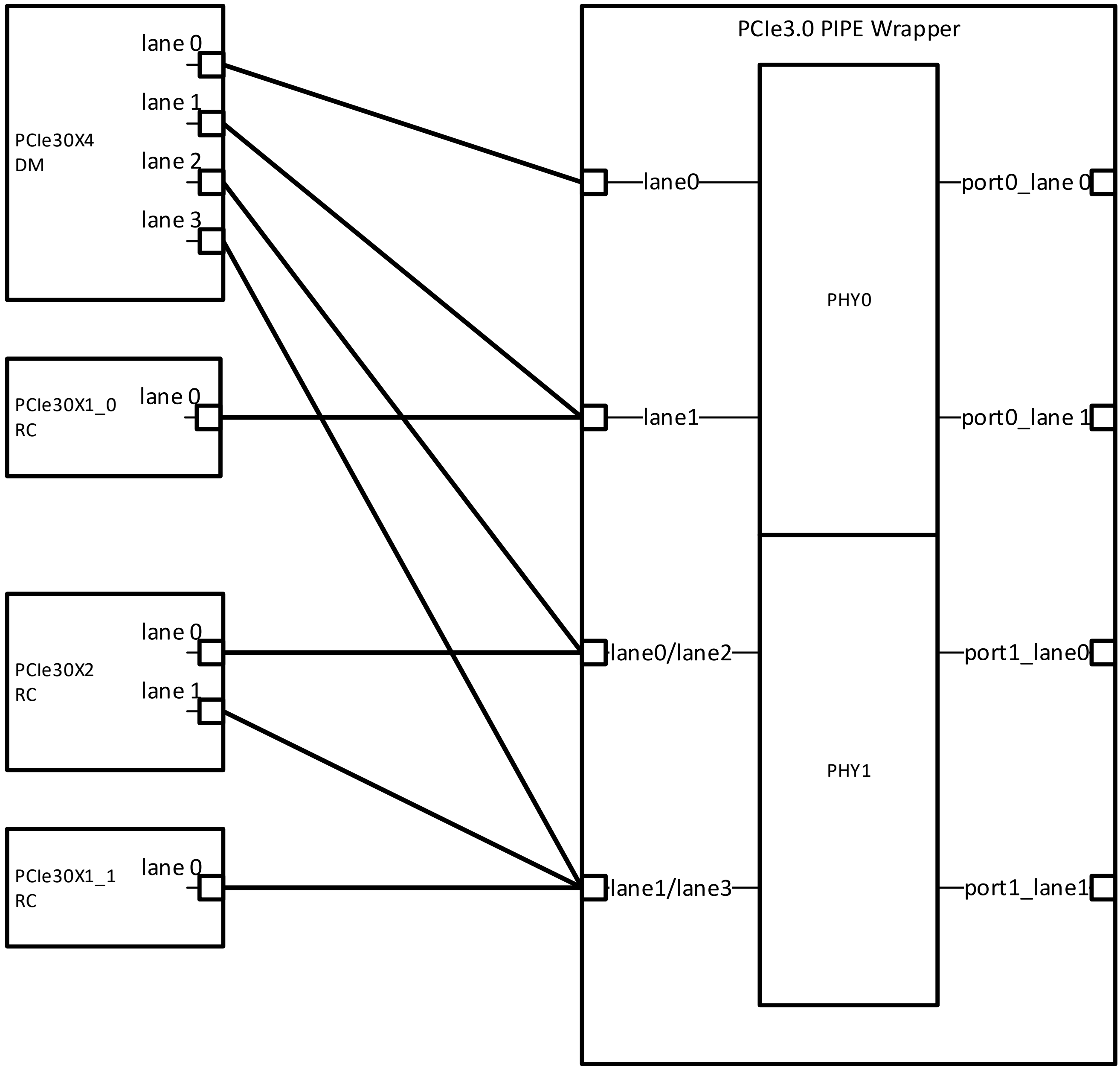

Fig. 16-8 Full Mapped Interconnection of PCIe 3.0 PHY

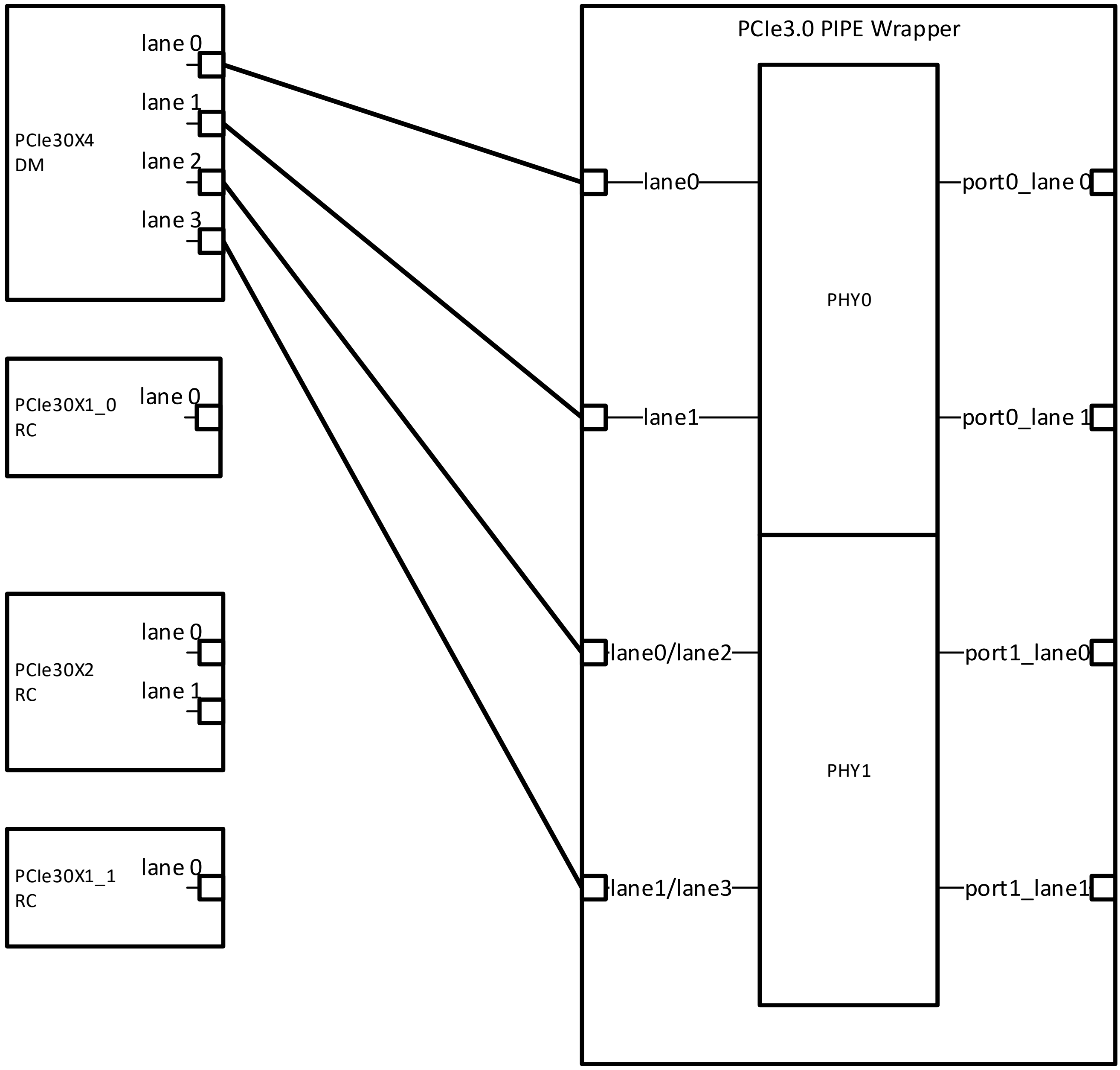

Fig. 16-9 Config1 -- Aggregation of PCIe 3.0 PHY0 and PHY1

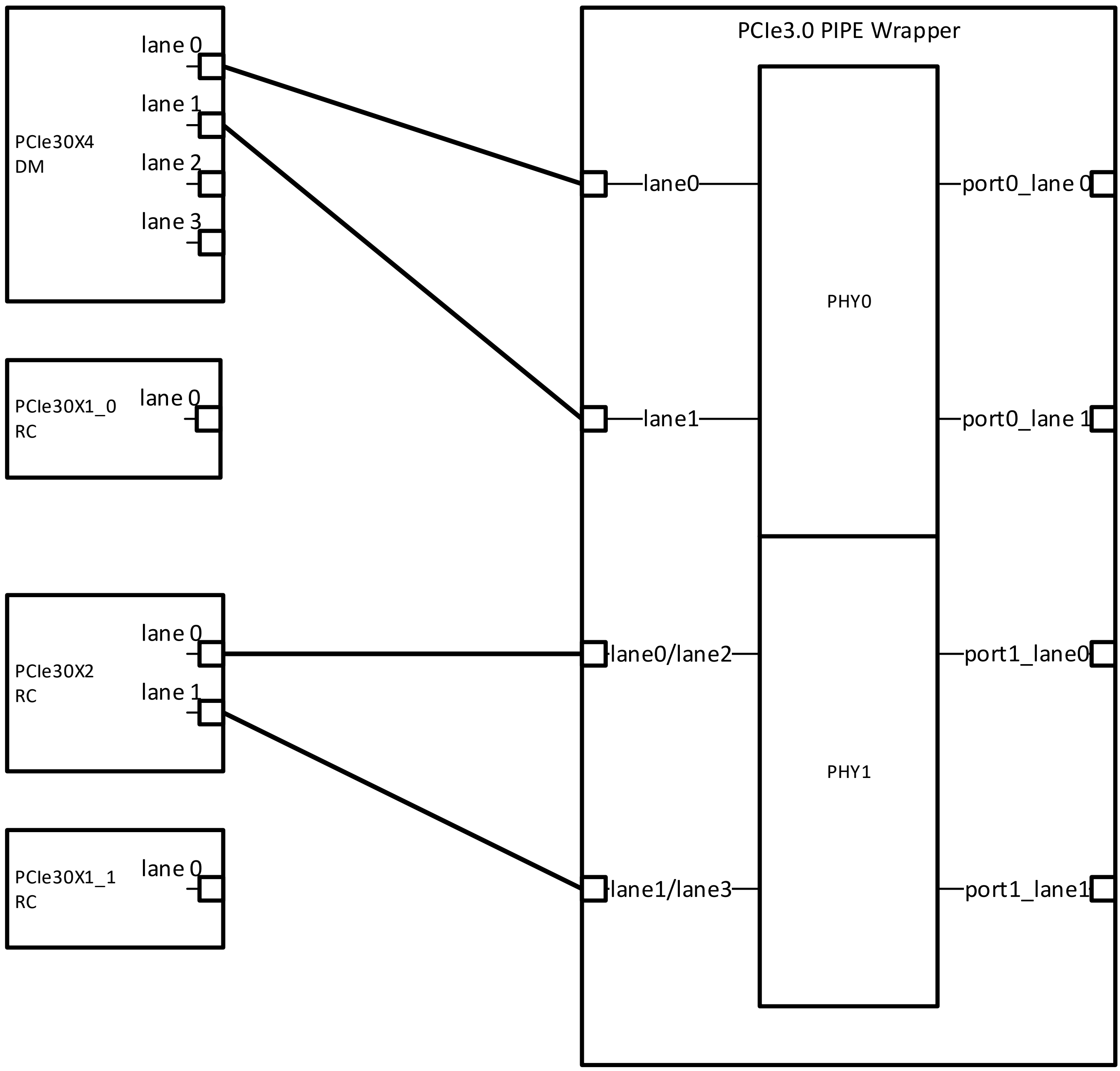

Fig. 16-10 Config2 -- Non-Aggregation and Non-Bifurcation of PHY0 and PHY1

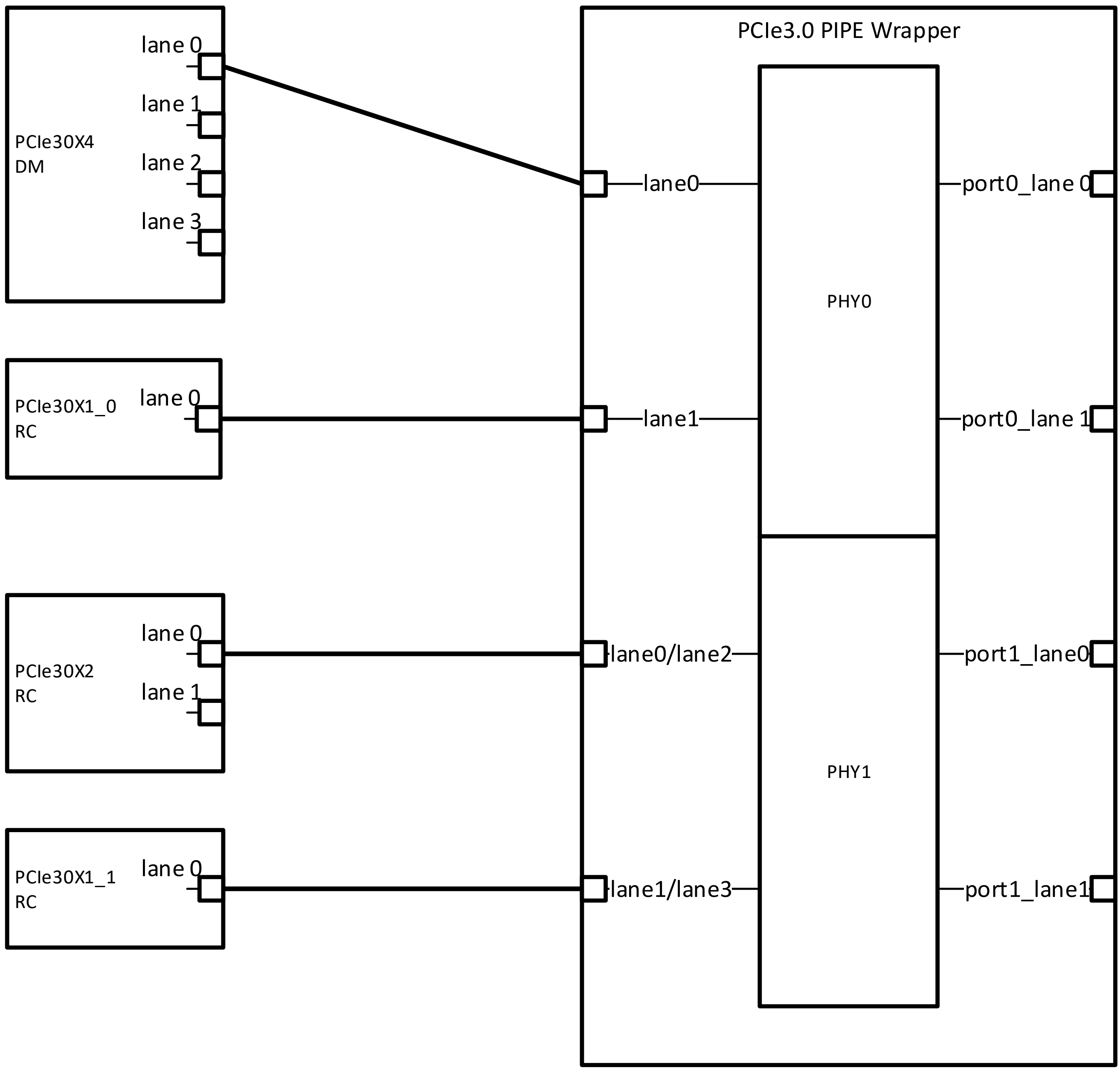

Fig. 16-11 Config3 -- Bifurcation for Both PHY0 and PHY1

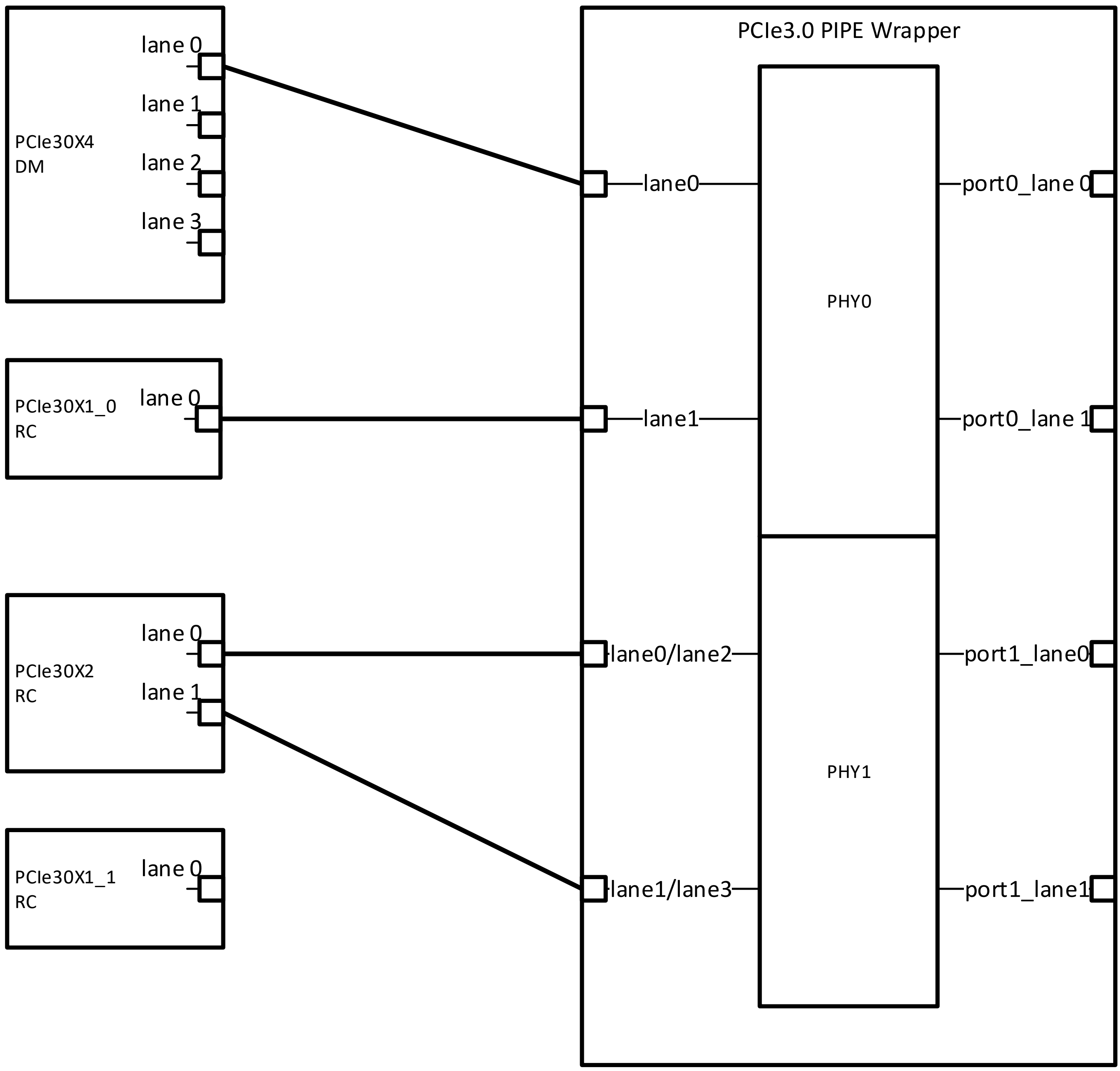

Fig. 16-12 Config4 -- Only PHY0 Bifurcation

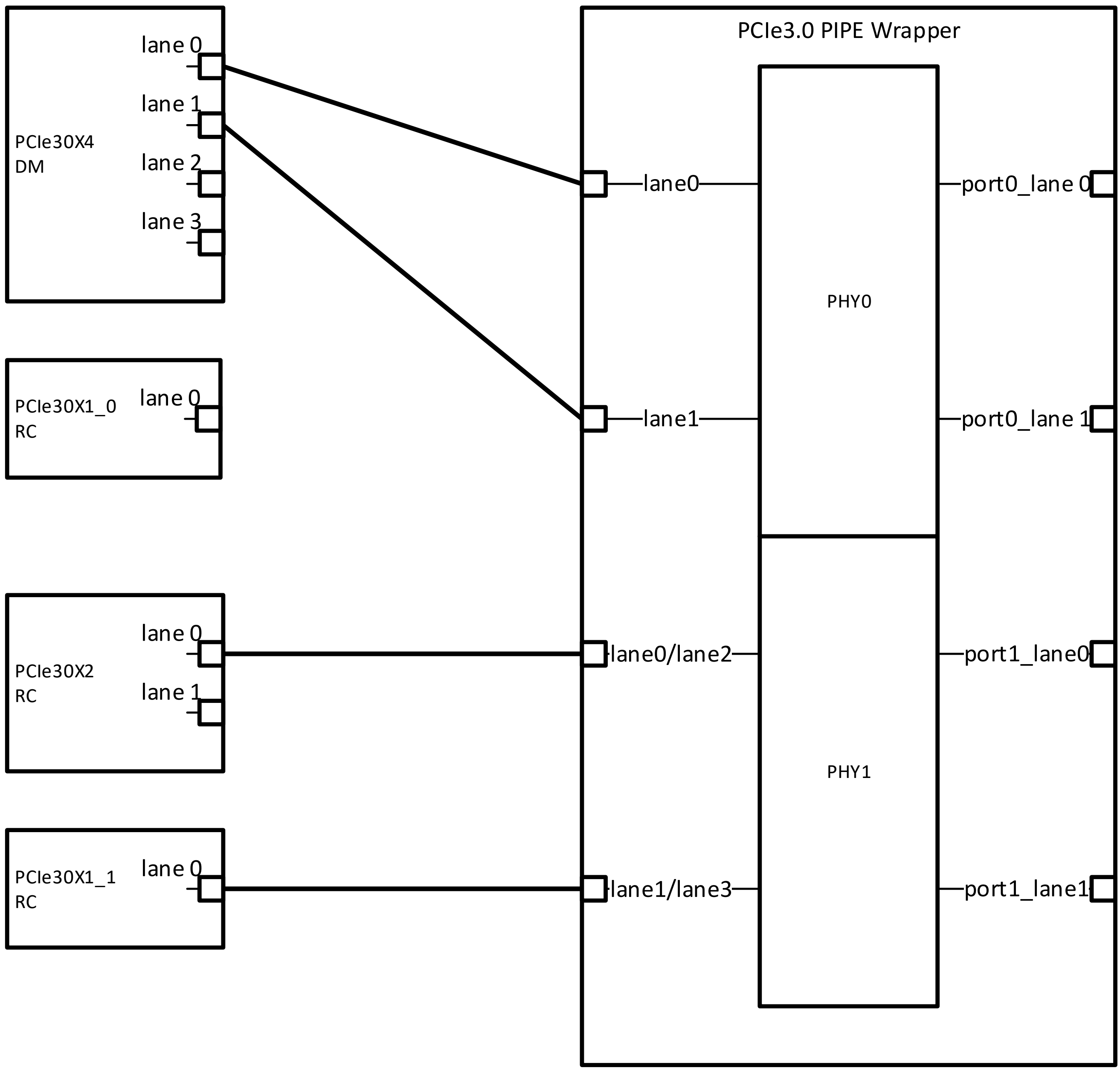

Fig. 16-13 Config5 -- Only PHY1 Bifurcation

16.5.3.2 PHY Power-Up

Power up the vp* and vph power supplies in any order and then proceed with the PHY reset and initialization sequence (vp* indicates the grouping of all core supplies; vp, vpdig, and vptxX).

- The state of the PHY is unknown after power up but before assertion of reset. The PHY may exhibit unwanted behavior such as TX enabled, or RX terminations activated.
- While the unknown state is undesirable, the PHY has been designed to prevent damage if it is left in this state.
- Use a ramp time of no faster than 10 μs and a rate no faster than (supply voltage)/10 us. The ramp requirement is set based on our ESD clamp triggering time.

16.5.3.3 PHY Initialization and Reset Sequences

During PHY reset and initialization sequence, the PHY performs power up circuit calibrations and enters the configuration mode defined by the primary inputs. The PHY does not require any clocks to be supplied to enter the reset state (assertion of phy_reset). Exit from the reset state is indicated by de-assertion of txX_ack/rxX_ack and requires a reference clock to be supplied and ref_clk_en input to be asserted.

When phy_reset is asserted, the TX and RX terminations are disabled and txX_p/m are tri-stated for all lanes of the PHY. In addition to global phy_reset, txX_reset/rxX_reset inputs can be used to reset individual lanes in the PHY. When txX_reset is asserted, the txX_pstate is similar to P2, the TX terminations are disabled and txX_p/m are tri-stated for lane X. When rxX_reset is asserted, the rxX_pstate is similar to P2, the RX terminations are disabled for lane X. TxX_reset/rxX_reset are ignored when phy_reset is asserted. Asserting either txX_reset or rxX_reset during phy_reset assertion stalls the Raw_PCS FSM operation before internal registers are updated for lane X after phy_reset is de-asserted.

16.5.3.4 Lane Disabling and Up/Down-Configuration

16.5.3.4.1 RX Standby Mode

A lane in an active link can be disabled by setting pcs_txX_elecidle = 1 and pcs_rxX_standby = 1 while keeping pcs_laneX_powerdown set to P0. This setting maintains the TX common mode on the lane while turning off the transmit driver and disabling the CDR—keeping the rest of receiver circuitry on. The disabled lanes can be enabled again with minimal supported wake-up time by setting pcs_txX_elecidle = 0 and pcs_rxX_standby = 0.

16.5.3.4.2 PIPE Lane Disable

A lane in an active link can be disabled by setting pcs_txX_elecidle = 1 and pcs_tx1_compliance = 1. In this state, the PHY’s TX and RX are placed in a P2-equivalent state (TX and RX circuits off). This state is a significantly lower power state as compared to disabling the lane using pcs_txX_elecidle = 1 and pcs_rxX_standby = 1. The disabled lanes can be enabled again according to the requirements defined in the PIPE 4.3 specification, “Multi-lane PIPE – PCI Express Mode” section. Therefore, the MAC must either assert pcs_laneX_reset_n or set pcs_laneX_powerdown to P1 at the same time as exiting the disabled state

16.5.3.4.2.1 Exception

The PIPE 4.3 specification states that the PHY should ignore the PIPE signals when a lane is disabled using pcs_txX_elecidle = 1 and pcs_tx1_compliance = 1.
When in such a disabled state, the Consumer PCIe 3.0 PCS supports the following two modes:

- upcs_pipe_config[0] = 0: The Consumer PCIe 3.0 PCS ignores PIPE interface signals. In this mode, the pcs_laneX_pcs_clk output is gated.
- upcs_pipe_config[0] = 1: The Consumer PCIe 3.0 PCS monitors the PIPE interface signal, pcs_laneX_powerdown. Therefore, if pcs_laneX_powerdown is set to P0/P0s/P1 , the pcs_laneX_pcs_clk output is available. This mode enables the MAC to continue using the pcs_laneX_pcs_clk output from a particular lane in a link to sample/launch PIPE signals for other active lanes in the same link, resulting in a simpler clock architecture in the MAC. Without this mode, the MAC would be required to use the pcs_laneX_pcs_clk output of each lane to sample/launch data of the same lane.

16.5.3.4.3 P1.2 State

A lane can also be disabled by placing the lane in a P1.2 state. If all other lanes in the link and all lanes on one PHY are in a P1.2 state, this mode is the most power-efficient mode, because in this case the reference clock for that PHY can be turned off.

16.5.3.5 Configuration for a Disabled PHY

There are several methods to disable a PHY, if the PHY is not being used in application (one or more PHYs are disabled). To disable a PHY, follow the methods outlined in below table.

Table 16-15 Signal Connections if the PHY is Not Used

Signal	Method 1: All Power Supplies (vp, vph, vptxX, vpdig, gd) at Nominal Voltage and IDDQ = 1	Method 2: All Power Supplies (vp, vph, vptxX, vpdig, gd) Connected to Ground	Method 3: All Power Supplies (vp, vph, vptxX, vpdig, gd) Left Unconnected (Floating)
PMA inputs from Raw PCS	Automatically engaged isolation	Tie all inputs to ground—	Tie all inputs to ground—

Signal	Method 1: All Power Supplies (vp, vph, vptxX, vpdig, gd) at Nominal Voltage and IDDQ = 1	Method 2: All Power Supplies (vp, vph, vptxX, vpdig, gd) Connected to Ground	Method 3: All Power Supplies (vp, vph, vptxX, vpdig, gd) Left Unconnected (Floating)
	cells	recommended	recommended
PMA outputs to Raw PCS	Insert isolation gate-recommended	Insert isolation gate	Insert isolation gate
rxX_p, rxX_m	Leave floating or tie low	Leave floating or tie low	Leave floating or tie low
txX_p, txX_m	Leave floating	Leave floating	Leave floating
resref	Leave floating	Leave floating	Leave floating
ref_pad_clk_p, ref_pad_clk_m	Tie low	Tie low	Tie low
ref_alt_clk_p, ref_alt_clk_m	Tie low	Tie low	Tie low

- For methods 2 and 3, to ensure that the outputs do not float high nor drive any active logic, you must use isolation gates on PHY outputs, this is achieved by set pcie30_clamp_n to "0" . Furthermore, to prevent the PHY circuitry from inadvertently toggling, it is good practice to tie all the inputs to the ground.
- If REXT is being shared with other PHYs, use only method 1. For REXT sharing, the request and ack handshake logic within each PHY must be powered and should allow the handshake signals from other PHYs to propagate through.
- If clock is being repeated, ensure that you do not power down the PMAs in the chain.
- For more information about IDDQ mode, set test_burnin =0 && test_powerdown =1

16.5.3.6 Reference Clock Implementation

The PHY supports a differential reference clock source. The source may be driven through either external pads or internal pins. The reference clock must meet specific requirements for signal swing and jitter. The clock frequency supported by current PHY is 100M.

There are two types of reference clock implementations:

- External off-chip reference clocks using ref_pad_clk_p/ref_pad_clk_m
- On-chip reference clocks using ref_alt_clk_p/ref_alt_clk_m, from internal CRU

The external off-chip reference clock implementation support either a differential clock or a CMOS single ended clock. The external off-chip reference clock input is an unterminated, AC coupled input. If the reference clock is a single-ended CMOS clock, one of the clock inputs (such as ref_pad_clk_p) must be a full-swing CMOS clock, and the other input (such as ref_pad_clk_m) should be tied to either high or low. If the reference clock is differential, it may be CML or LVDS, or any differential specification that meets the specification. Any reference clock inputs that are not being used should be tied to ground.

The on-chip reference clock implementation supports only a CMOS level clock implementation. The on-chip reference clock can we input either differentially or single-ended. If the on-chip reference clock is sent in single-ended then ref_alt_clk_p must be used and ref_alt_clk_m should be tied to ground.

16.5.3.6.1 External Off-Chip Clock Sources

When routing reference clocks in from off-chip, a signal integrity (SI) analysis should be performed using a model of the clock input, package, board traces, and clock source. This analysis should confirm that the reference clock input specification is being met across the external on-chip reference clock input (ref_pad_clk_p/ref_pad_clk_m).

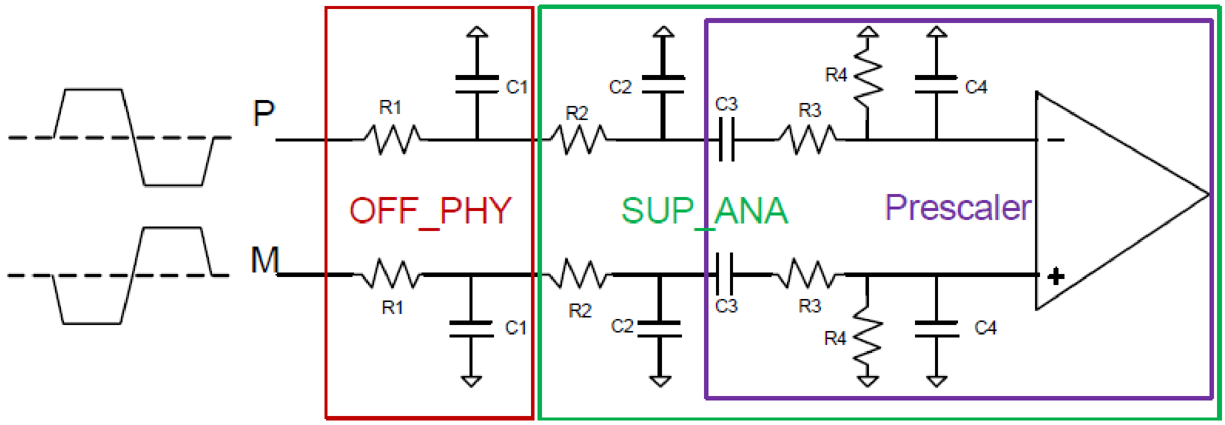

Fig. 16-14 Model of Reference Clock Pad Input Load

Table 16-16 Reference Clock External Pad Input Parasitics

Location	Parasitic Device	Value	Unit
OFF PHY	R1	≤50	Ohm
OFF PHY	C1	≤1	pF
Within PHY: Bump to prescaler input	R2	≤50	Ohm
Within PHY: Bump to prescaler input	C2	≤1	pF
Within prescaler: 2nd ESD Prot resistor	R3	400	Ohm
Within prescaler: AC cap	C3	840	fF
Within prescaler: DC Bias resistor	R4	456k	Ohm
Within prescaler: Input cap of prescaler input RX	C4	50	fF

To improve common-mode rejection ratio (CMRR), differential traces should be as well matched as possible

The reference clock inputs are not terminated. This is to allow for connection of reference clocks to multiple PHYs at the same time. If termination is used, it should be placed on your board as close to the chip as possible. For PCIe, see the PCIe CEM specification for detail on how to implement the on-board termination

16.5.3.6.2 On-Chip Clock Sources

Many applications require an on-chip reference clock. The challenge is getting the reference clock to the PHY without adding supply-noise-induced jitter to the clock. The ref_alt_clk_p/ref_alt_clk_m is supplied by PHP PLL which powered by PMU VDD to get cleaner clock.

16.5.3.7 External SRAM Support

The Raw PCS stores the instruction code to execute the calibration and adaptation algorithms. In order to minimize the area of the Raw PCS, this pre-optimized and pre-validated code is stored in the form of hardcoded lookup table. An external SRAM must be included for the purpose of updating the IP firmware. This provides flexibility for future and post-silicon product enhancements.

After de-assertion of phy_reset, the boot loader in the Raw PCS loads the code from the internal lookup table to the external SRAM and asserts output signal, sram_init_done. After initialization of SRAM, user can change the SRAM contents (or access any PHY register) using either the JTAG or the CR Parallel Interface by addressing the SRAM address space in the register map. After external access to the SRAM (or any other PHY register) is complete, input sram_ext_ld_done should be set high, allowing the FSMs in the Raw PCS to start executing the code from SRAM.

When sram_bypass is asserted, the access to the SRAM is bypassed and the lane FSMs execute the code from the hard-coded lookup table in the Raw PCS. This signal is meant to be used only for debugging purposes and must not change after phy_reset is negated.

The offset of the each PHY’s SRAM begins at 0x18000, ends at 0x1BFFC.

Chapter 17 Process-Voltage-Temperature Monitor (PVTM)

17.1 Overview

The Process-Voltage-Temperature Monitor (PVTM) is used to monitor the chip performance variance caused by chip process, voltage and temperature.
PVTM supports the following features:

- A clock oscillation ring is integrated and used to generate a clock like signal, the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit.
- A calculation logic is used to measure the frequency of the clock oscillation ring.
- Follow PVTM blocks are supported:
  - BIGCORE0_PVTM, used near A76_0/1
  - BIGCORE1_PVTM, used near A76_2/3
  - LITCORE_PVTM, used near DSU and A55_0/1/2/3
  - NPU_PVTM, used near NPU
  - GPU_PVTM, used near GPU
  - PMU_PVTM, used near PMU

17.2 Block Diagram

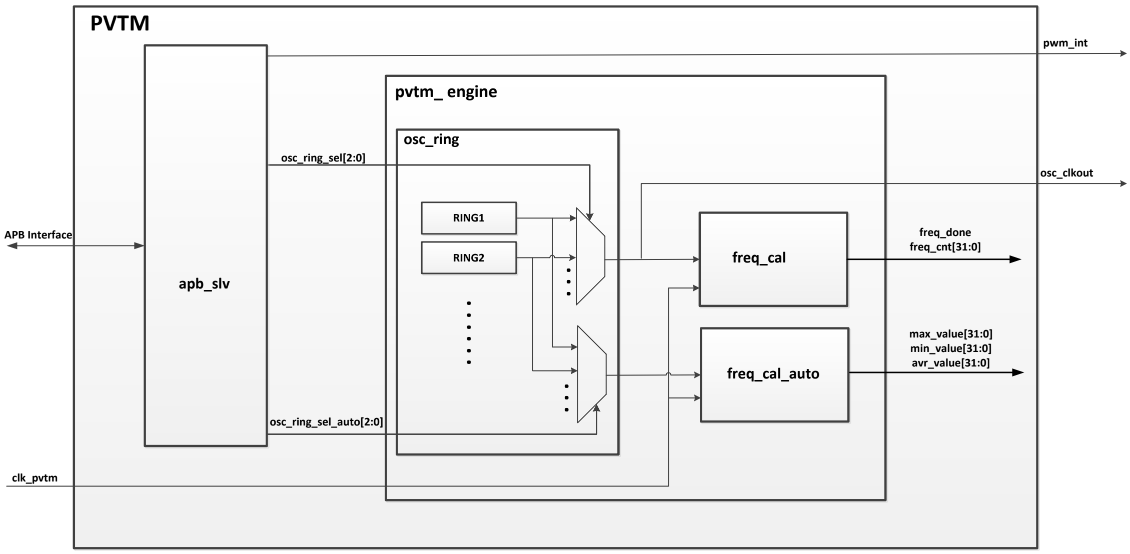

Fig. 17-1 PVTM Block Diagram

The PVTM include two main blocks:

- apb_slv

APB slave interface with 32-bit bus width.

- pvtm_engine

It is composed with inverters with odd number, which is used to generate a clock.
BIGCORE0/BIGCORE1/LITCORE_PVTM/GPU/NPU_PVTM supports several clock oscillation-rings, and finally selects one. PMU_PVTM only supports one clock oscillation rings.
The frequency calculation logic of BIGCORE0/BIGCORE1/LITCORE_PVTM/GPU/NPU_PVTM support manual mode and auto mode, and these two modes can be used at simultaneously.
The PMU_PVTM only support manual mode.

17.3 Function Description

17.3.1 Frequency Calculation

A clock is generated by the oscillation ring and a frequency fixed clock clk_pvtm is used to calculate the cycles of the clock. Supposing the time period is 1s, then the clock period of oscillation ring clock is T= 1/clock_counter(s), the cell delay value is T/2.
For manual mode, user can only get one frequency result for a calculation.
For auto mode, user can set the calculation times, and get the maximum, minimum and average frequency during calculation. It also supports to generate an interrupt when the minimum or average frequency below a threshold. The threshold can be configured.

17.3.2 Low power mode usage

A clock divided from PMU_PVTM oscillation ring is used in low power mode, which can replace the function of 32KHz clock source

17.4 Register Description

17.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PVTM_VERSION	0x0000	W	0x00000203	PVTM version register
PVTM_CON0	0x0004	W	0x00000000	PVTM control register0
PVTM_CON1	0x0008	W	0x00000000	PVTM control register 1
PVTM_CON2	0x000C	W	0x00000000	PVTM control register 2
PVTM_CON3	0x0010	W	0x00000000	PVTM control register 3
PVTM_CON4	0x0014	W	0x00000000	PVTM control register 4
PVTM_CON5	0x0018	W	0x00000000	PVTM control register 5
PVTM_CON6	0x001C	W	0x00000000	PVTM control register 6
PVTM_INT_EN	0x0070	W	0x00000000	PVTM Interrupt Enable Register
PVTM_INTSTS	0x0074	W	0x00000000	PVTM Interrupt Status Register
PVTM_STATUS0	0x0080	W	0x00000000	PVTM status register0
PVTM_STATUS1	0x0084	W	0x00000000	PVTM status register1
PVTM_STATUS2	0x0088	W	0x00000000	PVTM status register2
PVTM_STATUS3	0x008C	W	0x00000000	PVTM status register3
PVTM_STATUS4	0x0090	W	0x00000000	PVTM status register4
PVTM_STATUS5	0x0094	W	0x00000000	PVTM status register5
PVTM_STATUS6	0x0098	W	0x00000000	PVTM status register6
PVTM_STATUS7	0x009C	W	0x00000000	PVTM status register7

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.2 Detail Register Description

PVTM_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RU	0x0203	version PVTM version

PVTM_CON0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	pvtm_rnd_seed_en Set high to enable the round seed in PVTM.

Bit	Attr	Reset Value	Description
4:2	RW	0x0	pvtm_osc_sel Oscillation ring selection For CPU_PVTM: 3'b000: oscillation ring 0 3'b001: oscillation ring 1 3'b010: oscillation ring 2 3'b100: oscillation ring 4 3'b101: oscillation ring 5 3'b110: oscillation ring 6 others: Reserved For GPU/NPU/TOP_PVTM: 3'b000: oscillation ring 0 3'b001: oscillation ring 1 others: Reserved For PMU_PVTM: 3'b000: oscillation ring 0 others: Reserved
1	RW	0x0	pvtm_osc_en Set high to enable the oscillation ring in the PVTM.
0	RW	0x0	pvtm_start Set high to start PVTM.

PVTM_CON1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_cal_cnt PVTM calculation counter

PVTM_CON2

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	pvtm_osc_ring_autosel_en PVTM oscillation ring auto select enable control. It will take turns the oscillation ring (enabled by pvtm_osc_ring_autosel_en[7:0]) in order and then loop back. When none of them is enabled, use the oscillation ring selected by pvtm_osc_sel_auto. For example, when set pvtm_osc_ring_autosel_en[7:0]=8'b00000111, it will take turns oscillation ring 0, oscillation ring 1 and oscillation ring 2 in order to test and then loopback, other rings will not be tested.

Bit	Attr	Reset Value	Description
7	RW	0x0	pvtm_avr_cal_mode PVTM average value calculate mode 1'b0: The average value = (summary_value-max_value-min_value) /(measurement_number-2) 1'b1: The average value = summary_value /measurement_number
6	RW	0x0	pvtm_avr_update_mode PVTM average value update mode 1'b0: Only when the number of measurements arrive pvtm_avr_period, the average value is updated. 1'b1: When the number of measurements is equal to or greater than 3, the average value is updated gradually.
5	RW	0x0	pvtm_start_auto_mode PVTM start mode 1'b0: When the number of measurements arrive pvtm_cal_period, calculate stop and pvtm_start_auto is cleared. 1'b1: When the number of measurements arrive pvtm_cal_period, calculate don't stop and pvtm_start_auto is not cleared.
4:2	RW	0x0	pvtm_osc_sel_auto Oscillation ring selection for auto mode For CPU_PVTM: 3'b000: oscillation ring 0 3'b001: oscillation ring 1 3'b010: oscillation ring 2 3'b100: oscillation ring 4 3'b101: oscillation ring 5 3'b110: oscillation ring 6 others: Reserved For GPU/NPU/TOP_PVTM: 3'b000: oscillation ring 0 3'b001: oscillation ring 1 others: Reserved For PMU_PVTM: 3'b000: oscillation ring 0 others: Reserved
1	RW	0x0	pvtm_osc_en_auto Set high to enable the oscillation ring in the PVTM for auto mode.
0	RW	0x0	pvtm_start_auto Set high to start PVTM for auto mode.

PVTM_CON3
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_cal_cnt_auto PVTM calculation counter for auto mode

PVTM_CON4

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pvtm_avr_period PVTM average calculation period
15:0	RW	0x0000	pvtm_cal_period PVTM calculation period

PVTM_CON5

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_min_threshold PVTM minimum value threshold

PVTM_CON6

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_avr_threshold PVTM average value threshold

PVTM_INT_EN

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	cal_done_Int_en 1'b0: Calculation done Interrupt disabled 1'b1: Calculation done Interrupt enabled
1	RW	0x0	avr_value_Int_en 1'b0: Average value Interrupt disabled 1'b1: Average value Interrupt enabled
0	RW	0x0	min_value_Int_en 1'b0: Minimum value Interrupt disabled 1'b1: Minimum value Interrupt enabled

PVTM_INTSTS

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	cal_done_IntSts 1'b0: Calculation done Interrupt not generated 1'b1: Calculation done Interrupt generated

Bit	Attr	Reset Value	Description
1	W1C	0x0	avr_value_IntSts 1'b0: Average value Interrupt not generated 1'b1: Average value Interrupt generated
0	W1C	0x0	min_value_IntSts 1'b0: Minimum value Interrupt not generated 1'b1: Minimum value Interrupt generated

PVTM_STATUS0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pvtm_freq_done Indicates PVTM frequency count done.

PVTM_STATUS1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_freq_cnt Indicates the cycle counts of the OSC_RING clock.

PVTM_STATUS2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_rnd_seed_low_bits Indicates low 32bits of the cycle count of round seed.

PVTM_STATUS3

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_rnd_seed_high_bits Indicates high 32bits of the cycle count of round seed.

PVTM_STATUS4

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_min_value PVTM minimum value

PVTM_STATUS5

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_avr_value PVTM average value

PVTM_STATUS6

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvtm_max_value PVTM maximum value

PVTM_STATUS7

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pvtm_avr_cnt PVTM average calculation current count
15:0	RO	0x0000	pvtm_cal_cnt PVTM calculation current counter

17.5 Application Notes

17.5.1 PVTM Manual mode Usage Flow

1. Enable the frequency fixed clock clk_pvtm.
2. Reset the PVTM.
3. Set pvtm_osc_en to enable the generated clock.
4. Set pvtm_osc_sel to select the clock oscillation ring.
5. Set the pvtm_cal_cnt to an appropriate value.
6. Set pvtm_start to calculate the cycles of the generated clock.
7. Wait the pvtm_freq_done is asserted, then get the value of pvtm_freq_cnt. The period OSC_RING clock is T= cal_cnt*(Period of clk_pvtm clock)/freq_cnt, the cell delay value is T/2.

17.5.2 PVTM Auto mode Usage Flow

1. Enable the frequency fixed clock clk_pvtm.
2. Reset the PVTM.
3. Set pvtm_osc_en_auto to enable the generated clock.
4. Set pvtm_osc_sel_auto to select the clock oscillation ring.
5. Set pvtm_cal_cnt_auto to an appropriate value.
6. Set pvtm_cal_period to configure all the calculation times.
7. Set pvtm_avr_period to configure the average times.
8. Set cal_done_Int_en to enable the interrupt.
9. Set pvtm_start_auto to calculate the cycles of the generated clock.
10. Wait the interrupt is asserted, then get the value of pvtm_min_value/pvtm_max_value/ pvtm_avr_value. The minimum period OSC_RING clock is T= cal_cnt_auto*(Period of clk_pvtm clock)/pvtm_min_value, the minimum cell delay value is T/2. The frequency calculation of average and maximum value is same with minimum value.

Chapter 18 PVTPLL

18.1 Overview

PVTPLL is used to monitor the chip performance variance caused by chip process, voltage and temperature, and generate a set of reference signals for adjusting the voltage of the chip.
PVTPLL supports the following features:

- A clock oscillation ring is integrated and used to generate a clock like signal (osc_clk), the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit
- A frequency counter(osc_cnt) is used to measure the frequency of 'osc_clk'
- A externally input clock (ref_clk) is used as a reference clock for detecting the frequency of 'osc_clk'
- A calculation counter uses 'ref_clk' to generate a configurable periodic timing window
- The time-counter is used to measure the frequency of 'osc_clk'
- Support for dividing the ref_clk and osc_clk
- Support for configuring the effective polarity of the voltage regulator signal 'OUT'
- Six PVTPLL are instantiated in RK3588: PVTPLL_BIGCORE0, PVTPLL_BIGCORE1, PVTPLL_LITCORE, PVTPLL_DSU, PVTPLL_GPU and PVTPLL_NPU
- PVTPLL_BIGCORE0, PVTPLL_BIGCORE1, PVTPLL_LITCORE, PVTPLL_DSU
  - Support 6 different types of inverter cell selection
- PVTPLL_GPU and PVTPLL_NPU
  - Support 2 different types of inverter cell selection
- Support 64 levels of different length inverter osc_ring selection

18.2 Block Diagram

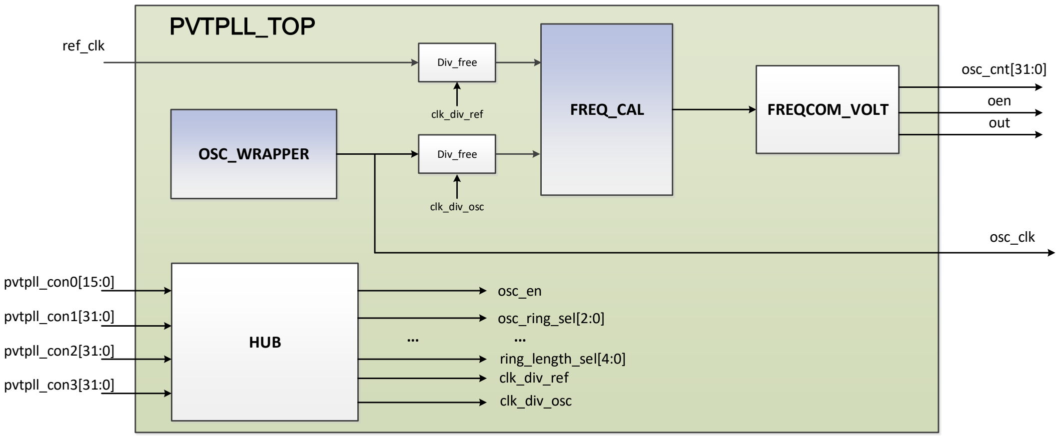

Fig. 18-1 VTPLL Block Diagram

The PVTPLL include four main blocks:
(1)OSC_RING: it is composed with inverters with odd number, which is used to generate a clock. And PVTPLL support multiple type clock oscillation ring and different length osc_ring.
(2)FREQ_CAL: it is used to measure the frequency of clock which generated from the RING_OSC block.
(3)FREQCOMP_VOLT: it is used to generate a set of reference signals for adjusting the voltage of the chip.
(4)HUB: it is used to split GRF signals into internal functional signals.

18.3 Function Description

18.3.1 Interfaces

The PVTPLL is controlled by GRF and CRU, and the monitoring results are obtained by GRF.

Table 18-1 PVTPLL Interfaces

Clock and Reset			
ref_clk	I		Reference Clock
resetn	I		LOW : active
DFT Signals			
soc_scan_mode	I		SOC scan mode control

scan_clk_pvtpll	I		Scan Clock
soc_test_mode	I		SOC test mode enable
tm_pvtpll_oen	O		Test mode
tm_pvtpll_out	O		Test mode
tm_pvtpll_osc_cnt_valid	O		Test mode
Control Signals			
pvtpll_con0[31:0]	I	pvtpll_con0[0]	pvtpll_start PVT_PLL monitor start control
		pvtpll_con0[1]	osc_en osc_ring enable
		pvtpll_con0[2]	out_polar 0: ‘out=1’ when need to increase volt 1: ‘out=0’ when need to increase volt
		pvtpll_con0[7:3]	Reserved
		pvtpll_con0[10:8]	osc_ring_sel[2:0] osc_ring channel select
		pvtpll_con0[12:11]	clk_div_ref[1:0] Frequency division factor for ref_clk
		pvtpll_con0[14:13]	clk_div_osc[1:0] Frequency division factor for osc_clk
		pvtpll_con0[15]	bypass 0: Support glitch-free frequency switching 1: Not support
		pvtpll_con0[21:16]	ring_length_sel[5:0] osc_ring inverter length select
		pvtpll_con0[31:22]	Reserved
pvtpll_con1[31:0]	I		cal_cnt[31:0] Frequency measurement period
pvtpll_con2[31:0]	I	pvtpll_con2[15:0]	threshold[15:0] Count difference threshold value
		pvtpll_con2[31:16]	ckg_val[15:0] Clk-gating interval control count value
pvtpll_con3[31:0]	I		ref_cnt[31:0] Target reference frequency value
Output Signals			
oen	O		Voltage regulation enable signal Low active
out	O		Voltage regulation indication signal
osc_cnt[31:0]	O		osc_clk counter value
osc_cnt_avg[31:0]	O		osc_clk counter average
osc_clk	O		osc_ring output clock

Table 18-2 The Registers used to control PVTPLL

PVTPLL I/O	PVTPLL_BIGCORE0/1	PVTPLL_LITCORE	PVTPLL_DSU	PVTPLL_GPU	PVTPLL_NPU
pvtpll_con0[15:0]	BIGCORE_GRF_PVTPLL_CON0_L	LITCORE_GRF_PVTPLL_CON0_L	DSU_GRF_PVTPLL_CON0_L	GPU_GRF_PVTPLL_CON0_L	NPU_GRF_PVTPLL_CON0_L
pvtpll_con0[31:16]	BIGCORE_GRF_PVTPLL	LITCORE_GRF_PVTP	DSU_GRF_PVTPL	GPU_GRF_PVTPL	NPU_GRF_PVTP

PVTPLL I/O	PVTPLL_BIGCORE0/1	PVTPLL_LITCORE	PVTPLL_DSU	PVTPLL_GPU	PVTPLL_NPU
	_CON0_H	LL_CON0_H	L_CON0_H	L_CON0_H	LL_CON0_H
pvtpll_con1[31:0]	BIGCORE_GRF_PVTPLL_CON1	LITCORE_GRF_PVTPLL_CON1	DSU_GRF_PVTPLL_CON1	GPU_GRF_PVTPLL_CON1	NPU_GRF_PVTPLL_CON1
pvtpll_con2[31:0]	BIGCORE_GRF_PVTPLL_CON2	LITCORE_GRF_PVTPLL_CON2	DSU_GRF_PVTPLL_CON2	GPU_GRF_PVTPLL_CON2	NPU_GRF_PVTPLL_CON2
pvtpll_con3[31:0]	BIGCORE_GRF_PVTPLL_CON3	LITCORE_GRF_PVTPLL_CON3	DSU_GRF_PVTPLL_CON3	GPU_GRF_PVTPLL_CON3	NPU_GRF_PVTPLL_CON3
osc_cnt[31:0]	BIGCORE_GRF_PVTPLL_STATUS0	LITCORE_GRF_PVTPLL_STATUS0	DSU_GRF_PVTPLL_STATUS0	GPU_GRF_PVTPLL_STATUS0	NPU_GRF_PVTPLL_STATUS0
osc_cnt_avg[31:0]	BIGCORE_GRF_PVTPLL_STATUS1	LITCORE_GRF_PVTPLL_STATUS1	DSU_GRF_PVTPLL_STATUS1	GPU_GRF_PVTPLL_STATUS1	NPU_GRF_PVTPLL_STATUS1

18.3.2 OSC RING

Each PVTPLL contains multiple OSC_RINGs that use different types of inverter cell. The number of OSC_RING is defined according to the requirements of each item. “osc_ring_sel[2:0]” is used to select which OSC_RING to use. The correspondence between “osc_ring_sel[2:0]” and the type of inverter cell is shown in the following table 1-2. The number of inverters in each OSC_RING can also be selected by the interface signal “ring_legth_sel[4:0]”. The correspondence between “ring_length_sel[5:0]” and the number of inverters is shown in the following table 1-3.

Table 18-3 Inverter Cell Type

Instance	osc_ring_sel	Inverter Cell Type
PVTPLL_BIGCORE0 PVTPLL_BIGCORE1 PVTPLL_LITCORE PVTPLL_DSU	0	HDBLVT20_INV_S_4
	1	HDBLVT22_INV_S_4
	2	Reserved
	3	HDBSVT22_INV_S_4
	4	HDBLVT20_INV_SHSDB_4
	5	HDBLVT22_INV_SHSDB_4
	6	Reserved
	7	HDBSVT22_INV_SHSDB_4
PVTPLL_GPU PVTPLL_NPU	0	UDBLVT20_INV_S_4
	1	UDBSVT20_INV_S_4

Table 18-4 Inverter Length Select

Instance	ring_length_sel	Number of Inverters
PVTPLL_BIGCORE0 PVTPLL_BIGCORE1 PVTPLL_LITCORE PVTPLL_DSU	0	10
	1	12
	2	14
	...	...
	n	(n+5)*2
	...	...
	61	132
	62	134
	63	136
PVTPLL_GPU PVTPLL_NPU	0	40
	1	42
	2	44
	...	...
	n	(n+20)*2
	...	...
	61	162

Instance	ring_length_sel	Number of Inverters
	62	164
	63	166

18.3.3 Frequency Measurement

'osc_clk' is generated by the internal OSC_RING. The time-counter is used to measure the frequency of 'osc_clk', and the time-counter uses ref_clk as counting clock. PVTPLL generates a signal for frequency stabilization by comparing the count values of osc_cnt and ref_cnt in the same time period.

The measurement period is configured through the interface signal cal_cnt[31:0]. At the end of each measurement period, the value of osc_cnt is equivalent to the frequency of osc_clk. The osc_cnt value is compared with the reference value ref_cnt to generate a signal(out) for external voltage regulation.

18.3.4 Voltage Regulation Signal

After starting the auto-regulation function, if osc_cnt[31:0] > (ref_cnt[31:0]+threshold[31:0]) or osc_cnt[31:0] < (ref_cnt[31:0]-threshold[31:0]), the voltage regulation enable signal 'oen' is set to 0, and the value of the voltage adjustment signal 'out' changes according to the set voltage regulation polarity signal 'out_polar', and the corresponding relationship is as shown below:

Out_polar=0: 'out=1' when need to increase voltage; 'out=0' when need to reduce voltage.

Out_polar=1: 'out=0' when need to increase voltage; 'out=1' when need to reduce voltage.

18.4 Application Notes

1. Configure osc_ring_sel and ring_length_sel.
2. Set osc_en to 1 to enable the generated clock.
3. Configure cal_cnt, ref_cnt and threshold, and set out_polar to appropriate value.
4. Set pvtpll_start to 1 to start automatic detection of the frequency and output voltage regulation signal 'out'.

Chapter 19 MIPI CSI HOST

19.1 Overview

The CSI-2 Host Controller is designed to receive data from a CSI-2 compliant camera sensor. A D-PHY configured as a Slave acts as the physical layer.
The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01.00-9 November 2010
- Interface with MIPI D-PHY v1.2/D-PHY v2.0/C-PHY v1.1
- Up to four D-PHY RX data lanes or three C-PHY RX data lanes.
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Several Frame formats
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data Type (Packet or Frame Level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- All primary and secondary data formats
  - RGB, YUV, and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
- Error detection and correction
  - PHY level
  - Packet level
  - Line level
  - Frame level
- Support DSI video mode/command mode

19.2 Block Diagram

The following diagram shows the MIPI CSI-2 Host Controller architecture.

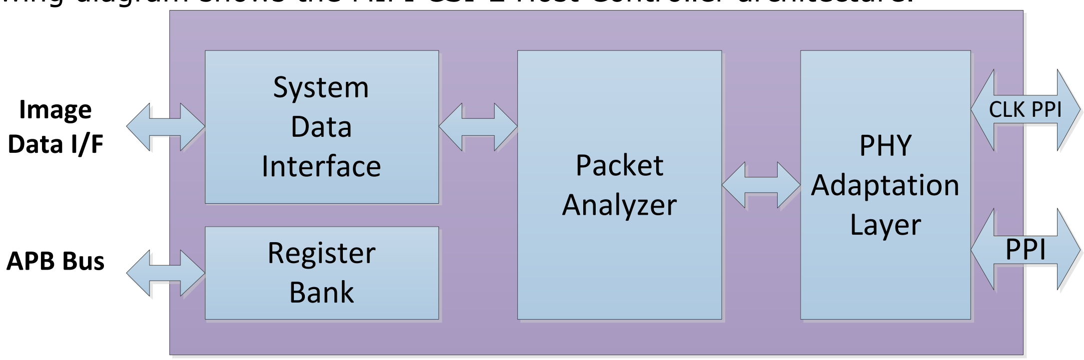

Fig. 19-1 MIPI CSI-2 Host Controller Architecture

- **PHY Adaptation Layer**: Manages the D-PHY PPI interface
- **Packet Analyzer**: Merges the data from the different lanes
- **Image Data Interface**: Reorders pixels into 32-bit data for memory storage and generates timing accurate video synchronization signals
- **AMBA-APB Register Bank**: Provides access to configuration and control registers

19.3 Function Description

19.3.1 Supported Resolutions and Frame Rates

The CSI-2 specification does not define the supported standard resolutions or frame rates. Camera sensor resolution, blanking periods, synchronization events, frame rates, and pixel color depth play a fundamental role in the required bandwidth. All these variables make it difficult to define a standard procedure to estimate the minimum lane rate and the minimum number of lanes that support a specific CSI-2 device.
Following table presents some predefined and supported camera settings, assuming the following:

- Clock lane frequency is 500 MHz or 750 MHz that results in a bandwidth of 1 Gbps or 1.5 Gbps respectively, for each data lane.
- No significant control/reserved traffic is present on the link when pixel data is being transmitted.

The last column of following table presents the minimum number of lanes required for each configuration.

Table 19-1 Supported Camera Settings

Mega Pixels	Mega Pixels with Overhead	Refresh Rate (Hz)	Color Depth (bpp)	CSI2 BW (Mbits)	D-PHY at 1 Gbps Number of Lanes	D-PHY at 1.5Gbps Number of Lanes
2MP	2560000	15	24	922	1	1
2MP	2560000	30	24	1843	2	2
3MP	3840000	15	16	922	1	1
3MP	3840000	30	16	1843	2	2
3MP	3840000	30	24	2765	3	2
5MP	6400000	15	16	1536	2	2
5MP	6400000	15	24	2304	3	2
5MP	6400000	30	16	3072	4	3
8MP	10240000	15	16	2458	3	2
8MP	10240000	15	24	3686	4	3
8MP	10240000	30	12	3686	4	3
12MP	15360000	15	12	2765	3	2
12MP	15360000	15	16	3686	4	3
14MP	17920000	15	12	3226	4	3
16MP	20480000	15	12	3686	4	3
Video Formats						
1280x720 pixels(720p)	921600	30	24	664	1	1
1280x720 pixels(720p)	921600	60	24	1327	2	1
1920x1080 pixels(1080p)	2073600	60	24	2986	3	2

19.3.2 Error Detection

The CSI-2 Host Controller analyzes the received packets and determines if there are protocol errors. It is possible to monitor the following errors:

- Frame errors such as incorrect Frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End
- Line errors such as incorrect line sequence and mismatch between Line Start and Line End
- Packet errors such as ECC or CRC mismatch
- D-PHY errors such as synchronization pattern mismatch

Following table shows all the errors that CSI-2 Host Controller can identify.

Table 19-2 Errors Identified by the CSI-2 Host Controller

Error	Description	Level	Action
phy_errsotsynchs_*	Start of transmission error on data lane* with no synchronization achieved	PHY	Packets with this error are not delivered in IDI interface
phy_erresc_*	Escape entry error (ULPM) on data lane*	PHY	Informative only. Error is acknowledged in the register and the interrupt pin is raised.
phy_errsoths_*	Start of transmission	PHY	Informative only since

	error on data lane* but synchronization can still be achieved		PHY can recover from this error. Error is acknowledged in register and the interrupt pin is raised.
vc*_err_crc	Checksum error detected on virtual channel*	Packe t	Informative only. Error is acknowledged in the register and Interrupt pin is raised.
vc*_err_crc	Header ECC contains one error detected on virtual channel*	Packe t	Informative only since controller can recover the correct header. Error is acknowledged in the register and the interrupt pin is raised.
err_ecc_double	Header ECC contains two errors. Unrecoverable.	Packe t	Packets with this error are not delivered in IDI.s
err_id_vc*	Unrecognized or unimplemented data type detected in virtual channel*	Packe t	Informative only. Error is acknowledged in the register and the interrupt pin is raised
err_f_bndry_matc h_vc*	Error matching Frame Start with Frame End for virtual channel*	Fram e	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_f_seq_vc*	Incorrect Frame Sequence detected in virtual channel*	Fram e	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_frame_data_v c*	Last received frame, in virtual channel*, had at least one CRC error	Fram e	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

19.4 Register Description

19.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI2HOST_VERSION	0x0000	W	0x00000000	Controller version identification
CSI2HOST_N_LANES	0x0004	W	0x00000000	Number of active data lanes
CSI2HOST_CSI2_RESETN	0x0010	W	0x00000000	CSI2 controller reset
CSI2HOST_PHY_STATE	0x0014	W	0x00000000	General settings for all blocks
CSI2HOST_ERR1	0x0020	W	0x00000000	Error state register 1
CSI2HOST_ERR2	0x0024	W	0x00000000	Error state register 2
CSI2HOST_MSK1	0x0028	W	0x00000000	Masks for errors 1
CSI2HOST_MSK2	0x002C	W	0x00000000	Masks for errors 2
CSI2HOST_CONTROL	0x0040	W	0x0C204000	Control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

19.4.2 Detail Registers Description

CSI2HOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	version Version of the csi2host.

CSI2HOST_N_LANES

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	n_lanes Number of active data lanes. 2'b00: 1 data lane(lane 0) 2'b01: 2 data lanes(lane0 and 1) 2'b10: 3 data lanes(lane0,1,and 2) 2'b11: 4 data lanes(ALL) Can only be updated when the D-PHY lane is in the Stop state.

CSI2HOST_CSI2_RESETN

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	csi2_resetn CSI2 controller reset output. Active low.

CSI2HOST_PHY_STATE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	bypass_2ecc_tst Payload Bypass test mode for double ECC errors.
30:15	RO	0x0000	reserved
14	RO	0x0	phy_rxactivehs_3 Lane3 high-speed receive active. Active high.
13	RO	0x0	phy_rxactivehs_2 Lane2 high-speed receive active. Active high.
12	RO	0x0	phy_rxactivehs_1 Lane1 high-speed receive active. Active high.
11	RO	0x0	phy_rxactivehs_0 Lane0 high-speed receive active. Active high.
10	RO	0x0	phy_stopstateclk Clock lane in Stop state.

Bit	Attr	Reset Value	Description
9	RO	0x0	phy_rxulpsclknot This signal indicates that the clock lane module has entered the Ultra Low Power state. Active low.
8	RO	0x0	phy_rxclkactivehs Indicates that the clock lane is actively receiving a DDR clock.
7	RO	0x0	phy_stopstatedata_3 Data lane 3 in Stop state.
6	RO	0x0	phy_stopstatedata_2 Data lane 2 in Stop state.
5	RO	0x0	phy_stopstatedata_1 Data lane 1 in Stop state.
4	RO	0x0	phy_stopstatedata_0 Data lane 0 in Stop state.
3	RO	0x0	phy_rxulpsesc_3 Lane module0 has entered the Ultra Low Power mode.
2	RO	0x0	phy_rxulpsesc_2 Lane module2 has entered the Ultra Low Power mode.
1	RO	0x0	phy_rxulpsesc_1 Lane module1 has entered the Ultra Low Power mode.
0	RO	0x0	phy_rxulpsesc_0 Lane module0 has entered the Ultra Low Power mode.

CSI2HOST_ERR1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	err_ph_crc_lane2 Packet crc error of lane2 when sw_cphy_en=1.
30	RW	0x0	err_ph_crc_lane1 Packet crc error of lane1 when sw_cphy_en=1.
29	RW	0x0	err_ph_crc_lane0 Packet crc error of lane0 when sw_cphy_en=1.
28	RO	0x0	err_ecc_double Header ECC contains 2 errors, unrecoverable.
27	RO	0x0	vc3_err_crc Checksum error detected on virtual channel 3.
26	RO	0x0	vc2_err_crc Checksum error detected on virtual channel 2.
25	RO	0x0	vc1_err_crc Checksum error detected on virtual channel 1.
24	RO	0x0	vc0_err_crc Checksum error detected on virtual channel 0.
23:16	RO	0x00	reserved

Bit	Attr	Reset Value	Description
15	RO	0x0	err_frame_data_vc3 Last received frame, in virtual channel 3, had at least one CRC error.
14	RO	0x0	err_frame_data_vc2 Last received frame, in virtual channel 2, had at least one CRC error.
13	RO	0x0	err_frame_data_vc1 Last received frame, in virtual channel 1, had at least one CRC error.
12	RO	0x0	err_frame_data_vc0 Last received frame, in virtual channel 0, had at least one CRC error.
11	RO	0x0	err_f_seq_vc3 Incorrect frame sequence detected in virtual channel 3.
10	RO	0x0	err_f_seq_vc2 Incorrect frame sequence detected in virtual channel 2.
9	RO	0x0	err_f_seq_vc1 Incorrect frame sequence detected in virtual channel 1.
8	RO	0x0	err_f_seq_vc0 Incorrect frame sequence detected in virtual channel 0.
7	RO	0x0	err_f_bndry_match_vc3 Error matching frame start with frame end for virtual channel 3.
6	RO	0x0	err_f_bndry_match_vc2 Error matching frame start with frame end for virtual channel 2.
5	RO	0x0	err_f_bndry_match_vc1 Error matching frame start with frame end for virtual channel 1.
4	RO	0x0	err_f_bndry_match_vc0 Error matching frame start with frame end for virtual channel 0.
3	RO	0x0	phy_errsotsynchs_3 Start of transmission error on data lane 3.
2	RO	0x0	phy_errsotsynchs_2 Start of transmission error on data lane 2.
1	RO	0x0	phy_errsotsynchs_1 Start of transmission error on data lane 1.
0	RO	0x0	phy_errsotsynchs_0 Start of transmission error on data lane 0(no synchronization achieved).

CSI2HOST_ERR2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	cphy_errcodehs_3 Lane 3 receive invalid code whensw_cphy_en=1.

Bit	Attr	Reset Value	Description
26	RW	0x0	cphy_errcodehs_2 Lane 2 receive invalid code whensw_cphy_en=1.
25	RW	0x0	cphy_errcodehs_1 Lane 1 receive invalid code whensw_cphy_en=1.
24	RW	0x0	cphy_errcodehs_0 Lane 0 receive invalid code whensw_cphy_en=1.
23:16	RO	0x00	reserved
15	RW	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3.
14	RW	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2.
13	RW	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1.
12	RW	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0.
11	RW	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3.
10	RW	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2.
9	RW	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1.
8	RW	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0.
7	RW	0x0	phy_errsoths_3 Start of transmission error on data lane 3(synchronization can still be achieved).
6	RW	0x0	phy_errsoths_2 Start of transmission error on data lane 2(synchronization can still be achieved).
5	RW	0x0	phy_errsoths_1 Start of transmission error on data lane 1(synchronization can still be achieved).
4	RW	0x0	phy_errsoths_0 Start of transmission error on data lane 0(synchronization can still be achieved).
3	RW	0x0	phy_erresc_3 Escape entry error(ULPM) on data lane 3.
2	RW	0x0	phy_erresc_2 Escape entry error(ULPM) on data lane 2.
1	RW	0x0	phy_erresc_1 Escape entry error(ULPM) on data lane 1.

Bit	Attr	Reset Value	Description
0	RW	0x0	phy_erresc_0 Escape entry error(ULPM) on data lane 0.

CSI2HOST_MSK1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31	RW	0x0	mask_err_ph_crc_lane2 Mask for err_ph_crc_lane2.
30	RW	0x0	mask_err_ph_crc_lane1 Mask for err_ph_crc_lane1.
29	RW	0x0	mask_err_ph_crc_lane0 Mask for err_ph_crc_lane0.
28	RW	0x0	mask_err_ecc_double Mask for err_ecc_double.
27	RW	0x0	mask_vc3_err_crc Mask for vc3_err_crc.
26	RW	0x0	mask_vc2_err_crc Mask for vc2_err_crc.
25	RW	0x0	mask_vc1_err_crc Mask for vc1_err_crc.
24	RW	0x0	mask_vc0_err_crc Mask for vc0_err_crc.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_frame_data_vc3 Mask for err_frame_data_vc3.
14	RW	0x0	mask_err_frame_data_vc2 Mask for err_frame_data_vc2.
13	RW	0x0	mask_err_frame_data_vc1 Mask for err_frame_data_vc1.
12	RW	0x0	mask_err_frame_data_vc0 Mask for err_frame_data_vc0.
11	RW	0x0	mask_err_f_seq_vc3 Mask for err_f_seq_vc3.
10	RW	0x0	mask_err_f_seq_vc2 Mask for err_f_seq_vc2.
9	RW	0x0	mask_err_f_seq_vc1 Mask for err_f_seq_vc1.
8	RW	0x0	mask_err_f_seq_vc0 Mask for err_f_seq_vc0.
7	RW	0x0	mask_err_f_bndry_match_vc3 Mask for err_f_bndry_match_vc3.
6	RW	0x0	mask_err_f_bndry_match_vc2 Mask for err_f_bndry_match_vc2.

Bit	Attr	Reset Value	Description
5	RW	0x0	mask_err_f_bndry_match_vc1 Mask for err_f_bndry_match_vc1.
4	RW	0x0	mask_err_f_bndry_match_vc0 Mask for err_f_bndry_match_vc0.
3	RW	0x0	mask_phy_errsotsynchs_3 Mask for phy_errsotsynchs_3.
2	RW	0x0	mask_phy_errsotsynchs_2 Mask for phy_errsotsynchs_2.
1	RW	0x0	mask_phy_errsotsynchs_1 Mask for phy_errsotsynchs_1.
0	RW	0x0	mask_phy_errsotsynchs_0 Mask for phy_errsotsynchs_0.

CSI2HOST_MSK2

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	mask_phy_errcodehs_3 Mask for phy_errcodehs_3.
26	RW	0x0	mask_phy_errcodehs_2 Mask for phy_errcodehs_2.
25	RW	0x0	mask_phy_errcodehs_1 Mask for phy_errcodehs_1.
24	RW	0x0	mask_phy_errcodehs_0 Mask for phy_errcodehs_0.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_id_vc3 Mask for err_id_vc3.
14	RW	0x0	mask_err_id_vc2 Mask for err_id_vc2.
13	RW	0x0	mask_err_id_vc1 Mask for err_id_vc1.
12	RW	0x0	mask_err_id_vc0 Mask for err_id_vc0.
11	RW	0x0	mask_vc3_err_ecc_corrected Mask for vc3_err_ecc_corrected.
10	RW	0x0	mask_vc2_err_ecc_corrected Mask for vc2_err_ecc_corrected.
9	RW	0x0	mask_vc1_err_ecc_corrected Mask for vc1_err_ecc_corrected.
8	RW	0x0	mask_vc0_err_ecc_corrected Mask for vc0_err_ecc_corrected.
7	RW	0x0	mask_phy_errsoths_3 Mask for phy_errsoths_3.

Bit	Attr	Reset Value	Description
6	RW	0x0	mask_phy_errsoths_2 Mask for phy_errsoths_2.
5	RW	0x0	mask_phy_errsoths_1 Mask for phy_errsoths_1
4	RW	0x0	mask_phy_errsoths_0 Mask for phy_errsoths_0.
3	RW	0x0	mask_phy_erresc_3 Mask for phy_erresc_3.
2	RW	0x0	mask_phy_erresc_2 Mask for phy_erresc_2.
1	RW	0x0	mask_phy_erresc_1 Mask for phy_erresc_1.
0	RW	0x0	mask_phy_erresc_0 Mask for phy_erresc_0.

CSI2HOST_CONTROL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RW	0x03	sw_datatype_le The datatype of line end.
25:20	RW	0x02	sw_datatype_ls The datatype of line start.
19:14	RW	0x01	sw_datatype_fe The datatype of frame end.
13:8	RW	0x00	sw_datatype_fs The datatype of frame start.
7:5	RO	0x0	reserved
4	RW	0x0	sw_dsi_en 1'b0: For csi2 1'b1: For dsi
3:1	RO	0x0	reserved
0	RW	0x0	sw_cphy_en 1'b0: For dphy 1'b1: For cphy

19.5 Application Notes

- The most important step is configuring the right CSI2HOST_N_LANES before pulling up csi_resetn. If the host is used to receive DSI data, the sw_dsi_en must be enabled, and the sw_datatype_fs, sw_datatype_fe, sw_datatype_ls, sw_datatype_le must be configured correctly. When the sw_dsi_en is enabled, those debug or error detection registers are useless.
- There are six MIPI CSI HOST in RK3588 SOC, CSI HOST0 is connected to MIPI CD Combo PHY0, CSI HOST1 is connected to MIPI CD Combo PHY1, CSI HOST2/3 are connected to MIPI DPHY0, CSI HOST4/5 are connected to MIPI DPHY1.
- When MIPI DPHY0 works in full mode, the SYS_GRF SOC_CON2[6] should be set to 0, and the CSI HOST2/3 are both connected to MIPI DPHY0 4 lanes. In this case CSI HOST3 is suggested not to use.
- When MIPI DPHY0 works in split mode, the SYS_GRF SOC_CON2[6] should be set to 1,

and CSI HOST2/3 could be connected to MIPI DPHY0 lane0/1 or lane2/3 according to the SYS_GRF SOC_CON2[8]/[9].

- When MIPI DPHY1 works in full mode, the SYS_GRF SOC_CON2[7] should be set to 0, and the CSI HOST4/5 are both connected to MIPI DPHY1 4 lanes. In this case CSI HOST5 is suggested not to use.
- When MIPI DPHY1 works in split mode, the SYS_GRF SOC_CON2[7] should be set to 1, and CSI HOST4/5 could be connected to MIPI DPHY1 lane0/1 or lane2/3 according to the SYS_GRF SOC_CON2[10]/[11].

Chapter 20 MIPI CSI DPHY

20.1 Overview

The features of MIPI CSI DPHY are as follow:

- Analog mixed-signal hard-macro LP/HS Receiver solution
- Designed to MIPI v1.2 Specifications
- Integrated PHY Protocol Interface(PPI) interfaces to DSI/CSI and UniPro MIPI protocols
- 2.5 Gbps maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 10 Gbps transfer rate
- HS-RX, LP-RX, LP-TX and Calibration supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Buffers with tunable On-Die-Termination
- Includes embedded ESD, boundary scan and BIST
- Dual clock lanes mode supported

20.2 Block Diagram

MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Figure below shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane types. The requirements for the ‘Control and Interface Logic’(CIL) function depend on the Lane type and Lane side.

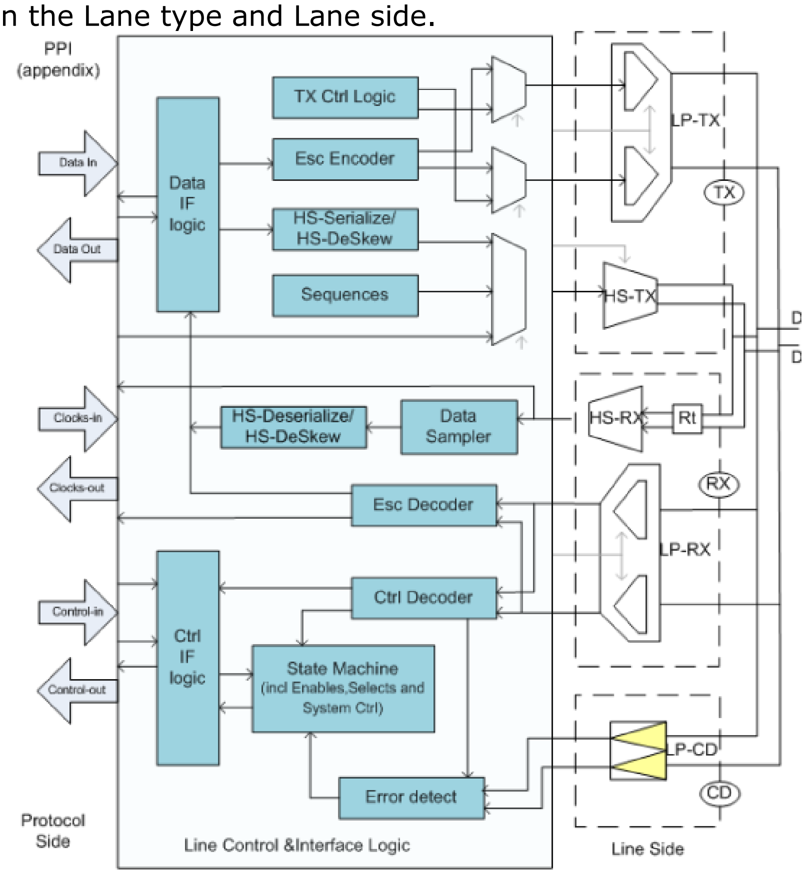

Fig. 20-1 MIPI CSI DPHY Block Diagram

20.3 Register Description

20.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI_DPHY_LANE_EN	0x0000	W	0x00000001	Clk/data lane enable
CSI_DPHY_LANE_CK1_EN	0x002C	W	0x0000001E	Clk1 lane enable

Name	Offset	Size	Reset Value	Description
CSI_DPHY_DIGITAL_CLK_PHASE	0x0034	W	0x000000C0	Digital clock phase
CSI_DPHY_LANE_CLK_3_PHASE	0x0038	W	0x00000036	Lane clock/3 phase
CSI_DPHY_LANE_2_1_0_PHASE	0x003C	W	0x000000DB	Data lane 2/1/0 phase
CSI_DPHY_DIGITAL_CLK_REVERSE	0x0048	W	0x00000010	Digital clock reverse
CSI_DPHY_DUAL_CLK_ENABLE	0x0080	W	0x0000001F	MIPI/LVDS enable
CSI_DPHY_LANE_CLK1_PHASE	0x00CC	W	0x00000030	Lane clock1 phase
CSI_DPHY_LANE_CK_MODE	0x0128	W	0x0000000F	Clock lane mode
CSI_DPHY_LANE_CK_MSB	0x0138	W	0x00000086	MSB enable
CSI_DPHY_LANE_CK_TTAGO	0x0140	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_CK_TTASURE	0x0144	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_CK_TTAWAIT	0x0148	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_CK_THSSETTLE	0x0160	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_CK_CAL_EN	0x0168	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_0_MSB	0x01B8	W	0x00000086	MSB enable
CSI_DPHY_LANE_0_TTAGO	0x01C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_0_TTASURE	0x01C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_0_TTAWAIT	0x01C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_0_THSSETTLE	0x01E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_0_CAL_EN	0x01E8	W	0x00000000	Calibration reception enable
CSI_DPHY_LANE_1_MSB	0x0238	W	0x00000086	MSB enable
CSI_DPHY_LANE_1_TTAGO	0x0240	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_1_TTASURE	0x0244	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_1_TTAWAIT	0x0248	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_1_THSSETTLE	0x0260	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_1_CAL_EN	0x0268	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_2_MSB	0x02B8	W	0x00000086	MSB enable
CSI_DPHY_LANE_2_TTAGO	0x02C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_2_TTASURE	0x02C4	W	0x00000001	The value of counter for Tta-sure of turnaround

Name	Offset	Size	Reset Value	Description
CSI_DPHY_LANE_2_TTAWAIT	0x02C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_2_THSSETTLE	0x02E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_2_CAL_EN	0x02E8	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_3_MSB	0x0338	W	0x00000086	MSB enable
CSI_DPHY_LANE_3_TTAGO	0x0340	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_3_TTASURE	0x0344	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_3_TTAWAIT	0x0348	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_3_THSSETTLE	0x0360	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_3_CAL_EN	0x0368	W	0x0000007F	Calibration reception enable
CSI_DPHY_LANE_CK1_MODE	0x03A8	W	0x00000000	Clock lane1 mode
CSI_DPHY_LANE_CK1_MSB	0x03B8	W	0x00000086	MSB enable
CSI_DPHY_LANE_CK1_TTAGO	0x03C0	W	0x00000004	The value of counter for Tta-go of turnaround
CSI_DPHY_LANE_CK1_TTASURE	0x03C4	W	0x00000001	The value of counter for Tta-sure of turnaround
CSI_DPHY_LANE_CK1_TTAWAIT	0x03C8	W	0x00000032	The value of counter for Tta-wait of turnaround
CSI_DPHY_LANE_CK1_THSSETTLE	0x03E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
CSI_DPHY_LANE_CK1_CAL_EN	0x03E8	W	0x0000007F	Calibration reception enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

20.3.2 Detail Registers Description

CSI_DPHY_LANE_EN

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_en_ck Enable D-PHY clock lane:active high.
5	RW	0x0	lane_en_3 Enable D-PHY lane3:active high.
4	RW	0x0	lane_en_2 Enable D-PHY lane2:active high.
3	RW	0x0	lane_en_1 Enable D-PHY lane1:active high.
2	RW	0x0	lane_en_0 Enable D-PHY lane0:active high.
1:0	RW	0x1	reserved Reserved

CSI_DPHY_LANE_CK1_EN

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	reserved1 Reserved
6	RW	0x0	lane_en_ck1 Enable D-PHY clock1 lane:active high.
5:0	RW	0x1e	reserved Reserved

CSI_DPHY_DIGITAL_CLK_PHASE

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x18	reserved Reserved
2:0	RW	0x0	digital_clk_phase 3'b000: Phase 0(default value) 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_LANE_CLK_3_PHASE

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x3	lane_clk_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
3:1	RW	0x3	lane_3_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
0	RW	0x0	lane_2_phase_msb See lane_2_phase for the details of the register.

CSI_DPHY_LANE_2_1_0_PHASE
Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x3	lane_2_phase {lane_2_phase_msb,lane_2_phase} 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
5:3	RW	0x3	lane_1_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
2:0	RW	0x3	lane_0_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_DIGITAL_CLK_REVERSE
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	digital_clk_reverse 1'b0: Make the digital sample clock positive(default value) 1'b1: Reverse the digital sample clock
6:0	RW	0x10	reserved Reserved

CSI_DPHY_DUAL_CLK_ENABLE
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	dual_clk_mode_en 1'b0: Enable single clock lane mode 1'b1: Enable dual clock lanes mode

Bit	Attr	Reset Value	Description
5:1	RW	0x0f	reserved Reserved
0	RW	0x1	reg_dig_rstn 1'b0: Reset 1'b1: Normal

CSI_DPHY_LANE_CLK1_PHASE
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x3	lane_clk1_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
3	RO	0x0	reserved
2:0	RW	0x0	digital_clk1_phase 3'b000: Phase 0(default value) 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

CSI_DPHY_LANE_CK_MODE
Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RW	0xf	reserved Reserved

CSI_DPHY_LANE_CK_MSB
Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_ck_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_CK_TTAGO

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_CK_TTASURE

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_CK_TTAWAIT

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_CK_THSSETTLE

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_ck_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_CK_CAL_EN

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_0_MSB

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_0_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_0_TTAGO

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x04	lane_0_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_0_TTASURE

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_0_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_0_TTAWAIT

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_0_THSSETTLE

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_0_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_0_CAL_EN

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	lane_0_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

CSI_DPHY_LANE_1_MSB

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_1_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_1_TTAGO

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_1_TTASURE

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_1_TTAWAIT

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_1_THSSETTLE

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_1_CAL_EN

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_2_MSB

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_2_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_2_TTAGO

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x04	lane_2_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_2_TTASURE

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_2_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_2_TTAWAIT

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_2_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_2_THSSETTLE

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_2_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_2_CAL_EN

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	lane_2_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_3_MSB
Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_3_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_3_TTAGO
Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_3_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_3_TTASURE
Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_3_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_3_TTAWAIT
Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_3_THSSETTLE
Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_3_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_3_CAL_EN

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_3_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

CSI_DPHY_LANE_CK1_MODE

Address: Operational Base + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck1_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RO	0x0	reserved

CSI_DPHY_LANE_CK1_MSB

Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	reserved1 Reserved
6	RW	0x0	lane_ck1_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5:0	RW	0x06	reserved Reserved

CSI_DPHY_LANE_CK1_TTAGO
Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_TTASURE
Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_TTAWAIT
Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

CSI_DPHY_LANE_CK1_THSSETTLE
Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_ck1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

CSI_DPHY_LANE_CK1_CAL_EN
Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RW	0x7f	reserved Reserved

20.4 Application Notes

20.4.1 MIPI SINGLE CLOCK LANE Mode Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.
step2: send 0x01f001f0 to register CSIDPHY_GRF_CON0.Enable the clock lane and 4 data lanes.
step3: According to data rate, write corresponding value to Ths-settle registers for lanes. If TX skew calibration function is on, send 0xff to register LANE_*_CAL_EN.

20.4.2 MIPI DUAL CLOCK LANES MODE Application

step1: send 0x7d to register CSI_DPHY_LANE_EN. Enable the D-PHY.
step2: send 0x5f to register CSI_DPHY_DUAL_CLK_ENABLE.Enable dual clock lanes mode.
step3: send 0x05f005f0 to register CSIDPHY_GRF_CON0.Enable 2 clock lanes and 4 data lanes.
step4: According to data rate, write corresponding value to Ths-settle registers for lanes. If TX skew calibration function is on, send 0xff to register LANE_*_CAL_EN.

Chapter 21 MIPI DSI-2 Host Controller

21.1 Overview

The Display Serial Interface 2 (DSI-2) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI DSI-2 Specification.
There are two DSI2 host controllers in PD_VOP subsystem, which provide an interface between the Video Output Process and MIPI D-PHY/C-PHY Combo PHY, allowing the communication with a DSI-2-compliant display.

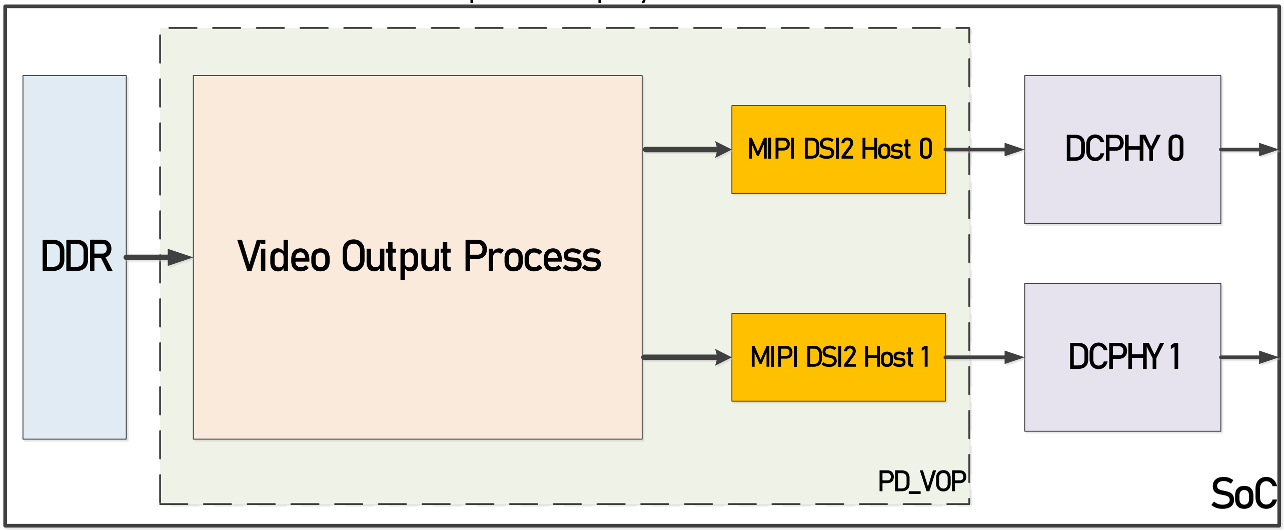

Fig. 21-1 DSI2 Host Controller In SoC

21.2 Features

- Compliant with MIPI Alliance standards
  - MIPI® Alliance Specification for Display Serial Interface 2 (DSI-2) Version 1.1
  - MIPI® Alliance Specification for Display Command Set (DCS) Version 1.4
  - MIPI® Alliance Specification for D-PHY v2.0
  - MIPI® Alliance Specification for C-PHY v1.1
  - AMBA 3.0 Specification (APB)
- Interface with MIPI D-PHY and MIPI C-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specifications
- All commands defined in the MIPI Alliance specification for Display Command Set (DCS)
  - Request of command packets through the APB interface
  - Low-power and high-speed transmission in Video, Data Stream, and Command modes
- Up to 4.5 Gbps per lane in D-PHY
- Up to 2.0 Gsps per trio in C-PHY
- Four data lanes on D-PHY and three data trios on C-PHY
- Bidirectional communication and escape mode through data lane 0
- Continuous and non-continuous clock modes on D-PHY and non-continuous clock mode on C-PHY
- Packet header ECC/CRC and packet payload CRC Checksum capabilities
- End of Transmission packet (EoTp)
- Fault recovery schemes
- Scrambling

21.2.1 Limitations

- The minimum region size (HAS,HBP,HACT,HFP) is 4 pixels
- The minimum value for the max_pix_pkt field of the IPI_PIX_PKT_CFG register should be 48 pixels. This applies to DataStream and Video Mode operating modes (except for Burst-Mode)
- Automatic Tear Effect is not supported, but can through I/O
- When changing from Video Mode, CRI busy must be cleared

● High-Speed clock period must be different from SYS clock period in the CPHY mode

21.2.2 Unsupported features

● Video pattern generator
● CPHY does not support the non-continuous clock mode
● EoTp is not supported in DataStream mode
● PRI calibration is not supported in CPHY
● PRI is not supported in CPHY

21.3 Function Description

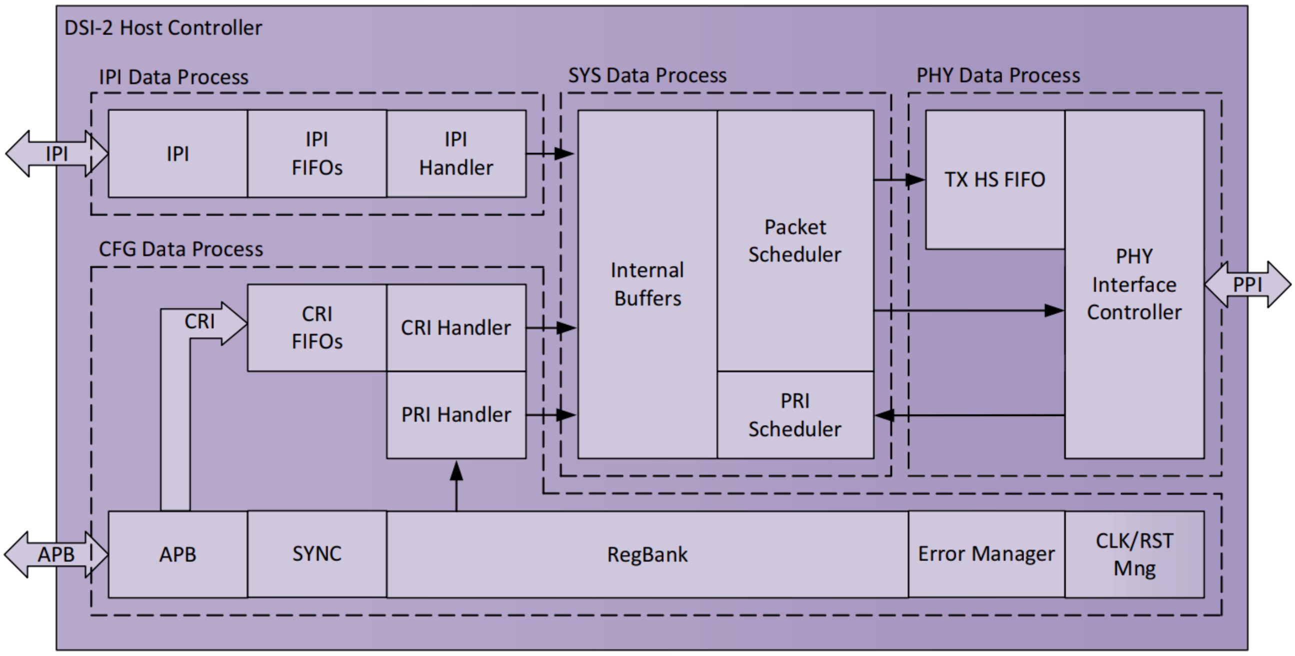

Fig. 21-2 The Architecture of MIPI DSI2 Host Controller

There are four main blocks inside MIPI DSI2 Host Controller:

● CFG Data Process
  1. Handles the AMBA APB 3 interface synchronization to sys_clk domain
  2. Stores and distributes DSI-2 Host configurations across the controller
  3. Manages clocks and resets
  4. Controls the changes between the controller operating modes and the routines for auto calculation
  5. Performs error processing
  6. Handles the CRI and PRI functional interfaces
● IPI Data Process
  1. Handles the Image Pixel Interface (IPI)
  2. Stores IPI events and IPI data into FIFOs to minimize Clock Domain Crossing (CDC) between ipi_clk and sys_clk
  3. Reorganizes IPI pixel data to DSI-2 pixel format
  4. Captures timing information
● SYS Data Process
  1. Contains the main FSMs for the different modes of operation
  2. Defines packet priorities and transmission modes
  3. Constructs the packets to be sent (header, payload, and associated ECC and CRC)
  4. Applies scrambling to the generated packets
● PHY Data Process
  1. Handles the PHY Protocol Interface (PPI)
  2. Sends high-speed data
  3. Sends and receives the low-power data
  4. Monitors PHY related timeouts

21.3.1 Controller Operating Mode

MIPI_DSI2_Host Controller has the following modes of operation:

- Idle Mode: In the Idle mode of operation
  - The controller stops data reception from the IPI, CRI, and PRI interfaces.
  - All the FIFOs are empty.
  - All the FSMs are in the INIT state.
  - There are no pending packets being transmitted or received.
- Auto-Calculation Mode: In the Auto-Calculation mode of operation, the controller
  - Stops the data reception from the IPI, CRI, and PRI interfaces.
  - Starts to calculate all the required PHY related timings.
  - Enters into the Idle mode when the procedure is complete.
- Video mode: In Video mode of operation
  - The controller accepts the IPI and CRI interfaces with IPI generating video frames.
  - The CRI interface requests are transmitted inside the video frame if there is enough time.
- Data Stream mode: In the Data Stream mode of operation, the controller
  - Accepts the IPI, CRI, and PRI interfaces with IPI generating data stream frames.
  - Prioritizes CRI over PRI and sends up to one packet from them at the end of each line from IPI.
- Command mode: In the Command mode of operation, the controller
  - Blocks the data reception from IPI.
  - Accepts CRI and PRI requests prioritizing the CRI requests

21.3.1.1 Idle Mode

Idle mode ensures that the controller is in a known and stable status with no pending packets to send, and ready to work in another operating mode. While changing the operating mode, the controller ensures that the new operating mode is preceded by the Idle mode even without explicitly requesting the Idle mode.
When an operating mode change is requested, or when Idle mode is directly requested, the controller immediately ignores any new request from the CRI and PRI interfaces, and blocks the data reception from IPI at the end of the current frame. Then, it waits until all the remaining packets from these sources are sent, and their respective FIFOs are empty. While in the Idle mode, it blocks the data reception from the IPI, CRI, and PRI interfaces, maintaining all controller FIFOs empty and all FSMs in an INIT state.

21.3.1.2 Video Mode

Video mode transmits the video frames received from IPI. These video frames are transformed in sync events and video packets. The controller attends requests from CRI or Display commands during BLLP (Blanking or low-power) region. MIPI DSI-2 protocol specifies the following video modes:

- Burst Mode
- on-Burst Mode with Sync Pulses
- on-Burst Mode with Sync Events

21.3.1.2.1 Burst Mode

In Burst mode, pixel transmission is time-compressed and the blanking regions are typically bigger. As the pixel transmission is time compressed, pixel data is sent in a single packet. The IPI_PIX_PKT_CFG register has no effect when the controller uses the Burst mode.

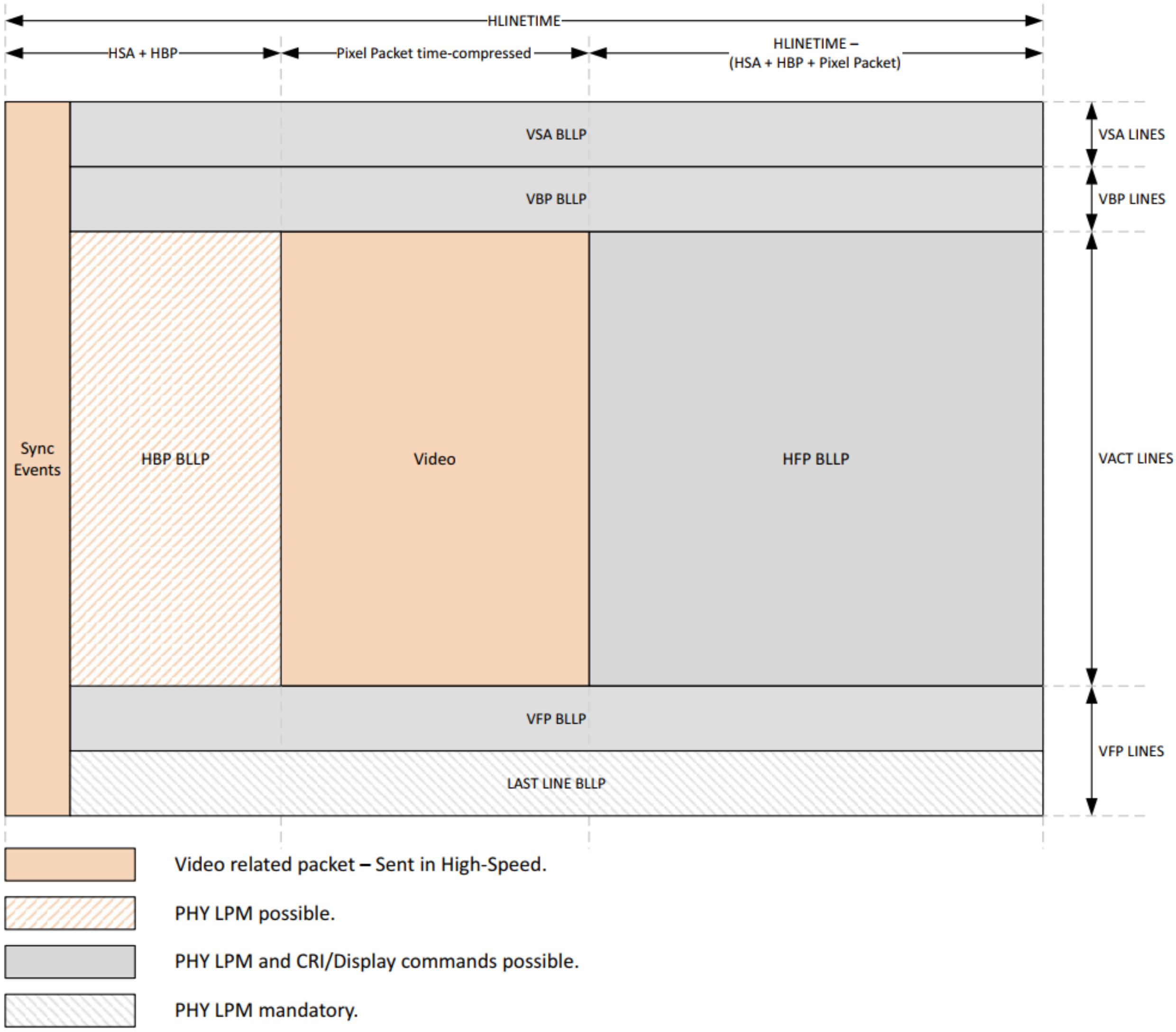

Fig. 21-3 Burst Mode Frame Behavior

21.3.1.2.2 Non-Burst Mode with Sync Pulses

Non-Burst mode with sync pulses enables the controller to accurately reconstruct original video timing and sync pulse widths. The Figure shows a DSI-2 frame transmitted in non-burst mode with sync pulses through PHY Protocol Interface (PPI).

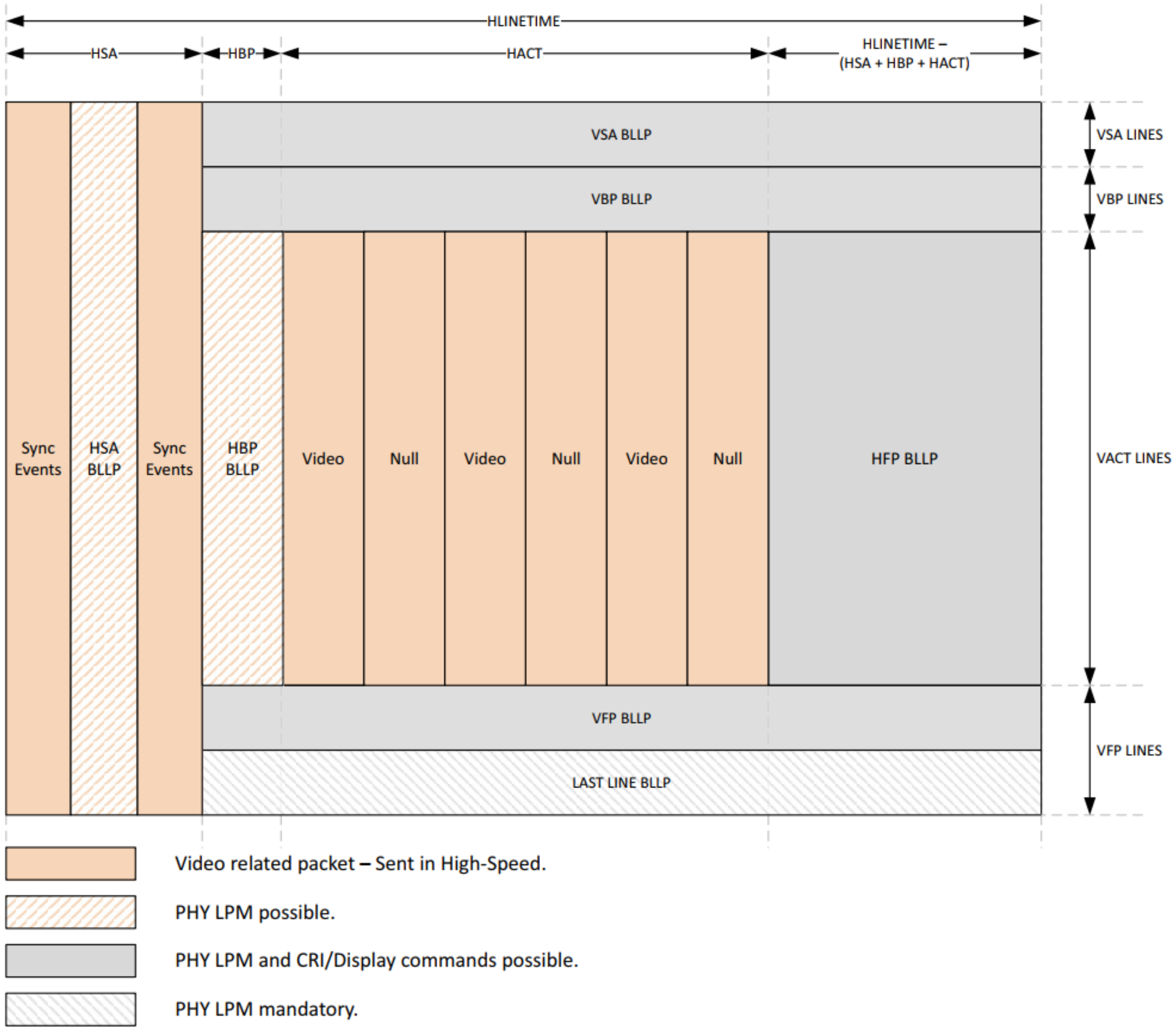

Fig. 21-4 Non-Burst With Sync Pulse Mode Frame Behavior

To adhere to the HACT timing coming from IPI interface, MIPI_DSI2_Host Controller splits the pixel stream in chunks. Each chunk is composed of a pixel packet, and an associated null packet. The number of chunks and pixel packets size depend on the programmed value in the IPI_PIX_PKT_CFG register.

21.3.1.2.3 Non-Burst Mode with Sync Events

The Non-Burst mode with sync events is similar to the Non-Burst mode with sync pulses, but accurate reconstruction of sync pulse widths is not required. The Figure shows a DSI-2 frame transmitted in non-burst mode with sync events through PHY Protocol Interface (PPI).

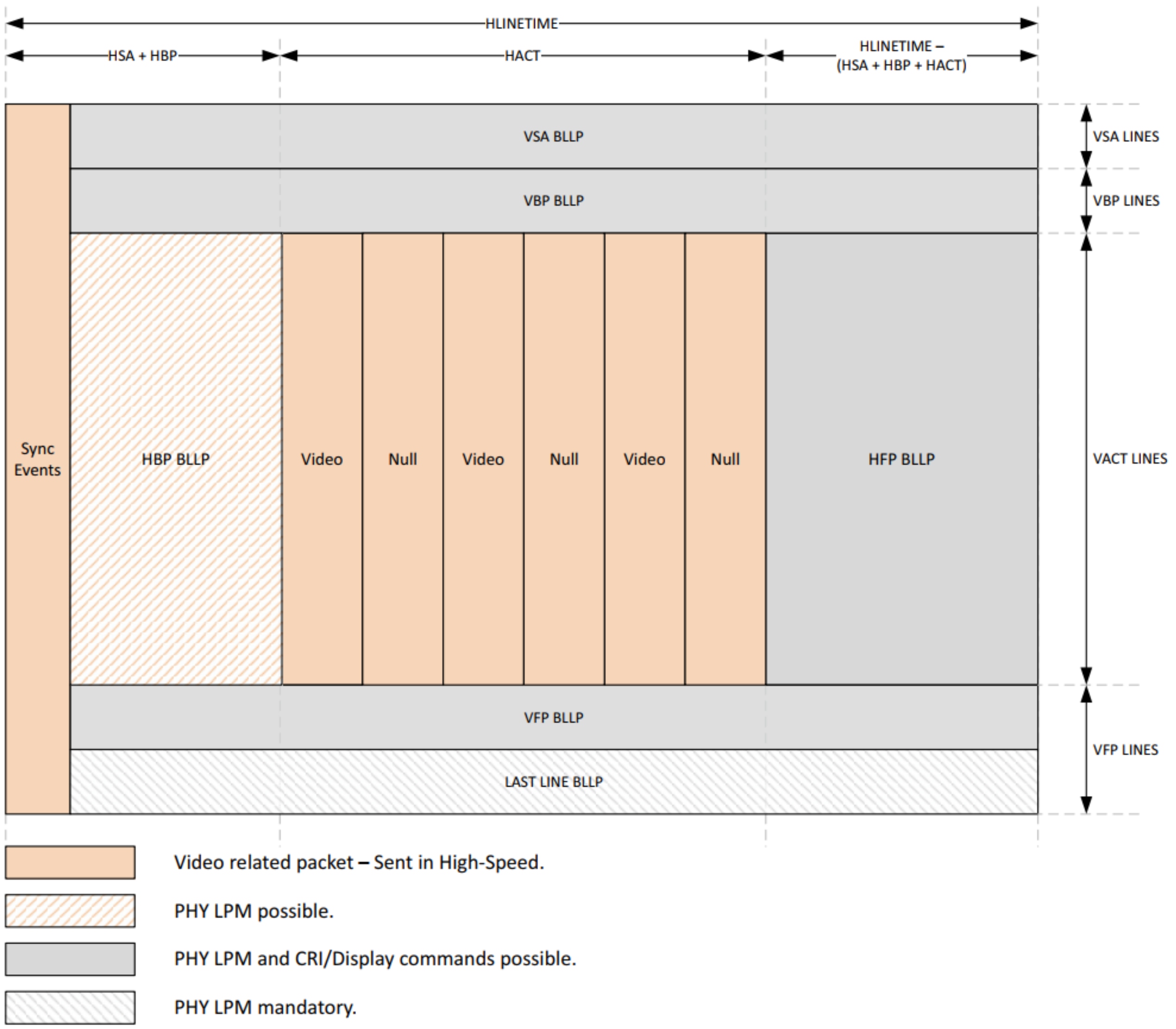

Fig. 21-5 Non-Burst With Sync Event Mode Frame Behavior

21.3.1.3 Data Stream Mode

Data Stream mode is an operating mode that transmits the data stream frames coming from IPI. These frames are transformed in DCS write packets using the Write Memory Start (WMS) and Write Memory Continue (WMC) commands, attending all pending requests from CRI or PRI after the last IPI related packet.

The controller processes the traffics in the following way:

- Start processing the IPI data stream traffic using a WMS command.
- Continue the IPI data stream traffic processing using WMC commands.
- After the last WMS/WMC command from the current frame is sent, process all pending CRI requests.
- Process all pending PRI requests

21.3.1.4 Command Mode

Command mode completely ignores IPI. The controller does not process any traffic that arrives through IPI interface. Instead, it processes requests coming from CRI or PRI interfaces on a first come, first served basis. If the requests are accumulated in the FIFOs of both interfaces, the controller prioritizes CRI traffic over PRI requests.

21.3.2 DSI-2 Options

MIPI_DSI2_Host Controller has a subset of programmable values related to the DSI-2 protocol.

MIPI_DSI2_Host Controller supports the following features:

- Virtual Channels
- Scrambling
- Video Transmission

- Device Compliance

21.3.2.1 Virtual Channels

To be able to transmit or receive packets, MIPI_DSI2_Host controller must be programmed with the virtual channel identifier. Use the DSI_VCID_CFG register:

- To program a virtual channel identifier for all transmitted packets
- To identify the read-back packets to process
- For CRI packet transmissions, virtual channel identifier is programmed in the virtual_channel field of the CRI_TX_HDR register and virtual channel for responses is made available in the virtual_channel field of the CRI_RX_HDR register

21.3.2.2 Scrambling

Data scrambling can be used to mitigate the effects of electromagnetic interferences on the transmissions using a data randomization technique described in DSI-2 specification. Scrambling is applied only on the data payload, and the footer of long packets transmitted in high speed.

Scrambling can be enabled through the DSI_SCRAMBLING_CFG[0] bit. By default, scrambling seed is 0xFFFF as recommended in DSI-2 specification. This value can be changed using the SI_SCRAMBLING_CFG [31:16] bits.

21.3.2.3 Video Transmission

In the Video mode, the transmission of video frames and related details can be programmed through the DSI_VID_TX_CFG register. The vid_mode_type field of the DSI_VID_TX_CFG register controls the video mode transmission type, between burst, non-burst with sync pulses, and non-burst with sync events. This originates different packet sequences in PPI, as described in DSI-2 specification, to precisely replicate the characteristics of each horizontal region. With respect to the horizontal active region data and timing:

- In Burst mode, the controller creates just one video packet which is sent as soon as possible.
- In Non-burst mode, the controller creates multiple video packets, interlacing each one with a null packet as per the IPI_PIX_PKT_CFG register programming.

The size of the null packets is calculated such that the duration of the horizontal active region is preserved in PPI as well.

The controller follows the defined behavior for each video region when the controller has no packets to send. The controller tries to go in low-power (if time allows) unless the option to fill that region with Blanking packets is set.

Display commands mentioned in DSI-2 specification (Turn On, Turn Off, Color Mode On, and Color Mode Off) can be programmed to be transmitted in low-power.

21.3.2.4 Device Compliance

To match the compatibility requirements of the coupled DSI-2 Device, MIPI_DSI2_Host Controller enables or disables some general features. This ensures that both Host and Device can communicate effectively. Following are the features that can be programmed through the DSI_GENERAL_CFG register:

- BTA enable: Determines whether the controller should send Bus Turnaround requests or disable them.
- EoTp transmission: Determines whether the controller should send EoTp in high-speed or not sent at all.

21.3.2.5 DSI-2 Host Controller Timeouts

MIPI_DSI2_Host Controller allows the configuration of several configurable timeouts. All timeouts are measured using phy_lptx_clk. Because it is a clock divided from sys_clk, it is always available to the controller.

When a given timeout period is violated, an interrupt will be triggered in INT_ST_TO register to inform which timeout is breached.

The timeouts measurement on the PPI interface can be divided in three main categories: high-speed transmission, low-power data transmission, and Turnaround.

21.3.3 Debug Capabilities

FIFOs control and status, and FSMs control and status are available through AMBA APB 3 interface to identify the possible error scenarios.

21.3.3.1 FIFO Control and Status

The status of the various FIFOs present on MIPI_DSI2_Host Controller can be read for debug purposes through the OBS_FIFO_STATUS register. This register reports one of the following statuses:

- Empty
- Almost empty - two positions from empty
- Half full
- Almost full - two positions from full
- Full
- Current Word Count

Manual FIFO flush control is provided through the OBS_FIFO_CTRL register, and automatic FIFO flush control is provided using the OBS_FIFO_CFG register.

21.3.3.2 FSM Control and Status

The status of the main FSM present on MIPI_DSI2_Host Controller can be read for debug purposes through the OBS_FSM_STATUS register. This register reports the following statuses:

- Current state
- Previous state
- Current state counter: Counts the number of cycles in the current state

Manual FSM initialization control is provided through the OBS_FSM_CTRL register, and automatic FSM initialization control is provided through the OBS_FSM_CFG register.

21.4 Register Description

21.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DSI2_CORE_ID	0x0000	W	0x3130302A	Core identification represented in ASCII
DSI2_VERSION	0x0004	W	0x1A020100	Core version number
DSI2_PWR_UP	0x000C	W	0x00000000	Controls the power up of the core
DSI2_SOFT_RESET	0x0010	W	0x00000007	Controls the soft-reset of individual parts of the IP
DSI2_INT_ST_MAIN	0x0014	W	0x00000000	Contains the status of individual interrupt sources
DSI2_MODE_CTRL	0x0018	W	0x00000000	Controller operating mode change request
DSI2_MODE_STATUS	0x001C	W	0x00000000	Controller operating mode status
DSI2_CORE_STATUS	0x0020	W	0x00000000	Core status
DSI2_MANUAL_MODE_CFG	0x0024	W	0x00000000	Manual mode for setting all timings.
DSI2_OBS_FSM_STATUS_SEL	0x0028	W	0x00000000	FSM selection for status reporting and debug
DSI2_OBS_FSM_STATUS	0x002C	W	0x00000000	Status of the selected FSM
DSI2_OBS_FSM_CFG	0x0030	W	0x00000000	Controls automatic FSM re-initialization options
DSI2_OBS_FSM_CTRL	0x0034	W	0x00000000	Controls manual FSM re-initialization options in case of an FSM stuck.
DSI2_OBS_FIFO_STATUS_SEL	0x0038	W	0x00000000	FIFO selection for status reporting and debugging
DSI2_OBS_FIFO_STATUS	0x003C	W	0x00000000	Status of the selected FSM
DSI2_OBS_FIFO_CFG	0x0040	W	0x00000000	Controls automatic FSM re-initialization options
DSI2_OBS_FIFO_CTRL	0x0044	W	0x00000000	Manual FIFOs flush

Name	Offset	Size	Reset Value	Description
DSI2_TIMEOUT_HSTX_CFG	0x0048	W	0x00000000	Configures the counter for high-speed TX timeout
DSI2_TIMEOUT_HSTXRDY_CFG	0x004C	W	0x00000000	Configures the counter for high-speed TX Ready timeout
DSI2_TIMEOUT_LPRX_CFG	0x0050	W	0x00000000	Configures the counter for low power RX timeout
DSI2_TIMEOUT_LPTXRDY_CFG	0x0054	W	0x00000000	Configures the counter for low-power TX DATA timeout
DSI2_TIMEOUT_LPTXTRIG_CFG	0x0058	W	0x00000000	Configures the counter for low power TX TRIGGER timeout
DSI2_TIMEOUT_LPTXULPS_CFG	0x005C	W	0x00000000	Configures the counter for low power TX ULPS timeout
DSI2_TIMEOUT_BTA_CFG	0x0060	W	0x00000000	Configures the counter for bus turnaround direction timeout
DSI2_PHY_MODE_CFG	0x0100	W	0x00000030	Configures the PHY interface
DSI2_PHY_CLK_CFG	0x0104	W	0x00000000	Configures the clock running type, and the division factor of the phy_lptx_clk clock
DSI2_PHY_STATUS	0x0108	W	0x00000000	Reports the status of PHY
DSI2_PHY_LP2HS_MAN_CFG	0x010C	W	0x00000000	Configures PHY transition time from low-power to high-speed transmission
DSI2_PHY_LP2HS_AUTO_CFG	0x0110	W	0x00000000	Reports measured value for PHY transition time from low-power to high-speed transmission
DSI2_PHY_HS2LP_MAN_CFG	0x0114	W	0x00000000	Configures PHY transition time from low-power to high-speed transmission
DSI2_PHY_HS2LP_AUTO_CFG	0x0118	W	0x00000000	Reports measured value for PHY transition time from low-power to high-speed transmission
DSI2_PHY_MAX_RD_T_MAN_CFG	0x011C	W	0x00000000	Configures the maximum read time
DSI2_PHY_MAX_RD_T_AUTO	0x0120	W	0x00000000	Reports the maximum read time, when in auto-mode
DSI2_PHY_ESC_CMD_T_MAN_CFG	0x0124	W	0x00000000	Configures PHY trigger time
DSI2_PHY_ESC_CMD_T_AUTO	0x0128	W	0x00000000	Reports PHY trigger time, when in auto-mode
DSI2_PHY_ESC_BYTE_T_MAN_CFG	0x012C	W	0x00000000	Configures PHY trigger time
DSI2_PHY_ESC_BYTE_T_AUTO	0x0130	W	0x00000000	Reports PHY trigger time, when in auto-mode
DSI2_PHY_IPI_RATIO_MAN_CFG	0x0134	W	0x00000000	Configures ratio between frequencies of HSTX clock and IPI clock
DSI2_PHY_IPI_RATIO_MAN_AUTO	0x0138	W	0x00000000	Reports the calculated ratio between frequencies of HSTX clock and IPI clock
DSI2_PHY_SYS_RATIO_MAN_CFG	0x013C	W	0x00000000	Configures ratio between frequencies of HSTX clock and SYS clock.

Name	Offset	Size	Reset Value	Description
DSI2_PHY_SYS_RATIO_MAN_AUTO	0x0140	W	0x00000000	Reports the calculated ratio between frequencies of HSTX clock and SYS clock
DSI2_PRI_TX_CMD	0x01C0	W	0x00000000	This register is used for transmitting all available PHY requests
DSI2_PRI_RX_CMD	0x01C4	W	0x00000000	This register contains calibration required time
DSI2_PRI_CAL_CTRL	0x01C8	W	0x00000000	This register contains calibration required time
DSI2_PRI_ULPS_CTRL	0x01CC	W	0x00000000	This register defines different modes for ULPS entry and exit
DSI2_DSI_GENERAL_CFG	0x0200	W	0x00000000	Configures the general options to meet the characteristics of the peripheral.
DSI2_DSI_VCID_CFG	0x0204	W	0x00000000	Configures the virtual channel for transmission
DSI2_DSI_SCRAMBLING_CFG	0x0208	W	0xFFFF0000	Configures data scrambling
DSI2_DSI_VID_TX_CFG	0x020C	W	0x00000000	Configures the video transmission options
DSI2_DSI_MAX_RPS_CFG	0x0210	W	0x00000000	Configures the maximum payload size that a received packet can contain
DSI2_CRI_TX_HDR	0x02C0	W	0x00000000	Header for packets to be sent in command mode
DSI2_CRI_TX_PLD	0x02C4	W	0x00000000	Payload for packets to be sent in command mode
DSI2_CRI_RX_HDR	0x02C8	W	0x00000000	Header of packets received from device side
DSI2_CRI_RX_PLD	0x02CC	W	0x00000000	Payload of packets received from device side
DSI2_IPI_COLOR_MAN_CFG	0x0300	W	0x00000000	Configures the color coding for the IPI interface in manual mode
DSI2_IPI_VID_HSA_MAN_CFG	0x0304	W	0x00000000	Configures the Horizontal Sync Active period
DSI2_IPI_VID_HSA_AUTO	0x0308	W	0x00000000	Reports the Horizontal Sync Active period, when in auto-mode
DSI2_IPI_VID_HBP_MAN_CFG	0x030C	W	0x00000000	Configures the Horizontal Back Porch period
DSI2_IPI_VID_HBP_AUTO	0x0310	W	0x00000000	Reports the Horizontal back porch period, when in auto-mode
DSI2_IPI_VID_HACT_MAN_CFG	0x0314	W	0x00000000	Configures the Horizontal Active line time HACT
DSI2_IPI_VID_HACT_AUTO	0x0318	W	0x00000000	Reports the Horizontal Active period, when in auto-mode
DSI2_IPI_VID_HLINE_MAN_CFG	0x031C	W	0x00000000	Configures the total line time
DSI2_IPI_VID_HLINE_AUTO	0x0320	W	0x00000000	Reports the total line time, when in auto-mode
DSI2_IPI_VID_VSA_MAN_CFG	0x0324	W	0x00000000	Configures the Vertical Sync Active period

Name	Offset	Size	Reset Value	Description
DSI2_IPI_VID_VSA_AUTO	0x0328	W	0x00000000	Reports the Vertical Sync Active period in auto-mode
DSI2_IPI_VID_VBP_MAN_CFG	0x032C	W	0x00000000	Configures the Vertical Back Porch period
DSI2_IPI_VID_VBP_AUTO	0x0330	W	0x00000000	Reports the Vertical Back Porch period in auto-mode
DSI2_IPI_VID_VACT_MAN_CFG	0x0334	W	0x00000000	Configures the Vertical Active region period
DSI2_IPI_VID_VACT_AUTO	0x0338	W	0x00000000	Reports the Vertical Active region period when in auto-mode
DSI2_IPI_VID_VFP_MAN_CFG	0x033C	W	0x00000000	Configures the Vertical Front Porch period
DSI2_IPI_VID_VFP_AUTO	0x0340	W	0x00000000	Reports the Vertical Front Porch period in auto-mode
DSI2_IPI_PIX_PKT_CFG	0x0344	W	0x00000000	Configures the number of pixels per packet
DSI2_INT_ST_PHY	0x0400	W	0x00000000	Groups the interrupt sources related to PHY
DSI2_INT_MASK_PHY	0x0404	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_PHY	0x0408	W	0x00000000	Forces the interrupt sources of the INT_ST_PHY register
DSI2_INT_ST_TO	0x0410	W	0x00000000	Groups the interrupt sources related to PHY
DSI2_INT_MASK_TO	0x0414	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_TO	0x0418	W	0x00000000	Forces the interrupt sources of the INT_ST_PHY register
DSI2_INT_ST_ACK	0x0420	W	0x00000000	Groups the interrupt sources related to Acknowledge and Error Report packet
DSI2_INT_MASK_ACK	0x0424	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_ACK register
DSI2_INT_FORCE_ACK	0x0428	W	0x00000000	Forces the interrupt sources of the INT_ST_ACK register
DSI2_INT_ST_IPI	0x0430	W	0x00000000	Groups the interrupt sources related to IPI
DSI2_INT_MASK_IPI	0x0434	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_IPI	0x0438	W	0x00000000	Forces the interrupt sources of the INT_ST_IPI register
DSI2_INT_ST_FIFO	0x0440	W	0x00000000	Groups the interrupt sources related to FIFOs
DSI2_INT_MASK_FIFO	0x0444	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_FIFO register
DSI2_INT_FORCE_FIFO	0x0448	W	0x00000000	Forces the interrupt sources of the INT_ST_FIFO register
DSI2_INT_ST_PRI	0x0450	W	0x00000000	Groups the interrupt sources related to PRI

Name	Offset	Size	Reset Value	Description
DSI2_INT_MASK_PRI	0x0454	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_PHY register
DSI2_INT_FORCE_PRI	0x0458	W	0x00000000	Forces the interrupt sources of the INT_ST_PRI register
DSI2_INT_ST_CRI	0x0460	W	0x00000000	Groups the interrupt sources related to CRI
DSI2_INT_MASK_CRI	0x0464	W	0x00000000	Configures masks for the interrupt sources of the INT_ST_CRI register
DSI2_INT_FORCE_CRI	0x0468	W	0x00000000	Forces the interrupt sources of the INT_ST_CRI register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.4.2 Detail Registers Description

DSI2_CORE_ID

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x3130302a	core_id Core identification. Byte-wise representation of ASCII characters containing the version of the IP.

DSI2_VERSION

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x1a020100	core_version Core version number.

DSI2_PWR_UP

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pwr_up Configures the core either to power-up or to reset. 1'b0: Reset 1'b1: Power-up

DSI2_SOFT_RESET

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x1	sys_rstn Soft-reset for SYS data process. Active low and used synchronously.
1	RW	0x1	phy_rstn Soft-reset for PHY data process. Active low and used synchronously.
0	RW	0x1	ipi_rstn Soft-reset for IPI data process. Active low and used synchronously.

DSI2_INT_ST_MAIN

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RC	0x0	int_st_cri Status of the INT_ST_CRI register
5	RC	0x0	int_st_pri Status of the INT_ST_PRI register
4	RC	0x0	int_st_fifo Status of the INT_ST_FIFO register
3	RC	0x0	int_st_ipi Status of the INT_ST_IPI register
2	RC	0x0	int_st_ack Status of the INT_ST_DSI register
1	RC	0x0	int_st_to Status of the INT_ST_TO register
0	RC	0x0	int_st_phy Status of the INT_ST_PHY register

DSI2_MODE_CTRL

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	mode_ctrl Requested operating mode: 3'b000: Idle mode 3'b001: AutoCalculation mode 3'b010: Command mode 3'b011: Video mode 3'b100: Data Stream mode Others: Reserved

DSI2_MODE_STATUS

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	mode_status Current operating mode: 3'b000: Idle mode 3'b001: AutoCalculation mode 3'b010: Command mode 3'b011: Video mode 3'b100: Data Stream mode Others: Reserved

DSI2_CORE_STATUS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	pri_rd_data_avail PRI has new read data available.
25	RO	0x0	pri_fifos_not_empty At least one PRI WR FIFO is not empty.
24	RO	0x0	pri_busy PRI interface is busy: - At least one PRI FIFO is not empty - [or] At least one PRI packet is being transmitted or processed.
23:19	RO	0x00	reserved

Bit	Attr	Reset Value	Description
18	RO	0x0	cri_rd_data_avail CRI has new read data available.
17	RO	0x0	cri_fifos_not_empty At least one CRI WR FIFO is not empty.
16	RO	0x0	cri_busy Command Interface is busy: - At least one CRI FIFO (internal and external) is not empty - [or] At least one CRI packet is being transmitted or processed.
15:10	RO	0x00	reserved
9	RO	0x0	ipi_fifos_not_empty At least one IPI FIFO (internal and external) is not empty.
8	RO	0x0	ipi_busy Image Pixel Interface is busy: - At least one IPI FIFO (internal and external) is not empty - [or] At least one IPI packet is being transmitted or processed.
7:2	RO	0x00	reserved
1	RO	0x0	core_fifos_not_empty At least one FIFO (internal and external) is not empty.
0	RO	0x0	core_busy mipidsi2_host is busy: - At least one FIFO (internal and external) is not empty - [or] At least one packet is being transmitted or processed.

DSI2_MANUAL_MODE_CFG

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	manual_mode_en Enables manual mode for setting all timings. When unset, timings are automatically calculated by measuring times and lines in the next frame. When set, all timing parameters need to be programmed through the register bank.

DSI2_OBS_FSM_STATUS_SEL

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	fsm_selector FSM selection for reporting and debugging. Current word count of the selected FSM: 4'b0000: ipi_vid_fsm 4'b0001: ipi_auto_calc_fsm 4'b0010: sys_main_fsm 4'b0011: sys_cmd_fsm 4'b0100: sys_pkt_build_fsm 4'b0101: phy_tx_ready_fsm Others: Reserved

DSI2_OBS_FSM_STATUS

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	current_state_cnt Number of clock cycles that the FSM has been in this state.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RO	0x00	previous_state Previous state.
7:6	RO	0x0	reserved
5	RO	0x0	stuck Flag to indicate that the FSM is stuck.
4:0	RO	0x00	current_state Current state.

DSI2_OBS_FSM_CFG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fsm0_auto_init Enables automatic re-initialization of FSM 0.

DSI2_OBS_FSM_CTRL

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fsm0_auto_init Manual re-initialization of FSM 0.

DSI2_OBS_FIFO_STATUS_SEL

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	fsm_selector FIFO selection for reporting and debugging. Current status of the selected FIFO: 4'b0000: cmd_rd_pld_fifo 4'b0001: cmd_wr_hdr_fifo 4'b0010: cmd_wr_pld_fifo 4'b0011: ipi_data_fifo 4'b0100: ipi_event_fifo 4'b0101: phy_txhs_fifo Others: Reserved

DSI2_OBS_FIFO_STATUS

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	current_word_count Current word count of the selected FIFO.
15:5	RO	0x000	reserved
4	RO	0x0	full Indicates that the selected FIFO is full.
3	RO	0x0	almost_full Indicates that the selected FIFO is almost full
2	RO	0x0	half_full Indicates that the selected FIFO is half full.
1	RO	0x0	almost_empty Indicates that the selected FIFO is almost empty.
0	RO	0x0	empty Indicates that the selected FIFO is empty.

DSI2_OBS_FIFO_CFG

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ipi_fifo_auto_flush Enables automatic flush for the IPI FIFO.
2	RW	0x0	cmd_wr_hdr_fifo_auto_flush Enables automatic flush for the cmd_wr_hdr FIFO.
1	RW	0x0	cmd_wr_pld_fifo_auto_flush Enables automatic flush for the cmd_wr_pld FIFO.
0	RW	0x0	cmd_rd_pld_fifo_auto_flush Enables automatic flush for the cmd_rd_pld FIFO.

DSI2_OBS_FIFO_CTRL

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ipi_fifo_maual_flush Enables manual flush for the IPI FIFO.
2	RW	0x0	cmd_wr_hdr_fifo_maual_flush Enables manual flush for the cmd_wr_hdr FIFO.
1	RW	0x0	cmd_wr_pld_fifo_maual_flush Enables manual flush for the cmd_wr_pld FIFO.
0	RW	0x0	cmd_rd_pld_fifo_maual_flush Enables manual flush for the cmd_rd_pld FIFO.

DSI2_TIMEOUT_HSTX_CFG

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_hstx_value Configures the counter that triggers a high-speed transmission timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_HSTXRDY_CFG

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_hstxrdy_value Configures the counter that triggers a high-speed transmission ready timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_LPRX_CFG

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_lprxrdy_value Configures the counter that triggers a low-power reception timeout (measured in phy_lptx_clk cycles).

DSI2_TIMEOUT_LPTXRDY_CFG

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	to_lptxrdy_value Configures the counter that triggers a low-power data transmission timeout (measured in phy_lptx_clk cycles).

DSI2_TIMEOUT_LPTXTRIG_CFG

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_lptxtrig_value Configures the counter that triggers a low-power trigger transmission timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_LPTXULPS_CFG

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_lptxulps_value Configures the counter that triggers a low-power ULPS entry timeout (measured in phy_lptx_clk cycles)

DSI2_TIMEOUT_BTA_CFG

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	to_bta_value Configures the counter that triggers a bus turnaround direction timeout (measured in phy_lptx_clk cycles)

DSI2_PHY_MODE_CFG

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	ppi_width 2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits 2'b11: Reserved
7:6	RO	0x0	reserved
5:4	RW	0x3	phy_lanes Configures the number of active lanes. 2'b00: 1 lane 2'b01: 2 lanes 2'b10: 3 lanes 2'b11: 4 lanes
3:1	RO	0x0	reserved
0	RW	0x0	phy_type Configures which PHY interface to be used: 1'b0: DPHY 1'b1: CPHY

DSI2_PHY_CLK_CFG

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x00	phy_lptx_clk_div Division factor for TX Escape clock to be generated from sys_clk. 5'b00000: phy_lptx_clk turned off 5'b00001: phy_lptx_clk = sys_clk / 2 5'b00010: phy_lptx_clk = sys_clk / 4 5'b00011: phy_lptx_clk = sys_clk / 6 ... 5'b11111: phy_lptx_clk = sys_clk / 62
7:1	RO	0x00	reserved
0	RW	0x0	clk_type Configures the behavior of the clock lane: 1'b0: Continuous clock 1'b1: Non-continuous clock

DSI2_PHY_STATUS

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	phy_l3_ulpsactivenot Indicates the status of the phy_l3_ulpsactivenot signal.
19	RW	0x0	phy_l2_ulpsactivenot Indicates the status of the phy_l2_ulpsactivenot signal.
18	RW	0x0	phy_l1_ulpsactivenot Indicates the status of the phy_l1_ulpsactivenot signal.
17	RW	0x0	phy_l0_ulpsactivenot Indicates the status of the phy_l0_ulpsactivenot signal.
16	RW	0x0	phy_clk_ulpsactivenot Indicates the status of the phy_clk_ulpsactivenot signal.
15:13	RO	0x0	reserved
12	RW	0x0	phy_l3_stopstate Indicates the status of the phy_l3_stopstate signal.
11	RW	0x0	phy_l2_stopstate Indicates the status of the phy_l2_stopstate signal.
10	RW	0x0	phy_l1_stopstate Indicates the status of the phy_l1_stopstate signal.
9	RW	0x0	phy_l0_stopstate Indicates the status of the phy_l0_stopstate signal.
8	RW	0x0	phy_clk_stopstate Indicates the status of the phy_clk_stopstate signal.
7:1	RO	0x00	reserved
0	RW	0x0	phy_direction Indicates the status of the phy_direction signal. 1'b0: TX 1'b1: RX

DSI2_PHY_LP2HS_MAN_CFG

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_lp2hs_time Configures the time measured in cycles of phy_hstx_clk that is necessary for PHY to switch any clock or data lane from low-power to high-speed transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_LP2HS_AUTO_CFG
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	phy_lp2hs_time_auto Indicates the time measured by the controller in cycles of phy_hstx_clk that PHY takes to switch any clock or data lane from low-power to high-speed transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_HS2LP_MAN_CFG
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_hs2lp_time Configures the time measured by the controller in cycles of phy_hstx_clk that PHY takes to switch any clock or data lane from high-speed to low-power transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_HS2LP_AUTO_CFG
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	phy_hs2lp_time_auto Indicates the time measured by the controller in cycles of phy_hstx_clk that PHY takes to switch any clock or data lane from high-speed to low-power transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_MAX_RD_T_MAN_CFG
Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	phy_max_rd_time Configures the time measured in cycles of phy_hstx_clk that is necessary for receiving a response packet of maximum size. Note that if there is the possibility that an "Acknowledge and Error Report" and/or an EoTp come together with the packet of max size, this value need to reflect the time that is needed to receive them all. This is an integer value (no fractional bits)

DSI2_PHY_MAX_RD_T_AUTO
Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	phy_max_rd_time_auto Indicates the time measured in cycles of phy_hstx_clk that is necessary for receiving a response packet of maximum size. Note that if there is the possibility that an "Acknowledge and Error Report" and/or an EoTp come together with the packet of max size, this value need to reflect the time that is needed to receive them all. This is an integer value (no fractional bits)

DSI2_PHY_ESC_CMD_T_MAN_CFG

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_esc_cmd_time Configures the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit an escape mode command. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_ESC_CMD_T_AUTO

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	phy_esc_cmd_time_auto Indicates the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit an escape mode command. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_ESC_BYTE_T_MAN_CFG

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	phy_esc_byte_time Configures the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit a byte in low-power data transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_ESC_BYTE_T_AUTO

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	phy_esc_byte_time_auto Indicates the time measured in cycles of phy_hstx_clk that is necessary for the PHY to transmit a byte in low-power data transmission. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_PHY_IPI_RATIO_MAN_CFG

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	phy_ipi_ratio Configures the ratio calculated as HSTX clock frequency / IPI clock frequency. This is a fixed-point value with 6 integral bits and 16 fractional bits

DSI2_PHY_IPI_RATIO_MAN_AUTO

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:0	RO	0x000000	phy_ipi_ratio_auto Indicates the ratio calculated as HSTX clock frequency / IPI clock frequency. This is a fixed-point value with 6 integral bits and 16 fractional bits

DSI2_PHY_SYS_RATIO_MAN_CFG
Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	phy_sys_ratio Configures Ratio calculated as HSTX clock frequency / SYS clock frequency. This is a fixed-point value with 1 integral bit and 16 fractional bits.

DSI2_PHY_SYS_RATIO_MAN_AUTO
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	phy_sys_ratio_auto Ratio calculated as HSTX clock frequency / SYS clock frequency. This is a fixed-point value with 1 integral bit and 16 fractional bits.

DSI2_PRI_TX_CMD
Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	W1C	0x0	phy_bta Enables PHY bus turnaround request.
15:14	RO	0x0	reserved
13	W1C	0x0	phy_ulps_exit Enables PHY ULPS exit request. Note that this request is valid only if the previous one was a phy_ulps_entry, and if it was successfully transmitted.
12	W1C	0x0	phy_ulps_entry Enables PHY ULPS entry request. Note that two consecutives phy_ulps_entry requests (and when first is successful sent by controller) will result in an interrupt.
11:9	RO	0x0	reserved
8	W1C	0x0	phy_cal Enables PHY calibration request
7:4	RO	0x0	reserved
3	W1C	0x0	phy_tx_trigger_3 Requests sending a trigger 3
2	W1C	0x0	phy_tx_trigger_2 Requests sending a trigger 2
1	W1C	0x0	phy_tx_trigger_1 Requests sending a trigger 1
0	W1C	0x0	phy_tx_trigger_0 Requests sending a trigger 0

DSI2_PRI_RX_CMD
Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RC	0x0	phy_rx_trigger_3 This bit indicates that a trigger 3 has been received.
2	RC	0x0	phy_rx_trigger_2 This bit indicates that a trigger 2 has been received.
1	RC	0x0	phy_rx_trigger_1 This bit indicates that a trigger 1 has been received.
0	RC	0x0	phy_rx_trigger_0 This bit indicates that a trigger 0 has been received.

DSI2_PRI_CAL_CTRL

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	phy_cal_time Time needed to complete deskew calibration, given in cycles of sys_clk.

DSI2_PRI_ULPS_CTRL

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	phy_wakeup_time Configures the PHY wakeup time that controller will consider when performing an ULPS exit request. This time is measured in cycles of phy_lptx_clk and shall represent at least 1 ms, to meet the twakeup time requirement found in D-PHY and C-PHY specifications.
15:5	RO	0x000	reserved
4	RW	0x0	phy_ulps_clk_lane ULPS request command is active for the clock lane
3:1	RO	0x0	reserved
0	RW	0x0	phy_ulps_data_lanes ULPS request command is active for all active data lanes

DSI2_DSI_GENERAL_CFG

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	bta_en Enables Bus Turn Around (BTA) procedures.
0	RW	0x0	eotp_tx_en Enables the EoTp transmission in high-speed.

DSI2_DSI_VCID_CFG

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	tx_vcid Identifies virtual channel for transmitted packets.

DSI2_DSI_SCRAMBLING_CFG

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0xffff	scrambling_seed Scrambling seed.
15:1	RO	0x0000	reserved
0	RW	0x0	scrambling_en Scrambling enable.

DSI2_DSI_VID_TX_CFG

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	lpdt_display_cmd_en Enables the transmission of commands to be done only in low-power mode.
19:15	RO	0x00	reserved
14	RW	0x0	blk_vfp_hs_en Enables filling the VFP period with blanking packets. If unset and time allows, controller returns to the low-power mode
13	RW	0x0	blk_vbp_hs_en Enables filling the VBP period with blanking packets. If unset and time allows, controller returns to the low-power mode
12	RW	0x0	blk_vsa_hs_en Enables filling the VSA period with blanking packets. If unset and time allows, controller returns to the low-power mode
11:7	RO	0x00	reserved
6	RW	0x0	blk_hfp_hs_en Enables filling the HFP period with blanking packets. If unset and time allows, controller returns to the low-power mode
5	RW	0x0	blk_hbp_hs_en Enables filling the HBP period with blanking packets. If unset and time allows, controller returns to the low-power mode
4	RW	0x0	blk_hsa_hs_en Enables filling the HSA period with blanking packets. If unset and time allows, controller returns to the low-power mode
3:2	RO	0x0	reserved
1:0	RW	0x0	vid_mode_type Configures the video mode transmission type. 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events Others: Burst mode

DSI2_DSI_MAX_RPS_CFG

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	max_rt_pkt_sz Maximum payload size that a received packet can contain, in bytes.

DSI2_CRI_TX_HDR

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29	WO	0x0	cmd_hdr_long Configures the packet as a long packet. This is used only when the programmed data type is a reserved value
28	WO	0x0	cmd_hdr_rd Configures the packet as a read request command. This is used only when the programmed data type is a reserved value.
27:25	RO	0x0	reserved
24	WO	0x0	cmd_tx_mode Configures the transmission mode of the packet. 1'b0: High-speed transmission 1'b1: Low-power transmission
23:16	WO	0x00	wc_msb Configures the most significant byte for the word count field of long packets, or data 1 for short packets.
15:8	WO	0x00	wc_lsb Configures the least significant byte for the word count field of long packets, or data 0 for short packets.
7:6	WO	0x0	virtual_channel Configures the virtual channel for the packet.
5:0	WO	0x00	data_type Configures the data type for the packet.

DSI2_CRI_TX_PLD
Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	byte_3 The fourth byte of current word of payload.
23:16	WO	0x00	byte_2 The third byte of current word of payload.
15:8	WO	0x00	byte_1 The second byte of current word of payload.
7:0	WO	0x00	byte_0 The first byte of current word of payload.

DSI2_CRI_RX_HDR
Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RC	0x00	wc_msb The most significant byte for the word count field of long packets, or data 1 for short packets.
15:8	RC	0x00	wc_lsb The least significant byte for the word count field of long packets, or data 0 for short packets.
7:6	RC	0x0	virtual_channel The virtual channel for the packet.
5:0	RC	0x00	data_type The data type for the packet.

DSI2_CRI_RX_PLD
Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	byte_3 The fourth byte of current word of payload.

Bit	Attr	Reset Value	Description
23:16	RO	0x00	byte_2 The third byte of current word of payload.
15:8	RO	0x00	byte_1 The second byte of current word of payload.
7:0	RO	0x00	byte_0 The first byte of current word of payload.

DSI2_IPI_COLOR_MAN_CFG
Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ipi_depth Configures the IPI color depth. 4'b0010: 5-6-5 bits 4'b0011: 6 bits 4'b0101: 8 bits 4'b0110: 10 bits Others: Reserved
3:0	RW	0x0	ipi_format Configures the IPI pixel format. 4'b0000: RGB 4'b1011: Compressed Data Others: Reserved

DSI2_IPI_VID_HSA_MAN_CFG
Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	vid_hsa_time Configures the Horizontal Sync Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HSA_AUTO
Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	vid_hsa_time_auto Horizontal Sync Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HBP_MAN_CFG
Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	vid_hbp_time Configures the Horizontal Back Porch period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HBP_AUTO
Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	vid_hbp_time_auto Horizontal Sync Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HACT_MAN_CFG

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	vid_hact_time Configures the Horizontal Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HACT_AUTO

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	vid_hact_time_auto Horizontal Active period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_HLINE_MAN_CFG

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vid_hline_time Configures the total line time (HSA+HBP+HACT+HFP) measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits

DSI2_IPI_VID_HLINE_AUTO

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	vid_hline_time_auto Total line period measured in cycles of phy_hstx_clk. This is a fixed-point value with 13 integral bits and 16 fractional bits.

DSI2_IPI_VID_VSA_MAN_CFG

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vid_vsa_lines Configures the Vertical Sync Active period measured in lines.

DSI2_IPI_VID_VSA_AUTO

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	vid_vsa_lines_auto Vertical Sync Active period measured in lines, as seen by the controller.

DSI2_IPI_VID_VBP_MAN_CFG

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vid_vbp_lines Configures the Vertical Back Porch measured in lines.

DSI2_IPI_VID_VBP_AUTO

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	vid_vbp_lines_auto Vertical Back Porch period measured in lines, as seen by the controller.

DSI2_IPI_VID_VACT_MAN_CFG

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	vid_vact_lines Configures the Vertical Active period measured in lines.

DSI2_IPI_VID_VACT_AUTO

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	vid_vsa_lines_auto Vertical Active period measured in lines, as seen by the controller.

DSI2_IPI_VID_VFP_MAN_CFG

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	vid_vfp_lines Configures the Vertical Front Porch period measured in lines.

DSI2_IPI_VID_VFP_AUTO

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	vid_vfp_lines_auto Vertical Front Porch period measured in lines, as seen by the controller.

DSI2_IPI_PIX_PKT_CFG

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	max_pix_pkt Configures the number of pixels in a single video packet, used in Video mode (for non-burst modes) and Data Stream mode. A value of 0 or bigger than the HACT pixels will originate one single video packet per line, in Video mode. For RGB-10bit color coding, this value must be a multiple of 4.

DSI2_INT_ST_PHY

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	err_phy0 Error PHY 0

DSI2_INT_MASK_PHY

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	mask_err_phy0 Write 1 to unmask each error report.

DSI2_INT_FORCE_PHY

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	force_err_phy0 Force Error PHY 0

DSI2_INT_ST_TO

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RC	0x0	err_to_bta Indicates that a bus turnaround direction timeout has occurred.
5	RC	0x0	err_to_lptxulps Indicates that a low-power TX ULPS timeout has occurred.
4	RC	0x0	err_to_lptxtrig Indicates that a low-power TX TRIGGER timeout has occurred.
3	RC	0x0	err_to_lptxrdy Indicates that a low-power TX DATA timeout has occurred.
2	RC	0x0	err_to_lprx Indicates that a low-power RX timeout has occurred.
1	RC	0x0	err_to_hstxrdy Indicates that a high-speed TX RDY timeout has occurred.
0	RC	0x0	err_to_hstx Indicates that a high-speed TX timeout has occurred.

DSI2_INT_MASK_TO

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	mask_err_to_bta Write 1 to unmask this error report.
5	RW	0x0	mask_err_to_lptxulps Write 1 to unmask this error report.
4	RW	0x0	mask_err_to_lptxtrig Write 1 to unmask this error report.
3	RW	0x0	mask_err_to_lptxrdy Write 1 to unmask this error report.
2	RW	0x0	mask_err_to_lprx Write 1 to unmask this error report.
1	RW	0x0	mask_err_to_hstxrdy Write 1 to unmask this error report.

Bit	Attr	Reset Value	Description
0	RW	0x0	mask_err_to_hstx Write 1 to unmask this error report.

DSI2_INT_FORCE_TO

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	W1C	0x0	force_err_to_bta Forces the interrupt sources
5	W1C	0x0	force_err_to_lptxulps Forces the interrupt sources
4	W1C	0x0	force_err_to_lptxtrig Forces the interrupt sources
3	W1C	0x0	force_err_to_lptxrdy Forces the interrupt sources
2	W1C	0x0	force_err_to_lprx Forces the interrupt sources
1	W1C	0x0	force_err_to_hstxrdy Forces the interrupt sources
0	W1C	0x0	force_err_to_hstx Forces the interrupt sources

DSI2_INT_ST_ACK

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RC	0x0	err_ack_rpt_15 Retrieves the DSI Protocol Violation error bit from the Acknowledge error report.
14	RC	0x0	err_ack_rpt_14 Retrieves the Reserved (specific to device) error bit from the Acknowledge error report.
13	RC	0x0	err_ack_rpt_13 Retrieves the Invalid Transmission Length error bit from the Acknowledge error report.
12	RC	0x0	err_ack_rpt_12 Retrieves the DSI VC ID Invalid error bit from the Acknowledge error report.
11	RC	0x0	err_ack_rpt_11 Retrieves the DSI Data Type not recognized error bit from the Acknowledge error report.
10	RC	0x0	err_ack_rpt_10 Retrieves the Payload Checksum error bit (long packet only) from the Acknowledge error report.
9	RC	0x0	err_ack_rpt_9 Retrieves the header ECC/SSDC/Checksum multi-bit (detected, not corrected) error bit from the Acknowledge error report.
8	RC	0x0	err_ack_rpt_8 Retrieves the header ECC/SSDC/Checksum single-bit (detected and corrected) error bit from the Acknowledge error report.
7	RC	0x0	err_ack_rpt_7 Retrieves the Contention Detected error bit from the Acknowledge error report.

Bit	Attr	Reset Value	Description
6	RC	0x0	err_ack_rpt_6 Retrieves the False Control error bit from the Acknowledge error report.
5	RC	0x0	err_ack_rpt_5 Retrieves the Peripheral Timeout error bit from the Acknowledge error report.
4	RC	0x0	err_ack_rpt_4 Retrieves the Low-Power Transmit Sync error bit from the Acknowledge error report.
3	RC	0x0	err_ack_rpt_3 Retrieves the Escape Mode Entry Command error bit from the Acknowledge error report.
2	RC	0x0	err_ack_rpt_2 Retrieves the EoT Sync error bit from the Acknowledge error report.
1	RC	0x0	err_ack_rpt_1 Retrieves the SoT Sync error bit from the Acknowledge error report.
0	RC	0x0	err_ack_rpt_0 Retrieves the SoT error bit from the Acknowledge error report.

DSI2_INT_MASK_ACK

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	mask_err_ack_rpt_15 Write 1 to unmask this error report.
14	RW	0x0	mask_err_ack_rpt_14 Write 1 to unmask this error report.
13	RW	0x0	mask_err_ack_rpt_13 Write 1 to unmask this error report.
12	RW	0x0	mask_err_ack_rpt_12 Write 1 to unmask this error report.
11	RW	0x0	mask_err_ack_rpt_11 Write 1 to unmask this error report.
10	RW	0x0	mask_err_ack_rpt_10 Write 1 to unmask this error report.
9	RW	0x0	mask_err_ack_rpt_9 Write 1 to unmask this error report.
8	RW	0x0	mask_err_ack_rpt_8 Write 1 to unmask this error report.
7	RW	0x0	mask_err_ack_rpt_7 Write 1 to unmask this error report.
6	RW	0x0	mask_err_ack_rpt_6 Write 1 to unmask this error report.
5	RW	0x0	mask_err_ack_rpt_5 Write 1 to unmask this error report.
4	RW	0x0	mask_err_ack_rpt_4 Write 1 to unmask this error report.
3	RW	0x0	mask_err_ack_rpt_3 Write 1 to unmask this error report.
2	RW	0x0	mask_err_ack_rpt_2 Write 1 to unmask this error report.

Bit	Attr	Reset Value	Description
1	RW	0x0	mask_err_ack_rpt_1 Write 1 to unmask this error report.
0	RW	0x0	mask_err_ack_rpt_0 Write 1 to unmask this error report.

DSI2_INT_FORCE_ACK

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	W1C	0x0	force_err_ack_rpt_15 Force err_ack_rpt_015
14	W1C	0x0	force_err_ack_rpt_14 Force err_ack_rpt_14
13	W1C	0x0	force_err_ack_rpt_13 Force err_ack_rpt_13
12	W1C	0x0	force_err_ack_rpt_12 Force err_ack_rpt_12
11	W1C	0x0	force_err_ack_rpt_11 Force err_ack_rpt_11
10	W1C	0x0	force_err_ack_rpt_10 Force err_ack_rpt_10
9	W1C	0x0	force_err_ack_rpt_9 Force err_ack_rpt_9
8	W1C	0x0	force_err_ack_rpt_8 Force err_ack_rpt_8
7	W1C	0x0	force_err_ack_rpt_7 Force err_ack_rpt_7
6	W1C	0x0	force_err_ack_rpt_6 Force err_ack_rpt_6
5	W1C	0x0	force_err_ack_rpt_5 Force err_ack_rpt_5
4	W1C	0x0	force_err_ack_rpt_4 Force err_ack_rpt_4
3	W1C	0x0	force_err_ack_rpt_3 Force err_ack_rpt_3
2	W1C	0x0	force_err_ack_rpt_2 Force err_ack_rpt_2
1	W1C	0x0	force_err_ack_rpt_1 Force err_ack_rpt_1
0	W1C	0x0	force_err_ack_rpt_0 Force err_ack_rpt_0

DSI2_INT_ST_IPI

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RC	0x0	err_display_cmd_ovfl Display command request ignored by the controller due to internal buffer overflow.
1	RC	0x0	err_display_cmd_time Display command request ignored by the controller due to timing.

Bit	Attr	Reset Value	Description
0	RC	0x0	err_ipi_dtype No DSI-2 data type is a direct match for the choice made by the pair ipi_format and ipi_depth. Data is captured and delivered as for Packed Pixel Stream, 24-bit forma.

DSI2_INT_MASK_IPI
Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	mask_err_display_cmd_ovfl Write 1 to unmask this error report.
1	RW	0x0	mask_err_display_cmd_time Write 1 to unmask this error report.
0	RW	0x0	mask_err_ipi_dtype Write 1 to unmask this error report.

DSI2_INT_FORCE_IPI
Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	force_err_display_cmd_ovfl force err_display_cmd_ovfl
1	W1C	0x0	force_err_display_cmd_time force err_display_cmd_time
0	W1C	0x0	force_err_ipi_dtype force err_ipi_dtype

DSI2_INT_ST_FIFO
Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	err_phy0 Groups the interrupt sources related to FIFOs.

DSI2_INT_MASK_FIFO
Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	mask_err_phy0 Write 1 to unmask FIFOs error report.

DSI2_INT_FORCE_FIFO
Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RC	0x0	force_err_phy0 Force FIFOs Error.

DSI2_INT_ST_PRI
Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RC	0x0	err_pri_tx_time PRI request ignored due to timing error (Video Mode only).

Bit	Attr	Reset Value	Description
0	RC	0x0	err_pri_tx_cmd PHY request cannotbe attended and will be discarded.

DSI2_INT_MASK_PRI

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RC	0x0	mask_err_pri_tx_time Write 1 to unmask FIFOs error report.
0	RC	0x0	mask_err_pri_tx_cmd Write 1 to unmask FIFOs error report.

DSI2_INT_FORCE_PRI

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RC	0x0	force_err_pri_tx_time force err_pri_tx_time
0	RC	0x0	force_err_pri_tx_cmd force err_pri_tx_cmd

DSI2_INT_ST_CRI

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RC	0x0	err_cri_rpt_6 CRI request ignored due to timing error (Video Mode only).
15:14	RO	0x0	reserved
13	RC	0x0	err_cri_rpt_5 CRI received packet length invalid.
12	RC	0x0	err_cri_rpt_4 CRI received packet header invalid virtual channel.
11	RC	0x0	err_cri_rpt_3 CRI received packet header invalid data type
10	RC	0x0	err_cri_rpt_2 CRI received long packet CRC error
9	RC	0x0	err_cri_rpt_1 CRI received packet header fatal ECC error
8	RC	0x0	err_cri_rpt_0 CRI received packet header single ECC error
7:0	RO	0x00	reserved

DSI2_INT_MASK_CRI

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	mask_err_cri_rpt_6 Write 1 to unmask this error report.
15:14	RO	0x0	reserved
13	RW	0x0	mask_err_cri_rpt_5 Write 1 to unmask this error report.
12	RW	0x0	mask_err_cri_rpt_4 Write 1 to unmask this error report.

Bit	Attr	Reset Value	Description
11	RW	0x0	mask_err_cri_rpt_3 Write 1 to unmask this error report.
10	RW	0x0	mask_err_cri_rpt_2 Write 1 to unmask this error report.
9	RW	0x0	mask_err_cri_rpt_1 Write 1 to unmask this error report.
8	RW	0x0	mask_err_cri_rpt_0 Write 1 to unmask this error report.
7:0	RO	0x00	reserved

DSI2_INT_FORCE_CRI
Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	force_err_cri_rpt_6 Forces err_cri_cmd_time
15:14	RO	0x0	reserved
13	RW	0x0	force_err_cri_rpt_5 Forces err_cri_invalid_rx_length
12	RW	0x0	force_err_cri_rpt_4 Forces err_cri_invalid_vc
11	RW	0x0	force_err_cri_rpt_3 Forces err_cri_invalid_dt
10	RW	0x0	force_err_cri_rpt_2 Forces err_cri_crc
9	RW	0x0	force_err_cri_rpt_1 Forces err_cri_ecc_fatal
8	RW	0x0	force_err_cri_rpt_0 Forces err_cri_ecc
7:0	RO	0x00	reserved

21.5 Application Notes

21.5.1 System-level Interaction

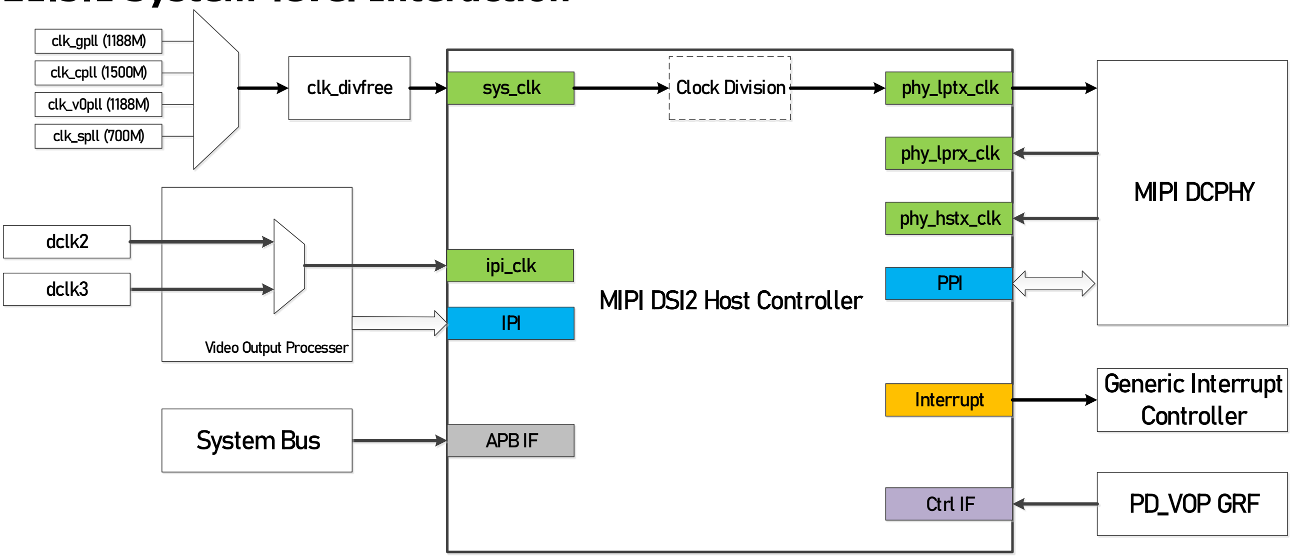

Fig. 21-6 System Level Overview

21.5.1.1 Clock

- **ipi_clk**: Image Pixel Interface clock. It's generated in VOP internal clock generation unit, used to synchronize IPI sync and pixel data.
- **sys_clk**: Always On system core clock. Used for phy_lptx_clk generation. Should be the

clock with the highest frequency inside DSI2 host controller. It could be configured the source and frequency by *CRU_CLKSEL_CON114* and *CRU_CLKSEL_CON115* register in CRU block. The default frequency of sys_clk = 350Mhz selecting clk_spll source and clk_divfree = 1.

- **phy_hstx_clk**: The PHY High-Speed Transmit Word Clock. The frequency of phy_hstx_clk is dependent upon the PPI width, which is fixed to 16 bits in DCPHY, so in DPHY mode, the High-Speed Transmit Word Clock (phy_hstx_clk) is exactly 1/16 the Lane high-speed data rate; In CPHY mode, the High-Speed Transmit Word Clock (phy_hstx_clk) is exactly 1/7 the trio high speed symbol rate.
- **phy_lptx_clk**: PHY low-power TX clock
- **phy_lprx_clk**: PHY low-power RX clock

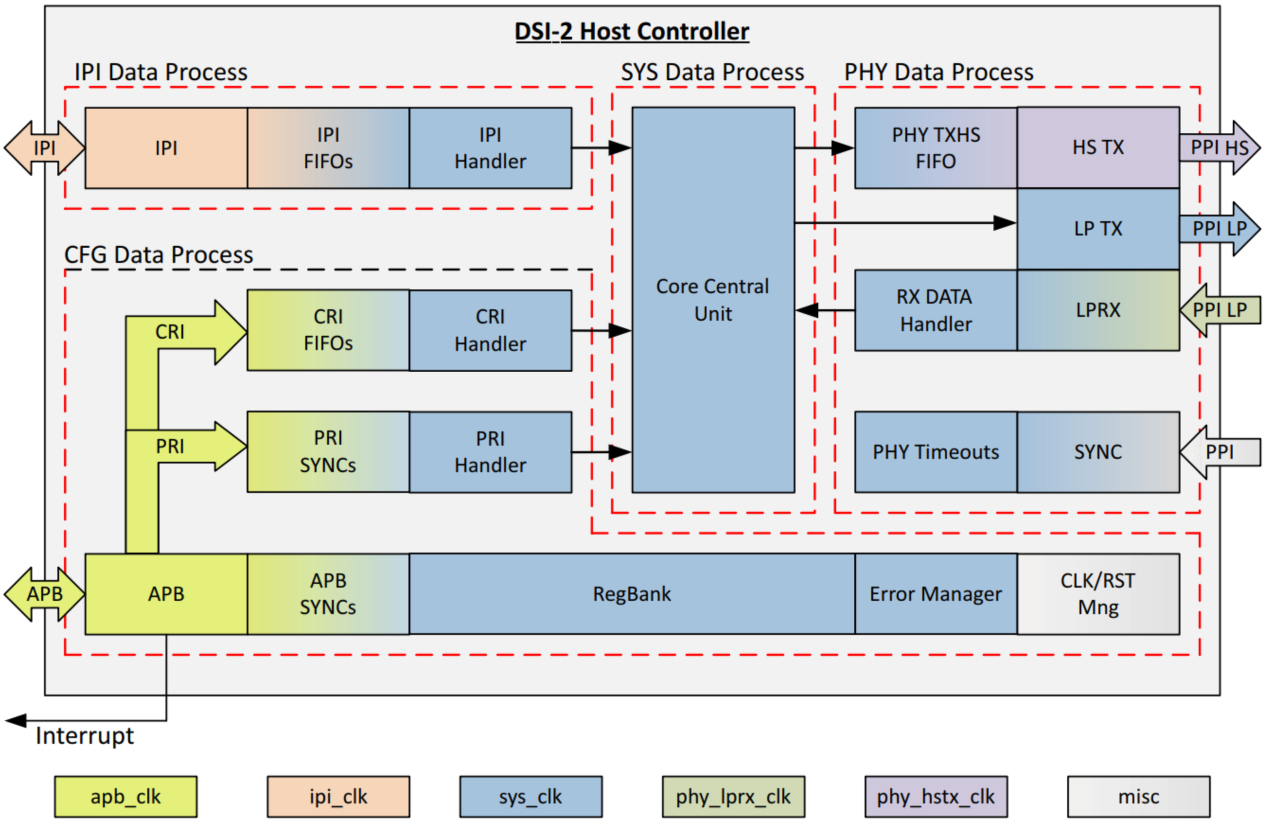

Fig. 21-7 Internal Clock Domain Architecture

21.5.1.2 AMBA APB 3 Interface

The AMBA APB 3 interface in MIPI DSI2 host controller is used to configure the controller, to control operating modes, and to obtain various statuses. The AMBA APB 3 interface is also used to complement the interrupt interface, and is a physical support for the Command Request Interface (CRI) and PHY Request Interface (PRI).

Table 21-1 DSI2 Host Controller Register Base Address

IP	Base Address
MIPI_DSI2HOST_0	0xFDE20000
MIPI_DSI2HOST_1	0xFDE30000

21.5.1.3 Interrupt Interface

There is a single interrupt pin connected to the GIC.

Table 21-2 DSI2 Host Controller Interrupt Number

IP	IRQ number
MIPI_DSI2HOST_0	32+167
MIPI_DSI2HOST_1	32+168

The implementation sets the interrupt pin and the applicable Interrupt Status registers at same time. The default value of the INT_MASK_<group> (Interrupt Mask) registers is 0, and this corresponds to masking the interrupts. By default, the interrupt pin is disabled.

The INT_ST_MAIN register indicates the names of the INT_ST_<group> (Interrupt Status) registers that have triggered the interrupt. The INT_ST_<group> (Interrupt Status) registers contain the status of the individual interrupt sources, regardless of the contents of the associated INT_MASK_<group> registers. So, it is possible to service the INT_ST_<group> (Interrupt Status) registers by polling. The INT_ST_<group> (Interrupt Status) registers are cleared when read. Reading the INT_ST_MAIN register also clears the interrupt pin.
The INT_FORCE_<group> (Interrupt Force) registers are used for testing purpose. These registers allow triggering interrupt events individually, without activating the conditions that trigger the interrupt sources. This feature also facilitates the development and testing of the software associated with the interrupt events. The INT_FORCE_<group> registers are auto-cleared. The circuitry minimizes the gate count overhead because it does not need the Interrupt Force registers.

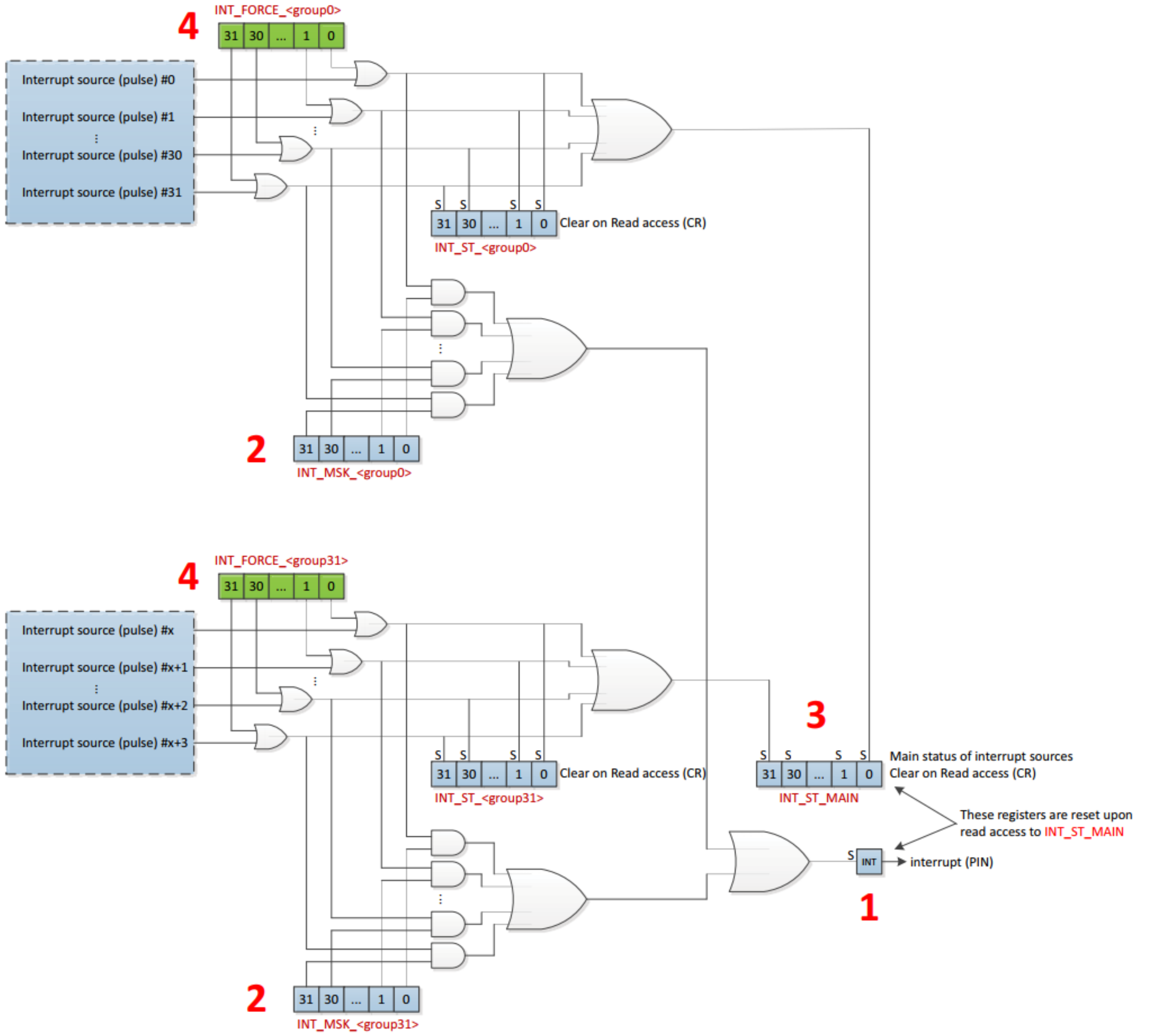

Fig. 21-8 Interrupt Structure

21.5.1.4 System Control Signals

There are some control signals configured through *VOP_GRF_VOP_CON0* and *VOP_GRF_VOP_CON1*.

Table 21-3 DSI2 Host Controller interfaced with PD_VOP GRF

Signal Name	Description
ipi_format[3:0]	IPI Pixel Format, only used when DSI2 controller operate in auto mode.
ipi_color_depth[3:0]	IPI Pixel Color Depth, only used when DSI2 controller operate in auto mode.
ipi_shutdown	IPI Shutdown command

Signal Name	Description
ipi_colormode	IPI Color Mode command
mem_clk_gating_en	Set 1 to this bit enables clock gating function of DSI2 Host memory for low power consideration.

The ipi_shutdown and ipi_colormode signals can be used to send display commands. These signals are toggle sensitive.
ipi_shutdown signal:

- When this signal rises, it corresponds to Shut Down Peripheral Command request.
- When this signal falls, it corresponds to Turn On Peripheral Command request.

ipi_colormode signal:

- When this signal rises, it corresponds to Color Mode On Command request.
- When this signal falls, it corresponds to Color Mode Off Command request.

To guarantee the order of display commands inside video frame, the following conditions should be met:

- Up to one display command request can be made per line
- Last line cannot receive display command requests
- Display command requests must occur after the HSYNC period

The transmission mode is controlled by lpdt_display_cmd_en bit from DSI_VID_TX_CFG register.

21.5.2 Programming Flow

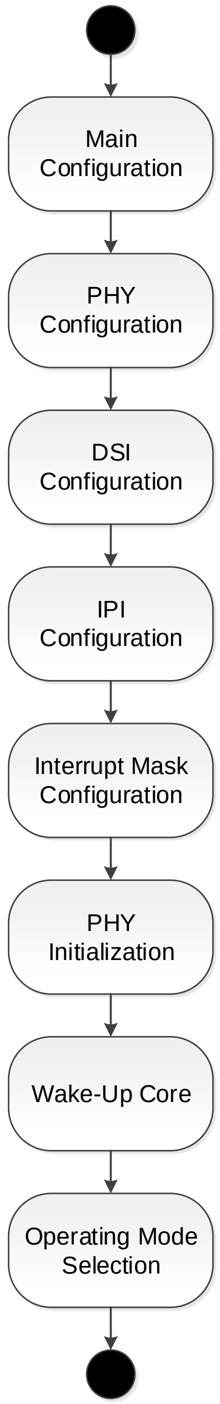

Fig. 21-9 Configuration Sequence

1) Configure controller MAIN registers by following the programming sequence in “MAIN Registers Configuration”
2) Configure PHY related registers by following the programming sequence in “PHY Configuration”
3) Configure DSI2 features by following the programming sequence in “DSI2 Protocol Configuration”
4) Configure IPI related registers by following the programming sequence in “Image Pixel Interface (IPI) Configuration”
5) Enable the errors that should trigger the interrupt pin, by writing in the different INT_MSK_<group>.
6) Perform the necessary operations to initialize the PHY, as described in the PHY documentation.
7) Assert the bit PWR_UP[0] to power up the IP.
8) Select the desired operating mode by following the sequence in “Selecting Operating Modes”

21.5.2.1 MAIN Registers Configuration

1. Configure the available timeouts, if desired, by using the following registers:
- TO_HSTX_CFG: Configures the counter for high-speed transfer timeout.
- TO_HSTXRDY_CFG: Configures the counter for high-speed ready signal timeout.
- TO_LPRX_CFG: Configures the counter for low-power data reception timeout.
- TO_LPTXRDY_CFG: Configures the counter for low-power ready signal timeout.
- TO_LPTXTRIG_CFG: Configures the counter for low-power trigger transmission timeout.
- TO_LPTXULPS_CFG: Configures the counter for ULPS entry timeout.
- TO_BTA_CFG: Configures the counter for bus turn-around procedure timeout.

2. Select if the controller is intended to work in Manual or Automatic mode, by writing in MANUAL_MODE_CFG register.

21.5.2.2 PHY Configuration

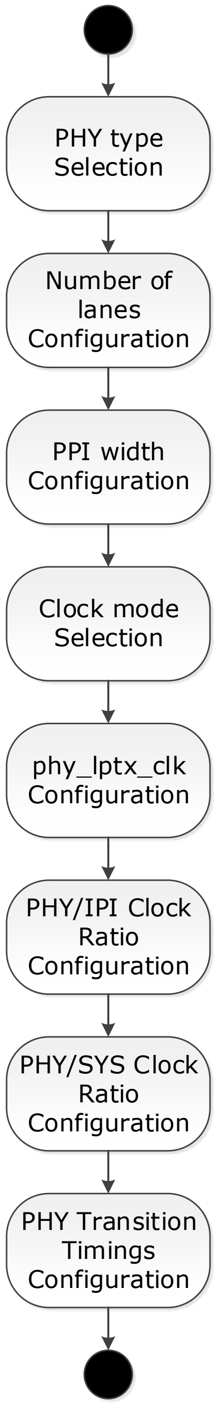

Fig. 21-10 PHY Related Configuration Sequence

Select the type of PHY to be used using the phy_type field of the PHY_MODE_CFG register.

1. Configure the number of PHY lanes using the phy_lanes field of the PHY_MODE_CFG

register.
2. Configure the PPI width of the PHY data lanes using the ppi_width field of the PHY_MODE_CFG register.
3. Configure the PHY Clock mode using the clk_type field of the PHY_CLK_CFG register.
4. Configure the phy_lptx_clk frequency using the divisor factor field of the PHY_CLK_CFG register. If the controller is not set to work in automatic mode (MANUAL_MODE_CFG register), follow these steps:
5. Configure the PHY/IPI clock ratio value in PHY_IPI_RATIO_MAN_CFG register.
6. Configure the PHY/SYS clock ratio value in PHY_SYS_RATIO_MAN_CFG register.
7. Configure the PHY low-power to high-speed and high-speed to low-power transition timings, by writing into the PHY_LP2HS_MAN_CFG and PHY_HS2LP_MAN_CFG registers, respectively.
8. Configure the maximum read time, by writing into the PHY_MAX_RD_T_MAN_CFG register.
9. Configure the escape command duration, by writing into the PHY_ESC_CMD_T_MAN_CFG register.
10. Configure the escape byte duration, by writing into the PHY_ESC_BYTE_T_MAN_CFG register.

21.5.2.3 DSI2 Protocol Configuration

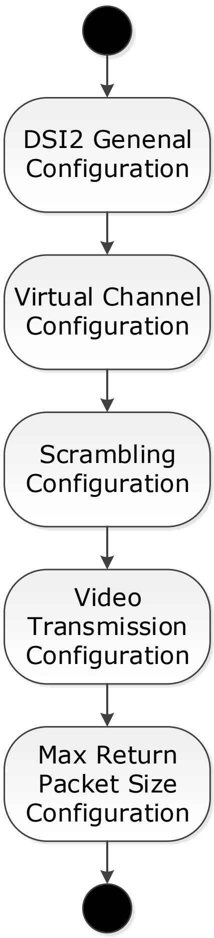

Fig. 21-11 DSI2 related Configuration Sequence

1. Configure EoTp and BTA options to meet peripheral characteristics using the DSI_GENERAL_CFG register.
2. Configure the virtual channel for transmission using the DSI_VCID_CFG register.
3. If required, enable the Scrambling feature using bit 0 of the DSI_SCRAMBLING_CFG register. By default, the scrambling polynomial is as defined in MIPI DSI-2 Specification; however, it can be changed using the DSI_SCRAMBLING_CFG register.
4. Configure the video transmission options using the DSI_VID_TX_CFG register.
5. Configure the maximum return packet size that the peripheral can send, using the DSI_MAX_RPS_CFG register. The set maximum return packet size command allows

the host processor to limit the size of the response packets coming from a peripheral. The initial value of the maximum return packet size is one byte. To get more than one byte, the host has to send this command with the desired size as a parameter before sending a read command.

Note: The maximum return packet size must not exceed the DSI2 host controller read FIFO size in order to avoid an overflow. The DSI2 host controller read FIFO has 256 bytes' size.

21.5.2.4 Image Pixel Interface (IPI) Configuration

The Image Pixel Interface (IPI) can be used to transmit an image using Video mode or Data Stream mode. Follow the programming sequence described in Below Figure to configure Image Pixel Interface.

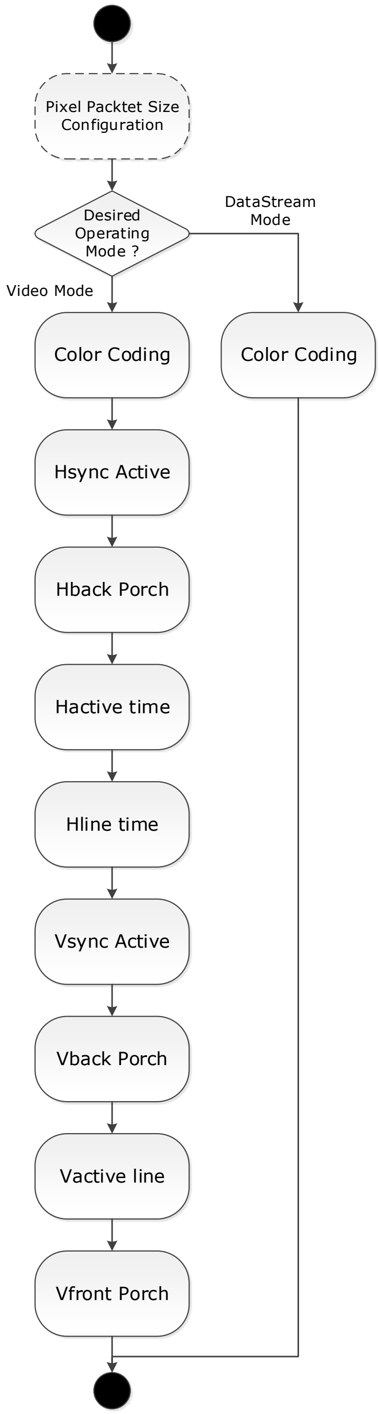

Fig. 21-12 Video Format related Configuration Sequence

1. If required, configure the number of pixels per packet using the IPI_PIX_PKT_CFG register
2. If controller is not set to work in automatic mode (MANUAL_MODE_CFG register), follow the next steps:

3. Configure the IPI Color Coding, by writing into the IPI_COLOR_MAN_CFG register.
4. If the controller is intended to operate in Data Stream mode, no more steps are required. If it is intended to operate in Video mode, follow these steps:
5. Configure the Horizontal Sync Active time by writing into the IPI_VID_HSA_MAN_CFG register.
6. Configure the Horizontal Back Porch time by writing IPI_HBP_MAN_CFG register.
7. Configure the Horizontal Active time by writing IPI_HACT_MAN_CFG register.
8. Configure the Total line time (HSA+HBP+HACT+HFP) by writing IPI_HLINE_MAN_CFG register.
9. Configure the Vertical Sync Active period in lines by writing IPI_VSA_MAN_CFG register.
10. Configure the Vertical Back Porch period in lines by writing IPI_VBP_MAN_CFG register.
11. Configure the Vertical Active period in lines by writing IPI_VACT_MAN_CFG register.
12. Configure the Vertical Front Porch period in lines by writing IPI_VFP_MAN_CFG register

21.5.2.5 Selecting Operating Modes

1. Request MIPI_DSI2_Host Controller to enter into the selected mode by writing in the in the MODE_CTRL register.
2. Verify that the MIPI_DSI2_Host Controller has entered into the selected mode by reading the MODE_STATUS register.

21.5.2.6 Using the Command Request Interface (CRI)

Follow the sequence illustrated in below Figure to send and receive packets through CRI

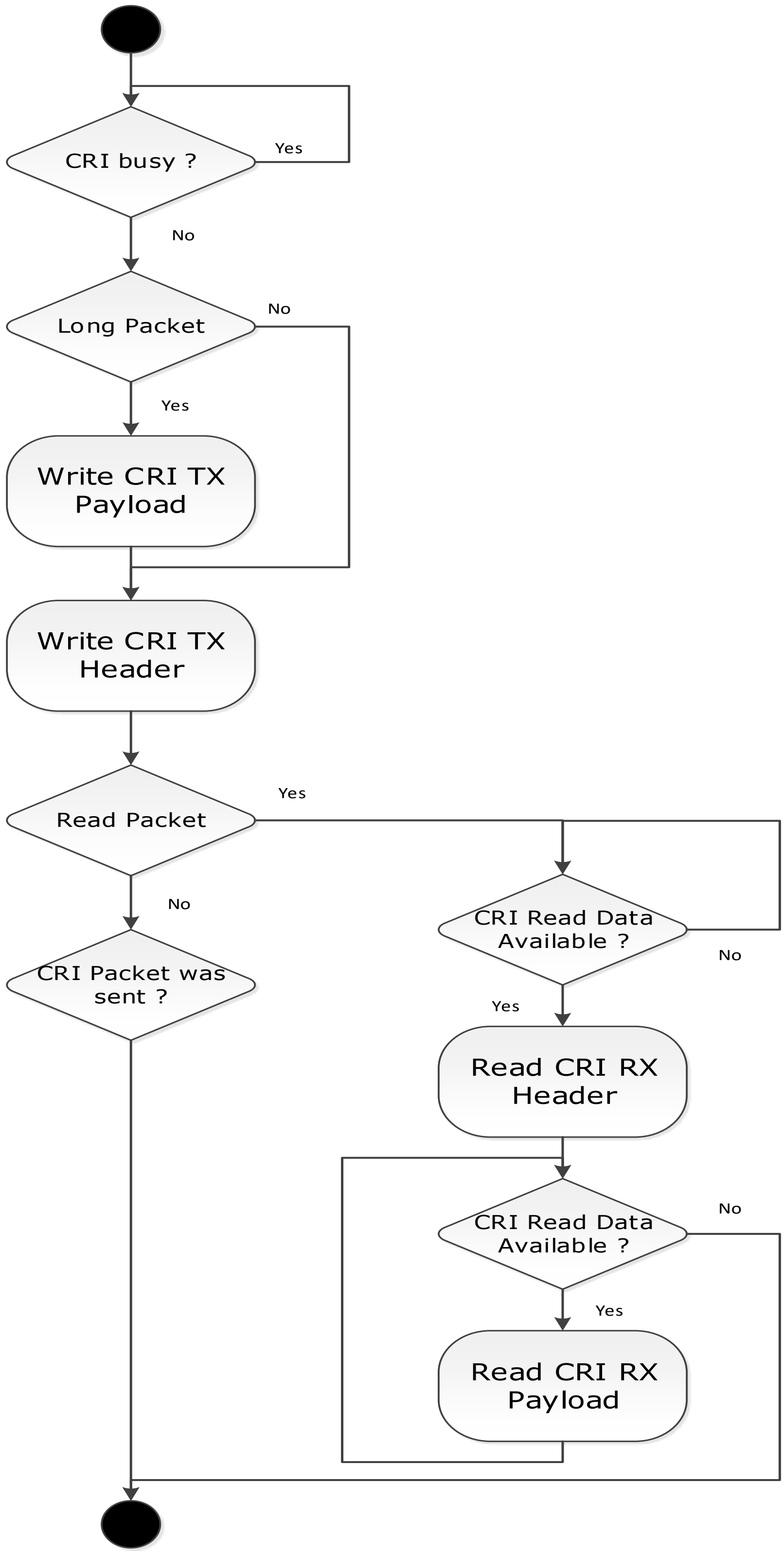

Fig. 21-13 Command related Configuration Sequence

1) Read the CORE_STATUS register to ensure that CRI is not busy.
2) If the requested packet is a long packet, write the respective payload through the CRI_TX_PLD register, four bytes per write, from the first to the last payload byte. Multiple writes may be required if the payload is bigger than 4 bytes.
3) Configure the packet header and the desired transmission mode, by writing the CRI_TX_HDR register. If the packet is not described in DSI2 specification, configure the additional cmd_hdr_rd and cmd_hdr_long bits also, to identify if the packet is a write/read and short/long.
4) If desired, when the request packet is not a read packet, check if the packet is

completely sent by reading the CRI busy status in the CORE_STATUS register. When sending read packets, the controller receives the peripheral responses and makes them available. To get the response data, follow these steps:

5) Read the CORE_STATUS register cri_rd_data_avail bit to check if there is CRI read data available.
6) Read the CRI_RX_HDR register to obtain the response header.
7) If the response is long, the CORE_STATUS register continues flagging CRI read data available until all payload bytes are read.
8) Obtain the response payload bytes by reading the CRI_RX_PLD register, four bytes per read, from the first to the last payload byte.

Note: The maximum command write payload size is 640 bytes.

21.5.3 Configuration examples

Since the PPI width of the High-Speed Transmit Data in DCPHY is fixed to 16 bits, the MIPI DSI2 host controller's PPI width should be set 16 to match it.

21.5.3.1 Case 1

Case1 related parameter:

- Video Mode, Burst Mode
- DPHY - 2Gbps/Lanes
- Video Format 1920x1080@60HZ, RGB888, uncompressed

Configuration Sequence:

1) set MANUAL_MODE_CFG = 1
2) set phy_type = 0 (DPHY), phy_lanes = 3 (4 Lanes), ppi_width = 1 (16 bits) in PHY_MODE_CFG
3) set clk_type = 0 (Continuous Clocks) in PHY_CLK_CFG
4) set vid_mode_type = 2 (Burst Mode) in DSI_VID_TX_CFG
5) set ipi_depth = 3 (8 bits), ipi_format = 0 (RGB) in IPI_COLOR_MAN_CFG
6) set IPI_HSA_MAN_CFG
7) set IPI_HBP_MAN_CFG
8) set IPI_HACT_MAN_CFG
9) set IPI_HLINE_MAN_CFG
10) set IPI_VSA_MAN_CFG = vsa
11) set IPI_VBP_MAN_CFG = vbp
12) set IPI_VACT_MAN_CFG = vact
13) set IPI_VFP_MAN_CFG = vfp
14) set IPI_RATIO_MAN_CFG = $\frac{MIPI\_DCPHY\_HSCLK\_Freq\ (125M)}{IPI\_CLK\_Freq\ (37.125M)}$
15) set SYS_RATIO_MAN_CFG = $\frac{MIPI\_DCPHY\_HSCLK\_Freq\ (125M)}{SYS\_CLK\_Freq\ (350M)}$
16) set PHY_LP2HS_MAN_CFG = PHY_LP2HS_TIME << 16, PHY_HS2LP_MAN_CFG = PHY_HS2LP_TIME << 16 , where
17) PHY_LP2HS_TIME = (TLPX + THS-PREPARE + THS-ZERO) / Tphy_hstx_clk
18) PHY_HS2LP_TIME = (THS-TRAIL + THS-EXIT) / Tphy_hstx_clk
19) Power up MIPI DCPHY
20) set pwr_up = 1 to power up DSI2 core
21) set MODE_CTRL = 3 (Video Mode)
22) enable VOP to transmitting video

21.5.3.2 Case 2

Case2 related parameter:

- Data Stream Mode
- DPHY - 2Gbps/Lanes
- Video Format 4K@60HZ, RGB888, compressed

Configuration Sequence:

1) set MANUAL_MODE_CFG = 1
2) set phy_type = 0 (DPHY), phy_lanes = 3 (4 Lanes), ppi_width = 1 (16 bits) in PHY_MODE_CFG

3) set clk_type = 0 (Continuous Clocks) in PHY_CLK_CFG
4) set ipi_depth = 3 (8 bits) and ipi_format = 11 (Compressed) in IPI_COLOR_MAN_CFG
5) set dsihost*_ipi_color_depth = 3 (8 bits) and dsihost*_ipi_format = 11 (Compressed) in VOP_GRF_VOP_CON0/1 in VOP_GRF
6) set max_pix_pkt = 3840 which equal to one compressed line byte number
7) set IPI_RATIO_MAN_CFG
8) set SYS_RATIO_MAN_CFG
9) set PHY_LP2HS_MAN_CFG = PHY_LP2HS_TIME << 16, PHY_HS2LP_MAN_CFG = PHY_HS2LP_TIME << 16
10) Power up MIPI DCPHY
11) set pwr_up = 1 to power up DSI2 core
12) set MODE_CTRL = 2 (Command Mode)
13) start transmitting power-up command and DSC PPS to display panel using CRI_TX_PLD and CRI_TX_HDR
14) set MODE_CTRL = 4 (DataStream Mode)
15) enable VOP to transmitting video

Chapter 22 MIPI D-PHY / C-PHY Combo PHY

22.1 Overview

The MIPI D-PHY / C-PHY Combo PHY is a high speed, low power, low cost PHY, especially suited for mobile applications. It is commonly used for connecting a mobile display driver or a camera sensor to a host processor according to MIPI Alliance DPHY V2.0 and C-PHY V1.1 specification. Nevertheless, it can be applied to many other applications.

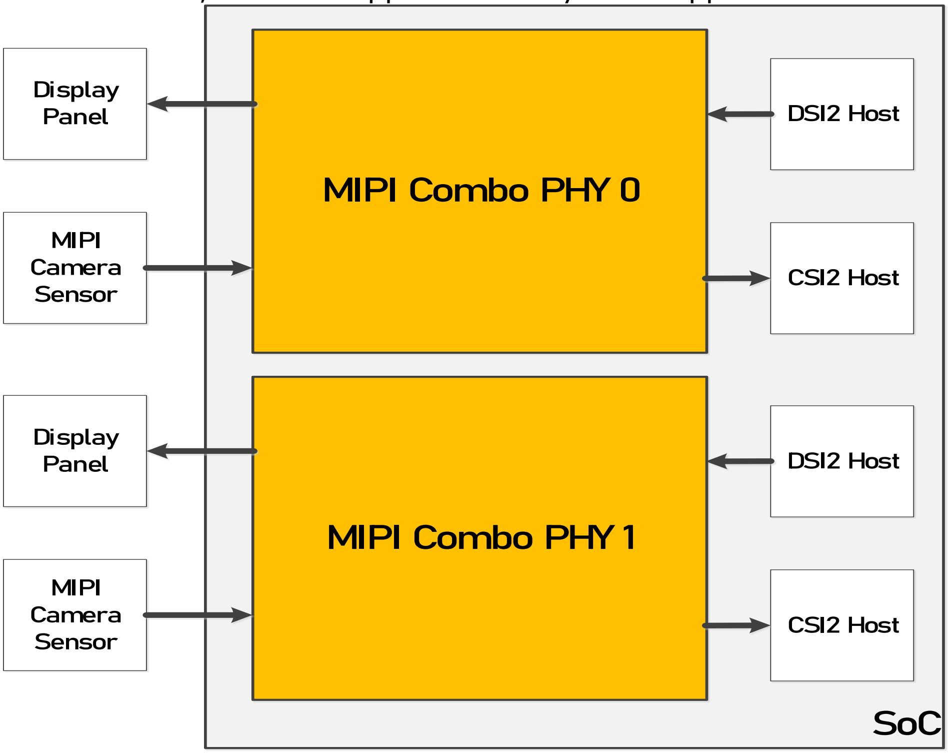

Fig. 22-1 MIPI Combo PHY

The features of D-PHY are:

- D-PHY spec v2.0 compatible
- Supports 1 Clock lane and up to 4 data lanes scalability in TX and RX respectively
- High-Speed mode: Differential and terminated: 80Mbps ~ 4500 Mbps.
- Low-Power mode: Single-ended and non-terminated, 1.2 V swing: 10 Mbps maximum
- All lanes support high-speed transmission in the forward direction.
- Bi-directional data transmission in Low-Power mode at the Master Data Lane 0 only.
- Synchronous link between Master (data source) and Slave (data sink).

The features of C-PHY are:

- C-PHY spec v1.1 compatible
- Supports up to 3 trios scalability in TX and RX respectively
- High-Speed mode: Differential and terminated
  - TX: 80Msps ~ 2000Msps
  - RX: 80Msps ~ 2500Msps
- Low-Power mode: Single-ended and non-terminated: 10Mbps maximum

Note: The TX and RX only support operate in the same PHY mode.

22.2 Block Diagram

The 4-lane D-PHY architecture including lanes and common block is shown in the below figure. IP is composed of common block (BIAS/PLL), Master clock lane, Master data 4 lanes, Slave clock lane, and Slave data 4 lanes. PLL offers the operating clock for Master block operation. Slave block uses clock from Slave clock lane input PAD at the normal operation mode. BIAS block make the analog reference voltages and currents for analog function according to MIPI specification. HS mode 0.4V voltage regulator is embedded into IP and is just used for Master blocks.

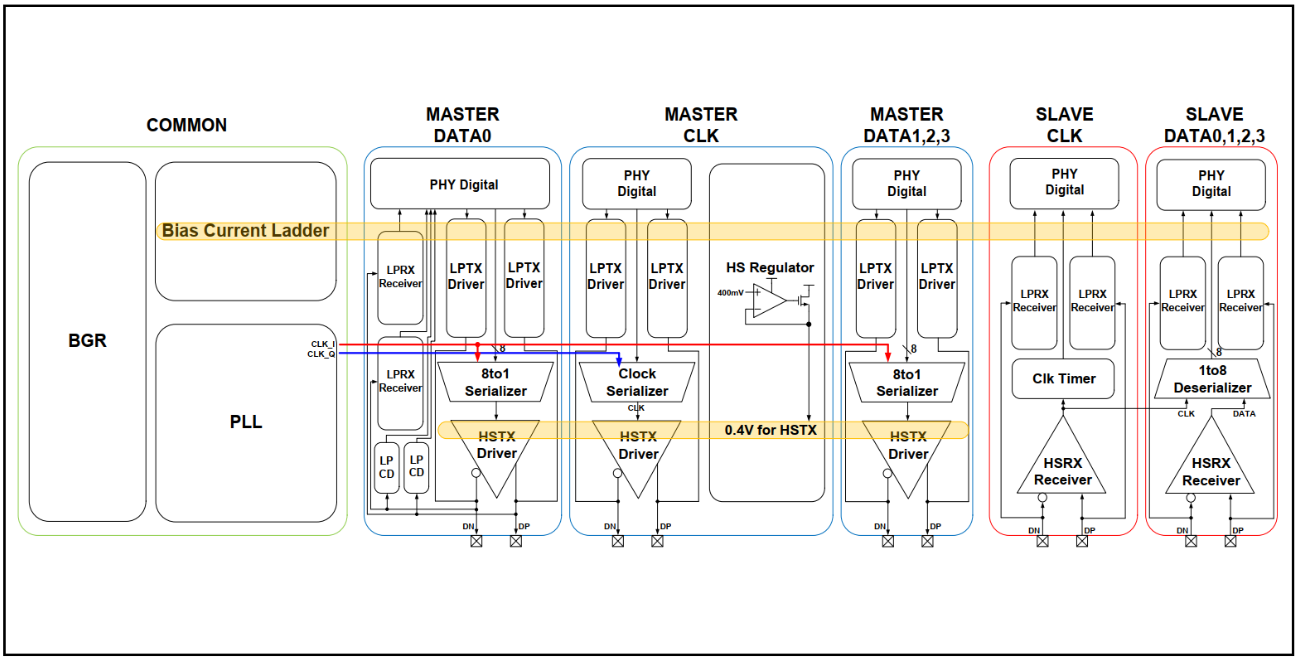

Fig. 22-2 MIPI Combo PHY Block Diagram

MIPI Combo PHY comprises with:

- BGR and bias generator
- Phase Locked Loop (PLL)
- Serializer
- HS TX Driver
- LP TX Driver
- Deserializer
- HS RX Receiver
- LP RX Receiver

22.3 Function Description

22.3.1 BGR and bias generator

The BGR circuit generates high-accuracy reference voltage of 820mV across PVT variation. A bias generator makes internal-resistor (RMRES)-referred currents, and these currents are distributed to each block in Common and Lanes. The internal resistor-referred current is generated using internally integrated replica resistor to compensate resistance error across PVT variation.

22.3.2 Phase Locked Loop (PLL)

The PLL in the Common synthesizes high-speed clock, which is used for TX serializer from a reference clock. In the PHY, the high frequency clock from PLL is used in the serialization of TX data. The following are the main features of the PLL.

- Supports output frequency from 80MHz to 2.5GHz clock
- Supports pre-defined and programmable divider setting for MIPI D-PHY specification
- Supports spread spectrum clocking (SSC) with sigma-delta modulated fractional divider

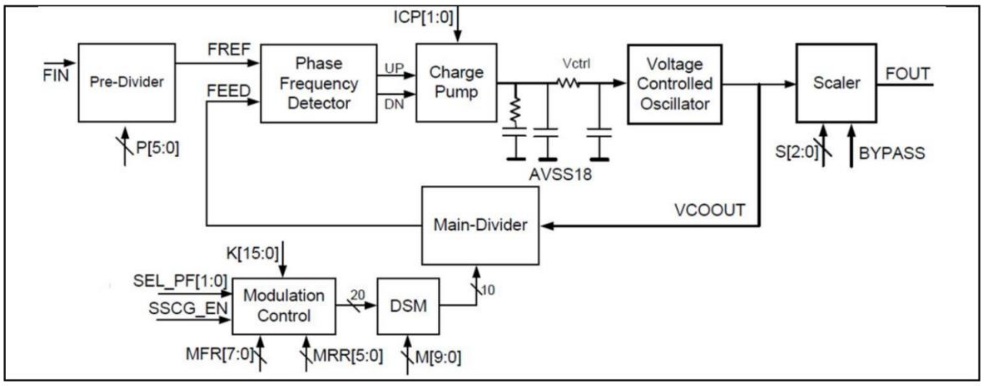

Fig. 22-3 PLL Diagram

22.3.3 Serializer

The serializer accepts 8-bit data from the PHY digital which is synchronized to TX byte clock. The parallel data is converted to the high-speed serial data. Finally, serializer transmits the serial data through the driver.

22.3.4 HS TX Driver

The driver generates baud-rate voltage waveform on TX output pads. The driver comprises of pre-driver and main-driver. The output data of serializer are delivered to the main-driver via the pre-driver. The main driver is based on voltage-mode driver to achieve a small power consumption and voltage swing.

22.3.5 LP TX Driver

In the low power mode, LP TX driver sends the low frequency data under 10Mbps. Generally, LP-11 stop state and HS enter sequence (LP-11 - LP-01 - LP-00) are used mostly.

22.3.6 Deserializer

In the BIST (Built-In Self-Test) mode, the serial data from the serializer is fed back to the de-serializer. And in the real mode, the real data from HS-RX receiver is sent to the de-serializer. De-serializer converted serial data to 8-bit parallel data and transferred them into PHY digital circuit for sending data to link or checking bit error at BIST mode.

22.3.7 HS RX Receiver

The high speed data from the MIPI D-PHY master has the MIPI D-PHY electrical characteristics. HS RX receiver convert it to the TTL CMOS level and send it to de-serializer for making the low parallel data.

22.3.8 LP RX Receiver

In the low power mode, LP RX receiver make esc clock from LP signal and converts the voltage level from 1.2V level to TTL CMOS logic level. And it sends them to PHY digital for command interpretation. And LP RX receiver always watches the DP/DN signal level. If DP/DN goes to LP-11, PHY recognizes Stop-state, and enters to low power mode.

22.3.9 PLL and Clock Lane Connection

The below figure illustrates the PLL and Clock Lane connection. MIPI D-PHY is source synchronous system. Master clock lane sends high speed differential clock to Slave clock lane. During LP mode (Low Power mode), LP signals are sent by master block. LP-TX sends the LP signals for changing mode between LP mode and HS mode. Slave block has the termination resistor between differential signals that is enabled during HS mode. Master PLL generates the high speed clock from input clock.

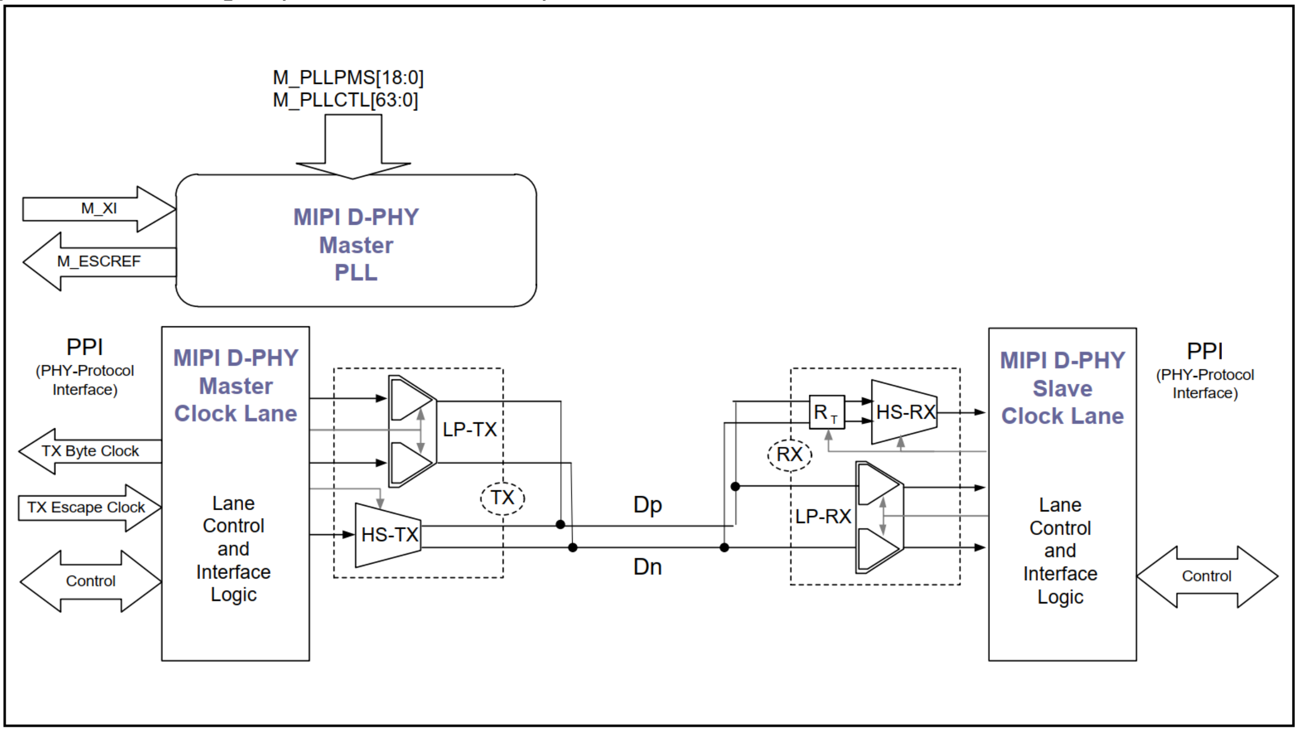

Fig. 22-4 Clock Lane Connection

22.3.10 Data Lane Connection

The below figure illustrates the Data0 Lane connection between Master and the Slave.

Master Data0 lane is the special lane for DSI interface because it has LP-CD and LP-RX. LP-RX is used for Turn-Around function according to MIPI standard specification. It is used to be called as BTA (Bus Turn-Around). It is known that BTA is needed for sending the Low Power Data Transmission from Slave to Master. LP-CD (Low Power Contention Detector) is used for detecting the abnormal state when the both of Master LP-TX and Slave LP-TX at BTA mode are enabled and the output signals are conflicted.

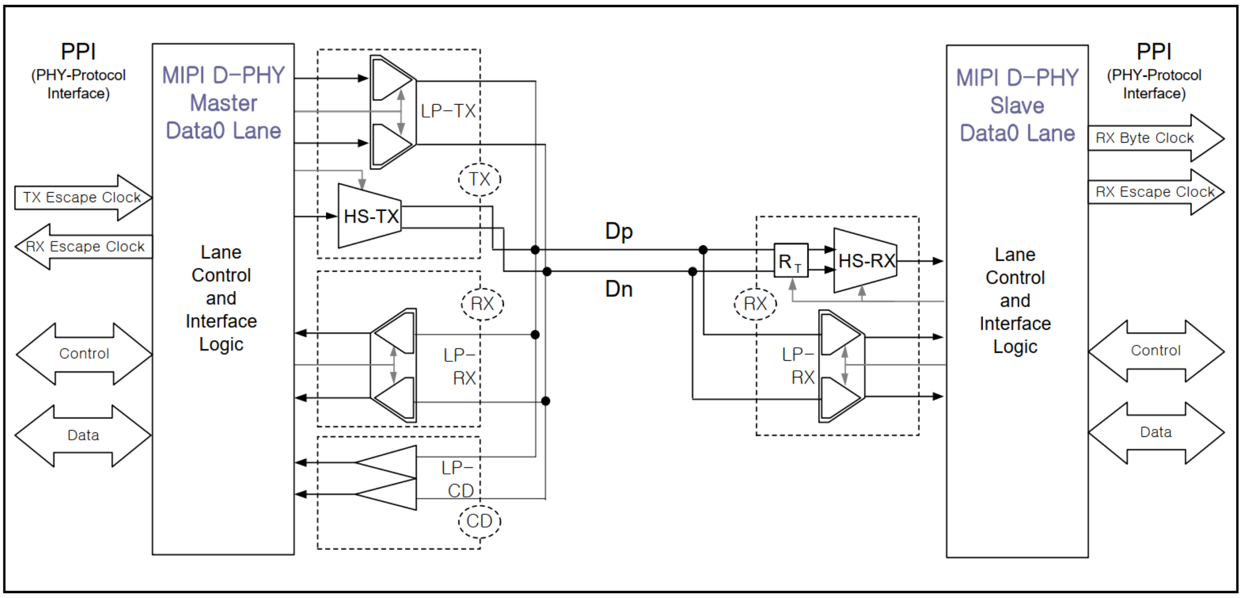

Fig. 22-5 Data 0 Lane Connection

The below figure illustrates the Data1/2/3 Lane connection between Master and the Slave. LP mode signals are used for switching mode between LP mode and HS mode. HS mode is used for interfacing high speed signals. All interface pins between PHY and protocol layer are defined at MIPI stand specification, PPI (PHY-Protocol Interface). Slave block has the termination resistor between differential signals that is enabled during HS mode.

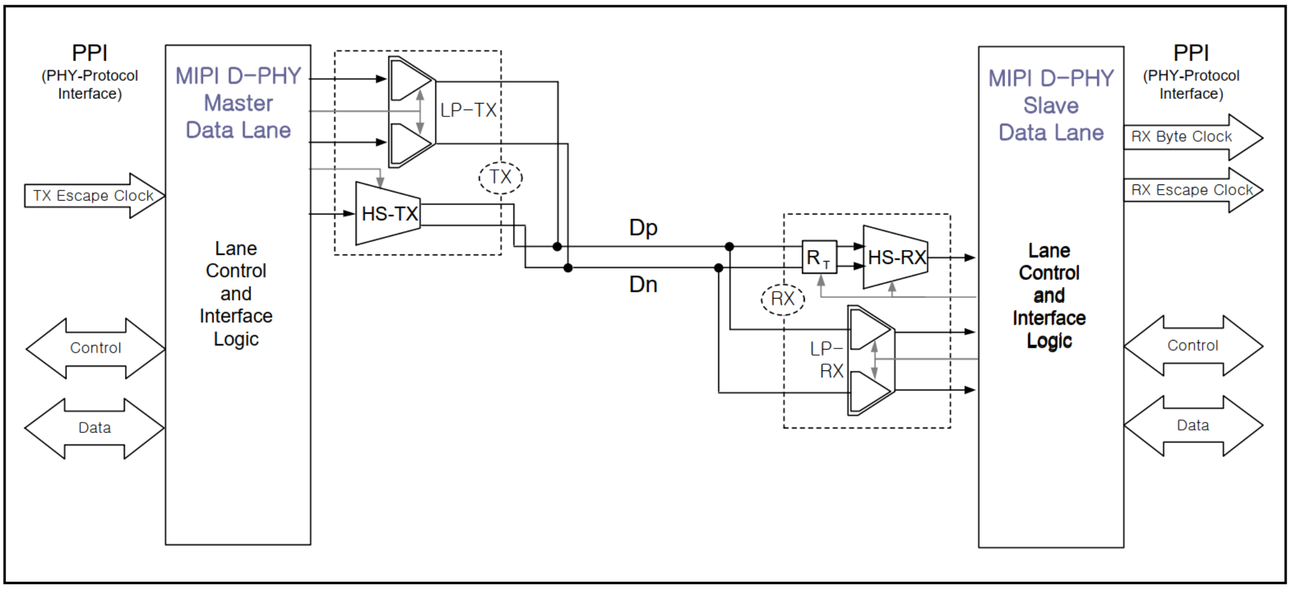

Fig. 22-6 Data 1/2/3 Lane Connection

22.4 Register Description

22.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 22-1 DCPHY Address Mapping

Base Address[11:8]	Device	Address Length	Offset Address Range
4’b0000	BIAS	256 BYTE	0x0000 ~ 0x00ff
4’b0001	PLL	256 BYTE	0x0100 ~ 0x01ff

4’b0011	Master Clock Lane	256 BYTE	0x0300 ~ 0x03ff
4’b0100	Master Data 0 Lane	256 BYTE	0x0400 ~ 0x04ff
4’b0101	Master Data 1 Lane	256 BYTE	0x0500 ~ 0x05ff
4’b0110	Master Data 2 Lane	256 BYTE	0x0600 ~ 0x06ff
4’b0111	Master Data 3 Lane	256 BYTE	0x0700 ~ 0x07ff
4’b1011	Slave Clock Lane	256 BYTE	0x0b00 ~ 0x0bff
4’b1100	Slave Data 0 Lane	256 BYTE	0x0c00 ~ 0x0cff
4’b1101	Slave Data 1 Lane	256 BYTE	0x0d00 ~ 0x0dff
4’b1110	Slave Data 2 Lane	256 BYTE	0x0e00 ~ 0x0eff
4’b1111	Slave Data 3 Lane	256 BYTE	0x0f00 ~ 0x0fff

22.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DCPHY_M0_BIAS_CON0	0x0000	W	0x00000010	BIAS Control Register0
DCPHY_M0_BIAS_CON1	0x0004	W	0x00000110	BIAS Control Register1
DCPHY_M0_BIAS_CON2	0x0008	W	0x00003223	BIAS Control Register2
DCPHY_M0_BIAS_CON4	0x0010	W	0x00000000	BIAS Control Register4
DCPHY_M0_PLL_CON0	0x0100	W	0x00000000	PLL Control Register0
DCPHY_M0_PLL_CON1	0x0104	W	0x00000000	PLL Control Register1
DCPHY_M0_PLL_CON2	0x0108	W	0x00000000	PLL Control Register2
DCPHY_M0_PLL_CON3	0x010C	W	0x00000000	PLL Control Register3
DCPHY_M0_PLL_CON4	0x0110	W	0x00000000	PLL Control Register4
DCPHY_M0_PLL_CON5	0x0114	W	0x00000000	PLL Control Register5
DCPHY_M0_PLL_CON6	0x0118	W	0x00000000	PLL Control Register6
DCPHY_M0_PLL_CON7	0x011C	W	0x00000000	PLL Control Register7
DCPHY_M0_PLL_CON8	0x0120	W	0x00000000	PLL Control Register8
DCPHY_M0_PLL_STAT0	0x0140	W	0x00000000	PLL Status Register0
DCPHY_M0_DPHY_MC_GNR_CON0	0x0300	W	0x00000000	D-PHY Master Clock Lane General Control Register0
DCPHY_M0_DPHY_MC_GNR_CON1	0x0304	W	0x00000000	D-PHY Master Clock Lane General Control Register1
DCPHY_M0_DPHY_MC_ANA_CON0	0x0308	W	0x00007133	D-PHY Master Clock Lane Analog Block Control Register0
DCPHY_M0_DPHY_MC_ANA_CON1	0x030C	W	0x00000000	D-PHY Master Clock Lane Analog Block Control Register1
DCPHY_M0_DPHY_MC_ANA_CON2	0x0310	W	0x00000000	D-PHY Master Clock Lane Analog Block Control Register2
DCPHY_M0_DPHY_MC_ANA_CON3	0x0314	W	0x00000000	D-PHY Master Clock Lane Analog Block Control Register3
DCPHY_M0_DPHY_MC_TIME_CON0	0x0330	W	0x00000000	D-PHY Master Clock Lane Timing Control Register0
DCPHY_M0_DPHY_MC_TIME_CON1	0x0334	W	0x00000000	D-PHY Master Clock Lane Timing Control Register1
DCPHY_M0_DPHY_MC_TIME_CON2	0x0338	W	0x00000000	D-PHY Master Clock Lane Timing Control Register2
DCPHY_M0_DPHY_MC_TIME_CON3	0x033C	W	0x00000000	D-PHY Master Clock Lane Timing Control Register3
DCPHY_M0_DPHY_MC_TIME_CON4	0x0340	W	0x00000000	D-PHY Master Clock Lane Timing Control Register4
DCPHY_M0_DPHY_MC_DATA_CON0	0x0344	W	0x00000000	D-PHY Master Clock Lane Data Control Register0
DCPHY_M0_DPHY_MC_DESKEW_CON0	0x0350	W	0x00000000	D-PHY Master Clock Lane Skew Calibration Control Register0

Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_MD0_GNR_CON0	0x0400	W	0x00000000	DC-PHY Combo Master Data 0 Lane General Control Register0
DCPHY_M0_COMBO_MD0_GNR_CON1	0x0404	W	0x00000000	DC-PHY Combo Master Data 0 Lane General Control Register1
DCPHY_M0_COMBO_MD0_ANA_CON0	0x0408	W	0x00007133	DC-PHY Combo Master Data 0 Lane Analog Block Control Register0
DCPHY_M0_COMBO_MD0_ANA_CON1	0x040C	W	0x00000000	DC-PHY Combo Master Data 0 Lane Analog Block Control Register1
DCPHY_M0_COMBO_MD0_ANA_CON2	0x0410	W	0x00000000	DC-PHY Combo Master Data 0 Lane Analog Block Control Register2
DCPHY_M0_COMBO_MD0_TIME_CON0	0x0430	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register0
DCPHY_M0_COMBO_MD0_TIME_CON1	0x0434	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register1
DCPHY_M0_COMBO_MD0_TIME_CON2	0x0438	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register2
DCPHY_M0_COMBO_MD0_TIME_CON3	0x043C	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register3
DCPHY_M0_COMBO_MD0_TIME_CON4	0x0440	W	0x00000000	DC-PHY Combo Master Data 0 Lane Timing Control Register4
DCPHY_M0_COMBO_MD0_DATA_CON0	0x0444	W	0x00000000	DC-PHY Combo Master Data 0 Lane Data Control Register0
DCPHY_M0_COMBO_MD0_PRGSEQ_CON0	0x0460	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register0
DCPHY_M0_COMBO_MD0_PRGSEQ_CON1	0x0464	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register1
DCPHY_M0_COMBO_MD0_PRGSEQ_CON2	0x0468	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register2
DCPHY_M0_COMBO_MD0_PRGSEQ_CON3	0x046C	W	0x00000000	DC-PHY Combo Master Data 0 Lane Programmable Sequence Control Register3
DCPHY_M0_COMBO_MD1_GNR_CON0	0x0500	W	0x00000000	DC-PHY Combo Master Data 1 Lane General Control Register0
DCPHY_M0_COMBO_MD1_GNR_CON1	0x0504	W	0x00000000	DC-PHY Combo Master Data 1 Lane General Control Register1
DCPHY_M0_COMBO_MD1_ANA_CON0	0x0508	W	0x00007133	DC-PHY Combo Master Data 1 Lane Analog Block Control Register0
DCPHY_M0_COMBO_MD1_ANA_CON1	0x050C	W	0x00000000	DC-PHY Combo Master Data 1 Lane Analog Block Control Register1
DCPHY_M0_COMBO_MD1_ANA_CON2	0x0510	W	0x00000000	DC-PHY Combo Master Data 1 Lane Analog Block Control Register2
DCPHY_M0_COMBO_MD1_TIME_CON0	0x0530	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register0
DCPHY_M0_COMBO_MD1_TIME_CON1	0x0534	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register1

Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_MD1_TIME_CON2	0x0538	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register2
DCPHY_M0_COMBO_MD1_TIME_CON3	0x053C	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register3
DCPHY_M0_COMBO_MD1_TIME_CON4	0x0540	W	0x00000000	DC-PHY Combo Master Data 1 Lane Timing Control Register4
DCPHY_M0_COMBO_MD1_DATA_CON0	0x0544	W	0x00000000	DC-PHY Combo Master Data 1 Lane Data Control Register0
DCPHY_M0_COMBO_MD1_PRGSEQ_CON0	0x0560	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register0
DCPHY_M0_COMBO_MD1_PRGSEQ_CON1	0x0564	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register1
DCPHY_M0_COMBO_MD1_PRGSEQ_CON2	0x0568	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register2
DCPHY_M0_COMBO_MD1_PRGSEQ_CON3	0x056C	W	0x00000000	DC-PHY Combo Master Data 1 Lane Programmable Sequence Control Register3
DCPHY_M0_COMBO_MD2_GNR_CON0	0x0600	W	0x00000000	DC-PHY Combo Master Data 2 Lane General Control Register0
DCPHY_M0_COMBO_MD2_GNR_CON1	0x0604	W	0x00000000	DC-PHY Combo Master Data 2 Lane General Control Register1
DCPHY_M0_COMBO_MD2_ANA_CON0	0x0608	W	0x00007133	DC-PHY Combo Master Data 2 Lane Analog Block Control Register0
DCPHY_M0_COMBO_MD2_ANA_CON1	0x060C	W	0x00000000	DC-PHY Combo Master Data 2 Lane Analog Block Control Register1
DCPHY_M0_COMBO_MD2_ANA_CON2	0x0610	W	0x00000000	DC-PHY Combo Master Data 2 Lane Analog Block Control Register2
DCPHY_M0_COMBO_MD2_TIME_CON0	0x0630	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register0
DCPHY_M0_COMBO_MD2_TIME_CON1	0x0634	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register1
DCPHY_M0_COMBO_MD2_TIME_CON2	0x0638	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register2
DCPHY_M0_COMBO_MD2_TIME_CON3	0x063C	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register3
DCPHY_M0_COMBO_MD2_TIME_CON4	0x0640	W	0x00000000	DC-PHY Combo Master Data 2 Lane Timing Control Register4
DCPHY_M0_COMBO_MD2_DATA_CON0	0x0644	W	0x00000000	DC-PHY Combo Master Data 2 Lane Data Control Register0
DCPHY_M0_COMBO_MD2_PRGSEQ_CON0	0x0660	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register0
DCPHY_M0_COMBO_MD2_PRGSEQ_CON1	0x0664	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register1
DCPHY_M0_COMBO_MD2_PRGSEQ_CON2	0x0668	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register2

Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_MD2_PRGSEQ_CON3	0x066C	W	0x00000000	DC-PHY Combo Master Data 2 Lane Programmable Sequence Control Register3
DCPHY_M0_DPHY_MD3_GNR_CON0	0x0700	W	0x00000000	D-PHY Master Data 3 Lane General Control Register0
DCPHY_M0_DPHY_MD3_GNR_CON1	0x0704	W	0x00000000	D-PHY Master Data 3 Lane General Control Register1
DCPHY_M0_DPHY_MD3_ANA_CON0	0x0708	W	0x00007133	D-PHY Master Data 3 Lane Analog Block Control Register0
DCPHY_M0_DPHY_MD3_ANA_CON1	0x070C	W	0x00000000	D-PHY Master Data 3 Lane Analog Block Control Register1
DCPHY_M0_DPHY_MD3_ANA_CON2	0x0710	W	0x00000000	D-PHY Master Data 3 Lane Analog Block Control Register2
DCPHY_M0_DPHY_MD3_TIME_CON0	0x0730	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register0
DCPHY_M0_DPHY_MD3_TIME_CON1	0x0734	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register1
DCPHY_M0_DPHY_MD3_TIME_CON2	0x0738	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register2
DCPHY_M0_DPHY_MD3_TIME_CON3	0x073C	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register3
DCPHY_M0_DPHY_MD3_TIME_CON4	0x0740	W	0x00000000	D-PHY Master Data 3 Lane Timing Control Register4
DCPHY_M0_DPHY_MD3_DATA_CON0	0x0744	W	0x00000000	D-PHY Master Data 3 Lane Data Control Register0
DCPHY_M0_DPHY_SC_GNR_CON0	0x0B00	W	0x00000000	D-PHY Slave Clock Lane General Control Register0
DCPHY_M0_DPHY_SC_GNR_CON1	0x0B04	W	0x00000000	D-PHY Slave Clock Lane General Control Register1
DCPHY_M0_DPHY_SC_ANA_CON0	0x0B08	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register0
DCPHY_M0_DPHY_SC_ANA_CON1	0x0B0C	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register1
DCPHY_M0_DPHY_SC_ANA_CON2	0x0B10	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register2
DCPHY_M0_DPHY_SC_ANA_CON3	0x0B14	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register3
DCPHY_M0_DPHY_SC_ANA_CON4	0x0B18	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register4
DCPHY_M0_DPHY_SC_ANA_CON5	0x0B1C	W	0x00000000	D-PHY Slave Clock Lane Analog Block Control Register5
DCPHY_M0_DPHY_SC_TIME_CON0	0x0B30	W	0x00000000	D-PHY Slave Clock Lane Timing Control Register0
DCPHY_M0_COMBO_SD0_GNR_CON0	0x0C00	W	0x00000000	DC-PHY Combo Slave Data 0 Lane General Control Register0
DCPHY_M0_COMBO_SD0_GNR_CON1	0x0C04	W	0x00000000	DC-PHY Combo Slave Data 0 Lane General Control Register1
DCPHY_M0_COMBO_SD0_ANA_CON0	0x0C08	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register0
DCPHY_M0_COMBO_SD0_ANA_CON1	0x0C0C	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register1
DCPHY_M0_COMBO_SD0_ANA_CON2	0x0C10	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register2

Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_SD0_ANA_CON3	0x0C14	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register3
DCPHY_M0_COMBO_SD0_ANA_CON4	0x0C18	W	0x00000000	DC-PHY Combo Slave Data0 Lane Analog Block Control Register4
DCPHY_M0_COMBO_SD0_ANA_CON6	0x0C20	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register6
DCPHY_M0_COMBO_SD0_ANA_CON7	0x0C24	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Analog Block Control Register7
DCPHY_M0_COMBO_SD0_TIME_CON0	0x0C30	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Timing Control Register0
DCPHY_M0_COMBO_SD0_TIME_CON1	0x0C34	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Timing Control Register1
DCPHY_M0_COMBO_SD0_DATA_CON0	0x0C38	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Data Control Register0
DCPHY_M0_COMBO_SD0_DESKEW_CON0	0x0C40	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register0
DCPHY_M0_COMBO_SD0_DESKEW_CON1	0x0C44	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register1
DCPHY_M0_COMBO_SD0_DESKEW_CON2	0x0C48	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register2
DCPHY_M0_COMBO_SD0_DESKEW_CON3	0x0C4C	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register3
DCPHY_M0_COMBO_SD0_DESKEW_CON4	0x0C50	W	0x00000000	DC-PHY Combo Slave Data 0 Lane Skew Calibration Control Register4
DCPHY_M0_COMBO_SD0_CRC_CON0	0x0C60	W	0x00000000	DC-PHY Combo Slave Data 0 Lane CRC Control Register0
DCPHY_M0_COMBO_SD0_CRC_CON1	0x0C64	W	0x00000000	DC-PHY Combo Slave Data 0 Lane CRC Control Register1
DCPHY_M0_COMBO_SD0_CRC_CON2	0x0C68	W	0x00000000	DC-PHY Combo Slave Data 0 Lane CRC Control Register2
DCPHY_M0_COMBO_SD1_GNR_CON0	0x0D00	W	0x00000000	DC-PHY Combo Slave Data 1 Lane General Control Register0
DCPHY_M0_COMBO_SD1_GNR_CON1	0x0D04	W	0x00000000	DC-PHY Combo Slave Data 1 Lane General Control Register1
DCPHY_M0_COMBO_SD1_ANA_CON0	0x0D08	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register0
DCPHY_M0_COMBO_SD1_ANA_CON1	0x0D0C	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register1
DCPHY_M0_COMBO_SD1_ANA_CON2	0x0D10	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register2
DCPHY_M0_COMBO_SD1_ANA_CON3	0x0D14	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register3
DCPHY_M0_COMBO_SD1_ANA_CON4	0x0D18	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register4
DCPHY_M0_COMBO_SD1_ANA_CON6	0x0D20	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register6
DCPHY_M0_COMBO_SD1_ANA_CON7	0x0D24	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Analog Block Control Register7

Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_SD1_TIME_CON0	0x0D30	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Timing Control Register0
DCPHY_M0_COMBO_SD1_TIME_CON1	0x0D34	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Timing Control Register1
DCPHY_M0_COMBO_SD1_DATA_CON0	0x0D38	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Data Control Register0
DCPHY_M0_COMBO_SD1_DESKEW_CON0	0x0D40	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register0
DCPHY_M0_COMBO_SD1_DESKEW_CON1	0x0D44	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register1
DCPHY_M0_COMBO_SD1_DESKEW_CON2	0x0D48	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register2
DCPHY_M0_COMBO_SD1_DESKEW_CON3	0x0D4C	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register3
DCPHY_M0_COMBO_SD1_DESKEW_CON4	0x0D50	W	0x00000000	DC-PHY Combo Slave Data 1 Lane Skew Calibration Control Register4
DCPHY_M0_COMBO_SD1_CRC_CON0	0x0D60	W	0x00000000	DC-PHY Combo Slave Data 1 Lane CRC Control Register0
DCPHY_M0_COMBO_SD1_CRC_CON1	0x0D64	W	0x00000000	DC-PHY Combo Slave Data 1 Lane CRC Control Register1
DCPHY_M0_COMBO_SD1_CRC_CON2	0x0D68	W	0x00000000	DC-PHY Combo Slave Data 1 Lane CRC Control Register2
DCPHY_M0_COMBO_SD2_GNR_CON0	0x0E00	W	0x00000000	DC-PHY Combo Slave Data 2 Lane General Control Register0
DCPHY_M0_COMBO_SD2_GNR_CON1	0x0E04	W	0x00000000	DC-PHY Combo Slave Data 2 Lane General Control Register1
DCPHY_M0_COMBO_SD2_ANA_CON0	0x0E08	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register0
DCPHY_M0_COMBO_SD2_ANA_CON1	0x0E0C	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register1
DCPHY_M0_COMBO_SD2_ANA_CON2	0x0E10	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register2
DCPHY_M0_COMBO_SD2_ANA_CON3	0x0E14	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register3
DCPHY_M0_COMBO_SD2_ANA_CON4	0x0E18	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register4
DCPHY_M0_COMBO_SD2_ANA_CON6	0x0E20	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register6
DCPHY_M0_COMBO_SD2_ANA_CON7	0x0E24	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Analog Block Control Register7
DCPHY_M0_COMBO_SD2_TIME_CON0	0x0E30	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Timing Control Register0
DCPHY_M0_COMBO_SD2_TIME_CON1	0x0E34	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Timing Control Register1
DCPHY_M0_COMBO_SD2_DATA_CON0	0x0E38	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Data Control Register0
DCPHY_M0_COMBO_SD2_DESKEW_CON0	0x0E40	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register0

Name	Offset	Size	Reset Value	Description
DCPHY_M0_COMBO_SD2_DESKEW_CON1	0x0E44	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register1
DCPHY_M0_COMBO_SD2_DESKEW_CON2	0x0E48	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register2
DCPHY_M0_COMBO_SD2_DESKEW_CON3	0x0E4C	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register3
DCPHY_M0_COMBO_SD2_DESKEW_CON4	0x0E50	W	0x00000000	DC-PHY Combo Slave Data 2 Lane Skew Calibration Control Register4
DCPHY_M0_COMBO_SD2_CRC_CON0	0x0E60	W	0x00000000	DC-PHY Combo Slave Data 2 Lane CRC Control Register0
DCPHY_M0_COMBO_SD2_CRC_CON1	0x0E64	W	0x00000000	DC-PHY Combo Slave Data 2 Lane CRC Control Register1
DCPHY_M0_COMBO_SD2_CRC_CON2	0x0E68	W	0x00000000	DC-PHY Combo Slave Data 2 Lane CRC Control Register2
DCPHY_M0_DPHY_SD3_GNR_CON0	0x0F00	W	0x00000000	D-PHY Slave Data 3 Lane General Control Register0
DCPHY_M0_DPHY_SD3_GNR_CON1	0x0F04	W	0x00000000	D-PHY Slave Data 3 Lane General Control Register1
DCPHY_M0_DPHY_SD3_ANA_CON0	0x0F08	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register0
DCPHY_M0_DPHY_SD3_ANA_CON1	0x0F0C	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register1
DCPHY_M0_DPHY_SD3_ANA_CON2	0x0F10	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register2
DCPHY_M0_DPHY_SD3_ANA_CON3	0x0F14	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register3
DCPHY_M0_DPHY_SD3_ANA_CON4	0x0F18	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register4
DCPHY_M0_DPHY_SD3_ANA_CON5	0x0F1C	W	0x00000000	D-PHY Slave Data 3 Lane Analog Block Control Register5
DCPHY_M0_DPHY_SD3_TIME_CON0	0x0F30	W	0x00000000	D-PHY Slave Data 3 Lane Timing Control Register0
DCPHY_M0_DPHY_SD3_TIME_CON1	0x0F34	W	0x00000000	D-PHY Slave Data 3 Lane Timing Control Register1
DCPHY_M0_DPHY_SD3_DATA_CON0	0x0F38	W	0x00000000	D-PHY Slave Data 3 Lane Data Control Register0
DCPHY_M0_DPHY_SD3_DESKEW_CON0	0x0F40	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register0
DCPHY_M0_DPHY_SD3_DESKEW_CON1	0x0F44	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register1
DCPHY_M0_DPHY_SD3_DESKEW_CON2	0x0F48	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register2
DCPHY_M0_DPHY_SD3_DESKEW_CON3	0x0F4C	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register3
DCPHY_M0_DPHY_SD3_DESKEW_CON4	0x0F50	W	0x00000000	D-PHY Slave Data 3 Lane Skew Calibration Control Register4

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

22.4.3 Detail Registers Description

DCPHY_M0_BIAS_CON0
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x1	I_RES_CNTL Bias current control 3'b000: 59.2uA 3'b001: 100.2uA 3'b010: 94.2uA 3'b011: 113.8uA 3'b100: 89.7uA 3'b101: 111.8uA 3'b110: 108.2uA 3'b111: 120.8uA
3:2	RO	0x0	reserved
1:0	RW	0x0	I_DIV_SEL BGR Chopper Clock Divider Control 2b'00: DIV 6 2b'01: DIV 12 2b'10: DIV 20 2b'11: DIV 40

DCPHY_M0_BIAS_CON1
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x1	I_VBG_SEL BGR Reference Voltage 820mV Control 2b'00: vbg_780mV 2b'01: vbg_820mV 2b'10: vbg_860mV 2b'11: vbg_900mV
7:6	RO	0x0	reserved
5:4	RW	0x1	I_BGR_VREF_SEL Bias Reference Voltage 820mV Control 2b'00: S<0> 810mV 2b'01: S<1> 820mV 2b'10: S<2> 830mV 2b'11: S<3> 840mV
3	RO	0x0	reserved
2:0	RW	0x0	I_LADDER_SEL BGR Resistor Ladder Voltage Control 3'b000: 1V 3'b001: 0.96V 3'b010: 0.92V 3'b011: 0.88V 3'b100: 0.84V 3'b101: 0.8V 3'b110: 0.76V 3'b111: 0.72V

DCPHY_M0_BIAS_CON2
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x3	REG_325M Reference voltage-325mV for CD Function control pin 3'b000: 295mV 3'b001: 305mV 3'b010: 315mV 3'b011: 325mV 3'b100: 335mV 3'b101: 345mV 3'b110: 355mV 3'b111: 365mV
11	RO	0x0	reserved
10:8	RW	0x2	REG_LP_400M Reference voltage-400mV for LP_REG Function control pin 3'b000: 380mV 3'b001: 390mV 3'b010: 400mV 3'b011: 410mV 3'b100: 420mV 3'b101: 430mV 3'b110: 440mV 3'b111: 450mV
7	RO	0x0	reserved
6:4	RW	0x2	REG_400M Reference voltage-400mV/200mV for HS Function control pin, the left value is selected when I_MUX_SEL is set to 0x0 and the right value is selected when I_MUX_SEL is set to 0x1. 3'b000: 380mV / 230mV 3'b001: 390mV / 220mV 3'b010: 400mV / 210mV 3'b011: 410mV / 200mV 3'b100: 420mV / 190mV 3'b101: 430mV / 180mV 3'b110: 440mV / 170mV 3'b111: 450mV / 160mV
3	RO	0x0	reserved
2:0	RW	0x3	REG_645M Reference voltage-645mV for LP Function control pin 3'b000: 605mV 3'b001: 625mV 3'b010: 635mV 3'b011: 645mV 3'b100: 655mV 3'b101: 665mV 3'b110: 685mV 3'b111: 725mV

DCPHY_M0_BIAS_CON4
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	I_MUX_SEL Output Voltage(400mV/200mV/530mV) selction pin 2b'00 : 400mV 2b'01 : 200mV 2b'10 : 530mV 2b'11 : 530mV D-PHY: 2'b00 C-PHY: 2'b10
4:0	RO	0x00	reserved

DCPHY_M0_PLL_CON0
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	PLL_EN PLL Control Logic Block Enable Register. For use PLL in PHY module, user can set this register after setting registers.
11	RO	0x0	reserved
10:8	RW	0x0	S Register for Division Value of the 3-bit Programmable Scaler.
7:6	RO	0x0	reserved
5:0	RW	0x00	P Register for Division Value of the 6-bit Programmable Pre-Divider. PLL has to be reset if P value is changed.

DCPHY_M0_PLL_CON1
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	K Value of 16-bit DSM.

DCPHY_M0_PLL_CON2
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	USE_SDW_REG Shadow Register Enable Register. For using frequency hopping function in PHY, user can set this register before controlling the interface signal PLL_CFG_UPDT.
14	RW	0x0	M_ESCREF_EN M_ESCREF Output Enable Register. When user wants to measure the Escape Clock of Master Lanes, set this register.
13	RW	0x0	FOUT_MASK Register for Scaler's Re-initialization Time Control Pin. Default value is 1'b0.
12	RW	0x0	FEED_EN Register for Monitoring Pin. If FEED_EN is 1, FEED_OUT is enabled. Default value is 1'b0.
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	M Register for Division Value of the 10-bit Programmable Main-Divider. PLL has to be reset if M value is changed.

DCPHY_M0_PLL_CON3
Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	MRR Register for Value of 6-bit Modulation Rate Control. PLL has to be reset if MRR is changed.
7:0	RW	0x00	MFR Register for Value of 8-bit Modulation Frequency Control. PLL has to be reset if MFR is changed.

DCPHY_M0_PLL_CON4
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	SSCG_EN Register for Enable Pin for Dithered Mode(Active-high).
10	RW	0x0	FSEL Register for Monitoring Pin. If FSEL is 0, FEED_OUT is FREF If FSEL is 1, FEED_OUT is FEED Default value is 1'b0.
9	RW	0x0	BYPASS Register for Bypass Function of PLL. If BYPASS is 1, bypass mode is enabled. (FOUT: FIN) If BYPASS is 0, PLL operates normally.
8	RW	0x0	AFC_ENB Register for Monitoring Pin. If AFC_ENB is 0, AFC is enabled and VCO is calibrated automatically. If AFC_ENB is 1, AFC is disabled and VCO is calibrated manually by EXTAFC[4:0] for the test of VCO range. Default value is 1'b0.
7:5	RO	0x0	reserved
4:0	RW	0x00	EXTAFC Register for Monitoring Pin. If AFC_ENB is 1, AFC is disabled and VCO is calibrated manually by EXTAFC[4:0] for the test of VCO range. Default value is 5'b0_0000.

DCPHY_M0_PLL_CON5
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CLK_BUFF_EN_SEL Clock Buffering Enable Selection Register. 1'b0: Clock buffering is enabled when PLL_EN is set. 1'b1: Clock buffering is enabled when ENABLE(M%_DPHY_M#C_GNR_CON0) is set.

Bit	Attr	Reset Value	Description
14	RW	0x0	F_OUT_EN PLL Output to External Module Enable Control Register. For sharing PLL signals of this module with other module, user can set this register before enabling the PLL.
13	RW	0x0	CAL_SEL_CK Clock I-Q Phase Change Control Register. 1'b0: Use Q Phase. 1'b1: Use I Phase. (Changed)
12	RW	0x0	CAL_SEL_DATA Data I-Q Phase Change Control Register. 1'b0: Use I Phase. 1'b1: Use Q Phase. (Changed)
11	RW	0x0	SEL_EXTCLK PLL of External Module Enable Register. For using shared clock and clock signals by PLL of external module, user can set this register without enabling the PLL in this module. 1'b0: Use Internal PLL. (Default) 1'b1: Use External PLL.
10	RW	0x0	RESET_N_SEL Clock Divider Reset Selection Register. 1'b0: Release clock divider reset when PLL_EN is set. 1'b1: Release clock divider reset when ENABLE(M%_DPHY_M#C_GNR_CON0) is set.
9	RW	0x0	MS_ENABLECLK_SEL PLL Buffering Enable Selection Register. 1'b0: PLL buffering is enabled when ENABLE(M%_DPHY_M#C_GNR_CON0) is set. 1'b1: PLL buffering is enabled when ENABLE(M%_DPHY_S#C_GNR_CON0) is set.
8	RW	0x0	PLL_ENABLE_SEL PLL Buffering Enable Selection Register. 1'b0: PLL buffering is enabled when PLL_EN is set. 1'b1: PLL buffering is enabled when ENABLE(M%_DPHY_M#C_GNR_CON0) is set.
7:6	RO	0x0	reserved
5:4	RW	0x0	ICP Register for Controls the Charge-Pump Current. Default value: 2'b00
3:2	RO	0x0	reserved
1:0	RW	0x0	SEL_PF Register for Value of 2-bit Modulation Method Control. 00: Down spread 01: Up spread 1x: Center spread. PLL has to be reset if SEL_PF is changed.

DCPHY_M0_PLL_CON6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12	RW	0x0	CLK_BUFF_EN_SEL Clock Gating Disable Control Register. 1'b0: Clock gating function is available. 1'b1: Clock gating function is not available when PLL_WCLK_EN is asserted.
11:8	RW	0x0	WCLK_BUF_SFT_CNT Word Clock Buffer Shift Count Control Register. Please set this register as below. Roundup((Word Clock Period) / 38.46 + 2)
7	RW	0x0	PLL_TEST_DIV_EN PLL Test Divider Enable Control Register. For measuring frequency in ATE test environment, user can set this register and measure the divided clock frequency at the port "PLL_TEST_DIV_TM."
6	RW	0x0	D2A_CLK_BUF_EN_SEL D2A_CLK_BUF_EN Enable Selection Register. 1'b0: D2A_CLK_BUF_EN 1'b1: ENABLE(M%_DPHY_M#C_GNR_CON0)
5	RW	0x0	INTERNAL_LOOPBACK_EN Internal Loopback Test Enable Register. 1'b1: Internal Loopback Test
4	RW	0x0	M_RESETN_IQ_SEL M_RESETN Phase Control Register. 1'b0: I Phase 1'b1: Q Phase
3	RW	0x0	BITCLKDIV2_OUT_ENB Bit Clock /2 Divider Output Enable Control Register. 1'b0: Enable 1'b1: Disable
2	RW	0x0	BITCLKDIV4_OUT_ENB Bit Clock /4 Divider Output Enable Control Register. 1'b0: Enable 1'b1: Disable
1	RW	0x0	BITCLKDIV8_OUT_ENB Bit Clock /8 Divider Output Enable Control Register. 1'b0: Enable 1'b1: Disable
0	RW	0x0	BGR_REF_CLK_EN BGR_REF_CLK Output Enable Control Register. 1'b0: Disable 1'b1: Enable

DCPHY_M0_PLL_CON7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PLL_LOCK_CNT PLL Lock Timing Control Register. This reigster is the count value of PLL lock indication. When set the PLL_EN register, PHY lock counter starts to count. And when count value reaches to the value of this register, PLL_LOCK(M%_PLL_STAT0[0]) is set to HIGH. Generally, 200us is needed for locking the PLL.

DCPHY_M0_PLL_CON8

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PLL_STB_CNT PLL Stabilization Timing Control Register. This register is the count value of PLL stablization is done. When the signal PLL_CFG_UPDT is asserted for frequency hopping function, PHY stabilizing counter starts to count. And when count value reaches to the value of this register, the signal PLL_CFG_READY is set to HIGH. Generally, 100us is needed for stablizing PLL in frequency hopping.

DCPHY_M0_PLL_STAT0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	PLL_LOCK PLL Lock Indicate Register. This register is set when output clock of PLL is locked and ready to operate after setting PLL_EN. User can control setting timing of this register using PLL_LOCK_CNT(M0_PLL_CON7[15:0]) register. And user can control ENABLE register of each Lanes after PLL_LOCK is set.

DCPHY_M0_DPHY_MC_GNR_CON0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_M#C_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_MC_GNR_CON1

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_M#C_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_MC_ANA_CON0

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY 3'b111 In case of C-PHY 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_DPHY_MC_ANA_CON1
Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Releated with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00 : Default 2b'01 or 2b'10 : Decrease slew rate by 1% 2b'11 : Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_DPHY_MC_ANA_CON2

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	HS_VREG_AMP_ICON High Speed Voltage Regulator Current Control Register 2'b00 : Clock hstx enable HS VREG after lp sequence 2'b10 : Clock bias enable HS VREG after lane enable

DCPHY_M0_DPHY_MC_ANA_CON3

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	HIZ_EN Master dn/dp differential output floating mode enable register when hs_tx disable. 1b'0 = normal mode 1b'1 = hi-z mode
14:0	RO	0x0000	reserved

DCPHY_M0_DPHY_MC_TIME_CON0

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing speicfications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:0	RO	0x0	reserved

DCPHY_M0_DPHY_MC_TIME_CON1

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_CLK_ZERO TCLK-ZERO Timing Counter Register. This count value is used in High-Speed Transmit operation.
7:0	RW	0x00	T_CLK_PREPARE TCLK-PREPARE Timing Counter Register. This count value is used in High-Speed Transmit operation.

DCPHY_M0_DPHY_MC_TIME_CON2

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation.
7:0	RW	0x00	T_CLK_TRAIL TCLK-TRAIL Timing Counter Register. This count value is used in High-Speed Transmit operation.

DCPHY_M0_DPHY_MC_TIME_CON3

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_CLK_POST TCLK-POST Timing Counter Register. This count value is used in High-Speed Transmit operation.

DCPHY_M0_DPHY_MC_TIME_CON4

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_DPHY_MC_DATA_CON0

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RO	0x0	reserved

DCPHY_M0_DPHY_MC_DESKEW_CON0

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_RUN_TIME Periodic Skew Calibration Running Time Control Register. This count value is used in Periodic Skew Calibration. If this register is set to 0, the Periodic Skew Calibration running time is same as when set this register to 4'h4.
11:8	RW	0x0	SKEW_CAL_INIT_RUN_TIME Initial Skew Calibration Running Time Control Register. This count value is used in Initial Skew Calibration. If this register is set to 0, the Initial Skew Calibration running time is same as when set this register to 4'h7.
7:4	RW	0x0	SKEW_CAL_INIT_WAIT_TIME Initial Skew Calibration Waiting Time Control Register. This count value is used in Initial Skew Calibration. After power-on sequence, count will be started. If this register is set to 0, the Initial Skew Calibration is not goint to work.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register. This register enables Skew Calibration logic and circuits. For using Skew Calibration function through PPI "TXSKEWCALHS," set this register before enabling the lanes. If the operating data rate is 1.5Gbps or above, the Skew Calibration is madatory function.

DCPHY_M0_COMBO_MD0_GNR_CON0

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(COMBO_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_MD0_GNR_CON1
Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(COMBO_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_MD0_ANA_CON0
Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY 3'b111 In case of C-PHY 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.

Bit	Attr	Reset Value	Description
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_COMBO_MD0_ANA_CON1
Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.

Bit	Attr	Reset Value	Description
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Releated with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00 : Default 2b'01 or 2b'10 : Decrease slew rate by 1% 2b'11 : Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_COMBO_MD0_ANA_CON2

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

DCPHY_M0_COMBO_MD0_TIME_CON0
Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing speicfications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_COMBO_MD0_TIME_CON1
Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_COMBO_MD0_TIME_CON2
Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD0_TIME_CON3
Address: Operational Base + offset (0x043C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD0_TIME_CON4
Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_COMBO_MD0_DATA_CON0
Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:6	RO	0x0	reserved
5	RW	0x0	LPTX_SWAP Low-Power Signal Swap Control Register. This register is only valid in C-PHY mode. When this register is set to HIGH, the Low-Power signal output A/C will be swapped.
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol input will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON0
Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	PROG_SEQ_EN Programmable Sequence Enable Register. When this register is set to HIGH, Programmable Sequence of the Preamble is used as setting value in PROG_SEQ{COMBO_M#D#_PRGSEQ_CON1[9:0], COMBO_M#D#_PRGSEQ_CON2[15:0], COMBO_M#D#_PRGSEQ_CON3[15:0]}.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON1
Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON2
Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD0_PRGSEQ_CON3
Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD1_GNR_CON0
Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(COMBO_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_MD1_GNR_CON1
Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(COMBO_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_MD1_ANA_CON0
Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY 3'b111 In case of C-PHY 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_COMBO_MD1_ANA_CON1

Address: Operational Base + offset (0x050C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Releated with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00 : Default 2b'01 or 2b'10 : Decrease slew rate by 1% 2b'11 : Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_COMBO_MD1_ANA_CON2

Address: Operational Base + offset (0x0510)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.

Bit	Attr	Reset Value	Description
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

DCPHY_M0_COMBO_MD1_TIME_CON0
Address: Operational Base + offset (0x0530)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing speicfications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_COMBO_MD1_TIME_CON1
Address: Operational Base + offset (0x0534)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_COMBO_MD1_TIME_CON2
Address: Operational Base + offset (0x0538)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD1_TIME_CON3
Address: Operational Base + offset (0x053C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD1_TIME_CON4
Address: Operational Base + offset (0x0540)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_COMBO_MD1_DATA_CON0

Address: Operational Base + offset (0x0544)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:6	RO	0x0	reserved
5	RW	0x0	LPTX_SWAP Low-Power Signal Swap Control Register. This register is only valid in C-PHY mode. When this register is set to HIGH, the Low-Power signal output A/C will be swapped.
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol input will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON0

Address: Operational Base + offset (0x0560)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	PROG_SEQ_EN Programmable Sequence Enable Register. When this register is set to HIGH, Programmable Sequence of the Preamble is used as setting value in PROG_SEQ{COMBO_M#D#_PRGSEQ_CON1[9:0], COMBO_M#D#_PRGSEQ_CON2[15:0], COMBO_M#D#_PRGSEQ_CON3[15:0]}.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON1

Address: Operational Base + offset (0x0564)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON2

Address: Operational Base + offset (0x0568)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD1_PRGSEQ_CON3

Address: Operational Base + offset (0x056C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD2_GNR_CON0

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(COMBO_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_MD2_GNR_CON1

Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(COMBO_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_MD2_ANA_CON0

Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY 3'b111 In case of C-PHY 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_COMBO_MD2_ANA_CON1
Address: Operational Base + offset (0x060C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RO	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Releated with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00 : Default 2b'01 or 2b'10 : Decrease slew rate by 1% 2b'11 : Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_COMBO_MD2_ANA_CON2

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.

Bit	Attr	Reset Value	Description
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

DCPHY_M0_COMBO_MD2_TIME_CON0

Address: Operational Base + offset (0x0630)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing speicfications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_COMBO_MD2_TIME_CON1

Address: Operational Base + offset (0x0634)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_COMBO_MD2_TIME_CON2

Address: Operational Base + offset (0x0638)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD2_TIME_CON3

Address: Operational Base + offset (0x063C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_COMBO_MD2_TIME_CON4

Address: Operational Base + offset (0x0640)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_COMBO_MD2_DATA_CON0
Address: Operational Base + offset (0x0644)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:6	RO	0x0	reserved
5	RW	0x0	LPTX_SWAP Low-Power Signal Swap Control Register. This register is only valid in C-PHY mode. When this register is set to HIGH, the Low-Power signal output A/C will be swapped.
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol input will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON0
Address: Operational Base + offset (0x0660)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	PROG_SEQ_EN Programmable Sequence Enable Register. When this register is set to HIGH, Programmable Sequence of the Preamble is used as setting value in PROG_SEQ{COMBO_M#D#_PRGSEQ_CON1[9:0], COMBO_M#D#_PRGSEQ_CON2[15:0], COMBO_M#D#_PRGSEQ_CON3[15:0]}.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON1
Address: Operational Base + offset (0x0664)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON2
Address: Operational Base + offset (0x0668)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_COMBO_MD2_PRGSEQ_CON3
Address: Operational Base + offset (0x066C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	PROG_SEQ Programmable Sequence Register. When PROG_SEQ_EN(COMBO_M#D#_PRGSEQ_CON0[0]) is set to HIGH, the 7-symbol set as the registers COMBO_M#D#_PRGSEQ_CON1~3 is output Programmable Sequence of the Preamble.

DCPHY_M0_DPHY_MD3_GNR_CON0
Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_M#D#_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_MD3_GNR_CON1
Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_M#D#_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_MD3_ANA_CON0
Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x7	EDGE_CON Cap Peaking Control Register. Set the register as below. In case of D-PHY 3'b111 In case of C-PHY 3'b001
11:10	RO	0x0	reserved
9	RW	0x0	EDGE_CON_DIR Cap Peaking Direction Control Register. Set the register as below. In case of D-PHY,1'b0 In case of C-PHY,1'b1
8	RW	0x1	EDGE_CON_EN Cap Peaking Enable Register.
7:4	RW	0x3	RES_UP High-Speed Driver Up Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm
3:0	RW	0x3	RES_DN High-Speed Driver Down Resistor Control Register. 4'b0000: 43 ohm 4'b0001: 46 ohm 4'b0010: 49 ohm 4'b0011: 52 ohm 4'b0100: 56 ohm 4'b0101: 60 ohm 4'b0110: 66 ohm 4'b0111: 73 ohm 4'b1000: 30 ohm 4'b1001: 31.2 ohm 4'b1010: 32.5 ohm 4'b1011: 34 ohm 4'b1100: 35.5 ohm 4'b1101: 37 ohm 4'b1110: 39 ohm 4'b1111: 41 ohm

DCPHY_M0_DPHY_MD3_ANA_CON1
Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	IQ_RESETN_POL_CON I-Q Clock Polarity Control Register.
14	RW	0x0	VREG12_VALID 1.2V Voltage Regulator Valid Control Register.
13	RW	0x0	VREG12_VALID_SEL 1.2V Voltage Regulator Valid Select Register.
12	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.
11	RW	0x0	ATB_SEL_GND Analog Test Bus Select for SER Ground Register.
10	RW	0x0	ATB_SEL_VDD Analog Test Bus Select for SER Power Register.
9:8	RW	0x0	LPTX_SR_UP Low-Power TX Driver Slew Rate Up Enable Register. Releated with LPTX_SR_CTRL Register. 2b'1X : Max slew rate 2b'0X : Default
7:6	RO	0x0	reserved
5:4	RW	0x0	LPTX_SR_CTRL Low-Power TX Driver Slew Rate Control Register. When LPTX_SR_UP is 2b'0X, 2b'00 : Default 2b'01 or 2b'10 : Decrease slew rate by 1% 2b'11 : Decrease slew rate by 2%
3:2	RO	0x0	reserved
1:0	RW	0x0	EMP De-Emphasis Control Register. In case of D-PHY: Data Rate >=4.5Gbps: 2'b01 Data Rate < 4.5Gbps: 2'b00 2'b00: 0 dB 2'b01: -1.5 dB 2'b10: -3.5 dB 2'b11: -6.5 dB In case of C-PHY, Data Rate <= 2Gsps 2'b00: 0dB 2'b01: NA 2'b10: NA 2'b11: NA

DCPHY_M0_DPHY_MD3_ANA_CON2

Address: Operational Base + offset (0x0710)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	LPRX_HYS_SEL Low-Power RX Hysterisis Select Register.
11	RO	0x0	reserved
10:8	RW	0x0	DTB_SEL Digital Test Bus Select Register.
7	RW	0x0	CNT_REJECTION_PULSE Pulse Rejection Control Register.

Bit	Attr	Reset Value	Description
6	RW	0x0	SEL_ESCPOL Escape Mode Clock Polarity Select Register.
5	RW	0x0	SEL_VREF Reference Voltage Select Register.
4	RW	0x0	CNT_ULPSHYS ULPS Hysterisis Control Register.
3	RW	0x0	EN_RSTN_SEL Reset Enable Select Register.
2	RW	0x0	PULSE_REJ_ENB Pulse Rejection Enable Register.
1	RW	0x0	LPCD_HYS_SEL Low-Power Contention Detect Hysterisis Select Register.
0	RW	0x0	DPDN_SWAP DP/DN Swap Control Register.

DCPHY_M0_DPHY_MD3_TIME_CON0

Address: Operational Base + offset (0x0730)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	HSTX_CLK_SEL HS-TX State Machine Clock Select Register. HS-TX Clock is used for counting some of timing speicfications. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
11:4	RW	0x00	T_LPX TLPX Timing Counter Register. This count value is specially used in High-Speed Transmit operation
3:2	RW	0x0	T_LP_EXIT_SKEW High-Speed Data Transmission End-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the End-of-Transmission procedure of High-Speed Data Transmission.
1:0	RW	0x0	T_LP_ENTRY_SKEW High-Speed Data Transmission Start-of-Transmission Low-Power Signal Skew Control Register. This register is used for making the skew of Low-Power Signals of Data Lanes in the Start-of-Transmission procedure of High-Speed Data Transmission.

DCPHY_M0_DPHY_MD3_TIME_CON1

Address: Operational Base + offset (0x0734)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_ZERO THS-ZERO (D-PHY) / T3-PREBEGIN (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	T_HS_PREPARE THS-PREPARE (D-PHY) / T3-PREPARE (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance..

DCPHY_M0_DPHY_MD3_TIME_CON2
Address: Operational Base + offset (0x0738)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	T_HS_EXIT THS-EXIT Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.
7:0	RW	0x00	T_HS_TRAIL THS-TRAIL (D-PHY) / T3-POST (C-PHY) Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" or "Specification for C-PHYSM" of mipi alliance.

DCPHY_M0_DPHY_MD3_TIME_CON3
Address: Operational Base + offset (0x073C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	T_TA_GET TTA-GET Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.
3:0	RW	0x0	T_TA_GO TTA-GO Timing Counter Register. This count value is used in Turn-around operation. For getting detailed information of this timing specification, please refer to "Specification of D-PHYSM" or "Specification of C-PHYSM" of mipi alliance.

DCPHY_M0_DPHY_MD3_TIME_CON4
Address: Operational Base + offset (0x0740)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	T_ULPS_EXIT Ultra-Low Power Exit Timing Counter Register. This count value is used in Ultra-Low Power operation. For exiting Ultra-Low Power State, the Link layer can set PPI signal "TXULPSEXIT" to HIGH. There are two conditions for moving the state of PHY to "TX-ULPS-Exit." One is that the Link layer control PPI signal "TXULPSCLK" to LOW. Another way is to use the counter in PHY.

DCPHY_M0_DPHY_MD3_DATA_CON0
Address: Operational Base + offset (0x0744)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	ERR_CONTENTION_DISABLE Contention Error Detect Disable Control Register. When this register is set to HIGH, the contention error will not occur through "ERRCONTENTIONLP0/1."
11:9	RO	0x0	reserved
8	RW	0x0	TRIG_EXIT_CLK_EN Trigger Mode Exit Clock Toggle Enable Register. When this register is set to HIGH, after transmitting the trigger command, DP signal is toggled as period of Escape mode clock until "TXREQUESTESC" goes to LOW.
7:2	RO	0x00	reserved
1	RW	0x0	CLK_INV Clock Inversion Control Register. When this register is set to HIGH, the clock output of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data input will be swapped.

DCPHY_M0_DPHY_SC_GNR_CON0
Address: Operational Base + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#C_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_SC_GNR_CON1
Address: Operational Base + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#C_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_SC_ANA_CON0
Address: Operational Base + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_DPHY_SC_ANA_CON1

Address: Operational Base + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0:550uA 1'b1:650uA [14:13]: 2nd stage amp bias current 2'b00:500uA 2'b01:550uA 2'b10:600uA 2'b11:650uA [12:11]: 1st stage amp bias current 2'b00:700uA 2'b01:850uA 2'b10:350uA 2'b11:500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. 5'b00000: forbidden (infinite resistance) 5b'00001: 330 Ohm 5b'00100: 660 Ohm 5b'01000: 1.3k Ohm 5b'01100: 440 Ohm 5b'01111: 130 Ohm (min) 5b'10000: 2.6k Ohm (max) 5b'10100: 530 Ohm 5b'10101: 200 Ohm 24d~31d: forbidden
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz ** MSB[2]: gain/freq control of 2nd amp

DCPHY_M0_DPHY_SC_ANA_CON2
Address: Operational Base + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CLK_HSRX_ENABLE_MAN CLK_HSRX_ENABLE, Only Test mode for DPHY
14:12	RO	0x0	reserved
11	RW	0x0	CLK_TERM_EN_MAN CLK Term enable, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal 1'b1: Test mode
9:8	RW	0x0	CLK_DIV1234_MC clk div 1/2/3/4 ctrl, 2'b00: Div4 2'b01: Div3 2'b10: Div2 2'b11: Div1
7	RW	0x0	SKEWCAL_CLK_SEL Skew Calibration Clock Rate Control Register. 1'b0: Fin/8 1'b1: Fin/4 Fin is input clock speed.
6	RO	0x0	reserved
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	HS_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_DPHY_SC_ANA_CON3
Address: Operational Base + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal, 1'b1: Swap

Bit	Attr	Reset Value	Description
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS Ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_DPHY_SC_ANA_CON4

Address: Operational Base + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x0	CLK_DBL_CTRL clk doubler pulse width ctrl, 2'b00: 1nS 2'b01: 2nS 2'b10: 3nS 2'b11: 4ns
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:8	RO	0x0	reserved
7	RW	0x0	ATB_SEL_VREF ATB Enable, 1'b0: Switch off, 1'b1: Switch on(Vref 645MV)
6	RW	0x0	VREF_BGRVDD_SEL Slave Reference Voltage 520mV Selection Control, 1'b0: BGR, 1'b1: R-ladder
5:4	RW	0x0	LP_VREF520_SW ULPS reference voltage option selection
3:0	RW	0x0	ATB_SEL_DMY ATB Enable, 1'b0: Switch off, 1'b1: Switch on(AVSS, AVSS, AVDDL, AVSS)

DCPHY_M0_DPHY_SC_ANA_CON5

Address: Operational Base + offset (0x0B1C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CLK_MISS_DISABLE Clock Miss Disable Control Register.
14:12	RO	0x0	reserved
11	RW	0x0	NON_MIPI_ENABLE 1'b0: Non mipi feature disable 1'b1: Non mipi feature enable
10	RO	0x0	reserved
9:0	RW	0x000	RXBIAS_CNT Slave DPHY I bias ctrl, ([1:0]-SD0, [3:2]-SD1, [5:4]-SD2, [7:6]-SD3, [9:8]-SC) 2'b00: 50uA 2'b01: 37.5uA 2'b10: 37.5uA 2'b11: 25uA

DCPHY_M0_DPHY_SC_TIME_CON0

Address: Operational Base + offset (0x0B30)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	T_CLK_MISS Clock Miss Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting Clock Miss. If the clock is not detected in Slave Clock Lane until the watchdog timer is expired, then internal flag is set. Please refer to "Supplement Guide" for setting this register.
7:0	RW	0x00	T_CLK_SETTLE TCLK-SETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD0_GNR_CON0
Address: Operational Base + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D0_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_SD0_GNR_CON1
Address: Operational Base + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D0_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_SD0_ANA_CON0
Address: Operational Base + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_COMBO_SD0_ANA_CON1

Address: Operational Base + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. In case of DPHY 5'b00000: Forbidden (infinite resistance) 5b'00101: 200 Ohm 5b'00001: 300 Ohm 5b'00010: 400 Ohm 5b'10100: 480 Ohm 5b'00100: 600 Ohm 5b'11000: 800 Ohm In case of CPHY 5'b00000: Forbidden (infinite resistance) 5b'01111: 220 Ohm 5b'00110: 280 Ohm 5b'10010: 430 Ohm 5b'10100: 600 Ohm 5b'00100: 700 Ohm 5b'00001: 1300 Ohm
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. ** MSB[3]: gain/freq control of 2nd amp In case of DPHY 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz In case of CPHY 4'b0000: Small capacitance 4'b0001: Large capacitance HS_RX_CAPCNT[1:0]: Reserved

DCPHY_M0_COMBO_SD0_ANA_CON2

Address: Operational Base + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal, DPHY only. 0x0: Fine delay 0x1: Bypass
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, DPHY only. 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <= Data Rate <= 6.5Gbps: 2'b00 3.0Gbps <= Data Rate < 4.0Gbps: 2'b01 2.0Gbps <= Data Rate < 3.0Gbps: 2'b10 1.5Gbps <= Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_COMBO_SD0_ANA_CON3

Address: Operational Base + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	EN_RSTN_SEL Internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder

Bit	Attr	Reset Value	Description
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_COMBO_SD0_ANA_CON4
Address: Operational Base + offset (0x0C18)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:0	RO	0x000	reserved

DCPHY_M0_COMBO_SD0_ANA_CON6
Address: Operational Base + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DL_COMP_CTRL UI mask code output control - sec control
7:6	RO	0x0	reserved
5:4	RW	0x0	UI_MASK_CTRL UI Mask control - sec control
3	RW	0x0	EXT_DL_MUX_EN 1UI data sampling type - sec control
2:0	RO	0x0	reserved

DCPHY_M0_COMBO_SD0_ANA_CON7
Address: Operational Base + offset (0x0C24)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	CLK_DBL_CTRL XI to doubler clock delay cotrol - sec control
5:0	RO	0x00	reserved

DCPHY_M0_COMBO_SD0_TIME_CON0
Address: Operational Base + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD0_TIME_CON1
Address: Operational Base + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_COMBO_SD0_DATA_CON0
Address: Operational Base + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol data will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_COMBO_SD0_DESKEW_CON0
Address: Operational Base + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON1
Address: Operational Base + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.

Bit	Attr	Reset Value	Description
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON2
Address: Operational Base + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON3
Address: Operational Base + offset (0x0C4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_COMBO_SD0_DESKEW_CON4
Address: Operational Base + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

DCPHY_M0_COMBO_SD0_CRC_CON0
Address: Operational Base + offset (0x0C60)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:4	RW	0x00	CRC_FORCE_CODE CRC Forcing Mode Code Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	CRC_FORCE_CODE_EN CRC Forcing Mode Enable Register.

DCPHY_M0_COMBO_SD0_CRC_CON1
Address: Operational Base + offset (0x0C64)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CRC_POST_GATING_CNT CRC Post Gating Count Register.

Bit	Attr	Reset Value	Description
7	RW	0x0	CRC_POST_GATING_EN CRC Post Gating Enable Register.
6:4	RW	0x0	CRC_SETTLE_MASK_SEL CRC Clock Polarity Control Register.
3	RW	0x0	CRC_POL_SEL CRC Clock Polarity Control Register.
2	RW	0x0	CRC_SOT_SYNC_ERR_CHK CRC SoT Sync Error Check Enable Register.
1:0	RW	0x0	CRC_AVG_SEL CRC Code Average Select Register.

DCPHY_M0_COMBO_SD0_CRC_CON2
Address: Operational Base + offset (0x0C68)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	CRC_BURST_CNT CRC Multiple Burst Count for Average Code Register.
11:9	RO	0x0	reserved
8	RW	0x0	CRC_CODE_FIX CRC Code Fix Control Register.
7:4	RW	0x0	CRC_CODE_TOL CRC Code Tolerance Control Register.
3:0	RW	0x0	CRC_CODE_TUNE CRC Code Tuning Register.

DCPHY_M0_COMBO_SD1_GNR_CON0
Address: Operational Base + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D1_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_SD1_GNR_CON1
Address: Operational Base + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D1_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_SD1_ANA_CON0
Address: Operational Base + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_COMBO_SD1_ANA_CON1

Address: Operational Base + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. In case of DPHY 5'b00000: Forbidden (infinite resistance) 5b'00101: 200 Ohm 5b'00001: 300 Ohm 5b'00010: 400 Ohm 5b'10100: 480 Ohm 5b'00100: 600 Ohm 5b'11000: 800 Ohm In case of CPHY 5'b00000: Forbidden (infinite resistance) 5b'01111: 220 Ohm 5b'00110: 280 Ohm 5b'10010: 430 Ohm 5b'10100: 600 Ohm 5b'00100: 700 Ohm 5b'00001: 1300 Ohm

Bit	Attr	Reset Value	Description
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. ** MSB[3]: gain/freq control of 2nd amp In case of DPHY 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz In case of CPHY 4'b0000: Small capacitance 4'b0001: Large capacitance HS_RX_CAPCNT[1:0]: Reserved

DCPHY_M0_COMBO_SD1_ANA_CON2
Address: Operational Base + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal, DPHY only. 0x0: Fine delay 0x1: Bypass
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, DPHY only. 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <= Data Rate <= 6.5Gbps: 2'b00 3.0Gbps <= Data Rate < 4.0Gbps: 2'b01 2.0Gbps <= Data Rate < 3.0Gbps: 2'b10 1.5Gbps <= Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_COMBO_SD1_ANA_CON3
Address: Operational Base + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL Internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable

Bit	Attr	Reset Value	Description
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_COMBO_SD1_ANA_CON4
Address: Operational Base + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:0	RO	0x000	reserved

DCPHY_M0_COMBO_SD1_ANA_CON6
Address: Operational Base + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DL_COMP_CTRL UI mask code output control - sec control
7:6	RO	0x0	reserved
5:4	RW	0x0	UI_MASK_CTRL UI Mask control - sec control
3	RW	0x0	EXT_DL_MUX_EN 1UI data sampling type - sec control
2:0	RO	0x0	reserved

DCPHY_M0_COMBO_SD1_ANA_CON7
Address: Operational Base + offset (0x0D24)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	CLK_DBL_CTRL XI to doubler clock delay cotrol - sec control
5:0	RO	0x00	reserved

DCPHY_M0_COMBO_SD1_TIME_CON0

Address: Operational Base + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD1_TIME_CON1

Address: Operational Base + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_COMBO_SD1_DATA_CON0

Address: Operational Base + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol data will be swapped.
3:2	RO	0x0	reserved
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_COMBO_SD1_DESKEW_CON0

Address: Operational Base + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON1
Address: Operational Base + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON2
Address: Operational Base + offset (0x0D48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON3
Address: Operational Base + offset (0x0D4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_COMBO_SD1_DESKEW_CON4
Address: Operational Base + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

DCPHY_M0_COMBO_SD1_CRC_CON0
Address: Operational Base + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:4	RW	0x00	CRC_FORCE_CODE CRC Forcing Mode Code Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	CRC_FORCE_CODE_EN CRC Forcing Mode Enable Register.

DCPHY_M0_COMBO_SD1_CRC_CON1
Address: Operational Base + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CRC_POST_GATING_CNT CRC Post Gating Count Register.
7	RW	0x0	CRC_POST_GATING_EN CRC Post Gating Enable Register.
6:4	RW	0x0	CRC_SETTLE_MASK_SEL CRC Clock Polarity Control Register.
3	RW	0x0	CRC_POL_SEL CRC Clock Polarity Control Register.
2	RW	0x0	CRC_SOT_SYNC_ERR_CHK CRC SoT Sync Error Check Enable Register.
1:0	RW	0x0	CRC_AVG_SEL CRC Code Average Select Register.

DCPHY_M0_COMBO_SD1_CRC_CON2
Address: Operational Base + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	CRC_BURST_CNT CRC Multiple Burst Count for Average Code Register.
11:9	RO	0x0	reserved
8	RW	0x0	CRC_CODE_FIX CRC Code Fix Control Register.
7:4	RW	0x0	CRC_CODE_TOL CRC Code Tolerance Control Register.
3:0	RW	0x0	CRC_CODE_TUNE CRC Code Tuning Register.

DCPHY_M0_COMBO_SD2_GNR_CON0
Address: Operational Base + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D2_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_COMBO_SD2_GNR_CON1
Address: Operational Base + offset (0x0E04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D2_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_COMBO_SD2_ANA_CON0

Address: Operational Base + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_COMBO_SD2_ANA_CON1

Address: Operational Base + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. In case of DPHY 5'b00000: Forbidden (infinite resistance) 5b'00101: 200 Ohm 5b'00001: 300 Ohm 5b'00010: 400 Ohm 5b'10100: 480 Ohm 5b'00100: 600 Ohm 5b'11000: 800 Ohm In case of CPHY 5'b00000: Forbidden (infinite resistance) 5b'01111: 220 Ohm 5b'00110: 280 Ohm 5b'10010: 430 Ohm 5b'10100: 600 Ohm 5b'00100: 700 Ohm 5b'00001: 1300 Ohm
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. ** MSB[3]: gain/freq control of 2nd amp In case of DPHY 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz In case of CPHY 4'b0000: Small capacitance 4'b0001: Large capacitance HS_RX_CAPCNT[1:0]: Reserved

DCPHY_M0_COMBO_SD2_ANA_CON2

Address: Operational Base + offset (0x0E10)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal, DPHY only. 0x0: Fine delay 0x1: Bypass
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, DPHY only. 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode

Bit	Attr	Reset Value	Description
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <= Data Rate <= 6.5Gbps: 2'b00 3.0Gbps <= Data Rate < 4.0Gbps: 2'b01 2.0Gbps <= Data Rate < 3.0Gbps: 2'b10 1.5Gbps <= Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_COMBO_SD2_ANA_CON3

Address: Operational Base + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL Internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal 1'b1: Swap

Bit	Attr	Reset Value	Description
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL Rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_COMBO_SD2_ANA_CON4
Address: Operational Base + offset (0x0E18)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:0	RO	0x000	reserved

DCPHY_M0_COMBO_SD2_ANA_CON6
Address: Operational Base + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	DL_COMP_CTRL UI mask code output control - sec control
7:6	RO	0x0	reserved
5:4	RW	0x0	UI_MASK_CTRL UI Mask control - sec control
3	RW	0x0	EXT_DL_MUX_EN 1UI data sampling type - sec control
2:0	RO	0x0	reserved

DCPHY_M0_COMBO_SD2_ANA_CON7
Address: Operational Base + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	CLK_DBL_CTRL XI to doubler clock delay cotrol - sec control
5:0	RO	0x00	reserved

DCPHY_M0_COMBO_SD2_TIME_CON0
Address: Operational Base + offset (0x0E30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_COMBO_SD2_TIME_CON1
Address: Operational Base + offset (0x0E34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_COMBO_SD2_DATA_CON0
Address: Operational Base + offset (0x0E38)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SYMBOL_SWAP Symbol Swap Control Register. When this register is set to HIGH, 7-symbol data will be swapped.
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_COMBO_SD2_DESKEW_CON0

Address: Operational Base + offset (0x0E40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON1

Address: Operational Base + offset (0x0E44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON2

Address: Operational Base + offset (0x0E48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON3

Address: Operational Base + offset (0x0E4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_COMBO_SD2_DESKEW_CON4
Address: Operational Base + offset (0x0E50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

DCPHY_M0_COMBO_SD2_CRC_CON0
Address: Operational Base + offset (0x0E60)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:4	RW	0x00	CRC_FORCE_CODE CRC Forcing Mode Code Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	CRC_FORCE_CODE_EN CRC Forcing Mode Enable Register.

DCPHY_M0_COMBO_SD2_CRC_CON1
Address: Operational Base + offset (0x0E64)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CRC_POST_GATING_CNT CRC Post Gating Count Register.
7	RW	0x0	CRC_POST_GATING_EN CRC Post Gating Enable Register.
6:4	RW	0x0	CRC_SETTLE_MASK_SEL CRC Clock Polarity Control Register.
3	RW	0x0	CRC_POL_SEL CRC Clock Polarity Control Register.
2	RW	0x0	CRC_SOT_SYNC_ERR_CHK CRC SoT Sync Error Check Enable Register.
1:0	RW	0x0	CRC_AVG_SEL CRC Code Average Select Register.

DCPHY_M0_COMBO_SD2_CRC_CON2
Address: Operational Base + offset (0x0E68)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	CRC_BURST_CNT CRC Multiple Burst Count for Average Code Register.
11:9	RO	0x0	reserved
8	RW	0x0	CRC_CODE_FIX CRC Code Fix Control Register.
7:4	RW	0x0	CRC_CODE_TOL CRC Code Tolerance Control Register.
3:0	RW	0x0	CRC_CODE_TUNE CRC Code Tuning Register.

DCPHY_M0_DPHY_SD3_GNR_CON0
Address: Operational Base + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	PHY_READY PHY Ready Indicate Register. This register is set when PHY is ready to operate after stablizing biasing. User can control setting timing of this register using T_PHY_READY(DPHY_S#D3_GNR_CON1[15:0]) register. And user should release the RESETN of the Lane after all of PHY_READY register in lanes are set.
0	RW	0x0	ENABLE PHY Enable Register. For using Lane, user can set this register after PLL is locked.

DCPHY_M0_DPHY_SD3_GNR_CON1
Address: Operational Base + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	T_PHY_READY PHY Ready Timing Control Register. This register is the count value of PHY ready indication. When set the ENABLE register, PHY ready counter starts to count. And when count value reaches to the value of this register, PHY_READY(DPHY_S#D3_GNR_CON0[1]) is set to HIGH. Generally, 200us is needed for stablizing the bias and the ready counter operates with Reference Clocks.

DCPHY_M0_DPHY_SD3_ANA_CON0
Address: Operational Base + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	HS_RX_CNT_ROUT Output Resistor of HSRX AFE's 1st Stage Amp 3'b000: 282 Ohm 3'b001: 188 Ohm 3'b011: 141 Ohm 3'b100: 565 Ohm

DCPHY_M0_DPHY_SD3_ANA_CON1
Address: Operational Base + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x00	HS_RX_BIAS_CON [15]: Diff to CMOS Level shifter's current 1'b0: 550uA 1'b1: 650uA [14:13]: 2nd stage amp bias current 2'b00: 500uA 2'b01: 550uA 2'b10: 600uA 2'b11: 650uA [12:11]: 1st stage amp bias current 2'b00: 700uA 2'b01: 850uA 2'b10: 350uA 2'b11: 500uA
10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	HS_RX_FLATBAND EQ On/Off Control Register. 1'b0: EQ off, 1'b1: EQ on
8	RO	0x0	reserved
7:4	RW	0x0	HS_RX_RSELCNT EQ Resistor Control Register. 5'b00000: Forbidden (infinite resistance) 5b'00001: 330 Ohm 5b'00100: 660 Ohm 5b'01000: 1.3k Ohm 5b'01100: 440 Ohm 5b'01111: 130 Ohm (min) 5b'10000: 2.6k Ohm (max) 5b'10100: 530 Ohm 5b'10101: 200 Ohm 24d~31d: Forbidden
3:0	RW	0x0	HS_RX_CAPCNT EQ Capacitor Control (Covered Freq.) Register. 4'b0000: 7.43GHz 4'b0001: 4.82GHz 4'b0010: 4.09GHz 4'b0011: 3.58GHz 4'b0100: 3.44GHz 4'b0101: 3.12GHz 4'b0110: 2.87GHz 4'b0111: 2.7GHz ** MSB[2]: gain/freq control of 2nd amp

DCPHY_M0_DPHY_SD3_ANA_CON2

Address: Operational Base + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	RESETN_CFG_SEL Reset Selection Register for 2+2 Configuration 1'b0: 4-Lane 1'b1: 2+2 Lane
14	RW	0x0	SEL_FDLY Fine delay on/off control pin for skew cal 0x0: Fine delay 0x1: Bypass
13:12	RW	0x0	UDLY_SPDCNT Fine delay selection for Skew cal, 2'b00: 4.89ps, 2'b10: 7.72ps
11	RW	0x0	HS_TERM_EN_MAN TERM_ENABLE, Only Test mode for DPHY
10	RW	0x0	HSMODE_MAN_SEL Only Test mode for DPHY, 1'b0: Normal, 1'b1: Test mode

Bit	Attr	Reset Value	Description
9:8	RW	0x0	SKEW_DLYSEL Set the register as below. 4.0Gbps <: Data Rate <: 6.5Gbps: 2'b00 3.0Gbps <: Data Rate < 4.0Gbps: 2'b01 2.0Gbps <: Data Rate < 3.0Gbps: 2'b10 1.5Gbps <: Data Rate < 2.0Gbps: 2'b11 2'b00 for the rest.
7	RW	0x0	RXDDRCLKHS_SEL Clock selection pin for Data patch clock 0x0: CLK1 0x1: CLK2
6	RW	0x0	SKEW_CAL_EXT_FORCE Manual Skew Calibration control 0x0: Disable 0x1: Enable
5	RW	0x0	HS_UNTERM_EN Termination control pin for DPHY HS-RX, 1'b0: Term, 1'b1: Un-Term
4:3	RO	0x0	reserved
2:0	RW	0x0	RX_TERM_SW HS-RX Termination Impedance Control 3b'000: 102 Ohm 3b'001: 99.1 Ohm 3b'010: 96.6 Ohm (default) 3b'011: 94.1 Ohm 3b'100: 113 Ohm 3b'101: 110 Ohm 3b'110: 107 Ohm 3b'111: 104 Ohm

DCPHY_M0_DPHY_SD3_ANA_CON3
Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	EN_RSTN_SEL internal resetn sel. 0x0: Enabel_D2A 0x1: ResetN_D2A
14	RW	0x0	DPDN_SWAP DPDN swap, 1'b0: Normal, 1'b1: Swap
13:12	RW	0x0	HS_DELAY_CON Clk delay control for loopback test at Clock lane 2'b00: 20pS 2'b01: 40pS 2'b10: 60pS 2'b11: 80pS
11	RW	0x0	SEL_ESCPOL LP ESCCLK Polarity sel 1'b0: Normal, 1'b1: Swap

Bit	Attr	Reset Value	Description
10:8	RW	0x0	ULPS_HYS_SW_DPHY ULPS Hysterisis Level Control 3'b000: 126mV 3'b001: 135mV 3'b010: 143mV 3'b011: 150mV 3'b100: 64.6mV 3'b101: 82.2mV 3'b110: 104mV 3'b111: 117mV
7	RW	0x0	CNT_REJECT_PULSE LP Pulse Reject Time Control 1b'0: Default 1b'1: Smaller Reject Time
6	RW	0x0	LP_EN_PRECHARGE_SEL LPRX Pre-charge Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
5:4	RW	0x0	LP_HYS_SW LP-RX Hysteresis Level Control 2'b00: 45mV 2'b01: 65mV 2'b10: 85mV 2'b11: 100mV
3	RW	0x0	PULSE_REJ_ENB Pulse Rejecter Enable/Disable Control, 1'b0: Enable, 1'b1: Disable
2	RW	0x0	CULPS_HYS ulps vref sel, 1'b0: Self bias, 1'b1: From r-ladder
1:0	RW	0x0	LPRX_BIAS_CTRL rx normal LP bias sel, 2'b00: 25uA 2'b01: 35uA 2'b10: 20uA 2'b11: 25uA

DCPHY_M0_DPHY_SD3_ANA_CON4

Address: Operational Base + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	REG05_11 Forcing HS-RX Mode Enable/Disable Control 0x0: Disable 0x1: Enable
10:6	RO	0x00	reserved
5:4	RW	0x0	ATB_SEL_POWER_IR ULPS reference voltage option selection
3:0	RW	0x0	ATB_SEL_DMY ATB Enable, 1'b0: Switch off, 1'b1: Switch on(AVSS, AVSS, AVDDL, AVSS)

DCPHY_M0_DPHY_SD3_ANA_CON5
Address: Operational Base + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	DESER_DELAY_ENABLE 1'b0 : Deserializer enable delay off 1'b1 : Deserializer enable delay on
11	RW	0x0	NON_MIPI_ENABLE 1'b0 : Non mipi feature disable 1'b1 : Non mipi feature enable
10:0	RO	0x000	reserved

DCPHY_M0_DPHY_SD3_TIME_CON0
Address: Operational Base + offset (0x0F30)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	SETTLE_CLK_SEL Settle Counter Clock Select Register. Settle Clock is used for counting TCLK-SETTLE. 1'b0: Divide-by-16 Clock from Serial Clock. Use this when data rate is 1500Mbps or above. 1'b1: Divide-by-2 Clock from Serial Clock. Use this when data rate is under 1500Mbps.
7:0	RW	0x00	T_HS_SETTLE TSETTLE Timing Counter Register. This count value is used in High-Speed Transmit operation. For getting detailed information of this timing specification, please refer to "Specification for D-PHYSM" of mipi alliance. And please refer to "Supplement Guide" for setting this register according to data rate.

DCPHY_M0_DPHY_SD3_TIME_CON1
Address: Operational Base + offset (0x0F34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	T_ERR_SOT_SYNC SoT Sync Error Detect Timing Control Register. This count value is used in High-Speed Transmit operation. There is a watchdog timer in Receive logic for detecting SoT Sync Error. If the Sync Pattern is not detected until the watchdog timer is expired, then the PPI signal "ERRSOTSYNC" goes to HIGH.

DCPHY_M0_DPHY_SD3_DATA_CON0
Address: Operational Base + offset (0x0F38)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	DATA_INV Data Inversion Control Register. When this register is set to HIGH, the data input of DP/DN will be inverted.
0	RW	0x0	DATA_SWAP Data Swap Control Register. When this register is set to HIGH, 16-bit data output will be swapped.

DCPHY_M0_DPHY_SD3_DESKEW_CON0
Address: Operational Base + offset (0x0F40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SKEW_CAL_DES_SEL Skew Calibration Clock Division Ratio Control Register.
3:1	RO	0x0	reserved
0	RW	0x0	SKEW_CAL_EN Skew Calibration Enable Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON1
Address: Operational Base + offset (0x0F44)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	SKEW_CAL_FINAL_COMP_TIME Skew Calibration Final Compare Time Control Register.
7:6	RW	0x0	SKEW_CAL_COMP_TOL Skew Calibration Compare Tolerance Control Register.
5:4	RW	0x0	SKEW_CAL_COMP_WAIT_TIME Skew Calibration Compare Wait Time Control Register.
3:0	RW	0x0	SKEW_CAL_COMP_RUN_TIME Skew Calibration Compare Run Time Control Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON2
Address: Operational Base + offset (0x0F48)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	SKEW_CAL_DATA_COARSE_SET Skew Calibration Manual Data Coarse Delay Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_CLK_COARSE_SET Skew Calibration Manual Data Fine Delay Control Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON3
Address: Operational Base + offset (0x0F4C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	SKEW_CAL_DATA_FINE_FALL_SET Skew Calibration Manual Data Fine Falling Delay Control Register.
11:8	RW	0x0	SKEW_CAL_DATA_FINE_RISE_SET Skew Calibration Manual Data Fine Rising Delay Control Register.
7:4	RW	0x0	SKEW_CAL_CLK_FINE_FALL_SET Skew Calibration Manual Clock Fine Falling Delay Control Register.
3:0	RW	0x0	SKEW_CAL_CLK_FINE_RISE_SET Skew Calibration Manual Clock Fine Rising Delay Control Register.

DCPHY_M0_DPHY_SD3_DESKEW_CON4
Address: Operational Base + offset (0x0F50)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	SKEW_CAL_FINE_MAX_SET Skew Calibration Maximum Fine Delay Step Control Register.
7:5	RO	0x0	reserved
4:0	RW	0x00	SKEW_CAL_COARSE_MAX_SET Skew Calibration Maximum Coarse Delay Step Control Register.

22.5 Interface Description

Table 22-2 MIPI Combo PHY0 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
MS_VDD0P85	I/O	MIPI_D/C_PHY0_VDD	N/A
MS_VDD18	I/O	MIPI_D/C_PHY0_VDD_1V8	N/A
M_VDD12	I/O	MIPI_D/C_PHY0_VDD_1V2	N/A
M_VREG_0P4V	I/O	MIPI_D/C_PHY0_VREG	N/A
M_DNCLK_B1	I/O	MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	N/A
M_DNDATA0_A0	I/O	MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	N/A
M_DNDATA1_C0	I/O	MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	N/A
M_DNDATA2_A2	I/O	MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	N/A
M_DNDATA3_C2	I/O	MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	N/A
M_DPCLK_C1	I/O	MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	N/A
M_DPDATA0_B0	I/O	MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	N/A
M_DPDATA1_A1	I/O	MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	N/A
M_DPDATA2_B2	I/O	MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	N/A
M_DPDATA3	I/O	MIPI_DPHY0_TX_D3P/NO_USE	N/A
S_DNCLK_B1	I/O	MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	N/A
S_DNDATA0_A0	I/O	MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	N/A
S_DNDATA1_C0	I/O	MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	N/A
S_DNDATA2_A2	I/O	MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	N/A
S_DNDATA3_C2	I/O	MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	N/A
S_DPCLK_C1	I/O	MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	N/A
S_DPDATA0_B0	I/O	MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	N/A
S_DPDATA1_A1	I/O	MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	N/A
S_DPDATA2_B2	I/O	MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	N/A
S_DPDATA3	I/O	MIPI_DPHY0_RX_D3P/NO_USE	N/A

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 22-3 MIPI Combo PHY1 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
MS_VDD0P85	I/O	MIPI_D/C_PHY1_VDD	N/A
MS_VDD18	I/O	MIPI_D/C_PHY1_VDD_1V8	N/A
M_VDD12	I/O	MIPI_D/C_PHY1_VDD_1V2	N/A
M_VREG_0P4V	I/O	MIPI_D/C_PHY1_VREG	N/A
M_DNCLK_B1	I/O	MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	N/A
M_DNDATA0_A0	I/O	MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	N/A
M_DNDATA1_C0	I/O	MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	N/A
M_DNDATA2_A2	I/O	MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	N/A
M_DNDATA3_C2	I/O	MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	N/A
M_DPCLK_C1	I/O	MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	N/A
M_DPDATA0_B0	I/O	MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	N/A
M_DPDATA1_A1	I/O	MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	N/A
M_DPDATA2_B2	I/O	MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	N/A
M_DPDATA3	I/O	MIPI_DPHY1_TX_D3P/NO_USE	N/A
S_DNCLK_B1	I/O	MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	N/A
S_DNDATA0_A0	I/O	MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	N/A
S_DNDATA1_C0	I/O	MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	N/A
S_DNDATA2_A2	I/O	MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	N/A
S_DNDATA3_C2	I/O	MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	N/A
S_DPCLK_C1	I/O	MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	N/A

Module Pin	Dir	Pad Name	IOMUX Setting
S_DPDATA0_B0	I/O	MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	N/A
S_DPDATA1_A1	I/O	MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	N/A
S_DPDATA2_B2	I/O	MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	N/A
S_DPDATA3	I/O	MIPI_DPHY1_RX_D3P/NO_USE	N/A

Notes: I=input, O=output, I/O=input/output, bidirectional

22.6 Application Notes

22.6.1 System-level Interaction

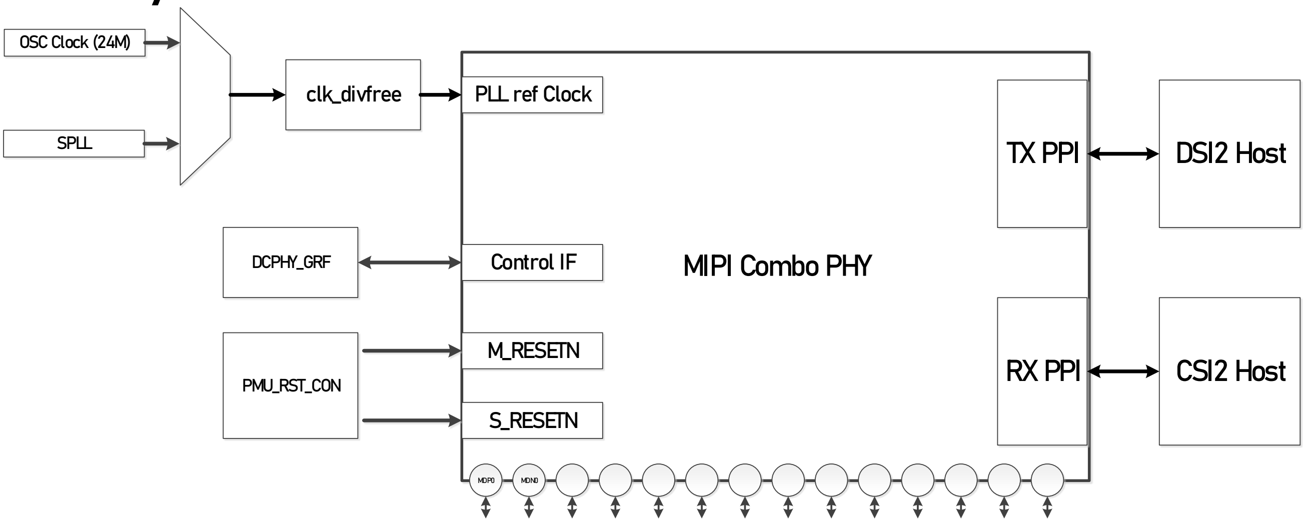

Fig. 22-7 DCPHY System Level Interaction

22.6.1.1 Clock

- **pll_ref_clk**: MIPI Combo PHY PLL reference clock could be configured to choose the source from external oscillator 24Mhz clock or system PLL clock. The default setting is oscillator 24Mhz clock for clock quality consideration.

22.6.1.2 Reset

- **M_RESETN**: reset to PLL block, TX Clock lane block and data lane 0/1/2/3 block.
- **S_RESETN**: reset to RX Clock lane block and data lane 0/1/2/3 block.

M_RESETN and S_RESETN are programmed in *PMU1CRU_SOFTRST_CON04 register.*

22.6.1.3 AMBA APB 3 Interface

MIPI D-PHY/C-PHY combo PHY has internal registers to control the PHY itself and to debug. These internal registers are accessible through the APB interface, and each register is a maximum of 16bits wide. The APB slave in the PHY is completely compatible with AMBA 3.0 APB specification.

Table 22-4 DCPHY APB Base Address

IP	Base Address
MIPI_Combo_PHY_0	0xFEDA0000
MIPI_Combo_PHY_1	0xFEDB0000

22.6.1.4 System Control Signals

MIPI Combo PHY mode and some debug status are interacted with their corresponding GRF.

Table 22-5 DCPHY GRF Base Address

IP	Base Address
MIPI_Combo_PHY_GRF0	0xFD5E8000
MIPI_Combo_PHY_GRF1	0xFD5EC000

M/S_CPHY_MODE: D-PHY / C-PHY mode select signal of bias / DTB / PLL / TX / RX block.

22.6.2 PLL Programmability

PLL in MIPI Combo PHY is a 1.8V/0.75V dual supply-voltage phase locked loop (PLL) with a wide-output-frequency-range for frequency synthesis. It consists of a phase frequency detector (PFD), a charge pump, a voltage-controlled oscillator (VCO), a 6-bit predivider, a 10-bit main-divider, a 3-bit scaler, a delta-sigma modulator (DSM) and an automatic

frequency control (AFC).
The output frequency (Fout) is related to the input frequency (Fin) using the following equation.

$$Fvco = \frac{((M + \frac{K}{65536}) \times 2 \times Fin)}{P}$$

$$Fout = \frac{((M + \frac{K}{65536}) \times 2 \times Fin)}{(P \times 2^{s})}$$

where p, m, s, and k are the division values in decimal numbers for pre-divider, main-divider, scaler, and DSM, respectively.
Frequency of VCO's output: 2600MHz ≤ F_{vco} ≤ 6600MHz
P[5:0], M[9:0] and S[2:0] are unsigned integers. K[15:0] is a two's complement integer.

- 6'b000001 ≤ P[5:0] ≤ 6'b11 1111 and 6MHz ≤ FFREF(FFIN / p) ≤ 30MHz
- 10'b00_0100_0000 ≤ M[9:0] ≤ 10'b11_1111_1111
- 3'b000 ≤ S[2:0] ≤ 3'b110
- 16'b1000_0000_0000_0000 ≤ K[15:0] ≤ 16'b0111_1111_1111_1111

22.6.3 Start-up Sequence

The below figure illustrates the initialization sequence.

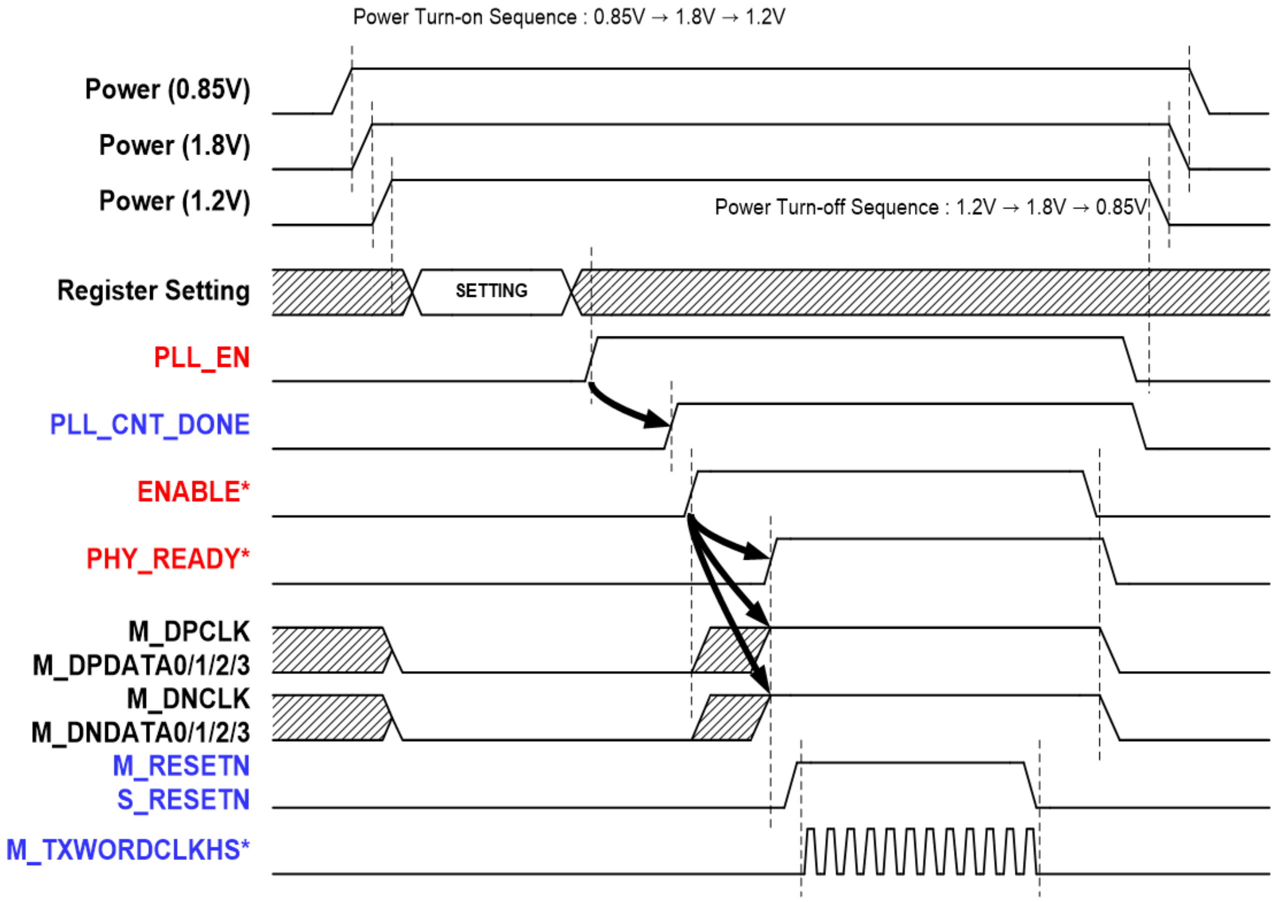

Fig. 22-8 DCPHY Start Up Sequence

(1) Turn the powers on by the sequence according to the initialization sequence figure. After power sequence is done, drivers in PHY are stabilized and DP/DN pad outputs of each Lane become LP-00 state.
(2) Set the special function registers through APB interface including the registers of PLL. DO NOT set PLL_EN and ENABLE register in this time.
    - PLL_EN: PLL_CON0[12]
    - ENABLE: DPHY_M0C_GNR_CON0[0] / DPHY_M0D#_GNR_CON0[0] / COMBO_M0D#_GNR_CON[0] / DPHY_S0C_GNR_CON0[0] /

DPHY_S0D#_GNR_CON0[0] / COMBO_S0D#_GNR_CON[0]
(3) Enable PLL by set PLL_EN register to HIGH. If Slave Lanes are only used, then PLL sequence can be skipped at the real set.
(4) When PLL_EN is set to HIGH, PLL lock counter is started for getting stabilized clock. The lock counter is expired when the count value is reached to the value set as REG_PLL_LOCK_CNT (PLL_CON7[15:0]). And then, the interface signal PLL_CNT_DONE is asserted.
(5) Through ENABLE registers, the Lanes are enabled (# = 0/1/2/3).
- ENABLE: DPHY_M0C_GNR_CON0[0] / DPHY_M0D#_GNR_CON0[0] / COMBO_M0D#_GNR_CON[0] / DPHY_S0C_GNR_CON0[0] / DPHY_S0D#_GNR_CON0[0] / COMBO_S0D#_GNR_CON[0]

(6) When ENABLE is set to HIGH, the circuits need 200us for initializing Low-Power regulator and stabilizing bias block. For this, there are PHY ready counter in each Lanes. The counter is expired when the count value is reached to the value set as T_PHY_READY (GNR_CON1[15:0]). And then, PHY_READY (GNR_CON0[1]) register is set to HIGH.
- T_PHY_READY : DPHY_M0C_GNR_CON1[15:0] / DPHY_M0D#_GNR_CON1[15:0] / COMBO_M0D#_GNR_CON1[15:0] / DPHY_S0C_GNR_CON1[15:0] / DPHY_S0D#_GNR_CON1[15:0] / COMBO_S0D#_GNR_CON1[15:0]
- PHY_READY: DPHY_M0C_GNR_CON0[1] / DPHY_M0D#_GNR_CON0[1] / COMBO_M0D#_GNR_CON0[1] / DPHY_S0C_GNR_CON0[1] / DPHY_S0D#_GNR_CON0[1] / COMBO_S0D#_GNR_CON0[1]

(7) After PHY_READY is set to HIGH, the pad outputs DP/DN are stabilized to LP-11 state.
(8) After all of PHY_READY of each Lane, user can release reset of PHY "M_RESETN" or "S_RESETN".
(9) M_TXWORDCLKHS* are toggled after releasing the reset.

22.6.4 Configuration examples

22.6.4.1 Case 1 (TX operate at 4.5Gbps DPHY Mode, Ref_Clk = 24Mhz)

Configuration Sequence:

① set PMU1CRU_SOFTRST_CON04[3] = 1 to assert M_RESETN
② set BIAS block
- BIAS_CON0 = 0x0010
- BIAS_CON1 = 0x0110
- BIAS_CON2 = 0x3223

③ set TX PLL
- PLL_CON0 = 0x0002 (P = 2, S = 0)
- PLL_CON1 = 0x7fff (K = 32767)
- PLL_CON2 = 0x00bb (M = 187)
- PLL_CON3 = 0x3f08
- PLL_CON4 = 0x0800
- PLL_CON5 = 0x0500
- PLL_CON7 = 0xF000
- PLL_CON8 = 0xF000

④ set TX clock lane
1) set MC_GNR_CON0 = 0xf000
2) set MC_ANA_CON0 = 0x7133
3) set MC_ANA_CON1 = 0x0001
4) set timing parameters through
MC_TIME_CON0/MC_TIME_CON1/MC_TIME_CON2/MC_TIME_CON3 refer to the Supplement Guide Timing Table.
5) set DPHY_MC_DESKEW_CON0 = 0x9cb1 to enable deskew calibration function.

⑤ set TX data lane (* = 0,1,2,3)
1) set COMBO_MD*_GNR_CON1 = 0x2000
2) set COMBO_MD*_ANA_CON0 = 0x7133
3) set COMBO_MD*_ANA_CON0 = 0x0001
4) set timing parameters through
COMBO_MD*_TIME_CON0/COMBO_MD*_TIME_CON1/COMBO_MD*_TIME_CON2

/COMBO_MD*_TIME_CON3/COMBO_MD*_TIME_CON4 refer to the Supplement Guide Timing Table.

⑥ set PLL_EN = 1(PLL_CON0[0])

⑦ wait PLL is locked (read the PLL_STAT0[0])

⑧ set DPHY_MC_GNR_CON0[0]/COMBO_MD0_GNR_CON0[0]/COMBO_MD1_GNR_CON0[0]/COMBO_MD2_GNR_CON0[0]/COMBO_MD3_GNR_CON0[0] = 0x1 to enable lanes.

⑨ wait clock lane and data lanes' PHY_READY (GNR_CON0[1]) register is set to HIGH

⑩ set PMU1CRU_SOFTRST_CON04[3] = 0 to deassert M_RESETN

22.6.4.2 Case 2 (TX operate at 2Gbps CPHY Mode, Ref_Clk = 24Mhz)

Configuration Sequence:

① set MIPI_Combo_PHY_GRF_CON0 = 0x9 (M_CPHY_MODE = 1)

② set PMU1CRU_SOFTRST_CON04[3] = 1 to assert M_RESETN

③ set BIAS block
- BIAS_CON0 = 0x0010
- BIAS_CON1 = 0x0110
- BIAS_CON2 = 0x3223
- BIAS_CON4.I_MUX_SEL = 0x2
- DPHY_MC_ANA_CON2.HS_VREG_AMP_ICON = 0x2

④ set TX PLL
- PLL_CON0 = 0x0003 (P = 3, S = 0)
- PLL_CON1 = 0x7fff (K = 32767)
- PLL_CON2 = 0x007C (M = 124)
- PLL_CON3 = 0x3f08
- PLL_CON4 = 0x0800
- PLL_CON5 = 0x0500
- PLL_CON7 = 0xF000
- PLL_CON8 = 0xF000

⑤ set TX data lane (* = 0,1,2)
1) set COMBO_MD*_GNR_CON1 = 0x2000
2) set timing parameters through COMBO_MD*_TIME_CON0/COMBO_MD*_TIME_CON1/COMBO_MD*_TIME_CON2/COMBO_MD*_TIME_CON3/COMBO_MD*_TIME_CON4 refer to the Supplement Guide Timing Table.

⑥ set PLL_EN = 1 (PLL_CON0[0])

⑦ wait PLL is locked (read the PLL_STAT0[0])

⑧ set COMBO_MD0_GNR_CON0[0]/COMBO_MD1_GNR_CON0[0]/COMBO_MD2_GNR_CON0[0] = 0x1 to enable lanes.

⑨ wait data lanes' PHY_READY (GNR_CON0[1]) register is set to HIGH

⑩ set PMU1CRU_SOFTRST_CON04[3] = 0 to deassert M_RESETN

22.6.4.3 Case 3 (RX operate at 2.5Gbps DPHY Mode)

Configuration Sequence:

① set PMU1CRU_SOFTRST_CON04[4] = 1 to assert S_RESETN

② set RX clock lane timing parameter
   set DPHY_SC_TIME_CON0 = 0x301.

③ set RX data lane (* = 0,1,2,3) timing parameter (refer to the Supplement Guide Timing Table)
   set COMBO_SD*_TIME_CON0 = 0xd.
   set COMBO_SD*_TIME_CON1 = 0x3.

④ set DPHY_SC_GNR_CON0[0]/COMBO_SD0_GNR_CON0[0]/COMBO_SD1_GNR_CON0[0]/COMBO_SD2_GNR_CON0[0]/COMBO_SD3_GNR_CON0[0] = 0x1 to enable lanes.

⑤ wait clock lane and data lanes' PHY_READY (GNR_CON0[1]) register is set to HIGH

⑥ set PMU1CRU_SOFTRST_CON04[4] = 0 to deassert S_RESETN

22.6.4.4 Case 4 (RX operate at 2.5Gsps CPHY Mode)

Configuration Sequence:

① set MIPI_Combo_PHY_GRF_CON0 = 0x9 (CPHY_MODE = 1)
② set PMU1CRU_SOFTRST_CON04[4] = 1 to assert S_RESETN
③ set RX data lane (* = 0,1,2) timing parameter (refer to the Supplement Guide Timing Table)
set COMBO_SD*_TIME_CON0 = 0x1.
set COMBO_SD*_TIME_CON1 = 0x32.
④ set COMBO_SD0_GNR_CON0[0]/COMBO_SD1_GNR_CON0[0]/COMBO_SD2_GNR_CON0[0] = 0x1 to enable lanes.
⑤ wait data lanes' PHY_READY (GNR_CON0[1]) register is set to HIGH
⑥ set PMU1CRU_SOFTRST_CON04[4] = 0 to deassert S_RESETN

Chapter 23 EDP TX Controller

23.1 Overview

This eDP TX is compliant with DisplayPort standard 1.2a and standard eDP 1.3. DisplayPort is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and consumer electronics (CE) industries. It consolidates the internal and external connection methods to reduce device complexity and cost, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

EDP TX Controller supports the following features:

- Compliant with DisplayPort™ Specification, Version 1.2
- Compliant with eDP™ Specification, Version 1.3
- Main link containing 4 physical lanes of 5.4/2.7/1.62 Gbps/lane
- Bi-directional auxiliary link with up to 1Mbps speed
- Support RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10 bit per component video format
- Support HDCP v1.3, integrated HDCP encryption engine for transmitting protected audio and video content
- Support PSR
- Support I2S audio interface, the maximum number of channels is 8
- Support S/PDIF audio interface
- 24 MHz crystal clock
- PRBS or programmable transmitter pattern for main link quality test
- Hot plug and unplug detection and link status monitor
- Supports reading of the display EDID

23.2 Block Diagram

EDP TX Controller comprises with:

- Video Data Capture
- Audio Data Capture
- DP Transmitter
- APB Slave Interface
- DPTX PHY

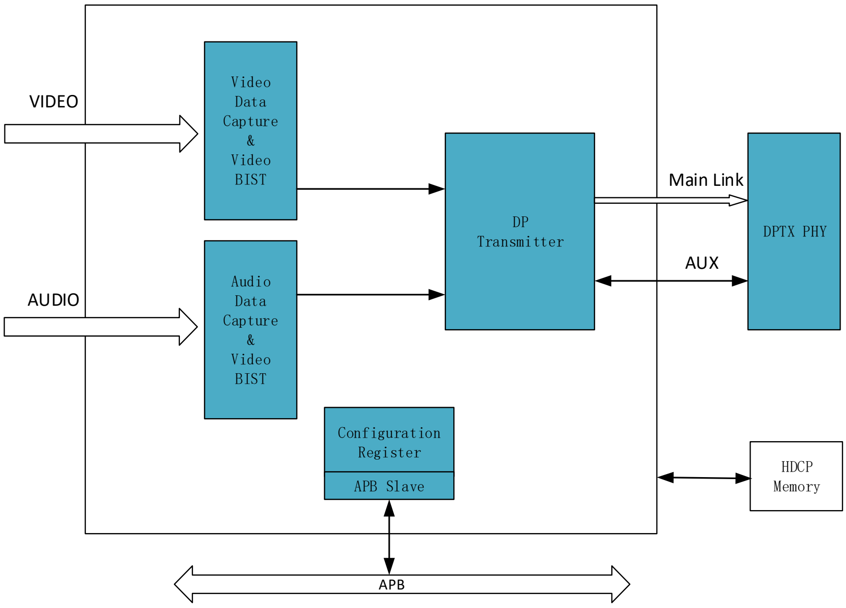

Fig. 23-1 EDP TX Controller Block Diagram

23.3 Function Description

23.3.1 Video Data Capture

The video data comes from VOP. The eDP TX receives signals and stores the video signals into the buffer. Afterward, the DP transmitter reads data from the buffer.

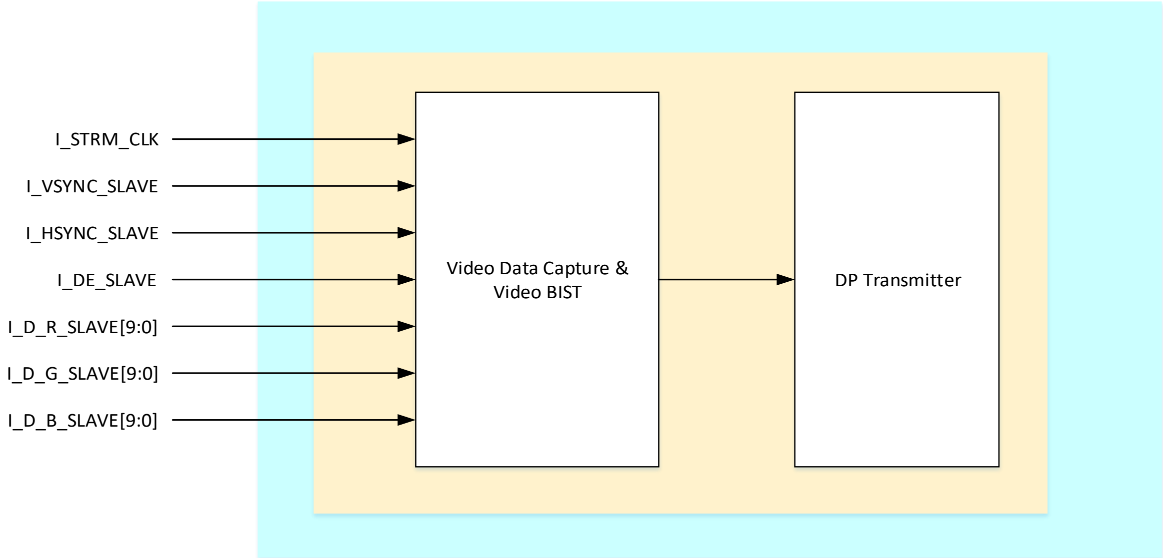

Fig. 23-2 Block diagram of Video Interface

23.3.2 Audio Data Capture

The audio data comes from I2S or S/PDIF. For audio, there are two interface: S/PDIF slave and I2S slave. In S/PDIF slave mode, the audio stream is sent from the S/PDIF input. In I2S slave mode, the audio stream is sent from the I2S S/PDIF input.

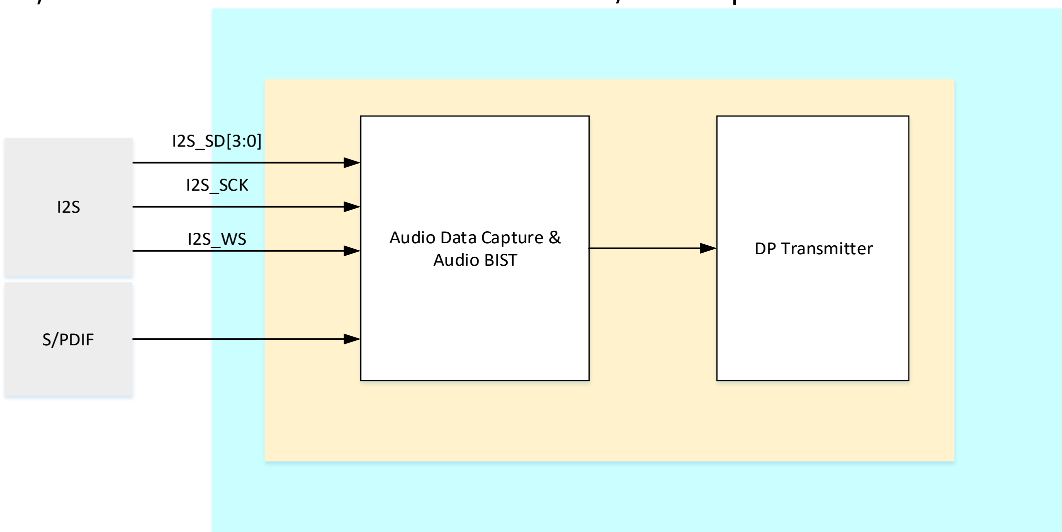

Fig. 23-3 Audio data interface block diagram

23.3.3 DP Transmitter

The DP_TX gets the video data from the Video FIFO module. Then the video data will be packed into TU (Transfer Unit). The Info Frame is passed directly through the APB interface. Some main link attributes data come from APB interface, but the information of input video timing of main link attribute come from Video Capture module.

23.3.4 APB Slave Interface

The APB slave interface is used at the configuration registers interface. Configure eDP TX and get its status. HDCP key memory is whiten by the APB slave interface, too.

23.3.5 DPTX PHY

The eDP TX PHY is combo transmit eDP and HDMI. In eDP mode, it can support 4 physical lanes of 5.4/2.7/1.62 Gbps/lane and bi-directional auxiliary link with up to 1Mbps speed.

23.4 Register Description

23.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
EDPTX_DP_TX_VERSION	0x0010	W	0x00000060	DPTX Version
EDPTX_FUNC_EN_1	0x0018	W	0x0000007D	Function Enable Register 1
EDPTX_FUNC_EN_2	0x001C	W	0x00000087	Function Enable Register 2
EDPTX_VIDEO_CTL_1	0x0020	W	0x00000000	Video Control Register 1
EDPTX_VIDEO_CTL_2	0x0024	W	0x00000010	Video Control Register 2
EDPTX_VIDEO_CTL_3	0x0028	W	0x00000000	Video Control Register 3
EDPTX_VIDEO_CTL_4	0x002C	W	0x00000000	Video Control Register 4
EDPTX_VIDEO_CTL_8	0x003C	W	0x00000020	Video Control Register 8
EDPTX_VIDEO_CTL_10	0x0044	W	0x00000000	Video Control Register 10
EDPTX_TOTAL_LINE_CFG_L	0x0048	W	0x00000000	Total Line Byte Configure Register
EDPTX_TOTAL_LINE_CFG_H	0x004C	W	0x00000000	Total Line High Byte Configure Register
EDPTX_ACTIVE_LINE_CFG_L	0x0050	W	0x00000000	Active Line Low Byte Configure Register
EDPTX_ACTIVE_LINE_CFG_H	0x0054	W	0x00000000	Active Line High Byte Configure Register
EDPTX_V_F_PORCH_CFG	0x0058	W	0x00000000	Vertical Front Porch Configure Register
EDPTX_V_SYNC_WIDTH_CFG	0x005C	W	0x00000000	Vertical Sync Width Configure Register
EDPTX_V_B_PORCH_CFG	0x0060	W	0x00000000	Vertical Back Porch Configure Register
EDPTX_TOTAL_PIXEL_CFG_L	0x0064	W	0x00000000	Total Pixel Low Byte Configure Register
EDPTX_TOTAL_PIXEL_CFG_H	0x0068	W	0x00000000	Total Pixel High Byte Configure Register
EDPTX_ACTIVE_PIXEL_CFG_L	0x006C	W	0x00000000	Active Pixel Low Byte Configure Register
EDPTX_ACTIVE_PIXEL_CFG_H	0x0070	W	0x00000000	Active Pixel High Byte Configure Register
EDPTX_H_F_PORCH_CFG_L	0x0074	W	0x00000000	Horizon Front Porch Low Byte Configure Register
EDPTX_H_F_PORCH_CFG_H	0x0078	W	0x00000000	Horizon Front Porch High Byte Configure Register
EDPTX_H_SYNC_CFG_L	0x007C	W	0x00000000	Horizon Sync Width Low Byte Configure Register
EDPTX_H_SYNC_CFG_H	0x0080	W	0x00000000	Horizon Sync Width High Byte Configure Register
EDPTX_H_B_PORCH_CFG_L	0x0084	W	0x00000000	Horizon Back Porch Low Byte Configure Register
EDPTX_H_B_PORCH_CFG_H	0x0088	W	0x00000000	Horizon Back Porch High Byte Configure Register
EDPTX_VIDEO_STATUS	0x008C	W	0x00000000	Input Video Status Register
EDPTX_TOTAL_LINE_STA_L	0x0090	W	0x00000000	Total Line Status Low Byte Register
EDPTX_TOTAL_LINE_STA_H	0x0094	W	0x00000000	Total Line Status High Byte Register
EDPTX_ACTIVE_LINE_STA_L	0x0098	W	0x00000000	Active Line Status Low Byte Register
EDPTX_ACTIVE_LINE_STA_H	0x009C	W	0x00000000	Active Line Status High Byte Register

Name	Offset	Size	Reset Value	Description
EDPTX_V_F_PORCH_STA	0x00A0	W	0x00000001	Vertical Front Porch Status Register
EDPTX_V_SYNC_STA	0x00A4	W	0x00000000	Vertical Sync Width Status Register
EDPTX_V_B_PORCH_STA	0x00A8	W	0x00000000	Vertical Back Porch Status Register
EDPTX_TOTAL_PIXEL_STA_L	0x00AC	W	0x00000000	Total Pixel Status Low Byte Register
EDPTX_TOTAL_PIXEL_STA_H	0x00B0	W	0x00000000	Total Pixel Status High Byte Register
EDPTX_ACTIVE_PIXEL_STA_L	0x00B4	W	0x00000000	Active Pixel Status Low Byte Register
EDPTX_ACTIVE_PIXEL_STA_H	0x00B8	W	0x00000000	Active Pixel Status High Byte Register
EDPTX_H_F_PORCH_STA_L	0x00BC	W	0x00000000	Horizon Front Porch Status Low Byte Register
EDPTX_H_F_PORCH_STA_H	0x00C0	W	0x00000000	Horizon Front Porch Status High Byte Register
EDPTX_H_SYNC_STA_L	0x00C4	W	0x00000000	Horizon Sync Width Status Low Byte Register
EDPTX_H_SYNC_STA_H	0x00C8	W	0x00000000	Horizon Sync Width Status High Byte Register
EDPTX_H_B_PORCH_STA_L	0x00CC	W	0x00000000	Horizon Back Porch Status Low Byte Register
EDPTX_H_B_PORCH_STA_H	0x00D0	W	0x00000000	Horizon Back Porch Status High Byte Register
EDPTX_SPDIF_AUDIO_CTL_0	0x00D8	W	0x00000000	SPDIF Audio Control Register 0
EDPTX_DP_AUDIO_CTL_1	0x00DC	W	0x00000000	DP Audio Control Register 1
EDPTX_SPDIF_AUDIO_STA_0	0x00E0	W	0x00000000	SPDIF Audio Status Register 0
EDPTX_SPDIF_AUDIO_STA_1	0x00E4	W	0x00000000	Audio SPDIF Status Register 1
EDPTX_SPDIF_ERR_THRD	0x00E8	W	0x00000001	SPDIF Error Threshold Register
EDPTX_SPDIF_ERR_CNT	0x00EC	W	0x00000000	SPDIF Error Counter Register
EDPTX_AUDIO_BIST_CTL	0x00F0	W	0x00000000	Audio BIST Control Register
EDPTX_AUD_FREQ_CNT_1	0x00F4	W	0x00000000	Audio Input Clock Frequency Counter Register 1
EDPTX_AUD_FREQ_CNT_2	0x00F8	W	0x00000000	Audio Input Clock Frequency Counter Register 2
EDPTX_AVI_DB	0x01D0	W	0x00000000	AVI InfoFrame Packet Data Byte, address is Base + 0x01D0 ~ Base + 0x0200, AVI_DB1 ~ AVI_DB13
EDPTX_AUDIO_DB	0x021C	W	0x00000000	Audio InfoFrame Packet Data Byte, address is Base + 0x021C ~ Base + 0x0240, AUDIO_DB1 ~ AUDIO_DB10
EDPTX_IF_TYPE	0x0244	W	0x00000000	InfoFrame Packet Type Code.
EDPTX_IF_PKT_DB	0x0254	W	0x00000000	InfoFrame Packet Data Byte, address is Base + 0x0254 ~ Base + 0x02B4, IF_PKT_DB1 ~ IF_PKT_DB25

Name	Offset	Size	Reset Value	Description
EDPTX_MPEG_DB	0x02D0	W	0x00000000	MPEG Source InfoFrame Packet Data Byte, address is Base + 0x02D0 ~ Base + 0x02F4, MPEG_DB1 ~ MPEG_DB10
EDPTX_REUSE_SPD_HB	0x02F8	W	0x00000000	Reuse SPD HB0 ~ HB3, address is Base + 0x02F8 ~ Base + 0x0304
EDPTX_REUSE_SPD_PB	0x0308	W	0x00000000	Reuse SPD PB0 ~ PB3, address is Base + 0x0308 ~ Base + 0x0314
EDPTX_PSR_FRAME_UPDATA_CTRL	0x0318	W	0x00000000	PSR frame update control
EDPTX_VSC_SHADOW_DB	0x031C	W	0x00000000	VSC shadow data bytes 0 ~ 7, address is Base+ 0x031C ~ Base+ 0x0338, VSC_SHADOW_DB0 ~ VSC_SHADOW_DB7
EDPTX_VSC_SHADOW_PB	0x033C	W	0x00000000	VSC shadow parity bytes 0 ~ 1, address is Base+ 0x033C ~ Base+ 0x0340, VSC_SHADOW_PB0 ~ VSC_SHADOW_PB1
EDPTX_AUDIO_I2S_CH_STA1	0x0344	W	0x00000000	Audio I2S Channel Status Register 1
EDPTX_AUDIO_I2S_CH_STA2	0x0348	W	0x00000000	Audio I2S Channel Status Register 2
EDPTX_AUDIO_I2S_CH_STA3	0x034C	W	0x00000000	Audio I2S Channel Status Register 3
EDPTX_AUDIO_I2S_CH_STA4	0x0350	W	0x00000000	I2S Channel Status Register 4
EDPTX_AUDIO_I2S_CH_STA5	0x0354	W	0x00000000	Audio Channel Status Register 5
EDPTX_LANE_MAP	0x035C	W	0x00000055	Lane Map Register
EDPTX_INT_STATE	0x03C0	W	0x00000000	Interrupt Status Register
EDPTX_COMMON_INT_STA_1	0x03C4	W	0x00000000	Common Interrupt Status Register 1
EDPTX_COMMON_INT_STA_2	0x03C8	W	0x00000000	Common Interrupt Status Register 2
EDPTX_COMMON_INT_STA_3	0x03CC	W	0x00000000	Common Interrupt Status Register 3
EDPTX_COMMON_INT_STA_4	0x03D0	W	0x00000000	Common Interrupt Status Register 4
EDPTX_SPDIF_BIPHASE_INT_STA	0x03D4	W	0x00000000	SPDIF Biphase Interrupt Status Register
EDPTX_DP_INT_STA	0x03DC	W	0x00000000	DisplayPort Interrupt Status Register
EDPTX_COMMON_INT_MASK_1	0x03E0	W	0x00000000	Interrupt Mask Register
EDPTX_COMMON_INT_MASK_2	0x03E4	W	0x00000000	Interrupt Mask Register
EDPTX_COMMON_INT_MASK_3	0x03E8	W	0x00000000	Interrupt Mask Register
EDPTX_COMMON_INT_MASK_4	0x03EC	W	0x00000000	Interrupt Mask Register
EDPTX_DP_INT_STA_MASK	0x03F8	W	0x00000000	Interrupt enable Register

Name	Offset	Size	Reset Value	Description
EDPTX_INT_CTL	0x03FC	W	0x00000001	Interrupt Control Register
EDPTX_SYS_CTL_1	0x0600	W	0x00000000	System Control Register 1
EDPTX_SYS_CTL_2	0x0604	W	0x00000000	System Control Register 2
EDPTX_SYS_CTL_3	0x0608	W	0x00000000	System Control Register 3
EDPTX_SYS_CTL_4	0x060C	W	0x00000000	System Control Register 4
EDPTX_DP_VID_CTL	0x0610	W	0x00000000	DP Video Control Register
EDPTX_PKT_SEND_CTL	0x0640	W	0x00000000	Packet Send Control Register.
EDPTX_DP_HDCP_CTL	0x0648	W	0x00000000	DisplayPort HDCP Control Register.
EDPTX_SPDIF_PHASE1_CTL_0	0x0650	W	0x00000000	This register control SPDIF 1 cycle phase counter value [7:0]
EDPTX_SPDIF_PHASE1_CTL_1	0x0654	W	0x00000000	This register enables force of the 1 cycle phase counter value [8]
EDPTX_SPDIF_PHASE2_CTL_0	0x0658	W	0x00000000	This register control SPDIF 2 cycle phase counter value [7:0]
EDPTX_SPDIF_PHASE2_CTL_1	0x065C	W	0x00000000	This register control SPDIF 2 cycle phase counter value [8]
EDPTX_SPDIF_PHASE3_CTL_0	0x0660	W	0x00000000	This register control SPDIF 3 cycle phase counter value [7:0]
EDPTX_SPDIF_PHASE3_CTL_1	0x0664	W	0x00000000	This register control SPDIF 3 cycle phase counter value [8]
EDPTX_LINK_BW_SET	0x0680	W	0x0000000A	Main link bandwidth setting
EDPTX_LANE_COUNT_SET	0x0684	W	0x00000000	Main link lane count
EDPTX_DP_TRAINING_PTN_SET	0x0688	W	0x00000000	DP Training Pattern Set Register
EDPTX_DP_LN0_LINK_TRAINING_CTL	0x068C	W	0x00000000	DP Lane 0 Link Training Control Register.
EDPTX_DP_LN1_LINK_TRAINING_CTL	0x0690	W	0x00000000	DP Lane 1 Link Training Control Register.
EDPTX_DP_LN2_LINK_TRAINING_CTL	0x0694	W	0x00000000	DP Lane 2 Link Training Control Register.
EDPTX_DP_LN3_LINK_TRAINING_CTL	0x0698	W	0x00000000	DP Lane 3 Link Training Control Register.
EDPTX_DP_HW_LINK_TRAINING_CTL	0x06A0	W	0x00000000	DP hardware training control registers.
EDPTX_HPD_DEGLITCH_L	0x06C4	W	0x0000005E	HPD_DEGLITCH is used to de-glitch the HPD signal.
EDPTX_HPD_DEGLITCH_H	0x06C8	W	0x0000001A	HPD_DEGLITCH is used to de-glitch the HPD signal.
EDPTX_POLLING_PERIOD	0x06CC	W	0x0000000E	POLLING_PERIOD
EDPTX_DP_LINK_DEBUG_CTL	0x06E0	W	0x00000000	DP Link Debug Control Register
EDPTX_DP_SINK_COUNT	0x06E4	W	0x00000000	SINK_COUNT
EDPTX_DP_IRD_VECTOR	0x06E8	W	0x00000000	IRQ_VECTOR
EDPTX_DP_LINK_STATUS0	0x06EC	W	0x00000000	DP_LINK_STATUS0
EDPTX_DP_LINK_STATUS1	0x06F0	W	0x00000000	DP_LINK_STATUS1
EDPTX_DP_ALIGN_STATUS	0x06F4	W	0x00000000	ALIGN_STATUS
EDPTX_M_VID_0	0x0700	W	0x00000000	M_VID[7:0]
EDPTX_M_VID_1	0x0704	W	0x00000000	M_VID[15:8]
EDPTX_M_VID_2	0x0708	W	0x00000000	M_VID[23:16]

Name	Offset	Size	Reset Value	Description
EDPTX_N_VID_0	0x070C	W	0x00000000	N_VID[7:0]
EDPTX_N_VID_1	0x0710	W	0x00000000	N_VID[15:8]
EDPTX_N_VID_2	0x0714	W	0x00000000	N_VID[23:16]
EDPTX_M_VID_MON	0x0718	W	0x00000000	M_VID value monitoring register
EDPTX_DP_VIDEO_FIFO_THRD	0x0730	W	0x00000000	DP Video Data FIFO Threshold Register
EDPTX_DP_GNS_CTRL	0x0734	W	0x00000000	DP GNS CONTROL REGISTER
EDPTX_DP_AUDIO_MARGIN	0x073C	W	0x00000000	DP Audio Margin Register
EDPTX_M_AUD_MON	0x0740	W	0x00000000	M_AUD value monitoring register
EDPTX_M_AUD_0	0x0748	W	0x00000000	M_AUD[7:0]
EDPTX_M_AUD_1	0x074C	W	0x00000000	M_AUD[15:8]
EDPTX_M_AUD_2	0x0750	W	0x00000000	M_AUD[23:16]
EDPTX_N_AUD_0	0x0754	W	0x00000000	N_AUD[7:0]
EDPTX_N_AUD_1	0x0758	W	0x00000000	N_AUD[15:8]
EDPTX_N_AUD_2	0x075C	W	0x00000000	N_AUD[23:16]
EDPTX_DP_M_CAL_CTL	0x0760	W	0x00000000	DP M Value Calculation Control Register
EDPTX_M_VID_GEN_FILTER_TH	0x0764	W	0x00000004	The threshold of M_VID generation filter
EDPTX_M_AUD_GEN_FILTER_TH	0x0778	W	0x00000002	The threshold of M_AUD generation filter
EDPTX_AUX_CH_STA	0x0780	W	0x00000000	AUX Channel Access Status Register
EDPTX_AUX_ERR_NUM	0x0784	W	0x00000000	AUX Channel Access Error Code Register
EDPTX_AUX_CH_DEFER_CTL	0x0788	W	0x0000007F	DP AUX CH DEFER Control Register
EDPTX_AUX_RX_COMM	0x078C	W	0x00000000	AUX CH received command
EDPTX_BUFFER_DATA_CTL	0x0790	W	0x00000000	DP Buffer Data Count Register
EDPTX_AUX_CH_CTL_1	0x0794	W	0x00000000	DP AUX Channel Control Register 1
EDPTX_AUX_ADDR_7_0	0x0798	W	0x00000000	AUX_ADDR[7:0]
EDPTX_AUX_ADDR_15_8	0x079C	W	0x00000000	AUX_ADDR[15:8]
EDPTX_AUX_ADDR_19_16	0x07A0	W	0x00000000	AUX_ADDR[19:16]
EDPTX_AUX_CH_CTL_2	0x07A4	W	0x00000000	DP AUX CH Control Register 2
EDPTX_BUF_DATA	0x07C0	W	0x000000FF	AUX CH buffer data 0 ~ 15, address is Base + 0x07C0 ~ Base+0x07FC
EDPTX_SOC_GENERAL_CTL	0x0800	W	0x00000000	General control register
EDPTX_DP_TEST_80B_PATTERN0	0x081C	W	0x00000000	DP test 80bit pattern0
EDPTX_DP_TEST_80B_PATTERN1	0x0820	W	0x00000000	DP test 80bit pattern1
EDPTX_DP_TEST_80B_PATTERN2	0x0824	W	0x00000000	DP test 80bit pattern2
EDPTX_AUD_CTL	0x0834	W	0x00000000	Audio Control register
EDPTX_CRC_CON	0x0890	W	0x00000000	CRC check control
EDPTX_CRC_RESULT	0x0894	W	0x00000000	CRC result
EDPTX_I2S_CTRL	0x09C8	W	0x00000000	I2S_CTRL

Name	Offset	Size	Reset Value	Description
EDPTX_I2S_CH_SWAP	0x09CC	W	0x0000000B	I2S channel swap
EDPTX_I2S_CH_CTRL	0x09D0	W	0x000000E4	I2S channel control
EDPTX_I2S_CH_CTRL1	0x09D4	W	0x00000000	I2S channel control 1
EDPTX_LINK_POLICY	0x09D8	W	0x00000050	Link_Policy

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.4.3 Detail Register Description

EDPTX_DP_TX_VERSION

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	dp_tx_version DPTX Version

EDPTX_FUNC_EN_1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	vid_cap_func_en_n Video capture functions enable. 1'b0: Normal operation 1'b1: Disable video capture
5	RW	0x1	vid_fifo_func_en_n Video FIFO functions enable. 1'b0: Normal operation 1'b1: Disable video FIFO
4	RW	0x1	aud_fifo_func_en_n Audio FIFO functions enable. 1'b0: Normal operation. 1'b1: Disable audio FIFO.
3	RW	0x1	aud_func_en_n Audio FIFO and capture module function enable. 1'b0: Normal operation 1'b1: Disable audio FIFO and capture module If audio data (DMA or SPDIF) should be transmitted, AUD_FUNC_EN_N and AUD_FIFO_FUNC_EN_N should be set to 0 (enable).
2	RW	0x1	hdcp_func_en_n HDCP module functions enable. 1'b0: Normal operation 1'b1: Disable HDCP logic By disabling and enabling HDCP, all of registers in HDCP are cleared, except for the HDCP key inside of SPSRAM. Therefore, as an easy way to prepare re-authentication, firmware can disable and enable again to clear all HDCP registers.
1	RO	0x0	reserved
0	RW	0x1	sw_func_en_n Software defined function enable. 1'b0: Normal operation 1'b1: Disable all the function modules The bit has the highest priority, if the bit is 1, other function enable bits does not work.

EDPTX_FUNC_EN_2

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ssc_func_en_n SSC module enable. 1'b0: Normal mode 1'b1: Disable SSC module To apply updated SSC parameters into SSC operation, firmware must disable and enable this bit.
6:3	RO	0x0	reserved
2	RW	0x1	aux_func_en_n AUX channel module function enable. 1'b0: Normal operation 1'b1: Disable AUX channel module
1	RW	0x1	serdes_fifo_func_en_n Serdes FIFO function enable. 1'b0: Normal mode 1'b1: Disable Serdes FIFO To reset the serdes fifo, firmware must disable and enable this bit.
0	RW	0x1	ls_clk_domain_func_en_n Link symbol clock domain modules functions enable. 1'b0: Normal mode 1'b1: Disable the modules in link symbol clock domain. To reset the modules in link symbol clock domain, firmware must disable and enable this bit.

EDPTX_VIDEO_CTL_1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	video_en Video data input enable. 1'b0: Disable video data input 1'b1: Enable video data input It takes effect at next video frame.
6	RW	0x0	video_mute Video mute enable. In video mute mode, the solid color, specified in Base + 0x04A8 ~ Base + 0x04B0, is displayed. 1'b0: Disable 1'b1: Enable Output video data is changed properly as soon as this bit is configured.
5:0	RO	0x00	reserved

EDPTX_VIDEO_CTL_2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	in_d_range Dynamic range. This bit field is used to specify video data format in main stream attribute data. 1'b1: CEA range (16 ~ 235) 1'b0: VESA range (0 ~ 255)

Bit	Attr	Reset Value	Description
6:4	RW	0x1	in_bpc Video input bit per color/ component (bpc). This bit field is used to specify video data format in main stream attribute data. Note that 6 bpc mode is invalid in YCbCr 422 mode. 3'b011: 12 bits 3'b010: 10 bits 3'b001: 8 bits 3'b000: 6 bits Other: Reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	in_color_f Colorimetric format of input video. This is used to specify video data format in main stream attribute data. 2'b11: Reserved 2'b10: YCbCr444 2'b01: YcbCr422 2'b00: RGB

EDPTX_VIDEO_CTL_3
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	in_yc_coeffi YCbCr Coefficients of input video. This is used to specify video data format in main stream attribute data. 1'b1: ITU709 1'b0: ITU601
6:5	RO	0x0	reserved
4	RW	0x0	vid_chk_update_type Select video format stability check method in video capture block. 1'b1: Check stability with the difference between adjacent frames. 1'b0: Check stability with the difference of differences between adjacent frames. Compares difference of 1st and 2nd to difference of 3rd and 4th frame.
3:0	RO	0x0	reserved

EDPTX_VIDEO_CTL_4
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	bist_en Video BIST enable. 1'b1: Enable video BIST 1'b0: Normal operation mode
2	RW	0x0	bist_width Control display BIST color bar width. 1'b1: Each bar is 64 pixel width. 1'b0: Each bar is 32 pixel width.
1:0	RW	0x0	bist_type Display BIST type. 2'b00: Color bar 2'b01: White, gray and black bar 2'b10: Mobile white bar 2'b11: Reserved

EDPTX_VIDEO_CTL_8

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x2	vid_hres_th Video Frame Horizontal Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.
3:0	RW	0x0	vid_vres_th Video Frame Vertical Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.

EDPTX_VIDEO_CTL_10

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	f_sel Video format select. 1'b1: Video format information from register 1'b0: Video format information from video_capture module According to the configuration of this bit field, the values of video format status registers in Base + 0x008C~ 0x00D0 are determined, which are transferred as main stream attribute packet. Note that if BIST_EN is set to 1, F_SEL must be cleared to 0 although video format information comes from registers set by user.
3	RO	0x0	reserved
2	RW	0x0	slave_i_scan_cfg Interlace scan mode configuration. 1'b0: Progressive 1'b1: Interlace When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.
1	RW	0x0	slave_vsync_p_cfg Slave mode VSYNC polarity configuration. 1'b1: Low is active. 1'b0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.
0	RW	0x0	slave_hsync_p_cfg Slave mode HSYNC polarity configuration. 1'b1: Low is active. 1'b0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_LINE_CFG_L

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_line_cfg_l TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_LINE_CFG_H

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	total_line_cfg_h TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When Video BIST_EN is enabled, this bit must be configured right to generate right video format.

EDPTX_ACTIVE_LINE_CFG_L

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_line_cfg_l ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_ACTIVE_LINE_CFG_H

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	active_line_cfg_h ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_V_F_PORCH_CFG

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	v_f_porch_cfg This is used to specify the number of lines in vertical front porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_V_SYNC_WIDTH_CFG

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_sync_width_cfg This is used to specify the number of lines in VSYNC period. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_V_B_PORCH_CFG

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_b_porch_cfg This is used to specify the number of lines in frame back porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_PIXEL_CFG_L

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_pixel_cfg_l TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG[7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_TOTAL_PIXEL_CFG_H

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	total_pixel_cfg_h TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_ACTIVE_PIXEL_CFG_L
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_pixel_cfg_l ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_ACTIVE_PIXEL_CFG_H
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	active_pixel_cfg_h ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_F_PORCH_CFG_L
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_f_porch_cfg_l H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG[7:0] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_F_PORCH_CFG_H
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_f_porch_cfg_h H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG [11:8] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_SYNC_CFG_L
Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	h_sync_cfg_l H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_SYNC_CFG_H

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	h_sync_cfg_h H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_B_PORCH_CFG_L

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_b_porch_cfg_l H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_H_B_PORCH_CFG_H

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	h_b_porch_cfg_h H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDPTX_VIDEO_STATUS

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	field_s Interlace scan field status. 1'b1: Second field. 1'b0: First field. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

Bit	Attr	Reset Value	Description
2	RW	0x0	i_scan_s Auto-detect interlace or progressive scan status: 1'b1: Interlace scan. 1'b0: Progressive scan. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.
1	RW	0x0	vsync_p_s Auto-detect VSYNC polarity: 1'b1: Low is active. 1'b0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.
0	RW	0x0	hsync_p_s Auto-detect HSYNC polarity: 1'b1: Low is active. 1'b0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_LINE_STA_L
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_line_sta_l TOTAL_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_LINE_STA_H
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	total_line_sta_h TOTAL_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_LINE_STA_L
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_line_sta_l ACTIVE_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_LINE_STA_H
Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	active_line_sta_h ACTIVE_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_V_F_PORCH_STA
Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	v_f_porch_sta V_F_PORCH (vertical front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_V_SYNC_STA
Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_sync_sta V_SYNC_WIDTH (vertical sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_V_B_PORCH_STA
Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_b_porch_sta V_B_PORCH (vertical back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_PIXEL_STA_L
Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_pixel_sta_l TOTAL_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_TOTAL_PIXEL_STA_H
Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	total_pixel_sta_h TOTAL_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_PIXEL_STA_L
Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_pixel_sta_l ACTIVE_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_ACTIVE_PIXEL_STA_H
Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	active_pixel_sta_h ACTIVE_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_F_PORCH_STA_L
Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_f_porch_sta_l H_F_PORCH [7:0] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_F_PORCH_STA_H
Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_f_porch_sta_h H_F_PORCH [11:8] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_SYNC_STA_L
Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	h_sync_sta_l H_SYNC [7:0] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_SYNC_STA_H
Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_sync_sta_h H_SYNC [11:8] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_B_PORCH_STA_L
Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_b_porch_sta_l H_B_PORCH [7:0] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_H_B_PORCH_STA_H
Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_b_porch_sta_h H_B_PORCH [11:8] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDPTX_SPDIF_AUDIO_CTL_0
Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	aud_spdif_en Set SPDIF audio stream input enable. 1'b0: Disable 1'b1: Enable
6:4	RO	0x0	reserved
3	RW	0x0	reuse_spd_en Reuse spd inforframe registers.

Bit	Attr	Reset Value	Description
2	RW	0x0	force_spdif_det Force SPDIF_STREAM_DET, which is SPDIF detect status, to 1. (Test purpose only) 1'b1: Force SPDIF_STREAM_DET to 1. 1'b0: SPDIF_STREAM_DET is set by hardware detector.
1	RW	0x0	spdif_parity_ctrl Control the SPDIF parity generation scheme. In the IEC-60958, audio packet is 28-bit. But in the DP standard v1.1, the audio packet is 32-bit, 4 more control bits have been added. The control bit selects the parity scheme of original 28 bit defined in IEC-60958 or parity scheme of 32 bit defined in DP standard v1.1. 1'b1: Parity of DP link audio sample 32 bit. 1'b0: Parity of SPDIF audio sample 28 bit.
0	RW	0x0	spdif_clk_det_reset_bypass Bypass SPDIF clock detect auto reset: 1'b1: Bypass SPDIF clock detect auto reset, SPDIF module will not be reset even SPDIF clock is not detected. 1'b0: If SPDIF clock is not detected, SPDIF module is reset automatically.

EDPTX_DP_AUDIO_CTL_1

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	aud_mute_en4 Audio data auto mute control enable for audio FIFO under run interrupt. 1'b1: Enable 1'b0: Disable
4	RW	0x0	aud_mute_en3 Audio data auto mute control enable for audio FIFO overrun interrupt. 1'b1: Enable 1'b0: Disable
3	RW	0x0	aud_mute_en2 Audio data auto mute control enable for HDCP failed interrupt. 1'b1: Enable 1'b0: Disable
2	RW	0x0	aud_mute_en1 Audio data auto mute control enable for SPDIF unstable interrupt. 1'b1: Enable 1'b0: Disable
1	RW	0x0	aud_mute_en0 Audio data auto mute control enable for Audio clock change interrupt. 1'b1: Enable 1'b0: Disable
0	RO	0x0	reserved

EDPTX_SPDIF_AUDIO_STA_0

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	spdif_clk_det SPDIF audio clock detected flag. 1'b1: Clock detected 1'b0: Clock not detected
6:1	RO	0x00	reserved
0	RW	0x0	spdif_stream_det SPDIF audio stream detected flag. 1'b1: Input detected 1'b0: No input detected

EDPTX_SPDIF_AUDIO_STA_1

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	spdif_fs_freq Sampling clock frequency (corresponding to channel status bits [27:24]). 4'b0000: 44.1 KHz 4'b0010: 48 KHz 4'b0011: 32 KHz 4'b1000: 88.2 KHz 4'b1010: 96 KHz 4'b1110: 192 KHz Others: Reserved SPDIF_FS_FREQ can be read when SPDIF_STREAM_DET and VSYNC_DET are high.
3:0	RW	0x0	spdif_word_len Audio word length (corresponding to channel status bits [35:32]). 4'b0010: 16 bits 4'b0011: 20 bits 4'b0100: 18 bits 4'b0101: 22 bits 4'b1000: 19 bits 4'b1001: 23 bits 4'b1010: 20 bits 4'b1011: 24 bits 4'b1100: 17 bits 4'b1101: 21 bits SPDIF_WORD_LEN can be read when SPDIF_STREAM_DET and VSYNC_SET are high.

EDPTX_SPDIF_ERR_THRD

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	spdif_err_thrd SPDIF parity error threshold for the SPDIF_ERR interrupt. When SPDIF stream data parity error occurs, the SPDIF_ERR_CNT will increase by 1. And when SPDIF_ERR_CNT equals to SPDIF_ERR_THRD, SPDIF_ERR interrupt happens.

EDPTX_SPDIF_ERR_CNT

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	spdif_err_cnt SPDIF parity errors counter. Write any value to clear.

EDPTX_AUDIO_BIST_CTL

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sin_ampl Set the Sin wave amplitude for audio BIST data. 4'b0000: 255 4'b0001: 510 4'b0010: 1020 4'b0011: 2040 4'b0100: 4080 4'b0101: 8160 4'b0110: 16320 4'b0111: 32640 4'b1000: 65280 4'b1001: 130560 4'b1010: 261120 4'b1011: 522240 4'b1100: 1044480 4'b1101: 2088960 4'b1110: 4177920 4'b1111: 8355840
3:1	RO	0x0	reserved
0	RW	0x0	aud_bist_en Audio BIST enable. 1'b1: Enable 1'b0: Disable

EDPTX_AUD_FREQ_CNT_1

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aud_freq_cnt_l Audio input clock frequency counter register. For test purpose only.

EDPTX_AUD_FREQ_CNT_2

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aud_freq_cnt_h Audio input clock frequency counter register. For test purpose only.

EDPTX_AVI_DB

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avi_db AVI InfoFrame Packet Data Byte 1 ~ 13

EDPTX_AUDIO_DB

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	audio_db Audio InfoFrame Packet Data Byte 1 ~ 10

EDPTX_IF_TYPE

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	if_type InfoFrame Packet Type Code. It can be set as (0x80 + InfoFrame Type Code) and send any type of infoframe defined in CEA-861C. Commonly, we set it as 0x83(0x80 + 0x03, 0x03 is the type code of SPD InfoFrame) and send SPD infoframe.

EDPTX_IF_PKT_DB

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	if_pkt_db InfoFrame Packet Data Byte 1 ~ 25. The registers define the data in the InfoFrame and the InfoFrame type is defined by IF_TYPE.

EDPTX_MPEG_DB

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	mpeg_db MPEG Source InfoFrame Packet Data Byte 1 ~ 10

EDPTX_REUSE_SPD_HB

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	reuse_spd_hb Reuse SPD HB0 ~ HB3

EDPTX_REUSE_SPD_PB

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	reuse_spd_pb Reuse SPD PB0 ~ PB3

EDPTX_PSR_FRAME_UPDATA_CTRL

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	psr_frame_up_type Select PSR Frame Update type. 1'b1: Burst single frame update 1'b0: Single frame update

Bit	Attr	Reset Value	Description
0	RW	0x0	psr_frame_update Enable PSR Frame Update

EDPTX_VSC_SHADOW_DB

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	vsc_shadow_db VSC shadow data bytes 0 ~ 7

EDPTX_VSC_SHADOW_PB

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	vsc_shadow_pb VSC shadow parity bytes 0 ~ 1

EDPTX_AUDIO_I2S_CH_STA1

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	audio_mode 2'b00: PCM Audio Others: No PCM Audio stream
5:3	RW	0x0	pcm_mode 3'b000: 2 audio channels without pre-emphasis 3'b001: 2 audio channels with 50/15 pre-emphasis
2	RW	0x0	sw_cprgt 1'b0: Software for which copyright is asserted 1'b1: Software for which no copyright is asserted
1	RW	0x0	non_pcm 1'b0: Audio sample word represents linear PCM samples 1'b1: Audio sample word used for other purposes
0	RW	0x0	audio_i2s_ch_sta1 1'b0: Consumer applications 1'b1: Professional applications

EDPTX_AUDIO_I2S_CH_STA2

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	cat_code Category code (corresponding to channel status bits [15:8])

EDPTX_AUDIO_I2S_CH_STA3

Address: Operational Base + offset (0x034C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ch_num Channel number (corresponding to channel status bits [23:20]). Only 2_channel is supported in BIST mode.
3:0	RW	0x0	source_num Source number (corresponding to channel status bits [19:16]). Only 2_channel is supported in BIST mode.

EDPTX_AUDIO_I2S_CH_STA4

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	chnl_bit1 Corresponding to channels status bits [31:30].
5:4	RW	0x0	clk_accur Clock accuracy (corresponding to channels status bits [29:28]). These two bits define the sampling frequency tolerance. The bits are set in the transmitter.
3:0	RW	0x0	fs_freq Sampling clock frequency (corresponding to channel status bits [27:24]). 4'b0000: 44.1 KHz 4'b0010: 48 KHz 4'b0011: 32 KHz 4'b1000: 88.2 KHz 4'b1010: 96 KHz 4'b1110: 192 KHz Others: Reserved When set SPDIF_FS_OVRWR to "1", the four bits sample clock frequency in channel status is replaced by this register setting. Note that the audio sine wave frequency equals to Audio Sample Frequency/128. For example, if the sampling clock frequency is 44.1K, the sine wave frequency is 44,100/128 = 344.6Hz.

EDPTX_AUDIO_I2S_CH_STA5

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	chnl_bit2 Corresponding to channels status bits [39:36].
3:1	RW	0x0	word_length Audio word length (corresponding to channel status bits [35:33]). When WORD_MAX: 0, 3'b001: 16 bits 3'b010: 18 bits 3'b100: 19 bits 3'b101: 20 bits 3'b110: 17 bits When WORD_MAX: 1, 3'b001: 20 bits 3'b010: 22 bits 3'b100: 23 bits 3'b101: 24 bits 3'b110: 21 bits
0	RW	0x0	word_max Audio word length Max (corresponding to channel status bits 32). 1'b0: Maximal word length is 20 bits. 1'b1: Maximal word length is 24 bits.

EDPTX_LANE_MAP

Address: Operational Base + offset (0x035C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x1	lane3_map Control physical lane 3 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
5:4	RW	0x1	lane2_map Control physical lane 2 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
3:2	RW	0x1	lane1_map Control physical lane 1 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
1:0	RW	0x1	lane0_map Control physical lane 0 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0

EDPTX_INT_STATE
Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	int_state Interrupt request status 1'b1: Interrupt service is requested. 1'b0: No interrupt service is requested.

EDPTX_COMMON_INT_STA_1
Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	vsync_det 1'b1: VSYNC active edge has been detected.
6	RW	0x0	pll_lock_chg 1'b1: PLL lock state is changed. Check PLL_LOCK of register DP_DEBUG_CTL for PLL lock status.
5	RW	0x0	spdif_err 1'b1: SPDIF parity errors Write 1 to clear. Software can change this interrupt generation by setting the register SPDIF_ERR_THRD. When SPDIF_ERR, software shall check SPDIF status on register SPDIF_AUDIO_STA_0.
4	RW	0x0	spdif_unstbl 1'b1: Not find expected preamble for SPDIF input.
3	RW	0x0	vid_format_chg 1'b1: Video input format change is detected.
2	RW	0x0	aud_clk_chg 1'b1: Audio input clock change is detected.

Bit	Attr	Reset Value	Description
1	RW	0x0	vid_clk_chg 1'b1: Video input clock change is detected.
0	RW	0x0	sw_int 1'b1: Software-induced interrupt.

EDPTX_COMMON_INT_STA_2

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	enc_en_chg 1'b1: HDCP_ENC_EN changed detected. Write 1 to clear. ENC_EN_CHG happens whenever HDCP_ENC_EN is changed from 1 to 0 or form 0 to 1. This interrupt is generated when the internal HDCP cipher module find out that encryption status is changed. Software can check encryption status on bit ENCRYPT of register HDCP_STA.
5:4	RO	0x0	reserved
3	RW	0x0	hw_bksv_rdy 1'b1: BKSV is ready. Write 1 to clear. It is for H/W HDCP.
2	RW	0x0	hw_sha_done 1'b1: HDCP hardware computing V has ended. Write 1 to clear. During H/W HDCP authentication, it is generated after calculating V.
1	RW	0x0	hw_auth_state_chg 1'b1: H/W HDCP authentication state has changed. HW_AUTH_STATE_CHG happens after H/W HDCP is enabled. Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA. This bit is set only when authentication success or failure status is changed. So, successive authentication failure does not set this bit.
0	RW	0x0	hw_auth_done 1'b1: H/W HDCP authentication has ended. This bit is set when H/W HDCP authentication is finished regardless of success or failure. Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA.

EDPTX_COMMON_INT_STA_3

Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	afifo_under 1'b1: Audio FIFO is under run. Write 1 to clear.
6	RW	0x0	afifo_over 1'b1: Audio FIFO is overrun. Write 1 to clear.

Bit	Attr	Reset Value	Description
5	RW	0x0	r0_chk_flag For hardware authentication (with HDCP repeater): 1'b1: R0 check is finished. For software authentication: 1'b1: R0 is ready for software check. Write 1 to clear. If H/W re-authentication is needed and this bit is set to 1, then this bit must be cleared before H/W re-authentication.
4	RW	0x0	dpcd_specific_irq 1'b1: Sink specific interrupt in DPCD is detected. Write 1 to clear
3	RW	0x0	mydp_plug_in 1'b1: MYDP plug out event is detected. Write 1 to clear
2	RW	0x0	mydp_plug_out 1'b1: MYDP plug out event is detected. Write 1 to clear
1	RW	0x0	mydp_hpd_irq 1'b1: MYDP HPD interrupt is detected. Write 1 to clear
0	RW	0x0	hdcp_link_check_fail 1'b1: HDCP link check failure is detected. Write 1 to clear.

EDPTX_COMMON_INT_STA_4
Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	spdif_bi_phase_err 1'b1: SPDIF bi-phase error has occurred. Write 1 to clear. Software reset will not clear this interrupt.
4:3	RO	0x0	reserved
2	RW	0x0	hotplug_chg 1'b1: Hot plug change detected. Write 1 to clear. HOTPLUG_CHG happens whenever the pin I_DP_HDP changes and the change remains for at least hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H. When HOTPLUG_CHG is high, software shall check the status of HPD signal on register HPD_STATUS.
1	RW	0x0	hpd_lost Hot plug detect signal lost timer larger than 2ms, that means cable is plugged out: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
0	RW	0x0	plug Hot plug detect signal lost time is larger than 2ms before cable plugged, it means cable is plugged in: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.

EDPTX_SPDIF_BIPHASE_INT_STA
Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_biphase_err_clr SPDIF biphase error
6:0	RO	0x00	reserved

EDPTX_DP_INT_STA
Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	int_hpd IRQ (HPD de-asserted less than 2ms) detect interrupt: 1'b1: IRQ interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
5	RW	0x0	hw_training_finish Training FSM module finish link training procedure: 1'b1: Hardware link training finished 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
4	RO	0x0	reserved
3	RW	0x0	sink_lost Sink lost interrupt 1'b1: Sink lost occurred 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
2	RW	0x0	link_lost Link lost interrupt 1'b1: Link lost occurred 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
1	RW	0x0	rply_receiv AUX channel command reply is received: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
0	RW	0x0	aux_err AUX channel access error interrupt: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.

EDPTX_COMMON_INT_MASK_1
Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	common_int_mask_1 Each bit corresponds to the same bit in Common Interrupt Status Register 1. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_COMMON_INT_MASK_2
Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	common_int_mask_2 Each bit corresponds to the same bit in Common Interrupt Status Register 2. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_COMMON_INT_MASK_3

Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	common_int_mask_3 Each bit corresponds to the same bit in Common Interrupt Status Register 3. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_COMMON_INT_MASK_4

Address: Operational Base + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	common_int_mask_4 Each bit corresponds to the same bit in Common Interrupt Status Register 3. 1'b0: Mask interrupt 1'b1: Enable interrupt

EDPTX_DP_INT_STA_MASK

Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	dp_int_sta_mask Each bit corresponds to the same bit in DisplayPort Interrupt Status Register (DP_INT_STA). 1'b1: Enable interrupt 1'b0: Mask interrupt

EDPTX_INT_CTL

Address: Operational Base + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	serdes_overflow_clear 1'b1: Clear SerDes FIFO overflow flag
4	RW	0x0	serdes_underflow_clear 1'b1: Clear SerDes FIFO underflow flag
3	RO	0x0	reserved
2	RW	0x0	soft_int_ctrl Set Software Interrupt: 1'b1: Set interrupt 1'b0: Do not set interrupt
1	RO	0x0	reserved
0	RW	0x1	int_pol INT pin assertion polarity: 1'b1: Assert high 1'b0: Assert low

EDPTX_SYS_CTL_1

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	hbr2_eye_sy_ctrl HBR2 pattern control
2	RW	0x0	det_sta Video stream clock detect status, It will not affect video output. 1'b1: Stream clock detected 1'b0: Stream clock not detected Write any value to update the current status.
1	RW	0x0	force_det Force video stream clock detect, this bit is only active when DET_CTRL is 1 1'b1: Force video stream clock detected 1'b0: Force video stream clock not detected This bit's type is R/W.
0	RW	0x0	det_ctrl Video stream clock detect status control: 1'b1: Use force detect status 1'b0: Use auto-detected status This bit's type is R/W.

EDPTX_SYS_CTL_2

Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	cha_cri Pixel clock change detection threshold. The incoming pixel clock input is counted continuously by the 24MHz reference clock. This register defines a number, if the counter number change is more than this value for 2 pixel clock edges, the CHA_STA bit is asserted. This bit's type is R/W.
3	RO	0x0	reserved
2	RW	0x0	cha_sta Video stream clock change status, It will not affect video output 1'b1: Clock frequency changed. 1'b0: Clock frequency not changed. Write any value to update the current status.
1	RW	0x0	force_cha Force stream clock change status, this bit only active when CHA_CTRL is 1. 1'b1: Force clock change. When asserted, CHA_STA is '1'. 1'b0: Force clock not change. This bit's type is R/W.
0	RW	0x0	cha_ctrl Pixel clock frequency change status control 1'b1: Use force change status 1'b0: Use auto-detected status This bit's type is R/W.

EDPTX_SYS_CTL_3

Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	hpd_status Hot plug detect status. 1'b1: HPD is 1. 1'b0: HPD is 0. This bit's type is RO. When this bit is 0, AUX CH will not work. Note that the HPD_STATUS is only changed after the change of the pin I_DP_HPD remains for no less than hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H.
5	RW	0x0	f_hpd Force hot plug detect. 1'b1: Force HPD 1. 1'b0: Force HPD 0. This bit's type is R/W.
4	RW	0x0	hpd_ctrl Hot plug detect manual control. 1'b1: Force HPD with F_HPD. 1'b0: Use PIN_HPD state. This bit's type is R/W.
3	RO	0x0	hdcp_rdy HDCP ready status. 1'b1: HDCP is ready. 1'b0: HDCP is not ready. This bit's type is RO. This bit is an indicator of whether HDCP is ready to perform. Usually, it is set as soon as HPD signal is detected as plugged.
2	RW	0x0	strm_valid Input stream have constant video format, and this stream is valid to send out through link. 1'b1: Input stream is valid. 1'b0: Input stream is not valid. Write any value to update the current status. Hardware will not send out video through link when this bit is 0.
1	RW	0x0	f_valid Force stream valid, this bit only active when VALID_CTRL is 1. 1'b1: Force input video stream valid. 1'b0: Force input video stream not valid. This bit's type is R/W.
0	RW	0x0	valid_ctrl Stream valid control. 1'b1: Use F_VALID bit to control video stream valid status 1'b0: Use video stream valid auto-detect This bit's type is R/W.

EDPTX_SYS_CTL_4

Address: Operational Base + offset (0x060C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	fix_m_aud Fix M_AUD value 1'b1: Use register M_AUD value to be sent out. 1'b0: Use calculates M_AUD value to be sent out.

Bit	Attr	Reset Value	Description
3	RW	0x0	enhanced DisplayPort Enhanced mode enable 1'b1: Enhanced mode 1'b0: Normal mode
2	RW	0x0	fix_m_vid Fix M_VID value 1'b1: Use register M_VID value to be sent out. 1'b0: Use calculates M_VID value to be sent out.
1:0	RW	0x0	m_vid_update_ctrl Control M_VID update frequency 2'b11: 1/8 X update rate 2'b10: 1/4 X update rate 2'b01: 1/2 X update rate 2'b00: Normal rate

EDPTX_DP_VID_CTL

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	bpc Bit per color/ component with video which transferred via DP main link 3'b011: 12 bits 3'b010: 10 bits 3'b001: 8 bits 3'b000: 6 bits Other: Reserved
4	RW	0x0	yc_coeff YCbCr Coefficients with video which transferred via DP main link 1'b1: ITU709 1'b0: ITU601
3	RW	0x0	d_range Dynamic range 1'b1: CEA range 1'b0: VESA range (from 0 to the maximum)
2:1	RW	0x0	color_f Colorimetric format with video which transferred via DP main link 2'b11: Reserved 2'b10: YcbCr444 2'b01: YcbCr422 2'b00: RGB
0	RO	0x0	reserved

EDPTX_PKT_SEND_CTL

Address: Operational Base + offset (0x0640)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	audio_info_up Audio InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after Audio Packet Content Registers have been configured as Audio InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.

Bit	Attr	Reset Value	Description
6	RW	0x0	avi_info_up AVI InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after AVI Packet Content Registers have been configured as AVI InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
5	RW	0x0	mpeg_info_up MPEG InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after MPEG Packet Content Registers have been configured as MPEG InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
4	RW	0x0	if_up Configurable InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after IF_TYPE and IF_PKT_DB1~25 Registers have been configured as configurable InfoFrame content have been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
3	RW	0x0	audio_info_en Audio InfoFrame send enable. 1'b1: Send Audio InfoFrame 1'b0: Don't send Audio InfoFrame Make sure that the Audio Packet Content Registers had been configured correctly and the AUDIO_INFO_UP had been written with 1. This bit's type is R/W.
2	RW	0x0	avi_info_en AVI InfoFrame send enable. 1'b1: Send AVI InfoFrame 1'b0: Don't send AVI InfoFrame Make sure that the AVI Packet Content Registers had been configured correctly and the AVI_INFO_UP had been written with 1. This bit's type is R/W.
1	RW	0x0	mpeg_info_en MPEG InfoFrame send enable. 1'b1: Send MPEG InfoFrame 1'b0: Don't send MPEG InfoFrame Make sure that the MPEG Packet Content Registers had been configured correctly and the MPEG_INFO_UP had been written with 1. This bit's type is R/W.
0	RW	0x0	pkt_send_ctl Configurable InfoFrame send enable. 1'b1: Send InfoFrame defined in IF_TYPE and IF_PKT_DB1~25. 1'b0: Don't send InfoFrame. Make sure that the IF_TYPE and IF_PKT_DB1~25 Registers had been configured correctly and the IF_UP had been written with 1. This bit's type is R/W.

EDPTX_DP_HDCP_CTL

Address: Operational Base + offset (0x0648)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	hdcp_hpd_rst HDCP block reset control. 1'b0: No reset for HDCP block when HPD is low. 1'b1: Reset HDCP when HPD is low.
5:2	RO	0x0	reserved
1	RW	0x0	link_check_mode HDCP link integrity check mode: 1'b1: HDCP polling link integrity check status, and re-start HDCP Authentication automatically when detected link integrity check fail. 1'b0: HDCP don't polling link integrity check status.
0	RW	0x0	hw_hdcp_int The DP receiver initiates a HDCP interrupt through Hot Plug Detect Pin to DP transmitter whenever DP receiver finds R0' calculation done, downstream KSV list is ready and V' calculation done, or HDCP link integrity check failure. A firmware on DP transmitter must set this bit to 1 in order to make H/W HDCP authentication module do some proper action when firmware of DP transmitter find it out that the interrupt about HDCP. This bit is self cleared.

EDPTX_SPDIF_PHASE1_CTL_0

Address: Operational Base + offset (0x0650)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	spdif_phase1_ctl_0 This register control SPDIF 1 cycle phase counter value [7:0], if bit SPDIF_PHASE1_CTL_EN is 0, the 1 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE1_CTL should be set as Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 135,000,000/ (32*44,100*2*2) = 23.9. SPDIF_PHASE1_CTL should set to 24.

EDPTX_SPDIF_PHASE1_CTL_1

Address: Operational Base + offset (0x0654)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase1_ctl_en This register enables force of the 1 cycle phase counter value function. 1'b0: SPDIF 1 cycle phase counter value use chip counted value. 1'b1: SPDIF 1 cycle phase counter value use the data written to register SPDIF_PHASE1_CTL_0 and SPDIF_PHASE1_CTL_1.
6:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	spdif_phase1_ctl_1 This register control SPDIF 1 cycle phase counter value [8], if bit PHASE_1_CONTROL_EN is 0, the 1 cycle phase counter value [8] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register.

EDPTX_SPDIF_PHASE2_CTL_0

Address: Operational Base + offset (0x0658)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	spdif_phase2_ctl_0 This register control SPDIF 2 cycle phase counter value [7:0], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE2_CTL should be set as 2*Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 2*135,000,000/ (32*44,100*2*2) = 47.8. SPDIF_PHASE2_CTL should set to 48.

EDPTX_SPDIF_PHASE2_CTL_1

Address: Operational Base + offset (0x065C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase2_ctl_en This register enables force of the 2 cycle phase counter value function. 1'b0: SPDIF 2 cycle phase counter value use chip counted value. 1'b1: SPDIF 2 cycle phase counter value use the data written to register SPDIF_PHASE2_CTL_0 and SPDIF_PHASE2_CTL_1.
6:1	RO	0x00	reserved
0	RW	0x0	spdif_phase2_ctl_1 This register control SPDIF 2 cycle phase counter value [8], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [8] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register.

EDPTX_SPDIF_PHASE3_CTL_0

Address: Operational Base + offset (0x0660)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	spdif_phase3_ctl_0 This register control SPDIF 3 cycle phase counter value [7:0], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE3_CTL should be set as 3*Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 3*135,000,000/ (32*44,100*2*2) = 71.7. SPDIF_PHASE3_CTL should set to 72.

EDPTX_SPDIF_PHASE3_CTL_1

Address: Operational Base + offset (0x0664)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase3_ctl_en This register enables force of the 3 cycle phase counter value function. 1'b0: SPDIF 3 cycle phase counter value use chip counted value. 1'b1: SPDIF 3 cycle phase counter value use the data written to register SPDIF_PHASE3_CTL_0 and SPDIF_PHASE3_CTL_1.
6:1	RO	0x00	reserved
0	RW	0x0	spdif_phase3_ctl_1 This register control SPDIF 3 cycle phase counter value [8], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [8] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register.

EDPTX_LINK_BW_SET

Address: Operational Base + offset (0x0680)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0xa	link_bw_set Main link bandwidth setting: 4'b0110: 1.62Gpbs per lane 4'b1010: 2.7Gpbs per lane Other: Reserved

EDPTX_LANE_COUNT_SET

Address: Operational Base + offset (0x0684)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	lane_count_set Main link lane count 3'b001: one lane 3'b010: two lanes 3'b100: four lanes Other: Reserved

EDPTX_DP_TRAINING_PTN_SET

Address: Operational Base + offset (0x0688)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	scrambling_disable Disable scramble 1'b1: Disable 1'b0: Normal operation
4:2	RW	0x0	link_qual_pattern_set Link quality pattern setting. 3'b101: HBR2 Compliance 3'b100: 80 bit test pattern 3'b011: PRBS 7 bit 3'b010: symbol error rate measurement pattern is sent 3'b001: D10.2 test pattern is sent 3'b000: link quality test pattern not sent
1:0	RW	0x0	sw_training_pattern_set Link training pattern setting. SW_TRAINING_PATTERN_SET has higher priority than LINK_QUAL_PATTER_SET. 2'b11: Reserved 2'b10: Sending training pattern 2 2'b01: Sending training pattern 1 2'b00: Training pattern not sent

EDPTX_DP_LN0_LINK_TRAINING_CTL
Address: Operational Base + offset (0x068C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_0 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.
4:3	RW	0x0	pre_emphasis_set_0 Lane 0 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_0 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For test purpose only. This bit's type is RO. For more information, refer to MAX_PRE_REACH_0.
1:0	RW	0x0	drive_current_set_0 Lane 0 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_LN1_LINK_TRAINING_CTL
Address: Operational Base + offset (0x0690)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_1 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.

Bit	Attr	Reset Value	Description
4:3	RW	0x0	pre_emphasis_set_1 Lane 1 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_1 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_1. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_1 Lane 1 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_LN2_LINK_TRAINING_CTL

Address: Operational Base + offset (0x0694)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_2 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.
4:3	RW	0x0	pre_emphasis_set_2 Lane 2 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_2 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_2. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_2 Lane 2 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_LN3_LINK_TRAINING_CTL

Address: Operational Base + offset (0x0698)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_3 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.

Bit	Attr	Reset Value	Description
4:3	RW	0x0	pre_emphasis_set_3 Lane 3 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RO	0x0	max_drive_reach_3 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_3. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_3 Lane 3 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDPTX_DP_HW_LINK_TRAINING_CTL

Address: Operational Base + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	hw_training_error_code Training error code 3'b000: OK 3'b001: AUX_WRITE_ERROR 3'b010: MAX_DRIVE_REACHED 3'b011: WRONG_LANE_COUNT_SETTING 3'b100: LOOP_SAME_5_TIME 3'b101: CR_FAIL_IN_EQ 3'b110: EQ_LOOP_5_TIME
3:1	RO	0x0	reserved
0	RW	0x0	hw_training_en Link training sequence enable Write 1 to enable training sequence, write 0 to force training sequence stop, this bit will self-clear when training done.

EDPTX_HPD_DEGLITCH_L

Address: Operational Base + offset (0x06C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5e	hpd_deglitch_l HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal This register is HPD_DEGLITCH [7:0]. The default value is 0x5E for 280.75 us deglitch time.

EDPTX_HPD_DEGLITCH_H

Address: Operational Base + offset (0x06C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1a	hpd_deglitch_h HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal. This register is HPD_DEGLITCH [13:8]. The default value is 0x1A for 280.75 us deglitch time.

EDPTX_POLLING_PERIOD

Address: Operational Base + offset (0x06CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x0e	polling_period This register controls the interval between each time of polling operation. Interval time = POLLING_PERIOD * 2^16 * Period of 24M clock.

EDPTX_DP_LINK_DEBUG_CTL

Address: Operational Base + offset (0x06E0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	new_prbs7 Control the PRBS 7 formula. 1'b1: Use new PRBS7 formula in DP 1.1 version 1'b0: Use old PRBS7 formula in DP 1.0 version
3	RW	0x0	dis_fifo_rst Disable video FIFO reset every line 1'b1: Disable 1'b0: Reset video FIFO every line
2	RW	0x0	disable_auto_reset_encoder Disable 8b/10 encoder auto reset 1'b1: Disabled auto reset 8b/10 encode before sending Link Training Pattern 2 1'b0: Auto reset 8b/10 encode before sending Link Training Pattern 2
1	RO	0x0	reserved
0	RW	0x0	prbs31_en Enable DisplayPort PRBS 31. 1'b1: Enabled 1'b0: Normal mode

EDPTX_DP_SINK_COUNT

Address: Operational Base + offset (0x06E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_sink_count Sink Count

EDPTX_DP_IRD_VECTOR

Address: Operational Base + offset (0x06E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_ird_vector Irq_vector

EDPTX_DP_LINK_STATUS0

Address: Operational Base + offset (0x06EC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln1_sybol_lock Lane1 symbol lock

Bit	Attr	Reset Value	Description
5	RW	0x0	ln1_eq_done Lane1 EQ done
4	RW	0x0	ln1_cr_done Lane1 CR done
3	RO	0x0	reserved
2	RW	0x0	ln0_sybol_lock Lane0 symbol lock
1	RW	0x0	ln0_eq_done Lane0 EQ done
0	RW	0x0	ln0_cr_done Lane0 CR done

EDPTX_DP_LINK_STATUS1
Address: Operational Base + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	inter_ln_align Interlace align
6	RW	0x0	ln3_sybol_lock Lane3 symbol lock
5	RW	0x0	ln3_eq_done Lane3 EQ done
4	RW	0x0	ln3_cr_done Lane3 CR done
3	RO	0x0	reserved
2	RW	0x0	ln2_sybol_lock Lane2 symbol lock
1	RW	0x0	ln2_eq_done Lane2 EQ done
0	RW	0x0	ln2_cr_done Lane2 CR done

EDPTX_DP_ALIGN_STATUS
Address: Operational Base + offset (0x06F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_align_status ALIGN_STATUS

EDPTX_M_VID_0
Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_0 M_VID [7:0]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDPTX_M_VID_1
Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_1 M_VID [15:8]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDPTX_M_VID_2

Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_2 M_VID [23:16]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDPTX_N_VID_0

Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_0 N_VID[7:0] The maximum value of M_VID is 0xFFFF in ASYNC mode.

EDPTX_N_VID_1

Address: Operational Base + offset (0x0710)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_1 N_VID[15:8]

EDPTX_N_VID_2

Address: Operational Base + offset (0x0714)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_2 N_VID[23:16]

EDPTX_M_VID_MON

Address: Operational Base + offset (0x0718)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	m_vid_mon This register shows M_VID value which is actually transmitted to Rx for monitoring purpose.

EDPTX_DP_VIDEO_FIFO_THRD

Address: Operational Base + offset (0x0730)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	video_th_ctrl Video Data FIFO threshold control enables. 1'b1: Video Data FIFO threshold uses VIDEO_TH_VALUE. 1'b0: Video Data FIFO threshold uses internal calculate value automatically.
3:0	RW	0x0	video_th_value Video Data FIFO threshold value. If VIDEO_TH_CTRL is 1, and data count in video data FIFO have reached FIFO threshold value, video data is read out from FIFO.

EDPTX_DP_GNS_CTRL

Address: Operational Base + offset (0x0734)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	eq_training_loop_control 1'b1: Enable 1'b0: Disable
5	RO	0x0	reserved
4	RW	0x0	scramble_ctrl Scramble formula control: 1'b1: New formula 1'b0: Old formula
3	RW	0x0	in_ex Control scrambler structure: 1'b1: Internal type 1'b0: External type
2	RW	0x0	disable_serdes_fifo_rset 1'b1: Disable serdes FIFO auto reset. 1'b0: Enable serdes FIFO auto reset.
1	RW	0x0	video_map_ctrl Control use or not the video data map in YCbCr 4:2:2 mode: 1'b1: Use video data map in YCbCr 4:2:2 mode 1'b0: Don't use
0	RW	0x0	rs_ctrl Control RS parameter: 1'b1: Parameter define by V1.0 1'b0: Parameter in GNS

EDPTX_DP_AUDIO_MARGIN
Address: Operational Base + offset (0x073C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	force_audio_margin Force audio margin 1'b1: Audio margin use register value AUDIO_MARGIN. 1'b0: Audio margin use hardware calculation. It is the default setting.
6:0	RW	0x00	audio_margin Audio packet is sent out during vertical blank or horizontal blank. This register is used to specify minimum stream clock cycles to transfer audio stream packet. If current remaining stream clock cycles before sending active video data is less than the value, DP postpone sending audio stream packets to the next video blank interval. AUDIO_MARGIN only takes effect when FORCE_AUDIO_MARGIN is set 1.

EDPTX_M_AUD_MON
Address: Operational Base + offset (0x0740)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	m_aud_mon This register shows M_AUD value which is actually transmitted to Rx for monitoring purpose.

EDPTX_M_AUD_0
Address: Operational Base + offset (0x0748)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_aud_0 M_AUD [7:0]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDPTX_M_AUD_1

Address: Operational Base + offset (0x074C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_aud_1 M_AUD [15:8]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDPTX_M_AUD_2

Address: Operational Base + offset (0x0750)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	m_aud_2 M_AUD [23:16]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDPTX_N_AUD_0

Address: Operational Base + offset (0x0754)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_0 N_AUD[7:0]

EDPTX_N_AUD_1

Address: Operational Base + offset (0x0758)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_1 N_AUD[15:8]

EDPTX_N_AUD_2

Address: Operational Base + offset (0x075C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_2 N_AUD[23:16]

EDPTX_DP_M_CAL_CTL

Address: Operational Base + offset (0x0760)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	m_aud_gen_filter_en Enable M_AUD value generation filter to reduce the variation of M_AUD value. This filter is a low-pass filter to smooth out the M_AUD variation 1'b1: Enable the filter 1'b0: Disable the filter

Bit	Attr	Reset Value	Description
2	RW	0x0	m_vid_gen_filter_en Enable M_VID value generation filter to reduce the variation of M_VID value. This filter is a low-pass filter to smooth out the M_VID variation 1'b1: Enable the filter 1'b0: Disable the filter
1	RO	0x0	reserved
0	RW	0x0	m_gen_clk_sel Select which link clock is used to generate the M value 1'b1: Clock with down spreading is used 1'b0: Clock without down spreading is used

EDPTX_M_VID_GEN_FILTER_TH

Address: Operational Base + offset (0x0764)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	m_vid_gen_filter_th The threshold of M_VID generation filter. It only takes effect when M_VID_GEN_FILTER_EN is set to 1

EDPTX_M_AUD_GEN_FILTER_TH

Address: Operational Base + offset (0x0778)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	m_aud_gen_filter_th The threshold of M_AUD generation filter. It only takes effect when M_AUD_GEN_FILTER_EN is set to 1

EDPTX_AUX_CH_STA

Address: Operational Base + offset (0x0780)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	aux_busy AUX channel status bit. If this bit is read as 1, AUX channel access should be halted. 1'b1: AUX CH is busy 1'b0: AUX CH is idle
3:0	RW	0x0	aux_status This register indicate the AUX channel access status 4'b0000: OK 4'b0001: NACK_ERROR 4'b0010: TIMEOUT_ERROR 4'b0011: UNKNOWN_ERROR 4'b0100: MUCH_DEFER_ERROR 4'b0101: TX_SHORT_ERROR 4'b0110: RX_SHORT_ERROR 4'b0111: NACK_WITHOUT_M_ERROR 4'b1000: I2C_NACK_ERROR Other: Reserved

EDPTX_AUX_ERR_NUM

Address: Operational Base + offset (0x0784)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	aux_err_num The error number counter of AUX channel counts when AUX channel access failed. In AUX CH reading, this number indicates the number of read back byte. In AUX CH writing, this number indicates the number of reply command.

EDPTX_AUX_CH_DEFER_CTL

Address: Operational Base + offset (0x0788)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	defer_ctrl_en AUX CH received DEFER command count control enable 1'b1: If the count that AUX CH receive DEFER command equal to (DEFER_COUNT * 64), the AUX CH transaction is terminated, and the AUX_STATUS is 0100 1'b0: The count that AUX CH receive DEFER command is unlimited
6:0	RW	0x7f	defer_count The count is defined to limit the max count AUX CH receive DEFER command. When DEFER_CTRL_EN is 1 and AUX CH received (DEFER_COUNT * 64) DEFER command, the AUX CH will terminate the transaction

EDPTX_AUX_RX_COMM

Address: Operational Base + offset (0x078C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aux_rx_comm AUX CH received command

EDPTX_BUFFER_DATA_CTL

Address: Operational Base + offset (0x0790)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	buf_clr Write 1 to this bit to clear AUX CH data buffer (BUF_DATA_0 ~ BUF_DATA_15). Always read back 0 from this bit. This bit's type is R/W. This bit is self cleared. Note: For the write operation, set this bit to 1 before writing data to BUF_DATA_0~15. And for READ operation, this bit has only to be set before starting data transfer by setting AUX_EN.
6:5	RO	0x0	reserved
4	RW	0x0	buf_have_data 1'b0: Buffer have data 1'b1: Buffer have not data
3:0	RW	0x0	buffer_data_count The counts of data AUX CH buffer have.

EDPTX_AUX_CH_CTL_1

Address: Operational Base + offset (0x0794)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	aux_length Register control AUX CH transaction length.
3:0	RW	0x0	aux_tx_comm Register control AUX CH transaction command.

EDPTX_AUX_ADDR_7_0

Address: Operational Base + offset (0x0798)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aux_addr_7_0 AUX_ADDR[7:0], Register control AUX CH address.

EDPTX_AUX_ADDR_15_8

Address: Operational Base + offset (0x079C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aux_addr_15_8 AUX_ADDR[15:8], Register control AUX CH address

EDPTX_AUX_ADDR_19_16

Address: Operational Base + offset (0x07A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aux_addr_19_16 AUX_ADDR[7:0], Register control AUX CH address.

EDPTX_AUX_CH_CTL_2

Address: Operational Base + offset (0x07A4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	pd_aux_idle Power down AUX CH when AUX CH is in idle state. 1'b1: Power down AUX CH in idle state. 1'b0: Keep AUX CH power up in idle state.
2	RW	0x0	aux_pn_inv Invert AUX CH PN 1'b1: Invert PN 1'b0: Normal mode
1	RW	0x0	addr_only AUX CH issue "address only" command 1'b1: Issue "address only" command 1'b0: Normal AUX CH command
0	RW	0x0	aux_en Register control AUX CH operation enable Write 1 to this bit to enable AUX CH operation This bit will self-clear when AUX CH operation is finished. This bit is self cleared.

EDPTX_BUF_DATA

Address: Operational Base + offset (0x07C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xff	buf_data AUX CH buffer data 0 ~ 15

EDPTX_SOC_GENERAL_CTL

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	audio_bit_mapping_type Audio bit mapping type in 16bit audio mode 2'b00: Type 0 2'b01: Type 1 2'b10: Type 2 2'b11: Reserved
15	RO	0x0	reserved
14:13	RW	0x0	pcm_size PCM data bit size 2'b00: 16 bit 2'b01: 20 bit 2'b10: 24 bit 2'b11: Reserved
12:5	RO	0x00	reserved
4:0	RW	0x00	audio_ch_status_same Select the channel status bits for audio channel 3~8. 1'b1: Use the same data channel status bits from AUDIO_GP0_STATUS_n registers. 1'b0: Use each channel status bits from the corresponding AUDIO_GPx_STATUS_n registers.

EDPTX_DP_TEST_80B_PATTERN0

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dp_test_80b_pattern0 DP test 80bit pattern0[29:0]

EDPTX_DP_TEST_80B_PATTERN1

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dp_test_80b_pattern1 DP test 80bit pattern0[59:30]

EDPTX_DP_TEST_80B_PATTERN2

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	dp_test_80b_pattern2 DP test 80bit pattern0[79:60]

EDPTX_AUD_CTL

Address: Operational Base + offset (0x0834)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	aud_channel_count Audio Channel Number 3'b001: 2 channel 3'b011: 4 channel 3'b101: 6 channel 3'b111: 8 channel

EDPTX_CRC_CON

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	vid_crc_flush Video CRC flush enable. The video CRC value is initialized at every v-sync.
1	RO	0x0	reserved
0	RW	0x0	vid_crc_enable Video CRC enable. 1'b0: Disable 1'b1: Enable

EDPTX_CRC_RESULT

Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	aud_crc_result Audio CRC result
15:0	RW	0x0000	vid_crc_result Video CRC result

EDPTX_I2S_CTRL

Address: Operational Base + offset (0x09C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	i2s_en I2S enable
3:0	RW	0x0	i2s_fmt_ctrl I2S Format Control

EDPTX_I2S_CH_SWAP

Address: Operational Base + offset (0x09CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	i2s_ch_swap I2S channel swap
3:0	RW	0xb	i2s_wd_len I2S word length

EDPTX_I2S_CH_CTRL

Address: Operational Base + offset (0x09D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xe4	i2s_ch_ctrl I2S channel control

EDPTX_I2S_CH_CTRL1

Address: Operational Base + offset (0x09D4)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	i2s_aud_layout Audio layout
1	RW	0x0	i2s_aud_v_bit Audio v_bit
0	RW	0x0	i2s_aut_ext_sta Audio ext channel status

EDPTX_LINK_POLICY

Address: Operational Base + offset (0x09D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	alternate_sr_en Alternate SR enable
6:4	RW	0x5	link_train_cr_lp_in Link training CR loop in
3	RW	0x0	link_train_wr_en Training first write en
2	RO	0x0	reserved
1	RW	0x0	link_train_inv Invert training bit enable
0	RW	0x0	frame_change_en Framing change enable

23.5 Interface Description

Table 23-1 EDP TX Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
edptx0_ln0_txdp	O	HDMI_TX0_D0P/eDP_TX0_D0P	NS
edptx0_ln0_txdn	O	HDMI_TX0_D0N/eDP_TX0_D0N	NS
edptx0_ln1_txdp	O	HDMI_TX0_D1P/eDP_TX0_D1P	NS
edptx0_ln1_txdn	O	HDMI_TX0_D1N/eDP_TX0_D1N	NS
edptx0_ln2_txdp	O	HDMI_TX0_D2P/eDP_TX0_D2P	NS
edptx0_ln2_txdn	O	HDMI_TX0_D2N/eDP_TX0_D2N	NS
edptx0_ln3_txdp	O	HDMI_TX0_D3P/eDP_TX0_D3P	NS
edptx0_ln3_txdn	O	HDMI_TX0_D3N/eDP_TX0_D3N	NS
edptx0_sbdp	I/O	HDMI_TX0_SBDP/eDP_TX0_AUXP	NS
edptx0_sbdn	I/O	HDMI_TX0_SBDN/eDP_TX0_AUXN	NS
edptx1_ln0_txdp	O	HDMI_TX1_D0P/eDP_TX1_D0P	NS
edptx1_ln0_txdn	O	HDMI_TX1_D0N/eDP_TX1_D0N	NS
edptx1_ln1_txdp	O	HDMI_TX1_D1P/eDP_TX1_D1P	NS
edptx1_ln1_txdn	O	HDMI_TX1_D1N/eDP_TX1_D1N	NS
edptx1_ln2_txdp	O	HDMI_TX1_D2P/eDP_TX1_D2P	NS
edptx1_ln2_txdn	O	HDMI_TX1_D2N/eDP_TX1_D2N	NS
edptx1_ln3_txdp	O	HDMI_TX1_D3P/eDP_TX1_D3P	NS
edptx1_ln3_txdn	O	HDMI_TX1_D3N/eDP_TX1_D3N	NS
edptx1_sbdp	I/O	HDMI_TX1_SBDP/eDP_TX1_AUXP	NS
edptx1_sbdn	I/O	HDMI_TX1_SBDN/eDP_TX1_AUXN	NS

Module Pin	Direction	Pad Name	IOMUX Setting
edptx0_hpd_m0	I	HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[7:4]=4'h5
edptx0_hpd_m1	I	HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d	BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0]=4'h3
edptx1_hpd_m0	I	HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[11:8]=4'h5
edptx1_hpd_m1	I	GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d	BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4'h5

Notes: I=input, O=output, I/O=input/output, bidirectional, NS=Not Set

23.6 Application Notes

23.6.1 EDP TX Clock Domain Overview

The eDP TX clock domain can be seen in the figure below. The clock frequency of "o_tx_link_sym_clk" and "o_tx_hs_clk" should be set according to PHY registers. From the figure, can get this frequency relation,

o_tx_link_sym_clk = I_CH_TXD_CLK = I_CLK_DIV2 = i_tx_data_clk
o_tx_hs_clk = I_LINK_CLK
o_tx_hs_clk = 2 * o_tx_link_sym_clk

The clock o_tx_hs_clk has twice the frequency of o_tx_link_sym_clk. For example, link rate is 2.7Gbps, o_tx_hs_clk should be 270M and o_tx_link_sym_clk should be 135M.

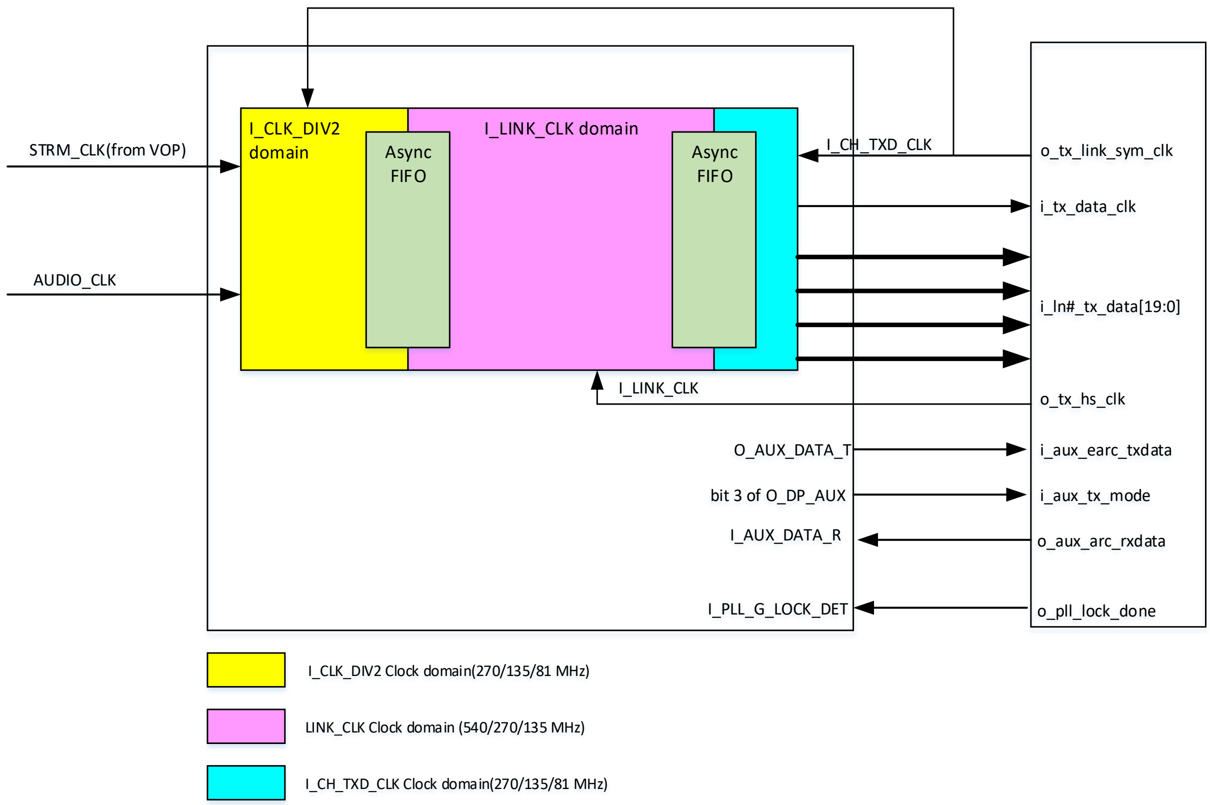

Fig. 23-4 DP Clock Domain

23.6.2 EDP TX Controller Programming Guide

After PHY is ready, the eDP TX controller can begin to work.

23.6.2.1 How to Initialize DP

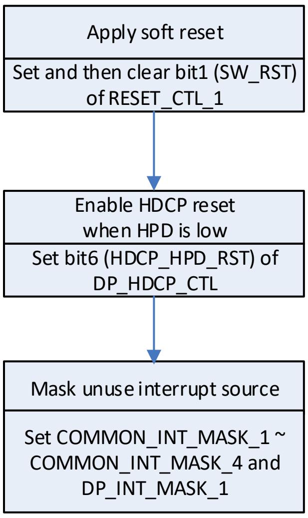

Fig. 23-5 DP controller Initial

23.6.2.2 How to Detect Hot Plug Insertion

In Wait Hot Plug state, chip is in power down status. System only responses to hot plug change interrupt. When a hot plug interrupt is detected, in the interrupt routine, firmware will judge whether it is a receiver plug-in or un-plug or link training request. If plug-in, chip will be powered on and system state will be set to Read and Parse EDID.

23.6.2.3 How to Access DPCD Space in DP Rx

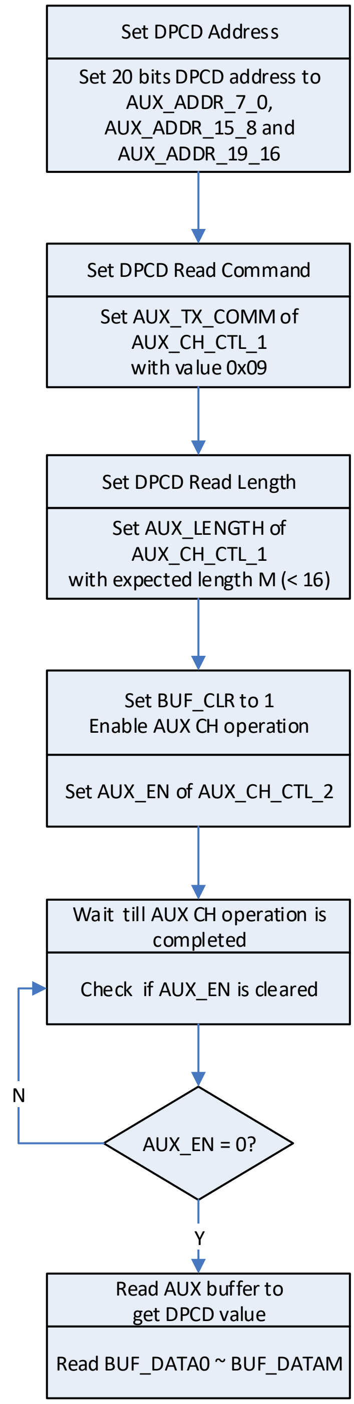

Fig. 23-6 DP DPCD Read

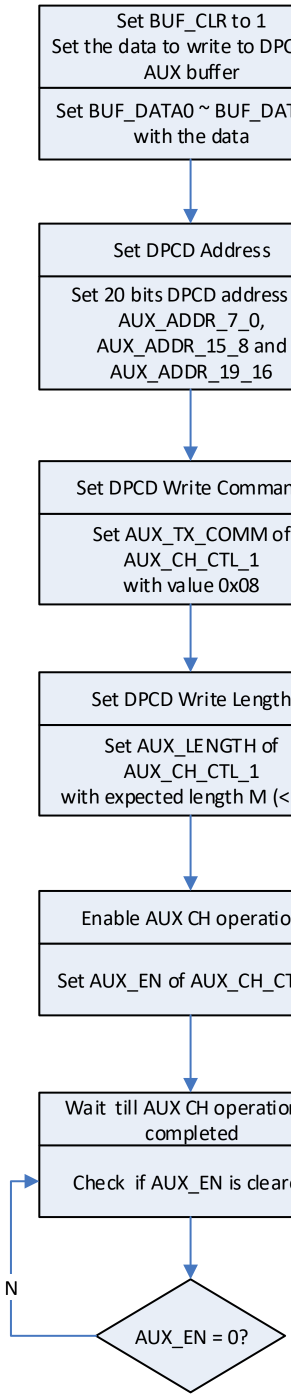

Fig. 23-7 DP DPCD Write

23.6.2.4 How to Write into EDID space in DP Rx

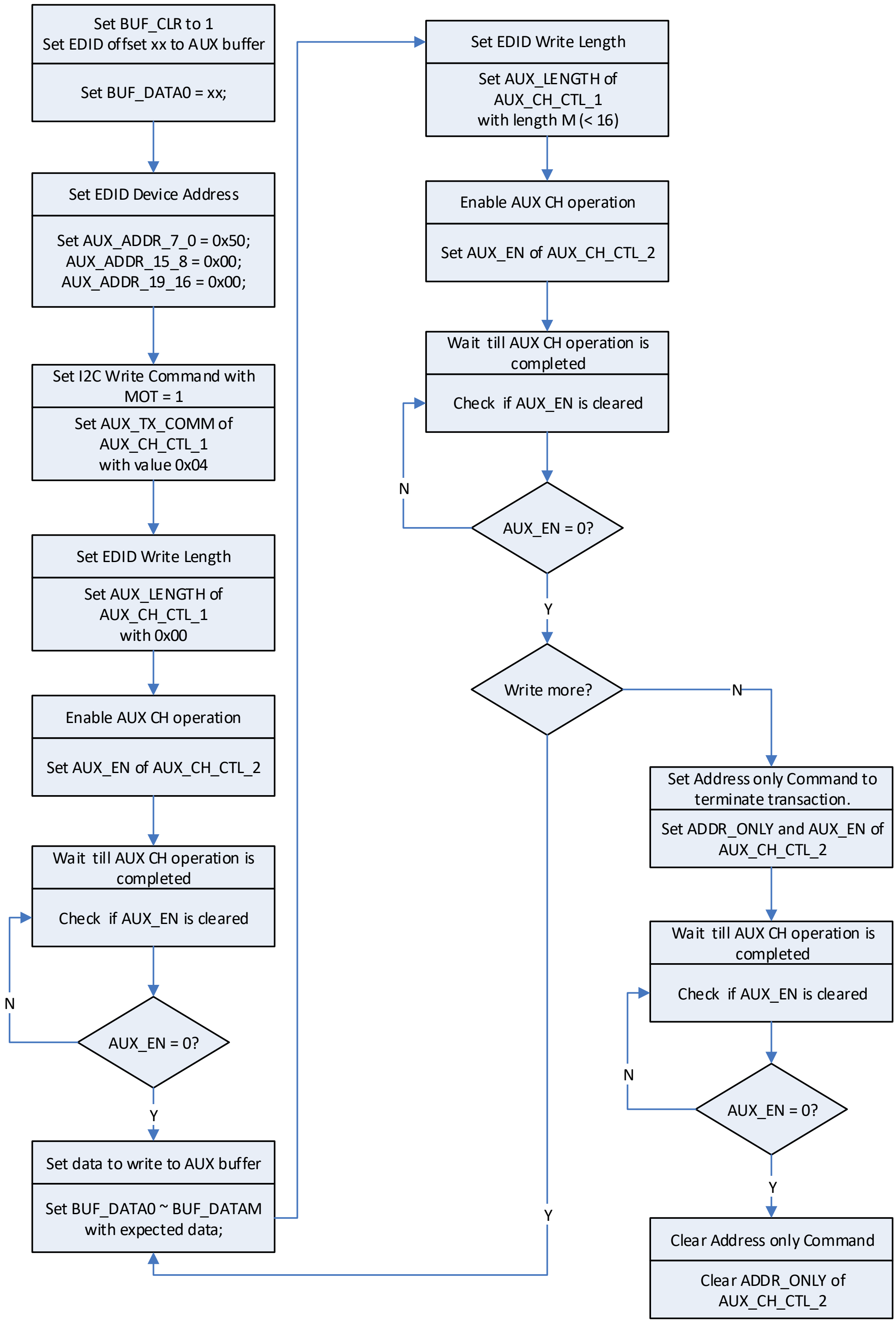

Fig. 23-8 Write into EDID space in DP Rx

23.6.2.5 How to READ From EDID Space in DP Rx

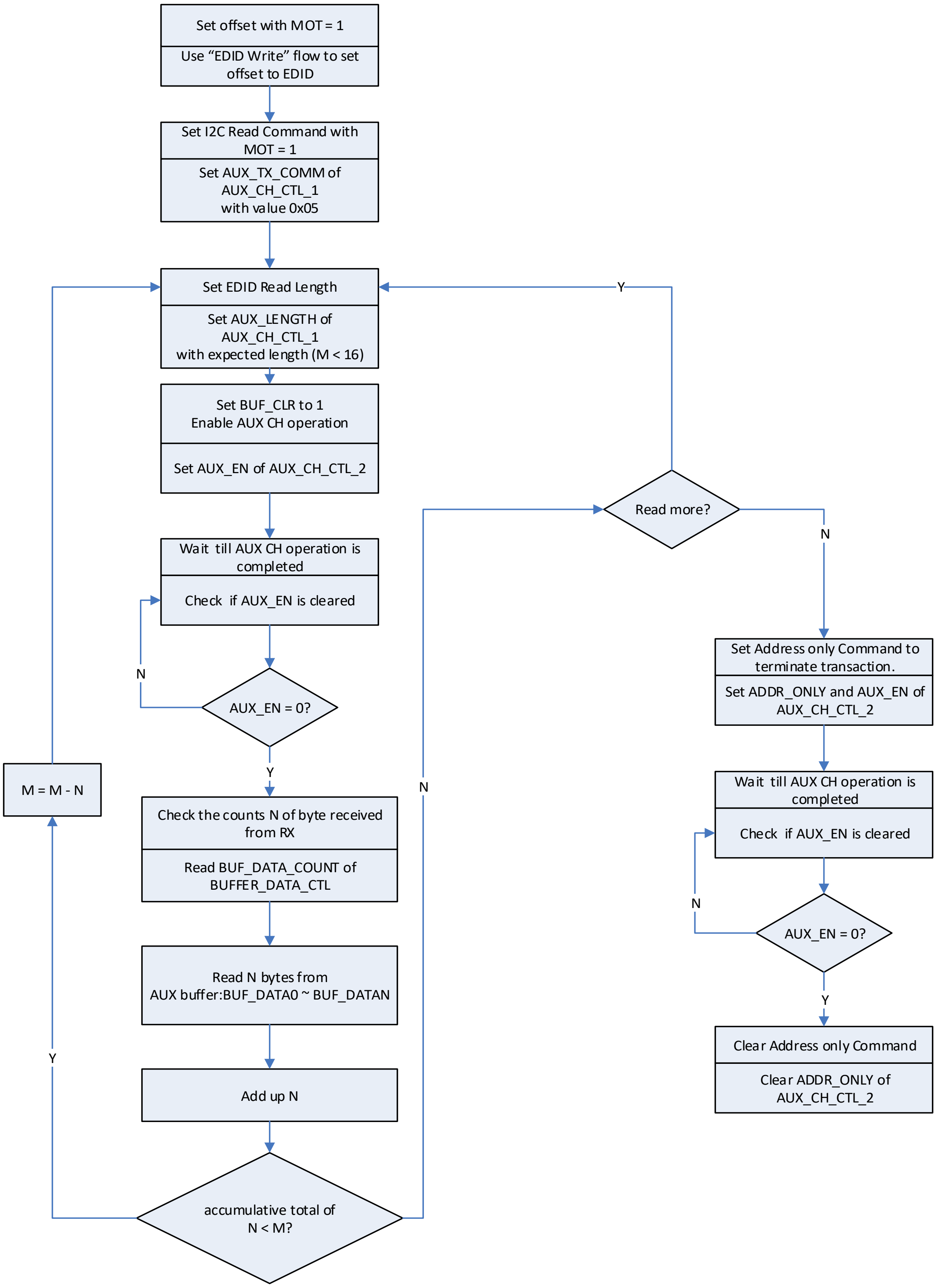

Fig. 23-9 Read from EDID space in DP Rx

23.6.2.6 How to do SW Link Training

23.6.2.6.1 State Machine of SW Link Training

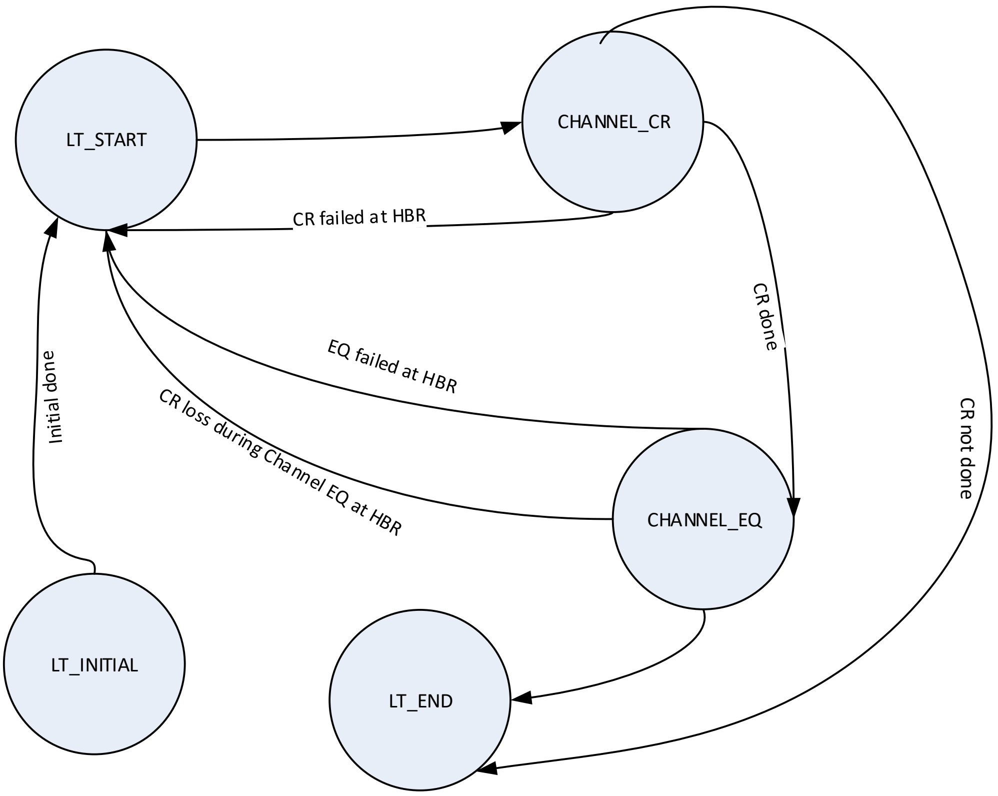

Fig. 23-10 State Machine of SW Link Training

23.6.2.6.2 State LT_INITIAL

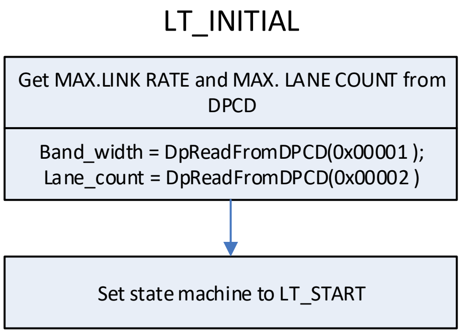

Fig. 23-11 State LT_INITIAL

23.6.2.6.3 State LT_START

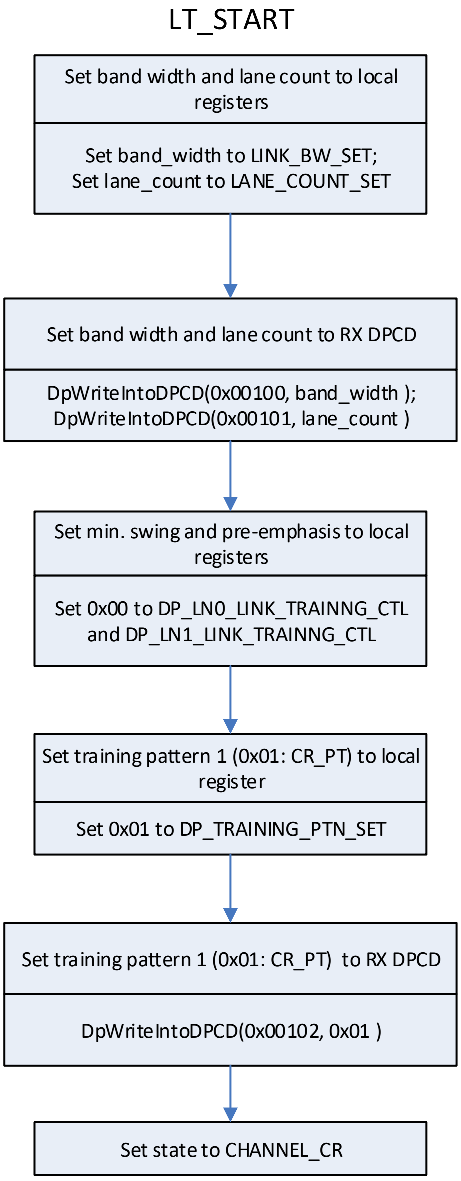

Fig. 23-12 State LT_START

23.6.2.6.4 State CHANNEL_CR

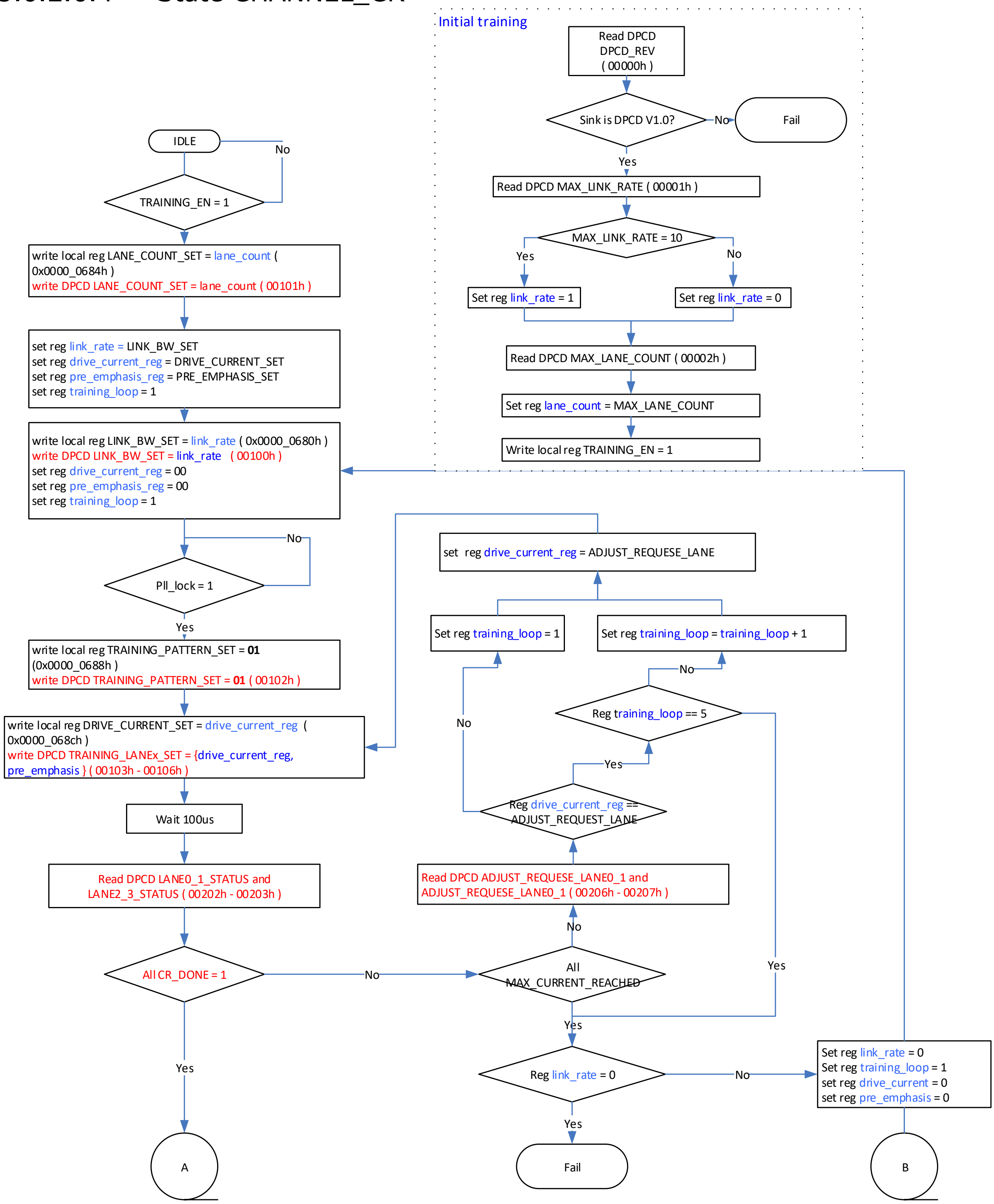

Fig. 23-13 Link Training Initial and Clock Recovery Training

23.6.2.6.5 State CHANNEL_EQ

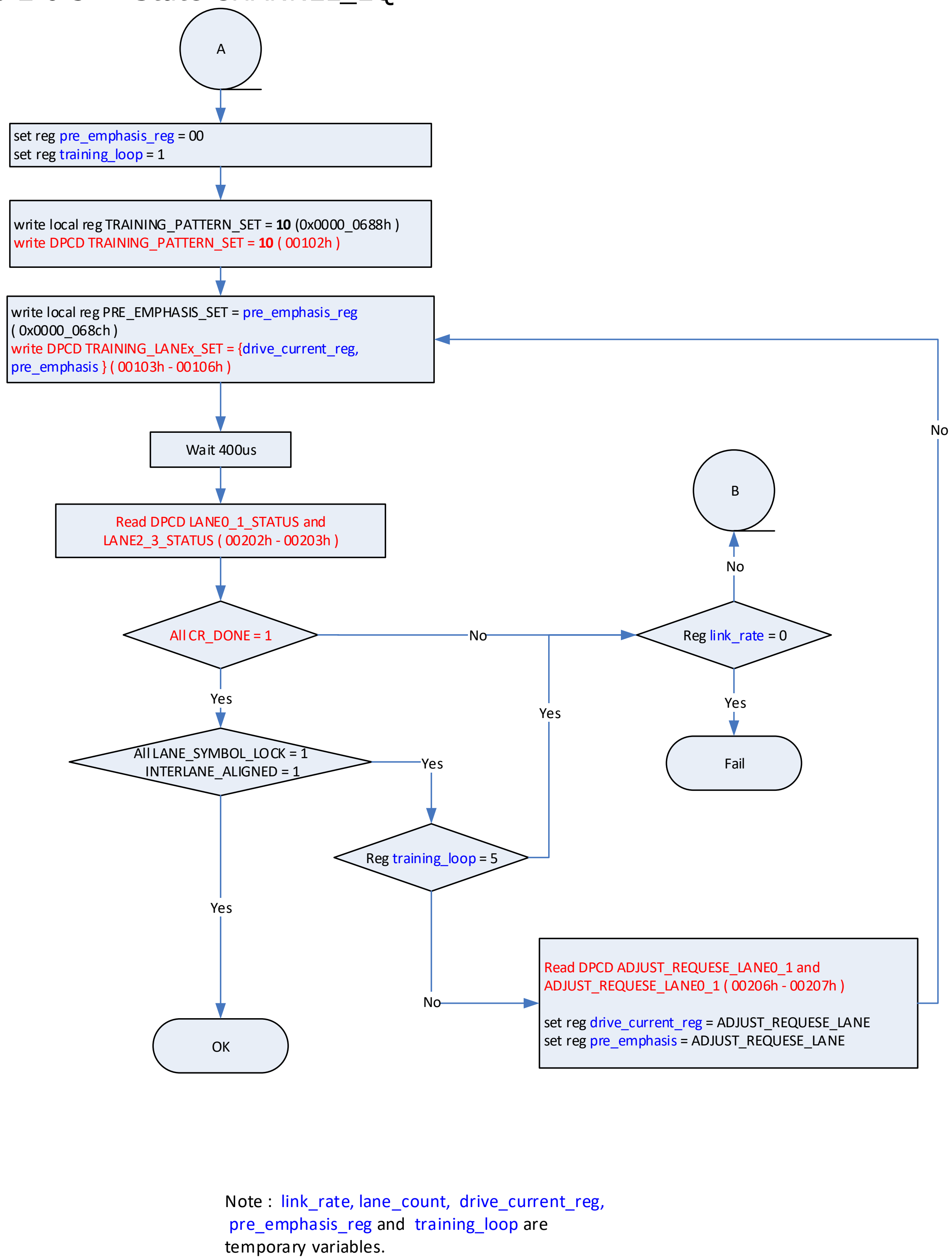

Fig. 23-14 Equalizer Training

23.6.2.7 How to Setup Main Stream Attribute Data

23.6.2.7.1 Attribute of Video timing

Chip hardware setups attribute of video timing automatically.

23.6.2.7.2 Attribute of Color Depth

Set IN_BPC of VIDEO_CTL_2 with correct value.

23.6.2.7.3 Attribute of Color Space

Set IN_COLOR_F of VIDEO_CTL_2 [1:0] with correct value.
IN_YC_COEFFI of VIDEO_CTL_3 [7] also must be set.

23.6.2.8 How to do HDCP Authentication and Encryption

23.6.2.8.1 Initialize HDCP Key

Taking eDP0 as an example, the configuration process is as follows.
<Step 1>Set HDCP Key write enable. <BUS_SGRF_SOC_CON21>[12] = 1’b0
<Step 2>Write HDCP Key into memory. The base HDCP key address for eDP0 is 0xFDF18000.
<Step 3>Set HDCP Key access by controller. <BUS_SGRF_SOC_CON21>[12] = 1’b1

For eDP1
<Step 1>Set HDCP Key write enable. <BUS_SGRF_SOC_CON21>[13] = 1’b0
<Step 2>Write HDCP Key into memory. The base HDCP key address for eDP1 is 0xFDF1C000.
<Step 3>Set HDCP Key access by controller. <BUS_SGRF_SOC_CON21>[13] = 1’b1

23.6.2.8.2 SW HDCP State Machine

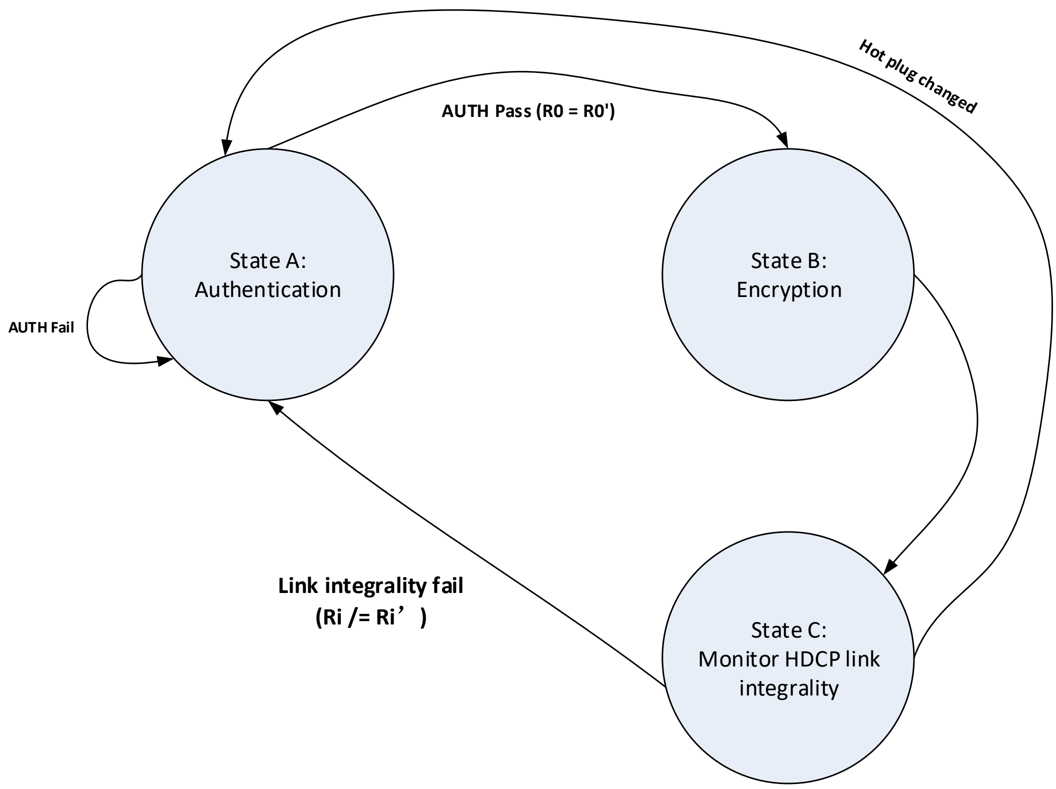

Fig. 23-15 SW HDCP State Machine

23.6.2.8.3 SW HDCP Flowchart

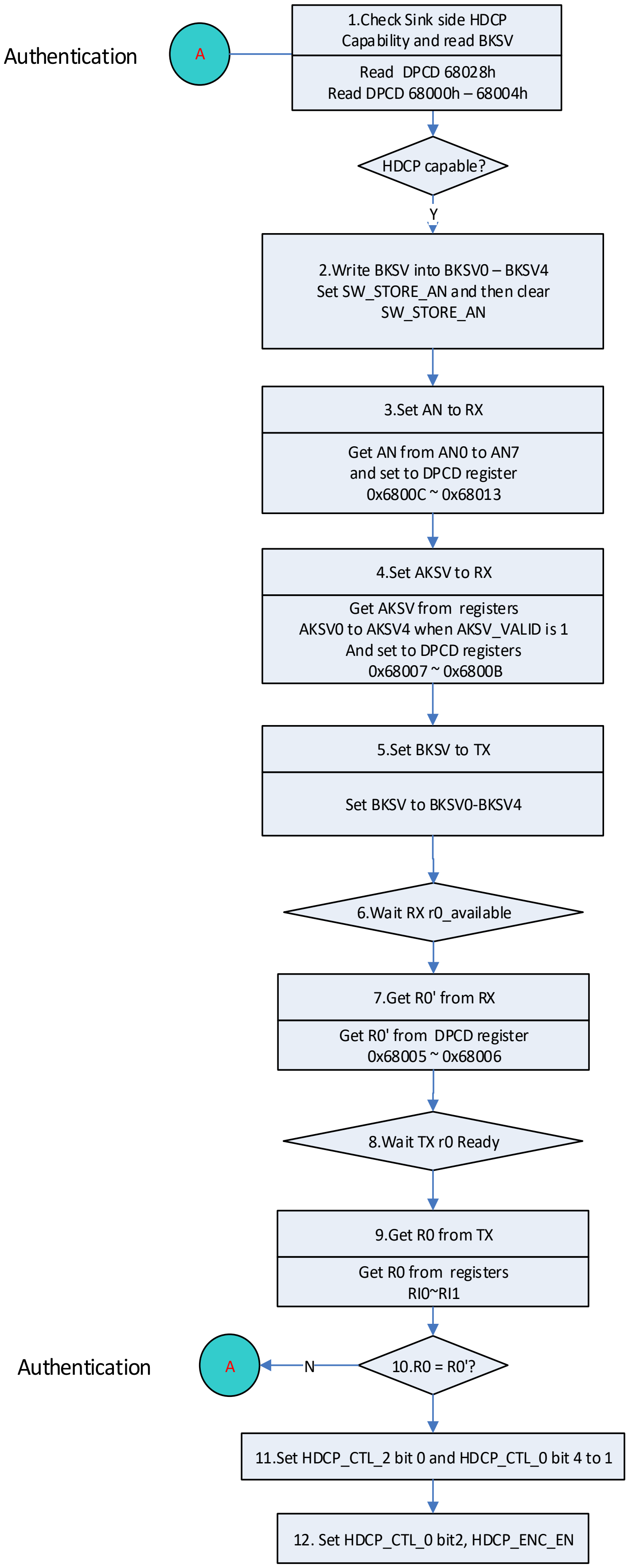

Fig. 23-16 SW HDCP Flowchart A

Note that BKSV to BKSV0~BKSV4 are loaded two times in step2 and in step5. With the first BKSV writing, AKSV starts to be loaded and SW_STORE_AN function is enabled. As another function, validity of BKSV is possible by the bit filed, BKSV_VALID. In the other hand, the second BKSV writing starts the R0 calculation.

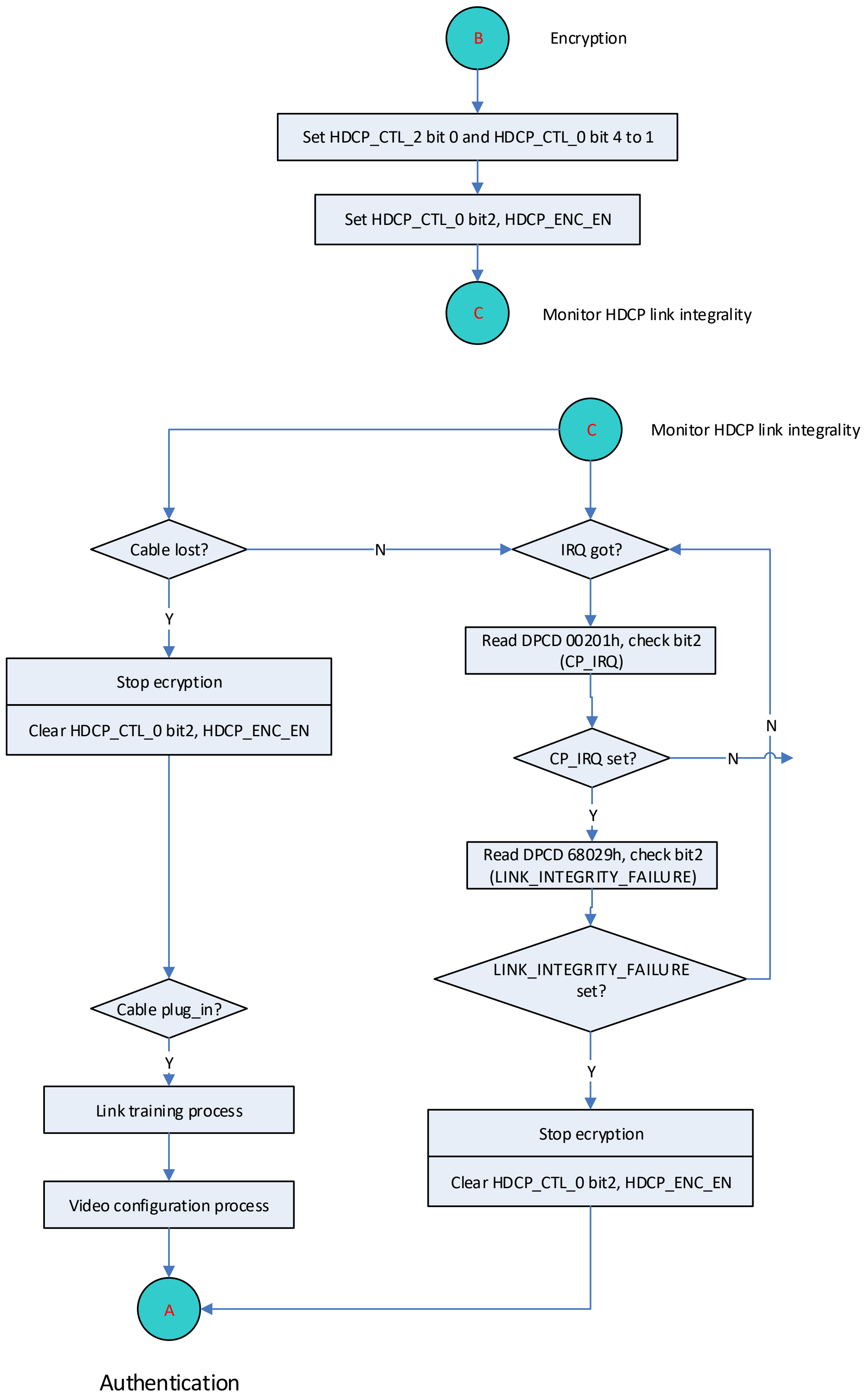

Fig. 23-17 SW HDCP Flowchart B

23.6.2.9 How to Configure Video

We suggest using M value auto-generated mode.
Slave mode video configuration process (M value auto-generated)

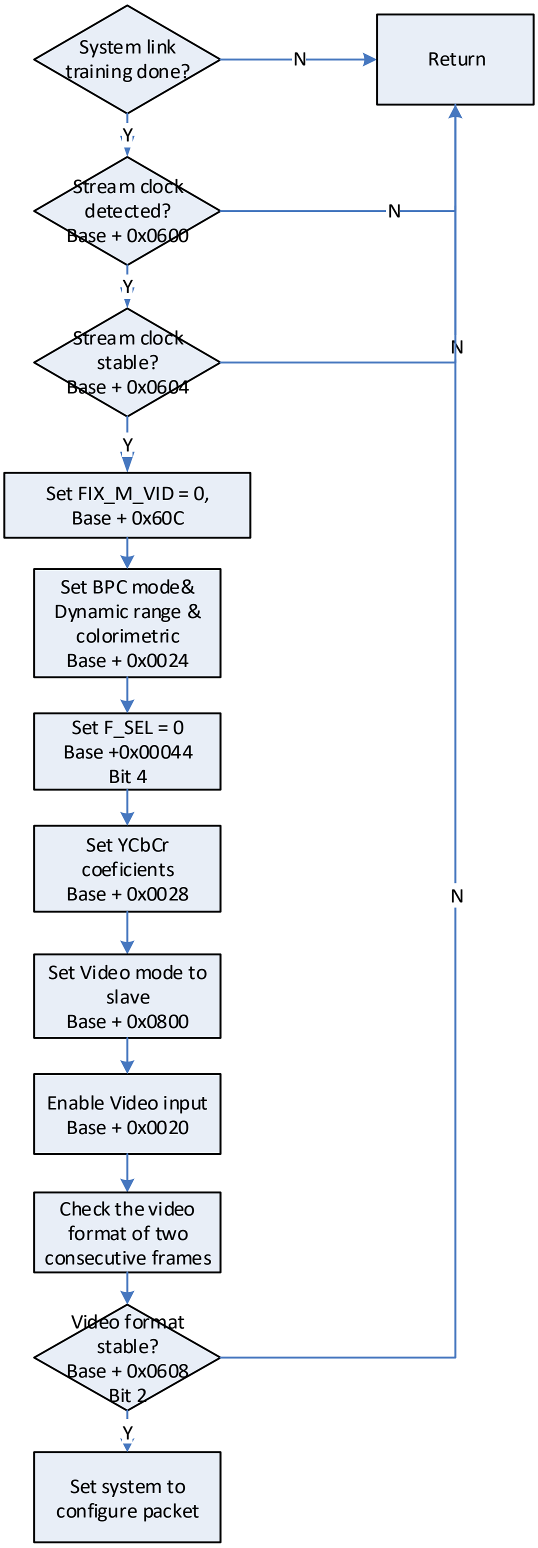

Fig. 23-18 Slave mode video configuration process (M value auto-generated)

Slave mode video configuration process (M value register defined 1400x1050/108M, RGB888, 2.7G)

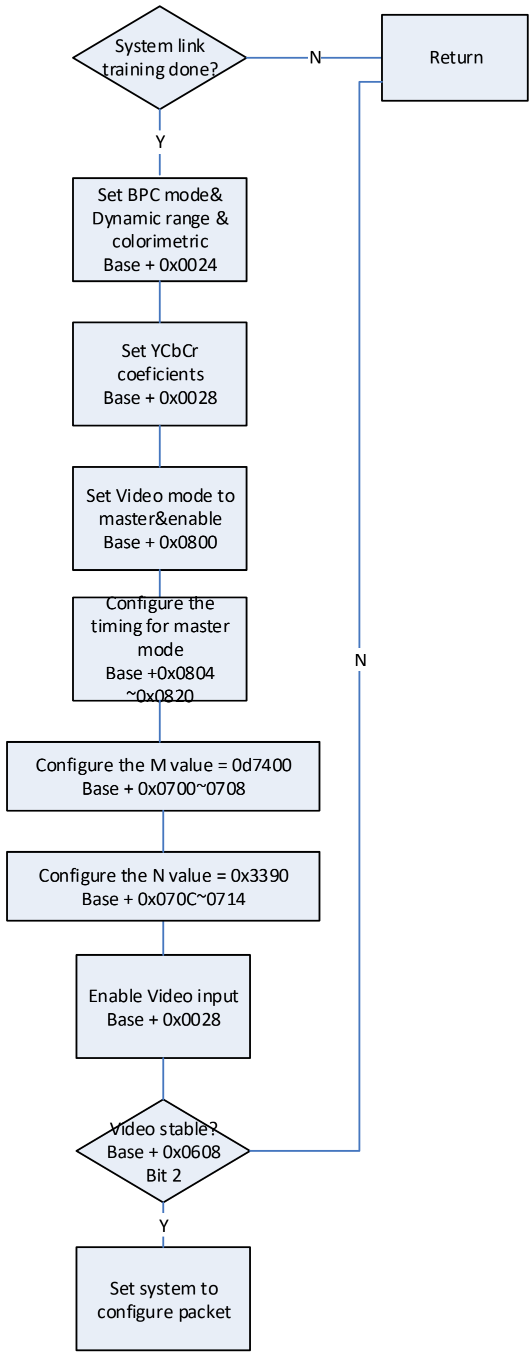

Fig. 23-19 Slave mode video configuration process (M value register defined)

Notes: Usually, you do not need to set FIX_M_VID to 1. We suggest that set FIX_M_VID to 0.

If FIX_M_VID is 0, then the hardware calculated M_VID value is used. But, if FIX_M_VID must be set to 1 by any reason, then M_VID_0, M_VID_1 and M_VID_2 should be set by using following formula.
M_VID = F_STRM_CLK * N_VID / FDIV2_CLK
Notes: F_STRM_CLK means the frequency of STRM_CLK, FDIV2_CLK means the frequency of I_CLK_DIV2. STRM_CLK and I_CLK_DIV2 can be found in figure DP Clock Domain.

N_VID must be choose let the result of this equation is an integer, for example N_VID is 13500 (0x34bc) in 2.7G and 8100 (0x1fa4) in 1.62G.
2.7G: M_VID = F_STRM_CLK*0x34BC/135M
1.62G: M_VID = F_STRM_CLK*0x1FA4/81M
For example, if input is 1400x1050/108M, RGB888, 2.7G,
M_VID = 108*0x34BC/135= 0x2A30,
set M_VID_0 = 0x30, set M_VID_1 = 0x2A, set M_VID_2 = 0.

23.6.2.10 How to Configure Audio

If want to transfer S/PDIF or I2S by eDP TX, please set these GRF registers first.
<VO1_GRF_VO1_CON0>[3] = 1'b1 //eDP0 I2S
<VO1_GRF_VO1_CON0>[4] = 1'b1 //eDP0 S/PDIF
<VO1_GRF_VO1_CON1>[3] = 1'b1 //eDP1 I2S
<VO1_GRF_VO1_CON1>[4] = 1'b1 //eDP1 S/PDIF
The controller should be set as below. We suggest using M value auto-generated mode.
Slave mode audio configuration process (M value auto-generated)

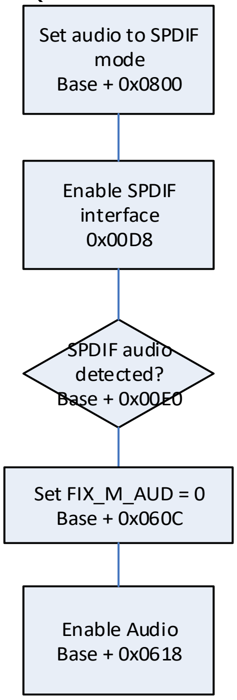

Fig. 23-20 Slave mode audio configuration process (M value auto-generated)

For example audio type is I2S, which is 2CH, 44.1kHz, 16 bits sample, setting as below

```
<EDPTX_DP_AUD_CTL>        = 0x11
<EDPTX_FUNC_EN_1>         = 0x04
<EDPTX_AUD_CTL>           = 0x01
<EDPTX_I2S_CTRL>          = 0x10
<EDPTX_I2S_CH_SWAP>       = 0x02
<EDPTX_DP_AUD_CTL>        = 0x15
<EDPTX_I2S_CH_CTRL1>      = 0x00

//I2S STA
<EDPTX_AUDIO_I2S_CH_STA1>       = 0x00
<EDPTX_AUDIO_I2S_CH_STA2>       = 0x00
<EDPTX_AUDIO_I2S_CH_STA3>       = 0x21
<EDPTX_AUDIO_I2S_CH_STA4>       = 0x10
<EDPTX_AUDIO_I2S_CH_STA5>       = 0x01
```

For other sample_rate, channel number and bits_per_sample, change the setting value.
If I2S is 8CH, <EDPTX_I2S_CH_CTRL1> bit2 should be 1'b1.
Slave mode audio configuration process (Register defined M value, 48 KHz, 2.7 G)

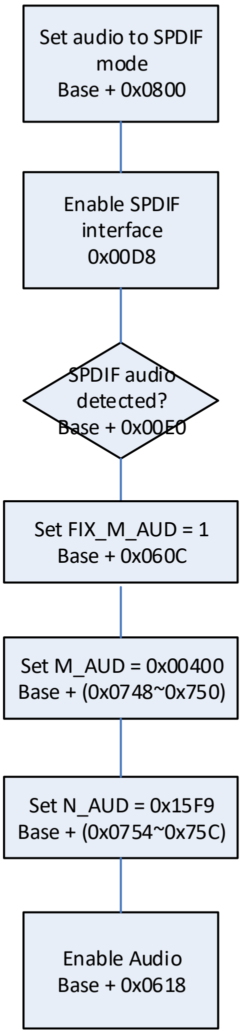

Fig. 23-21 Slave mode audio configuration process (Register defined M value)

Notes: Usually, you do not need to set FIX_M_AUD to 1. We suggest that set FIX_M_AUD to 0.

If FIX_M_AUD is 0, then the hardware calculated M_AUD value is used. But, if FIX_M_AUD must be set to 1 by any reason, then M_AUD_0, M_AUD_1, M_AUD_2 and N_AUD_0, N_AUD_1, N_AUD_2 should be set by using following formula.
M_AUD = 512*Faud_sample* N_AUD / 2 * FLS_CLK
Notes: Faud_sample is the sampling frequency of the audio stream being transported. FLS_CLK is the frequency of I_LINK_CLK. I_LINK_CLK can be found in figure 1-4 DP Clock Domain.

For example,
2.7G M_AUD = 512*Faud_sample *N_AUD/270,000,000
1.62G M_AUD = 512*Faud_sample*N_AUD/162,000,000

23.6.2.11 How to PROCESS interrupt

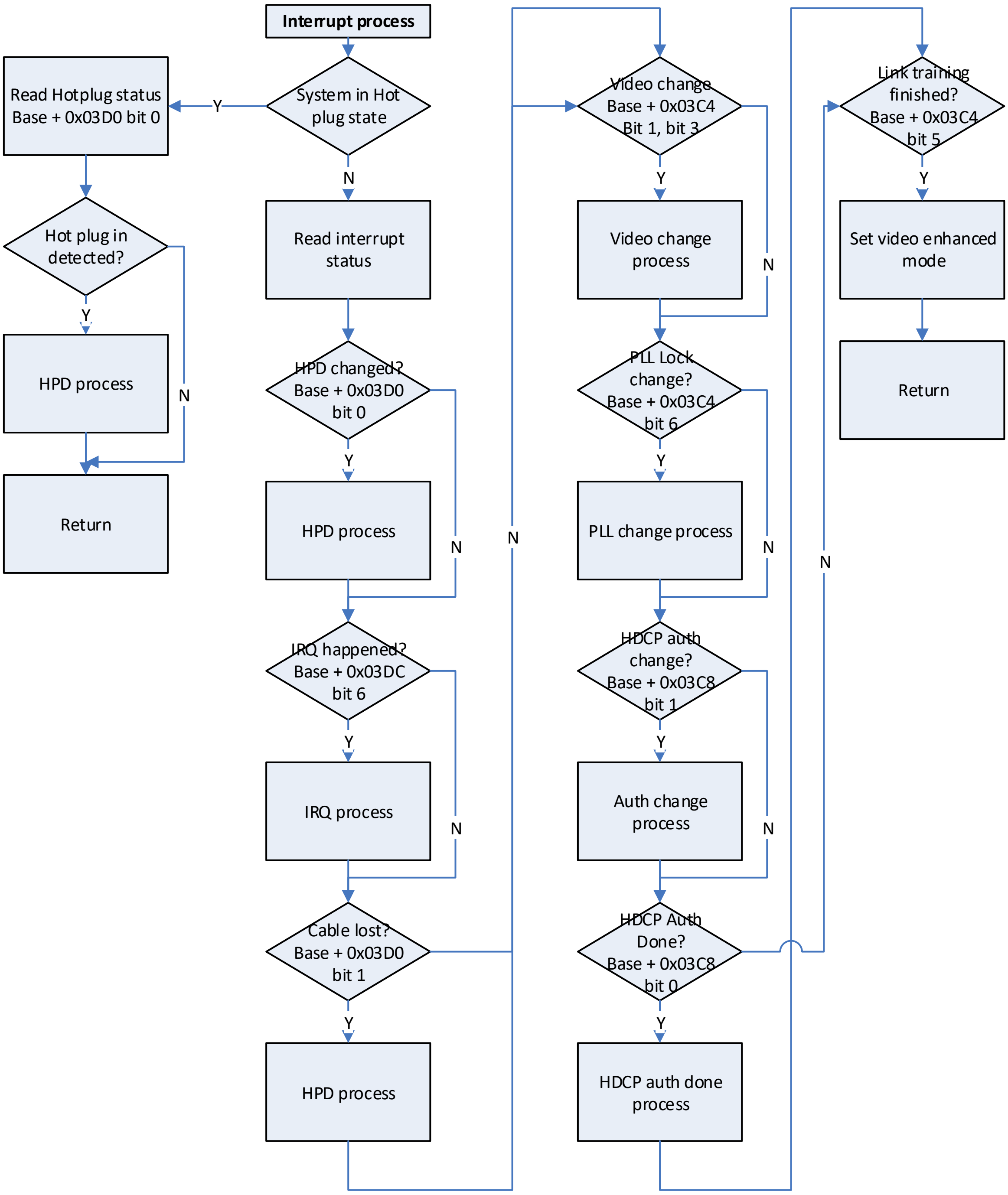

Fig. 23-22 Interrupt process

23.6.2.12 How to Send Auxiliary Information Packets

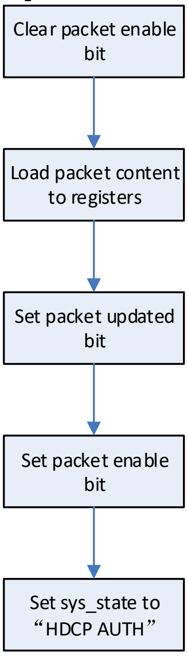

Fig. 23-23 Send Auxiliary Information Packets

23.6.3 GRF Setting for EDP TX

There are two eDP TX in this system. They both need to set GRF correctly.

eDP0:

```
<HDPTXPHY_GRF_CON0> [0]   = 1'b1 //PHY0
<VO1_GRF_VO1_CON0>[0]     = 1'b1
<VOP_GRF_VOP_CON2>[1:0]   = 2'b01
```

eDP1:

```
<HDPTXPHY_GRF_CON0> [0]   = 1'b1 //PHY1
<VO1_GRF_VO1_CON1>[0]     = 1'b1
<VOP_GRF_VOP_CON2>[4:3]   = 2'b01
```

If want to transfer S/PDIF or I2S, please set these registers.

<VO1_GRF_VO1_CON0>[3] = 1'b1 //eDP0 I2S
<VO1_GRF_VO1_CON0>[4] = 1'b1 //eDP0 S/PDIF
<VO1_GRF_VO1_CON1>[3] = 1'b1 //eDP1 I2S
<VO1_GRF_VO1_CON1>[4] = 1'b1 //eDP1 S/PDIF

Chapter 24 HDMI TX Controller

24.1 Overview

The HDMI TX Controller supports the following features:HDMI 2.1 Compliance

- Fixed Rate Link (FRL) stream
- Support for 4K@120 Hz and 8K@60 Hz video modes
- Extended Metadata Packets
- Variable Refresh Rate (VRR) including Quick Media Switching (QMS) which is also known as Cinema VRR)
- Fast Vactive (FVA), which is also known as Quick Frame Transport (QFT)
- Transmission of Compressed Video
- Reed-Solomon Forward Error Correction (RSFEC)
- SCDC I2C DDC access
- TMDS Scrambler to enable support for 2160 p@60 Hz with RGB/YCbCr 4:4:4
- YCbCr 4:2:0 support to enable 2160 p@60 Hz at lower HDMI link speeds
- Character Error Detection
- Multi-stream Audio Support (Multi-stream Audio Sample)
- Enhanced Audio Return Channel (EARC)

HDCP 1.4 Compliance

- According to HDMI 2.1 Specification, support for this HDCP encryption/decryption method is not available when operating in Fixed Rate Link mode
- For HDMI 2.0 and lower version specifications, HDCP 1.4 content protection engine is available

HDCP 2.3 Compliance

- External HDCP 2 interface is provided, which allows connecting HDCP 2 Embedded Security Module IP that can be licensed separately

Single-channel DVI 1.0 backward compatibility (dual-link DVI is not supported) All HDMI sources are compatible with all DVI-compliant sinks and all HDMI sinks are compatible with DVI-compliant sources. All HDMI devices are compatible to the DVI 1.0 Specification, except some rules. For more information on these rules, see the *HDMI 1.4b Specification*.
Supports the following video formats:

- RGB 4:4:4 8-bit normal color mode
- RGB 4:4:4 10-bit deep color mode
- YCBCR 4:4:4 8-bit normal color mode
- YCBCR 4:4:4 10-bit deep color mode
- YCBCR 4:2:0 8-bit normal color mode
- YCBCR 4:2:0 10-bit deep color mode
- Up to 4K x 2K video format (HDMI 1.4b)
- CEA-861-F video format (HDMI 2.0)
- CTA-861-G video format (HDMI 2.1)

Supports encoded audio data:

- L-PCM
- L-PCM multi-channel
- High Bit-Rate audio

Supports CEC function. CEC is a protocol that provides high-level control functions between all of the various audiovisual products in your environment. The CEC bus allows all products in the system to potentially discover and communicate with each other.
Support eARC function. The eARC TX uses the HPD and utility lines of the HDMI connector to receive audio samples from HDMI sink to HDMI source, along with bidirectional control data packets.
The supported audio formats include:

- L-PCM (up to 32 channels)

24.2 Block Diagram

HDMI TX CONTROLLER comprises with:

- MM: Main Module
- APB: APB Interface Module
- AVP: Audio Video Packet Module

- EARC: Enhanced Audio Return Channel Receiver (eARC Rx) Controller
- CEC Module: Consumer Electronics Control Module
- HDCP 2.x Encoder (External)
- IPI: Image Pixel Interface
- STI: SPDIF Tx Interface
- ITI: I2S Tx Interface
- SRI: S/PDIF Rx Interface
- IRI: I2S Rx Interface

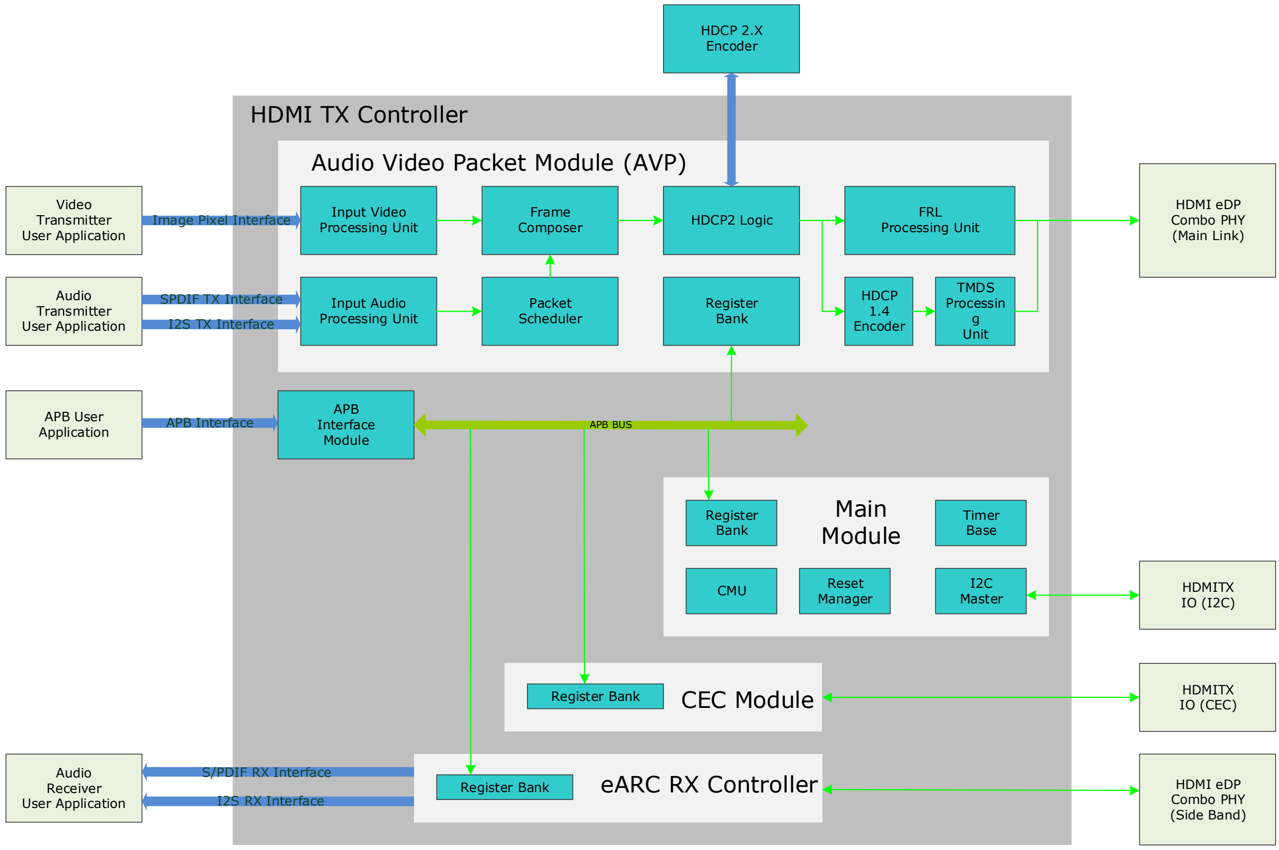

Fig. 24-1 HDMI TX Controller Block Diagram

24.3 Function Description

24.3.1 Main Module

This includes the following sub modules which can be common or completely independent of the remaining macro blocks.

- Reset Manager Module
- Timer Base Module
- Control Measurement Unit
- Status and Control Data Channel Module
- Display Data Channel
- I2C Master Module

24.3.1.1 Reset Manager Module

The Reset Manager module, generates all reset and initial signals required by the other functional modules; Synchronizes the resets to different clock domains; Guarantees that the resets from different clock domains to the same functional modules; Overlap when asserted the reset architecture of the HDMI TX Controller comprises of three types of clearing logic: the asynchronous reset, software initials, and software disables.

24.3.1.2 Timer Base Module

The Timer Base module generates timer bases for the reference counters of the different timers. The timer bases are calculated based on the timer_reference_base (frequency of the reference clock - refclk) field of the timer_base_config0 registers.

24.3.1.3 Control Measurement Unit

The Control Measurement Unit (CMU) measures the frequency and provides watchdog of imeasclk signal (frequency greater than 2 KHz). Frequency= ocfgr_clk_freq[19:0]/base time signal or evaluation period.

24.3.1.4 Status and Control Data Channel Module

The Status and Data Control Channel (SCDC) operates as a point-to-point communication protocol to exchange data between the HDMI Source and the HDMI Sink. It is an I2C-based system and makes use of the same I2C interface used for E-EDID (DDC) accesses and for HDCP (I2C Bus) accesses. This protocol extends the I2C standard by providing a mechanism for the Sink device (I2C Slave) to request a Source device (I2C Master) to initiate a status check read. The SCDC access is used for Read/Write operations into the SCDC registers for retrieving information about the actual status of the controller.

24.3.1.5 Display Data Channel

The Display Data Channel (DDC) reads E-EDID and SCDC structure to determine the capabilities and characteristics of the Sink. DDC implements the I2C Master for DDC/E-DDC channel in HDMI TX controller.

The DDC Controls all I2C transactions Interfaces with HDCP 1.4, HDCP 2.x, SCDC, and software The I2C Master complies with the *I2C Bus Specification, Version 2.1*.

24.3.1.6 I2C Master Module

The I2C Master module implements the I2C Master for E-DDC channel in HDMI TX Controller. It is responsible for all I2C transactions and it can interface with HDCP 1.4, HDCP 2.x, SCDC, and software (SW). The software interface allows reading the Sink's E-EDID based on system needs. The I2C Master complies with the *I2C Bus Specification 2.1*.

24.3.2 AMBA APB Interface Module

The APB Interface communicates between the AMBA 3 APB Slave Interface module and the HDMI TX Register Bank. The AMBA APB Interface module. Receives the APB Master's Read/Write operations and translates them into the internal Register Bank Access (RBK) protocol; Multiplexes the Register Bank access to the several domains based on the APB address; Synchronizes the Register Bank access protocol into/from the corresponding clock domain For more information, see *AMBA 3 APB Protocol*.

24.3.3 Audio Video Packets (AVP) Module

The Audio Video Packets (AVP) module packages the input audio, video, and packet information into a TMDS stream and prepares it for transmission in to the FRL or TMDS stream. This stream can be redirected for encryption to an external HDCP 2.x encoder. An HDCP 1.4 encoder is used internally for the TMDS stream. AVP module consists of the following modules: "Video Processing Unit","FRL Processing Unit","TDMS Processing Unit" ,"Audio Processing Unit".

24.3.3.1 Video Processing Unit

The Video Processing Unit receives the video stream from the user application side to transmit into the HDMI stream. The Video Processing Unit of the AVP module consists of the components shown in Figure 24 -2.

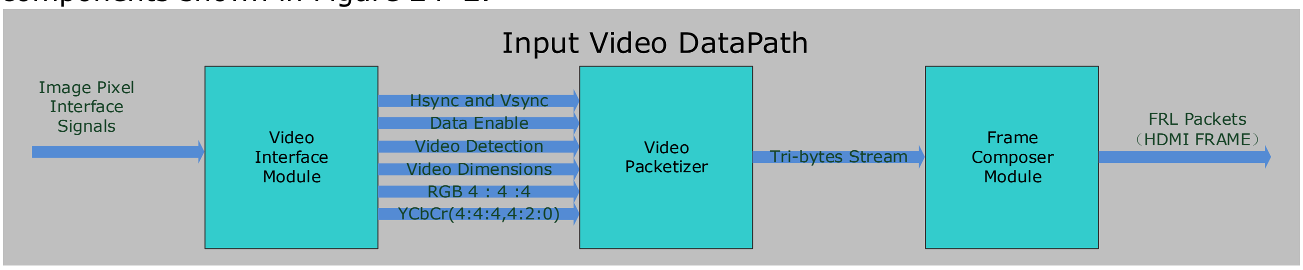

Fig. 24-2 Input Video Data Path

The Video Interface module detects and measures the video parameters and characteristics of the input video stream (IPI). The Video Interface module also samples the Image Pixel Interface (IPI) and maps the correspondent video data to the internal blocks. The measured video parameters are: Hfront, Hback, Hblank, Hactive, Htotal, Hsync Width, Vsync Width, Vback, Vblank, Vactive, Vtotal.

The measured video characteristics are Vsync polarity, Hsync polarity, Alternative video detection, Field detection, Progressive or Interlaced video detection.

24.3.3.2 FRL Processing Unit

The FRL Processing Unit of the AVP module consists of the components shown in Figure24-3.

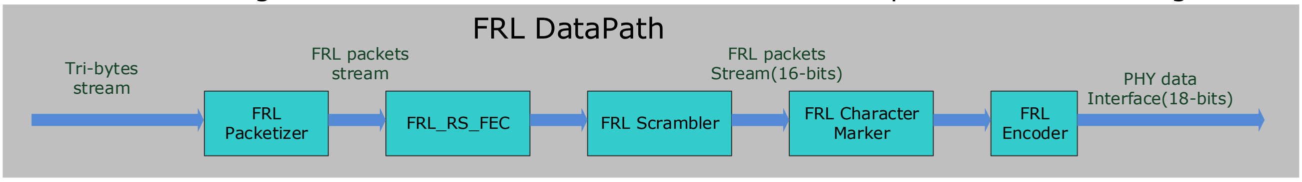

Fig. 24-3 FRL Data Path

24.3.3.3 TMDS Processing Unit

The TMDS Processing Unit processes the TMDS stream which includes audio, video, and auxiliary data stream. The TMDS Processing Unit of the AVP module consists of the components shown in Figure 24-4.

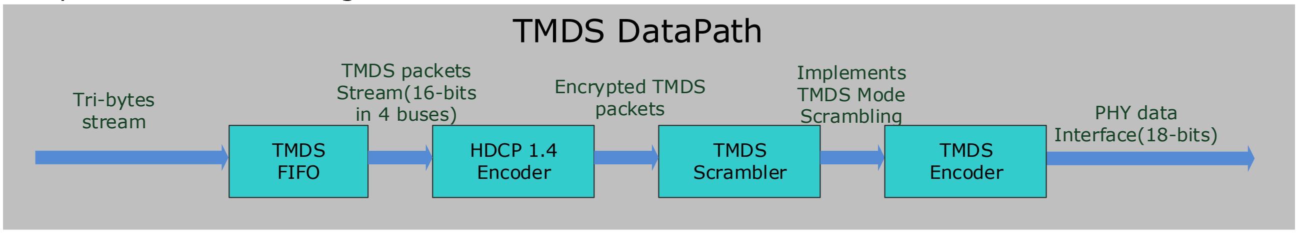

Fig. 24-4 TMDS Data Path

24.3.3.4 HDCP 1.4 Encoder

The HDCP 1.4 Encoder module receives the data from the TMDS Datapath from the four buses (a, b, c and d). This data includes the following: Video, Data Island, Control Period, HSYNC and VSYNC Indication, Data Enable This module encrypts the TMDS Stream. HDCP 1.4 uses an custom cipher for data encoding, a Finite State Machine to control the encryption operation and a dedicated access to the I2C Master present in the HDMI TX controller. For more information about the HDCP protocol, see the *HDCP 1.4 Specification*.

24.3.3.5 Audio Processing Unit

The Input Audio Processing Unit receives the audio data-Inter-IC Sound (I2S) Interface, and Sony/Philips Digital Interface (S/PDIF), from the application side to transmit into the HDMI stream. The Input Audio Processing Unit of the AVP module consists of the components shown in Figure 24-5.

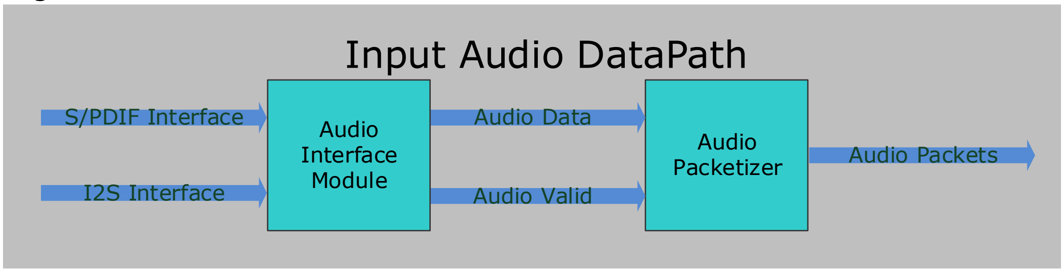

Fig. 24-5 Input Audio Data Path

24.3.3.6 Packet Scheduler

The Packet Scheduler schedules enabled packets and transfers it to the Frame Composer module. You can configure the priorities of the packets.

24.3.4 Enhanced Audio Return Channel Receiver (eARC Rx) Controller

The eARC Rx controller Uses the HPD and Utility lines to receive audio samples from the eARC Rx sink. Supports bi-directional communication of data packets. The data packets are read and written through the register bank. The following are the audio output selectable interfaces: Sony/Philips Digital Interface (S/PDIF) (up to 8 audio channels); Inter-IC Sound (I2S) (up to 8 audio channels)

24.3.5 Consumer Electronics Control Module

The Consumer Electronics Control (CEC) module Provides high-level control functions for all the various audio-visual products connected to the HDMI. Uses a single bidirectional line for transmission and reception of messages. The following terms are commonly used for CEC module: Message–The information (payload data) received by CEC application/software level. Frame–A frame is one burst of a data flow (including payload and overhead data) received by the CEC controller after triggered by the CEC software. The maximum size of a frame is 16 data blocks (including a header block). Data/Header block–One data/header block consists of 10-bits, in which 8-bits are payload data and 2-bits are overhead. There are two operation modes for a CEC module. Initiator mode–In this mode, the CEC module sends out messages and waits for a follower for feed-back. CEC module works in this mode when it sends a frame. After the transmission is complete, it reverts to the follower mode automatically. Follower mode–In this mode, the CEC module receives messages and sends appropriate acknowledgment to the initiator. The CEC module always works in the follower mode whenever it does not transmit any data. There can be more than one followers.

24.3.6 HDCP 2.x Encoder(External)

The HDCP 2.x Encoder encrypts the Tri-bytes stream using the HDCP 2.x encryption protocol. The HDCP 2.x specification includes a more powerful authentication protocol and a locality check that ensures the sink and source are close together. HDCP 2.x is not backward compatible with HDCP 1.4, so both protection systems co-exist in the HDMI TX controller. The controller provides support for HDCP 2.x, through external HDCP 2.x encoder. HDCP 2.x Encoder (HDCP2 ESM) can be automatically configured and integrated with the controller. The verification environment also supports this encryption engine.

24.3.7 Register Bank

The register bank comprises of 32-bit registers that can be seen from the software side, as read-only, write-only, read-write. The configuration shell module placed per clock domain and functional area reduces the number of synchronizations. Synchronization is done at the APB level instead at the bit field or signal levels. The Register Bank of the HDMI TX controller is divided into four regions that is placed within the functional domain, AVP, MAIN, CEC, eARC RX.

24.4 Register Description

24.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

24.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_CORE_ID	0x0000	W	0x48515458	IP Identification Register
HDMI TX Controller_VER_NUMBER	0x0004	W	0x30313030	IP Version Number Register
HDMI TX Controller_VER_TYPE	0x0008	W	0x6C753030	IP Version Type Register
HDMI TX Controller_CONFIG_REG	0x000C	W	0x11E0D501	IP Configuration Identification Register
HDMI TX Controller_CORE_TIMESTAMP_HHMM	0x0014	W	0x31373336	IP Timestamp HHMM Register
HDMI TX Controller_CORE_TIMESTAMP_MMDD	0x0018	W	0x30333131	IP Timestamp MMDD Register
HDMI TX Controller_CORE_TIMESTAMP_YYYY	0x001C	W	0x32303231	IP Timestamp YYYY Register
HDMI TX Controller_GLOBAL_SWRESET_REQUEST	0x0040	W	0x00000000	Main Controller Software Reset Register
HDMI TX Controller_GLOBAL_SWDISABLE	0x0044	W	0x00000000	Main Controller Synchronous Disable Register

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_RESET_MANAGER_CONFIG0	0x0048	W	0x00000000	Main Controller Software Configuration Register 0
HDMI TX Controller_RESET_MANAGER_STATUS0	0x0050	W	0x00000000	Main Controller Software Status Register 0
HDMI TX Controller_RESET_MANAGER_STATUS1	0x0054	W	0x00000000	Main Controller Software Status Register 1
HDMI TX Controller_RESET_MANAGER_STATUS2	0x0058	W	0x00000000	Main Controller Software Status Register 2
HDMI TX Controller_TIMER_BASE_CONFIG0	0x0080	W	0x198B7B25	Timer Base Configuration Register 0
HDMI TX Controller_TIMER_BASE_STATUS0	0x0084	W	0x00000000	Timer Base Status Register 0
HDMI TX Controller_I2CM_SM_SCL_CONFIG0	0x00E0	W	0x085E085E	I2C Master Standard-mode SCL configuration 0
HDMI TX Controller_I2CM_FM_SCL_CONFIG0	0x00E4	W	0x02170217	I2C Master Fast-mode SCL configuration 0
HDMI TX Controller_I2CM_CONFIG0	0x00E8	W	0x00000000	I2C Master configuration 0
HDMI TX Controller_I2CM_CONTROL0	0x00EC	W	0x00000000	I2C Master control 0
HDMI TX Controller_I2CM_STATUS0	0x00F0	W	0x00000000	I2C Master status 0
HDMI TX Controller_I2CM_INTERFACE_CONTROL0	0x00F4	W	0x00000000	I2C Master Interface SW access control 0
HDMI TX Controller_I2CM_INTERFACE_CONTROL1	0x00F8	W	0x00000000	I2C Master Interface SW access control 1
HDMI TX Controller_I2CM_INTERFACE_WRDATA_0_3	0x00FC	W	0x00000000	I2C Master Interface SW write data, byte 0 to 3
HDMI TX Controller_I2CM_INTERFACE_WRDATA_4_7	0x0100	W	0x00000000	I2C Master Interface SW write data, byte 4 to 7
HDMI TX Controller_I2CM_INTERFACE_WRDATA_8_11	0x0104	W	0x00000000	I2C Master Interface SW write data, byte 8 to 11
HDMI TX Controller_I2CM_INTERFACE_WRDATA_12_15	0x0108	W	0x00000000	I2C Master Interface SW write data, byte 12 to 15
HDMI TX Controller_I2CM_INTERFACE_RDDATA_0_3	0x010C	W	0x00000000	I2C Master Interface SW read data, byte 0 to 3

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_I2CM_INTERFACE_RDDATA_4_7	0x0110	W	0x00000000	I2C Master Interface SW read data, byte 4 to 7
HDMI TX Controller_I2CM_INTERFACE_RDDATA_8_11	0x0114	W	0x00000000	I2C Master Interface SW read data, byte 8 to 11
HDMI TX Controller_I2CM_INTERFACE_RDDATA_12_15	0x0118	W	0x00000000	I2C Master Interface SW read data, byte 12 to 15
HDMI TX Controller_SCDC_CONFIG0	0x0140	W	0x00000080	SCDC configuration 0
HDMI TX Controller_SCDC_CONTROL0	0x0148	W	0x00000000	SCDC control 0
HDMI TX Controller_SCDC_STATUS0	0x0150	W	0x00000000	SCDC status 0
HDMI TX Controller_FLT_CONFIG0	0x0160	W	0x00000000	FRL Link Training configuration 0
HDMI TX Controller_FLT_CONFIG1	0x0164	W	0x00000000	FRL Link Training configuration 1
HDMI TX Controller_FLT_CONFIG2	0x0168	W	0x00000000	FRL Link Training configuration 2
HDMI TX Controller_FLT_CONTROL0	0x0170	W	0x00000000	FRL Link Training control 0
HDMI TX Controller_MAINUNIT_STATUS0	0x0180	W	0x00000000	Main Unit Status Register 0
HDMI TX Controller_VIDEO_INTERFACE_CONFIG0	0x0800	W	0x00000000	Video Interface configuration Register 0
HDMI TX Controller_VIDEO_INTERFACE_CONFIG2	0x0808	W	0x00000000	Video Interface configuration Register 2
HDMI TX Controller_VIDEO_INTERFACE_CONTROL0	0x080C	W	0x00000000	Video Interface control Register 0
HDMI TX Controller_VIDEO_INTERFACE_STATUS0	0x0814	W	0x00000000	Video Interface status Register 0
HDMI TX Controller_VIDEO_PACKING_CONFIG0	0x081C	W	0x00000000	Video Packing configuration Register 0
HDMI TX Controller_AUDIO_INTERFACE_CONFIG0	0x0820	W	0x00000000	Audio Interface configuration Register 0
HDMI TX Controller_AUDIO_INTERFACE_CONFIG1	0x0824	W	0x00000000	Audio Interface configuration Register 1
HDMI TX Controller_AUDIO_INTERFACE_CONTROL0	0x082C	W	0x00000000	Audio Interface control Register 0

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDIO_INTERFACE_STATUS0	0x0834	W	0x00000000	Audio Interface status Register 0
HDMI TX Controller_FRAME_COMPOSER_CONFIG0	0x0840	W	0x42000000	Frame Composer configuration Register 0
HDMI TX Controller_FRAME_COMPOSER_CONFIG1	0x0844	W	0xFFF0FF00	Frame Composer configuration Register 1
HDMI TX Controller_FRAME_COMPOSER_CONFIG2	0x0848	W	0x00000000	Frame Composer configuration Register 2
HDMI TX Controller_FRAME_COMPOSER_CONFIG3	0x084C	W	0x00000000	Frame Composer configuration Register 3
HDMI TX Controller_FRAME_COMPOSER_CONFIG4	0x0850	W	0x00000000	Frame Composer configuration Register 4
HDMI TX Controller_FRAME_COMPOSER_CONFIG5	0x0854	W	0x00000000	Frame Composer configuration Register 5
HDMI TX Controller_FRAME_COMPOSER_CONFIG6	0x0858	W	0x00000000	Frame Composer configuration Register 6
HDMI TX Controller_FRAME_COMPOSER_CONFIG7	0x085C	W	0x00000000	Frame Composer configuration Register 7
HDMI TX Controller_FRAME_COMPOSER_CONFIG8	0x0860	W	0x00010000	Frame Composer configuration Register 8
HDMI TX Controller_FRAME_COMPOSER_CONFIG9	0x0864	W	0x00000100	Frame Composer configuration Register 9
HDMI TX Controller_FRAME_COMPOSER_CONTROL0	0x086C	W	0x00000000	Frame Composer control Register 0
HDMI TX Controller_VIDEO_MONITOR_CONFIG0	0x0880	W	0x00000000	Video Monitor configuration Register 0
HDMI TX Controller_VIDEO_MONITOR_STATUS0	0x0884	W	0x00000000	Video Monitor status Register 0
HDMI TX Controller_VIDEO_MONITOR_STATUS1	0x0888	W	0x00000000	Video Monitor status Register 1
HDMI TX Controller_VIDEO_MONITOR_STATUS2	0x088C	W	0x00000000	Video Monitor status Register 2
HDMI TX Controller_VIDEO_MONITOR_STATUS3	0x0890	W	0x00000000	Video Monitor status Register 3
HDMI TX Controller_VIDEO_MONITOR_STATUS4	0x0894	W	0x00000000	Video Monitor status Register 4

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_VIDEO_MONITOR_STATUS5	0x0898	W	0x00000000	Video Monitor status Register 5
HDMI TX Controller_VIDEO_MONITOR_STATUS6	0x089C	W	0x00000000	Video Monitor status Register 6
HDMI TX Controller_HDCP2LOGIC_CONFIG0	0x08E0	W	0x00000000	HDCP 2 Logic Configuration Register 0
HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_IN	0x08E4	W	0x00000000	HDCP 2 Logic GPIO Inputs
HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_OUT	0x08E8	W	0x00000000	HDCP 2 Logic GPIO Outputs
HDMI TX Controller_HDCP14_CONFIG0	0x0900	W	0x00010000	HDCP 1.4 Configuration Register 0
HDMI TX Controller_HDCP14_CONTROL0	0x0904	W	0x00000000	HDCP 1.4 Configuration Register 1
HDMI TX Controller_HDCP14_CONFIG1	0x0908	W	0x00000000	HDCP 1.4 Configuration Register 2
HDMI TX Controller_HDCP14_CONFIG2	0x090C	W	0x00000000	HDCP 1.4 Configuration Register 3
HDMI TX Controller_HDCP14_KEY_SEED	0x0914	W	0x00000000	HDCP 1.4 Key Decryption Seed Register
HDMI TX Controller_HDCP14_KEY_H	0x0918	W	0x00000000	HDCP 1.4 Key High Configuration Register
HDMI TX Controller_HDCP14_KEY_L	0x091C	W	0x00000000	HDCP 1.4 Key Low Configuration Register
HDMI TX Controller_HDCP14_KEY_STATUS	0x0920	W	0x00000000	HDCP 1.4 Key Status Register
HDMI TX Controller_HDCP14_AKSV_H	0x0924	W	0x00000000	HDCP 1.4 AKSV High Configuration Register
HDMI TX Controller_HDCP14_AKSV_L	0x0928	W	0x00000000	HDCP 1.4 AKSV Low Configuration Register
HDMI TX Controller_HDCP14_AN_H	0x092C	W	0x00000000	HDCP 1.4 An High Configuration Register
HDMI TX Controller_HDCP14_AN_L	0x0930	W	0x00000000	HDCP 1.4 An Low Configuration Register
HDMI TX Controller_HDCP14_STATUS0	0x0934	W	0x00000000	HDCP 1.4 Status Register 0

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_HDCP14_STATUS1	0x0938	W	0x00000000	HDCP 1.4 Status Register 1
HDMI TX Controller_SCRAMB_CONFIG0	0x0960	W	0x00000000	Scrambler config register 0
HDMI TX Controller_LINK_CONFIG0	0x0968	W	0x00000010	Link config register 0
HDMI TX Controller_TMDS_FIFO_CONFIG0	0x0970	W	0x00000001	TMDS FIFO Configuration Register 0
HDMI TX Controller_TMDS_FIFO_CONTROL0	0x0974	W	0x00000000	TMDS FIFO Control Register 0
HDMI TX Controller_FRL_RSFEC_CONFIG0	0x0A20	W	0x00000000	FRL Reed-Solomon FEC Configuration Register 0
HDMI TX Controller_FRL_RSFEC_STATUS0	0x0A30	W	0x00000000	FRL Reed-Solomon FEC Status Register 0
HDMI TX Controller_FRL_PKTZ_CONFIG0	0x0A40	W	0x00000000	FRL Packetizer Configuration Register 0
HDMI TX Controller_FRL_PKTZ_CONTROL0	0x0A44	W	0x00000000	FRL Packetizer Control Register 0
HDMI TX Controller_FRL_PKTZ_CONTROL1	0x0A50	W	0x00000000	FRL Packetizer Control Register 1
HDMI TX Controller_FRL_PKTZ_STATUS1	0x0A54	W	0x00000000	FRL Packetizer Status Register 1
HDMI TX Controller_PKTSCHED_CONFIG0	0x0A80	W	0x00000006	Packet Scheduler Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE0_CONFIG0	0x0A84	W	0x00030201	Packet Scheduler Priority Queue 0 Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE1_CONFIG0	0x0A88	W	0x09070D08	Packet Scheduler Priority Queue 1 Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG0	0x0A8C	W	0x06050C04	Packet Scheduler Priority Queue 2 Configuration Register 0
HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG1	0x0A90	W	0x0E0F0B0A	Packet Scheduler Priority Queue 2 Configuration Register 1
HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG2	0x0A94	W	0x00001110	Packet Scheduler Priority Queue 2 Configuration Register 2
HDMI TX Controller_PKTSCHED_PKT_CONFIG0	0x0A98	W	0x00764807	Packet Scheduler - Packet Configuration Register 0

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKTSCHED_PKT_CONFIG1	0x0A9C	W	0x00007F00	Packet Scheduler - Packet Configuration Register 1
HDMI TX Controller_PKTSCHED_PKT_CONFIG2	0x0AA0	W	0x11001000	Packet Scheduler - Packet Configuration Register 2
HDMI TX Controller_PKTSCHED_PKT_CONFIG3	0x0AA4	W	0x00000000	Packet Scheduler - Packet Configuration Register 3
HDMI TX Controller_PKTSCHED_PKT_EN	0x0AA8	W	0x00000000	Packet Scheduler - Packet Enable Control Register
HDMI TX Controller_PKTSCHED_PKT_CONTROL0	0x0AAC	W	0x00000000	Packet Scheduler - Packet Control Register 0
HDMI TX Controller_PKTSCHED_PKT_SEND	0x0AB0	W	0x00000000	Packet Scheduler - Packet Send Request
HDMI TX Controller_PKTSCHED_PKT_STATUS0	0x0AB4	W	0x00000000	Packet Scheduler - Status Register 0
HDMI TX Controller_PKTSCHED_PKT_STATUS1	0x0AB8	W	0x00000000	Packet Scheduler - Status Register 1
HDMI TX Controller_PKT_NULL_CONTENTS0	0x0B00	W	0x00000000	NULL - Null - Packet contents register 0
HDMI TX Controller_PKT_NULL_CONTENTS1	0x0B04	W	0x00000000	NULL - Null - Packet contents register 1
HDMI TX Controller_PKT_NULL_CONTENTS2	0x0B08	W	0x00000000	NULL - Null - Packet contents register 2
HDMI TX Controller_PKT_NULL_CONTENTS3	0x0B0C	W	0x00000000	NULL - Null - Packet contents register 3
HDMI TX Controller_PKT_NULL_CONTENTS4	0x0B10	W	0x00000000	NULL - Null - Packet contents register 4
HDMI TX Controller_PKT_NULL_CONTENTS5	0x0B14	W	0x00000000	NULL - Null - Packet contents register 5
HDMI TX Controller_PKT_NULL_CONTENTS6	0x0B18	W	0x00000000	NULL - Null - Packet contents register 6
HDMI TX Controller_PKT_NULL_CONTENTS7	0x0B1C	W	0x00000000	NULL - Null - Packet contents register 7
HDMI TX Controller_PKT_ACP_CONTENTS0	0x0B20	W	0x00000000	ACP - Audio Content Protection - Packet contents register 0
HDMI TX Controller_PKT_ACP_CONTENTS1	0x0B24	W	0x00000000	ACP - Audio Content Protection - Packet contents register 1

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_ACP_CONTENTS2	0x0B28	W	0x00000000	ACP - Audio Content Protection - Packet contents register 2
HDMI TX Controller_PKT_ACP_CONTENTS3	0x0B2C	W	0x00000000	ACP - Audio Content Protection - Packet contents register 3
HDMI TX Controller_PKT_ACP_CONTENTS4	0x0B30	W	0x00000000	ACP - Audio Content Protection - Packet contents register 4
HDMI TX Controller_PKT_ACP_CONTENTS5	0x0B34	W	0x00000000	ACP - Audio Content Protection - Packet contents register 5
HDMI TX Controller_PKT_ACP_CONTENTS6	0x0B38	W	0x00000000	ACP - Audio Content Protection - Packet contents register 6
HDMI TX Controller_PKT_ACP_CONTENTS7	0x0B3C	W	0x00000000	ACP - Audio Content Protection - Packet contents register 7
HDMI TX Controller_PKT_ISRC1_CONTENTS0	0x0B40	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 0
HDMI TX Controller_PKT_ISRC1_CONTENTS1	0x0B44	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 1
HDMI TX Controller_PKT_ISRC1_CONTENTS2	0x0B48	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 2
HDMI TX Controller_PKT_ISRC1_CONTENTS3	0x0B4C	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 3
HDMI TX Controller_PKT_ISRC1_CONTENTS4	0x0B50	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 4
HDMI TX Controller_PKT_ISRC1_CONTENTS5	0x0B54	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 5
HDMI TX Controller_PKT_ISRC1_CONTENTS6	0x0B58	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 6
HDMI TX Controller_PKT_ISRC1_CONTENTS7	0x0B5C	W	0x00000000	ISRC1 - Intl Std Recording Code 1 - Packet contents register 7
HDMI TX Controller_PKT_ISRC2_CONTENTS0	0x0B60	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 0
HDMI TX Controller_PKT_ISRC2_CONTENTS1	0x0B64	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 1
HDMI TX Controller_PKT_ISRC2_CONTENTS2	0x0B68	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 2
HDMI TX Controller_PKT_ISRC2_CONTENTS3	0x0B6C	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 3

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_ISRC2_CONTENTS4	0x0B70	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 4
HDMI TX Controller_PKT_ISRC2_CONTENTS5	0x0B74	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 5
HDMI TX Controller_PKT_ISRC2_CONTENTS6	0x0B78	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 6
HDMI TX Controller_PKT_ISRC2_CONTENTS7	0x0B7C	W	0x00000000	ISRC2 - Intl Std Recording Code 2 - Packet contents register 7
HDMI TX Controller_PKT_GMD_CONTENTS0	0x0B80	W	0x00000000	GMD - Gamut Metadata - Packet contents register 0
HDMI TX Controller_PKT_GMD_CONTENTS1	0x0B84	W	0x00000000	GMD - Gamut Metadata - Packet contents register 1
HDMI TX Controller_PKT_GMD_CONTENTS2	0x0B88	W	0x00000000	GMD - Gamut Metadata - Packet contents register 2
HDMI TX Controller_PKT_GMD_CONTENTS3	0x0B8C	W	0x00000000	GMD - Gamut Metadata - Packet contents register 3
HDMI TX Controller_PKT_GMD_CONTENTS4	0x0B90	W	0x00000000	GMD - Gamut Metadata - Packet contents register 4
HDMI TX Controller_PKT_GMD_CONTENTS5	0x0B94	W	0x00000000	GMD - Gamut Metadata - Packet contents register 5
HDMI TX Controller_PKT_GMD_CONTENTS6	0x0B98	W	0x00000000	GMD - Gamut Metadata - Packet contents register 6
HDMI TX Controller_PKT_GMD_CONTENTS7	0x0B9C	W	0x00000000	GMD - Gamut Metadata - Packet contents register 7
HDMI TX Controller_PKT_AMD_CONTENTS0	0x0BA0	W	0x00000000	AMD - Audio Metadata - Packet contents register 0
HDMI TX Controller_PKT_AMD_CONTENTS1	0x0BA4	W	0x00000000	AMD - Audio Metadata - Packet contents register 1
HDMI TX Controller_PKT_AMD_CONTENTS2	0x0BA8	W	0x00000000	AMD - Audio Metadata - Packet contents register 2
HDMI TX Controller_PKT_AMD_CONTENTS3	0x0BAC	W	0x00000000	AMD - Audio Metadata - Packet contents register 3
HDMI TX Controller_PKT_AMD_CONTENTS4	0x0BB0	W	0x00000000	AMD - Audio Metadata - Packet contents register 4
HDMI TX Controller_PKT_AMD_CONTENTS5	0x0BB4	W	0x00000000	AMD - Audio Metadata - Packet contents register 5

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_AMD_CONTENTS6	0x0BB8	W	0x00000000	AMD - Audio Metadata - Packet contents register 6
HDMI TX Controller_PKT_AMD_CONTENTS7	0x0BBC	W	0x00000000	AMD - Audio Metadata - Packet contents register 7
HDMI TX Controller_PKT_VSI_CONTENTS0	0x0BC0	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_VSI_CONTENTS1	0x0BC4	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_VSI_CONTENTS2	0x0BC8	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_VSI_CONTENTS3	0x0BCC	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_VSI_CONTENTS4	0x0BD0	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_VSI_CONTENTS5	0x0BD4	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_VSI_CONTENTS6	0x0BD8	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_VSI_CONTENTS7	0x0BDC	W	0x00000000	VSI - Vendor Specific InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_AVI_CONTENTS0	0x0BE0	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_AVI_CONTENTS1	0x0BE4	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_AVI_CONTENTS2	0x0BE8	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_AVI_CONTENTS3	0x0BEC	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_AVI_CONTENTS4	0x0BF0	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_AVI_CONTENTS5	0x0BF4	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_AVI_CONTENTS6	0x0BF8	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_AVI_CONTENTS7	0x0BFC	W	0x00000000	AVI - Auxiliary Video InfoFrame - Packet contents register 7

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_SPDI_CONTENTS0	0x0C00	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_SPDI_CONTENTS1	0x0C04	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_SPDI_CONTENTS2	0x0C08	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_SPDI_CONTENTS3	0x0C0C	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_SPDI_CONTENTS4	0x0C10	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_SPDI_CONTENTS5	0x0C14	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_SPDI_CONTENTS6	0x0C18	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_SPDI_CONTENTS7	0x0C1C	W	0x00000000	SPDI - Source Product Descriptor InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_AUDI_CONTENTS0	0x0C20	W	0x000A0100	AUDI - Audio InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_AUDI_CONTENTS1	0x0C24	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_AUDI_CONTENTS2	0x0C28	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_AUDI_CONTENTS3	0x0C2C	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_AUDI_CONTENTS4	0x0C30	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_AUDI_CONTENTS5	0x0C34	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_AUDI_CONTENTS6	0x0C38	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_AUDI_CONTENTS7	0x0C3C	W	0x00000000	AUDI - Audio InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_NVI_CONTENTS0	0x0C40	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_NVI_CONTENTS1	0x0C44	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 1

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_NVI_CONTENTS2	0x0C48	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_NVI_CONTENTS3	0x0C4C	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_NVI_CONTENTS4	0x0C50	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_NVI_CONTENTS5	0x0C54	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_NVI_CONTENTS6	0x0C58	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_NVI_CONTENTS7	0x0C5C	W	0x00000000	NVI - NTSC VBI InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_DRMI_CONTENTS0	0x0C60	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 0
HDMI TX Controller_PKT_DRMI_CONTENTS1	0x0C64	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 1
HDMI TX Controller_PKT_DRMI_CONTENTS2	0x0C68	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 2
HDMI TX Controller_PKT_DRMI_CONTENTS3	0x0C6C	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 3
HDMI TX Controller_PKT_DRMI_CONTENTS4	0x0C70	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 4
HDMI TX Controller_PKT_DRMI_CONTENTS5	0x0C74	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 5
HDMI TX Controller_PKT_DRMI_CONTENTS6	0x0C78	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 6
HDMI TX Controller_PKT_DRMI_CONTENTS7	0x0C7C	W	0x00000000	DRMI - Dynamic Range and Mastering InfoFrame - Packet contents register 7
HDMI TX Controller_PKT_GHDMI1_CONTENTS0	0x0C80	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 0
HDMI TX Controller_PKT_GHDMI1_CONTENTS1	0x0C84	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 1
HDMI TX Controller_PKT_GHDMI1_CONTENTS2	0x0C88	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 2
HDMI TX Controller_PKT_GHDMI1_CONTENTS3	0x0C8C	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 3

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_GHDMI1_CONTENTS4	0x0C90	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 4
HDMI TX Controller_PKT_GHDMI1_CONTENTS5	0x0C94	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 5
HDMI TX Controller_PKT_GHDMI1_CONTENTS6	0x0C98	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 6
HDMI TX Controller_PKT_GHDMI1_CONTENTS7	0x0C9C	W	0x00000000	GHDMI1 - Generic HDMI 1 - Packet contents register 7
HDMI TX Controller_PKT_GHDMI2_CONTENTS0	0x0CA0	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 0
HDMI TX Controller_PKT_GHDMI2_CONTENTS1	0x0CA4	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 1
HDMI TX Controller_PKT_GHDMI2_CONTENTS2	0x0CA8	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 2
HDMI TX Controller_PKT_GHDMI2_CONTENTS3	0x0CAC	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 3
HDMI TX Controller_PKT_GHDMI2_CONTENTS4	0x0CB0	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 4
HDMI TX Controller_PKT_GHDMI2_CONTENTS5	0x0CB4	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 5
HDMI TX Controller_PKT_GHDMI2_CONTENTS6	0x0CB8	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 6
HDMI TX Controller_PKT_GHDMI2_CONTENTS7	0x0CBC	W	0x00000000	GHDMI2 - Generic HDMI 2 - Packet contents register 7
HDMI TX Controller_PKT_EMP_CONFIG0	0x0CE0	W	0x00000000	EMP Packetizer Config Register 0
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS0	0x0D00	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 0
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS1	0x0D04	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 1
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS2	0x0D08	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 2
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS3	0x0D0C	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 3
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS4	0x0D10	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 4

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS5	0x0D14	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 5
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS6	0x0D18	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 6
HDMI TX Controller_PKT_EMP_VTEM_CONTENTS7	0x0D1C	W	0x00000000	VTEM - Video Timing Extended Metadata - Packet contents register 7
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS0	0x0D20	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 0
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS1	0x0D24	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 1
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS2	0x0D28	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 2
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS3	0x0D2C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 3
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS4	0x0D30	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 4
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS5	0x0D34	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 5
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS6	0x0D38	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 6
HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS7	0x0D3C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 0 contents register 7
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS0	0x0D40	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 0
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS1	0x0D44	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 1
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS2	0x0D48	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 2
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS3	0x0D4C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 3
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS4	0x0D50	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 4
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS5	0x0D54	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 5
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS6	0x0D58	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 6

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS7	0x0D5C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 1 contents register 7
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS0	0x0D60	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 0
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS1	0x0D64	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 1
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS2	0x0D68	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 2
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS3	0x0D6C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 3
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS4	0x0D70	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 4
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS5	0x0D74	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 5
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS6	0x0D78	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 6
HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS7	0x0D7C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 2 contents register 7
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS0	0x0D80	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 0
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS1	0x0D84	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 1
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS2	0x0D88	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 2
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS3	0x0D8C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 3
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS4	0x0D90	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 4
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS5	0x0D94	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 5
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS6	0x0D98	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 6
HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS7	0x0D9C	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 3 contents register 7
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS0	0x0DA0	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 0

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS1	0x0DA4	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 1
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS2	0x0DA8	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 2
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS3	0x0DAC	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 3
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS4	0x0DB0	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 4
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS5	0x0DB4	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 5
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS6	0x0DB8	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 6
HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS7	0x0DBC	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 4 contents register 7
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS0	0x0DC0	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 0
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS1	0x0DC4	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 1
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS2	0x0DC8	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 2
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS3	0x0DCC	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 3
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS4	0x0DD0	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 4
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS5	0x0DD4	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 5
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS6	0x0DD8	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 6
HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS7	0x0DDC	W	0x00000000	CVTEM - Compressed Video Timing Extended Metadata - Packet 5 contents register 7
HDMI TX Controller_AUDPKT_CONTROL0	0x0E20	W	0x00000000	Audio Packetizer Control Register 0
HDMI TX Controller_AUDPKT_CONTROL1	0x0E24	W	0x00000000	Audio Packetizer Control Register 1
HDMI TX Controller_AUDPKT_ACR_CONTROL0	0x0E40	W	0x00000000	Audio Packetizer ACR Control Register 0

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDPKT_ACR_CONTROL1	0x0E44	W	0x00000000	Audio Packetizer ACR Control Register 1
HDMI TX Controller_AUDPKT_ACR_STATUS0	0x0E4C	W	0x00000000	Audio Packetizer ACR Status Register 0
HDMI TX Controller_AUDPKT_CHSTATUS_OVR0	0x0E60	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 0
HDMI TX Controller_AUDPKT_CHSTATUS_OVR1	0x0E64	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 1
HDMI TX Controller_AUDPKT_CHSTATUS_OVR2	0x0E68	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 2
HDMI TX Controller_AUDPKT_CHSTATUS_OVR3	0x0E6C	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 3
HDMI TX Controller_AUDPKT_CHSTATUS_OVR4	0x0E70	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 4
HDMI TX Controller_AUDPKT_CHSTATUS_OVR5	0x0E74	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 5
HDMI TX Controller_AUDPKT_CHSTATUS_OVR6	0x0E78	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 6
HDMI TX Controller_AUDPKT_CHSTATUS_OVR7	0x0E7C	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 7
HDMI TX Controller_AUDPKT_CHSTATUS_OVR8	0x0E80	W	0x00000000	Audio Packetizer - Channel Status OverrideRegister 8
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC0	0x0EA0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 0
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC1	0x0EA4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 1
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC2	0x0EA8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 2
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC3	0x0EAC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 3
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC4	0x0EB0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 4

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC5	0x0EB4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 5
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC6	0x0EB8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 6
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC7	0x0EBC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 7
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC8	0x0EC0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 8
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC9	0x0EC4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 9
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC10	0x0EC8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 10
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC11	0x0ECC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 11
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC12	0x0ED0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 12
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC13	0x0ED4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 13
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC14	0x0ED8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 14
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC15	0x0EDC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 15
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC16	0x0EE0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 16
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC17	0x0EE4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 17

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC18	0x0EE8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 18
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC19	0x0EEC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 19
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC20	0x0EF0	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 20
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC21	0x0EF4	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 21
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC22	0x0EF8	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 22
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC23	0x0EFC	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 23
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC24	0x0F00	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 24
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC25	0x0F04	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 25
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC26	0x0F08	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 26
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC27	0x0F0C	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 27
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC28	0x0F10	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 28
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC29	0x0F14	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 29
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC30	0x0F18	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 30

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC31	0x0F1C	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 31
HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC32	0x0F20	W	0x00000000	Audio Packetizer - User Data Override Generic Message Payload Register 32
HDMI TX Controller_AUDPKT_VBIT_OVR0	0x0F24	W	0x00000000	Audio Packetizer - Validity Bit Override Register 0
HDMI TX Controller_CEC_TX_CONTROL	0x1000	W	0x00000000	CEC Transmit Control Register
HDMI TX Controller_CEC_STATUS	0x1004	W	0x00000000	CEC Status Register
HDMI TX Controller_CEC_CONFIG	0x1008	W	0x00000110	CEC Configuration Register
HDMI TX Controller_CEC_ADDR	0x100C	W	0x00000000	CEC Logical Address Register
HDMI TX Controller_CEC_TX_COUNT	0x1020	W	0x00000000	CEC Transmitter Buffer Counter Register
HDMI TX Controller_CEC_TX_DATA3_0	0x1024	W	0x00000000	CEC Byte 0-3 Transmitter Data Buffer Register
HDMI TX Controller_CEC_TX_DATA7_4	0x1028	W	0x00000000	CEC Byte 4-7 Transmitter Data Buffer Register
HDMI TX Controller_CEC_TX_DATA11_8	0x102C	W	0x00000000	CEC Byte 8-11 Transmitter Data Buffer Register
HDMI TX Controller_CEC_TX_DATA15_12	0x1030	W	0x00000000	CEC Byte 12-15 Transmitter Data Buffer Register
HDMI TX Controller_CEC_RX_COUNT_STATUS	0x1040	W	0x00000000	CEC Receiver Buffer Counter and Lock Status Register
HDMI TX Controller_CEC_RX_DATA3_0	0x1044	W	0x00000000	CEC Byte 0-3 Receiver Data Buffer Register
HDMI TX Controller_CEC_RX_DATA7_4	0x1048	W	0x00000000	CEC Byte 4-7 Receiver Data Buffer Register
HDMI TX Controller_CEC_RX_DATA11_8	0x104C	W	0x00000000	CEC Byte 8-11 Receiver Data Buffer Register
HDMI TX Controller_CEC_RX_DATA15_12	0x1050	W	0x00000000	CEC Byte 12-15 Receiver Data Buffer Register
HDMI TX Controller_CEC_LOCK_CONTROL	0x1054	W	0x00000000	CEC Lock Control Register

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_CEC_RXQUAL_BITTIME_CONFIG	0x1060	W	0x00033333	CEC RX Bit Qualifier Timings
HDMI TX Controller_CEC_RX_BITTIME_CONFIG	0x1064	W	0x00333333	CEC RX Bit Qualifier Timings
HDMI TX Controller_CEC_TX_BITTIME_CONFIG	0x1068	W	0x63444444	CEC TX Bit Qualifier Timings
HDMI TX Controller_EARCRX_CMDC_CONFIG0	0x1800	W	0x07040004	eARC RX - CMDC Configuration Register 0
HDMI TX Controller_EARCRX_CMDC_CONFIG1	0x1804	W	0x00D1D074	eARC RX - CMDC Configuration Register 1
HDMI TX Controller_EARCRX_CMDC_CONTROL	0x1808	W	0x00000010	eARC RX - CMDC Control Register
HDMI TX Controller_EARCRX_CMDC_WHITELIST0_CONFIG	0x180C	W	0xD27400A0	eARC RX - CMDC Transaction Device ID and Offset Whitelist Configuration Register - Part 0
HDMI TX Controller_EARCRX_CMDC_WHITELIST1_CONFIG	0x1810	W	0x0000D374	eARC RX - CMDC Transaction Device ID and Offset Whitelist Configuration Register - Part 1
HDMI TX Controller_EARCRX_CMDC_WHITELIST2_CONFIG	0x1814	W	0x00000000	eARC RX - CMDC Transaction Device ID and Offset Whitelist Configuration Register - Part 2
HDMI TX Controller_EARCRX_CMDC_WHITELIST3_CONFIG	0x1818	W	0x00000000	eARC RX - CMDC Transaction Device ID and Offset Whitelist Configuration Register - Part 3
HDMI TX Controller_EARCRX_CMDC_STATUS	0x181C	W	0x00000000	eARC RX - CMDC Status Register
HDMI TX Controller_EARCRX_CMDC_XACT_INFO	0x1820	W	0x00000000	eARC RX - CMDC Received Transaction Information Register
HDMI TX Controller_EARCRX_CMDC_XACT_ACTION	0x1824	W	0x00000000	eARC RX - CMDC Transaction Action Register
HDMI TX Controller_EARCRX_CMDC_HEARTBEAT_RXSTAT_SET	0x1828	W	0x00000000	eARC RX - CMDC Heartbeat RXSTAT Register
HDMI TX Controller_EARCRX_CMDC_HEARTBEAT_STATUS	0x182C	W	0x00000000	eARC RX - CMDC Heartbeat Status Register
HDMI TX Controller_EARCRX_CMDC_XACT_WR0	0x1840	W	0x00000000	eARC RX - CMDC Write Transaction Register 0
HDMI TX Controller_EARCRX_CMDC_XACT_WR1	0x1844	W	0x00000000	eARC RX - CMDC Write Transaction Register 1

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_WR2	0x1848	W	0x00000000	eARC RX - CMDC Write Transaction Register 2
HDMI TX Controller_EARCRX_CMDC_XACT_WR3	0x184C	W	0x00000000	eARC RX - CMDC Write Transaction Register 3
HDMI TX Controller_EARCRX_CMDC_XACT_WR4	0x1850	W	0x00000000	eARC RX - CMDC Write Transaction Register 4
HDMI TX Controller_EARCRX_CMDC_XACT_WR5	0x1854	W	0x00000000	eARC RX - CMDC Write Transaction Register 5
HDMI TX Controller_EARCRX_CMDC_XACT_WR6	0x1858	W	0x00000000	eARC RX - CMDC Write Transaction Register 6
HDMI TX Controller_EARCRX_CMDC_XACT_WR7	0x185C	W	0x00000000	eARC RX - CMDC Write Transaction Register 7
HDMI TX Controller_EARCRX_CMDC_XACT_WR8	0x1860	W	0x00000000	eARC RX - CMDC Write Transaction Register 8
HDMI TX Controller_EARCRX_CMDC_XACT_WR9	0x1864	W	0x00000000	eARC RX - CMDC Write Transaction Register 9
HDMI TX Controller_EARCRX_CMDC_XACT_WR10	0x1868	W	0x00000000	eARC RX - CMDC Write Transaction Register 10
HDMI TX Controller_EARCRX_CMDC_XACT_WR11	0x186C	W	0x00000000	eARC RX - CMDC Write Transaction Register 11
HDMI TX Controller_EARCRX_CMDC_XACT_WR12	0x1870	W	0x00000000	eARC RX - CMDC Write Transaction Register 12
HDMI TX Controller_EARCRX_CMDC_XACT_WR13	0x1874	W	0x00000000	eARC RX - CMDC Write Transaction Register 13
HDMI TX Controller_EARCRX_CMDC_XACT_WR14	0x1878	W	0x00000000	eARC RX - CMDC Write Transaction Register 14
HDMI TX Controller_EARCRX_CMDC_XACT_WR15	0x187C	W	0x00000000	eARC RX - CMDC Write Transaction Register 15
HDMI TX Controller_EARCRX_CMDC_XACT_WR16	0x1880	W	0x00000000	eARC RX - CMDC Write Transaction Register 16
HDMI TX Controller_EARCRX_CMDC_XACT_WR17	0x1884	W	0x00000000	eARC RX - CMDC Write Transaction Register 17
HDMI TX Controller_EARCRX_CMDC_XACT_WR18	0x1888	W	0x00000000	eARC RX - CMDC Write Transaction Register 18
HDMI TX Controller_EARCRX_CMDC_XACT_WR19	0x188C	W	0x00000000	eARC RX - CMDC Write Transaction Register 19

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_WR20	0x1890	W	0x00000000	eARC RX - CMDC Write Transaction Register 20
HDMI TX Controller_EARCRX_CMDC_XACT_WR21	0x1894	W	0x00000000	eARC RX - CMDC Write Transaction Register 21
HDMI TX Controller_EARCRX_CMDC_XACT_WR22	0x1898	W	0x00000000	eARC RX - CMDC Write Transaction Register 22
HDMI TX Controller_EARCRX_CMDC_XACT_WR23	0x189C	W	0x00000000	eARC RX - CMDC Write Transaction Register 23
HDMI TX Controller_EARCRX_CMDC_XACT_WR24	0x18A0	W	0x00000000	eARC RX - CMDC Write Transaction Register 24
HDMI TX Controller_EARCRX_CMDC_XACT_WR25	0x18A4	W	0x00000000	eARC RX - CMDC Write Transaction Register 25
HDMI TX Controller_EARCRX_CMDC_XACT_WR26	0x18A8	W	0x00000000	eARC RX - CMDC Write Transaction Register 26
HDMI TX Controller_EARCRX_CMDC_XACT_WR27	0x18AC	W	0x00000000	eARC RX - CMDC Write Transaction Register 27
HDMI TX Controller_EARCRX_CMDC_XACT_WR28	0x18B0	W	0x00000000	eARC RX - CMDC Write Transaction Register 28
HDMI TX Controller_EARCRX_CMDC_XACT_WR29	0x18B4	W	0x00000000	eARC RX - CMDC Write Transaction Register 29
HDMI TX Controller_EARCRX_CMDC_XACT_WR30	0x18B8	W	0x00000000	eARC RX - CMDC Write Transaction Register 30
HDMI TX Controller_EARCRX_CMDC_XACT_WR31	0x18BC	W	0x00000000	eARC RX - CMDC Write Transaction Register 31
HDMI TX Controller_EARCRX_CMDC_XACT_WR32	0x18C0	W	0x00000000	eARC RX - CMDC Write Transaction Register 32
HDMI TX Controller_EARCRX_CMDC_XACT_WR33	0x18C4	W	0x00000000	eARC RX - CMDC Write Transaction Register 33
HDMI TX Controller_EARCRX_CMDC_XACT_WR34	0x18C8	W	0x00000000	eARC RX - CMDC Write Transaction Register 34
HDMI TX Controller_EARCRX_CMDC_XACT_WR35	0x18CC	W	0x00000000	eARC RX - CMDC Write Transaction Register 35
HDMI TX Controller_EARCRX_CMDC_XACT_WR36	0x18D0	W	0x00000000	eARC RX - CMDC Write Transaction Register 36
HDMI TX Controller_EARCRX_CMDC_XACT_WR37	0x18D4	W	0x00000000	eARC RX - CMDC Write Transaction Register 37

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_WR38	0x18D8	W	0x00000000	eARC RX - CMDC Write Transaction Register 38
HDMI TX Controller_EARCRX_CMDC_XACT_WR39	0x18DC	W	0x00000000	eARC RX - CMDC Write Transaction Register 39
HDMI TX Controller_EARCRX_CMDC_XACT_WR40	0x18E0	W	0x00000000	eARC RX - CMDC Write Transaction Register 40
HDMI TX Controller_EARCRX_CMDC_XACT_WR41	0x18E4	W	0x00000000	eARC RX - CMDC Write Transaction Register 41
HDMI TX Controller_EARCRX_CMDC_XACT_WR42	0x18E8	W	0x00000000	eARC RX - CMDC Write Transaction Register 42
HDMI TX Controller_EARCRX_CMDC_XACT_WR43	0x18EC	W	0x00000000	eARC RX - CMDC Write Transaction Register 43
HDMI TX Controller_EARCRX_CMDC_XACT_WR44	0x18F0	W	0x00000000	eARC RX - CMDC Write Transaction Register 44
HDMI TX Controller_EARCRX_CMDC_XACT_WR45	0x18F4	W	0x00000000	eARC RX - CMDC Write Transaction Register 45
HDMI TX Controller_EARCRX_CMDC_XACT_WR46	0x18F8	W	0x00000000	eARC RX - CMDC Write Transaction Register 46
HDMI TX Controller_EARCRX_CMDC_XACT_WR47	0x18FC	W	0x00000000	eARC RX - CMDC Write Transaction Register 47
HDMI TX Controller_EARCRX_CMDC_XACT_WR48	0x1900	W	0x00000000	eARC RX - CMDC Write Transaction Register 48
HDMI TX Controller_EARCRX_CMDC_XACT_WR49	0x1904	W	0x00000000	eARC RX - CMDC Write Transaction Register 49
HDMI TX Controller_EARCRX_CMDC_XACT_WR50	0x1908	W	0x00000000	eARC RX - CMDC Write Transaction Register 50
HDMI TX Controller_EARCRX_CMDC_XACT_WR51	0x190C	W	0x00000000	eARC RX - CMDC Write Transaction Register 51
HDMI TX Controller_EARCRX_CMDC_XACT_WR52	0x1910	W	0x00000000	eARC RX - CMDC Write Transaction Register 52
HDMI TX Controller_EARCRX_CMDC_XACT_WR53	0x1914	W	0x00000000	eARC RX - CMDC Write Transaction Register 53
HDMI TX Controller_EARCRX_CMDC_XACT_WR54	0x1918	W	0x00000000	eARC RX - CMDC Write Transaction Register 54
HDMI TX Controller_EARCRX_CMDC_XACT_WR55	0x191C	W	0x00000000	eARC RX - CMDC Write Transaction Register 55

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_WR56	0x1920	W	0x00000000	eARC RX - CMDC Write Transaction Register 56
HDMI TX Controller_EARCRX_CMDC_XACT_WR57	0x1924	W	0x00000000	eARC RX - CMDC Write Transaction Register 57
HDMI TX Controller_EARCRX_CMDC_XACT_WR58	0x1928	W	0x00000000	eARC RX - CMDC Write Transaction Register 58
HDMI TX Controller_EARCRX_CMDC_XACT_WR59	0x192C	W	0x00000000	eARC RX - CMDC Write Transaction Register 59
HDMI TX Controller_EARCRX_CMDC_XACT_WR60	0x1930	W	0x00000000	eARC RX - CMDC Write Transaction Register 60
HDMI TX Controller_EARCRX_CMDC_XACT_WR61	0x1934	W	0x00000000	eARC RX - CMDC Write Transaction Register 61
HDMI TX Controller_EARCRX_CMDC_XACT_WR62	0x1938	W	0x00000000	eARC RX - CMDC Write Transaction Register 62
HDMI TX Controller_EARCRX_CMDC_XACT_WR63	0x193C	W	0x00000000	eARC RX - CMDC Write Transaction Register 63
HDMI TX Controller_EARCRX_CMDC_XACT_WR64	0x1940	W	0x00000000	eARC RX - CMDC Write Transaction Register 64
HDMI TX Controller_EARCRX_CMDC_XACT_RD0	0x1960	W	0x00000000	eARC RX - CMDC Read Transaction Register 0
HDMI TX Controller_EARCRX_CMDC_XACT_RD1	0x1964	W	0x00000000	eARC RX - CMDC Read Transaction Register 1
HDMI TX Controller_EARCRX_CMDC_XACT_RD2	0x1968	W	0x00000000	eARC RX - CMDC Read Transaction Register 2
HDMI TX Controller_EARCRX_CMDC_XACT_RD3	0x196C	W	0x00000000	eARC RX - CMDC Read Transaction Register 3
HDMI TX Controller_EARCRX_CMDC_XACT_RD4	0x1970	W	0x00000000	eARC RX - CMDC Read Transaction Register 4
HDMI TX Controller_EARCRX_CMDC_XACT_RD5	0x1974	W	0x00000000	eARC RX - CMDC Read Transaction Register 5
HDMI TX Controller_EARCRX_CMDC_XACT_RD6	0x1978	W	0x00000000	eARC RX - CMDC Read Transaction Register 6
HDMI TX Controller_EARCRX_CMDC_XACT_RD7	0x197C	W	0x00000000	eARC RX - CMDC Read Transaction Register 7
HDMI TX Controller_EARCRX_CMDC_XACT_RD8	0x1980	W	0x00000000	eARC RX - CMDC Read Transaction Register 8

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_RD9	0x1984	W	0x00000000	eARC RX - CMDC Read Transaction Register 9
HDMI TX Controller_EARCRX_CMDC_XACT_RD10	0x1988	W	0x00000000	eARC RX - CMDC Read Transaction Register 10
HDMI TX Controller_EARCRX_CMDC_XACT_RD11	0x198C	W	0x00000000	eARC RX - CMDC Read Transaction Register 11
HDMI TX Controller_EARCRX_CMDC_XACT_RD12	0x1990	W	0x00000000	eARC RX - CMDC Read Transaction Register 12
HDMI TX Controller_EARCRX_CMDC_XACT_RD13	0x1994	W	0x00000000	eARC RX - CMDC Read Transaction Register 13
HDMI TX Controller_EARCRX_CMDC_XACT_RD14	0x1998	W	0x00000000	eARC RX - CMDC Read Transaction Register 14
HDMI TX Controller_EARCRX_CMDC_XACT_RD15	0x199C	W	0x00000000	eARC RX - CMDC Read Transaction Register 15
HDMI TX Controller_EARCRX_CMDC_XACT_RD16	0x19A0	W	0x00000000	eARC RX - CMDC Read Transaction Register 16
HDMI TX Controller_EARCRX_CMDC_XACT_RD17	0x19A4	W	0x00000000	eARC RX - CMDC Read Transaction Register 17
HDMI TX Controller_EARCRX_CMDC_XACT_RD18	0x19A8	W	0x00000000	eARC RX - CMDC Read Transaction Register 18
HDMI TX Controller_EARCRX_CMDC_XACT_RD19	0x19AC	W	0x00000000	eARC RX - CMDC Read Transaction Register 19
HDMI TX Controller_EARCRX_CMDC_XACT_RD20	0x19B0	W	0x00000000	eARC RX - CMDC Read Transaction Register 20
HDMI TX Controller_EARCRX_CMDC_XACT_RD21	0x19B4	W	0x00000000	eARC RX - CMDC Read Transaction Register 21
HDMI TX Controller_EARCRX_CMDC_XACT_RD22	0x19B8	W	0x00000000	eARC RX - CMDC Read Transaction Register 22
HDMI TX Controller_EARCRX_CMDC_XACT_RD23	0x19BC	W	0x00000000	eARC RX - CMDC Read Transaction Register 23
HDMI TX Controller_EARCRX_CMDC_XACT_RD24	0x19C0	W	0x00000000	eARC RX - CMDC Read Transaction Register 24
HDMI TX Controller_EARCRX_CMDC_XACT_RD25	0x19C4	W	0x00000000	eARC RX - CMDC Read Transaction Register 25
HDMI TX Controller_EARCRX_CMDC_XACT_RD26	0x19C8	W	0x00000000	eARC RX - CMDC Read Transaction Register 26

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_RD27	0x19CC	W	0x00000000	eARC RX - CMDC Read Transaction Register 27
HDMI TX Controller_EARCRX_CMDC_XACT_RD28	0x19D0	W	0x00000000	eARC RX - CMDC Read Transaction Register 28
HDMI TX Controller_EARCRX_CMDC_XACT_RD29	0x19D4	W	0x00000000	eARC RX - CMDC Read Transaction Register 29
HDMI TX Controller_EARCRX_CMDC_XACT_RD30	0x19D8	W	0x00000000	eARC RX - CMDC Read Transaction Register 30
HDMI TX Controller_EARCRX_CMDC_XACT_RD31	0x19DC	W	0x00000000	eARC RX - CMDC Read Transaction Register 31
HDMI TX Controller_EARCRX_CMDC_XACT_RD32	0x19E0	W	0x00000000	eARC RX - CMDC Read Transaction Register 32
HDMI TX Controller_EARCRX_CMDC_XACT_RD33	0x19E4	W	0x00000000	eARC RX - CMDC Read Transaction Register 33
HDMI TX Controller_EARCRX_CMDC_XACT_RD34	0x19E8	W	0x00000000	eARC RX - CMDC Read Transaction Register 34
HDMI TX Controller_EARCRX_CMDC_XACT_RD35	0x19EC	W	0x00000000	eARC RX - CMDC Read Transaction Register 35
HDMI TX Controller_EARCRX_CMDC_XACT_RD36	0x19F0	W	0x00000000	eARC RX - CMDC Read Transaction Register 36
HDMI TX Controller_EARCRX_CMDC_XACT_RD37	0x19F4	W	0x00000000	eARC RX - CMDC Read Transaction Register 37
HDMI TX Controller_EARCRX_CMDC_XACT_RD38	0x19F8	W	0x00000000	eARC RX - CMDC Read Transaction Register 38
HDMI TX Controller_EARCRX_CMDC_XACT_RD39	0x19FC	W	0x00000000	eARC RX - CMDC Read Transaction Register 39
HDMI TX Controller_EARCRX_CMDC_XACT_RD40	0x1A00	W	0x00000000	eARC RX - CMDC Read Transaction Register 40
HDMI TX Controller_EARCRX_CMDC_XACT_RD41	0x1A04	W	0x00000000	eARC RX - CMDC Read Transaction Register 41
HDMI TX Controller_EARCRX_CMDC_XACT_RD42	0x1A08	W	0x00000000	eARC RX - CMDC Read Transaction Register 42
HDMI TX Controller_EARCRX_CMDC_XACT_RD43	0x1A0C	W	0x00000000	eARC RX - CMDC Read Transaction Register 43
HDMI TX Controller_EARCRX_CMDC_XACT_RD44	0x1A10	W	0x00000000	eARC RX - CMDC Read Transaction Register 44

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_RD45	0x1A14	W	0x00000000	eARC RX - CMDC Read Transaction Register 45
HDMI TX Controller_EARCRX_CMDC_XACT_RD46	0x1A18	W	0x00000000	eARC RX - CMDC Read Transaction Register 46
HDMI TX Controller_EARCRX_CMDC_XACT_RD47	0x1A1C	W	0x00000000	eARC RX - CMDC Read Transaction Register 47
HDMI TX Controller_EARCRX_CMDC_XACT_RD48	0x1A20	W	0x00000000	eARC RX - CMDC Read Transaction Register 48
HDMI TX Controller_EARCRX_CMDC_XACT_RD49	0x1A24	W	0x00000000	eARC RX - CMDC Read Transaction Register 49
HDMI TX Controller_EARCRX_CMDC_XACT_RD50	0x1A28	W	0x00000000	eARC RX - CMDC Read Transaction Register 50
HDMI TX Controller_EARCRX_CMDC_XACT_RD51	0x1A2C	W	0x00000000	eARC RX - CMDC Read Transaction Register 51
HDMI TX Controller_EARCRX_CMDC_XACT_RD52	0x1A30	W	0x00000000	eARC RX - CMDC Read Transaction Register 52
HDMI TX Controller_EARCRX_CMDC_XACT_RD53	0x1A34	W	0x00000000	eARC RX - CMDC Read Transaction Register 53
HDMI TX Controller_EARCRX_CMDC_XACT_RD54	0x1A38	W	0x00000000	eARC RX - CMDC Read Transaction Register 54
HDMI TX Controller_EARCRX_CMDC_XACT_RD55	0x1A3C	W	0x00000000	eARC RX - CMDC Read Transaction Register 55
HDMI TX Controller_EARCRX_CMDC_XACT_RD56	0x1A40	W	0x00000000	eARC RX - CMDC Read Transaction Register 56
HDMI TX Controller_EARCRX_CMDC_XACT_RD57	0x1A44	W	0x00000000	eARC RX - CMDC Read Transaction Register 57
HDMI TX Controller_EARCRX_CMDC_XACT_RD58	0x1A48	W	0x00000000	eARC RX - CMDC Read Transaction Register 58
HDMI TX Controller_EARCRX_CMDC_XACT_RD59	0x1A4C	W	0x00000000	eARC RX - CMDC Read Transaction Register 59
HDMI TX Controller_EARCRX_CMDC_XACT_RD60	0x1A50	W	0x00000000	eARC RX - CMDC Read Transaction Register 60
HDMI TX Controller_EARCRX_CMDC_XACT_RD61	0x1A54	W	0x00000000	eARC RX - CMDC Read Transaction Register 61
HDMI TX Controller_EARCRX_CMDC_XACT_RD62	0x1A58	W	0x00000000	eARC RX - CMDC Read Transaction Register 62

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_CMDC_XACT_RD63	0x1A5C	W	0x00000000	eARC RX - CMDC Read Transaction Register 63
HDMI TX Controller_EARCRX_CMDC_XACT_RD64	0x1A60	W	0x00000000	eARC RX - CMDC Read Transaction Register 64
HDMI TX Controller_EARCRX_CMDC_SYNC_CONFIG	0x1B00	W	0x0000040E	eARC RX - CMDC Synchronization Configuration Register
HDMI TX Controller_EARCRX_DMAC_PHY_CONTROL	0x1C00	W	0x00000000	eARC RX - DMAC PHY Control Register
HDMI TX Controller_EARCRX_DMAC_CONFIG	0x1C08	W	0x00000001	eARC RX - DMAC Configuration Register
HDMI TX Controller_EARCRX_DMAC_CONTROL0	0x1C0C	W	0x00000001	eARC RX - DMAC Control Register 0
HDMI TX Controller_EARCRX_DMAC_CONTROL1	0x1C10	W	0x00000000	eARC RX - DMAC Control Register 1
HDMI TX Controller_EARCRX_DMAC_STATUS	0x1C14	W	0x00000000	eARC RX - DMAC Status Register
HDMI TX Controller_EARCRX_DMAC_CHSTATUS0	0x1C18	W	0x00000000	eARC RX - DMAC Audio Channel Status Register 0
HDMI TX Controller_EARCRX_DMAC_CHSTATUS1	0x1C1C	W	0x00000000	eARC RX - DMAC Audio Channel Status Register 1
HDMI TX Controller_EARCRX_DMAC_CHSTATUS2	0x1C20	W	0x00000000	eARC RX - DMAC Audio Channel Status Register 2
HDMI TX Controller_EARCRX_DMAC_CHSTATUS3	0x1C24	W	0x00000000	eARC RX - DMAC Audio Channel Status Register 3
HDMI TX Controller_EARCRX_DMAC_CHSTATUS4	0x1C28	W	0x00000000	eARC RX - DMAC Audio Channel Status Register 4
HDMI TX Controller_EARCRX_DMAC_CHSTATUS5	0x1C2C	W	0x00000000	eARC RX - DMAC Audio Channel Status Register 5
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT0	0x1C30	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 0
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT1	0x1C34	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 1
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT2	0x1C38	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 2

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT3	0x1C3C	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 3
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT4	0x1C40	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 4
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT5	0x1C44	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 5
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT6	0x1C48	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 6
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT7	0x1C4C	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 7
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT8	0x1C50	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 8
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT9	0x1C54	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 9
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT10	0x1C58	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 10
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT11	0x1C5C	W	0x00000000	eARC RX - DMAC User Data H14b ACP Message Payload Register 11
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT0	0x1C60	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 0
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT1	0x1C64	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 1
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT2	0x1C68	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 2
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT3	0x1C6C	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 3

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT4	0x1C70	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 4
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT5	0x1C74	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 5
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT6	0x1C78	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 6
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT7	0x1C7C	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 7
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT8	0x1C80	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 8
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT9	0x1C84	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 9
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT10	0x1C88	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 10
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT11	0x1C8C	W	0x00000000	eARC RX - DMAC User Data H14b ISRC1 Message Payload Register 11
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT0	0x1C90	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 0
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT1	0x1C94	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 1
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT2	0x1C98	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 2
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT3	0x1C9C	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 3
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT4	0x1CA0	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 4

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT5	0x1CA4	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 5
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT6	0x1CA8	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 6
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT7	0x1CAC	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 7
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT8	0x1CB0	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 8
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT9	0x1CB4	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 9
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT10	0x1CB8	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 10
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT11	0x1CBC	W	0x00000000	eARC RX - DMAC User Data H14b ISRC2 Message Payload Register 11
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC0	0x1CC0	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 0
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC1	0x1CC4	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 1
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC2	0x1CC8	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 2
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC3	0x1CCC	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 3
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC4	0x1CD0	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 4
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC5	0x1CD4	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 5

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC6	0x1CD8	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 6
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC7	0x1CDC	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 7
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC8	0x1CE0	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 8
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC9	0x1CE4	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 9
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC10	0x1CE8	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 10
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC11	0x1CEC	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 11
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC12	0x1CF0	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 12
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC13	0x1CF4	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 13
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC14	0x1CF8	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 14
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC15	0x1CFC	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 15
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC16	0x1D00	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 16
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC17	0x1D04	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 17
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC18	0x1D08	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 18

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC19	0x1D0C	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 19
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC20	0x1D10	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 20
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC21	0x1D14	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 21
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC22	0x1D18	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 22
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC23	0x1D1C	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 23
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC24	0x1D20	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 24
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC25	0x1D24	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 25
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC26	0x1D28	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 26
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC27	0x1D2C	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 27
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC28	0x1D30	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 28
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC29	0x1D34	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 29
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC30	0x1D38	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 30
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC31	0x1D3C	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 31

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC32	0x1D40	W	0x00000000	eARC RX - DMAC User Data Generic Message Payload Register 32
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER0	0x1D44	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 0
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER1	0x1D48	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 1
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER2	0x1D4C	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 2
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER3	0x1D50	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 3
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER4	0x1D54	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 4
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER5	0x1D58	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 5
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER6	0x1D5C	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 6
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER7	0x1D60	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 7
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER8	0x1D64	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 8
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER9	0x1D68	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 9
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER10	0x1D6C	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 10
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER11	0x1D70	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 11
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER12	0x1D74	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 12
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER13	0x1D78	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 13
HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER14	0x1D7C	W	0x00000000	eARC RX - DMAC Audio Channel Status Streamer Register 14
HDMI TX Controller_EARCRX_DMAC_USRDATA_STREAMER0	0x1D80	W	0x00000000	eARC RX - DMAC Audio User Data Streamer Register 0

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_MAIN_INTVEC_INDEX	0x3000	W	0x00000000	Main Unit Interrupt Vector Table Register
HDMI TX Controller_MAINUNIT_0_INT_STATUS	0x3010	W	0x00000000	Main Unit 0 Interrupt Status Register
HDMI TX Controller_MAINUNIT_0_INT_MASK_N	0x3014	W	0x80000000	Main Unit 0 Interrupt Mask Register
HDMI TX Controller_MAINUNIT_0_INT_CLEAR	0x3018	W	0x00000000	Main Unit 0 Interrupt Clear Register
HDMI TX Controller_MAINUNIT_0_INT_FORCE	0x301C	W	0x00000000	Main Unit 0 Interrupt Force Register
HDMI TX Controller_MAINUNIT_1_INT_STATUS	0x3020	W	0x00000000	Main Unit 1 Interrupt Status Register
HDMI TX Controller_MAINUNIT_1_INT_MASK_N	0x3024	W	0x00000000	Main Unit 1 Interrupt Mask Register
HDMI TX Controller_MAINUNIT_1_INT_CLEAR	0x3028	W	0x00000000	Main Unit 1 Interrupt Clear Register
HDMI TX Controller_MAINUNIT_1_INT_FORCE	0x302C	W	0x00000000	Main Unit 1 Interrupt Force Register
HDMI TX Controller_AVP_INTVEC_INDEX	0x3800	W	0x00000000	AVP Interrupt Vector Table Register
HDMI TX Controller_AVP_0_INT_STATUS	0x3810	W	0x00000000	AVPUNIT 0 Interrupt Status Register
HDMI TX Controller_AVP_0_INT_MASK_N	0x3814	W	0x00000000	AVPUNIT 0 Interrupt Mask Register
HDMI TX Controller_AVP_0_INT_CLEAR	0x3818	W	0x00000000	AVPUNIT 0 Interrupt Clear Register
HDMI TX Controller_AVP_0_INT_FORCE	0x381C	W	0x00000000	AVPUNIT 0 Interrupt Force Register
HDMI TX Controller_AVP_1_INT_STATUS	0x3820	W	0x00000000	AVPUNIT 1 Interrupt Status Register
HDMI TX Controller_AVP_1_INT_MASK_N	0x3824	W	0x00000000	AVPUNIT 1 Interrupt Mask Register
HDMI TX Controller_AVP_1_INT_CLEAR	0x3828	W	0x00000000	AVPUNIT 1 Interrupt Clear Register
HDMI TX Controller_AVP_1_INT_FORCE	0x382C	W	0x00000000	AVPUNIT 1 Interrupt Force Register

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AVP_2_INT_STATUS	0x3830	W	0x00000000	AVPUNIT 2 Interrupt Status Register
HDMI TX Controller_AVP_2_INT_MASK_N	0x3834	W	0x00000000	AVPUNIT 2 Interrupt Mask Register
HDMI TX Controller_AVP_2_INT_CLEAR	0x3838	W	0x00000000	AVPUNIT 2 Interrupt Clear Register
HDMI TX Controller_AVP_2_INT_FORCE	0x383C	W	0x00000000	AVPUNIT 2 Interrupt Force Register
HDMI TX Controller_AVP_3_INT_STATUS	0x3840	W	0x00000000	AVPUNIT 3 Interrupt Status Register
HDMI TX Controller_AVP_3_INT_MASK_N	0x3844	W	0x00000000	AVPUNIT 3 Interrupt Mask Register
HDMI TX Controller_AVP_3_INT_CLEAR	0x3848	W	0x00000000	AVPUNIT 3 Interrupt Clear Register
HDMI TX Controller_AVP_3_INT_FORCE	0x384C	W	0x00000000	AVPUNIT 3 Interrupt Force Register
HDMI TX Controller_AVP_4_INT_STATUS	0x3850	W	0x00000000	AVPUNIT 4 Interrupt Status Register
HDMI TX Controller_AVP_4_INT_MASK_N	0x3854	W	0x00000000	AVPUNIT 4 Interrupt Mask Register
HDMI TX Controller_AVP_4_INT_CLEAR	0x3858	W	0x00000000	AVPUNIT 4 Interrupt Clear Register
HDMI TX Controller_AVP_4_INT_FORCE	0x385C	W	0x00000000	AVPUNIT 4 Interrupt Force Register
HDMI TX Controller_AVP_5_INT_STATUS	0x3860	W	0x00000000	AVPUNIT 5 Interrupt Status Register
HDMI TX Controller_AVP_5_INT_MASK_N	0x3864	W	0x00000000	AVPUNIT 5 Interrupt Mask Register
HDMI TX Controller_AVP_5_INT_CLEAR	0x3868	W	0x00000000	AVPUNIT 5 Interrupt Clear Register
HDMI TX Controller_AVP_5_INT_FORCE	0x386C	W	0x00000000	AVPUNIT 5 Interrupt Force Register
HDMI TX Controller_AVP_6_INT_STATUS	0x3870	W	0x00000000	AVPUNIT 6 Interrupt Status Register
HDMI TX Controller_AVP_6_INT_MASK_N	0x3874	W	0x00000000	AVPUNIT 6 Interrupt Mask Register

Name	Offset	Size	Reset Value	Description
HDMI TX Controller_AVP_6_INT_CLEAR	0x3878	W	0x00000000	AVPUNIT 6 Interrupt Clear Register
HDMI TX Controller_AVP_6_INT_FORCE	0x387C	W	0x00000000	AVPUNIT 6 Interrupt Force Register
HDMI TX Controller_CEC_INT_STATUS	0x4000	W	0x00000000	CEC Interrupt Status Register
HDMI TX Controller_CEC_INT_MASK_N	0x4004	W	0x00000000	CEC Interrupt Mask Register
HDMI TX Controller_CEC_INT_CLEAR	0x4008	W	0x00000000	CEC Interrupt Clear Register
HDMI TX Controller_CEC_INT_FORCE	0x400C	W	0x00000000	CEC Interrupt Force Register
HDMI TX Controller_EARCRX_INTVEC_INDEX	0x4800	W	0x00000000	eARC RX Interrupt Vector Table Register
HDMI TX Controller_EARCRX_0_INT_STATUS	0x4810	W	0x00000000	eARC RX Interrupt Status Register 0
HDMI TX Controller_EARCRX_0_INT_MASK_N	0x4814	W	0x00000000	eARC RX Interrupt Mask Register 0
HDMI TX Controller_EARCRX_0_INT_CLEAR	0x4818	W	0x00000000	eARC RX Interrupt Clear Register 0
HDMI TX Controller_EARCRX_0_INT_FORCE	0x481C	W	0x00000000	eARC RX Interrupt Force Register 0
HDMI TX Controller_EARCRX_1_INT_STATUS	0x4820	W	0x00000000	eARC RX Interrupt Status Register 1
HDMI TX Controller_EARCRX_1_INT_MASK_N	0x4824	W	0x00000000	eARC RX Interrupt Mask Register 1
HDMI TX Controller_EARCRX_1_INT_CLEAR	0x4828	W	0x00000000	eARC RX Interrupt Clear Register 1
HDMI TX Controller_EARCRX_1_INT_FORCE	0x482C	W	0x00000000	eARC RX Interrupt Force Register 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

24.4.3 Detail Registers Description

HDMI TX Controller_CORE_ID

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x48	CORE_ID_ASCII3 ASCII encoded value of the first character of the IP identification code. Values: 0x48 (ASCII_H): H ASCII Character Value After Reset:0x48
23:16	RO	0x51	CORE_ID_ASCII2 ASCII encoded value of the second character of the IP identification code. Values: 0x51 (ASCII_Q): Q ASCII Character Value After Reset:0x51
15:8	RO	0x54	CORE_ID_ASCII1 ASCII encoded value of the third character of the IP identification code. Values: 0x54 (ASCII_T): T ASCII Character Value After Reset:0x54
7:0	RO	0x58	CORE_ID_ASCII0 ASCII encoded value of the fourth character of the IP identification code. Values: 0x58 (ASCII_X): X ASCII Character Value After Reset:0x58

HDMI TX Controller_VER_NUMBER

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x30	VER_NUMBER_ASCII3 ASCII encoded value of the first character of the IP version. Value After Reset:0x30
23:16	RO	0x31	VER_NUMBER_ASCII2 ASCII encoded value of the second character of the IP version. Value After Reset:0x31
15:8	RO	0x30	VER_NUMBER_ASCII1 ASCII encoded value of the third character of the IP version. Value After Reset:0x30
7:0	RO	0x30	VER_NUMBER_ASCII0 ASCII encoded value of the fourth character of the IP version. Value After Reset:0x30

HDMI TX Controller_VER_TYPE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x6c	VER_TYPE_ASCII3 ASCII encoded value of the first character of the IP release type. Value After Reset:0x6c
23:16	RO	0x75	VER_TYPE_ASCII2 ASCII encoded value of the second character of the IP release type. Value After Reset:0x75
15:8	RO	0x30	VER_TYPE_ASCII1 ASCII encoded value of the third character of the IP release type. Value After Reset:0x30

Bit	Attr	Reset Value	Description
7:0	RO	0x30	VER_TYPE_ASCII0 ASCII encoded value of the fourth character of the IP release type. Value After Reset:0x30

HDMI TX Controller_CONFIG_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved5 Reserved Field:Yes
28	RO	0x1	CEC The CEC interface is present in the generated controller RTL. Value After Reset:0x1
27:25	RW	0x0	Reserved4 Reserved Field:Yes
24	RO	0x1	EARCRX Enhanced Audio Return Channel (eARC) RX interface is present in the generated controller RTL. Value After Reset:0x1
23	RO	0x1	AUD_UD Support for IEC 60958 User Data channel is present in the generated controller RTL. Value After Reset:0x1
22	RO	0x1	AUD_MS Support for Multi-Stream Audio is present in the generated controller RTL. Value After Reset:0x1
21	RO	0x1	AUD_HBR Support for High Bit Rate Audio is present in the generated controller RTL. Value After Reset:0x1
20	RO	0x0	AUD_3D Support for 3D Audio is present in the generated controller RTL. Value After Reset:0x0
19:16	RW	0x0	Reserved3 Reserved Field:Yes
15	RO	0x1	CVTEM Support for Compressed Video Timing Extended Metadata (CVTEM) Packets is present in the generated controller RTL. Value After Reset:0x1
14	RO	0x1	VTEM Support for Video Timing Extended Metadata (VTEM) Packets is present in the generated controller RTL. Value After Reset:0x1
13	RO	0x0	EEMP Support for External Extended Metadata Packets (EEMP) is present in the generated controller RTL. Value After Reset:0x0
12	RO	0x1	FRL The Fixed Rate Link (FRL) feature is present in the generated controller RTL. Value After Reset:0x1
11	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
10	RO	0x1	HDCP14_SW_SHA1CALC The hardware for the SHA-1 calculation for HDCP 1.4 Protocol is not present in the generated controller RTL and the software calculates the SHA-1. Value After Reset:0x1
9	RO	0x0	HDCP14_DKSET_EXTERNAL The Device Key Set from the HDCP 1.4 Protocol is stored in the external memory. Value After Reset:0x0
8	RO	0x1	HDCP14 Support for HDCP1.4 Encryption is present in the generated controller RTL. Value After Reset:0x1
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	PR Support for Pixel Repetition is present in the generated controller RTL. Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RO	0x1	AVP The HDMI TX Audio, Video, and Packet (AVP) processing is present in the generated controller RTL. Value After Reset:0x1

HDMI TX Controller_CORE_TIMESTAMP_HHMM

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x31	CORE_TIMESTAMP_HHMM_ASCII3 ASCII value of the tens digit of the hour. Values: 0x30 (TENS_OF_HOURS_0): 0 is the tens digit of the hours 0x31 (TENS_OF_HOURS_1): 1 is the tens digit of the hours 0x32 (TENS_OF_HOURS_2): 2 is the tens digit of the hours Value After Reset:0x31
23:16	RO	0x37	CORE_TIMESTAMP_HHMM_ASCII2 ASCII value of the units digit of the hour. Values: 0x30 (HOUR_0): 0 is the units digit of the hours 0x31 (HOUR_1): 1 is the units digit of the hours 0x32 (HOUR_2): 2 is the units digit of the hours 0x33 (HOUR_3): 3 is the units digit of the hours 0x34 (HOUR_4): 4 is the units digit of the hours 0x35 (HOUR_5): 5 is the units digit of the hours 0x36 (HOUR_6): 6 is the units digit of the hours 0x37 (HOUR_7): 7 is the units digit of the hours 0x38 (HOUR_8): 8 is the units digit of the hours 0x39 (HOUR_9): 9 is the units digit of the hours Value After Reset:0x37

Bit	Attr	Reset Value	Description
15:8	RO	0x33	CORE_TIMESTAMP_HHMM_ASCII1 ASCII value of the tens digit of the minute. Values: 0x30 (TENS_OF_MINUTES_0): 0 is the tens digit of the minutes 0x31 (TENS_OF_MINUTES_1): 1 is the tens digit of the minutes 0x32 (TENS_OF_MINUTES_2): 2 is the tens digit of the minutes 0x33 (TENS_OF_MINUTES_3): 3 is the tens digit of the minutes 0x34 (TENS_OF_MINUTES_4): 4 is the tens digit of the minutes 0x35 (TENS_OF_MINUTES_5): 5 is the tens digit of the minutes Value After Reset:0x33
7:0	RO	0x36	CORE_TIMESTAMP_HHMM_ASCII0 ASCII value of the units digit of the minute. Values: 0x30 (MINUTE_0): 0 is the units digit of the minutes 0x31 (MINUTE_1): 1 is the units digit of the minutes 0x32 (MINUTE_2): 2 is the units digit of the minutes 0x33 (MINUTE_3): 3 is the units digit of the minutes 0x34 (MINUTE_4): 4 is the units digit of the minutes 0x35 (MINUTE_5): 5 is the units digit of the minutes 0x36 (MINUTE_6): 6 is the units digit of the minutes 0x37 (MINUTE_7): 7 is the units digit of the minutes 0x38 (MINUTE_8): 8 is the units digit of the minutes 0x39 (MINUTE_9): 9 is the units digit of the minutes Value After Reset:0x36

HDMI TX Controller_CORE_TIMESTAMP_MMDD

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x3033	CORE_TIMESTAMP_MM ASCII value of the month (in numerical format) Values: 0x3031 (MONTH_01): Month 1 of the year 0x3032 (MONTH_02): Month 2 of the year 0x3033 (MONTH_03): Month 3 of the year 0x3034 (MONTH_04): Month 4 of the year 0x3035 (MONTH_05): Month 5 of the year 0x3036 (MONTH_06): Month 6 of the year 0x3037 (MONTH_07): Month 7 of the year 0x3038 (MONTH_08): Month 8 of the year 0x3039 (MONTH_09): Month 9 of the year 0x3130 (MONTH_10): Month 10 of the year 0x3131 (MONTH_11): Month 11 of the year 0x3132 (MONTH_12): Month 12 of the year Value After Reset:0x3036

Bit	Attr	Reset Value	Description
15:0	RO	0x3131	CORE_TIMESTAMP_DD ASCII value of the day Values: 0x3031 (DAY_01): Day 1 of the month 0x3032 (DAY_02): Day 2 of the month 0x3033 (DAY_03): Day 3 of the month 0x3034 (DAY_04): Day 4 of the month 0x3035 (DAY_05): Day 5 of the month 0x3036 (DAY_06): Day 6 of the month 0x3037 (DAY_07): Day 7 of the month 0x3038 (DAY_08): Day 8 of the month 0x3039 (DAY_09): Day 9 of the month 0x3130 (DAY_10): Day 10 of the month 0x3131 (DAY_11): Day 11 of the month 0x3132 (DAY_12): Day 12 of the month 0x3133 (DAY_13): Day 13 of the month 0x3134 (DAY_14): Day 14 of the month 0x3135 (DAY_15): Day 15 of the month 0x3136 (DAY_16): Day 16 of the month 0x3137 (DAY_17): Day 17 of the month 0x3138 (DAY_18): Day 18 of the month 0x3139 (DAY_19): Day 19 of the month 0x3230 (DAY_20): Day 20 of the month 0x3231 (DAY_21): Day 21 of the month 0x3232 (DAY_22): Day 22 of the month 0x3233 (DAY_23): Day 23 of the month 0x3234 (DAY_24): Day 24 of the month 0x3235 (DAY_25): Day 25 of the month 0x3236 (DAY_26): Day 26 of the month 0x3237 (DAY_27): Day 27 of the month 0x3238 (DAY_28): Day 28 of the month 0x3239 (DAY_29): Day 29 of the month 0x3330 (DAY_30): Day 30 of the month 0x3331 (DAY_31): Day 31 of the month Value After Reset:0x3136

HDMI TX Controller_CORE_TIMESTAMP_YYYY

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x32	CORE_TIMESTAMP_YYYY_ASCII3 ASCII value of the thousands digit of the year Values: 0x31 (YEAR_THOUSANDS_1): 1 is the thousands digit of the year 0x32 (YEAR_THOUSANDS_2): 2 is the thousands digit of the year Value After Reset:0x32
23:16	RO	0x30	CORE_TIMESTAMP_YYYY_ASCII2 ASCII value of the hundreds digit of the year Values: 0x30 (YEAR_HUNDREDS_0): 0 is the hundreds digit of the year 0x39 (YEAR_HUNDREDS_9): 9 is the hundreds digit of the year Value After Reset:0x30

Bit	Attr	Reset Value	Description
15:8	RO	0x32	CORE_TIMESTAMP_YYYY_ASCII1 ASCII value of the tens digit of the year Values: 0x30 (YEAR_TENS_0): 0 is the tens digit of the year 0x31 (YEAR_TENS_1): 1 is the tens digit of the year 0x32 (YEAR_TENS_2): 2 is the tens digit of the year 0x33 (YEAR_TENS_3): 3 is the tens digit of the year 0x34 (YEAR_TENS_4): 4 is the tens digit of the year 0x35 (YEAR_TENS_5): 5 is the tens digit of the year 0x36 (YEAR_TENS_6): 6 is the tens digit of the year 0x37 (YEAR_TENS_7): 7 is the tens digit of the year 0x38 (YEAR_TENS_8): 8 is the tens digit of the year 0x39 (YEAR_TENS_9): 9 is the tens digit of the year Value After Reset:0x32
7:0	RO	0x31	CORE_TIMESTAMP_YYYY_ASCII0 ASCII value of the units digit of the year. Values: 0x30 (YEAR_UNITS_0): 0 is the units digit of the year 0x31 (YEAR_UNITS_1): 1 is the units digit of the year 0x32 (YEAR_UNITS_2): 2 is the units digit of the year 0x33 (YEAR_UNITS_3): 3 is the units digit of the year 0x34 (YEAR_UNITS_4): 4 is the units digit of the year 0x35 (YEAR_UNITS_5): 5 is the units digit of the year 0x36 (YEAR_UNITS_6): 6 is the units digit of the year 0x37 (YEAR_UNITS_7): 7 is the units digit of the year 0x38 (YEAR_UNITS_8): 8 is the units digit of the year 0x39 (YEAR_UNITS_9): 9 is the units digit of the year Value After Reset:0x31

HDMI TX Controller_GLOBAL_SWRESET_REQUEST

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27	WO	0x0	EARCRX_CMDC_SWINIT_P Reset control field that when activated resets the CMDC controller in the EARCRX functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
26	WO	0x0	EARCRX_DMAC_SWINIT_P Reset control field that when activated resets the DMAC controller in the EARCRX functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

Bit	Attr	Reset Value	Description
25	WO	0x0	EARCRX_SWINIT_P Reset control field that when activated resets the EARCRX functional unit, including all configuration and status bits. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
24:19	RW	0x00	Reserved2 Reserved Field:Yes
18	WO	0x0	CEC_CTRL_SWINIT_P Reset control field that when activated resets the controller in the CEC functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
17	WO	0x0	CEC_SWINIT_P Reset control field that when activated resets the CEC functional unit, including all configuration and status bits. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
16	WO	0x0	I2C_SWINIT_P Reset control field that when activated resets the I2C Master in the MAIN functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
15:12	RW	0x0	Reserved1 Reserved Field:Yes
11	WO	0x0	AVP_DATAPATH_PACKET_METADATA_SWINIT_P Reset control field that when activated resets the Extended Metadata Packets data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
10	WO	0x0	AVP_DATAPATH_PACKET_AUDIO_SWINIT_P Reset control field that when activated resets the audio data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

Bit	Attr	Reset Value	Description
9	WO	0x0	AVP_DATAPATH_PACKET_SWINIT_P Reset control field that when activated resets the packet data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
8	WO	0x0	AVP_DATAPATH_HDCP_KEYS_SWINIT_P Reset control field that when activated resets the HDCP keys used in the data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
7	WO	0x0	AVP_DATAPATH_VIDEO_SWINIT_P Reset control field that when activated resets the video data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
6	WO	0x0	AVP_DATAPATH_SWINIT_P Reset control field that when activated resets the data path of the AVP functional unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
5	WO	0x0	AVP_SWINIT_P Reset control field that when activated resets the AVP functional unit, including all configuration and status bits. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0
4:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	MASTER_NOMAINRB_SWINIT_P Main reset control field that when activated resets all functional units. Also resets all configuration and status bits except those that are part of the MAIN unit. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	WO	0x0	MASTER_SWINIT_P Main reset control field that when activated resets all functional units and all configuration registers. This bit is self clearing: Values: 0x0 (NO_ACTION): no action 0x1 (START_RESET): start reset Value After Reset:0x0

HDMI TX Controller GLOBAL SWDISABLE

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved3 Reserved Field:Yes
26	RW	0x0	EARCRX_CTRL_SWDISABLE Disable control field that when activated disables the controllers in the EARCRX functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_EARCRX_CTRL): disable affected units Value After Reset:0x0
25	RW	0x0	EARCRX_SWDISABLE Disable control field that when activated disables the EARCRX functional unit. Also reset all contained configuration and status bits. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_EARCRX): disable affected units Value After Reset:0x0
24:19	RW	0x00	Reserved2 Reserved Field:Yes
18	RW	0x0	CEC_CTRL_SWDISABLE Disable control field that when activated disables the controller in the CEC functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_CEC_CTRL): disable affected units Value After Reset:0x0
17	RW	0x0	CEC_SWDISABLE Disable control field that when activated disables the CEC functional unit. Also reset all contained configuration and status bits. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_CEC): disable affected units Value After Reset:0x0
16	RW	0x0	I2C_SWDISABLE Disable control field that when activated disables the I2C Master in the MAIN functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_I2C): disable affected units Value After Reset:0x0
15:12	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
11	RW	0x0	AVP_DATAPATH_PACKET_METADATA_SWDISABLE Disable control field that when activated disables the Extended Metadata Packet data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_PACKET_METADATA): disable affected units Value After Reset:0x0
10	RW	0x0	AVP_DATAPATH_PACKET_AUDIO_SWDISABLE Disable control field that when activated disables the audio data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_PACKET_AUDIO): disable affected units Value After Reset:0x0
9	RW	0x0	AVP_DATAPATH_PACKET_SWDISABLE Disable control field that when activated disables the packet data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_PACKET): disable affected units Value After Reset:0x0
8	RW	0x0	AVP_DATAPATH_TMDS_SWDISABLE Disable control field that when activated disables the TMDS data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_TMDS): disable affected units Value After Reset:0x0
7	RW	0x0	AVP_DATAPATH_FRL_SWDISABLE Disable control field that when activated disables the FRL data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_FRL): disable affected units Value After Reset:0x0
6	RW	0x0	AVP_DATAPATH_VIDEO_SWDISABLE Disable control field that when activated disables the video data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH_VIDEO): disable affected units Value After Reset:0x0
5	RW	0x0	AVP_DATAPATH_SWDISABLE Disable control field that when activated disables the data path of the AVP functional unit. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP_DATAPATH): disable affected units Value After Reset:0x0

Bit	Attr	Reset Value	Description
4	RW	0x0	AVP_SWDISABLE Disable control field that when activated disables the AVP functional unit. Also reset all contained configuration and status bits. Values: 0x0 (NO_ACTION): no action 0x1 (DISABLE_AVP): disable affected units Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller RESET MANAGER CONFIG0

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	RW	0x0	RESET_MANAGER_EARC_BPCLK_OVR_VALUE Influence of earc_bpclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that earc_bpclk is in a OFF state. The Reset Manager does not overlap other domains with the earc_bpclk. 0x1 (CLK_ON): Indicates that earc_bpclk is in a ON state. The Reset Manager overlaps other domains with the earc_bpclk. Value After Reset:0x0
11	RW	0x0	RESET_MANAGER_AUDCLK_OVR_VALUE Influence of audclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that audclk is in a OFF state. The Reset Manager does not overlap other domains with the audclk. 0x1 (CLK_ON): Indicates that audclk is in a ON state. The Reset Manager overlaps other domains with the audclk. Value After Reset:0x0
10	RW	0x0	RESET_MANAGER_LINKQPCLK_OVR_VALUE Influence of linkqpclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that linkqpclk is in a OFF state. The Reset Manager does not overlap other domains with the linkqpclk. 0x1 (CLK_ON): Indicates that linkqpclk is in a ON state. The Reset Manager overlaps other domains with the linkqpclk. Value After Reset:0x0
9	RW	0x0	RESET_MANAGER_VIDQPCLK_OVR_VALUE Influence of vidqpclk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that vidqpclk is in a OFF state. The Reset Manager does not overlap other domains with the vidqpclk. 0x1 (CLK_ON): Indicates that vidqpclk is in a ON state. The Reset Manager overlaps other domains with the vidqpclk. Value After Reset:0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	RESET_MANAGER_IPI_CLK_OVR_VALUE Influence of ipi_clk in Reset Manager Override Value. Values: 0x0 (CLK_OFF): Indicates that ipi_clk is in a OFF state. The Reset Manager does not overlap other domains with the ipi_clk. 0x1 (CLK_ON): Indicates that ipi_clk is in a ON state. The Reset Manager overlaps other domains with the ipi_clk. Value After Reset:0x0
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4	RW	0x0	RESET_MANAGER_EARC_BPCLK_OVR_EN Influence of earc_bpclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.earc_bpclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_earc_bpclk_value used. Value After Reset:0x0
3	RW	0x0	RESET_MANAGER_AUDCLK_OVR_EN Influence of audclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.audclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_audclk_value used. Value After Reset:0x0
2	RW	0x0	RESET_MANAGER_LINKQPCLK_OVR_EN Influence of linkqpclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.linkqpclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_linkqpclk_value used. Value After Reset:0x0
1	RW	0x0	RESET_MANAGER_VIDQPCLK_OVR_EN Influence of vidqpclkclk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.vidqpclkclk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_vidqpclk_value used. Value After Reset:0x0
0	RW	0x0	RESET_MANAGER_IPI_CLK_OVR_EN Influence of ipi_clk in Reset Manager Override Enable. Values: 0x0 (OVERRIDE_DISABLE): Override Disable. Value of cmu_status.ipi_clk_off_st used. 0x1 (OVERRIDE_ENABLE): Override Enable. Value of reset_manager_config0.reset_manager_ipi_clk_value used. Value After Reset:0x0

HDMI TX Controller_RESET_MANAGER_STATUS0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes
29	RO	0x0	AVP_DATAPATH_VIDEO_AUDCLK_STATUS Status of the Video Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
28	RO	0x0	AVP_DATAPATH_VIDEO_LINKQPCLK_STATUS Status of the Video Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
27	RO	0x0	AVP_DATAPATH_VIDEO_VIDQPCLK_STATUS Status of the Video Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
26	RO	0x0	AVP_DATAPATH_VIDEO_IPI_CLK_STATUS Status of the Video Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
25	RO	0x0	AVP_DATAPATH_VIDEO_REFCLK_STATUS Status of the Video Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
24	RO	0x0	AVP_DATAPATH_AUDCLK_STATUS Status of the DATAPATH Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
23	RO	0x0	AVP_DATAPATH_LINKQPCLK_STATUS Status of the DATAPATH Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
22	RO	0x0	AVP_DATAPATH_VIDQPCLK_STATUS Status of the DATAPATH Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
21	RO	0x0	AVP_DATAPATH_IPI_CLK_STATUS Status of the DATAPATH Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
20	RO	0x0	AVP_DATAPATH_REFCLK_STATUS Status of the DATAPATH Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
19	RO	0x0	AVP_APB_PCLK_STATUS Status of the AVP Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
18	RO	0x0	AVP_AUDCLK_STATUS Status of the AVP Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
17	RO	0x0	AVP_LINKQPCLK_STATUS Status of the AVP Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
16	RO	0x0	AVP_VIDQPCLK_STATUS Status of the AVP Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
15	RO	0x0	AVP_IPI_CLK_STATUS Status of the AVP Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
14	RO	0x0	AVP_REFCLK_STATUS Status of the AVP Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
13	RO	0x0	MASTER_NOMAINRB_APB_PCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
12	RO	0x0	MASTER_NOMAINRB_EARC_BPCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at earc_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
11	RO	0x0	MASTER_NOMAINRB_AUDCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
10	RO	0x0	MASTER_NOMAINRB_LINKQPCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
9	RO	0x0	MASTER_NOMAINRB_VIDQPCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
8	RO	0x0	MASTER_NOMAINRB_IPI_CLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at ipi_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
7	RO	0x0	MASTER_NOMAINRB_REFCLK_STATUS Status of the MASTER_NOMAINRB Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
6	RO	0x0	MASTER_APB_PCLK_STATUS Status of the MASTER Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
5	RO	0x0	MASTER_EARC_BPCLK_STATUS Status of the MASTER Functional Group Init at earc_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
4	RO	0x0	MASTER_AUDCLK_STATUS Status of the MASTER Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
3	RO	0x0	MASTER_LINKQPCLK_STATUS Status of the MASTER Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
2	RO	0x0	MASTER_VIDQPCLK_STATUS Status of the MASTER Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
1	RO	0x0	MASTER_IPI_CLK_STATUS Status of the MASTER Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
0	RO	0x0	MASTER_REFCLK_STATUS Status of the MASTER Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

HDMI TX Controller_RESET_MANAGER_STATUS1
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved Field:Yes
28	RO	0x0	APB_REFCLK_STATUS Status of the APB Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
27	RO	0x0	APB_EARC_BPCLK_STATUS Status of the APB Functional Group Init at earc_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
26	RO	0x0	APB_AUDCLK_STATUS Status of the APB Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
25	RO	0x0	APB_LINKQPCLK_STATUS Status of the APB Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
24	RO	0x0	APB_VIDQPCLK_STATUS Status of the APB Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
23	RO	0x0	APB_IPI_CLK_STATUS Status of the APB Functional Group Init at ipi_clk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
22	RO	0x0	APB_APB_PCLK_STATUS Status of the APB Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
21	RO	0x0	EARCRX_CMDC_REFCLK_STATUS Status of the EARCRX_CMDC Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
20	RO	0x0	EARCRX_DMAC_EARC_BPCLK_STATUS Status of the EARCRX_DMAC Functional Group Init at earc_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
19	RO	0x0	EARCRX_CTRL_REFCLK_STATUS Status of the EARCRX_CTRL Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
18	RO	0x0	EARCRX_CTRL_EARC_BPCLK_STATUS Status of the EARCRX_CTRL Functional Group Init at earc_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
17	RO	0x0	EARCRX_APB_PCLK_STATUS Status of the EARCRX Functional Group Init at apb_pclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
16	RO	0x0	EARCRX_REFCLK_STATUS Status of the EARCRX Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
15	RO	0x0	EARCRX_EARC_BPCLK_STATUS Status of the EARCRX Functional Group Init at earc_bpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
14	RO	0x0	CEC_CTRL_REFCLK_STATUS Status of the CEC_CTRL Functional Group Init at refclk: Values: 0x0 (ASSERT): Init_n is asserted. 0x1 (NOT_ASSERT): Init_n is not asserted. Value After Reset:0x0
13	RO	0x0	CEC_REFCLK_STATUS Status of the CEC Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
12	RO	0x0	I2C_LINKQPCLK_STATUS Status of the I2C Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
11	RO	0x0	I2C_REFCLK_STATUS Status of the I2C Functional Group Init at refclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
10	RO	0x0	AVP_DATAPATH_PACKET_METADATA_VIDQPCLK_STATUS Status of the METADATA Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
9	RO	0x0	AVP_DATAPATH_PACKET_AUDIO_VIDQPCLK_STATUS Status of the AUDIO Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
8	RO	0x0	AVP_DATAPATH_PACKET_AUDIO_AUDCLK_STATUS Status of the AUDIO Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
7	RO	0x0	AVP_DATAPATH_PACKET_LINKQPCLK_STATUS Status of the PACKET Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
6	RO	0x0	AVP_DATAPATH_PACKET_AUDCLK_STATUS Status of the PACKET Functional Group Init at audclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
5	RO	0x0	AVP_DATAPATH_PACKET_VIDQPCLK_STATUS Status of the PACKET Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
4	RO	0x0	AVP_DATAPATH_HDCP_LINKQPCLK_STATUS Status of the HDCP Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
3	RO	0x0	AVP_DATAPATH_TMDS_LINKQPCLK_STATUS Status of the TMDS Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
2	RO	0x0	AVP_DATAPATH_TMDS_VIDQPCLK_STATUS Status of the TMDS Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
1	RO	0x0	AVP_DATAPATH_FRL_LINKQPCLK_STATUS Status of the FRL Functional Group Init at linkqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0
0	RO	0x0	AVP_DATAPATH_FRL_VIDQPCLK_STATUS Status of the FRL Functional Group Init at vidqpclk: Values: 0x0 (ASSERTED): Init_n is asserted. 0x1 (NOT_ASSERTED): Init_n is not asserted. Value After Reset:0x0

HDMI TX Controller_RESET_MANAGER_STATUS2

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4	RO	0x0	RESET_MANAGER_EARC_BPCLK_ON_STATUS Influence of earc_bpclk in Reset Manager: Values: 0x0 (CLK_OFF): The earc_bpclk is not used in Reset Manager. The logic at earc_bpclk is not affected by any init_n/disable. 0x1 (CLK_ON): The earc_bpclk is used in Reset Manager overlap function. Value After Reset:0x0
3	RO	0x0	RESET_MANAGER_AUDCLK_ON_STATUS Influence of audclk in Reset Manager: Values: 0x0 (CLK_OFF): The audclk is not used in Reset Manager. The logic at audclk is not affected by any init_n/disable. 0x1 (CLK_ON): The audclk is used in Reset Manager overlap function. Value After Reset:0x0
2	RO	0x0	RESET_MANAGER_LINKQPCLK_ON_STATUS Influence of linkqpclk in Reset Manager: Values: 0x0 (CLK_OFF): The linkqpclk is not used in Reset Manager. The logic at linkqpclk is not affected by any init_n/disable. 0x1 (CLK_ON): The linkqpclk is used in Reset Manager overlap function. Value After Reset:0x0
1	RO	0x0	RESET_MANAGER_VIDQPCLK_ON_STATUS Influence of vidqpclk in Reset Manager: Values: 0x0 (CLK_OFF): The vidqpclk is not used in Reset Manager. The logic at vidqpclk is not affected by any init_n/disable. 0x1 (CLK_ON): The vidqpclk is used in Reset Manager overlap function. Value After Reset:0x0
0	RO	0x0	RESET_MANAGER_IPI_CLK_ON_STATUS Influence of ipi_clk in Reset Manager: Values: 0x0 (CLK_OFF): The ipi_clk is not used in Reset Manager. The logic at ipi_clk is not affected by any init_n/disable. 0x1 (CLK_ON): The ipi_clk is used in Reset Manager overlap function. Value After Reset:0x0

HDMI TX Controller_TIMER_BASE_CONFIG0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved Field:Yes
28:0	RW	0x198b7b25	TIMER_REFERENCE_BASE Timer Reference Base, this represents the number of irefclk cycles in 1 second. This is the frequency of the refclk. Attention: This register is always consistent with input irefclk clock frequency. Example of configured value for irefclk of 428.571429 MHz is 29'd428571429. Value After Reset:0x198b7b25

HDMI TX Controller_TIMER_BASE_STATUS0

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	TIMER_BASE_LOCKED_ST Timer base locked status flag. Note: Writing a new Timer Reference Base to the register global_timer_ref_base initiates new Timer Base calculations. While these are in progress, this status is expected to fall momentaneously and when the calculations are finally done it is expected to rise, together with corresponding interrupt request timer_base_locked_irq. Values: 0x0 (NOT_LOCKED): Timer Base calculations in progress and not locked. 0x1 (LOCKED): Timer Base calculations completed and locked. Value After Reset:0x0

HDMI TX Controller_I2CM_SM_SCL_CONFIG0

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x085e	I2CM_SM_SCL_HIGH_CNT I2C Master Standard-mode SCL High Control Value After Reset:0x85e
15:0	RW	0x085e	I2CM_SM_SCL_LOW_CNT I2C Master Standard-mode SCL Low Control Value After Reset:0x85e

HDMI TX Controller_I2CM_FM_SCL_CONFIG0

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0217	I2CM_FM_SCL_HIGH_CNT I2C Master Fast-mode SCL High Control Value After Reset:0x217
15:0	RW	0x0217	I2CM_FM_SCL_LOW_CNT I2C Master Fast-mode SCL Low Control Value After Reset:0x217

HDMI TX Controller_I2CM_CONFIG0

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved1 Reserved Field:Yes
15:8	RW	0x00	I2CM_SDA_HOLD I2C Master SDA hold time Value After Reset:0x0
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x00	I2CM_RXFILTER_PULSE_WIDTH I2C Master Rx filter pulse width Value After Reset:0x0

HDMI TX Controller_I2CM_CONTROL0

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	I2CM_BUS_CLEAR_P I2C Master Bus Clear Value After Reset:0x0

HDMI TX Controller_I2CM_STATUS0

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	I2CM_ARB_LOST I2C Master arbitration lost Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_CONTROL0

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:20	RW	0x0	I2CM_NBYTES I2C Master Interface number of bytes minus 1 to read/write: Values: 0x0 (BYTES1): 1 byte to read/write 0x1 (BYTES2): 2 bytes to read/write 0x2 (BYTES3): 3 bytes to read/write 0x3 (BYTES4): 4 bytes to read/write 0x4 (BYTES5): 5 bytes to read/write 0x5 (BYTES6): 6 bytes to read/write 0x6 (BYTES7): 7 bytes to read/write 0x7 (BYTES8): 8 bytes to read/write 0x8 (BYTES9): 9 bytes to read/write 0x9 (BYTES10): 10 bytes to read/write 0xa (BYTES11): 11 bytes to read/write 0xb (BYTES12): 12 bytes to read/write 0xc (BYTES13): 13 bytes to read/write 0xd (BYTES14): 14 bytes to read/write 0xe (BYTES15): 15 bytes to read/write 0xf (BYTES16): 16 bytes to read/write Value After Reset:0x0
19:12	RW	0x00	I2CM_ADDR I2C Master Interface read/write address Value After Reset:0x0
11:5	RW	0x00	I2CM_SLVADDR I2C Master Interface slave address Value After Reset:0x0
4	RW	0x0	I2CM_EXT_READ I2C Master Interface extended read operation Value After Reset:0x0
3	RW	0x0	I2CM_SHORT_READ I2C Master Interface short read operation Value After Reset:0x0
2	RW	0x0	I2CM_READ I2C Master Interface read operation Value After Reset:0x0

Bit	Attr	Reset Value	Description
1	RW	0x0	I2CM_WRITE I2C Master Interface write operation Value After Reset:0x0
0	RW	0x0	I2CM_FM_EN I2C Master Interface Fast-mode enable Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_CONTROL1

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14:7	RW	0x00	I2CM_SEG_PTR I2C Master Interface extended read access segment pointer Value After Reset:0x0
6:0	RW	0x00	I2CM_SEG_ADDR I2C Master Interface extended read access segment address Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_0_3

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_3 I2C Master Interface SW write data, byte 3 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_2 I2C Master Interface SW write data, byte 2 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_1 I2C Master Interface SW write data, byte 1 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_0 I2C Master Interface SW write data, byte 0 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_4_7

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_7 I2C Master Interface SW write data, byte 7 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_6 I2C Master Interface SW write data, byte 6 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_5 I2C Master Interface SW write data, byte 5 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_4 I2C Master Interface SW write data, byte 4 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_8_11

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_11 I2C Master Interface SW write data, byte 11 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_10 I2C Master Interface SW write data, byte 10 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_9 I2C Master Interface SW write data, byte 9 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_8 I2C Master Interface SW write data, byte 8 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_WRDATA_12_15
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	I2CM_WRDATA_15 I2C Master Interface SW write data, byte 15 Value After Reset:0x0
23:16	RW	0x00	I2CM_WRDATA_14 I2C Master Interface SW write data, byte 14 Value After Reset:0x0
15:8	RW	0x00	I2CM_WRDATA_13 I2C Master Interface SW write data, byte 13 Value After Reset:0x0
7:0	RW	0x00	I2CM_WRDATA_12 I2C Master Interface SW write data, byte 12 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_0_3
Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_3 I2C Master Interface SW read data, byte 3 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_2 I2C Master Interface SW read data, byte 2 Value After Reset:0x0
15:8	RO	0x00	I2CM_RDDATA_1 I2C Master Interface SW read data, byte 1 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_0 I2C Master Interface SW read data, byte 0 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_4_7
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_7 I2C Master Interface SW read data, byte 7 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_6 I2C Master Interface SW read data, byte 6 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RO	0x00	I2CM_RDDATA_5 I2C Master Interface SW read data, byte 5 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_4 I2C Master Interface SW read data, byte 4 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_8_11

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_11 I2C Master Interface SW read data, byte 11 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_10 I2C Master Interface SW read data, byte 10 Value After Reset:0x0
15:8	RO	0x00	I2CM_RDDATA_9 I2C Master Interface SW read data, byte 9 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_8 I2C Master Interface SW read data, byte 8 Value After Reset:0x0

HDMI TX Controller_I2CM_INTERFACE_RDDATA_12_15

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	I2CM_RDDATA_15 I2C Master Interface SW read data, byte 15 Value After Reset:0x0
23:16	RO	0x00	I2CM_RDDATA_14 I2C Master Interface SW read data, byte 14 Value After Reset:0x0
15:8	RO	0x00	I2CM_RDDATA_13 I2C Master Interface SW read data, byte 13 Value After Reset:0x0
7:0	RO	0x00	I2CM_RDDATA_12 I2C Master Interface SW read data, byte 12 Value After Reset:0x0

HDMI TX Controller_SCDC_CONFIG0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved2 Reserved Field:Yes
12	RW	0x0	SCDC_I2C_FM_EN SCDC I2C Fast-mode enable Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes
7	RW	0x1	SCDC_UPD_FLAGS_RD_CLR_NBYTES SCDC Update Flags number of bytes minus 1 to read/clear: Values: 0x0 (BYTES1): 1 byte to read/clear 0x1 (BYTES2): 2 bytes to read/clear Value After Reset:0x1

Bit	Attr	Reset Value	Description
6	RW	0x0	SCDC_UPD_FLAGS_AUTO_CLR SCDC Update Flags auto clear on read Value After Reset:0x0
5	RW	0x0	SCDC_UPD_FLAGS_POLL_CONT SCDC Update Flags Polling continuously Value After Reset:0x0
4	RW	0x0	SCDC_UPD_FLAGS_POLL_EN SCDC Update Flags Polling enable Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	SCDC_RR_REPLY_STOP SCDC Read Request reply with STOP Value After Reset:0x0
0	RW	0x0	SCDC_RR_EN SCDC Read Request enable Value After Reset:0x0

HDMI TX Controller_SCDC_CONTROL0
Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	WO	0x0	SCDC_UPD_FLAGS_CLR_P SCDC Update Flags clear request Value After Reset:0x0
0	WO	0x0	SCDC_UPD_FLAGS_RD_P SCDC Update Flags read request Value After Reset:0x0

HDMI TX Controller_SCDC_STATUS0
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:8	RO	0x00	SCDC_UPD_FLAGS_1 SCDC Update Flags 1 Value After Reset:0x0
7:0	RO	0x00	SCDC_UPD_FLAGS_0 SCDC Update Flags 0 Value After Reset:0x0

HDMI TX Controller_FLT_CONFIG0
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes
8	RW	0x0	FLT_NO_TIMEOUT FRL Link Training FLT_no_timeout Source Test Configuration Register Value After Reset:0x0
7:4	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
3:0	RW	0x0	FLT_FFE_LEVELS FRL Link Training FFE Levels Value After Reset:0x0

HDMI TX Controller_FLT_CONFIG1

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:16	RW	0x0	FLT_LTP_LANE3_OVR_VALUE Link Training Pattern to apply on Lane 3 override value Value After Reset:0x0
15:12	RW	0x0	FLT_LTP_LANE2_OVR_VALUE Link Training Pattern to apply on Lane 2 override value Value After Reset:0x0
11:8	RW	0x0	FLT_LTP_LANE1_OVR_VALUE Link Training Pattern to apply on Lane 1 override value Value After Reset:0x0
7:4	RW	0x0	FLT_LTP_LANE0_OVR_VALUE Link Training Pattern to apply on Lane 0 override value Value After Reset:0x0
3	RW	0x0	FLT_LTP_LANE3_OVR_EN Link Training Pattern to apply on Lane 3 override enable Value After Reset:0x0
2	RW	0x0	FLT_LTP_LANE2_OVR_EN Link Training Pattern to apply on Lane 2 override enable Value After Reset:0x0
1	RW	0x0	FLT_LTP_LANE1_OVR_EN Link Training Pattern to apply on Lane 1 override enable Value After Reset:0x0
0	RW	0x0	FLT_LTP_LANE0_OVR_EN Link Training Pattern to apply on Lane 0 override enable Value After Reset:0x0

HDMI TX Controller_FLT_CONFIG2

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:16	RW	0x0	FLT_TXFFE_LANE3_OVR_VALUE Link Training TxFFE setting to apply on Lane 3 override value Value After Reset:0x0
15:12	RW	0x0	FLT_TXFFE_LANE2_OVR_VALUE Link Training TxFFE setting to apply on Lane 2 override value Value After Reset:0x0
11:8	RW	0x0	FLT_TXFFE_LANE1_OVR_VALUE Link Training TxFFE setting to apply on Lane 1 override value Value After Reset:0x0
7:4	RW	0x0	FLT_TXFFE_LANE0_OVR_VALUE Link Training TxFFE setting to apply on Lane 0 override value Value After Reset:0x0
3	RW	0x0	FLT_TXFFE_LANE3_OVR_EN Link Training TxFFE setting to apply on Lane 3 override enable Value After Reset:0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	FLT_TXFFE_LANE2_OVR_EN Link Training TxFFE setting to apply on Lane 2 override enable Value After Reset:0x0
1	RW	0x0	FLT_TXFFE_LANE1_OVR_EN Link Training TxFFE setting to apply on Lane 1 override enable Value After Reset:0x0
0	RW	0x0	FLT_TXFFE_LANE0_OVR_EN Link Training TxFFE setting to apply on Lane 0 override enable Value After Reset:0x0

HDMI TX Controller_FLT_CONTROL0

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	FLT_START_P FRL Link Training LTS:3 start Value After Reset:0x0

HDMI TX Controller_MAINUNIT_STATUS0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	EARC_BPCLK_VALID_STABLE_ST eARC RX Biphase clock valid change interrupt status. Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_CONFIG0

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved0 Reserved Field:Yes
28	RW	0x0	VESA_DSC_48BITS_OVR_VALUE VESA DSC 48bits override value Value After Reset:0x0
27	RW	0x0	VESA_DSC_24BITS_OVR_VALUE VESA DSC 24bits override value Value After Reset:0x0
26:24	RW	0x0	HDMI_VIDEO_FORMAT_OVR_VALUE Video Format override value Value After Reset:0x0
23:20	RW	0x0	HDMI_COLOR_DEPTH_OVR_VALUE Color depth override value Value After Reset:0x0
19	RW	0x0	IPI_MAP_ENDIANNESS_OVR_VALUE Bit endianness of each mapped byte Values: 0x0 (LITTLE_ENDIAN): little-endian 0x1 (BIG_ENDIAN): big-endian Value After Reset:0x0
18:16	RW	0x0	IPI_MAP_BYTE5_OVR_VALUE Internal video vector where IPI byte 5 is mapped Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:13	RW	0x0	IPI_MAP_BYTE4_OVR_VALUE Internal video vector where IPI byte 4 is mapped Value After Reset:0x0
12:10	RW	0x0	IPI_MAP_BYTE3_OVR_VALUE Internal video vector where IPI byte 3 is mapped Value After Reset:0x0
9:7	RW	0x0	IPI_MAP_BYTE2_OVR_VALUE Internal video vector where IPI byte 2 is mapped Value After Reset:0x0
6:4	RW	0x0	IPI_MAP_BYTE1_OVR_VALUE Internal video vector where IPI byte 1 is mapped Value After Reset:0x0
3:1	RW	0x0	IPI_MAP_BYTE0_OVR_VALUE Internal video vector where IPI byte 0 is mapped Value After Reset:0x0
0	RW	0x0	IPI_MAP_OVR_EN IPI mapping override mechanism enable Values: 0x0 (OVERRIDE_OFF): No override mechanism 0x1 (OVERRIDE_ON): Override mechanism enabled Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_CONFIG2

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	RW	0x0	IPI_DESERIALIZER_EN IPI Deserializer configuration Values: 0x0 (DISABLE): IPI Data received in 4 buses (deserialization disabled) 0x1 (ENABLE): IPI Data Serialized and received only in interface 0 Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	VID_FIFO_INIT_ON_OVF Video Interface FIFO Init on overflow configuration Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_CONTROL0

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	VID_FIFO_CLR_P Video Interface FIFO clear Value After Reset:0x0

HDMI TX Controller_VIDEO_INTERFACE_STATUS0

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
18	RO	0x0	HSYNC_POLARITY Detected Hsync polarity status Values: 0x0 (HSYNC_NEG): Hsync pulse is active low 0x1 (HSYNC_POS): Hsync pulse is active high Value After Reset:0x0
17	RO	0x0	VSYNC_POLARITY Detected Vsync polarity status Values: 0x0 (VSYNC_NEG): Vsync pulse is active low 0x1 (VSYNC_POS): Vsync pulse is active high Value After Reset:0x0
16	RO	0x0	VESA_DSC_48BIT VESA DSC 48bit video mode Values: 0x0 (VESADSC48_NOT): VESA DSC 48bit video mode not in use 0x1 (VESADSC48_DET): VESA DSC 48bit video mode detected Value After Reset:0x0
15	RO	0x0	VESA_DSC_24BIT VESA DSC 24bit video mode Values: 0x0 (VESADSC24_NOT): VESA DSC 24bit video mode not in use 0x1 (VESADSC24_DET): VESA DSC 24bit video mode detected Value After Reset:0x0
14:12	RO	0x0	HDMI_VIDEO_FORMAT Video Format status Value After Reset:0x0
11:8	RO	0x0	HDMI_COLOR_DEPTH Color depth in use in HDMI Value After Reset:0x0
7:4	RO	0x0	IPI_COLOR_DEPTH Detected IPI color depth Value After Reset:0x0
3:0	RO	0x0	IPI_FORMAT IPI format Value After Reset:0x0

HDMI TX Controller_VIDEO_PACKING_CONFIG0
Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	GCP_DEFAULT_PHASE GCP Default_Phase selector (only applicable for 30bits or 36 bits) Values: 0x0 (DP0): Default Phase 0 0x1 (DP1): Default Phase 1 Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_CONFIG0
Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved4 Reserved Field:Yes

Bit	Attr	Reset Value	Description
28	RW	0x0	PAI_DISABLE_SAMPLE_PRESENT_LEFT PAI interface disable automatic sample present assertion for left-only channels Values: 0x0 (SP_PAI_LEFT_EN): Sample present is asserted for PAI Interface when left-only channel is received 0x1 (SP_PAI_LEFT_DIS): Sample present is not asserted for PAI Interface when left-only channel is received Value After Reset:0x0
27	RW	0x0	PAI_FORMAT_OVR_EN PAI interface format override enable Values: 0x0 (PAI_FRMT_OVR_DIS): PAI interface input audio format is used 0x1 (PAI_FRMT_OVR_EN): PAI interface input audio format is overriden to follow the value of 'aud_format' field Value After Reset:0x0
26:24	RW	0x0	AUD_FORMAT Audio Format: Values: 0x0 (AUD_ASP): Audio Sample (L-PCM and IEC 61937 compressed formats) 0x1 (AUD_OBA): One Bit Audio Sample Packet 0x2 (AUD_DST): DST Audio Packet 0x3 (AUD_HBR): High Bitrate (HBR) Audio Stream Packet (IEC 61937) - only valid when the configuration parameter HDMI_QP_TX_AUD_HBR is set 0x4 (AUD_MSASP): Multi-Stream Audio Sample Packet (L-PCM and IEC 61937 compressed formats) - only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set 0x5 (AUD_MSOBA): One-Bit Multi-Stream Audio Sample Packet - only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set 0x6 (AUD_3DASP): 3D Audio Sample Packet (L-PCM format only) - only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set 0x7 (AUD_3DOBA): One Bit 3D Audio Sample Packet - only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set Value After Reset:0x0
23:22	RW	0x0	Reserved3 Reserved Field:Yes
21:20	RW	0x0	SPDIF_PAIR_SEL SPDIF interface pair used to sample data Value After Reset:0x0
19:16	RW	0x0	SPDIF_LINES_EN SPDIF interface lines enable. Value After Reset:0x0
15:14	RW	0x0	Reserved2 Reserved Field:Yes
13	RW	0x0	I2S_BBIT_RIGHT I2S interface B bit selection Values: 0x0 (BBIT_L): B bit taken from left channel 0x1 (BBIT_R): B bit taken from right channel Value After Reset:0x0

Bit	Attr	Reset Value	Description
12	RW	0x0	I2S_BPCUV_EN I2S interface BPCUV insertion enable Values: 0x0 (BPCUV_RCV_DIS): BPCUV bits not received through the interface 0x1 (BPCUV_RCV_EN): BPCUV bits received through the interface Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes
7:4	RW	0x0	I2S_LINES_EN I2S interface lines enable. Value After Reset:0x0
3	RW	0x0	Reserved0 Reserved Field:Yes
2	RW	0x0	AUDFIFO_INIT_ON_OVF Audio FIFO init on overflow Value After Reset:0x0
1:0	RW	0x0	AUD_IF_SEL Audio Interface selection Note 1: Others values not listed default to 0 Values: 0x0 (PAI): PAI interface selection 0x1 (I2S): I2S interface selection 0x2 (SPDIF): SPDIF interface selection Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_CONFIG1

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved1 Reserved Field:Yes
28	RW	0x0	PAI_CHANNELSPREAD_THRESHOLD_OVR_EN PAI Interface channel spread threshold override enable Values: 0x0 (PAI_CHTHR_OVR_DIS): Uses PAI interface threshold configuration 0x1 (PAI_CHTHR_OVR_EN): Channel Spread Threshold override enabled, value from 'pai_channelspread_threshold_ovr_value' is used Value After Reset:0x0
27:20	RW	0x00	PAI_CHANNELSPREAD_THRESHOLD_OVR_VALUE PAI Interface channel threshold value override Value After Reset:0x0
19	RW	0x0	PAI_CHANNELSPREAD_DETECTED_OVR_EN PAI Interface channel spread detection override enable Values: 0x0 (PAI_CHSPREAD_OVR_DIS): Channel spread detected by PAI interface 0x1 (PAI_CHSPREAD_OVR_EN): Channel spread override enabled, value from 'pai_channelspread_detected_ovr_value' is used Value After Reset:0x0

Bit	Attr	Reset Value	Description
18	RW	0x0	PAI_CHANNELSPREAD_DETECTED_OVR_VALUE PAI Interface channel spread detection override Values: 0x0 (PAI_CHSPREAD_DIS): Channel spread disabled 0x1 (PAI_CHSPREAD_EN): Channel spread enabled Value After Reset:0x0
17	RW	0x0	Reserved0 Reserved Field:Yes
16	RW	0x0	PAI_PAIR_LAYOUT_OVR_EN PAI Interface pair layout override enable Values: 0x0 (PAI_PAIR_LAY_OVR_DIS): Pair layout determined by received pairs 0x1 (PAI_PAIR_LAY_OVR_EN): Pair layout override enabled, value from 'pai_pair_layout_ovr_value' is used Value After Reset:0x0
15:0	RW	0x0000	PAI_PAIR_LAYOUT_OVR_VALUE PAI Interface pair layout override Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_CONTROL0

Address: Operational Base + offset (0x082C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	AUDFIFO_CLR_P Audio FIFO clear Value After Reset:0x0

HDMI TX Controller_AUDIO_INTERFACE_STATUS0

Address: Operational Base + offset (0x0834)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23	RO	0x0	SPDIF_LINE3_LOCK S/PDIF Line 3 audio lock Values: 0x0 (SPDIF_LINE3_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE3_AUD_OK): Lane receiving audio correctly Value After Reset:0x0
22	RO	0x0	SPDIF_LINE2_LOCK S/PDIF Line 2 audio lock Values: 0x0 (SPDIF_LINE2_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE2_AUD_OK): Lane receiving audio correctly Value After Reset:0x0
21	RO	0x0	SPDIF_LINE1_LOCK S/PDIF Line 1 audio lock Values: 0x0 (SPDIF_LINE1_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE1_AUD_OK): Lane receiving audio correctly Value After Reset:0x0

Bit	Attr	Reset Value	Description
20	RO	0x0	SPDIF_LINE0_LOCK S/PDIF Line 0 audio lock Values: 0x0 (SPDIF_LINE0_AUD_NOK): Lane not receiving audio correctly 0x1 (SPDIF_LINE0_AUD_OK): Lane receiving audio correctly Value After Reset:0x0
19	RO	0x0	PAI_CHANNELSPREAD_DETECTED PAI channel spread detection: Values: 0x0 (PAI_CHSPREAD_DET_DIS): Channel spread disabled 0x1 (PAI_CHSPREAD_DET_EN): Channel spread enabled Value After Reset:0x0
18:16	RO	0x0	PAI_FORMAT PAI format status: Values: 0x0 (AUDPKT_TYPE_0X02): Audio sample 0x1 (AUDPKT_TYPE_0X07): One bit audio 0x2 (AUDPKT_TYPE_0X08): DST audio 0x3 (AUDPKT_TYPE_0X09): HBR audio (only valid when the configuration parameter HDMI_QP_TX_AUD_HBR is set) 0x4 (AUDPKT_TYPE_0X0e): MSA audio (only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set) 0x5 (AUDPKT_TYPE_0X0f): OBM audio (only valid when the configuration parameter HDMI_QP_TX_AUD_MS is set) 0x6 (AUDPKT_TYPE_0X0b): 3D audio sample (only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set) 0x7 (AUDPKT_TYPE_0X0c): 3D One bit audio (only valid when the configuration parameter HDMI_QP_TX_AUD_3D is set) Value After Reset:0x0
15:0	RO	0x0000	PAIR_LAYOUT Audio pair layout status Note: This register field only takes values greater than 15 when Audio 3D features are present in the configuration (HDMI_QP_TX_AUD_3D == 1) Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG0

Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:28	RW	0x4	EXTCTL_SPACING_SEL Maximum spacing between Extended Control Periods, set in ms. Note: The HDMI specification defines a maximum spacing (tEXTS,max_delay) of 50ms between Extended Control Periods. Values: 0x0 (ECP5ms): 5ms 0x1 (ECP10ms): 10ms 0x2 (ECP15ms): 15ms 0x3 (ECP20ms): 20ms 0x4 (ECP25ms): 25ms 0x5 (ECP30ms): 30ms 0x6 (ECP35ms): 35ms 0x7 (ECP40ms): 40ms 0x8 (ECP42ms): 42ms 0x9 (ECP45ms): 45ms 0xa (ECP46ms): 46ms 0xb (ECP47ms): 47ms 0xc (ECP48ms): 48ms 0xd (ECP49ms): 49ms 0xe (ECP50ms): 50ms 0xf (ECP55ms): 55ms Value After Reset:0x4
27	RW	0x0	Reserved2 Reserved Field:Yes
26:20	RW	0x20	EXTCTL_DURATION Extended Control Period duration, set in TMDS clock cycles (nominal pixels) This field can be set from 0 (disabled) to 127 clock cycles. Note: The HDMI specification defines a minimum (tEXTS,min) of 32 clock cycles for Extended Control Period duration. Value After Reset:0x20
19:6	RW	0x0000	Reserved1 Reserved Field:Yes
5:4	RW	0x0	MTW_FREQ_CFG Metadata Transmission Window - MTW Frequency configuration Values: 0x0 (MTW_FRAME): MTW is repeated every Frame 0x1 (MTW_FIELD): MTW is repeated every Field 0x2 (MTW_VBLANK): MTW is repeated every Vertical Blanking 0x3 (MTW_RES): Reserved Value After Reset:0x0

Bit	Attr	Reset Value	Description
3	RW	0x0	VIDEO_MEAS_OVR_EN Video Measures Override enable The following fields are used when the override mode is enabled: video_hfront_ovr_value video_hsyncwidth_ovr_value video_hback_ovr_value video_hblank_ovr_value video_hactive_ovr_value video_htotal_ovr_value video_vfront_ovr_value video_vsyncwidth_ovr_value video_vback_ovr_value video_vblank_ovr_value video_vactive_ovr_value video_vtotal_ovr_value Values: 0x0 (VIDMEAS_OVR_DIS): Video measures are performed by the internal Video Monitor block 0x1 (VIDMEAS_OVR_EN): Video measures are set by the fields video_*_ovr_value of registers frame_composer_config* Value After Reset:0x0
2	RW	0x0	SCRAMBLER_UCP_LINE Scrambler Unscrambled Control Period per line enable. This is a debug feature for testing proposes only. In normal operation it shall always be disabled. Values: 0x0 (NORMAL_UCP): Unscrambled Control Period per video field 0x1 (LINE_UCP): Unscrabled Control Period per line Value After Reset:0x0
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	FAPA_START_LOCATION FAPA_start_location value from E-EDID HF-VSDB This field shall be set from SW when it reads the E-EDID from the Sink device, with the value of bit 'FAPA_start_location' in HF-VSDB byte 8, bit 0. The FAPA region is the only allowed frame region for transmission of EMP - Extended Metadata Packets belonging to a Data Set with Sync=1. Value After Reset:0x0

HDMI TX Controller FRAME COMPOSER CONFIG1

Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:20	RW	0xfff	MAX_PACKETS_BLANK Maximum number of Data Island packets in a non-active video line (video blanking line) - 0 : No packets are transmitted - 1 : Number of packets limited to 1 - ... - 4094 : Number of packets limited to 4094 - 4095 : Unlimited number of packets, when configured value has all bits set (=1) Value After Reset:0xfff

Bit	Attr	Reset Value	Description
19:16	RW	0x0	Reserved1 Reserved Field:Yes
15:8	RW	0xff	MAX_PACKETS_ACTIVE Maximum number of Data Island packets in an active video line - 0 : No packets are transmitted - 1 : Number of packets limited to 1 - ... - 254 : Number of packets limited to 254 - 255 : Unlimited number of packets, when configured value has all bits set (=1) Value After Reset:0xff
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_FRAME_COMPOSER_CONFIG2

Address: Operational Base + offset (0x0848)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_HSYNCWIDTH_OVR_VALUE Video Hsync width override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_HFRONT_OVR_VALUE Video Hfront override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG3

Address: Operational Base + offset (0x084C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_HBLANK_OVR_VALUE Video Hblank override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_HBACK_OVR_VALUE Video Hback override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG4

Address: Operational Base + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_HTOTAL_OVR_VALUE Video Htotal override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_HACTIVE_OVR_VALUE Video Hactive override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG5

Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_VSYNCWIDTH_OVR_VALUE Video Vsync width override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_VFRONT_OVR_VALUE Video Vfront override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller FRAME COMPOSER CONFIG6

Address: Operational Base + offset (0x0858)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_VBLANK_OVR_VALUE Video Vblank override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_VBACK_OVR_VALUE Video Vback override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller FRAME COMPOSER CONFIG7

Address: Operational Base + offset (0x085C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VIDEO_VTOTAL_OVR_VALUE Video Vtotal override value Only used when video_meas_ovr_en=1 Value After Reset:0x0
15:0	RW	0x0000	VIDEO_VACTIVE_OVR_VALUE Video Vactive override value Only used when video_meas_ovr_en=1 Value After Reset:0x0

HDMI TX Controller FRAME COMPOSER CONFIG8

Address: Operational Base + offset (0x0860)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved Field:Yes
17:16	RW	0x1	KEEPOUT_WOO_CFG Configure when to enable the Keepout period for the HDCP Window of Opportunity. The start and end time for the keepout period are the same for all Enabled configurations. Note: When keepout_hdcp_authenticated_ovr_en=1, the HDCP Authenticated state is given by field keepout_hdcp_authenticated_ovr_val Values: 0x0 (KEEPOUT_WOO_DIS): Keepout period disabled. 0x1 (KEEPOUT_WOO_AUTH_FRL): Keepout period enabled when in FRL mode or HDCP is authenticated. 0x2 (KEEPOUT_WOO_ALWAYS): Keepout period always enabled. 0x3 (KEEPOUT_WOO_RSV): Reserved, don't use. Value After Reset:0x1

Bit	Attr	Reset Value	Description
15:8	RW	0x00	KEEPOUT_WOO_END_MARGIN Keepout period for the HDCP Window of Opportunity - End margin The keepout period end shall be (650 + keepout_woo_end_margin) tribytes from the active edge of Vsync Value After Reset:0x0
7:0	RW	0x00	KEEPOUT_WOO_START_MARGIN Keepout period for the HDCP Window of Opportunity - Start margin The keepout period start shall be (508 - keepout_woo_start_margin) tribytes from the active edge of Vsync Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONFIG9

Address: Operational Base + offset (0x0864)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved0 Reserved Field:Yes
9:8	RW	0x1	KEEPOUT_REKEY_CFG Configure when to enable the Keepout period for the HDCP14 hdcpRekeyCipher operation. The start and end time for the keepout period are the same for all Enabled configurations. Note: When keepout_hdcp_authenticated_ovr_en=1, the HDCP Authenticated state is given by field keepout_hdcp_authenticated_ovr_val Values: 0x0 (KEEPOUT_REKEY_DIS): Keepout period disabled. 0x1 (KEEPOUT_REKEY_AUTH): Keepout period enabled when HDCP is authenticated. 0x2 (KEEPOUT_REKEY_ALWAYS): Keepout period always enabled. 0x3 (KEEPOUT_REKEY_RSV): Reserved, don't use. Value After Reset:0x1
7:0	RW	0x00	KEEPOUT_REKEY_END_MARGIN Keepout period for the HDCP14 hdcpRekeyCipher operation - End margin The keepout period end shall be (58 + keepout_rekey_end_margin) tribytes from the end of each active video period Value After Reset:0x0

HDMI TX Controller_FRAME_COMPOSER_CONTROL0

Address: Operational Base + offset (0x086C)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x0	KEEPOUT_HDCP_AUTH_OVR_VALUE Override Value for the HDCP authenticated state, used only for controlling Keepout periods Values: 0x0 (KEEPOUT_NOTAUTH): HDCP Not Authenticated 0x1 (KEEPOUT_AUTH): HDCP Authenticated Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	KEEPOUT_HDCP_AUTH_OVR_EN Override Enable for the HDCP authenticated state, used only for controlling Keepout periods Values: 0x0 (KEEPOUT_AUTH_OVR_DIS): Disabled 0x1 (KEEPOUT_AUTH_OVR_EN): Enabled Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_CONFIG0

Address: Operational Base + offset (0x0880)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved0 Reserved Field:Yes
9	RW	0x0	VMON_IRQ_VACTIVE_EN Video monitor interrupt on Vactive change enable Value After Reset:0x0
8	RW	0x0	VMON_IRQ_VBACK_EN Video monitor interrupt on Vback change enable Value After Reset:0x0
7	RW	0x0	VMON_IRQ_VSYNCWIDTH_EN Video monitor interrupt on Vsync width change enable Value After Reset:0x0
6	RW	0x0	VMON_IRQ_VFRONT_EN Video monitor interrupt on Vfront change enable Value After Reset:0x0
5	RW	0x0	VMON_IRQ_VTOTAL_EN Video monitor interrupt on Vtotal change enable Value After Reset:0x0
4	RW	0x0	VMON_IRQ_HACTIVE_EN Video monitor interrupt on Hactive change enable Value After Reset:0x0
3	RW	0x0	VMON_IRQ_HBACK_EN Video monitor interrupt on Hback change enable Value After Reset:0x0
2	RW	0x0	VMON_IRQ_HSYNCWIDTH_EN Video monitor interrupt on Hsync width change enable Value After Reset:0x0
1	RW	0x0	VMON_IRQ_HFRONT_EN Video monitor interrupt on Hfront change enable Value After Reset:0x0
0	RW	0x0	VMON_IRQ_HTOTAL_EN Video monitor interrupt on Htotal change enable Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS0

Address: Operational Base + offset (0x0884)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_HSYNCWIDTH Video monitor measured Hsync width Value After Reset:0x0
15:0	RO	0x0000	VMON_HFRONT Video monitor measured Hfront Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS1

Address: Operational Base + offset (0x0888)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_HBLANK Video monitor measured Hblank Value After Reset:0x0
15:0	RO	0x0000	VMON_HBACK Video monitor measured Hback Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS2

Address: Operational Base + offset (0x088C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_HTOTAL Video monitor measured Htotal Value After Reset:0x0
15:0	RO	0x0000	VMON_HACTIVE Video monitor measured Hactive Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS3

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_VSYNCWIDTH Video monitor measured Vsync width Value After Reset:0x0
15:0	RO	0x0000	VMON_VFRONT Video monitor measured Vfront Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS4

Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_VBLANK Video monitor measured Vblank Value After Reset:0x0
15:0	RO	0x0000	VMON_VBACK Video monitor measured Vback Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS5

Address: Operational Base + offset (0x0898)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	VMON_VTOTAL Video monitor measured Vtotal Value After Reset:0x0
15:0	RO	0x0000	VMON_VACTIVE Video monitor measured Vactive Value After Reset:0x0

HDMI TX Controller_VIDEO_MONITOR_STATUS6

Address: Operational Base + offset (0x089C)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
1	RO	0x0	VMON_ILACE_DETECT Video Monitor - Interlaced Video mode detected Value After Reset:0x0
0	RO	0x0	VMON_ALT_DETECT Video Monitor - Field Alternative video mode detected Value After Reset:0x0

HDMI TX Controller_HDCP2LOGIC_CONFIG0

Address: Operational Base + offset (0x08E0)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes
4	RW	0x0	HDCP2_OPMODE_OVR_VALUE OPMODE Override Value Values: 0x0 (OPMODE_TMDS): The OPMODE indication is set to 1'b0, meaning the TMDS Mode. 0x1 (OPMODE_FRL): The AVMUTE indication is set to 1'b1, meaning the FRL Mode. Value After Reset:0x0
3	RW	0x0	HDCP2_OPMODE_OVR_EN OPMODE Override Enable Values: 0x0 (OVERRIDE_OFF): The OPMODE indication is defined internaly. 0x1 (OVERRIDE_ON): The OPMODE indication is overriden by the hdcp2_opmode_ovr_value field. Value After Reset:0x0
2	RW	0x0	HDCP2_AVMUTE_OVR_VALUE AVMUTE Override Value Values: 0x0 (AVMUTE_OFF): The AVMUTE indication is set to 1'b0. 0x1 (AVMUTE_ON): The AVMUTE indication is set to 1'b1. Value After Reset:0x0
1	RW	0x0	HDCP2_AVMUTE_OVR_EN AVMUTE Override Enable Values: 0x0 (OVERRIDE_OFF): The AVMUTE indication is defined internaly. 0x1 (OVERRIDE_ON): The AVMUTE indication is overriden by the hdcp2_avmute_ovr_value field. Value After Reset:0x0
0	RW	0x0	HDCP2_BYPASS Internal Bypass of HDCP2. Values: 0x0 (BYPASS_OFF): The video datapath goes through the External HDCP2 Module. 0x1 (BYPASS_ON): The video datapath bypasses the External HDCP2 Module. Value After Reset:0x0

HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_IN

Address: Operational Base + offset (0x08E4)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:4	RW	0x0	HDCP2_ESM_P0_GPIO_IN Port 0 General-Purpose inputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0
3:0	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_IN Global General-Purpose inputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0

HDMI TX Controller_HDCP2LOGIC_ESM_GPIO_OUT

Address: Operational Base + offset (0x08E8)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:4	RO	0x0000	HDCP2_ESM_P0_GPIO_OUT Port 0 General-Purpose outputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0
3:0	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT Global General-Purpose outputs to the HDCP2 ESM block - For more information, see the ESM Databook. The bit mapping is equivalent to the ESM Databook definition. Value After Reset:0x0

HDMI TX Controller_HDCP14_CONFIG0

Address: Operational Base + offset (0x0900)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved1 Reserved Field:Yes
30:23	RW	0x00	HDCP14_PREWOO_OVR_VALUE Number of clock cycles between the VSYNC active edge and the start of Window of Opportunity (Divided by 4) Needs the hdcp14_prewoo_ovr_en active. Value After Reset:0x0
22	RW	0x0	HDCP14_PREWOO_OVR_EN Window of Oportunity Start Override Enable Value After Reset:0x0
21:19	RW	0x0	Reserved0 Reserved Field:Yes
18	RW	0x0	HDCP14_RI_READ_MODE Ri Read Mode: Values: 0x0 (RI_RDMODE_128_FRAMES): Trigered every 128 Frames. 0x1 (RI_RDMODE_2_SECONDS): Trigered every 2 seconds. Value After Reset:0x0
17:15	RW	0x2	HDCP14_OESS_CTL3_PULSE_SIZE Duration of the CTL3 bit definition when in OESS mode. Note 1: The value must be devided by 4. Value After Reset:0x2

Bit	Attr	Reset Value	Description
14	RW	0x0	HDCP14_OESS_ESSS_OVR_VALUE EESS/OESS Override Value: Values: 0x0 (OESS): OESS 0x1 (EESS): EESS Value After Reset:0x0
13	RW	0x0	HDCP14_OESS_ESSS_OVR_EN EESS/OESS Override Enable Value After Reset:0x0
12	RW	0x0	HDCP14_AN_BYPASS An value definition: Values: 0x0 (AN_VALUE_HW): The An value is retrieved from the HDCP14 Cipher. 0x1 (AN_VALUE_SW): The An value is defined by the an_value register. Value After Reset:0x0
11	RW	0x0	HDCP14_AN_CIPHER_INPUT Chipher Input for An value calculation: Values: 0x0 (AN_CIPHER_HW): The Input of HDCP14 Cipher is connected directly from his outputs. 0x1 (AN_CIPHER_SW): The Input of HDCP14 Cipher is connected to an_value register. Value After Reset:0x0
10	RW	0x0	HDCP14_KEY_DECRYPT_EN HDCP Key Encryption enable: Values: 0x0 (HDCP_KEY_NONENC): HDCP Key is not encrypted. 0x1 (HDCP_KEY_ENC): HDCP Key is encrypted. Value After Reset:0x0
9	RW	0x0	HDCP14_FEATURES11_ENABLE Enable 1.1 Features for HDCP14. This option will only be applied if the connected HDCP Receiver also has the 1.1 Features Enabled. Value After Reset:0x0
8:5	RW	0x0	HDCP14_I2C_NACK_THRESHOLD Number of received I2C NACKs until the HDCP Transmitter became unauthenticated. If set to 4'b0, this check is disabled and the HDCP Transmitter never gets unauthenticated by the I2C NACK. Value After Reset:0x0
4	RW	0x0	HDCP14_I2C_SHORT_READ_DISABLE Disable I2C Short Read for HDCP14 Operations. Value After Reset:0x0
3	RW	0x0	HDCP14_I2C_FASTMODE Enable I2C Fast Mode for HDCP14 Operations. This option will only be applied if the connected HDCP Receiver also has the I2C Fast Mode Enabled. Value After Reset:0x0
2	RW	0x0	HDCP14_ENCRYPTION_ENABLE Encryption Enable Value After Reset:0x0

Bit	Attr	Reset Value	Description
1	RW	0x0	HDCP14_BYPASS HDCP 14 Bypass Value After Reset:0x0
0	RW	0x0	HDCP14_HPD HDCP 14 HDP Value After Reset:0x0

HDMI TX Controller_HDCP14_CONTROL0

Address: Operational Base + offset (0x0904)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	WO	0x0	HDCP14_SHA1_MSG_FAIL_P Software Indication that the SHA-1 Message failed. Value After Reset:0x0
3	WO	0x0	HDCP14_SHA1_MSG_CORRECT_P Software Indication that the SHA-1 Message was correctly digested. Value After Reset:0x0
2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	HDCP14_KSV_LIST_REVOCATED_P Software Indication that the KSV List was revocated. Value After Reset:0x0
0	WO	0x0	HDCP14_RESTART_P Restart HDCP14 Value After Reset:0x0

HDMI TX Controller_HDCP14_CONFIG1

Address: Operational Base + offset (0x0908)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved Field:Yes
27:19	RW	0x000	HDCP14_READY_TIMER_OVR_VALUE READY bit Timer Limit Limit Override Value The defined override value is in an 10ms timebase. Value After Reset:0x0
18	RW	0x0	HDCP14_READY_TIMER_OVR_EN READY bit Timer Limit Override Enable Value After Reset:0x0
17:16	RW	0x0	Reserved1 Reserved Field:Yes
15:8	RW	0x00	HDCP14_RI_TIMER_OVR_VALUE Ri Verification Timer Limit Override Value The defined override value is in an 10ms timebase. Value After Reset:0x0
7	RW	0x0	HDCP14_RI_TIMER_OVR_EN Ri Verification Timer Limit Override Enable Value After Reset:0x0
6:5	RW	0x0	Reserved0 Reserved Field:Yes
4:1	RW	0x0	HDCP14_R0_TIMER_OVR_VALUE R0 waiting Timer Limit Override Value The defined override value is in a 10ms base. Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	HDCP14_R0_TIMER_OVR_EN R0 waiting Timer Limit Override Enable Value After Reset:0x0

HDMI TX Controller_HDCP14_CONFIG2
Address: Operational Base + offset (0x090C)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14:1	RW	0x0000	HDCP14_I2C_TIMER_OVR_VALUE I2C operation watchdog Timer Limit Override Value The defined override value is in an 10ms timebase. Value After Reset:0x0
0	RW	0x0	HDCP14_I2C_TIMER_OVR_EN I2C operation watchdog Timer Limit Override Enable Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_SEED
Address: Operational Base + offset (0x0914)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	WO	0x0000	HDCP14_KEY_DECRYPT_SEED HDCP Key Decryption seed. 16-bit seed used in HDCP Key Decryption. Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_H
Address: Operational Base + offset (0x0918)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:0	WO	0x000000	HDCP14_KEY_HIGH HDCP Encrypted Key [55:32] portion. Encrypted secret key, only for external storage of encrypted HDCP keys. A key is written by first writing the high part of hdcpkey[55:32] in hdcp14_key_high register and then the low hdcpkey[31:0] to hdcp14_key_low register. Writing hdcp14_key_low triggers decryption and storage in the key table, as well as auto incrementing of the hdcp14_key_index. Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_L
Address: Operational Base + offset (0x091C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	HDCP14_KEY_LOW HDCP Encrypted Key [31:0] portion. Encrypted secret key, only for external storage of encrypted HDCP keys. A key is written by first writing the high part of hdcpkey[55:32] in hdcp14_key_high register and then the low hdcpkey[31:0] to hdcp14_key_low register. Writing hdcp14_key_low triggers decryption and storage in the key table, as well as auto incrementing of the hdcp14_key_index. Value After Reset:0x0

HDMI TX Controller_HDCP14_KEY_STATUS
Address: Operational Base + offset (0x0920)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes
8	RO	0x0	HDCP14_KEY_WR_OK HDCP Key write OK. Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RO	0x00	HDCP14_KEY_INDEX HDCP Key index. Valid range is 00h ... 27h. Value After Reset:0x0

HDMI TX Controller_HDCP14_AKSV_H
Address: Operational Base + offset (0x0924)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	HDCP14_AKSV_HIGH DDC AKSV register content (bits 39:32). Value After Reset:0x0

HDMI TX Controller_HDCP14_AKSV_L
Address: Operational Base + offset (0x0928)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCP14_AKSV_LOW DDC AKSV register content (bits 31:0). Value After Reset:0x0

HDMI TX Controller_HDCP14_AN_H
Address: Operational Base + offset (0x092C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCP14_AN_VALUE_HIGH An value register content (bits 63:32). Value After Reset:0x0

HDMI TX Controller_HDCP14_AN_L
Address: Operational Base + offset (0x0930)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDCP14_AN_VALUE_LOW An value register content (bits 31:0). Value After Reset:0x0

HDMI TX Controller_HDCP14_STATUS0

Address: Operational Base + offset (0x0934)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved2 Reserved Field:Yes
23:20	RO	0x0	HDCP14_I2C_NACK_CNT HDCP 1.4 Total of I2C NACK Received. Cleared when hdcp14_restart_p is set to 1 or the number of received I2C NACK reaches the value defined in hdcp14_i2c_nack_threshold. Value After Reset:0x0
19:17	RW	0x0	Reserved1 Reserved Field:Yes
16	RO	0x0	HDCP14_BKSV_REVOC_FAIL_ST HDCP 1.4 BKSV Revocation status. When changed, it triggers the bksv_revoc_fail_irq interrupt. Value After Reset:0x0
15:9	RO	0x00	HDCP14_RPT_DEVICE_COUNT HDCP 1.4 Receiver/Repeater DEVICE_COUNT. Total number of attached downstream devices. Always zero for HDCP Receivers. This count does not include the HDCP Repeater itself, but only downstream devices downstream from the HDCP Repeater Value After Reset:0x0
8	RO	0x0	HDCP14_RPT_MAX_DEVS_EXCEEDED HDCP 1.4 Receiver/Repeater MAX_DEVS_EXCEEDED. Topology error indicator. When set to one, more than 127 downstream devices, or the capacity of the KSV Fifo, are attached. Value After Reset:0x0
7:5	RO	0x0	HDCP14_RPT_DEPTH HDCP 1.4 Receiver/Repeater DEPTH. Three-bit repeater cascade depth. This value gives the number of attached levels through the connection topology. Value After Reset:0x0
4	RO	0x0	HDCP14_RPT_MAX_CASCADE_EXCEEDED HDCP 1.4 Receiver/Repeater MAX_CASCADE_EXCEEDED. Topology error indicator. When set to one, more than seven levels of video repeater have been cascaded together. Value After Reset:0x0
3	RO	0x0	HDCP14_RCV_HDMI_MODE HDCP 1.4 Receiver HDMI_MODE: Values: 0x0 (DVI_MODE): DVI Mode. 0x1 (HDMI_MODE): HDMI Mode. Value After Reset:0x0
2	RO	0x0	HDCP14_AUTH_ST HDCP 1.4 Authentication State: Values: 0x0 (NON_AUTHENTICATED): Not Authenticated 0x1 (AUTHENTICATED): Authenticated Value After Reset:0x0
1	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
0	RO	0x0	HDCP14_OESS_ESSS HDCP 1.4 Encryption Status Signaling status: Values: 0x0 (OESS): OESS 0x1 (EESS): EESS Value After Reset:0x0

HDMI TX Controller_HDCP14_STATUS1
Address: Operational Base + offset (0x0938)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved1 Reserved Field:Yes
6	RO	0x0	HDCP14_RCV_REPEATER HDCP 1.4 Receiver Bstatus - REPEATER Value After Reset:0x0
5	RO	0x0	HDCP14_RCV_KSV_FIFO_READY HDCP 1.4 Receiver Bstatus - READY bit Value After Reset:0x0
4	RO	0x0	HDCP14_RCV_FASTMODE HDCP 1.4 Receiver Bstatus - FAST Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RO	0x0	HDCP14_RCV_1_1_FEATURES HDCP 1.4 Receiver Bstatus - 1.1_FEATURES Value After Reset:0x0
0	RO	0x0	HDCP14_RCV_FAST_REAUTHENTICATION HDCP 1.4 Receiver Bstatus - FAST_REAUTHENTICATION Value After Reset:0x0

HDMI TX Controller_SCRAMB_CONFIG0
Address: Operational Base + offset (0x0960)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	TMDS_SCRAMB_ENABLE TMDS scrambling enable Value After Reset:0x0

HDMI TX Controller_LINK_CONFIG0
Address: Operational Base + offset (0x0968)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved4 Reserved Field:Yes
16	RW	0x0	PHY_WORD_REVERSE Output bit reverse Values: 0x0 (NOT_REVERSED): word order is not reversed for the output 0x1 (REVERSED): word order is reversed for the output Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12	RW	0x0	BIT_REVERSE Output bit reverse Values: 0x0 (NOT_REVERSED): Bit order is not reversed for the output 0x1 (REVERSED): Bit order is reversed for the output Value After Reset:0x0
11:9	RW	0x0	Reserved2 Reserved Field:Yes
8	RW	0x0	OPMODE_FRL_4LANES FRL number of active lanes Values: 0x0 (THREE_LANES): 3 lanes 0x1 (FOUR_LANES): 4 lanes Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x1	OPMODE_DVI HDMI / DVI configuration bit Values: 0x0 (HDMI): HDMI mode 0x1 (DVI): DVI mode Value After Reset:0x1
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	OPMODE_FRL TMDS / FRL configuration bit Values: 0x0 (TMDS): TMDS mode 0x1 (FRL): FRL mode Value After Reset:0x0

HDMI TX Controller_TMDS_FIFO_CONFIG0

Address: Operational Base + offset (0x0970)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x1	TMDSFIFO_INIT_ON_OVF TMDS FIFO Init on overflow configuration. Value After Reset:0x1

HDMI TX Controller_TMDS_FIFO_CONTROL0

Address: Operational Base + offset (0x0974)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	TMDSFIFO_CLR_P TMDS FIFO clear Value After Reset:0x0

HDMI TX Controller_FRL_RSFEC_CONFIG0

Address: Operational Base + offset (0x0A20)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
0	RW	0x0	FRL_RSFEC_ENC_BYP FRL Reed-Solomon FEC calculation bypass enable: Values: 0x0 (NORMAL_MODE): RS FEC block calculate RS parity data to be included in the FRL stream 0x1 (BYPASS_MODE): RS FEC block does not calculate RS parity data to be included in the FRL stream Value After Reset:0x0

HDMI TX Controller_FRL_RSFEC_STATUS0

Address: Operational Base + offset (0x0A30)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_ST FRL Reed-Solomon FEC Aligner Buffer Full Status. Values: 0x0 (NOT_FULL): RS FEC Aligner Buffer is in normal operation 0x1 (FULL): RS FEC Aligner Buffer is full Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_CONFIG0

Address: Operational Base + offset (0x0A40)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	PKTZ_FRLCHAR_FIFO_INIT_ON_OVF FRL Packetizer FIFO Init on Overflow control Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_CONTROL0

Address: Operational Base + offset (0x0A44)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	PKTZ_FRLCHAR_FIFO_CLR_P FRL Packetizer FIFO clear Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_CONTROL1

Address: Operational Base + offset (0x0A50)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	PKTZ_FRLCHAR_FIFO_MAX_FILL_LEVEL_CLR_P FRL Packetizer FIFO max level clear Value After Reset:0x0

HDMI TX Controller_FRL_PKTZ_STATUS1

Address: Operational Base + offset (0x0A54)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
6:0	RO	0x00	PKTZ_FRLCHAR_FIFO_MAX_FILL_LEVEL FRL Packetizer FIFO maximum fill level reached This value is cleared with the frl_pktz_control1.pktz_frlchar_fifo_max_fill_level_clr_p bit field Value After Reset:0x0

HDMI TX Controller_PKTSCHED_CONFIG0

Address: Operational Base + offset (0x0A80)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2	RW	0x1	PKTSCHED_PRQUEUE2_EXEC_TYPE Packet Priority Queue 2 - Execution type Values: 0x0 (PRIORITY): Priority List 0x1 (RROBIN): Round-Robin Value After Reset:0x1
1	RW	0x1	PKTSCHED_PRQUEUE1_EXEC_TYPE Packet Priority Queue 1 - Execution type Values: 0x0 (PRIORITY): Priority List 0x1 (RROBIN): Round-Robin Value After Reset:0x1
0	RW	0x0	PKTSCHED_PRQUEUE0_EXEC_TYPE Packet Priority Queue 0 - Execution type Values: 0x0 (PRIORITY): Priority List 0x1 (RROBIN): Round-Robin Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PRQUEUE0_CONFIG0

Address: Operational Base + offset (0x0A84)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20:16	RW	0x03	PKTSCHED_PRQUEUE0_P2 Priority queue 0, priority position 2 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x3
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x02	PKTSCHED_PRQUEUE0_P1 Priority queue 0, priority position 1 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x2
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x01	PKTSCHED_PRQUEUE0_P0 Priority queue 0, priority position 0 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x1

HDMI TX Controller_PKTSCHED_PRQUEUE1_CONFIG0

Address: Operational Base + offset (0x0A88)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x09	PKTSCHED_PRQUEUE1_P3 Priority queue 1, priority position 3 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x9
23:21	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20:16	RW	0x07	PKTSCHED_PRQUEUE1_P2 Priority queue 1, priority position 2 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x7
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x0d	PKTSCHED_PRQUEUE1_P1 Priority queue 1, priority position 1 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xd
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x08	PKTSCHED_PRQUEUE1_P0 Priority queue 1, priority position 0 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x8

HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG0

Address: Operational Base + offset (0x0A8C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x06	PKTSCHED_PRQUEUE2_P3 Priority queue 2, priority position 3 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x6
23:21	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20:16	RW	0x05	PKTSCHED_PRQUEUE2_P2 Priority queue 2, priority position 2 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x5
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x0c	PKTSCHED_PRQUEUE2_P1 Priority queue 2, priority position 1 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xc
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x04	PKTSCHED_PRQUEUE2_P0 Priority queue 2, priority position 0 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x4

HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG1

Address: Operational Base + offset (0x0A90)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x0e	PKTSCHED_PRQUEUE2_P7 Priority queue 2, priority position 7 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xe
23:21	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20:16	RW	0x0f	PKTSCHED_PRQUEUE2_P6 Priority queue 2, priority position 6 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xf
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x0b	PKTSCHED_PRQUEUE2_P5 Priority queue 2, priority position 5 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xb
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x0a	PKTSCHED_PRQUEUE2_P4 Priority queue 2, priority position 4 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0xa

HDMI TX Controller_PKTSCHED_PRQUEUE2_CONFIG2

Address: Operational Base + offset (0x0A94)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12:8	RW	0x11	PKTSCHED_PRQUEUE2_P9 Priority queue 2, priority position 9 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x11
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RW	0x10	PKTSCHED_PRQUEUE2_P8 Priority queue 2, priority position 8 - Assign packet type Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x10

HDMI TX Controller_PKTSCHED_PKT_CONFIG0
Address: Operational Base + offset (0x0A98)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes
29:22	RW	0x01	PKTSCHED_ISRC_TIMER Packet Type ISRC 1/2 (International Standard Recording Code) Schedule Timer The ISRC 1/2 packets shall be sent once every time interval set in this field. The timer base increment is defined in the register field pktsched_isrc_timer_base. Settings 0 and 1 have the same value; - 0 : 1 time the configured timer base - 1 : 1 time the configured timer base - 2 : 2 times the configured timer base - ... - 255 : 255 times the configured timer base Note: There may be some uncertainty in the real time interval due to Data Island location within a frame and overall packet type priority settings. Value After Reset:0x1
21:20	RW	0x3	PKTSCHED_ISRC_TIMER_BASE Packet Type ISRC 1/2 (International Standard Recording Code) Schedule Timer Base Values: 0x0 (ONE_US): Timer base of 1 microsecond (1 us) 0x1 (ONE_HUNDRED_US): Timer base of 100 microseconds (100 us) 0x2 (TEN_MS): Timer base of 10 miliseconds (10 ms) 0x3 (VSYNC): Timer base corresponding to the Vertical frequency of the Video Mode being sent Value After Reset:0x3

Bit	Attr	Reset Value	Description
19:12	RW	0x64	PKTSCHED_SPDI_TIMER Packet Type SPDI (Source Product Descriptor InfoFrame) Schedule Timer The SPDI packet shall be sent once every time interval set in this field. The timer base increment is defined in the register field pktsched_spdi_timer_base. Settings 0 and 1 have the same value; The recommended interval between SPDI packets per CTA-861-G specification is 1s; SPDI packets shall not be sent more than once per Video Frame, although it is possible for debug or custom usage. - 0 : 1 time the configured timer base - 1 : 1 time the configured timer base - 2 : 2 times the configured timer base - ... - 255 : 255 times the configured timer base Note: There may be some uncertainty in the real time interval due to Data Island location within a frame and overall packet type priority settings. Value After Reset:0x64
11:10	RW	0x2	PKTSCHED_SPDI_TIMER_BASE Packet Type SPDI (Source Product Descriptor InfoFrame) Schedule Timer Base Values: 0x0 (ONE_US): Timer base of 1 microsecond (1 us) 0x1 (ONE_HUNDRED_US): Timer base of 100 microseconds (100 us) 0x2 (TEN_MS): Timer base of 10 miliseconds (10 ms) 0x3 (VSYNC): Timer base corresponding to the Vertical frequency of the Video Mode being sent Value After Reset:0x2
9:2	RW	0x01	PKTSCHED_ACP_TIMER Packet Type ACP (Audio Content Protection) Schedule Timer The ACP packet shall be sent once every time interval set in this field. The timer base increment is defined in the register field pktsched_acp_timer_base. Settings 0 and 1 have the same value; The maximum interval between ACP packets per HDMI2.1 specification is 300ms; Larger values may be used for debug or custom usage. - 0 : 1 time the configured timer base - 1 : 1 time the configured timer base - 2 : 2 times the configured timer base - ... - 255 : 255 times the configured timer base Note: There may be some uncertainty in the real time interval due to Data Island location within a frame and overall packet type priority settings. Value After Reset:0x1

Bit	Attr	Reset Value	Description
1:0	RW	0x3	PKTSCHED_ACP_TIMER_BASE Packet Type ACP (Audio Content Protection) Schedule Timer Base Values: 0x0 (ONE_US): Timer base of 1 microsecond (1 us) 0x1 (ONE_HUNDRED_US): Timer base of 100 microseconds (100 us) 0x2 (TEN_MS): Timer base of 10 miliseconds (10 ms) 0x3 (VSYNC): Timer base corresponding to the Vertical frequency of the Video Mode being sent Value After Reset:0x3

HDMI TX Controller_PKTSCHED_PKT_CONFIG1

Address: Operational Base + offset (0x0A9C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved1 Reserved Field:Yes
15	RW	0x0	PKTSCHED_EMPFAPA_NOINTERLEAVE Packet Type EMP (Extended Metadata) Block interleaving other packets with SYNC=1 EMP packets during FAPA EMP packets with SYNC=1 bit setting within its contents shall be sent during the FAPA region of the frame. This field blocks any other packet types to be interleaved between SYNC=1 EMP packets during the FAPA region, except for packets that always take precedence per HDMI2.1 specification: ACR, AUDS, GCP. Values: 0x0 (INTERLEAVE): Other packet types can be interleaved with SYNC=1 EMP packet during FAPA region. 0x1 (NOINTERLEAVE): Other packet types are blocked from being interleaved with SYNC=1 EMP packet during FAPA region. Value After Reset:0x0
14	RW	0x1	PKTSCHED_VSI_FIELDRATE Packet type VSI (Vendor Specific InfoFrame) Send Rate Values: 0x0 (ONEFIELD): VSI packet sent once per One Video Field 0x1 (TWOFIELDS): VSI packet sent once per Two Video Fields Value After Reset:0x1
13	RW	0x1	PKTSCHED_DRMI_FIELDRATE Packet type DRMI (Dynamic Range and Mastering InfoFrame) Send Rate Values: 0x0 (ONEFIELD): DRMI packet sent once per One Video Field 0x1 (TWOFIELDS): DRMI packet sent once per Two Video Fields Value After Reset:0x1
12	RW	0x1	PKTSCHED_AVI_FIELDRATE Packet type AVI (Auxiliary Video InfoFrame) Send Rate Values: 0x0 (ONEFIELD): AVI packet sent once per One Video Field 0x1 (TWOFIELDS): AVI packet sent once per Two Video Fields Value After Reset:0x1

Bit	Attr	Reset Value	Description
11	RW	0x1	PKTSCHED_AUDI_BEFORE_NEW_AUDS Packet type AUDI (Audio InfoFrame) Send Before First New Audio Sample Packet When a new Audio Format is configured, and a new Audio stream is enabled to be sent (change 'pktsched_auds_tx_en' from 0 to 1), an AUDI packet shell be sent before the first Audio Sample packet Values: 0x0 (DISABLED): AUDS Audio Sample packets sent immediately 0x1 (ENABLED): AUDI packet sent before first new AUDS Audio Sample packet Value After Reset:0x1
10	RW	0x1	PKTSCHED_AMD_BEFORE_NEW_AUDS Packet type AMD (Audio Metadata) Send Before First New Audio Sample Packet When a new Audio Format is configured, and a new Audio stream is enabled to be sent (change 'pktsched_auds_tx_en' from 0 to 1), an AMD packet shell be sent before the first Audio Sample packet Values: 0x0 (DISABLED): AUDS Audio Sample packets sent immediately 0x1 (ENABLED): AMD packet sent before first new AUDS Audio Sample packet Value After Reset:0x1
9	RW	0x1	PKTSCHED_AUDI_FIELD_FORCE_SCHED Packet type AUDI (Audio Infoframe) Force Schedule In regular schedule, AUDI packets are sent once per video field. Per HDMI2.1 specificattion, when there is any change to the AUDI packet contents, or a new Audio stream is started, the AUDI packet should be sent before any new audio sample (AUDS packets) If a previous AUDI packet has already been sent in the current video frame, this bit forces the packet schedule to allow a new content AUDI packet to be sent as soon as it is available, instead of waiting for a new video frame. Values: 0x0 (AUDIFORCEEN): AUDI Force Schedule Disabled 0x1 (AUDIFORCEDIS): AUDI Force Schedule Enabled Value After Reset:0x1
8	RW	0x1	PKTSCHED_AMD_FIELD_FORCE_SCHED Packet type AMD (Audio Metadata) Force Schedule In regular schedule, AMD packets are sent once per video field. Per HDMI2.1 specificattion, when there is any change to the AMD packet contents, or a new Audio stream is started, the AMD packet should be sent before any new audio sample (AUDS packets) If a previous AMD packet has already been sent in the current video frame, this bit forces the packet schedule to allow a new content AMD packet to be sent as soon as it is available, instead of waiting for a new video frame. Values: 0x0 (AMDFORCEEN): AMD Force Schedule Disabled 0x1 (AMDFORCEDIS): AMD Force Schedule Enabled Value After Reset:0x1
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_CONFIG2

Address: Operational Base + offset (0x0AA0)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x11	PKTSCHED_GHDMI2_PKT_OVR_VALUE Packet type GHDMI2 (Generic HDMI 2) override to replace other packet type's content If this field is set to any value different from GHDMI2, the contents register fields (pkt_ghdmi2_contents[0-7]) will replace the selected packet type contents. The packet enable and schedule configuration for the overriden packet type are still controlled by that type's respective register fields and hardware behavior. Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x11
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20	RW	0x0	PKTSCHED_GHDMI2_UNIT Packet type GHDMI2 (Generic HDMI 2) Send Unit Set the send unit for the number defined in pktsched_ghdmi2_rate. Note: This field is not used if pktsched_ghdmi2_pkt_ovr_value is set to any value different from GHDMI2; Values: 0x0 (FRAME): Packets per Video Frame 0x1 (FIELD): Packets per Video Field Value After Reset:0x0

Bit	Attr	Reset Value	Description
19:16	RW	0x0	PKTSCHED_GHDMI2_RATE Packet type GHDMI2 (Generic HDMI 2) Send Rate Set the send rate for GHDMI2 packets, in number of packets per field or frame (depending on the setting of pktsched_ghdmi2_unit). Note: This field is not used if pktsched_ghdmi2_pkt_ovr_value is set to any value different from GHDMI2; Values: 0x0 (DISABLED): Send disabled 0x1 (SEND1): Send 1 packet per field/frame 0x2 (SEND2): Send 2 packets per field/frame 0x3 (SEND3): Send 3 packets per field/frame 0x4 (SEND4): Send 4 packets per field/frame 0x5 (SEND5): Send 5 packets per field/frame 0x6 (SEND6): Send 6 packets per field/frame 0x7 (SEND7): Send 7 packets per field/frame 0x8 (SEND8): Send 8 packets per field/frame 0x9 (SEND9): Send 9 packets per field/frame 0xa (SEND10): Send 10 packets per field/frame 0xb (SEND11): Send 11 packets per field/frame 0xc (SEND12): Send 12 packets per field/frame 0xd (SEND13): Send 13 packets per field/frame 0xe (SEND14): Send 14 packets per field/frame 0xf (SEND15): Send 15 packets per field/frame Value After Reset:0x0
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x10	PKTSCHED_GHDMI1_PKT_OVR_VALUE Packet type GHDMI1 (Generic HDMI 1) override to replace other packet type's content If this field is set to any value different from GHDMI1, the contents register fields (pkt_ghdmi1_contents[0-7]) will replace the selected packet type contents. The packet enable and schedule configuration for the overriden packet type are still controlled by that type's respective register fields and hardware behavior. Values: 0x0 (RSRV): Reserved 0x1 (ACR): Audio Clock Regeneration 0x2 (AUDS): Audio Sample 0x3 (GCP): General Control 0x4 (ACP): Audio Content Protection 0x5 (ISRC1): Intl Std Recording Code 1 0x6 (ISRC2): Intl Std Recording Code 2 0x7 (GMD): Gamut Metadata 0x8 (AMD): Audio Metadata 0x9 (EMP): Extended Metadata 0xa (VSI): Vendor Specific InfoFrame 0xb (AVI): Auxiliary Video InfoFrame 0xc (SPDI): Source Product Descriptor InfoFrame 0xd (AUDI): Audio InfoFrame 0xe (NVI): NTSC VBI InfoFrame 0xf (DRMI): Dynamic Range and Mastering InfoFrame 0x10 (GHDMI1): Generic HDMI packet 1 0x11 (GHDMI2): Generic HDMI packet 2 Value After Reset:0x10

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4	RW	0x0	PKTSCHED_GHDMI1_UNIT Packet type GHDMI1 (Generic HDMI 1) Send Unit Set the send unit for the number defined in pktsched_ghdmi1_rate. Note: Note: This field is not used if pktsched_ghdmi1_pkt_ovr_value is set to any value different from GHDMI1; Values: 0x0 (FRAME): Packets per Video Frame 0x1 (FIELD): Packets per Video Field Value After Reset:0x0
3:0	RW	0x0	PKTSCHED_GHDMI1_RATE Packet type GHDMI1 (Generic HDMI 1) Send Rate Set the send rate for GHDMI1 packets, in number of packets per field or frame (depending on the setting of pktsched_ghdmi1_unit). Note: Note: This field is not used if pktsched_ghdmi1_pkt_ovr_value is set to any value different from GHDMI1; Values: 0x0 (DISABLED): Send disabled 0x1 (SEND1): Send 1 packet per field/frame 0x2 (SEND2): Send 2 packets per field/frame 0x3 (SEND3): Send 3 packets per field/frame 0x4 (SEND4): Send 4 packets per field/frame 0x5 (SEND5): Send 5 packets per field/frame 0x6 (SEND6): Send 6 packets per field/frame 0x7 (SEND7): Send 7 packets per field/frame 0x8 (SEND8): Send 8 packets per field/frame 0x9 (SEND9): Send 9 packets per field/frame 0xa (SEND10): Send 10 packets per field/frame 0xb (SEND11): Send 11 packets per field/frame 0xc (SEND12): Send 12 packets per field/frame 0xd (SEND13): Send 13 packets per field/frame 0xe (SEND14): Send 14 packets per field/frame 0xf (SEND15): Send 15 packets per field/frame Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PKT_CONFIG3

Address: Operational Base + offset (0x0AA4)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	RW	0x0	PKTSCHED_GHDMI2_TX_ONCE GHDMI2 - Generic HDMI 2 packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0

Bit	Attr	Reset Value	Description
18	RW	0x0	PKTSCHED_GHDMI1_TX_ONCE GHDMI1 - Generic HDMI 1 packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
17	RW	0x0	PKTSCHED_DRMI_TX_ONCE DRMI - Dynamic Range and Mastering InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
16	RW	0x0	PKTSCHED_NVI_TX_ONCE NVI - NTSC VBI InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
15	RW	0x0	PKTSCHED_AUDI_TX_ONCE AUDI - Audio InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
14	RW	0x0	PKTSCHED_SPDI_TX_ONCE SPDI - Source Product Descriptor InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
13	RW	0x0	PKTSCHED_AVI_TX_ONCE AVI - Auxiliary Video InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0

Bit	Attr	Reset Value	Description
12	RW	0x0	PKTSCHED_VSI_TX_ONCE VSI - Vendor Specific InfoFrame packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
11:8	RW	0x0	Reserved2 Reserved Field:Yes
7	RW	0x0	PKTSCHED_GMD_TX_ONCE GMD - Gamut Metadata packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
6	RW	0x0	Reserved1 Reserved Field:Yes
5	RW	0x0	PKTSCHED_ISRC_TX_ONCE ISRC - Intl Std Recording Code packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
4	RW	0x0	PKTSCHED_ACP_TX_ONCE ACP - Audio Content Protection packet send frequency configuration; Values: 0x0 (CONTINUOUS): Packets are sent continuously, according to the packet type schedule settings 0x1 (ONCE): Packet is sent once per SW request in register pktsched_pkt_send Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_EN

Address: Operational Base + offset (0x0AA8)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved1 Reserved Field:Yes
19	RW	0x0	PKTSCHED_GHDMI2_TX_EN GHDMI2 - Generic HDMI 2 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

Bit	Attr	Reset Value	Description
18	RW	0x0	PKTSCHED_GHDMI1_TX_EN GHDMI1 - Generic HDMI 1 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
17	RW	0x0	PKTSCHED_DRMI_TX_EN DRMI - Dynamic Range and Mastering InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
16	RW	0x0	PKTSCHED_NVI_TX_EN NVI - NTSC VBI InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
15	RW	0x0	PKTSCHED_AUDI_TX_EN AUDI - Audio InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
14	RW	0x0	PKTSCHED_SPDI_TX_EN SPDI - Source Product Descriptor InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
13	RW	0x0	PKTSCHED_AVI_TX_EN AVI - Auxiliary Video InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
12	RW	0x0	PKTSCHED_VSI_TX_EN VSI - Vendor Specific InfoFrame packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
11	RW	0x0	Reserved0 Reserved Field:Yes
10	RW	0x0	PKTSCHED_EMP_CVTEM_TX_EN CVTEM - Compressed Video Timing Extended Metadata packet transmission control: Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

Bit	Attr	Reset Value	Description
9	RW	0x0	PKTSCHED_EMP_VTEM_TX_EN VTEM - Video Timing Extended Metadata packet transmission control: Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
8	RW	0x0	PKTSCHED_AMD_TX_EN AMD - Audio Metadata packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
7	RW	0x0	PKTSCHED_GMD_TX_EN GMD - Gamut Metadata packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
6	RW	0x0	PKTSCHED_ISRC2_TX_EN ISRC2 - Intl Std Recording Code 2 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
5	RW	0x0	PKTSCHED_ISRC1_TX_EN ISRC1 - Intl Std Recording Code 1 packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
4	RW	0x0	PKTSCHED_ACP_TX_EN ACP - Audio Content Protection packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
3	RW	0x0	PKTSCHED_GCP_TX_EN GCP - General Control packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
2	RW	0x0	PKTSCHED_AUDS_TX_EN AUDS - Audio Sample packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0
1	RW	0x0	PKTSCHED_ACR_TX_EN ACR - Audio Clock Regeneration packet transmission control; Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	PKTSCHED_NULL_TX_EN NULL - Null packet transmission control; This packet type is a filler for Data Island periods, when all other packet types are either not enabled or waiting for their respective scheduled slot. If disabled, when no other packets types are ready to be sent, the HDMI stream will be kept in Control Period, and no Data Island period is used. Values: 0x0 (DISABLED): Transmission disabled 0x1 (ENABLED): Transmission enabled Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PKT_CONTROL0

Address: Operational Base + offset (0x0AAC)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x0	PKTSCHED_GCP_CLEAR_AVMUTE GCP - General Control - Define the value of the Clear_AVMUTE field in GCP packets. If this field is set to '1', field 'pktsched_gcp_set_avmute' must be 0. Values: 0x0 (CLEAR_AVMUTE0): Clear_AVMUTE=0 0x1 (CLEAR_AVMUTE1): Clear_AVMUTE=1 Value After Reset:0x0
0	RW	0x0	PKTSCHED_GCP_SET_AVMUTE GCP - General Control - Define the value of the Set_AVMUTE field in GCP packets. If this field is set to '1', field 'pktsched_gcp_clear_avmute' must be 0. Values: 0x0 (SET_AVMUTE0): Set_AVMUTE=0 0x1 (SET_AVMUTE1): Set_AVMUTE=1 Value After Reset:0x0

HDMI TX Controller_PKTSCHED_PKT_SEND

Address: Operational Base + offset (0x0AB0)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved2 Reserved Field:Yes
19	WO	0x0	PKTSCHED_GHDMI2_TX_SEND_P GHDMI2 - Generic HDMI 2 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
18	WO	0x0	PKTSCHED_GHDMI1_TX_SEND_P GHDMI1 - Generic HDMI 1 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
17	WO	0x0	PKTSCHED_DRMI_TX_SEND_P DRMI - Dynamic Range and Mastering InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0

Bit	Attr	Reset Value	Description
16	WO	0x0	PKTSCHED_NVI_TX_SEND_P NVI - NTSC VBI InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
15	WO	0x0	PKTSCHED_AUDI_TX_SEND_P AUDI - Audio InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
14	WO	0x0	PKTSCHED_SPDI_TX_SEND_P SPDI - Source Product Descriptor InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
13	WO	0x0	PKTSCHED_AVI_TX_SEND_P AVI - Auxiliary Video InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
12	WO	0x0	PKTSCHED_VSI_TX_SEND_P VSI - Vendor Specific InfoFrame packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes
7	WO	0x0	PKTSCHED_GMD_TX_SEND_P GMD - Gamut Metadata packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
6	WO	0x0	PKTSCHED_ISRC2_TX_SEND_P ISRC2 - Intl Std Recording Code 2 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
5	WO	0x0	PKTSCHED_ISRC1_TX_SEND_P ISRC1 - Intl Std Recording Code 1 packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
4	WO	0x0	PKTSCHED_ACP_TX_SEND_P ACP - Audio Content Protection packet send request; Write '1' to request the packet type to be sent once. Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_STATUS0

Address: Operational Base + offset (0x0AB4)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved2 Reserved Field:Yes
19	RO	0x0	PKTSCHED_GHDMI2_TX_STATUS GHDMI2 - Generic HDMI 2 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0

Bit	Attr	Reset Value	Description
18	RO	0x0	PKTSCHED_GHDMI1_TX_STATUS GHDMI1 - Generic HDMI 1 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
17	RO	0x0	PKTSCHED_DRMI_TX_STATUS DRMI - Dynamic Range and Mastering InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
16	RO	0x0	PKTSCHED_NVI_TX_STATUS NVI - NTSC VBI InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
15	RO	0x0	PKTSCHED_AUDI_TX_STATUS AUDI - Audio InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
14	RO	0x0	PKTSCHED_SPDI_TX_STATUS SPDI - Source Product Descriptor InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
13	RO	0x0	PKTSCHED_AVI_TX_STATUS AVI - Auxiliary Video InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
12	RO	0x0	PKTSCHED_VSI_TX_STATUS VSI - Vendor Specific InfoFrame packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
11:8	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7	RO	0x0	PKTSCHED_GMD_TX_STATUS GMD - Gamut Metadata packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
6	RO	0x0	PKTSCHED_ISRC2_TX_STATUS ISRC2 - Intl Std Recording Code 2 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
5	RO	0x0	PKTSCHED_ISRC1_TX_STATUS ISRC1 - Intl Std Recording Code 1 packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
4	RO	0x0	PKTSCHED_ACP_TX_STATUS ACP - Audio Content Protection packet send request; Values: 0x0 (IDLE): Packet has been sent, or not requested yet; 0x1 (REQUESTED): Packet send has been requested, and is waiting for the schedule slot; Value After Reset:0x0
3:0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKTSCHED_PKT_STATUS1

Address: Operational Base + offset (0x0AB8)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	PKTSCHED_GCP_AVMUTE_SENT_STS Currently active AVMUTE status; i.e. last AVMUTE state sent to HDMI Sink in a GCP Packet Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS0

Address: Operational Base + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_NULL_HEADER_HB2 NULL - Null - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_NULL_HEADER_HB1 NULL - Null - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_NULL_CONTENTS1
Address: Operational Base + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB3_0 NULL - Null - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS2
Address: Operational Base + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB7_4 NULL - Null - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS3
Address: Operational Base + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB11_8 NULL - Null - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS4
Address: Operational Base + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB15_12 NULL - Null - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS5
Address: Operational Base + offset (0x0B14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB19_16 NULL - Null - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS6
Address: Operational Base + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB23_20 NULL - Null - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_NULL_CONTENTS7
Address: Operational Base + offset (0x0B1C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NULL_BODY_PB27_24 NULL - Null - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS0
Address: Operational Base + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
23:16	RW	0x00	PKT_ACP_HEADER_HB2 ACP - Audio Content Protection - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_ACP_HEADER_HB1 ACP - Audio Content Protection - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_ACP_CONTENTS1
Address: Operational Base + offset (0x0B24)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB3_0 ACP - Audio Content Protection - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS2
Address: Operational Base + offset (0x0B28)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB7_4 ACP - Audio Content Protection - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS3
Address: Operational Base + offset (0x0B2C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB11_8 ACP - Audio Content Protection - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS4
Address: Operational Base + offset (0x0B30)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB15_12 ACP - Audio Content Protection - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS5
Address: Operational Base + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB19_16 ACP - Audio Content Protection - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS6
Address: Operational Base + offset (0x0B38)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB23_20 ACP - Audio Content Protection - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_ACP_CONTENTS7

Address: Operational Base + offset (0x0B3C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ACP_BODY_PB27_24 ACP - Audio Content Protection - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS0

Address: Operational Base + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_ISRC1_HEADER_HB2 ISRC1 - Intl Std Recording Code 1 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_ISRC1_HEADER_HB1 ISRC1 - Intl Std Recording Code 1 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_ISRC1_CONTENTS1

Address: Operational Base + offset (0x0B44)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB3_0 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS2

Address: Operational Base + offset (0x0B48)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB7_4 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS3

Address: Operational Base + offset (0x0B4C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB11_8 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS4

Address: Operational Base + offset (0x0B50)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB15_12 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS5
Address: Operational Base + offset (0x0B54)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB19_16 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS6
Address: Operational Base + offset (0x0B58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB23_20 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC1_CONTENTS7
Address: Operational Base + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC1_BODY_PB27_24 ISRC1 - Intl Std Recording Code 1 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS0
Address: Operational Base + offset (0x0B60)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_ISRC2_HEADER_HB2 ISRC2 - Intl Std Recording Code 2 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_ISRC2_HEADER_HB1 ISRC2 - Intl Std Recording Code 2 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_ISRC2_CONTENTS1
Address: Operational Base + offset (0x0B64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB3_0 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS2
Address: Operational Base + offset (0x0B68)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB7_4 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS3

Address: Operational Base + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB11_8 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS4

Address: Operational Base + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB15_12 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS5

Address: Operational Base + offset (0x0B74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB19_16 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS6

Address: Operational Base + offset (0x0B78)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB23_20 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_ISRC2_CONTENTS7

Address: Operational Base + offset (0x0B7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_ISRC2_BODY_PB27_24 ISRC2 - Intl Std Recording Code 2 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS0

Address: Operational Base + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_GMD_HEADER_HB2 GMD - Gamut Metadata - Packet Header (byte HB2) Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x00	PKT_GMD_HEADER_HB1 GMD - Gamut Metadata - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_GMD_CONTENTS1

Address: Operational Base + offset (0x0B84)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB3_0 GMD - Gamut Metadata - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS2

Address: Operational Base + offset (0x0B88)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB7_4 GMD - Gamut Metadata - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS3

Address: Operational Base + offset (0x0B8C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB11_8 GMD - Gamut Metadata - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS4

Address: Operational Base + offset (0x0B90)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB15_12 GMD - Gamut Metadata - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS5

Address: Operational Base + offset (0x0B94)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB19_16 GMD - Gamut Metadata - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS6

Address: Operational Base + offset (0x0B98)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB23_20 GMD - Gamut Metadata - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_GMD_CONTENTS7

Address: Operational Base + offset (0x0B9C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GMD_BODY_PB27_24 GMD - Gamut Metadata - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS0

Address: Operational Base + offset (0x0BA0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_AMD_HEADER_HB2 AMD - Audio Metadata - Packet Header (byte HB2 - 'NUM_AUDIO_STR' and 'NUM_VIEWS' defaul values defined by HDMI specification) Value After Reset:0x0
15:8	RW	0x00	PKT_AMD_HEADER_HB1 AMD - Audio Metadata - Packet Header (byte HB1 - 'HDMI_3D_Audio' default value defined by HDMI specification) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_AMD_CONTENTS1

Address: Operational Base + offset (0x0BA4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB3_0 AMD - Audio Metadata - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS2

Address: Operational Base + offset (0x0BA8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB7_4 AMD - Audio Metadata - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS3

Address: Operational Base + offset (0x0BAC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB11_8 AMD - Audio Metadata - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS4

Address: Operational Base + offset (0x0BB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB15_12 AMD - Audio Metadata - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS5

Address: Operational Base + offset (0x0BB4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB19_16 AMD - Audio Metadata - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS6

Address: Operational Base + offset (0x0BB8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB23_20 AMD - Audio Metadata - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_AMD_CONTENTS7

Address: Operational Base + offset (0x0BBC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AMD_BODY_PB27_24 AMD - Audio Metadata - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS0

Address: Operational Base + offset (0x0BC0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_VSI_HEADER_HB2 VSI - Vendor Specific InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_VSI_HEADER_HB1 VSI - Vendor Specific InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_VSI_CONTENTS1

Address: Operational Base + offset (0x0BC4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB3_0 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS2

Address: Operational Base + offset (0x0BC8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB7_4 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS3

Address: Operational Base + offset (0x0BCC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB11_8 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS4
Address: Operational Base + offset (0x0BD0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB15_12 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS5
Address: Operational Base + offset (0x0BD4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB19_16 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS6
Address: Operational Base + offset (0x0BD8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB23_20 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_VSI_CONTENTS7
Address: Operational Base + offset (0x0BDC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_VSI_BODY_PB27_24 VSI - Vendor Specific InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS0
Address: Operational Base + offset (0x0BE0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_AVI_HEADER_HB2 AVI - Auxiliary Video InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_AVI_HEADER_HB1 AVI - Auxiliary Video InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_AVI_CONTENTS1
Address: Operational Base + offset (0x0BE4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB3_0 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS2
Address: Operational Base + offset (0x0BE8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB7_4 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS3
Address: Operational Base + offset (0x0BEC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB11_8 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS4
Address: Operational Base + offset (0x0BF0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB15_12 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS5
Address: Operational Base + offset (0x0BF4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB19_16 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS6
Address: Operational Base + offset (0x0BF8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB23_20 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_AVI_CONTENTS7
Address: Operational Base + offset (0x0BFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AVI_BODY_PB27_24 AVI - Auxiliary Video InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS0
Address: Operational Base + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_SPDI_HEADER_HB2 SPDI - Source Product Descriptor InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_SPDI_HEADER_HB1 SPDI - Source Product Descriptor InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_SPDI_CONTENTS1

Address: Operational Base + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB3_0 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS2

Address: Operational Base + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB7_4 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS3

Address: Operational Base + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB11_8 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS4

Address: Operational Base + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB15_12 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS5

Address: Operational Base + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB19_16 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS6

Address: Operational Base + offset (0x0C18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB23_20 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_SPDI_CONTENTS7
Address: Operational Base + offset (0x0C1C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_SPDI_BODY_PB27_24 SPDI - Source Product Descriptor InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS0
Address: Operational Base + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x0a	PKT_AUDI_HEADER_HB2 AUDI - Audio InfoFrame - Packet Header (byte HB2 - 'Length' default value defined by HDMI specification, shall only be changed for debug purposes) Value After Reset:0xa
15:8	RW	0x01	PKT_AUDI_HEADER_HB1 AUDI - Audio InfoFrame - Packet Header (byte HB1 - 'Version Number' value defined by HDMI specification, shall only be changed for debug purposes) Value After Reset:0x1
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_AUDI_CONTENTS1
Address: Operational Base + offset (0x0C24)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB3_0 AUDI - Audio InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS2
Address: Operational Base + offset (0x0C28)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB7_4 AUDI - Audio InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS3
Address: Operational Base + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB11_8 AUDI - Audio InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS4
Address: Operational Base + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB15_12 AUDI - Audio InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS5
Address: Operational Base + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB19_16 AUDI - Audio InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS6
Address: Operational Base + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB23_20 AUDI - Audio InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_AUDI_CONTENTS7
Address: Operational Base + offset (0x0C3C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_AUDI_BODY_PB27_24 AUDI - Audio InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS0
Address: Operational Base + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_NVI_HEADER_HB2 NVI - NTSC VBI InfoFrame - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_NVI_HEADER_HB1 NVI - NTSC VBI InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_NVI_CONTENTS1
Address: Operational Base + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB3_0 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS2
Address: Operational Base + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB7_4 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS3
Address: Operational Base + offset (0x0C4C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB11_8 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS4
Address: Operational Base + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB15_12 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS5
Address: Operational Base + offset (0x0C54)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB19_16 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS6
Address: Operational Base + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB23_20 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_NVI_CONTENTS7
Address: Operational Base + offset (0x0C5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_NVI_BODY_PB27_24 NVI - NTSC VBI InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS0
Address: Operational Base + offset (0x0C60)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_DRMI_HEADER_HB2 DRMI - Dynamic Range and Mastering InfoFrame - Packet Header (byte HB2) Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x00	PKT_DRMI_HEADER_HB1 DRMI - Dynamic Range and Mastering InfoFrame - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_DRMI_CONTENTS1

Address: Operational Base + offset (0x0C64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB3_0 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS2

Address: Operational Base + offset (0x0C68)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB7_4 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS3

Address: Operational Base + offset (0x0C6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB11_8 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS4

Address: Operational Base + offset (0x0C70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB15_12 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS5

Address: Operational Base + offset (0x0C74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB19_16 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS6

Address: Operational Base + offset (0x0C78)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB23_20 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_DRMI_CONTENTS7
Address: Operational Base + offset (0x0C7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_DRMI_BODY_PB27_24 DRMI - Dynamic Range and Mastering InfoFrame - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS0
Address: Operational Base + offset (0x0C80)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	PKT_GHDMI1_HEADER_HB2 GHDMI1 - Generic HDMI 1 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_GHDMI1_HEADER_HB1 GHDMI1 - Generic HDMI 1 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	PKT_GHDMI1_HEADER_HB0 GHDMI1 - Generic HDMI 1 - Packet Header (byte HB0) Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS1
Address: Operational Base + offset (0x0C84)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB3_0 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS2
Address: Operational Base + offset (0x0C88)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB7_4 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS3
Address: Operational Base + offset (0x0C8C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB11_8 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS4
Address: Operational Base + offset (0x0C90)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB15_12 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS5

Address: Operational Base + offset (0x0C94)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB19_16 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS6

Address: Operational Base + offset (0x0C98)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB23_20 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI1_CONTENTS7

Address: Operational Base + offset (0x0C9C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI1_BODY_PB27_24 GHDMI1 - Generic HDMI 1 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS0

Address: Operational Base + offset (0x0CA0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0x00	PKT_GHDMI2_HEADER_HB2 GHDMI2 - Generic HDMI 2 - Packet Header (byte HB2) Value After Reset:0x0
15:8	RW	0x00	PKT_GHDMI2_HEADER_HB1 GHDMI2 - Generic HDMI 2 - Packet Header (byte HB1) Value After Reset:0x0
7:0	RW	0x00	PKT_GHDMI2_HEADER_HB0 GHDMI2 - Generic HDMI 2 - Packet Header (byte HB0) Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS1

Address: Operational Base + offset (0x0CA4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB3_0 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB3,PB2,PB1,PB0} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS2

Address: Operational Base + offset (0x0CA8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB7_4 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB7,PB6,PB5,PB4} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS3

Address: Operational Base + offset (0x0CAC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB11_8 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB11,PB10,PB9,PB8} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS4
Address: Operational Base + offset (0x0CB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB15_12 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB15,PB14,PB13,PB12} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS5
Address: Operational Base + offset (0x0CB4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB19_16 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB19,PB18,PB17,PB16} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS6
Address: Operational Base + offset (0x0CB8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB23_20 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB23,PB22,PB21,PB20} Value After Reset:0x0

HDMI TX Controller_PKT_GHDMI2_CONTENTS7
Address: Operational Base + offset (0x0CBC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_GHDMI2_BODY_PB27_24 GHDMI2 - Generic HDMI 2 - Packet Body - bytes {PB27,PB26,PB25,PB24} Value After Reset:0x0

HDMI TX Controller_PKT_EMP_CONFIG0
Address: Operational Base + offset (0x0CE0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:1	RW	0x0	EMP_TX_ORDER Extended Metadata Packets transmission order (from left to right): Note 1: Others values not listed are reserved Values: 0x0 (VCX): VTEM, CVTEM, EMP_EXTMEM 0x1 (VXC): VTEM, EMP_EXTMEM, CVTEM 0x2 (CXV): CVTEM, EMP_EXTMEM,VTEM 0x3 (CVX): CVTEM, VTEM, EMP_EXTMEM 0x4 (XVC): EMP_EXTMEM, VTEM, CVTEM 0x5 (XCV): EMP_EXTMEM, CVTEM, VTEM Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	EMP_TX_MTW_VIOLATION_EN Extended Metadata Packets transmission control when new MTW begins: Values: 0x0 (EMP_NSTOP_TX): continue to transmit EMPs until the end of the Data Sets loaded by SW for transmission 0x1 (EMP_STOP_TX): stop transmission when the new MTW begins Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS0

Address: Operational Base + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT_EMP_VTEM_HEADER_HB2 VTEM - Video Timing Extended Metadata - Packet Header (byte HB2) Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT_EMP_VTEM_HEADER_HB1 VTEM - Video Timing Extended Metadata - Packet Header (byte HB1) Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS1

Address: Operational Base + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	RW	0x0000	PKT_EMP_VTEM_BODY_PB1_0 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB1,PB0} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS2

Address: Operational Base + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	PKT_EMP_VTEM_BODY_PB7_5 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB7,PB6,PB5} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS3

Address: Operational Base + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB11_8 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS4

Address: Operational Base + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB15_12 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS5

Address: Operational Base + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB19_16 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS6

Address: Operational Base + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB23_20 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT_EMP_VTEM_CONTENTS7

Address: Operational Base + offset (0x0D1C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT_EMP_VTEM_BODY_PB27_24 VTEM - Video Timing Extended Metadata - Packet Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of VTEM payload requires rewriting all registers (pkt_emp_vtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS0

Address: Operational Base + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
23:16	RW	0x00	PKT0_EMP_CVTEM_HEADER_HB2 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Header (byte HB2) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT0_EMP_CVTEM_HEADER_HB1 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Header (byte HB1) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS1
Address: Operational Base + offset (0x0D24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	RW	0x0000	PKT0_EMP_CVTEM_BODY_PB1_0 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Body - bytes {PB1,PB0} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS2
Address: Operational Base + offset (0x0D28)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	PKT0_EMP_CVTEM_BODY_PB7_5 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Body - bytes {PB7,PB6,PB5} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS3
Address: Operational Base + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT0_EMP_CVTEM_BODY_PB11_8 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS4
Address: Operational Base + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT0_EMP_CVTEM_BODY_PB15_12 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS5

Address: Operational Base + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT0_EMP_CVTEM_BODY_PB19_16 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS6

Address: Operational Base + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT0_EMP_CVTEM_BODY_PB23_20 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT0_EMP_CVTEM_CONTENTS7

Address: Operational Base + offset (0x0D3C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT0_EMP_CVTEM_BODY_PB27_24 CVTEM - Compressed Video Timing Extended Metadata - Packet 0 Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS0

Address: Operational Base + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT1_EMP_CVTEM_HEADER_HB2 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Header (byte HB2) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT1_EMP_CVTEM_HEADER_HB1 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Header (byte HB1) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS1
Address: Operational Base + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT1_EMP_CVTEM_BODY_PB3_0 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Body - bytes {PB3,PB2,PB1,PB0} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS2
Address: Operational Base + offset (0x0D48)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT1_EMP_CVTEM_BODY_PB7_4 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Body - bytes {PB7,PB6,PB5,PB4} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS3
Address: Operational Base + offset (0x0D4C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT1_EMP_CVTEM_BODY_PB11_8 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS4
Address: Operational Base + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT1_EMP_CVTEM_BODY_PB15_12 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS5
Address: Operational Base + offset (0x0D54)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT1_EMP_CVTEM_BODY_PB19_16 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS6
Address: Operational Base + offset (0x0D58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT1_EMP_CVTEM_BODY_PB23_20 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT1_EMP_CVTEM_CONTENTS7
Address: Operational Base + offset (0x0D5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT1_EMP_CVTEM_BODY_PB27_24 CVTEM - Compressed Video Timing Extended Metadata - Packet 1 Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS0
Address: Operational Base + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT2_EMP_CVTEM_HEADER_HB2 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Header (byte HB2) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT2_EMP_CVTEM_HEADER_HB1 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Header (byte HB1) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS1
Address: Operational Base + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT2_EMP_CVTEM_BODY_PB3_0 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Body (bytes PB3..0) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS2
Address: Operational Base + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT2_EMP_CVTEM_BODY_PB7_4 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Body - bytes {PB7,PB6,PB5,PB4} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS3
Address: Operational Base + offset (0x0D6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT2_EMP_CVTEM_BODY_PB11_8 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS4
Address: Operational Base + offset (0x0D70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT2_EMP_CVTEM_BODY_PB15_12 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS5
Address: Operational Base + offset (0x0D74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT2_EMP_CVTEM_BODY_PB19_16 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS6
Address: Operational Base + offset (0x0D78)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT2_EMP_CVTEM_BODY_PB23_20 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT2_EMP_CVTEM_CONTENTS7
Address: Operational Base + offset (0x0D7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT2_EMP_CVTEM_BODY_PB27_24 CVTEM - Compressed Video Timing Extended Metadata - Packet 2 Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS0
Address: Operational Base + offset (0x0D80)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT3_EMP_CVTEM_HEADER_HB2 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Header (byte HB2) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT3_EMP_CVTEM_HEADER_HB1 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Header (byte HB1) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS1
Address: Operational Base + offset (0x0D84)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT3_EMP_CVTEM_BODY_PB3_0 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Body (bytes PB3..0) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS2
Address: Operational Base + offset (0x0D88)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT3_EMP_CVTEM_BODY_PB7_4 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Body - bytes {PB7,PB6,PB5,PB4} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS3
Address: Operational Base + offset (0x0D8C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT3_EMP_CVTEM_BODY_PB11_8 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS4
Address: Operational Base + offset (0x0D90)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT3_EMP_CVTEM_BODY_PB15_12 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS5
Address: Operational Base + offset (0x0D94)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT3_EMP_CVTEM_BODY_PB19_16 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS6
Address: Operational Base + offset (0x0D98)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT3_EMP_CVTEM_BODY_PB23_20 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT3_EMP_CVTEM_CONTENTS7
Address: Operational Base + offset (0x0D9C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT3_EMP_CVTEM_BODY_PB27_24 CVTEM - Compressed Video Timing Extended Metadata - Packet 3 Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS0
Address: Operational Base + offset (0x0DA0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
23:16	RW	0x00	PKT4_EMP_CVTEM_HEADER_HB2 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Header (byte HB2) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT4_EMP_CVTEM_HEADER_HB1 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Header (byte HB1) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS1

Address: Operational Base + offset (0x0DA4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT4_EMP_CVTEM_BODY_PB3_0 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Body (bytes PB3..0) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS2

Address: Operational Base + offset (0x0DA8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT4_EMP_CVTEM_BODY_PB7_4 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Body - bytes {PB7,PB6,PB5,PB4} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS3

Address: Operational Base + offset (0x0DAC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT4_EMP_CVTEM_BODY_PB11_8 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS4

Address: Operational Base + offset (0x0DB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT4_EMP_CVTEM_BODY_PB15_12 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS5
Address: Operational Base + offset (0x0DB4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT4_EMP_CVTEM_BODY_PB19_16 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS6
Address: Operational Base + offset (0x0DB8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT4_EMP_CVTEM_BODY_PB23_20 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT4_EMP_CVTEM_CONTENTS7
Address: Operational Base + offset (0x0DBC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT4_EMP_CVTEM_BODY_PB27_24 CVTEM - Compressed Video Timing Extended Metadata - Packet 4 Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS0
Address: Operational Base + offset (0x0DC0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x00	PKT5_EMP_CVTEM_HEADER_HB2 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Header (byte HB2) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
15:8	RW	0x00	PKT5_EMP_CVTEM_HEADER_HB1 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Header (byte HB1) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS1
Address: Operational Base + offset (0x0DC4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT5_EMP_CVTEM_BODY_PB3_0 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Body (bytes PB3..0) Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS2
Address: Operational Base + offset (0x0DC8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT5_EMP_CVTEM_BODY_PB7_4 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Body - bytes {PB7,PB6,PB5,PB4} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS3
Address: Operational Base + offset (0x0DCC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT5_EMP_CVTEM_BODY_PB11_8 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Body - bytes {PB11,PB10,PB9,PB8} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS4
Address: Operational Base + offset (0x0DD0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT5_EMP_CVTEM_BODY_PB15_12 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Body - bytes {PB15,PB14,PB13,PB12} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS5
Address: Operational Base + offset (0x0DD4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT5_EMP_CVTEM_BODY_PB19_16 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Body - bytes {PB19,PB18,PB17,PB16} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS6
Address: Operational Base + offset (0x0DD8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT5_EMP_CVTEM_BODY_PB23_20 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Body - bytes {PB23,PB22,PB21,PB20} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_PKT5_EMP_CVTEM_CONTENTS7

Address: Operational Base + offset (0x0DDC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PKT5_EMP_CVTEM_BODY_PB27_24 CVTEM - Compressed Video Timing Extended Metadata - Packet 5 Body - bytes {PB27,PB26,PB25,PB24} Note 1: Any change of CVTEM payload requires rewriting all registers (pkt0..5_emp_cvtem_contents0..7) Value After Reset:0x0

HDMI TX Controller_AUDPKT_CONTROL0

Address: Operational Base + offset (0x0E20)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved4 Reserved Field:Yes
20	RW	0x0	AUDPKT_SAMPLE_FLAT_OVR_EN Audio flat / sample invalid bits override enable Values: 0x0 (FLAT_OVR_DIS): Flat bits from audio interface 0x1 (FLAT_OVR_EN): Flat bits override Value After Reset:0x0
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16	RW	0x0	AUDPKT_SAMPLE_PRESENT_OVR_EN Audio sample present bits override enable Values: 0x0 (SPL_PRST_OVR_DIS): Sample present bits from audio interface 0x1 (SPL_PRST_OVR_EN): Sample present bits override Value After Reset:0x0
15:13	RW	0x0	Reserved2 Reserved Field:Yes
12	RW	0x0	AUDPKT_PBIT_FORCE_EN Audio parity bit force enable Values: 0x0 (PARITY_FORCE_DIS): Parity bit from audio interface 0x1 (PARITY_FORCE_EN): Parity bit calculated internally Value After Reset:0x0
11:10	RW	0x0	Reserved1 Reserved Field:Yes
9	RW	0x0	AUDPKT_LAYOUT_OVR_EN Audio Layout bit override enable Values: 0x0 (LAYOUT_OVR_DIS): ENLayout bit estimated in audio interface 0x1 (LAYOUT_OVR_EN): Layout bit override Value After Reset:0x0

Bit	Attr	Reset Value	Description
8	RW	0x0	AUDPKT_LAYOUT_OVR_VALUE Audio Layout bit override value Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	RW	0x0	AUDPKT_DBL_DST_OVR_EN Audio DBL bit override enable Values: 0x0 (DBL_OVR_DIS): DBL bit from audio interface 0x1 (DBL_OVR_EN): DBL bit override Value After Reset:0x0
4	RW	0x0	AUDPKT_DBL_DST_OVR_VALUE Audio DBL bit override value Value After Reset:0x0
3	RW	0x0	AUDPKT_VBIT_OVR_EN Audio Packetizer IEC 60958 Validity bit override enable Note: This field should only be set after the Audio Packetizer Validity bit override registers (audpkt_vbit_ovr*) are configured. Values: 0x0 (VBIT_OVR_DIS): Validity bit from audio interface 0x1 (VBIT_OVR_EN): Validity bit override Value After Reset:0x0
2	RW	0x0	AUDPKT_USRDATA_SPREAD_EN_OVR_VALUE Audio Packetizer IEC 60958 User Data override spread enable when override values are used Note: This field should only be set after the Audio Packetizer User Data override registers (audpkt_usrdata_ovr*) are configured and enabled (audpkt_usrdata_ovr_en=1) Values: 0x0 (USRDATA_OVR_SPREAD_DIS): User Data spread accross the different audio pairs of an audio packet 0x1 (USRDATA_OVR_SPREAD_EN): Same User Data used for all audio pairs of an audio packet Value After Reset:0x0
1	RW	0x0	AUDPKT_USRDATA_OVR_EN Audio Packetizer IEC 60958 User Data override enable Note: This field should only be set after the Audio Packetizer User Data override registers (audpkt_usrdata_ovr*) are configured Values: 0x0 (USRDATA_OVR_DIS): User Data from audio interface 0x1 (USRDATA_OVR_EN): User Data override Value After Reset:0x0
0	RW	0x0	AUDPKT_CHSTATUS_OVR_EN Audio Packetizer IEC 60958 Channel Status override enable Note: This field should only be set after the Audio Packetizer Channel Status override registers (audpkt_chstatus_ovr*) are configured. Values: 0x0 (CHSTATUS_OVR_DIS): Channel status from audio interface 0x1 (CHSTATUS_OVR_EN): Channel status override Value After Reset:0x0

HDMI TX Controller_AUDPKT_CONTROL1

Address: Operational Base + offset (0x0E24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	AUDPKT_SAMPLE_FLAT_OVR_VALUE Audio flat / sample invalid bits override values Note 1: This register field only takes values greater than 15 when Audio 3D features are present in the configuration (HDMI_QP_TX_AUD_3D == 1) Value After Reset:0x0
15:0	RW	0x0000	AUDPKT_SAMPLE_PRESENT_OVR_VALUE Audio sample present bits override values Note 1: This register field only takes values greater than 15 when Audio 3D features are present in the configuration (HDMI_QP_TX_AUD_3D == 1) Value After Reset:0x0

HDMI TX Controller AUDPKT ACR CONTROL0

Address: Operational Base + offset (0x0E40)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved1 Reserved Field:Yes
25	RW	0x0	AUDPKT_ACR_PLL4X_OVR_VALUE Audio Clock Regeneration (ACR) PLL 4x multiplication override value Values: 0x0 (PLL1X_OVR_VAL): PLL 1x 0x1 (PLL4X_OVR_VAL): PLL 4x Value After Reset:0x0
24	RW	0x0	AUDPKT_ACR_PLL4X_OVR_EN Audio Clock Regeneration (ACR) PLL 4x multiplication override enable Values: 0x0 (PLL4X_OVR_DIS): PLL 4x override disabled 0x1 (PLL4X_OVR_EN): PLL 4x override enabled Value After Reset:0x0
23:20	RW	0x0	Reserved0 Reserved Field:Yes
19:0	RW	0x00000	AUDPKT_ACR_N_VALUE Audio Clock Regeneration (ACR) packet N value Note 1: This value is used in the calculation of ACR CTS value and in the composition of the ACR packet. Value After Reset:0x0

HDMI TX Controller AUDPKT ACR CONTROL1

Address: Operational Base + offset (0x0E44)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	AUDPKT_ACR_CTS_OFFSET_VALUE Audio Clock Regeneration (ACR) CTS offset value. This register field can be configured with a positive or negative value that is added to the CTS received in the ACR packet. Note 1: The register must be configured with a value represented in 2's complement Value After Reset:0x0
23:4	RW	0x00000	AUDPKT_ACR_CTS_OVR_VALUE Audio Clock Regeneration (ACR) CTS override value Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
1	RW	0x0	AUDPKT_ACR_CTS_OVR_EN Audio Clock Regeneration (ACR) CTS override enable Values: 0x0 (CTS_OVR_DIS): CTS override disabled 0x1 (CTS_OVR_EN): CTS overrride enabled Value After Reset:0x0
0	RW	0x0	AUDPKT_ACR_CTS_ZERO_NOCHG Audio Clock Regeneration (ACR) CTS send mode Values: 0x0 (CTS_CALC): Sending ACR CTS calculated value, even if no change in relation to the previous CTS sent 0x1 (CTS_ZERO): Sending ACR CTS values of zero to indicate no new value of CTS Value After Reset:0x0

HDMI TX Controller_AUDPKT_ACR_STATUS0

Address: Operational Base + offset (0x0E4C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19:0	RO	0x00000	AUDPKT_ACR_CTS_VALUE Audio Clock Regeneration (ACR) packet CTS calculated value Note: This value is calculated from the ACR N value and used in the composition of the ACR packet. Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR0

Address: Operational Base + offset (0x0E60)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	RW	0x0000	AUDPKT_CHSTATUS_COMMON_BYTES1_0_OVR_VALUE Common Audio Channel Status payload bytes 0 (LSB byte) to 1 Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR1

Address: Operational Base + offset (0x0E64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES6_3_OVR_VALUE Common Audio Channel Status payload bytes 3 (LSB byte) to 6 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR2

Address: Operational Base + offset (0x0E68)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES10_7_OVR_VALUE Common Audio Channel Status payload bytes 7 (LSB byte) to 10 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR3

Address: Operational Base + offset (0x0E6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES14_11_OVR_VALUE Common Audio Channel Status payload bytes 11 (LSB byte) to 14 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR4

Address: Operational Base + offset (0x0E70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES18_15_OVR_VALUE Common Audio Channel Status payload bytes 15 (LSB byte) to 18 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR5

Address: Operational Base + offset (0x0E74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_COMMON_BYTES22_19_OVR_VALUE Common Audio Channel Status payload bytes 19 (LSB byte) to 22 (MSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR6

Address: Operational Base + offset (0x0E78)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	AUDPKT_CHSTATUS_COMMON_BYTE23_OVR_VALUE Common Audio Channel Status payload byte 23 (LSB byte) Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR7

Address: Operational Base + offset (0x0E7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_CHANNELS4_1_BYTE2_OVR_VALUE Channels 1 (LSB byte) to 4 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_CHSTATUS_OVR8

Address: Operational Base + offset (0x0E80)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_CHSTATUS_CHANNELS8_5_BYTE2_OVR_VALUE Channels 5 (LSB byte) to 8 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Only used when audpkt_chstatus_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC0

Address: Operational Base + offset (0x0EA0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_4_1_OVR_VALUE User Data Generic message payload IUs 4 to 1 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 1, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 4. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC1

Address: Operational Base + offset (0x0EA4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_8_5_OVR_VALUE User Data Generic message payload IUs 8 to 5 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 5, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 8. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC2

Address: Operational Base + offset (0x0EA8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_12_9_OVR_VALUE User Data Generic message payload IUs 12 to 9 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 9, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 12. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC3

Address: Operational Base + offset (0x0EAC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_16_13_OVR_VALUE User Data Generic message payload IUs 16 to 13 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 13, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 16. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC4

Address: Operational Base + offset (0x0EB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_20_17_OVR_VALUE User Data Generic message payload IUs 20 to 17 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 17, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 20. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC5

Address: Operational Base + offset (0x0EB4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_24_21_OVR_VALUE User Data Generic message payload IUs 24 to 21 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 21, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 24. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC6

Address: Operational Base + offset (0x0EB8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_28_25_OVR_VALUE User Data Generic message payload IUs 28 to 25 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 25, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 28. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC7

Address: Operational Base + offset (0x0EBC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_32_29_OVR_VALUE User Data Generic message payload IUs 32 to 29 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 29, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 32. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC8

Address: Operational Base + offset (0x0EC0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_36_33_OVR_VALUE User Data Generic message payload IUs 36 to 33 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 33, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 36. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC9

Address: Operational Base + offset (0x0EC4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_40_37_OVR_VALUE User Data Generic message payload IUs 40 to 37 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 37, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 40. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC10

Address: Operational Base + offset (0x0EC8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_44_41_OVR_VALUE User Data Generic message payload IUs 44 to 41 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 41, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 44. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC11
Address: Operational Base + offset (0x0ECC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_48_45_OVR_VALUE User Data Generic message payload IUs 48 to 45 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 45, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 48. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC12
Address: Operational Base + offset (0x0ED0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_52_49_OVR_VALUE User Data Generic message payload IUs 52 to 49 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 49, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 52. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC13
Address: Operational Base + offset (0x0ED4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_56_53_OVR_VALUE User Data Generic message payload IUs 56 to 53 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 53, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 56. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC14
Address: Operational Base + offset (0x0ED8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_60_57_OVR_VALUE User Data Generic message payload IUs 60 to 57 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 57, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 60. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC15
Address: Operational Base + offset (0x0EDC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_64_61_OVR_VALUE User Data Generic message payload IUs 64 to 61 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 61, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 64. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC16
Address: Operational Base + offset (0x0EE0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_68_65_OVR_VALUE User Data Generic message payload IUs 68 to 65 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 65, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 68. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC17
Address: Operational Base + offset (0x0EE4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_72_69_OVR_VALUE User Data Generic message payload IUs 72 to 69 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 69, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 72. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC18
Address: Operational Base + offset (0x0EE8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_76_73_OVR_VALUE User Data Generic message payload IUs 76 to 73 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 73, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 76. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC19
Address: Operational Base + offset (0x0EEC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_80_77_OVR_VALUE User Data Generic message payload IUs 80 to 77 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 77, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 80. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC20
Address: Operational Base + offset (0x0EF0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_84_81_OVR_VALUE User Data Generic message payload IUs 84 to 81 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 81, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 84. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC21
Address: Operational Base + offset (0x0EF4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_88_85_OVR_VALUE User Data Generic message payload IUs 88 to 85 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 85, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 88. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC22
Address: Operational Base + offset (0x0EF8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_92_89_OVR_VALUE User Data Generic message payload IUs 92 to 89 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 89, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 92. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC23
Address: Operational Base + offset (0x0EFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_96_93_OVR_VALUE User Data Generic message payload IUs 96 to 93 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 93, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 96. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC24
Address: Operational Base + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_100_97_OVR_VALUE User Data Generic message payload IUs 100 to 97 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 97, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 100. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC25
Address: Operational Base + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_104_101_OVR_VALUE User Data Generic message payload IUs 104 to 101 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 101, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 104. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC26

Address: Operational Base + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_108_105_OVR_VALUE User Data Generic message payload IUs 108 to 105 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 105, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 108. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC27

Address: Operational Base + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_112_109_OVR_VALUE User Data Generic message payload IUs 112 to 109 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 109, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 112. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC28

Address: Operational Base + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_116_113_OVR_VALUE User Data Generic message payload IUs 116 to 113 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 113, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 116. Only used when audpkt_usrdata_ovr_en=1 Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC29

Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_120_117_OVR_VALUE User Data Generic message payload IUs 120 to 117 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 117, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 120. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC30

Address: Operational Base + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_124_121_OVR_VALUE User Data Generic message payload IUs 124 to 121 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 121, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 124. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC31

Address: Operational Base + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUDPKT_USRDATA_MSG_GENERIC_IU_128_125_OVR_VALUE User Data Generic message payload IUs 128 to 125 Only used when audpkt_usrdata_ovr_en=1 Note: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 125, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 128. Value After Reset:0x0

HDMI TX Controller_AUDPKT_USRDATA_OVR_MSG_GENERIC32

Address: Operational Base + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	AUDPKT_USRDATA_MSG_GENERIC_IU_129_OVR_VALUE User Data Generic message payload IUs 129 Only used when audpkt_usrdata_ovr_en=1 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 129, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 129. Value After Reset:0x0

HDMI TX Controller_AUDPKT_VBIT_OVR0

Address: Operational Base + offset (0x0F24)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	AUDPKT_VBIT_CHANNEL8_1_OVR_VALUE IEC 60958 Validity override value - Channels 1-8 Only used when audpkt_vbit_ovr_en=1 Note: The LSB (bit) of the field corresponds to channel 1 and the MSB (bit) to channel 8. Value After Reset:0x0

HDMI TX Controller_CEC_TX_CONTROL

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	WO	0x0	FRAME_SEND_CLR_P Prevents further re-transmissions. If the transmission is ongoing, it is attempted to completion. Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	WO	0x0	FRAME_SEND_SET_P Set by software to trigger CEC sending a frame as an initiator. If cec_cfg.txreq_discad_ifrxbusy==0, the frame is transmitted even after receiving a frame in between. Otherwise, the frame to be sent is discarded as soon as a new incoming frame arrives (before being able to transmit). Value After Reset:0x0

HDMI TX Controller_CEC_STATUS
Address: Operational Base + offset (0x1004)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved2 Reserved Field:Yes
8	RO	0x0	CECTX_BUSY_ST Hardware is busy transmitting a frame. When this bit changes, it generates the cectx_busy_irq interrupt. Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	CECRX_BUSY_ST Hardware is busy receiving a message frame. If 'send' is asserted for a new TX message to be sent, it is delayed until the ongoing RX message is done. When this bit changes, it generates the cecrx_busy_irq interrupt. Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RO	0x0	FRAME_SEND_PENDING_ST Frame send pending status: Values: 0x1 (FRAME_PENDING): A frame is set to be transmitted (waiting for the end of an incoming message or to have access to the line). This bit keeps at 1 while the transmission is going on. 0x0 (NO_FRAME_PENDING): CEC transmission is done (no matter successful or failed). Value After Reset:0x0

HDMI TX Controller_CEC_CONFIG
Address: Operational Base + offset (0x1008)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved3 Reserved Field:Yes

Bit	Attr	Reset Value	Description
13:12	RW	0x0	SIGNAL_FREE_TIME Selects the Signal Free Time period that is to be respected before attempting to transmit or re-transmit a frame. If 0 is selected then the core follows the HDMI specification in CEC 9.1 Signal free time. Values: 0x0 (AUTO): Follows HDMI specification 0x1 (THREE_BIT_PERIOD): Waits for 3-bit periods before attempt transmission 0x2 (FIVE_BIT_PERIOD): Waits for 5-bit periods before attempt transmission 0x3 (SEVEN_BIT_PERIOD): Waits for 7-bit periods before attempt transmission Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RW	0x0	RX_AUTOMATIC_DRIVE_ACKNOWLEDGE RX automatic drive acknowledge. Values: 0x0 (WAIT_FOR_INITIATOR_ACK): Wait for initiator to drive logic '1' at ACK/NACK bit position for follower to reply with ACK/NACK bit. 0x1 (DRIVE_ACK): Automatically drive ACK/NACK bit at 2.65 ms of EOM initiator bit. Value After Reset:0x0
8	RW	0x1	CECFILTER Filter enable. Active high. Values: 0x1 (FILTER_ACTIVE): CEC filter is active and filters spurious signals in the CEC line (filter pulses <0.1ms) 0x0 (NO_FILTER): CEC filter inactive Value After Reset:0x1
7:6	RW	0x0	Reserved1 Reserved Field:Yes
5:4	RW	0x1	FRAME_NRETRANS Select number of re-transmission the hardware attempts as initiator after an arbitration loss (cectx_arblost_irq) or line error detection (cectx_lineerror_irq) Values: 0x0 (NO_RETRANS): Re-transmission is not attempt 0x1 (RETRANS_1): Re-transmit one time 0x2 (RETRANS_2): Re-transmit two times 0x3 (RETRANS_3): Re-transmit three times Value After Reset:0x1
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	BROADCAST_NACK Broadcast State. Values: 0x1 (BROADCAST_NACK): Respond with Negative ACK to any received broadcast message. Message not stored in RX registers. 0x0 (RECEIVE_BROADCAST): Receive broadcast messages. Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RW	0x0	TXREQ_DISCARD_IF_RXBUSY Transmit request (cec_ctrl.send = 1) is discarded if a RX transfer is ongoing. Values: 0x1 (DISCARD_IF_BUSY): The transmit request is cancelled if there is an ongoing RX transfer on the CEC line, raising the RX busy interrupt. 0x0 (WAIT_TO_TRANSMIT): The transmit request is always recorded by the TX FIFO for immediate or later transmission, depending on the CEC line status. For instance, the transmit is performed as soon as possible. Value After Reset:0x0

HDMI TX Controller_CEC_ADDR

Address: Operational Base + offset (0x100C)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved0 Reserved Field:Yes
14	RW	0x0	CEC_FOLLOWER_ADDR_14 Allocated to the CEC device the Logical address 14 (Specific use) Values: 0x1 (LOGICAL_ADDRESS_14): Logical address 14 - Specific use 0x0 (ADDRESS_NOT_SELECTED): Logical address 14 not allocated Value After Reset:0x0
13	RW	0x0	CEC_FOLLOWER_ADDR_13 Allocated to the CEC device the Logical address 13 (Backup 2) Values: 0x1 (LOGICAL_ADDRESS_13): Logical address 13 - Backup 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 13 not allocated Value After Reset:0x0
12	RW	0x0	CEC_FOLLOWER_ADDR_12 Allocated to the CEC device the Logical address 12 (Backup 1) Values: 0x1 (LOGICAL_ADDRESS_12): Logical address 12 - Backup 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 12 not allocated Value After Reset:0x0
11	RW	0x0	CEC_FOLLOWER_ADDR_11 Allocated to the CEC device the Logical address 11 (Playback Device 3) Values: 0x1 (LOGICAL_ADDRESS_11): Logical address 11 - Playback Device 3 0x0 (ADDRESS_NOT_SELECTED): Logical address 11 not allocated Value After Reset:0x0
10	RW	0x0	CEC_FOLLOWER_ADDR_10 Allocated to the CEC device the Logical address 10 (Tuner 4) Values: 0x1 (LOGICAL_ADDRESS_10): Logical address 10 - Tuner 4 0x0 (ADDRESS_NOT_SELECTED): Logical address 10 not allocated Value After Reset:0x0

Bit	Attr	Reset Value	Description
9	RW	0x0	CEC_FOLLOWER_ADDR_09 Allocated to the CEC device the Logical address 9 (Recording Device 3) Values: 0x1 (LOGICAL_ADDRESS_09): Logical address 9 - Recording Device 3 0x0 (ADDRESS_NOT_SELECTED): Logical address 9 not allocated Value After Reset:0x0
8	RW	0x0	CEC_FOLLOWER_ADDR_08 Allocated to the CEC device the Logical address 8 (Playback Device 2) Values: 0x1 (LOGICAL_ADDRESS_08): Logical address 8 - Playback Device 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 8 not allocated Value After Reset:0x0
7	RW	0x0	CEC_FOLLOWER_ADDR_07 Allocated to the CEC device the Logical address 7 (Tuner 3) Values: 0x1 (LOGICAL_ADDRESS_07): Logical address 7 - Tuner 3 0x0 (ADDRESS_NOT_SELECTED): Logical address 7 not allocated Value After Reset:0x0
6	RW	0x0	CEC_FOLLOWER_ADDR_06 Allocated to the CEC device the Logical address 6 (Tuner 2) Values: 0x1 (LOGICAL_ADDRESS_06): Logical address 6 - Tuner 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 6 not allocated Value After Reset:0x0
5	RW	0x0	CEC_FOLLOWER_ADDR_05 Allocated to the CEC device the Logical address 5 (Audio System) Values: 0x1 (LOGICAL_ADDRESS_05): Logical address 5 - Audio System 0x0 (ADDRESS_NOT_SELECTED): Logical address 5 not allocated Value After Reset:0x0
4	RW	0x0	CEC_FOLLOWER_ADDR_04 Allocated to the CEC device the Logical address 4 (Playback Device 1) Values: 0x1 (LOGICAL_ADDRESS_04): Logical address 4 - Playback Device 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 4 not allocated Value After Reset:0x0
3	RW	0x0	CEC_FOLLOWER_ADDR_03 Allocated to the CEC device the Logical address 3 (Tuner 1) Values: 0x1 (LOGICAL_ADDRESS_03): Logical address 3 - Tuner 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 3 not allocated Value After Reset:0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	CEC_FOLLOWER_ADDR_02 Allocated to the CEC device the Logical address 2 (Recording Device 2) Values: 0x1 (LOGICAL_ADDRESS_02): Logical address 2 - Recording Device 2 0x0 (ADDRESS_NOT_SELECTED): Logical address 2 not allocated Value After Reset:0x0
1	RW	0x0	CEC_FOLLOWER_ADDR_01 Allocated to the CEC device the Logical address 1 (Recording Device 1) Values: 0x1 (LOGICAL_ADDRESS_01): Logical address 1 - Recording Device 1 0x0 (ADDRESS_NOT_SELECTED): Logical address 1 not allocated Value After Reset:0x0
0	RW	0x0	CEC_FOLLOWER_ADDR_00 Allocated to the CEC device the Logical address 0 (Device TV) Values: 0x1 (LOGICAL_ADDRESS_00): Logical address 0 - Device TV 0x0 (ADDRESS_NOT_SELECTED): Logical address 0 not allocated Value After Reset:0x0

HDMI TX Controller_CEC_TX_COUNT

Address: Operational Base + offset (0x1020)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	CEC_TXBUFFER_CNT Frame message size in bytes to be transmitted, including Header and Data blocks. Values: 0x0 (SEND_1_BYTE): Send 1 byte 0x1 (SEND_2_BYTES): Send 2 bytes 0x2 (SEND_3_BYTES): Send 3 bytes 0x3 (SEND_4_BYTES): Send 4 bytes 0x4 (SEND_5_BYTES): Send 5 bytes 0x5 (SEND_6_BYTES): Send 6 bytes 0x6 (SEND_7_BYTES): Send 7 bytes 0x7 (SEND_8_BYTES): Send 8 bytes 0x8 (SEND_9_BYTES): Send 9 bytes 0x9 (SEND_10_BYTES): Send 10 bytes 0xa (SEND_11_BYTES): Send 11 bytes 0xb (SEND_12_BYTES): Send 12 bytes 0xc (SEND_13_BYTES): Send 13 bytes 0xd (SEND_14_BYTES): Send 14 bytes 0xe (SEND_15_BYTES): Send 15 bytes 0xf (SEND_16_BYTES): Send 16 bytes Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA3_0

Address: Operational Base + offset (0x1024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_3 CEC Transmitter Buffer - Byte 3 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_2 CEC Transmitter Buffer - Byte 2 Value After Reset:0x0
15:8	RW	0x00	CEC_TXBUFFER_DATA_1 CEC Transmitter Buffer - Byte 1 Value After Reset:0x0
7:0	RW	0x00	CEC_TXBUFFER_DATA_0 CEC Transmitter Buffer - Byte 0 Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA7_4

Address: Operational Base + offset (0x1028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_7 CEC Transmitter Buffer - Byte 7 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_6 CEC Transmitter Buffer - Byte 6 Value After Reset:0x0
15:8	RW	0x00	CEC_TXBUFFER_DATA_5 CEC Transmitter Buffer - Byte 5 Value After Reset:0x0
7:0	RW	0x00	CEC_TXBUFFER_DATA_4 CEC Transmitter Buffer - Byte 4 Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA11_8

Address: Operational Base + offset (0x102C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_11 CEC Transmitter Buffer - Byte 11 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_10 CEC Transmitter Buffer - Byte 10 Value After Reset:0x0
15:8	RW	0x00	CEC_TXBUFFER_DATA_9 CEC Transmitter Buffer - Byte 9 Value After Reset:0x0
7:0	RW	0x00	CEC_TXBUFFER_DATA_8 CEC Transmitter Buffer - Byte 8 Value After Reset:0x0

HDMI TX Controller_CEC_TX_DATA15_12

Address: Operational Base + offset (0x1030)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	CEC_TXBUFFER_DATA_15 CEC Transmitter Buffer - Byte 15 Value After Reset:0x0
23:16	RW	0x00	CEC_TXBUFFER_DATA_14 CEC Transmitter Buffer - Byte 14 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x00	CEC_TXBUFFER_DATA_13 CEC Transmitter Buffer - Byte 13 Value After Reset:0x0
7:0	RW	0x00	CEC_TXBUFFER_DATA_12 CEC Transmitter Buffer - Byte 12 Value After Reset:0x0

HDMI TX Controller_CEC_RX_COUNT_STATUS

Address: Operational Base + offset (0x1040)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes
8	RO	0x0	LOCKED_RXBUFFER_ST Status: Values: 0x1 (MSG_RECEIVED_RXBUFFER_LOCKED): Message is received as follower and is available to be read at cec_rx_cnt /cec_rx_data_XX. Further received messages are NACKed. 0x0 (NEW_MSG_WILL_BE_RECEIVED): A new message can be received. This bit goes to zero, the software writes (cec_lock_ctrl.locked_rxbuffer_clear =1). Value After Reset:0x0
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RO	0x0	CEC_RXBUFFER_CNT Received frame message size in bytes, including Header and Data blocks: Values: 0x0 (RECEIVED_1_BYTE): 1 byte received 0x1 (RECEIVED_2_BYTES): 2 bytes received 0x2 (RECEIVED_3_BYTES): 3 bytes received 0x3 (RECEIVED_4_BYTES): 4 bytes received 0x4 (RECEIVED_5_BYTES): 5 bytes received 0x5 (RECEIVED_6_BYTES): 6 bytes received 0x6 (RECEIVED_7_BYTES): 7 bytes received 0x7 (RECEIVED_8_BYTES): 8 bytes received 0x8 (RECEIVED_9_BYTES): 9 bytes received 0x9 (RECEIVED_10_BYTES): 10 bytes received 0xa (RECEIVED_11_BYTES): 11 bytes received 0xb (RECEIVED_12_BYTES): 12 bytes received 0xc (RECEIVED_13_BYTES): 13 bytes received 0xd (RECEIVED_14_BYTES): 14 bytes received 0xe (RECEIVED_15_BYTES): 15 bytes received 0xf (RECEIVED_16_BYTES): 16 bytes received Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA3_0

Address: Operational Base + offset (0x1044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_3 CEC Receiver Buffer - Byte 3 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_2 CEC Receiver Buffer - Byte 2 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RO	0x00	CEC_RXBUFFER_DATA_1 CEC Receiver Buffer - Byte 1 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_0 CEC Receiver Buffer - Byte 0 Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA7_4
Address: Operational Base + offset (0x1048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_7 CEC Receiver Buffer - Byte 7 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_6 CEC Receiver Buffer - Byte 6 Value After Reset:0x0
15:8	RO	0x00	CEC_RXBUFFER_DATA_5 CEC Receiver Buffer - Byte 5 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_4 CEC Receiver Buffer - Byte 4 Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA11_8
Address: Operational Base + offset (0x104C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_11 CEC Receiver Buffer - Byte 11 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_10 CEC Receiver Buffer - Byte 10 Value After Reset:0x0
15:8	RO	0x00	CEC_RXBUFFER_DATA_9 CEC Receiver Buffer - Byte 9 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_8 CEC Receiver Buffer - Byte 8 Value After Reset:0x0

HDMI TX Controller_CEC_RX_DATA15_12
Address: Operational Base + offset (0x1050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	CEC_RXBUFFER_DATA_15 CEC Receiver Buffer - Byte 15 Value After Reset:0x0
23:16	RO	0x00	CEC_RXBUFFER_DATA_14 CEC Receiver Buffer - Byte 14 Value After Reset:0x0
15:8	RO	0x00	CEC_RXBUFFER_DATA_13 CEC Receiver Buffer - Byte 13 Value After Reset:0x0
7:0	RO	0x00	CEC_RXBUFFER_DATA_12 CEC Receiver Buffer - Byte 12 Value After Reset:0x0

HDMI TX Controller_CEC_LOCK_CONTROL
Address: Operational Base + offset (0x1054)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	LOCKED_RXBUFFER_CLR_P Write 1 to this bit to unlock the RX buffer and allow the controller to receive a new incoming message Value After Reset:0x0

HDMI TX Controller_CEC_RXQUAL_BITTIME_CONFIG
Address: Operational Base + offset (0x1060)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved4 Reserved Field:Yes
18:16	RW	0x3	RXQUAL_FOLLBIT_TIMET8_EARLSTART RX qualifier bit time for T8, the earliest time of the start of a new bit. Any fall edge before this time puts the bit qualifier fsm in abort state. Values: 0x0 (T8_1.90ms): 1.90 ms 0x1 (T8_1.95ms): 1.95 ms 0x2 (T8_2.00ms): 2.00 ms 0x3 (T8_2.04ms): 2.04 ms 0x4 (T8_2.10ms): 2.10 ms 0x5 (T8_2.15ms): 2.15 ms 0x6 (T8_2.20ms): 2.20 ms 0x7 (T8_2.25ms): 2.25 ms Value After Reset:0x3
15	RW	0x0	Reserved3 Reserved Field:Yes
14:12	RW	0x3	RXQUAL_FOLLBIT_TIMET7_LATERETHIGH RX qualifier bit time for T7, the latest return to high time. Any edge after this time puts the bit qualifier fsm in abort state. Values: 0x0 (T7_1.55ms): 1.55 ms 0x1 (T7_1.60ms): 1.60 ms 0x2 (T7_1.65ms): 1.65 ms 0x3 (T7_1.71ms): 1.71 ms 0x4 (T7_1.75ms): 1.75 ms 0x5 (T7_1.80ms): 1.80 ms 0x6 (T7_1.85ms): 1.85 ms 0x7 (T7_1.90ms): 1.90 ms Value After Reset:0x3
11	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
10:8	RW	0x3	RXQUAL_FOLLBIT_TIMET6_EARLRETHIGH RX qualifier bit time for T6, the earliest return to high time. Any edge before this time puts the bit qualifier fsm in abort state. Values: 0x0 (T6_1.15ms): 1.15 ms 0x1 (T6_1.20ms): 1.20 ms 0x2 (T6_1.25ms): 1.25 ms 0x3 (T6_1.29ms): 1.29 ms 0x4 (T6_1.35ms): 1.35 ms 0x5 (T6_1.40ms): 1.40 ms 0x6 (T6_1.45ms): 1.45 ms 0x7 (T6_1.50ms): 1.50 ms Value After Reset:0x3
7	RW	0x0	Reserved1 Reserved Field:Yes
6:4	RW	0x3	RXQUAL_FOLLBIT_TIMET3_LATERETHIGH RX qualifier bit time for T3, the latest return to high time. Any edge after this time puts the bit qualifier fsm in abort state. Values: 0x0 (T3_0.65ms): 0.65 ms 0x1 (T3_0.70ms): 0.70 ms 0x2 (T3_0.75ms): 0.75 ms 0x3 (T3_0.81ms): 0.81 ms 0x4 (T3_0.85ms): 0.85 ms 0x5 (T3_0.90ms): 0.90 ms 0x6 (T3_0.95ms): 0.95 ms 0x7 (T3_1.00ms): 1.00 ms Value After Reset:0x3
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x3	RXQUAL_FOLLBIT_TIMET2_EARLRETHIGH RX qualifier bit time for T2, the earliest return to high time. Any edge before this time puts the bit qualifier fsm in abort state. Values: 0x0 (T2_0.25ms): 0.25 ms 0x1 (T2_0.30ms): 0.30 ms 0x2 (T2_0.35ms): 0.35 ms 0x3 (T2_0.39ms): 0.39 ms 0x4 (T2_0.45ms): 0.45 ms 0x5 (T2_0.50ms): 0.50 ms 0x6 (T2_0.55ms): 0.55 ms 0x7 (T2_0.60ms): 0.60 ms Value After Reset:0x3

HDMI TX Controller_CEC_RX_BITTIME_CONFIG

Address: Operational Base + offset (0x1064)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved5 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22:20	RW	0x3	RX_FOLLBIT_TIMET9_AUTO_ACK When RX automatic ACK bit is enabled (rx_automatic_drive_acknowledge = 1) and current bit is EOM, the follower drives CEC line to zero thus starting the NACK/ACK bit time. This correspond to the end of a bit (time T9). Note: When RX automatic ACK bit is disabled (rx_automatic_drive_acknowledge = 0), the maximum bit time is defined by rx_follbit_timet9_endframe field register. Values: 0x0 (AUTOACK_T9_2.50ms): 2.50 ms 0x1 (AUTOACK_T9_2.55ms): 2.55 ms 0x2 (AUTOACK_T9_2.60ms): 2.60 ms 0x3 (AUTOACK_T9_2.65ms): 2.65 ms 0x4 (AUTOACK_T9_2.70ms): 2.70 ms 0x5 (AUTOACK_T9_2.75ms): 2.75 ms 0x6 (AUTOACK_T9_2.80ms): 2.80 ms 0x7 (AUTOACK_T9_2.85ms): 2.85 ms Value After Reset:0x3
19	RW	0x0	Reserved4 Reserved Field:Yes
18:16	RW	0x3	RX_STARTBIT_TIMET4_LATEND RX start bit time for T4, the latest time of the start of a new bit. If a fall edge is not detected before this time, the maximum width of a start bit has been exceeded and so the start bit is aborted. Values: 0x0 (T4_4.55ms): 4.55 ms 0x1 (T4_4.60ms): 4.60 ms 0x2 (T4_4.65ms): 4.65 ms 0x3 (T4_4.71ms): 4.71 ms 0x4 (T4_4.75ms): 4.75 ms 0x5 (T4_4.80ms): 4.80 ms 0x6 (T4_4.85ms): 4.85 ms 0x7 (T4_4.90ms): 4.90 ms Value After Reset:0x3
15	RW	0x0	Reserved3 Reserved Field:Yes
14:12	RW	0x3	RX_STARTBIT_TIMET3_EARLEND RX start bit time for T3, the earliest end of a start bit. Any edge before this time aborts the start bit. Values: 0x0 (T3_4.15ms): 4.15 ms 0x1 (T3_4.20ms): 4.20 ms 0x2 (T3_4.25ms): 4.25 ms 0x3 (T3_4.29ms): 4.29 ms 0x4 (T3_4.35ms): 4.35 ms 0x5 (T3_4.40ms): 4.40 ms 0x6 (T3_4.45ms): 4.45 ms 0x7 (T3_4.50ms): 4.50 ms Value After Reset:0x3
11	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
10:8	RW	0x3	RX_STARTBIT_TIMET2_LATERETHIGH RX start bit time for T2, the earliest return to high time. A fall edge after this time aborts the start bit. Values: 0x0 (T2_3.75ms): 3.75 ms 0x1 (T2_3.80ms): 3.80 ms 0x2 (T2_3.85ms): 3.85 ms 0x3 (T2_3.91ms): 3.91 ms 0x4 (T2_3.95ms): 3.95 ms 0x5 (T2_4.00ms): 4.00 ms 0x6 (T2_4.05ms): 4.05 ms 0x7 (T2_4.10ms): 4.10 ms Value After Reset:0x3
7	RW	0x0	Reserved1 Reserved Field:Yes
6:4	RW	0x3	RX_STARTBIT_TIMET1_EARLRETHIGH RX start bit time for T1, the earliest return to high time. Any edge before this time aborts the start bit. Values: 0x0 (T1_3.35ms): 3.35 ms 0x1 (T1_3.40ms): 3.40 ms 0x2 (T1_3.45ms): 3.45 ms 0x3 (T1_3.49ms): 3.49 ms 0x4 (T1_3.55ms): 3.55 ms 0x5 (T1_3.60ms): 3.60 ms 0x6 (T1_3.65ms): 3.65 ms 0x7 (T1_3.70ms): 3.70 ms Value After Reset:0x3
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x3	RX_FOLLBIT_TIMET9_ENDFRAME RX follower bit time for T9, the end of a frame. An edge after this time is considered as part of a new frame. Values: 0x0 (T9_2.60ms): 2.60 ms 0x1 (T9_2.65ms): 2.65 ms 0x2 (T9_2.70ms): 2.70 ms 0x3 (T9_2.76ms): 2.76 ms 0x4 (T9_2.80ms): 2.80 ms 0x5 (T9_2.85ms): 2.85 ms 0x6 (T9_2.90ms): 2.90 ms 0x7 (T9_2.95ms): 2.95 ms Value After Reset:0x3

HDMI TX Controller_CEC_TX_BITTIME_CONFIG

Address: Operational Base + offset (0x1068)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved7 Reserved Field:Yes

Bit	Attr	Reset Value	Description
30:28	RW	0x6	TX_ROUND_TRIP_DELAY TX round trip delay. The CEC input line is sampled after this delay to check if the drive zero of the CEC output is in fact in the line. This value is greater than the fall edge output delay of the CEC line output. Note: With the filter ON, the values below 0.1 ms works as the interrupt, drive_err_irq triggers since the delay caused by the filter is already greater than the specified value. Values: 0x0 (ROUND_TRIP_DELAY_0.02ms): 0.02 ms 0x1 (ROUND_TRIP_DELAY_0.04ms): 0.04 ms 0x2 (ROUND_TRIP_DELAY_0.06ms): 0.06 ms 0x3 (ROUND_TRIP_DELAY_0.08ms): 0.08 ms 0x4 (ROUND_TRIP_DELAY_0.10ms): 0.10 ms 0x5 (ROUND_TRIP_DELAY_0.13ms): 0.13 ms 0x6 (ROUND_TRIP_DELAY_0.16ms): 0.16 ms 0x7 (ROUND_TRIP_DELAY_0.20ms): 0.20 ms Value After Reset:0x6
27	RW	0x0	Reserved6 Reserved Field:Yes
26:24	RW	0x3	TX_STARTBIT_TIME_RISESAMPLE TX start bit rise sample. This is the time (counted from the fall edge of the startbit) when the CEC input line is sampled to check if the line is zero. Note: From this time on (and until the next bit fall edge), if the CEC line is zero the arbitration lost interrupt is triggered. Values: 0x0 (START_BIT_RISE_SAMPLE_3.75ms): 3.75 ms 0x1 (START_BIT_RISE_SAMPLE_3.80ms): 3.80 ms 0x2 (START_BIT_RISE_SAMPLE_3.85ms): 3.85 ms 0x3 (START_BIT_RISE_SAMPLE_3.91ms): 3.91 ms 0x4 (START_BIT_RISE_SAMPLE_3.95ms): 3.95 ms 0x5 (START_BIT_RISE_SAMPLE_4.00ms): 4.00 ms 0x6 (START_BIT_RISE_SAMPLE_4.05ms): 4.05 ms 0x7 (START_BIT_RISE_SAMPLE_4.10ms): 4.10 ms Value After Reset:0x3
23	RW	0x0	Reserved5 Reserved Field:Yes
22:20	RW	0x4	TX_STARTBIT_TIME_TOTALDURATION TX start bit total duration. This is the time when the next bit starts: Note: When the CEC Filter is enabled, both options 0 and 1, produces a start bit total duration of 4.40 ms, due to the delay added by the filter (0.1 ms). Values: 0x0 (START_BIT_TOTAL_DURATION_4.30ms): 4.30 ms (or 4.40 ms when CEC Filter is enabled) 0x1 (START_BIT_TOTAL_DURATION_4.35ms): 4.35 ms (or 4.40 ms when CEC Filter is enabled) 0x2 (START_BIT_TOTAL_DURATION_4.40ms): 4.40 ms 0x3 (START_BIT_TOTAL_DURATION_4.45ms): 4.45 ms 0x4 (START_BIT_TOTAL_DURATION_4.50ms): 4.50 ms 0x5 (START_BIT_TOTAL_DURATION_4.55ms): 4.55 ms 0x6 (START_BIT_TOTAL_DURATION_4.60ms): 4.60 ms 0x7 (START_BIT_TOTAL_DURATION_4.65ms): 4.65 ms Value After Reset:0x4

Bit	Attr	Reset Value	Description
19	RW	0x0	Reserved4 Reserved Field:Yes
18:16	RW	0x4	TX_STARTBIT_TIME_LH_TRANS TX start bit low to high transition time. This is the duration of the low period of the start bit. Values: 0x0 (START_BIT_LH_TRANS_3.50ms): 3.50 ms 0x1 (START_BIT_LH_TRANS_3.55ms): 3.55 ms 0x2 (START_BIT_LH_TRANS_3.60ms): 3.60 ms 0x3 (START_BIT_LH_TRANS_3.65ms): 3.65 ms 0x4 (START_BIT_LH_TRANS_3.70ms): 3.70 ms 0x5 (START_BIT_LH_TRANS_3.75ms): 3.75 ms 0x6 (START_BIT_LH_TRANS_3.80ms): 3.80 ms 0x7 (START_BIT_LH_TRANS_3.85ms): 3.85 ms Value After Reset:0x4
15	RW	0x0	Reserved3 Reserved Field:Yes
14:12	RW	0x4	TX_ERR_NOTIFY_TIME TX error notify time. This is the duration of the low logic value of the CEC line for an error notification. Values: 0x0 (ERR_NOTIFY_3.40ms): 3.40 ms 0x1 (ERR_NOTIFY_3.45ms): 3.45 ms 0x2 (ERR_NOTIFY_3.50ms): 3.50 ms 0x3 (ERR_NOTIFY_3.55ms): 3.55 ms 0x4 (ERR_NOTIFY_3.60ms): 3.60 ms 0x5 (ERR_NOTIFY_3.65ms): 3.65 ms 0x6 (ERR_NOTIFY_3.70ms): 3.70 ms 0x7 (ERR_NOTIFY_3.75ms): 3.75 ms Value After Reset:0x4
11	RW	0x0	Reserved2 Reserved Field:Yes
10:8	RW	0x4	TX_BIT_TIME_PERIOD TX initiator data bit period. The time when a new consecutive bit starts. Values: 0x0 (BIT_PERIOD_2.20ms): 2.20 ms 0x1 (BIT_PERIOD_2.25ms): 2.25 ms 0x2 (BIT_PERIOD_2.30ms): 2.30 ms 0x3 (BIT_PERIOD_2.35ms): 2.35 ms 0x4 (BIT_PERIOD_2.40ms): 2.40 ms 0x5 (BIT_PERIOD_2.45ms): 2.45 ms 0x6 (BIT_PERIOD_2.50ms): 2.50 ms 0x7 (BIT_PERIOD_2.55ms): 2.55 ms Value After Reset:0x4
7	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
6:4	RW	0x4	TX_BIT_TIME_RETHIGH TX initiator return to high data bit time when indicating a logic bit 0 (zero). Values: 0x0 (RETHIGH_1.30ms): 1.30 ms 0x1 (RETHIGH_1.35ms): 1.35 ms 0x2 (RETHIGH_1.40ms): 1.40 ms 0x3 (RETHIGH_1.45ms): 1.45 ms 0x4 (RETHIGH_1.50ms): 1.50 ms 0x5 (RETHIGH_1.55ms): 1.55 ms 0x6 (RETHIGH_1.60ms): 1.60 ms 0x7 (RETHIGH_1.65ms): 1.65 ms Value After Reset:0x4
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RW	0x4	TX_BIT_TIME_LH_TRANS TX initiator low to high data bit transition time when indicating a logical 1 (one). Values: 0x0 (LH_TRANS_0.40ms): 0.40 ms 0x1 (LH_TRANS_0.45ms): 0.45 ms 0x2 (LH_TRANS_0.50ms): 0.50 ms 0x3 (LH_TRANS_0.55ms): 0.55 ms 0x4 (LH_TRANS_0.60ms): 0.60 ms 0x5 (LH_TRANS_0.65ms): 0.65 ms 0x6 (LH_TRANS_0.70ms): 0.70 ms 0x7 (LH_TRANS_0.75ms): 0.75 ms Value After Reset:0x4

HDMI TX Controller_EARCRX_CMDC_CONFIG0

Address: Operational Base + offset (0x1800)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved4 Reserved Field:Yes
26	RW	0x1	EARCRX_XACTREAD_STOP_CFG eARC RX CMDC Read Transactions - After the eARC RX device sends an ACK in response to the Offset (state [ACK3]), if a STOP Command is received different behaviors that can be configured Values: 0x0 (XACTREAD_STOP_IDLE): The Read Transaction FSM will jump to [IDLE] as a failed transaction. 0x1 (XACTREAD_STOP_ACK4): The Read Transaction FSM will jump to [ACK4] and respond with ACK, finishing the transaction successfully. Value After Reset:0x1

Bit	Attr	Reset Value	Description
25	RW	0x1	EARCRX_XACTREAD_RETRY_CFG eARC RX CMDC Read Transactions - After the eARC RX device sends an ACK in response to the Offset (state [ACK3]), if a RETRY Command is received different behaviors that can be configured Values: 0x0 (XACTREAD_RETRY_ACK3): The Read Transaction FSM will stay in state [ACK3] and send ACK again. 0x1 (XACTREAD_RETRY_IDLE): The Read Transaction FSM will jump to [IDLE] without sending any response. This event will trigger interrupt earcrx_cmdc_heartbeat_lost_irq. Value After Reset:0x1
24	RW	0x1	EARCRX_CMDC_DSCVR_EARCVALID0_TO_DISC1 eARC RX CMDC Discovery - Enable jump from [RX eARC] to [RX DISC1] when a successful Heartbeat transaction is received with bit EARC_TX_STAT:EARC_VALID=0. Values: 0x0 (DSCVR_EARCVALID0_DISABLE): The Discovery FSM will not change state when bit EARC_TX_STAT:EARC_VALID=0 is received. 0x1 (DSCVR_EARCVALID0_ENABLE): When in state [RX eARC], the Discovery FSM will jump to state [RX DISC1] when bit EARC_TX_STAT:EARC_VALID=0 is received. Value After Reset:0x1
23:20	RW	0x0	Reserved3 Reserved Field:Yes
19	RW	0x0	EARCRX_CMDC_XACT_OVERFLOW_END_EN End a transaction on Data Overflow An Overflow condition is more than earcrx_cmdc_xact_rdsize bytes on a Read Transaction, or more than 256 bytes on a Write transaction. Note: Regardless of the value of this field, any data overflow situation will be notified through status bit earcrx_cmdc_status:earcrx_cmdc_xact_data_overflow at the end of the transaction. Values: 0x0 (ENDOVERFLOW_DISABLE): End on overflow disabled - If the eARC TX device sends more than earcrx_cmdc_xact_rdsize bytes of data or requests to receive more than 255 bytes of data, the eARC RX will respond indefinitely with <NACK> until a <STOP> is received to end the transaction. 0x1 (ENDOVERFLOW_ENABLE): End on overflow enabled - If the eARC TX device sends or requests to receive more than 255 bytes of data, the eARC RX will end the transaction imediately. Value After Reset:0x0

Bit	Attr	Reset Value	Description
18	RW	0x1	EARCRX_CMDC_XACT_RESTART_EN Allow for Transaction Re-Start if a eARC_READ or eARC_WRITE command packet is received out-of-place during a transaction; Note: Setting this field to 0 is a test mode, and should not be used in normal operation. Values: 0x0 (RESTART_DISABLE): Transaction Re-Start Disabled - Any unexpected Command Packet will terminate the transaction, signalled by register field earcrx_cmdc_status:earcrx_cmdc_xact_failed_unexpcmd=1. 0x1 (RESTART_ENABLE): Transaction Re-Start Enabled - Normal operation mode - During a transaction, if the eARC TX device sends an eARC_READ or eARC_WRITE command packet at any time other than at the start of a transaction, the eARC RX Controller will re-start and discard all data sent/received in the ongoing transaction. The transaction re-start event does not generate any interrupt, only at the end of the new transaction will the re-start be signalled by register field earcrx_cmdc_status:earcrx_cmdc_xact_restarted=1. Value After Reset:0x1
17	RW	0x0	Reserved2 Reserved Field:Yes
16	RW	0x0	EARCRX_CMDC_RX_COMMA_NOCOUNT During the Discovery [DISC1] and [DISC2] states, the eARC TX shall send COMMA ON/OFF sequence pairs, up to the spec count NeARC_RX_CONN_COMMA_COUNT(max), while waiting for Heartbeat transactions from eARC TX. This bit enables this behaviour. Values: 0x0 (COMMA_COUNT_ENABLE): Normal COMMA ON/OFF pair count is enabled, per HDMI2.1 spec. When the max count is reached, the line will be kept idle until TeARC_RX_TIMEOUT has expired, and Discovery times out. 0x1 (COMMA_COUNT_DISABLE): Disable COMMA ON/OFF pair count. The COMMA pairs will be sent regardless of the count, until TeARC_RX_TIMEOUT has expired, and Discovery times out. Value After Reset:0x0
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x00	EARCRX_CMDC_RX_XACT_TIMEOUT eARC RX timeout while waiting for an eARC TX Command during a Transaction Timeout value in increments of 1ms. When expired, this timeout will assert status bit earcrx_cmdc_xact_failed_timeout at the end of a transaction. Note 1: The HDMI2.1 specification does not state any timeout value for this function, except for an eventual Heartbeat Loss after nominal TeARC_LOST_HEARTBEAT of up to 130ms; - 0 : Disabled - 1 : 1ms - 2 : 2ms - 3 : 3ms - ... - 126 : 126ms - 127 : 127ms Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4	RW	0x0	EARCRX_CMDC_WHITELIST_EN Enable the CMDC Transaction Whitelist. Note: In the whitelist Device ID / Offset pairs, a value of 0x00 for the Offset means that any Offset value is accepted for that particular Device ID; Values: 0x0 (WHITELIST_DISABLE): Transaction Whitelist disabled; Any Device ID / Offset combination is accepted; 0x1 (WHITELIST_ENABLE): Transaction Whitelist Enabled. Only the selected pairs of Device ID and Offset will be accepted (registers earcrx_cmdc_whitelist0/1/2/3_config); Any transaction for a Device ID / Offset pair that is not included in the list will result in a NACK reply to the eARC TX's [DEVICE ID]or [OFFSET]command packets, as applicable; Value After Reset:0x0
3	RW	0x0	EARCRX_CMDC_ECC_INV_SYNBITORDER Invert ECC bit order, for both TX and RX packets, relative to the last stage on the LFSR syndrome generator as the LFSR-MSb: Values: 0x0 (ECCBITORD_MSBFIRST): LFSR-MSb sent first 0x1 (ECCBITORD_LSBFIRST): LFSR-LSb sent first Value After Reset:0x0
2	RW	0x1	EARCRX_CMDC_RXPKT_ECC_ERRCORRECT_EN ECC Error Correction enable for received packets Values: 0x0 (ECC_DISABLED): ECC Disabled - The received ECC syndrome bits are only checked against the locally calculated syndrome. 0x1 (ECC_ENABLED): ECC Enabled - The received ECC syndrome is used to correct bit errors in the package. Value After Reset:0x1
1	RW	0x0	EARCRX_CMDC_RXPKT_BADPAR_TOLERANT Accept RX packets with failed Parity check. Note: This action is independent from the value of earcrx_cmdc_rxpkt_badecc_tolerant. Value After Reset:0x0
0	RW	0x0	EARCRX_CMDC_RXPKT_BADECC_TOLERANT Accept RX packets with failed ECC check. Note 1: The ECC check depends on the value of earcrx_cmdc_rxpkt_ecc_errcorrect_en. Note 2: This action is independent from the value of earcrx_cmdc_rxpkt_badpar_tolerant. Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_CONFIG1

Address: Operational Base + offset (0x1804)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:16	RW	0xd1	EARCRX_CMDC_HEARTBEAT_WROFFSET Heartbeat Transactions - Write Offset Value After Reset:0xd1

Bit	Attr	Reset Value	Description
15:8	RW	0xd0	EARCRX_CMDC_HEARTBEAT_RDOFFSET Heartbeat Transactions - Read Offset Value After Reset:0xd0
7:0	RW	0x74	EARCRX_CMDC_HEARTBEAT_DEVICEID Heartbeat Transactions - Device ID Value After Reset:0x74

HDMI TX Controller_EARCRX_CMDC_CONTROL

Address: Operational Base + offset (0x1808)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved1 Reserved Field:Yes
5	RW	0x0	EARCRX_CMDC_DISCOVERY_FORCE_CONNECTED Force the [RX eARC] Discovery connected state. This mode bypasses the Discovery and COMMA process, and immediately enables CMDC transactions. The bypass state jump is done from any Discovery state except [DSCVR_OFF] and [RX H14b ARC]. The eARC Discovery field must be set for this mode to be activated (earcrx_cmdc_discovery_en=1). The HDMI1.4 ARC mode field must be cleared for this mode to be activated (earcrx_h14barc_active=0). Heartbeat periodic transactions are active in this mode. Heartbeat Loss detection depends on the value of field earcrx_cmdc_heartbeat_loss_en. Note: This is a test mode, and should not be used in normal operation. Values: 0x0 (FORCE_DISCOVERY_CONNECT_DISABLE): Disabled. The Controller will perform the normal Discovery process including COMMA ON/OFF periods. If already in [RX eARC] state, the Controller will continue normally in this state, until Heartbeat Loss of HPD is disabled. 0x1 (FORCE_DISCOVERY_CONNECT_ENABLE): Enabled. Will jump the Discovery FSM from any state into [RX eARC]. Note that the physical line HPD bit (earcrx_connector_hpd) must be set and Heartbeat transactions performed successfully for the Controller to remain in this state, otherwise it may enter a state loop in the Discovery FSM. Value After Reset:0x0

Bit	Attr	Reset Value	Description
4	RW	0x1	EARCRX_CMDC_HEARTBEAT_LOSS_EN Heartbeat Loss timeout enable This timeout event will trigger interrupt earcrx_cmdc_heartbeat_lost_irq. Note: Setting this field to 0 is a test mode, and should not be used in normal operation. Values: 0x0 (HEARTBEAT_LOSS_DISABLE): Heartbeat Loss Disabled. The Controller will never timeout on failed Heartbeat transaction pairs, and will keep the [RX eARC] Discovery state until the physical line HPD bit is cleared (earcrx_connector_hpd=0) or Discovery is disabled (earcrx_cmdc_discovery_en=0). 0x1 (HEARTBEAT_LOSS_ENABLE): Hearbeat Loss Enabled . Normal operation mode, Heartbeat Loss will be detected as a TeARC_LOST_HEARTBEAT timeout without a successfull Heartbeat transaction pair, when in Discovery [RX eARC] state. Value After Reset:0x1
3	RW	0x0	EARCRX_CMDC_DISCOVERY_EN eARC RX CMDC Discovery enable: Note 1: The eARC RX function cannot be enabled when HEC is in use. Note 2: This bit can be controlled independently from earcrx_dmac_audio_en. Values: 0x0 (DISCOVERY_DISABLE): Discovery Disabled - Discovery FSM will not progress from [RX IDLE1] state. If eARC is currently active, Discovery state reverts to [RX IDLE1] after any ongoing transaction is completed. 0x1 (DISCOVERY_ENABLE): Discovery Enabled - Allow Discovery state machine to progress from [RX IDLE1] when HPD is set high. Value After Reset:0x0
2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	EARCRX_CONNECTOR_HPD Set to the curent HPD value on the physical HDMI Connector. Value After Reset:0x0
0	RW	0x0	EARCRX_H14BARC_ACTIVE Set to 1 when H14b ARC is active. eARC Discovery is not possible when this bit is set. Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_WHITELIST0_CONFIG

Address: Operational Base + offset (0x180C)

Bit	Attr	Reset Value	Description
31:24	RW	0xd2	EARCRX_CMDC_WHITELIST_OFFSET1 Transaction Whitelist Pair 1 - Offset value - Default for ERX_LATENCY Audio Latency register A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0xd2
23:16	RW	0x74	EARCRX_CMDC_WHITELIST_DEVICEID1 Transaction Whitelist Pair 1 - Device ID value - Default for ERX_LATENCY Audio Latency register Value After Reset:0x74

Bit	Attr	Reset Value	Description
15:8	RW	0x00	EARCRX_CMDC_WHITELIST_OFFSET0 Transaction Whitelist Pair 0 - Offset value - Default for Capabilities Data Structure A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0x0
7:0	RW	0xa0	EARCRX_CMDC_WHITELIST_DEVICEID0 Transaction Whitelist Pair 0 - Device ID value - Default for Capabilities Data Structure Value After Reset:0xa0

HDMI TX Controller_EARCRX_CMDC_WHITELIST1_CONFIG
Address: Operational Base + offset (0x1810)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_WHITELIST_OFFSET3 Transaction Whitelist Pair 3 - Offset value A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_WHITELIST_DEVICEID3 Transaction Whitelist Pair 3 - Device ID value Value After Reset:0x0
15:8	RW	0xd3	EARCRX_CMDC_WHITELIST_OFFSET2 Transaction Whitelist Pair 2 - Offset value - Default for ERX_LATENCY_REQ Audio Latency register A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0xd3
7:0	RW	0x74	EARCRX_CMDC_WHITELIST_DEVICEID2 Transaction Whitelist Pair 2 - Device ID value - Default for ERX_LATENCY_REQ Audio Latency register Value After Reset:0x74

HDMI TX Controller_EARCRX_CMDC_WHITELIST2_CONFIG
Address: Operational Base + offset (0x1814)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_WHITELIST_OFFSET5 Transaction Whitelist Pair 5 - Offset value A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_WHITELIST_DEVICEID5 Transaction Whitelist Pair 5 - Device ID value Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_WHITELIST_OFFSET4 Transaction Whitelist Pair 4 - Offset value A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_WHITELIST_DEVICEID4 Transaction Whitelist Pair 4 - Device ID value Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_WHITELIST3_CONFIG
Address: Operational Base + offset (0x1818)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_WHITELIST_OFFSET7 Transaction Whitelist Pair 7 - Offset value A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_WHITELIST_DEVICEID7 Transaction Whitelist Pair 7 - Device ID value Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_WHITELIST_OFFSET6 Transaction Whitelist Pair 6 - Offset value A value of 0x00 in this field will accept any offset value for the respective Address; Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_WHITELIST_DEVICEID6 Transaction Whitelist Pair 6 - Device ID value Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_STATUS

Address: Operational Base + offset (0x181C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved1 Reserved Field:Yes
17	RO	0x0	EARCRX_CMDC_XACT_DATA_OVERFLOW 1: The eARC TX device has sent or requested to receive more than 256 bytes of data during a Write or Read Transaction Value After Reset:0x0
16	RO	0x0	EARCRX_CMDC_XACT_RESTARTED 1: Transaction was re-started due to received eARC_READ or eARC_WRITE command packet at an unexpected time during the previous transaction attempt. Note: This status bit will only be active if earcrx_cmdc_config0:earcrx_cmdc_xact_restart_en=1 Value After Reset:0x0
15:13	RO	0x0	EARCRX_CMDC_XACT_CORRECTED_ERRNUM Accumulated number of corrected single-bit errors in received packets, during a transaction Values: 0x0 (ACCUM_ERR0): No corrected errors 0x1 (ACCUM_ERR1): 1 corrected error 0x2 (ACCUM_ERR2): 2 corrected errors 0x3 (ACCUM_ERR3): 3 corrected errors 0x4 (ACCUM_ERR4): 4 corrected errors 0x5 (ACCUM_ERR5): 5 corrected errors 0x6 (ACCUM_ERR6): 6 corrected errors 0x7 (ACCUM_ERR7): 7 or more corrected errors Value After Reset:0x0
12	RO	0x0	EARCRX_CMDC_XACT_TIMEOUT Transaction Timeout status Values: 0x0 (XACT_TIMEOUT_OK): No timeout during transaction 0x1 (XACT_TIMEOUT_FAIL): Timeout occurred during a transaction, waiting for a packet from eARC TX (programmable time in field earcrx_cmdc_rx_xact_timeout) Value After Reset:0x0

Bit	Attr	Reset Value	Description
11	RO	0x0	EARCRX_CMDC_XACT_FAILED_UNCORRECTERR Transaction Uncorrectable Errors status Values: 0x0 (XACT_UNCORRECTERR_OK): No errors reported during transaction 0x1 (XACT_UNCORRECTERR_FAIL): Transaction failed due to Uncorrectable Error in packet from eARC TX Value After Reset:0x0
10	RO	0x0	EARCRX_CMDC_XACT_FAILED_UNEXPCMD Transaction Unexpected Command status Values: 0x0 (XACT_UNEXPCMD_OK): All received commands were ok 0x1 (XACT_UNEXPCMD_FAIL): Transaction failed due to Unexpected Command packet from eARC TX Value After Reset:0x0
9	RO	0x0	EARCRX_CMDC_XACT_SUCCESSFUL Transaction success status Values: 0x0 (XACT_SUCCESS_FAIL): Transaction has failed 0x1 (XACT_SUCCESS_OK): Transaction has been successful Value After Reset:0x0
8	RO	0x0	EARCRX_CMDC_XACT_FINISHED Transaction state Values: 0x0 (XACT_ONGOING): Transaction ongoing 0x1 (XACT_FINISHED): Transaction has finished Value After Reset:0x0
7	RO	0x0	EARCRX_CMDC_XACT_FAILED_OFFSET 1: Transaction failed due to unsupported Offset recieved from eARC TX Value After Reset:0x0
6	RO	0x0	EARCRX_CMDC_XACT_FAILED_DEVICEID 1: Transaction failed due to unsupported Device ID recieved from eARC TX Value After Reset:0x0
5	RO	0x0	EARCRX_CMDC_XACT_FAILED_STOP 1: Transaction failed due to STOP packet received from eARC TX before the Data stage, while in ACK[1,2,3] state Value After Reset:0x0
4	RW	0x0	Reserved0 Reserved Field:Yes
3:1	RO	0x0	EARCRX_CMDC_DISCOVERY_STATE eARC Discovery FSM current state Note: For more information on each state and operation, see the HDMI Controller Documentation. Values: 0x0 (DISCFSM_OFF): eARC is disabled 0x1 (DISCFSM_RXIDLE1): RX IDLE1 0x2 (DISCFSM_RXIDLE2): RX IDLE2 0x3 (DISCFSM_RXDISC1): RX DISC1 0x4 (DISCFSM_RXDISC2): RX DISC2 0x5 (DISCFSM_RXeARC): RX eARC 0x6 (DISCFSM_RXH14b): RX H14b ARC 0x7 (DISCFSM_RESERVED): Reserved, not used Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RO	0x0	EARCRX_CMDC_STUCKHIGH When set, indicates that the eARC line Common Mode is stuck high for longer than 2 bit lengths. Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_INFO

Address: Operational Base + offset (0x1820)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_SIZE Effectively transferred payload data size in bytes-1; that is, the number of bytes in this field is the transferred byte size minus one. - 0 : 1 bytes transferred - 1 : 2 bytes transferred - ... - 255 : 256 bytes transferred Note 1: This valued applies to both Read and Write transactions. Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_OFFSET Received Offset Valid even if rejected due to Whitelist restriction. Only valid if Device ID has been accepted. Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_DEVICEID Received Device ID Valid even if rejected due to Whitelist restriction. Value After Reset:0x0
7:1	RW	0x00	Reserved0 Reserved Field:Yes
0	RO	0x0	EARCRX_CMDC_XACT_TYPE Received Transaction Type: Values: 0x0 (XACT_RCV_READ): Read transaction received 0x1 (XACT_RCV_WRITE): Write transaction received Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_ACTION

Address: Operational Base + offset (0x1824)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	WO	0x0	EARCRX_CMDC_XACT_WRDATA_STORED_P After a Write Transaction, writing 1 to this field indicates to the HW that the SW has read all the data received in registers earcrx_cmdc_xact_wr[x]; Only after this write will the HW stop responding to any incoming [eARC_WRITE] command with NACK. Value After Reset:0x0
0	WO	0x0	EARCRX_CMDC_XACT_RDDATA_AVAIL_P During a Read Transaction, writing a 1 to this field triggers the HW to stop responding to eARC TX CONT packets with NACK, and respond with the data in registers earcrx_cmdc_xact_rd[x], up to the size indicated in earcrx_cmdc_xact_rd0:earcrx_cmdc_xact_rdsize. Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_HEARTBEAT_RXSTAT_SET
Address: Operational Base + offset (0x1828)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT7_SET Set value for Heartbeat EARC_RX_STAT[7] - Reserved for future use, set to 0; Value After Reset:0x0
6	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT6_SET Set value for Heartbeat EARC_RX_STAT[6] - Reserved for future use, set to 0; Value After Reset:0x0
5	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT5_SET Set value for Heartbeat EARC_RX_STAT[5] - Reserved for future use, set to 0; Value After Reset:0x0
4	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_STAT_CHNG_SET Set value for Heartbeat EARC_RX_STAT[4] - STAT_CHNG When this bit is set to 1, this will trigger bit EARC_RX_STAT:STAT_CHNG to be sent as 1 during Heartbeat transactions. The HW will revert back to sending EARC_RX_STAT:STAT_CHNG as 0 when the eARC TX device sends back EARC_TX_STAT:STAT_CHNG_CONF=1 SW shall set this bit to 1 within TEARC_STAT_CHNG_UPD of updating the ERX_LATENCY register. Note: During this handshaking process, the values of the STAT_CHNG and STAT_CHNG_CONF bits can be monitored by SW by reading status bits earcrx_cmdc_heartbeat_rxstat_stat_chng and earcrx_cmdc_heartbeat_txstat_stat_chng_conf; Value After Reset:0x0
3	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_CAP_CHNG_SET Set value for Heartbeat EARC_RX_STAT[3] - CAP_CHNG When this bit is set to 1, this will trigger bit EARC_RX_STAT:CAP_CHNG to be sent as 1 during Heartbeat transactions. The HW will revert back to sending EARC_RX_STAT:CAP_CHNG as 0 when the eARC TX device sends back EARC_TX_STAT:CAP_CHNG_CONF=1 SW shall set this bit to 1 within TEARC_CAP_CHNG_UPD of updating the Capabilities Data Structure. Note: During this handshaking process, the values of the CAP_CHNG and CAP_CHNG_CONF bits can be monitored by SW by reading status bits earcrx_cmdc_heartbeat_rxstat_cap_chng and earcrx_cmdc_heartbeat_txstat_cap_chng_conf; Value After Reset:0x0
2	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT2_SET Set value for Heartbeat EARC_RX_STAT[2] - Reserved for future use, set to 0; Value After Reset:0x0
1	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT1_SET Set value for Heartbeat EARC_RX_STAT[1] - Reserved for future use, set to 0; Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	WO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_EARC_HPD_SET Set value for Heartbeat EARC_RX_STAT[0] - EARC_HPD Soft EARC_HPB bit to be used while in an eARC active state (earcrx_cmdc_heartbeat_txstat_earc_valid==1). Reserved for future use, set to 0; Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_HEARTBEAT_STATUS
Address: Operational Base + offset (0x182C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_EARC_VALID Heartbeat Transactions - EARC_TX_STAT[7] - EARC_VALID Value After Reset:0x0
14	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_BIT6 Heartbeat Transactions - EARC_TX_STAT[6] - Reserved for future use Value After Reset:0x0
13	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_BIT5 Heartbeat Transactions - EARC_TX_STAT[5] - Reserved for future use Value After Reset:0x0
12	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_STAT_CHNG_CONF Heartbeat Transactions - EARC_TX_STAT[4] - STAT_CHNG_CONF Value After Reset:0x0
11	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_CAP_CHNG_CONF Heartbeat Transactions - EARC_TX_STAT[3] - CAP_CHNG_CONF Value After Reset:0x0
10	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_BIT2 Heartbeat Transactions - EARC_TX_STAT[2] - Reserved for future use Value After Reset:0x0
9	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_BIT1 Heartbeat Transactions - EARC_TX_STAT[1] - Reserved for future use Value After Reset:0x0
8	RO	0x0	EARCRX_CMDC_HEARTBEAT_TXSTAT_HDMI_HPD Heartbeat Transactions - EARC_TX_STAT[0] - HDMI_HPD Value After Reset:0x0
7	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT7 Heartbeat Transactions - EARC_RX_STAT[7] - Reserved for future use Value After Reset:0x0
6	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT6 Heartbeat Transactions - EARC_RX_STAT[6] - Reserved for future use Value After Reset:0x0
5	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT5 Heartbeat Transactions - EARC_RX_STAT[5] - Reserved for future use Value After Reset:0x0
4	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_STAT_CHNG Heartbeat Transactions - EARC_RX_STAT[4] - STAT_CHNG Value After Reset:0x0

Bit	Attr	Reset Value	Description
3	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_CAP_CHNG Heartbeat Transactions - EARC_RX_STAT[3] - CAP_CHNG Value After Reset:0x0
2	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT2 Heartbeat Transactions - EARC_RX_STAT[2] - Reserved for future use Value After Reset:0x0
1	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_BIT1 Heartbeat Transactions - EARC_RX_STAT[1] - Reserved for future use Value After Reset:0x0
0	RO	0x0	EARCRX_CMDC_HEARTBEAT_RXSTAT_EARC_HPD Heartbeat Transactions - EARC_RX_STAT[0] - EARC_HPD Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR0

Address: Operational Base + offset (0x1840)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT2 Write Transaction Data (TX) - Packet 2 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT1 Write Transaction Data (TX) - Packet 1 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT0 Write Transaction Data (TX) - Packet 0 Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_EARCRX_CMDC_XACT_WR1

Address: Operational Base + offset (0x1844)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT6 Write Transaction Data (TX) - Packet 6 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT5 Write Transaction Data (TX) - Packet 5 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT4 Write Transaction Data (TX) - Packet 4 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT3 Write Transaction Data (TX) - Packet 3 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR2

Address: Operational Base + offset (0x1848)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT10 Write Transaction Data (TX) - Packet 10 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT9 Write Transaction Data (TX) - Packet 9 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT8 Write Transaction Data (TX) - Packet 8 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT7 Write Transaction Data (TX) - Packet 7 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR3
Address: Operational Base + offset (0x184C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT14 Write Transaction Data (TX) - Packet 14 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT13 Write Transaction Data (TX) - Packet 13 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT12 Write Transaction Data (TX) - Packet 12 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT11 Write Transaction Data (TX) - Packet 11 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR4
Address: Operational Base + offset (0x1850)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT18 Write Transaction Data (TX) - Packet 18 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT17 Write Transaction Data (TX) - Packet 17 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT16 Write Transaction Data (TX) - Packet 16 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT15 Write Transaction Data (TX) - Packet 15 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR5
Address: Operational Base + offset (0x1854)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT22 Write Transaction Data (TX) - Packet 22 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT21 Write Transaction Data (TX) - Packet 21 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT20 Write Transaction Data (TX) - Packet 20 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT19 Write Transaction Data (TX) - Packet 19 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR6

Address: Operational Base + offset (0x1858)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT26 Write Transaction Data (TX) - Packet 26 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT25 Write Transaction Data (TX) - Packet 25 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT24 Write Transaction Data (TX) - Packet 24 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT23 Write Transaction Data (TX) - Packet 23 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR7

Address: Operational Base + offset (0x185C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT30 Write Transaction Data (TX) - Packet 30 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT29 Write Transaction Data (TX) - Packet 29 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT28 Write Transaction Data (TX) - Packet 28 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT27 Write Transaction Data (TX) - Packet 27 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR8

Address: Operational Base + offset (0x1860)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT34 Write Transaction Data (TX) - Packet 34 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT33 Write Transaction Data (TX) - Packet 33 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT32 Write Transaction Data (TX) - Packet 32 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT31 Write Transaction Data (TX) - Packet 31 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR9

Address: Operational Base + offset (0x1864)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT38 Write Transaction Data (TX) - Packet 38 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT37 Write Transaction Data (TX) - Packet 37 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT36 Write Transaction Data (TX) - Packet 36 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT35 Write Transaction Data (TX) - Packet 35 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR10

Address: Operational Base + offset (0x1868)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT42 Write Transaction Data (TX) - Packet 42 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT41 Write Transaction Data (TX) - Packet 41 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT40 Write Transaction Data (TX) - Packet 40 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT39 Write Transaction Data (TX) - Packet 39 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR11

Address: Operational Base + offset (0x186C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT46 Write Transaction Data (TX) - Packet 46 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT45 Write Transaction Data (TX) - Packet 45 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT44 Write Transaction Data (TX) - Packet 44 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT43 Write Transaction Data (TX) - Packet 43 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR12

Address: Operational Base + offset (0x1870)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT50 Write Transaction Data (TX) - Packet 50 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT49 Write Transaction Data (TX) - Packet 49 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT48 Write Transaction Data (TX) - Packet 48 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT47 Write Transaction Data (TX) - Packet 47 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR13

Address: Operational Base + offset (0x1874)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT54 Write Transaction Data (TX) - Packet 54 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT53 Write Transaction Data (TX) - Packet 53 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT52 Write Transaction Data (TX) - Packet 52 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT51 Write Transaction Data (TX) - Packet 51 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR14

Address: Operational Base + offset (0x1878)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT58 Write Transaction Data (TX) - Packet 58 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT57 Write Transaction Data (TX) - Packet 57 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT56 Write Transaction Data (TX) - Packet 56 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT55 Write Transaction Data (TX) - Packet 55 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR15

Address: Operational Base + offset (0x187C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT62 Write Transaction Data (TX) - Packet 62 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT61 Write Transaction Data (TX) - Packet 61 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT60 Write Transaction Data (TX) - Packet 60 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT59 Write Transaction Data (TX) - Packet 59 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR16

Address: Operational Base + offset (0x1880)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT66 Write Transaction Data (TX) - Packet 66 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT65 Write Transaction Data (TX) - Packet 65 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT64 Write Transaction Data (TX) - Packet 64 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT63 Write Transaction Data (TX) - Packet 63 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR17
Address: Operational Base + offset (0x1884)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT70 Write Transaction Data (TX) - Packet 70 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT69 Write Transaction Data (TX) - Packet 69 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT68 Write Transaction Data (TX) - Packet 68 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT67 Write Transaction Data (TX) - Packet 67 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR18
Address: Operational Base + offset (0x1888)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT74 Write Transaction Data (TX) - Packet 74 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT73 Write Transaction Data (TX) - Packet 73 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT72 Write Transaction Data (TX) - Packet 72 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT71 Write Transaction Data (TX) - Packet 71 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR19
Address: Operational Base + offset (0x188C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT78 Write Transaction Data (TX) - Packet 78 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT77 Write Transaction Data (TX) - Packet 77 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT76 Write Transaction Data (TX) - Packet 76 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT75 Write Transaction Data (TX) - Packet 75 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR20

Address: Operational Base + offset (0x1890)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT82 Write Transaction Data (TX) - Packet 82 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT81 Write Transaction Data (TX) - Packet 81 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT80 Write Transaction Data (TX) - Packet 80 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT79 Write Transaction Data (TX) - Packet 79 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR21

Address: Operational Base + offset (0x1894)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT86 Write Transaction Data (TX) - Packet 86 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT85 Write Transaction Data (TX) - Packet 85 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT84 Write Transaction Data (TX) - Packet 84 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT83 Write Transaction Data (TX) - Packet 83 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR22

Address: Operational Base + offset (0x1898)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT90 Write Transaction Data (TX) - Packet 90 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT89 Write Transaction Data (TX) - Packet 89 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT88 Write Transaction Data (TX) - Packet 88 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT87 Write Transaction Data (TX) - Packet 87 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR23
Address: Operational Base + offset (0x189C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT94 Write Transaction Data (TX) - Packet 94 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT93 Write Transaction Data (TX) - Packet 93 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT92 Write Transaction Data (TX) - Packet 92 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT91 Write Transaction Data (TX) - Packet 91 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR24
Address: Operational Base + offset (0x18A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT98 Write Transaction Data (TX) - Packet 98 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT97 Write Transaction Data (TX) - Packet 97 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT96 Write Transaction Data (TX) - Packet 96 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT95 Write Transaction Data (TX) - Packet 95 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR25
Address: Operational Base + offset (0x18A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT102 Write Transaction Data (TX) - Packet 102 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT101 Write Transaction Data (TX) - Packet 101 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT100 Write Transaction Data (TX) - Packet 100 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT99 Write Transaction Data (TX) - Packet 99 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR26
Address: Operational Base + offset (0x18A8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT106 Write Transaction Data (TX) - Packet 106 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT105 Write Transaction Data (TX) - Packet 105 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT104 Write Transaction Data (TX) - Packet 104 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT103 Write Transaction Data (TX) - Packet 103 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR27

Address: Operational Base + offset (0x18AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT110 Write Transaction Data (TX) - Packet 110 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT109 Write Transaction Data (TX) - Packet 109 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT108 Write Transaction Data (TX) - Packet 108 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT107 Write Transaction Data (TX) - Packet 107 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR28

Address: Operational Base + offset (0x18B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT114 Write Transaction Data (TX) - Packet 114 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT113 Write Transaction Data (TX) - Packet 113 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT112 Write Transaction Data (TX) - Packet 112 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT111 Write Transaction Data (TX) - Packet 111 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR29

Address: Operational Base + offset (0x18B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT118 Write Transaction Data (TX) - Packet 118 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT117 Write Transaction Data (TX) - Packet 117 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT116 Write Transaction Data (TX) - Packet 116 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT115 Write Transaction Data (TX) - Packet 115 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR30

Address: Operational Base + offset (0x18B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT122 Write Transaction Data (TX) - Packet 122 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT121 Write Transaction Data (TX) - Packet 121 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT120 Write Transaction Data (TX) - Packet 120 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT119 Write Transaction Data (TX) - Packet 119 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR31

Address: Operational Base + offset (0x18BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT126 Write Transaction Data (TX) - Packet 126 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT125 Write Transaction Data (TX) - Packet 125 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT124 Write Transaction Data (TX) - Packet 124 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT123 Write Transaction Data (TX) - Packet 123 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR32

Address: Operational Base + offset (0x18C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT130 Write Transaction Data (TX) - Packet 130 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT129 Write Transaction Data (TX) - Packet 129 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT128 Write Transaction Data (TX) - Packet 128 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT127 Write Transaction Data (TX) - Packet 127 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR33

Address: Operational Base + offset (0x18C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT134 Write Transaction Data (TX) - Packet 134 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT133 Write Transaction Data (TX) - Packet 133 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT132 Write Transaction Data (TX) - Packet 132 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT131 Write Transaction Data (TX) - Packet 131 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR34

Address: Operational Base + offset (0x18C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT138 Write Transaction Data (TX) - Packet 138 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT137 Write Transaction Data (TX) - Packet 137 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT136 Write Transaction Data (TX) - Packet 136 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT135 Write Transaction Data (TX) - Packet 135 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR35

Address: Operational Base + offset (0x18CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT142 Write Transaction Data (TX) - Packet 142 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT141 Write Transaction Data (TX) - Packet 141 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT140 Write Transaction Data (TX) - Packet 140 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT139 Write Transaction Data (TX) - Packet 139 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR36

Address: Operational Base + offset (0x18D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT146 Write Transaction Data (TX) - Packet 146 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT145 Write Transaction Data (TX) - Packet 145 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT144 Write Transaction Data (TX) - Packet 144 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT143 Write Transaction Data (TX) - Packet 143 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR37

Address: Operational Base + offset (0x18D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT150 Write Transaction Data (TX) - Packet 150 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT149 Write Transaction Data (TX) - Packet 149 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT148 Write Transaction Data (TX) - Packet 148 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT147 Write Transaction Data (TX) - Packet 147 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR38

Address: Operational Base + offset (0x18D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT154 Write Transaction Data (TX) - Packet 154 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT153 Write Transaction Data (TX) - Packet 153 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT152 Write Transaction Data (TX) - Packet 152 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT151 Write Transaction Data (TX) - Packet 151 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR39

Address: Operational Base + offset (0x18DC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT158 Write Transaction Data (TX) - Packet 158 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT157 Write Transaction Data (TX) - Packet 157 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT156 Write Transaction Data (TX) - Packet 156 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT155 Write Transaction Data (TX) - Packet 155 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR40

Address: Operational Base + offset (0x18E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT162 Write Transaction Data (TX) - Packet 162 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT161 Write Transaction Data (TX) - Packet 161 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT160 Write Transaction Data (TX) - Packet 160 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT159 Write Transaction Data (TX) - Packet 159 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR41

Address: Operational Base + offset (0x18E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT166 Write Transaction Data (TX) - Packet 166 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT165 Write Transaction Data (TX) - Packet 165 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT164 Write Transaction Data (TX) - Packet 164 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT163 Write Transaction Data (TX) - Packet 163 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR42

Address: Operational Base + offset (0x18E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT170 Write Transaction Data (TX) - Packet 170 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT169 Write Transaction Data (TX) - Packet 169 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT168 Write Transaction Data (TX) - Packet 168 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT167 Write Transaction Data (TX) - Packet 167 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR43

Address: Operational Base + offset (0x18EC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT174 Write Transaction Data (TX) - Packet 174 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT173 Write Transaction Data (TX) - Packet 173 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT172 Write Transaction Data (TX) - Packet 172 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT171 Write Transaction Data (TX) - Packet 171 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR44

Address: Operational Base + offset (0x18F0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT178 Write Transaction Data (TX) - Packet 178 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT177 Write Transaction Data (TX) - Packet 177 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT176 Write Transaction Data (TX) - Packet 176 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT175 Write Transaction Data (TX) - Packet 175 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR45

Address: Operational Base + offset (0x18F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT182 Write Transaction Data (TX) - Packet 182 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT181 Write Transaction Data (TX) - Packet 181 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT180 Write Transaction Data (TX) - Packet 180 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT179 Write Transaction Data (TX) - Packet 179 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR46

Address: Operational Base + offset (0x18F8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT186 Write Transaction Data (TX) - Packet 186 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT185 Write Transaction Data (TX) - Packet 185 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT184 Write Transaction Data (TX) - Packet 184 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT183 Write Transaction Data (TX) - Packet 183 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR47
Address: Operational Base + offset (0x18FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT190 Write Transaction Data (TX) - Packet 190 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT189 Write Transaction Data (TX) - Packet 189 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT188 Write Transaction Data (TX) - Packet 188 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT187 Write Transaction Data (TX) - Packet 187 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR48
Address: Operational Base + offset (0x1900)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT194 Write Transaction Data (TX) - Packet 194 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT193 Write Transaction Data (TX) - Packet 193 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT192 Write Transaction Data (TX) - Packet 192 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT191 Write Transaction Data (TX) - Packet 191 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR49
Address: Operational Base + offset (0x1904)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT198 Write Transaction Data (TX) - Packet 198 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT197 Write Transaction Data (TX) - Packet 197 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT196 Write Transaction Data (TX) - Packet 196 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT195 Write Transaction Data (TX) - Packet 195 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR50
Address: Operational Base + offset (0x1908)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT202 Write Transaction Data (TX) - Packet 202 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT201 Write Transaction Data (TX) - Packet 201 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT200 Write Transaction Data (TX) - Packet 200 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT199 Write Transaction Data (TX) - Packet 199 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR51

Address: Operational Base + offset (0x190C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT206 Write Transaction Data (TX) - Packet 206 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT205 Write Transaction Data (TX) - Packet 205 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT204 Write Transaction Data (TX) - Packet 204 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT203 Write Transaction Data (TX) - Packet 203 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR52

Address: Operational Base + offset (0x1910)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT210 Write Transaction Data (TX) - Packet 210 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT209 Write Transaction Data (TX) - Packet 209 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT208 Write Transaction Data (TX) - Packet 208 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT207 Write Transaction Data (TX) - Packet 207 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR53

Address: Operational Base + offset (0x1914)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT214 Write Transaction Data (TX) - Packet 214 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT213 Write Transaction Data (TX) - Packet 213 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT212 Write Transaction Data (TX) - Packet 212 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT211 Write Transaction Data (TX) - Packet 211 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR54

Address: Operational Base + offset (0x1918)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT218 Write Transaction Data (TX) - Packet 218 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT217 Write Transaction Data (TX) - Packet 217 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT216 Write Transaction Data (TX) - Packet 216 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT215 Write Transaction Data (TX) - Packet 215 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR55

Address: Operational Base + offset (0x191C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT222 Write Transaction Data (TX) - Packet 222 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT221 Write Transaction Data (TX) - Packet 221 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT220 Write Transaction Data (TX) - Packet 220 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT219 Write Transaction Data (TX) - Packet 219 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR56

Address: Operational Base + offset (0x1920)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT226 Write Transaction Data (TX) - Packet 226 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT225 Write Transaction Data (TX) - Packet 225 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT224 Write Transaction Data (TX) - Packet 224 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT223 Write Transaction Data (TX) - Packet 223 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR57
Address: Operational Base + offset (0x1924)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT230 Write Transaction Data (TX) - Packet 230 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT229 Write Transaction Data (TX) - Packet 229 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT228 Write Transaction Data (TX) - Packet 228 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT227 Write Transaction Data (TX) - Packet 227 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR58
Address: Operational Base + offset (0x1928)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT234 Write Transaction Data (TX) - Packet 234 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT233 Write Transaction Data (TX) - Packet 233 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT232 Write Transaction Data (TX) - Packet 232 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT231 Write Transaction Data (TX) - Packet 231 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR59
Address: Operational Base + offset (0x192C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT238 Write Transaction Data (TX) - Packet 238 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT237 Write Transaction Data (TX) - Packet 237 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT236 Write Transaction Data (TX) - Packet 236 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT235 Write Transaction Data (TX) - Packet 235 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR60
Address: Operational Base + offset (0x1930)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT242 Write Transaction Data (TX) - Packet 242 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT241 Write Transaction Data (TX) - Packet 241 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT240 Write Transaction Data (TX) - Packet 240 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT239 Write Transaction Data (TX) - Packet 239 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR61

Address: Operational Base + offset (0x1934)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT246 Write Transaction Data (TX) - Packet 246 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT245 Write Transaction Data (TX) - Packet 245 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT244 Write Transaction Data (TX) - Packet 244 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT243 Write Transaction Data (TX) - Packet 243 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR62

Address: Operational Base + offset (0x1938)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT250 Write Transaction Data (TX) - Packet 250 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT249 Write Transaction Data (TX) - Packet 249 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT248 Write Transaction Data (TX) - Packet 248 Value After Reset:0x0
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT247 Write Transaction Data (TX) - Packet 247 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR63

Address: Operational Base + offset (0x193C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT254 Write Transaction Data (TX) - Packet 254 Value After Reset:0x0
23:16	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT253 Write Transaction Data (TX) - Packet 253 Value After Reset:0x0
15:8	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT252 Write Transaction Data (TX) - Packet 252 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT251 Write Transaction Data (TX) - Packet 251 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_WR64

Address: Operational Base + offset (0x1940)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RO	0x00	EARCRX_CMDC_XACT_WRDATA_PKT255 Write Transaction Data (TX) - Packet 255 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD0

Address: Operational Base + offset (0x1960)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT2 Read Transaction Data (RX) - Packet 2 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT1 Read Transaction Data (RX) - Packet 1 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT0 Read Transaction Data (RX) - Packet 0 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDSIZE Read Transaction intended Data size in bytes-1. Note: Effectively transferred data size depends on the transaction execution; The actual transferred size is updated in earcrx_cmdc_xact_info:earcrx_cmdc_xact_size during the transaction; Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD1

Address: Operational Base + offset (0x1964)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT6 Read Transaction Data (RX) - Packet 6 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT5 Read Transaction Data (RX) - Packet 5 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT4 Read Transaction Data (RX) - Packet 4 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT3 Read Transaction Data (RX) - Packet 3 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD2

Address: Operational Base + offset (0x1968)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT10 Read Transaction Data (RX) - Packet 10 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT9 Read Transaction Data (RX) - Packet 9 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT8 Read Transaction Data (RX) - Packet 8 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT7 Read Transaction Data (RX) - Packet 7 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD3
Address: Operational Base + offset (0x196C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT14 Read Transaction Data (RX) - Packet 14 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT13 Read Transaction Data (RX) - Packet 13 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT12 Read Transaction Data (RX) - Packet 12 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT11 Read Transaction Data (RX) - Packet 11 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD4
Address: Operational Base + offset (0x1970)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT18 Read Transaction Data (RX) - Packet 18 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT17 Read Transaction Data (RX) - Packet 17 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT16 Read Transaction Data (RX) - Packet 16 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT15 Read Transaction Data (RX) - Packet 15 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD5
Address: Operational Base + offset (0x1974)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT22 Read Transaction Data (RX) - Packet 22 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT21 Read Transaction Data (RX) - Packet 21 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT20 Read Transaction Data (RX) - Packet 20 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT19 Read Transaction Data (RX) - Packet 19 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD6

Address: Operational Base + offset (0x1978)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT26 Read Transaction Data (RX) - Packet 26 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT25 Read Transaction Data (RX) - Packet 25 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT24 Read Transaction Data (RX) - Packet 24 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT23 Read Transaction Data (RX) - Packet 23 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD7

Address: Operational Base + offset (0x197C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT30 Read Transaction Data (RX) - Packet 30 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT29 Read Transaction Data (RX) - Packet 29 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT28 Read Transaction Data (RX) - Packet 28 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT27 Read Transaction Data (RX) - Packet 27 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD8

Address: Operational Base + offset (0x1980)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT34 Read Transaction Data (RX) - Packet 34 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT33 Read Transaction Data (RX) - Packet 33 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT32 Read Transaction Data (RX) - Packet 32 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT31 Read Transaction Data (RX) - Packet 31 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD9

Address: Operational Base + offset (0x1984)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT38 Read Transaction Data (RX) - Packet 38 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT37 Read Transaction Data (RX) - Packet 37 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT36 Read Transaction Data (RX) - Packet 36 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT35 Read Transaction Data (RX) - Packet 35 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD10

Address: Operational Base + offset (0x1988)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT42 Read Transaction Data (RX) - Packet 42 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT41 Read Transaction Data (RX) - Packet 41 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT40 Read Transaction Data (RX) - Packet 40 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT39 Read Transaction Data (RX) - Packet 39 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD11

Address: Operational Base + offset (0x198C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT46 Read Transaction Data (RX) - Packet 46 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT45 Read Transaction Data (RX) - Packet 45 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT44 Read Transaction Data (RX) - Packet 44 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT43 Read Transaction Data (RX) - Packet 43 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD12

Address: Operational Base + offset (0x1990)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT50 Read Transaction Data (RX) - Packet 50 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT49 Read Transaction Data (RX) - Packet 49 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT48 Read Transaction Data (RX) - Packet 48 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT47 Read Transaction Data (RX) - Packet 47 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD13
Address: Operational Base + offset (0x1994)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT54 Read Transaction Data (RX) - Packet 54 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT53 Read Transaction Data (RX) - Packet 53 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT52 Read Transaction Data (RX) - Packet 52 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT51 Read Transaction Data (RX) - Packet 51 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD14
Address: Operational Base + offset (0x1998)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT58 Read Transaction Data (RX) - Packet 58 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT57 Read Transaction Data (RX) - Packet 57 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT56 Read Transaction Data (RX) - Packet 56 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT55 Read Transaction Data (RX) - Packet 55 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD15
Address: Operational Base + offset (0x199C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT62 Read Transaction Data (RX) - Packet 62 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT61 Read Transaction Data (RX) - Packet 61 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT60 Read Transaction Data (RX) - Packet 60 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT59 Read Transaction Data (RX) - Packet 59 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD16

Address: Operational Base + offset (0x19A0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT66 Read Transaction Data (RX) - Packet 66 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT65 Read Transaction Data (RX) - Packet 65 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT64 Read Transaction Data (RX) - Packet 64 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT63 Read Transaction Data (RX) - Packet 63 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD17

Address: Operational Base + offset (0x19A4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT70 Read Transaction Data (RX) - Packet 70 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT69 Read Transaction Data (RX) - Packet 69 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT68 Read Transaction Data (RX) - Packet 68 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT67 Read Transaction Data (RX) - Packet 67 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD18

Address: Operational Base + offset (0x19A8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT74 Read Transaction Data (RX) - Packet 74 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT73 Read Transaction Data (RX) - Packet 73 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT72 Read Transaction Data (RX) - Packet 72 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT71 Read Transaction Data (RX) - Packet 71 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD19

Address: Operational Base + offset (0x19AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT78 Read Transaction Data (RX) - Packet 78 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT77 Read Transaction Data (RX) - Packet 77 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT76 Read Transaction Data (RX) - Packet 76 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT75 Read Transaction Data (RX) - Packet 75 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD20

Address: Operational Base + offset (0x19B0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT82 Read Transaction Data (RX) - Packet 82 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT81 Read Transaction Data (RX) - Packet 81 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT80 Read Transaction Data (RX) - Packet 80 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT79 Read Transaction Data (RX) - Packet 79 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD21

Address: Operational Base + offset (0x19B4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT86 Read Transaction Data (RX) - Packet 86 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT85 Read Transaction Data (RX) - Packet 85 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT84 Read Transaction Data (RX) - Packet 84 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT83 Read Transaction Data (RX) - Packet 83 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD22

Address: Operational Base + offset (0x19B8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT90 Read Transaction Data (RX) - Packet 90 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT89 Read Transaction Data (RX) - Packet 89 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT88 Read Transaction Data (RX) - Packet 88 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT87 Read Transaction Data (RX) - Packet 87 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD23

Address: Operational Base + offset (0x19BC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT94 Read Transaction Data (RX) - Packet 94 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT93 Read Transaction Data (RX) - Packet 93 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT92 Read Transaction Data (RX) - Packet 92 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT91 Read Transaction Data (RX) - Packet 91 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD24

Address: Operational Base + offset (0x19C0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT98 Read Transaction Data (RX) - Packet 98 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT97 Read Transaction Data (RX) - Packet 97 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT96 Read Transaction Data (RX) - Packet 96 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT95 Read Transaction Data (RX) - Packet 95 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD25

Address: Operational Base + offset (0x19C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT102 Read Transaction Data (RX) - Packet 102 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT101 Read Transaction Data (RX) - Packet 101 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT100 Read Transaction Data (RX) - Packet 100 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT99 Read Transaction Data (RX) - Packet 99 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD26

Address: Operational Base + offset (0x19C8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT106 Read Transaction Data (RX) - Packet 106 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT105 Read Transaction Data (RX) - Packet 105 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT104 Read Transaction Data (RX) - Packet 104 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT103 Read Transaction Data (RX) - Packet 103 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD27

Address: Operational Base + offset (0x19CC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT110 Read Transaction Data (RX) - Packet 110 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT109 Read Transaction Data (RX) - Packet 109 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT108 Read Transaction Data (RX) - Packet 108 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT107 Read Transaction Data (RX) - Packet 107 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD28

Address: Operational Base + offset (0x19D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT114 Read Transaction Data (RX) - Packet 114 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT113 Read Transaction Data (RX) - Packet 113 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT112 Read Transaction Data (RX) - Packet 112 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT111 Read Transaction Data (RX) - Packet 111 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD29

Address: Operational Base + offset (0x19D4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT118 Read Transaction Data (RX) - Packet 118 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT117 Read Transaction Data (RX) - Packet 117 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT116 Read Transaction Data (RX) - Packet 116 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT115 Read Transaction Data (RX) - Packet 115 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD30

Address: Operational Base + offset (0x19D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT122 Read Transaction Data (RX) - Packet 122 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT121 Read Transaction Data (RX) - Packet 121 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT120 Read Transaction Data (RX) - Packet 120 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT119 Read Transaction Data (RX) - Packet 119 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD31

Address: Operational Base + offset (0x19DC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT126 Read Transaction Data (RX) - Packet 126 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT125 Read Transaction Data (RX) - Packet 125 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT124 Read Transaction Data (RX) - Packet 124 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT123 Read Transaction Data (RX) - Packet 123 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD32

Address: Operational Base + offset (0x19E0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT130 Read Transaction Data (RX) - Packet 130 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT129 Read Transaction Data (RX) - Packet 129 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT128 Read Transaction Data (RX) - Packet 128 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT127 Read Transaction Data (RX) - Packet 127 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD33
Address: Operational Base + offset (0x19E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT134 Read Transaction Data (RX) - Packet 134 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT133 Read Transaction Data (RX) - Packet 133 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT132 Read Transaction Data (RX) - Packet 132 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT131 Read Transaction Data (RX) - Packet 131 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD34
Address: Operational Base + offset (0x19E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT138 Read Transaction Data (RX) - Packet 138 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT137 Read Transaction Data (RX) - Packet 137 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT136 Read Transaction Data (RX) - Packet 136 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT135 Read Transaction Data (RX) - Packet 135 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD35
Address: Operational Base + offset (0x19EC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT142 Read Transaction Data (RX) - Packet 142 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT141 Read Transaction Data (RX) - Packet 141 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT140 Read Transaction Data (RX) - Packet 140 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT139 Read Transaction Data (RX) - Packet 139 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD36
Address: Operational Base + offset (0x19F0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT146 Read Transaction Data (RX) - Packet 146 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT145 Read Transaction Data (RX) - Packet 145 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT144 Read Transaction Data (RX) - Packet 144 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT143 Read Transaction Data (RX) - Packet 143 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD37

Address: Operational Base + offset (0x19F4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT150 Read Transaction Data (RX) - Packet 150 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT149 Read Transaction Data (RX) - Packet 149 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT148 Read Transaction Data (RX) - Packet 148 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT147 Read Transaction Data (RX) - Packet 147 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD38

Address: Operational Base + offset (0x19F8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT154 Read Transaction Data (RX) - Packet 154 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT153 Read Transaction Data (RX) - Packet 153 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT152 Read Transaction Data (RX) - Packet 152 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT151 Read Transaction Data (RX) - Packet 151 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD39

Address: Operational Base + offset (0x19FC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT158 Read Transaction Data (RX) - Packet 158 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT157 Read Transaction Data (RX) - Packet 157 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT156 Read Transaction Data (RX) - Packet 156 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT155 Read Transaction Data (RX) - Packet 155 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD40

Address: Operational Base + offset (0x1A00)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT162 Read Transaction Data (RX) - Packet 162 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT161 Read Transaction Data (RX) - Packet 161 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT160 Read Transaction Data (RX) - Packet 160 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT159 Read Transaction Data (RX) - Packet 159 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD41

Address: Operational Base + offset (0x1A04)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT166 Read Transaction Data (RX) - Packet 166 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT165 Read Transaction Data (RX) - Packet 165 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT164 Read Transaction Data (RX) - Packet 164 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT163 Read Transaction Data (RX) - Packet 163 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD42

Address: Operational Base + offset (0x1A08)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT170 Read Transaction Data (RX) - Packet 170 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT169 Read Transaction Data (RX) - Packet 169 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT168 Read Transaction Data (RX) - Packet 168 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT167 Read Transaction Data (RX) - Packet 167 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD43

Address: Operational Base + offset (0x1A0C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT174 Read Transaction Data (RX) - Packet 174 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT173 Read Transaction Data (RX) - Packet 173 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT172 Read Transaction Data (RX) - Packet 172 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT171 Read Transaction Data (RX) - Packet 171 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD44

Address: Operational Base + offset (0x1A10)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT178 Read Transaction Data (RX) - Packet 178 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT177 Read Transaction Data (RX) - Packet 177 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT176 Read Transaction Data (RX) - Packet 176 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT175 Read Transaction Data (RX) - Packet 175 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD45

Address: Operational Base + offset (0x1A14)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT182 Read Transaction Data (RX) - Packet 182 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT181 Read Transaction Data (RX) - Packet 181 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT180 Read Transaction Data (RX) - Packet 180 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT179 Read Transaction Data (RX) - Packet 179 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD46

Address: Operational Base + offset (0x1A18)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT186 Read Transaction Data (RX) - Packet 186 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT185 Read Transaction Data (RX) - Packet 185 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT184 Read Transaction Data (RX) - Packet 184 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT183 Read Transaction Data (RX) - Packet 183 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD47

Address: Operational Base + offset (0x1A1C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT190 Read Transaction Data (RX) - Packet 190 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT189 Read Transaction Data (RX) - Packet 189 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT188 Read Transaction Data (RX) - Packet 188 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT187 Read Transaction Data (RX) - Packet 187 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD48

Address: Operational Base + offset (0x1A20)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT194 Read Transaction Data (RX) - Packet 194 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT193 Read Transaction Data (RX) - Packet 193 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT192 Read Transaction Data (RX) - Packet 192 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT191 Read Transaction Data (RX) - Packet 191 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD49

Address: Operational Base + offset (0x1A24)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT198 Read Transaction Data (RX) - Packet 198 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT197 Read Transaction Data (RX) - Packet 197 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT196 Read Transaction Data (RX) - Packet 196 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT195 Read Transaction Data (RX) - Packet 195 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD50

Address: Operational Base + offset (0x1A28)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT202 Read Transaction Data (RX) - Packet 202 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT201 Read Transaction Data (RX) - Packet 201 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT200 Read Transaction Data (RX) - Packet 200 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT199 Read Transaction Data (RX) - Packet 199 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD51

Address: Operational Base + offset (0x1A2C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT206 Read Transaction Data (RX) - Packet 206 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT205 Read Transaction Data (RX) - Packet 205 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT204 Read Transaction Data (RX) - Packet 204 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT203 Read Transaction Data (RX) - Packet 203 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD52

Address: Operational Base + offset (0x1A30)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT210 Read Transaction Data (RX) - Packet 210 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT209 Read Transaction Data (RX) - Packet 209 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT208 Read Transaction Data (RX) - Packet 208 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT207 Read Transaction Data (RX) - Packet 207 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD53

Address: Operational Base + offset (0x1A34)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT214 Read Transaction Data (RX) - Packet 214 Value After Reset:0x0

Bit	Attr	Reset Value	Description
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT213 Read Transaction Data (RX) - Packet 213 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT212 Read Transaction Data (RX) - Packet 212 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT211 Read Transaction Data (RX) - Packet 211 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD54

Address: Operational Base + offset (0x1A38)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT218 Read Transaction Data (RX) - Packet 218 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT217 Read Transaction Data (RX) - Packet 217 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT216 Read Transaction Data (RX) - Packet 216 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT215 Read Transaction Data (RX) - Packet 215 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD55

Address: Operational Base + offset (0x1A3C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT222 Read Transaction Data (RX) - Packet 222 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT221 Read Transaction Data (RX) - Packet 221 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT220 Read Transaction Data (RX) - Packet 220 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT219 Read Transaction Data (RX) - Packet 219 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD56

Address: Operational Base + offset (0x1A40)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT226 Read Transaction Data (RX) - Packet 226 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT225 Read Transaction Data (RX) - Packet 225 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT224 Read Transaction Data (RX) - Packet 224 Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT223 Read Transaction Data (RX) - Packet 223 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD57
Address: Operational Base + offset (0x1A44)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT230 Read Transaction Data (RX) - Packet 230 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT229 Read Transaction Data (RX) - Packet 229 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT228 Read Transaction Data (RX) - Packet 228 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT227 Read Transaction Data (RX) - Packet 227 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD58
Address: Operational Base + offset (0x1A48)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT234 Read Transaction Data (RX) - Packet 234 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT233 Read Transaction Data (RX) - Packet 233 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT232 Read Transaction Data (RX) - Packet 232 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT231 Read Transaction Data (RX) - Packet 231 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD59
Address: Operational Base + offset (0x1A4C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT238 Read Transaction Data (RX) - Packet 238 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT237 Read Transaction Data (RX) - Packet 237 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT236 Read Transaction Data (RX) - Packet 236 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT235 Read Transaction Data (RX) - Packet 235 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD60
Address: Operational Base + offset (0x1A50)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT242 Read Transaction Data (RX) - Packet 242 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT241 Read Transaction Data (RX) - Packet 241 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT240 Read Transaction Data (RX) - Packet 240 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT239 Read Transaction Data (RX) - Packet 239 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD61
Address: Operational Base + offset (0x1A54)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT246 Read Transaction Data (RX) - Packet 246 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT245 Read Transaction Data (RX) - Packet 245 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT244 Read Transaction Data (RX) - Packet 244 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT243 Read Transaction Data (RX) - Packet 243 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD62
Address: Operational Base + offset (0x1A58)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT250 Read Transaction Data (RX) - Packet 250 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT249 Read Transaction Data (RX) - Packet 249 Value After Reset:0x0
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT248 Read Transaction Data (RX) - Packet 248 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT247 Read Transaction Data (RX) - Packet 247 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD63
Address: Operational Base + offset (0x1A5C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT254 Read Transaction Data (RX) - Packet 254 Value After Reset:0x0
23:16	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT253 Read Transaction Data (RX) - Packet 253 Value After Reset:0x0

Bit	Attr	Reset Value	Description
15:8	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT252 Read Transaction Data (RX) - Packet 252 Value After Reset:0x0
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT251 Read Transaction Data (RX) - Packet 251 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_XACT_RD64

Address: Operational Base + offset (0x1A60)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	EARCRX_CMDC_XACT_RDDATA_PKT255 Read Transaction Data (RX) - Packet 255 Value After Reset:0x0

HDMI TX Controller_EARCRX_CMDC_SYNC_CONFIG

Address: Operational Base + offset (0x1B00)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:8	RW	0x04	EARCRX_CMDC_PULSE_FILTER_DATAOUT_DRV_EN_ACK Pulse filter depth in refclk clock cycles, for input "iearcrx_cmdc_dataout_drv_en_ack" The recommended minimum and maximum values depend on the eARC PHY, check its documentation for reference. Value After Reset:0x4
7:0	RW	0x0e	EARCRX_CMDC_PULSE_FILTER_DATAIN Pulse filter depth in refclk clock cycles, for input "iearcrx_cmdc_datain" The recommended minimum is based on CMDC data rise/fall TeARC_RISE_FALL_CM (max 30ns): Filter depth (min) = ceil((refclk freq in MHz/1000) * 30) The recommended maximum is based on the shortest width of any level (0 or 1) in the eARC CMDC line TeARC_TGL_CM = 475ns. Filter depth (max) = floor((refclk freq in MHz/1000) * 475) Value After Reset:0xe

HDMI TX Controller_EARCRX_DMAC_PHY_CONTROL

Address: Operational Base + offset (0x1C00)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	EARCRX_DMAC_PHY_RCV_EN eARC RX PHY DMAC Receiver enable Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CONFIG

Address: Operational Base + offset (0x1C08)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
7	RW	0x0	EARCRX_DMAC_SAO_I2S_BPCUV_EN Serial Audio Output IF - I2S bit mapping with BPCUV enable Values: 0x0 (SAO_I2SBPCUV_DISABLE): Disabled 0x1 (SAO_I2SBPCUV_ENABLE): Enabled Value After Reset:0x0
6	RW	0x0	EARCRX_DMAC_SAO_I2S_EN Serial Audio Output IF - I2S enable Note 1:This audio interface supports the following audio types referred in the HDMI Enhanced Audio Return Channel section of the HDMI 2.1 Specification: 2-channel L-PCM (I2S pairs enabled: 1) 8-channel L-PCM (I2S pairs enabled: 4) Compressed Audio Layout A (I2S pairs enabled: 1) Compressed Audio Layout B (I2S pairs enabled: 1) Values: 0x0 (SAO_I2S_DISABLE): Disabled 0x1 (SAO_I2S_ENABLE): Enabled Value After Reset:0x0
5	RW	0x0	EARCRX_DMAC_SAO_SPDIF_EN Serial Audio Output IF - S/PDIF enable Note:This audio interface supports the following audio types referred in the HDMI Enhanced Audio Return Channel section of the HDMI 2.1 Specification: 2-channel L-PCM (S/PDIF pairs enabled: 1) 8-channel L-PCM (S/PDIF pairs enabled: 4) Compressed Audio Layout A (S/PDIF pairs enabled: 1) Compressed Audio Layout B (S/PDIF pairs enabled: 1) Values: 0x0 (SAO_SPDIF_DISABLE): Disabled 0x1 (SAO_SPDIF_ENABLE): Enabled Value After Reset:0x0
4	RW	0x0	EARCRX_DMAC_PAO_EN Parallel Audio Output IF (PAO) enable Note 1:This audio interface supports all audio types referred in the HDMI Enhanced Audio Return Channel section of the HDMI 2.1 Specification. Values: 0x0 (PAO_DISABLE): Disabled 0x1 (PAO_ENABLE): Enabled Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	EARCRX_DMAC_ECC_INV_SYNDBITORDER Invert ECC bit order, relative to the last stage on the LFSR syndrome generator as the LFSR-MSb: Values: 0x0 (ECCBITORD_MSBFIRST): LFSR-MSb sent first 0x1 (ECCBITORD_LSBFIRST): LFSR-LSb sent first Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RW	0x1	EARCRX_DMAC_ECC_ERRCORRECT_EN ECC Error Correction enable for Compressed Audio Values: 0x0 (ECCERR_COMPAUD_DISABLE): Disabled - The received ECC syndrome bits are only checked against the locally calculated syndrome. 0x1 (ECCERR_COMPAUD_ENABLE): Enabled - The received ECC syndrome is used to correct bit errors in the Compressed Audio sample. Value After Reset:0x1

HDMI TX Controller_EARCRX_DMAC_CONTROL0

Address: Operational Base + offset (0x1C0C)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	Reserved1 Reserved Field:Yes
9:5	RW	0x00	EARCRX_DMAC_AUDIO_TYPE_OVR_VALUE Audio type override value: Note 1: Others values not listed are reserved Values: 0x0 (UNKNOWN): Unknown 0x1 (LPCM_2CH): Unencrypted L-PCM 2-ch 0x2 (MULTI_LPCM_2CH): Unencrypted Multi-Channel L-PCM 2-ch 0x3 (MULTI_LPCM_8CH): Unencrypted Multi-Channel L-PCM 8-ch 0x4 (MULTI_LPCM_16CH): Unencrypted Multi-Channel L-PCM 16-ch 0x5 (MULTI_LPCM_32CH): Unencrypted Multi-Channel L-PCM 32-ch 0x6 (OBA_6CH): Unencrypted OBA 6-ch 0x7 (OBA_12CH): Unencrypted OBA 12-ch 0x8 (CAUD_A): Unencrypted Compressed Audio Layout A 0x9 (CAUD_B): Unencrypted Compressed Audio Layout B 0xa (ENC_MULTI_LPCM_2CH): Encrypted Multi-Channel L-PCM 2-ch 0xb (ENC_MULTI_LPCM_8CH): Encrypted Multi-Channel L-PCM 8-ch 0xc (ENC_MULTI_LPCM_16CH): Encrypted Multi-Channel L-PCM 16-ch 0xd (ENC_MULTI_LPCM_32CH): Encrypted Multi-Channel L-PCM 32-ch 0xe (ENC_OBA_6CH): Encrypted OBA 6-ch 0xf (ENC_OBA_12CH): Encrypted OBA 12-ch 0x10 (ENC_CAUD_A): Encrypted Compressed Audio Layout A 0x11 (ENC_CAUD_B): Encrypted Compressed Audio Layout B Value After Reset:0x0
4	RW	0x0	EARCRX_DMAC_AUDIO_TYPE_OVR_EN Audio type override enable Values: 0x0 (DMAC_AUDTYPE_OVR_DISABLE): Disabled 0x1 (DMAC_AUDTYPE_OVR_ENABLE): Enabled Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
1	RW	0x0	EARCRX_DMAC_AUDIO_EN Audio output interfaces enable Values: 0x0 (DMAC_OUTIF_DISABLE): Disabled 0x1 (DMAC_OUTIF_ENABLE): Enabled Value After Reset:0x0
0	RW	0x1	EARCRX_DMAC_EN eARC RX DMAC Audio datapath enable Values: 0x0 (DMAC_AUDIO_DISABLE): Disabled 0x1 (DMAC_AUDIO_ENABLE): Enabled Value After Reset:0x1

HDMI TX Controller_EARCRX_DMAC_CONTROL1

Address: Operational Base + offset (0x1C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHANNEL_ALLOC Audio channel enable (up to 32 channel) Note 1: MSB: channel 32, LSB: channel 1 Note 2:The highest channel index must be aligned with DMAC audio type (e.g. for Multi-Channel L-PCM 16-ch, the highest channel index is 16). Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_STATUS

Address: Operational Base + offset (0x1C14)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved2 Reserved Field:Yes
13:12	RO	0x0	EARCRX_DMAC_EARC_BPCLK_MFACTOR eARC biphase clock frequency multiplication factor in relation to the eARC audio clock frequency (=128*Fs) of the incoming audio stream: Values: 0x0 (EARCBIPHASE0): eARC biphase = 1*eARC audio 0x1 (EARCBIPHASE1): eARC biphase = 4*eARC audio 0x2 (EARCBIPHASE2): eARC biphase = 8*eARC audio 0x3 (EARCBIPHASE3): eARC biphase = 16*eARC audio Value After Reset:0x0
11:9	RW	0x0	Reserved1 Reserved Field:Yes
8	RO	0x0	EARCRX_DMAC_AUDIO_MUTE_ST Audio mute status of the incoming audio stream Note:Changing this field register is followed by the interrupt earcrx_dmac_audio_mute_chg_irq. Values: 0x0 (AUDMUTE_NOTASSERT): Channel Status MUTE bit not asserted for at least two IEC 60958-1 blocks 0x1 (AUDMUTE_ASSERT): Channel Status MUTE bit asserted for at least two IEC 60958-1 blocks Value After Reset:0x0
7:5	RW	0x0	Reserved0 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4:0	RO	0x00	EARCRX_DMAC_AUDIO_TYPE_ST Audio type of the incoming audio stream Note 1: Others values not listed are reserved Note 2:Changing this field register is followed by the interrupt earcrx_dmac_audio_type_chg_irq Values: 0x0 (UNKNOWN): Unknown 0x1 (LPCM_2CH): Unencrypted L-PCM 2-ch 0x2 (MULTI_LPCM_2CH): Unencrypted Multi-Channel L-PCM 2-ch 0x3 (MULTI_LPCM_8CH): Unencrypted Multi-Channel L-PCM 8-ch 0x4 (MULTI_LPCM_16CH): Unencrypted Multi-Channel L-PCM 16-ch 0x5 (MULTI_LPCM_32CH): Unencrypted Multi-Channel L-PCM 32-ch 0x6 (OBA_6CH): Unencrypted OBA 6-ch 0x7 (OBA_12CH): Unencrypted OBA 12-ch 0x8 (CAUD_A): Unencrypted Compressed Audio Layout A 0x9 (CAUD_B): Unencrypted Compressed Audio Layout B 0xa (ENC_MULTI_LPCM_2CH): Encrypted Multi-Channel L-PCM 2-ch 0xb (ENC_MULTI_LPCM_8CH): Encrypted Multi-Channel L-PCM 8-ch 0xc (ENC_MULTI_LPCM_16CH): Encrypted Multi-Channel L-PCM 16-ch 0xd (ENC_MULTI_LPCM_32CH): Encrypted Multi-Channel L-PCM 32-ch 0xe (ENC_OBA_6CH): Encrypted OBA 6-ch 0xf (ENC_OBA_12CH): Encrypted OBA 12-ch 0x10 (ENC_CAUD_A): Encrypted Compressed Audio Layout A 0x11 (ENC_CAUD_B): Encrypted Compressed Audio Layout B Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS0

Address: Operational Base + offset (0x1C18)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_CHSTATUS_3_0 Audio Channel Status bytes 3 to 0 Note 1: Any change of Channel Status payload is followed by the interrupt earcrx_dmac_chstatus_block_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS1

Address: Operational Base + offset (0x1C1C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_CHSTATUS_7_4 Audio Channel Status bytes 7 to 4 Note 1: Any change of Channel Status payload is followed by the interrupt earcrx_dmac_chstatus_block_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS2

Address: Operational Base + offset (0x1C20)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_CHSTATUS_11_8 Audio Channel Status bytes 11 to 8 Note 1: Any change of Channel Status payload is followed by the interrupt earcrx_dmac_chstatus_block_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS3

Address: Operational Base + offset (0x1C24)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_CHSTATUS_15_12 Audio Channel Status bytes 15 to 12 Note 1: Any change of Channel Status payload is followed by the interrupt earcrx_dmac_chstatus_block_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS4

Address: Operational Base + offset (0x1C28)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_CHSTATUS_19_16 Audio Channel Status bytes 19 to 16 Note 1: Any change of Channel Status payload is followed by the interrupt earcrx_dmac_chstatus_block_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS5

Address: Operational Base + offset (0x1C2C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_CHSTATUS_23_20 Audio Channel Status bytes 23 to 20 Note 1: Any change of Channel Status payload is followed by the interrupt earcrx_dmac_chstatus_block_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT0

Address: Operational Base + offset (0x1C30)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_4_1_ST User Data HDMI 1.4b ACP message payload IUs 4 to 1 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 1, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 4. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT1

Address: Operational Base + offset (0x1C34)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_8_5_ST User Data HDMI 1.4b ACP message payload IUs 8 to 5 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 5, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 8. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT2
Address: Operational Base + offset (0x1C38)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_12_9_ST User Data HDMI 1.4b ACP message payload IUs 12 to 9 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 9, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 12. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT3
Address: Operational Base + offset (0x1C3C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_16_13_ST User Data HDMI 1.4b ACP message payload IUs 16 to 13 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 13, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 16. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT4
Address: Operational Base + offset (0x1C40)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_20_17_ST User Data HDMI 1.4b ACP message payload IUs 20 to 17 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 17, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 20. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT5
Address: Operational Base + offset (0x1C44)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_24_21_ST User Data HDMI 1.4b ACP message payload IUs 24 to 21 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 21, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 24. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT6

Address: Operational Base + offset (0x1C48)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_28_25_ST User Data HDMI 1.4b ACP message payload IUs 28 to 25 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 25, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 28. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT7

Address: Operational Base + offset (0x1C4C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_32_29_ST User Data HDMI 1.4b ACP message payload IUs 32 to 29 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 29, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 32. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT8

Address: Operational Base + offset (0x1C50)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_36_33_ST User Data HDMI 1.4b ACP message payload IUs 36 to 33 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 33, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 36. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT9

Address: Operational Base + offset (0x1C54)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_40_37_ST User Data HDMI 1.4b ACP message payload IUs 40 to 37 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 37, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 40. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT10

Address: Operational Base + offset (0x1C58)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_44_41_ST User Data HDMI 1.4b ACP message payload IUs 44 to 41 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 41, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 44. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT11

Address: Operational Base + offset (0x1C5C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:0	RO	0x000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_PKT_IU_47_45_ST User Data HDMI 1.4b ACP message payload IUs 47 to 45 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 45, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 47. Note 2: Any change of User Data HDMI 1.4b ACP message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT0

Address: Operational Base + offset (0x1C60)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_4_1_ST User Data HDMI 1.4b ISRC1 message payload IUs 4 to 1 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 1, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 4. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT1

Address: Operational Base + offset (0x1C64)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_8_5_ST User Data HDMI 1.4b ISRC1 message payload IUs 8 to 5 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 5, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 8. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT2

Address: Operational Base + offset (0x1C68)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_12_9_ST User Data HDMI 1.4b ISRC1 message payload IUs 12 to 9 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 9, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 12. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT3

Address: Operational Base + offset (0x1C6C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_16_13_ST User Data HDMI 1.4b ISRC1 message payload IUs 16 to 13 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 13, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 16. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT4

Address: Operational Base + offset (0x1C70)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_20_17_ST User Data HDMI 1.4b ISRC1 message payload IUs 20 to 17 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 17, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 20. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT5

Address: Operational Base + offset (0x1C74)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_24_21_ST User Data HDMI 1.4b ISRC1 message payload IUs 24 to 21 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 21, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 24. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT6

Address: Operational Base + offset (0x1C78)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_28_25_ST User Data HDMI 1.4b ISRC1 message payload IUs 28 to 25 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 25, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 28. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT7

Address: Operational Base + offset (0x1C7C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_32_29_ST User Data HDMI 1.4b ISRC1 message payload IUs 32 to 29 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 29, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 32. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT8

Address: Operational Base + offset (0x1C80)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_36_33_ST User Data HDMI 1.4b ISRC1 message payload IUs 36 to 33 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 33, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 36. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT9

Address: Operational Base + offset (0x1C84)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_40_37_ST User Data HDMI 1.4b ISRC1 message payload IUs 40 to 37 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 37, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 40. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT10
Address: Operational Base + offset (0x1C88)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_44_41_ST User Data HDMI 1.4b ISRC1 message payload IUs 44 to 41 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 41, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 44. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT11
Address: Operational Base + offset (0x1C8C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:0	RO	0x000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_PKT_IU_47_45_ST User Data HDMI 1.4b ISRC1 message payload IUs 47 to 45 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 45, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 47. Note 2: Any change of User Data HDMI 1.4b ISRC1 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT0
Address: Operational Base + offset (0x1C90)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_4_1_ST User Data HDMI 1.4b ISRC2 message payload IUs 4 to 1 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 1, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 4. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT1
Address: Operational Base + offset (0x1C94)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_8_5_ST User Data HDMI 1.4b ISRC2 message payload IUs 8 to 5 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 5, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 8. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT2

Address: Operational Base + offset (0x1C98)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_12_9_ST User Data HDMI 1.4b ISRC2 message payload IUs 12 to 9 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 9, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 12. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT3

Address: Operational Base + offset (0x1C9C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_16_13_ST User Data HDMI 1.4b ISRC2 message payload IUs 16 to 13 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 13, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 16. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT4

Address: Operational Base + offset (0x1CA0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_20_17_ST User Data HDMI 1.4b ISRC2 message payload IUs 20 to 17 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 17, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 20. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT5

Address: Operational Base + offset (0x1CA4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_24_21_ST User Data HDMI 1.4b ISRC2 message payload IUs 24 to 21 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 21, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 24. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT6

Address: Operational Base + offset (0x1CA8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_28_25_ST User Data HDMI 1.4b ISRC2 message payload IUs 28 to 25 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 25, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 28. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT7

Address: Operational Base + offset (0x1CAC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_32_29_ST User Data HDMI 1.4b ISRC2 message payload IUs 32 to 29 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 29, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 32. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT8

Address: Operational Base + offset (0x1CB0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_36_33_ST User Data HDMI 1.4b ISRC2 message payload IUs 36 to 33 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 33, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 36. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT9

Address: Operational Base + offset (0x1CB4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_40_37_ST User Data HDMI 1.4b ISRC2 message payload IUs 40 to 37 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 37, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 40. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT10
Address: Operational Base + offset (0x1CB8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_44_41_ST User Data HDMI 1.4b ISRC2 message payload IUs 44 to 41 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 41, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 44. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT11
Address: Operational Base + offset (0x1CBC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved0 Reserved Field:Yes
23:0	RO	0x000000	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_PKT_IU_47_45_ST User Data HDMI 1.4b ISRC2 message payload IUs 47 to 45 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 45, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 47. Note 2: Any change of User Data HDMI 1.4b ISRC2 message payload is followed by the interrupt earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC0
Address: Operational Base + offset (0x1CC0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_4_1_ST User Data Generic message payload IUs 4 to 1 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 1, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 4. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC1
Address: Operational Base + offset (0x1CC4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_8_5_ST User Data Generic message payload IUs 8 to 5 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 5, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 8. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC2

Address: Operational Base + offset (0x1CC8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_12_9_ST User Data Generic message payload IUs 12 to 9 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 9, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 12. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC3

Address: Operational Base + offset (0x1CCC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_16_13_ST User Data Generic message payload IUs 16 to 13 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 13, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 16. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC4

Address: Operational Base + offset (0x1CD0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_20_17_ST User Data Generic message payload IUs 20 to 17 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 17, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 20. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC5

Address: Operational Base + offset (0x1CD4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_24_21_ST User Data Generic message payload IUs 24 to 21 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 21, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 24. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC6

Address: Operational Base + offset (0x1CD8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_28_25_ST User Data Generic message payload IUs 28 to 25 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 25, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 28. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC7

Address: Operational Base + offset (0x1CDC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_32_29_ST User Data Generic message payload IUs 32 to 29 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 29, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 32. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC8

Address: Operational Base + offset (0x1CE0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_36_33_ST User Data Generic message payload IUs 36 to 33 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 33, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 36. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC9

Address: Operational Base + offset (0x1CE4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_40_37_ST User Data Generic message payload IUs 40 to 37 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 37, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 40. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC10

Address: Operational Base + offset (0x1CE8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_44_41_ST User Data Generic message payload IUs 44 to 41 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 41, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 44. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC11

Address: Operational Base + offset (0x1CEC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_48_45_ST User Data Generic message payload IUs 48 to 45 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 45, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 48. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC12

Address: Operational Base + offset (0x1CF0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_52_49_ST User Data Generic message payload IUs 52 to 49 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 49, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 52. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC13

Address: Operational Base + offset (0x1CF4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_56_53_ST User Data Generic message payload IUs 56 to 53 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 53, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 56. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC14

Address: Operational Base + offset (0x1CF8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_60_57_ST User Data Generic message payload IUs 60 to 57 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 57, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 60. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC15

Address: Operational Base + offset (0x1CFC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_64_61_ST User Data Generic message payload IUs 64 to 61 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 61, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 64. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC16

Address: Operational Base + offset (0x1D00)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_68_65_ST User Data Generic message payload IUs 68 to 65 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 65, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 68. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC17

Address: Operational Base + offset (0x1D04)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_72_69_ST User Data Generic message payload IUs 72 to 69 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 69, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 72. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC18

Address: Operational Base + offset (0x1D08)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_76_73_ST User Data Generic message payload IUs 76 to 73 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 73, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 76. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC19

Address: Operational Base + offset (0x1D0C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_80_77_ST User Data Generic message payload IUs 80 to 77 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 77, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 80. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC20

Address: Operational Base + offset (0x1D10)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_84_81_ST User Data Generic message payload IUs 84 to 81 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 81, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 84. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC21

Address: Operational Base + offset (0x1D14)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_88_85_ST User Data Generic message payload IUs 88 to 85 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 85, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 88. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC22

Address: Operational Base + offset (0x1D18)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_92_89_ST User Data Generic message payload IUs 92 to 89 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 89, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 92. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC23

Address: Operational Base + offset (0x1D1C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_96_93_ST User Data Generic message payload IUs 96 to 93 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 93, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 96. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC24

Address: Operational Base + offset (0x1D20)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_100_97_ST User Data Generic message payload IUs 100 to 97 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 97, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 100. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC25

Address: Operational Base + offset (0x1D24)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_104_101_ST User Data Generic message payload IUs 104 to 101 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 101, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 104. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC26

Address: Operational Base + offset (0x1D28)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_108_105_ST User Data Generic message payload IUs 108 to 105 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 105, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 108. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC27

Address: Operational Base + offset (0x1D2C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_112_109_ST User Data Generic message payload IUs 112 to 109 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 109, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 112. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC28

Address: Operational Base + offset (0x1D30)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_116_113_ST User Data Generic message payload IUs 116 to 113 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 113, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 116. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC29

Address: Operational Base + offset (0x1D34)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_120_117_ST User Data Generic message payload IUs 120 to 117 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 117, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 120. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC30

Address: Operational Base + offset (0x1D38)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_124_121_ST User Data Generic message payload IUs 124 to 121 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 121, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 124. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC31

Address: Operational Base + offset (0x1D3C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_128_125_ST User Data Generic message payload IUs 128 to 125 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 125, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 128. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_MSG_GENERIC32

Address: Operational Base + offset (0x1D40)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RO	0x00	EARCRX_DMAC_USRDATA_MSG_GENERIC_IU_129_ST User Data Generic message payload IUs 129 Note 1: The LSB (bit) of the 32-bit word corresponds to bit "W" of Information Unit 129, and the MSB (bit) of the 32-bit word corresponds to "start" bit of Information Unit 129. Note 2: Any change of User Data Generic message payload is followed by the interrupt earcrx_dmac_usrdata_msg_generic_chg_irq. Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER0

Address: Operational Base + offset (0x1D44)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved0 Reserved Field:Yes
15:0	RW	0x0000	EARCRX_DMAC_CHSTATUS_STREAMER_COMMON_BYTES1_0 Common Audio Channel Status payload bytes 0 (LSB byte) to 1 Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER1
Address: Operational Base + offset (0x1D48)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_COMMON_BYTES6_3 Common Audio Channel Status payload bytes 3 (LSB byte) to 6 (MSB byte) Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER2
Address: Operational Base + offset (0x1D4C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_COMMON_BYTES10_7 Common Audio Channel Status payload bytes 7 (LSB byte) to 10 (MSB byte) Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER3
Address: Operational Base + offset (0x1D50)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_COMMON_BYTES14_11 Common Audio Channel Status payload bytes 11 (LSB byte) to 14 (MSB byte) Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER4
Address: Operational Base + offset (0x1D54)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_COMMON_BYTES18_15 Common Audio Channel Status payload bytes 15 (LSB byte) to 18 (MSB byte) Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER5
Address: Operational Base + offset (0x1D58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_COMMON_BYTES22_19 Common Audio Channel Status payload bytes 19 (LSB byte) to 22 (MSB byte) Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER6
Address: Operational Base + offset (0x1D5C)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	EARCRX_DMAC_CHSTATUS_STREAMER_COMMON_BYTES23 Common Audio Channel Status payload byte 23 (LSB byte) Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER7
Address: Operational Base + offset (0x1D60)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS4_1_BYTE2 Channels 1 (LSB byte) to 4 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER8
Address: Operational Base + offset (0x1D64)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS8_5_BYTE2 Channels 5 (LSB byte) to 8 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER9
Address: Operational Base + offset (0x1D68)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS12_9_BYTE2 Channels 9 (LSB byte) to 12 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER10
Address: Operational Base + offset (0x1D6C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS16_13_BYTE2 Channels 13 (LSB byte) to 16 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER11
Address: Operational Base + offset (0x1D70)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS20_17_BYTE2 Channels 17 (LSB byte) to 20 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER12
Address: Operational Base + offset (0x1D74)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS24_21_BYTE2 Channels 21 (LSB byte) to 24 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER13
Address: Operational Base + offset (0x1D78)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS28_25_BYTE2 Channels 25 (LSB byte) to 28 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_CHSTATUS_STREAMER14
Address: Operational Base + offset (0x1D7C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EARCRX_DMAC_CHSTATUS_STREAMER_CHANNELS32_29_BYTE2 Channels 29 (LSB byte) to 32 (MSB byte) - Audio Channel Status block payload byte 2 {Source Number, Channel Number} Value After Reset:0x0

HDMI TX Controller_EARCRX_DMAC_USRDATA_STREAMER0
Address: Operational Base + offset (0x1D80)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	EARCRX_DMAC_USRDATA_STREAMER_TXMODE User Data Streamer transmission mode Note 1: The User Data Content received from eARC incoming stream are available in the following registers: earcrx_dmac_usrdata_msg_hdmi_acp/isrc1/isrc2_pkt11..0, earcrx_dmac_usrdata_msg_generic32..0. Values: 0x0 (UDATA_FORCE_ZEROS): Force sending zeros in all User Data bits of IEC 60958 subframes. 0x1 (UDATA_TRANSMIT): Transmit User Data Content received from eARC incoming stream (H14b ACP, ISRC1, ISRC2 and Generic (129 Ius) U-bits messages). Value After Reset:0x0

HDMI TX Controller_MAIN_INTVEC_INDEX
Address: Operational Base + offset (0x3000)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RO	0x0	MAINUNIT_1_INTVEC Main unit 1 Interrupt Vector triggered Value After Reset:0x0
0	RO	0x0	MAINUNIT_0_INTVEC Main unit 0 Interrupt Vector triggered Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_STATUS
Address: Operational Base + offset (0x3010)

Bit	Attr	Reset Value	Description
31	RO	0x0	APB_REGBANK_READY_IRQ Register Bank ready interrupt. Indicates all non-powered off units between AVPUNIT, PKTFIFO, and CEC (HDMI_QP_TX_CEC configs only) are ready. Value After Reset:0x0
30	RW	0x0	Reserved3 Reserved Field:Yes
29	RO	0x0	RESET_MANAGER_STATUS_END_IRQ Reset Manager Init_n/Disable end interrupt Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
24	RO	0x0	TIMER_BASE_LOCKED_IRQ Timer Base locked interrupt Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes
22	RO	0x0	EARC_BPCLK_VALID_STABLE_CHG_IRQ eARC RX Biphase Clock (earc_bpclk) valid change interrupt. Value After Reset:0x0
21	RO	0x0	EARC_BPCLK_OFF_CHG_IRQ eARC RX Biphase Clock (earc_bpclk) is off (not running) change interrupt. Value After Reset:0x0
20	RO	0x0	EARC_BPCLK_LOCKED_CHG_IRQ eARC RX Biphase Clock (earc_bpclk) locked change interrupt. Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	RO	0x0	AUDCLK_OFF_CHG_IRQ Audio Clock (audclk) is off (not running) change interrupt. Value After Reset:0x0
6	RO	0x0	AUDCLK_LOCKED_CHG_IRQ Audio Clock (audclk) locked change interrupt. Value After Reset:0x0
5	RO	0x0	LINKQPCLK_OFF_CHG_IRQ Link QP Clock (linkqpclk) is off (not running) change interrupt. Value After Reset:0x0
4	RO	0x0	LINKQPCLK_LOCKED_CHG_IRQ Link QP Clock (linkqpclk) locked change interrupt. Value After Reset:0x0
3	RO	0x0	VIDQPCLK_OFF_CHG_IRQ Video QP Clock (vidqpclk) is off (not running) change interrupt. Value After Reset:0x0
2	RO	0x0	VIDQPCLK_LOCKED_CHG_IRQ Video QP Clock (vidqpclk) locked change interrupt. Value After Reset:0x0
1	RO	0x0	IPI_CLK_OFF_CHG_IRQ IPI Clock (ipi_clk) is off (not running) change interrupt. Value After Reset:0x0
0	RO	0x0	IPI_CLK_LOCKED_CHG_IRQ IPI Clock (ipi_clk) locked change interrupt. Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_MASK_N

Address: Operational Base + offset (0x3014)

Bit	Attr	Reset Value	Description
31	RW	0x1	APB_REGBANK_READY_MASK_N Mask for apb_regbank_ready_irq. Values: 0x0 (MASK): Write 0 to mask apb_regbank_ready_irq. 0x1 (UNMASK): Write 1 to unmask apb_regbank_ready_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x1
30	RW	0x0	Reserved3 Reserved Field:Yes

Bit	Attr	Reset Value	Description
29	RW	0x0	RESET_MANAGER_STATUS_END_MASK_N Mask for reset_manager_status_end_irq. Values: 0x0 (MASK): Write 0 to mask reset_manager_status_end_irq. 0x1 (UNMASK): Write 1 to unmask reset_manager_status_end_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes
24	RW	0x0	TIMER_BASE_LOCKED_MASK_N Mask for timer_base_locked_irq. Values: 0x0 (MASK): Write 0 to mask timer_base_locked_irq. 0x1 (UNMASK): Write 1 to unmask timer_base_locked_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes
22	RW	0x0	EARC_BPCLK_VALID_STABLE_CHG_MASK_N Mask for earc_bpclk_valid_stable_chg_irq. Values: 0x0 (MASK): Write 0 to mask earc_bpclk_valid_stable_chg_irq. 0x1 (UNMASK): Write 1 to unmask earc_bpclk_valid_stable_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
21	RW	0x0	EARC_BPCLK_OFF_CHG_MASK_N Mask for earc_bpclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask earc_bpclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask earc_bpclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
20	RW	0x0	EARC_BPCLK_LOCKED_CHG_MASK_N Mask for earc_bpclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask earc_bpclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask earc_bpclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	RW	0x0	AUDCLK_OFF_CHG_MASK_N Mask for audclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask audclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask audclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
6	RW	0x0	AUDCLK_LOCKED_CHG_MASK_N Mask for audclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask audclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask audclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	LINKQPCLK_OFF_CHG_MASK_N Mask for linkqpclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask linkqpclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask linkqpclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	LINKQPCLK_LOCKED_CHG_MASK_N Mask for linkqpclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask linkqpclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask linkqpclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	VIDQPCLK_OFF_CHG_MASK_N Mask for vidqpclk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask vidqpclk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask vidqpclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	VIDQPCLK_LOCKED_CHG_MASK_N Mask for vidqpclk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask vidqpclk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask vidqpclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	IPI_CLK_OFF_CHG_MASK_N Mask for ipi_clk_off_chg_irq. Values: 0x0 (MASK): Write 0 to mask ipi_clk_off_chg_irq. 0x1 (UNMASK): Write 1 to unmask ipi_clk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	IPI_CLK_LOCKED_CHG_MASK_N Mask for ipi_clk_locked_chg_irq. Values: 0x0 (MASK): Write 0 to mask ipi_clk_locked_chg_irq. 0x1 (UNMASK): Write 1 to unmask ipi_clk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_CLEAR

Address: Operational Base + offset (0x3018)

Bit	Attr	Reset Value	Description
31	WO	0x0	APB_REGBANK_READY_CLEAR Clear for apb_regbank_ready_irq Values: 0x1 (CLEAR): Write 1 to clear apb_regbank_ready_irq Value After Reset:0x0
30	RW	0x0	Reserved3 Reserved Field:Yes
29	WO	0x0	RESET_MANAGER_STATUS_END_CLEAR Clear for reset_manager_status_end_irq Values: 0x1 (CLEAR): Write 1 to clear reset_manager_status_end_irq Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes
24	WO	0x0	TIMER_BASE_LOCKED_CLEAR Clear for timer_base_locked_irq Values: 0x1 (CLEAR): Write 1 to clear timer_base_locked_irq Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes
22	WO	0x0	EARC_BPCLK_VALID_STABLE_CHG_CLEAR Clear for earc_bpclk_valid_stable_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earc_bpclk_valid_stable_chg_irq Value After Reset:0x0
21	WO	0x0	EARC_BPCLK_OFF_CHG_CLEAR Clear for earc_bpclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earc_bpclk_off_chg_irq Value After Reset:0x0
20	WO	0x0	EARC_BPCLK_LOCKED_CHG_CLEAR Clear for earc_bpclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earc_bpclk_locked_chg_irq Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	WO	0x0	AUDCLK_OFF_CHG_CLEAR Clear for audclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear audclk_off_chg_irq Value After Reset:0x0
6	WO	0x0	AUDCLK_LOCKED_CHG_CLEAR Clear for audclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear audclk_locked_chg_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
5	WO	0x0	LINKQPCLK_OFF_CHG_CLEAR Clear for linkqpclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear linkqpclk_off_chg_irq Value After Reset:0x0
4	WO	0x0	LINKQPCLK_LOCKED_CHG_CLEAR Clear for linkqpclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear linkqpclk_locked_chg_irq Value After Reset:0x0
3	WO	0x0	VIDQPCLK_OFF_CHG_CLEAR Clear for vidqpclk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear vidqpclk_off_chg_irq Value After Reset:0x0
2	WO	0x0	VIDQPCLK_LOCKED_CHG_CLEAR Clear for vidqpclk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear vidqpclk_locked_chg_irq Value After Reset:0x0
1	WO	0x0	IPI_CLK_OFF_CHG_CLEAR Clear for ipi_clk_off_chg_irq Values: 0x1 (CLEAR): Write 1 to clear ipi_clk_off_chg_irq Value After Reset:0x0
0	WO	0x0	IPI_CLK_LOCKED_CHG_CLEAR Clear for ipi_clk_locked_chg_irq Values: 0x1 (CLEAR): Write 1 to clear ipi_clk_locked_chg_irq Value After Reset:0x0

HDMI TX Controller_MAINUNIT_0_INT_FORCE
Address: Operational Base + offset (0x301C)

Bit	Attr	Reset Value	Description
31	WO	0x0	APB_REGBANK_READY_FORCE Force for apb_regbank_ready_irq Values: 0x1 (FORCE): Write 1 to trigger apb_regbank_ready_irq Value After Reset:0x0
30	RW	0x0	Reserved3 Reserved Field:Yes
29	WO	0x0	RESET_MANAGER_STATUS_END_FORCE Force for reset_manager_status_end_irq Values: 0x1 (FORCE): Write 1 to trigger reset_manager_status_end_irq Value After Reset:0x0
28:25	RW	0x0	Reserved2 Reserved Field:Yes
24	WO	0x0	TIMER_BASE_LOCKED_FORCE Force for timer_base_locked_irq Values: 0x1 (FORCE): Write 1 to trigger timer_base_locked_irq Value After Reset:0x0
23	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22	WO	0x0	EARC_BPCLK_VALID_STABLE_CHG_FORCE Force for earc_bpclk_valid_stable_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earc_bpclk_valid_stable_chg_irq Value After Reset:0x0
21	WO	0x0	EARC_BPCLK_OFF_CHG_FORCE Force for earc_bpclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earc_bpclk_off_chg_irq Value After Reset:0x0
20	WO	0x0	EARC_BPCLK_LOCKED_CHG_FORCE Force for earc_bpclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earc_bpclk_locked_chg_irq Value After Reset:0x0
19:8	RW	0x000	Reserved0 Reserved Field:Yes
7	WO	0x0	AUDCLK_OFF_CHG_FORCE Force for audclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger audclk_off_chg_irq Value After Reset:0x0
6	WO	0x0	AUDCLK_LOCKED_CHG_FORCE Force for audclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger audclk_locked_chg_irq Value After Reset:0x0
5	WO	0x0	LINKQPCLK_OFF_CHG_FORCE Force for linkqpclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger linkqpclk_off_chg_irq Value After Reset:0x0
4	WO	0x0	LINKQPCLK_LOCKED_CHG_FORCE Force for linkqpclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger linkqpclk_locked_chg_irq Value After Reset:0x0
3	WO	0x0	VIDQPCLK_OFF_CHG_FORCE Force for vidqpclk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger vidqpclk_off_chg_irq Value After Reset:0x0
2	WO	0x0	VIDQPCLK_LOCKED_CHG_FORCE Force for vidqpclk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger vidqpclk_locked_chg_irq Value After Reset:0x0
1	WO	0x0	IPI_CLK_OFF_CHG_FORCE Force for ipi_clk_off_chg_irq Values: 0x1 (FORCE): Write 1 to trigger ipi_clk_off_chg_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	WO	0x0	IPI_CLK_LOCKED_CHG_FORCE Force for ipi_clk_locked_chg_irq Values: 0x1 (FORCE): Write 1 to trigger ipi_clk_locked_chg_irq Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_STATUS

Address: Operational Base + offset (0x3020)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes
22	RO	0x0	FLT_EXIT_TO_LTSL_IRQ Indicates a transition from FRL Link Training LTS:3 to LTS:L Value After Reset:0x0
21	RO	0x0	FLT_EXIT_TO_LTS4_IRQ Indicates a transition from FRL Link Training LTS:3 to LTS:4 Value After Reset:0x0
20	RO	0x0	FLT_EXIT_TO_LTSP_IRQ Indicates a transition from FRL Link Training LTS:3 to LTS:P Value After Reset:0x0
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	RO	0x0	SCDC_NACK_RCVD_IRQ Indicates that SCDC has received a NACK from I2C Master Value After Reset:0x0
11	RO	0x0	SCDC_RR_REPLY_STOP_IRQ Indicates that Source has replied with STOP to a Read Request Value After Reset:0x0
10	RO	0x0	SCDC_UPD_FLAGS_CLR_IRQ Indicates that Update Flags were cleared Value After Reset:0x0
9	RO	0x0	SCDC_UPD_FLAGS_CHG_IRQ Indicates that Update Flags have changed Value After Reset:0x0
8	RO	0x0	SCDC_UPD_FLAGS_RD_IRQ Indicates that Update Flags were read Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	RO	0x0	I2CM_NACK_RCVD_IRQ Indicates that I2C Master has received a NACK Value After Reset:0x0
1	RO	0x0	I2CM_READ_REQUEST_IRQ Indicates that I2C Master has received an SCDC Read Request Value After Reset:0x0
0	RO	0x0	I2CM_OP_DONE_IRQ Indicates that I2C Master operation has finished Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_MASK_N

Address: Operational Base + offset (0x3024)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes

Bit	Attr	Reset Value	Description
22	RW	0x0	FLT_EXIT_TO_LTSL_MASK_N Mask for flt_exit_to_ltsl_irq. Values: 0x0 (MASK): Write 0 to mask flt_exit_to_ltsl_irq. 0x1 (UNMASK): Write 1 to unmask flt_exit_to_ltsl_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
21	RW	0x0	FLT_EXIT_TO_LTS4_MASK_N Mask for flt_exit_to_lts4_irq. Values: 0x0 (MASK): Write 0 to mask flt_exit_to_lts4_irq. 0x1 (UNMASK): Write 1 to unmask flt_exit_to_lts4_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
20	RW	0x0	FLT_EXIT_TO_LTSP_MASK_N Mask for flt_exit_to_ltsp_irq. Values: 0x0 (MASK): Write 0 to mask flt_exit_to_ltsp_irq. 0x1 (UNMASK): Write 1 to unmask flt_exit_to_ltsp_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	RW	0x0	SCDC_NACK_RCVD_MASK_N Mask for scdc_nack_rcvd_irq. Values: 0x0 (MASK): Write 0 to mask scdc_nack_rcvd_irq. 0x1 (UNMASK): Write 1 to unmask scdc_nack_rcvd_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	SCDC_RR_REPLY_STOP_MASK_N Mask for scdc_rr_reply_stop_irq. Values: 0x0 (MASK): Write 0 to mask scdc_rr_reply_stop_irq. 0x1 (UNMASK): Write 1 to unmask scdc_rr_reply_stop_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	SCDC_UPD_FLAGS_CLR_MASK_N Mask for scdc_upd_flags_clr_irq. Values: 0x0 (MASK): Write 0 to mask scdc_upd_flags_clr_irq. 0x1 (UNMASK): Write 1 to unmask scdc_upd_flags_clr_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
9	RW	0x0	SCDC_UPD_FLAGS_CHG_MASK_N Mask for scdc_upd_flags_chg_irq. Values: 0x0 (MASK): Write 0 to mask scdc_upd_flags_chg_irq. 0x1 (UNMASK): Write 1 to unmask scdc_upd_flags_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	SCDC_UPD_FLAGS_RD_MASK_N Mask for scdc_upd_flags_rd_irq. Values: 0x0 (MASK): Write 0 to mask scdc_upd_flags_rd_irq. 0x1 (UNMASK): Write 1 to unmask scdc_upd_flags_rd_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	RW	0x0	I2CM_NACK_RCVD_MASK_N Mask for i2cm_nack_rcvd_irq. Values: 0x0 (MASK): Write 0 to mask i2cm_nack_rcvd_irq. 0x1 (UNMASK): Write 1 to unmask i2cm_nack_rcvd_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	I2CM_READ_REQUEST_MASK_N Mask for i2cm_read_request_irq. Values: 0x0 (MASK): Write 0 to mask i2cm_read_request_irq. 0x1 (UNMASK): Write 1 to unmask i2cm_read_request_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	I2CM_OP_DONE_MASK_N Mask for i2cm_op_done_irq. Values: 0x0 (MASK): Write 0 to mask i2cm_op_done_irq. 0x1 (UNMASK): Write 1 to unmask i2cm_op_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_CLEAR

Address: Operational Base + offset (0x3028)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes
22	WO	0x0	FLT_EXIT_TO_LTSL_CLEAR Clear for flt_exit_to_ltsl_irq Values: 0x1 (CLEAR): Write 1 to clear flt_exit_to_ltsl_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
21	WO	0x0	FLT_EXIT_TO_LTS4_CLEAR Clear for flt_exit_to_lts4_irq Values: 0x1 (CLEAR): Write 1 to clear flt_exit_to_lts4_irq Value After Reset:0x0
20	WO	0x0	FLT_EXIT_TO_LTSP_CLEAR Clear for flt_exit_to_ltsp_irq Values: 0x1 (CLEAR): Write 1 to clear flt_exit_to_ltsp_irq Value After Reset:0x0
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	WO	0x0	SCDC_NACK_RCVD_CLEAR Clear for scdc_nack_rcvd_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_nack_rcvd_irq Value After Reset:0x0
11	WO	0x0	SCDC_RR_REPLY_STOP_CLEAR Clear for scdc_rr_reply_stop_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_rr_reply_stop_irq Value After Reset:0x0
10	WO	0x0	SCDC_UPD_FLAGS_CLR_CLEAR Clear for scdc_upd_flags_clr_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_upd_flags_clr_irq Value After Reset:0x0
9	WO	0x0	SCDC_UPD_FLAGS_CHG_CLEAR Clear for scdc_upd_flags_chg_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_upd_flags_chg_irq Value After Reset:0x0
8	WO	0x0	SCDC_UPD_FLAGS_RD_CLEAR Clear for scdc_upd_flags_rd_irq Values: 0x1 (CLEAR): Write 1 to clear scdc_upd_flags_rd_irq Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	WO	0x0	I2CM_NACK_RCVD_CLEAR Clear for i2cm_nack_rcvd_irq Values: 0x1 (CLEAR): Write 1 to clear i2cm_nack_rcvd_irq Value After Reset:0x0
1	WO	0x0	I2CM_READ_REQUEST_CLEAR Clear for i2cm_read_request_irq Values: 0x1 (CLEAR): Write 1 to clear i2cm_read_request_irq Value After Reset:0x0
0	WO	0x0	I2CM_OP_DONE_CLEAR Clear for i2cm_op_done_irq Values: 0x1 (CLEAR): Write 1 to clear i2cm_op_done_irq Value After Reset:0x0

HDMI TX Controller_MAINUNIT_1_INT_FORCE

Address: Operational Base + offset (0x302C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Reserved2 Reserved Field:Yes
22	WO	0x0	FLT_EXIT_TO_LTSL_FORCE Force for flt_exit_to_ltsl_irq Values: 0x1 (FORCE): Write 1 to trigger flt_exit_to_ltsl_irq Value After Reset:0x0
21	WO	0x0	FLT_EXIT_TO_LTS4_FORCE Force for flt_exit_to_lts4_irq Values: 0x1 (FORCE): Write 1 to trigger flt_exit_to_lts4_irq Value After Reset:0x0
20	WO	0x0	FLT_EXIT_TO_LTSP_FORCE Force for flt_exit_to_ltsp_irq Values: 0x1 (FORCE): Write 1 to trigger flt_exit_to_ltsp_irq Value After Reset:0x0
19:13	RW	0x00	Reserved1 Reserved Field:Yes
12	WO	0x0	SCDC_NACK_RCVD_FORCE Force for scdc_nack_rcvd_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_nack_rcvd_irq Value After Reset:0x0
11	WO	0x0	SCDC_RR_REPLY_STOP_FORCE Force for scdc_rr_reply_stop_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_rr_reply_stop_irq Value After Reset:0x0
10	WO	0x0	SCDC_UPD_FLAGS_CLR_FORCE Force for scdc_upd_flags_clr_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_upd_flags_clr_irq Value After Reset:0x0
9	WO	0x0	SCDC_UPD_FLAGS_CHG_FORCE Force for scdc_upd_flags_chg_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_upd_flags_chg_irq Value After Reset:0x0
8	WO	0x0	SCDC_UPD_FLAGS_RD_FORCE Force for scdc_upd_flags_rd_irq Values: 0x1 (FORCE): Write 1 to trigger scdc_upd_flags_rd_irq Value After Reset:0x0
7:3	RW	0x00	Reserved0 Reserved Field:Yes
2	WO	0x0	I2CM_NACK_RCVD_FORCE Force for i2cm_nack_rcvd_irq Values: 0x1 (FORCE): Write 1 to trigger i2cm_nack_rcvd_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
1	WO	0x0	I2CM_READ_REQUEST_FORCE Force for i2cm_read_request_irq Values: 0x1 (FORCE): Write 1 to trigger i2cm_read_request_irq Value After Reset:0x0
0	WO	0x0	I2CM_OP_DONE_FORCE Force for i2cm_op_done_irq Values: 0x1 (FORCE): Write 1 to trigger i2cm_op_done_irq Value After Reset:0x0

HDMI TX Controller_AVP_INTVEC_INDEX
Address: Operational Base + offset (0x3800)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved0 Reserved Field:Yes
6	RO	0x0	AVP_6_INTVEC AVP 6 Interrupt Vector triggered Value After Reset:0x0
5	RO	0x0	AVP_5_INTVEC AVP 5 Interrupt Vector triggered Value After Reset:0x0
4	RO	0x0	AVP_4_INTVEC AVP 4 Interrupt Vector triggered Value After Reset:0x0
3	RO	0x0	AVP_3_INTVEC AVP 3 Interrupt Vector triggered Value After Reset:0x0
2	RO	0x0	AVP_2_INTVEC AVP 2 Interrupt Vector triggered Value After Reset:0x0
1	RO	0x0	AVP_1_INTVEC AVP 1 Interrupt Vector triggered Value After Reset:0x0
0	RO	0x0	AVP_0_INTVEC AVP 0 Interrupt Vector triggered Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_STATUS
Address: Operational Base + offset (0x3810)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	RO	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_IRQ Audio Packetizer Invalid Sample_Present bits configuration interrupt Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes
20	RO	0x0	PKTZ_FRLCHAR_FIFO_OVF_IRQ Packetizer FIFO Overflow interrupt. Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes

Bit	Attr	Reset Value	Description
16	RO	0x0	AUDFIFO_UDF_IRQ Audio Interface FIFO Underflow interrupt. Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	RO	0x0	TMDSFIFO_OVF_IRQ Detected TMDS FIFO Overflow interrupt. Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RO	0x0	EMP_TX_MTW_VIOLATION_IRQ Extended Metada Packets loaded by software were not all transmitted within a single MTW. If emp_tx_mtw_violation_en=1, the EMP Packet Scheduler continues to send the EMP packets until transmission is complete. Value After Reset:0x0
8	RO	0x0	EMP_TX_DONE_IRQ All Extended Metada Packets loaded by software were successfully transmitted. Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	RO	0x0	EMP_CVTEM_TX_DONE_IRQ CVTEM were successfully transmitted. Value After Reset:0x0
5	RO	0x0	EMP_VTEM_TX_DONE_IRQ VTEM were successfully transmitted. Value After Reset:0x0
4	RO	0x0	DEFAULT_PHASE_VIO_IRQ Default Phase rule violation Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RO	0x0	IPI_NOT_SUPPORTED_IRQ Detected IPI format and/or color depth not supported interrupt Note: Interrupt only active when ipi_override_map=0 Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_MASK_N

Address: Operational Base + offset (0x3814)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	RW	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_MASK_N Mask for audpkt_invalid_sample_present_irq. Values: 0x0 (MASK): Write 0 to mask audpkt_invalid_sample_present_irq. 0x1 (UNMASK): Write 1 to unmask audpkt_invalid_sample_present_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20	RW	0x0	PKTZ_FRLCHAR_FIFO_OVF_MASK_N Mask for pktz_frlchar_fifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask pktz_frlchar_fifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask pktz_frlchar_fifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes
16	RW	0x0	AUDFIFO_UDF_MASK_N Mask for audfifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask audfifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask audfifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	RW	0x0	TMDSFIFO_OVF_MASK_N Mask for tmdsfifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask tmdsfifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask tmdsfifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RW	0x0	EMP_TX_MTW_VIOLATION_MASK_N Mask for emp_tx_mtw_violation_irq. Values: 0x0 (MASK): Write 0 to mask emp_tx_mtw_violation_irq. 0x1 (UNMASK): Write 1 to unmask emp_tx_mtw_violation_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	EMP_TX_DONE_MASK_N Mask for emp_tx_done_irq. Values: 0x0 (MASK): Write 0 to mask emp_tx_done_irq. 0x1 (UNMASK): Write 1 to unmask emp_tx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	RW	0x0	EMP_CVTEM_TX_DONE_MASK_N Mask for emp_cvtem_tx_done_irq. Values: 0x0 (MASK): Write 0 to mask emp_cvtem_tx_done_irq. 0x1 (UNMASK): Write 1 to unmask emp_cvtem_tx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
5	RW	0x0	EMP_VTEM_TX_DONE_MASK_N Mask for emp_vtem_tx_done_irq. Values: 0x0 (MASK): Write 0 to mask emp_vtem_tx_done_irq. 0x1 (UNMASK): Write 1 to unmask emp_vtem_tx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	DEFAULT_PHASE_VIO_MASK_N Mask for default_phase_vio_irq. Values: 0x0 (MASK): Write 0 to mask default_phase_vio_irq. 0x1 (UNMASK): Write 1 to unmask default_phase_vio_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	IPI_NOT_SUPPORTED_MASK_N Mask for ipi_not_supported_irq. Values: 0x0 (MASK): Write 0 to mask ipi_not_supported_irq. 0x1 (UNMASK): Write 1 to unmask ipi_not_supported_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_CLEAR

Address: Operational Base + offset (0x3818)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	WO	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_CLEAR Clear for audpkt_invalid_sample_present_irq Values: 0x1 (CLEAR): Write 1 to clear audpkt_invalid_sample_present_irq Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes
20	WO	0x0	PKTZ_FRLCHAR_FIFO_OVF_CLEAR Clear for pktz_frlchar_fifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear pktz_frlchar_fifo_ovf_irq Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes
16	WO	0x0	AUDFIFO_UDF_CLEAR Clear for audfifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear audfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12	WO	0x0	TMDSFIFO_OVF_CLEAR Clear for tmdsfifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear tmdsfifo_ovf_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	WO	0x0	EMP_TX_MTW_VIOLATION_CLEAR Clear for emp_tx_mtw_violation_irq Values: 0x1 (CLEAR): Write 1 to clear emp_tx_mtw_violation_irq Value After Reset:0x0
8	WO	0x0	EMP_TX_DONE_CLEAR Clear for emp_tx_done_irq Values: 0x1 (CLEAR): Write 1 to clear emp_tx_done_irq Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	WO	0x0	EMP_CVTEM_TX_DONE_CLEAR Clear for emp_cvtem_tx_done_irq Values: 0x1 (CLEAR): Write 1 to clear emp_cvtem_tx_done_irq Value After Reset:0x0
5	WO	0x0	EMP_VTEM_TX_DONE_CLEAR Clear for emp_vtem_tx_done_irq Values: 0x1 (CLEAR): Write 1 to clear emp_vtem_tx_done_irq Value After Reset:0x0
4	WO	0x0	DEFAULT_PHASE_VIO_CLEAR Clear for default_phase_vio_irq Values: 0x1 (CLEAR): Write 1 to clear default_phase_vio_irq Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	WO	0x0	IPI_NOT_SUPPORTED_CLEAR Clear for ipi_not_supported_irq Values: 0x1 (CLEAR): Write 1 to clear ipi_not_supported_irq Value After Reset:0x0

HDMI TX Controller_AVP_0_INT_FORCE

Address: Operational Base + offset (0x381C)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved6 Reserved Field:Yes
24	WO	0x0	AUDPKT_INVALID_SAMPLE_PRESENT_FORCE Force for audpkt_invalid_sample_present_irq Values: 0x1 (FORCE): Write 1 to trigger audpkt_invalid_sample_present_irq Value After Reset:0x0
23:21	RW	0x0	Reserved5 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20	WO	0x0	PKTZ_FRLCHAR_FIFO_OVF_FORCE Force for pktz_frlchar_fifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger pktz_frlchar_fifo_ovf_irq Value After Reset:0x0
19:17	RW	0x0	Reserved4 Reserved Field:Yes
16	WO	0x0	AUDFIFO_UDF_FORCE Force for audfifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger audfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved3 Reserved Field:Yes
12	WO	0x0	TMDSFIFO_OVF_FORCE Force for tmdsfifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger tmdsfifo_ovf_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	WO	0x0	EMP_TX_MTW_VIOLATION_FORCE Force for emp_tx_mtw_violation_irq Values: 0x1 (FORCE): Write 1 to trigger emp_tx_mtw_violation_irq Value After Reset:0x0
8	WO	0x0	EMP_TX_DONE_FORCE Force for emp_tx_done_irq Values: 0x1 (FORCE): Write 1 to trigger emp_tx_done_irq Value After Reset:0x0
7	RW	0x0	Reserved1 Reserved Field:Yes
6	WO	0x0	EMP_CVTEM_TX_DONE_FORCE Force for emp_cvtem_tx_done_irq Values: 0x1 (FORCE): Write 1 to trigger emp_cvtem_tx_done_irq Value After Reset:0x0
5	WO	0x0	EMP_VTEM_TX_DONE_FORCE Force for emp_vtem_tx_done_irq Values: 0x1 (FORCE): Write 1 to trigger emp_vtem_tx_done_irq Value After Reset:0x0
4	WO	0x0	DEFAULT_PHASE_VIO_FORCE Force for default_phase_vio_irq Values: 0x1 (FORCE): Write 1 to trigger default_phase_vio_irq Value After Reset:0x0
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	WO	0x0	IPI_NOT_SUPPORTED_FORCE Force for ipi_not_supported_irq Values: 0x1 (FORCE): Write 1 to trigger ipi_not_supported_irq Value After Reset:0x0

HDMI TX Controller_AVP_1_INT_STATUS
Address: Operational Base + offset (0x3820)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes
20	RO	0x0	PKTZ_FRLCHAR_FIFO_UDF_IRQ Packetizer FIFO Underflow interrupt. Value After Reset:0x0
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	RO	0x0	TMDSFIFO_UDF_IRQ Detected TMDS FIFO Underflow interrupt. Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes
12	RO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_IRQ Indicates that the buffer on the FRL RSFEC Aligner has became full. For more information about the state of the buffer, refer to frl_rsfec_config0.frl_rsfec_align_buffer_full_st Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	RO	0x0	AUDPKT_ACR_CTS_CALC_IRQ Audio Clock Regeneration (ACR) CTS calculation done interrupt event Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	RO	0x0	HDCP14_AUTH_CHG_IRQ HDCP 1.4 Authenticated State Change. Check field hdcp14_auth_st for more information. Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	HDCP14_BKSV_REVOC_FAIL_IRQ HDCP 1.4 BKSV is in Revocation List Value After Reset:0x0
3	RO	0x0	HDCP14_I2C_NACK_RCV_IRQ HDCP 1.4 I2C NACK Received Value After Reset:0x0
2	RO	0x0	HDCP14_I2C_TIMEOUT_IRQ HDCP 1.4 I2C Operation Timeout Value After Reset:0x0
1	RO	0x0	HDCP14_KSV_LIST_DONE_IRQ HDCP 1.4 KSV List Write in Revocation Memory Done Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_1_INT_MASK_N
Address: Operational Base + offset (0x3824)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes

Bit	Attr	Reset Value	Description
20	RW	0x0	PKTZ_FRLCHAR_FIFO_UDF_MASK_N Mask for pktz_frlchar_fifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask pktz_frlchar_fifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask pktz_frlchar_fifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	RW	0x0	TMDSFIFO_UDF_MASK_N Mask for tmdsfifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask tmdsfifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask tmdsfifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes
12	RW	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_MASK_N Mask for frl_rsfec_align_buffer_full_irq. Values: 0x0 (MASK): Write 0 to mask frl_rsfec_align_buffer_full_irq. 0x1 (UNMASK): Write 1 to unmask frl_rsfec_align_buffer_full_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	RW	0x0	AUDPKT_ACR_CTS_CALC_MASK_N Mask for audpkt_acr_cts_calc_irq. Values: 0x0 (MASK): Write 0 to mask audpkt_acr_cts_calc_irq. 0x1 (UNMASK): Write 1 to unmask audpkt_acr_cts_calc_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	RW	0x0	HDCP14_AUTH_CHG_MASK_N Mask for hdcp14_auth_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_auth_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_auth_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
4	RW	0x0	HDCP14_BKSV_REVOC_FAIL_MASK_N Mask for hdcp14_bksv_revoc_fail_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_bksv_revoc_fail_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_bksv_revoc_fail_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	HDCP14_I2C_NACK_RCV_MASK_N Mask for hdcp14_i2c_nack_rcv_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_i2c_nack_rcv_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_i2c_nack_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	HDCP14_I2C_TIMEOUT_MASK_N Mask for hdcp14_i2c_timeout_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_i2c_timeout_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_i2c_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	HDCP14_KSV_LIST_DONE_MASK_N Mask for hdcp14_ksv_list_done_irq. Values: 0x0 (MASK): Write 0 to mask hdcp14_ksv_list_done_irq. 0x1 (UNMASK): Write 1 to unmask hdcp14_ksv_list_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_1_INT_CLEAR

Address: Operational Base + offset (0x3828)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes
20	WO	0x0	PKTZ_FRLCHAR_FIFO_UDF_CLEAR Clear for pktz_frlchar_fifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear pktz_frlchar_fifo_udf_irq Value After Reset:0x0
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	WO	0x0	TMDSFIFO_UDF_CLEAR Clear for tmdsfifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear tmdsfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12	WO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_CLEAR Clear for frl_rsfec_align_buffer_full_irq Values: 0x1 (CLEAR): Write 1 to clear frl_rsfec_align_buffer_full_irq Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	WO	0x0	AUDPKT_ACR_CTS_CALC_CLEAR Clear for audpkt_acr_cts_calc_irq Values: 0x1 (CLEAR): Write 1 to clear audpkt_acr_cts_calc_irq Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	WO	0x0	HDCP14_AUTH_CHG_CLEAR Clear for hdcp14_auth_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_auth_chg_irq Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes
4	WO	0x0	HDCP14_BKSV_REVOC_FAIL_CLEAR Clear for hdcp14_bksv_revoc_fail_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_bksv_revoc_fail_irq Value After Reset:0x0
3	WO	0x0	HDCP14_I2C_NACK_RCV_CLEAR Clear for hdcp14_i2c_nack_rcv_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_i2c_nack_rcv_irq Value After Reset:0x0
2	WO	0x0	HDCP14_I2C_TIMEOUT_CLEAR Clear for hdcp14_i2c_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_i2c_timeout_irq Value After Reset:0x0
1	WO	0x0	HDCP14_KSV_LIST_DONE_CLEAR Clear for hdcp14_ksv_list_done_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp14_ksv_list_done_irq Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_1_INT_FORCE

Address: Operational Base + offset (0x382C)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved6 Reserved Field:Yes
20	WO	0x0	PKTZ_FRLCHAR_FIFO_UDF_FORCE Force for pktz_frlchar_fifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger pktz_frlchar_fifo_udf_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
19:17	RW	0x0	Reserved5 Reserved Field:Yes
16	WO	0x0	TMDSFIFO_UDF_FORCE Force for tmdsfifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger tmdsfifo_udf_irq Value After Reset:0x0
15:13	RW	0x0	Reserved4 Reserved Field:Yes
12	WO	0x0	FRL_RSFEC_ALIGN_BUFFER_FULL_FORCE Force for frl_rsfec_align_buffer_full_irq Values: 0x1 (FORCE): Write 1 to trigger frl_rsfec_align_buffer_full_irq Value After Reset:0x0
11:9	RW	0x0	Reserved3 Reserved Field:Yes
8	WO	0x0	AUDPKT_ACR_CTS_CALC_FORCE Force for audpkt_acr_cts_calc_irq Values: 0x1 (FORCE): Write 1 to trigger audpkt_acr_cts_calc_irq Value After Reset:0x0
7	RW	0x0	Reserved2 Reserved Field:Yes
6	WO	0x0	HDCP14_AUTH_CHG_FORCE Force for hdcp14_auth_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_auth_chg_irq Value After Reset:0x0
5	RW	0x0	Reserved1 Reserved Field:Yes
4	WO	0x0	HDCP14_BKSV_REVOC_FAIL_FORCE Force for hdcp14_bksv_revoc_fail_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_bksv_revoc_fail_irq Value After Reset:0x0
3	WO	0x0	HDCP14_I2C_NACK_RCV_FORCE Force for hdcp14_i2c_nack_rcv_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_i2c_nack_rcv_irq Value After Reset:0x0
2	WO	0x0	HDCP14_I2C_TIMEOUT_FORCE Force for hdcp14_i2c_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_i2c_timeout_irq Value After Reset:0x0
1	WO	0x0	HDCP14_KSV_LIST_DONE_FORCE Force for hdcp14_ksv_list_done_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp14_ksv_list_done_irq Value After Reset:0x0
0	RW	0x0	Reserved0 Reserved Field:Yes

HDMI TX Controller_AVP_2_INT_STATUS
Address: Operational Base + offset (0x3830)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes
24	RO	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_IRQ GMD - Gamut Metadata - P0 profile packet was ready but was not sent within first VBLANK period in a frame Value After Reset:0x0
23	RO	0x0	PKTSCHED_GHDMI2_UNSENT_IRQ GHDMI2 - Generic HDMI 2 - Programmed number of packets per field/frame not fully sent Value After Reset:0x0
22	RO	0x0	PKTSCHED_GHDMI1_UNSENT_IRQ GHDMI1 - Generic HDMI 1 - Programmed number of packets per field/frame not fully sent Value After Reset:0x0
21	RO	0x0	PKTSCHED_ACR_TIMEOUT_IRQ ACR - Audio Clock Recovery - Packet not sent within a 128fs/N period Value After Reset:0x0
20	RO	0x0	PKTSCHED_ISRC_TIMEOUT_IRQ ISRC - International Standard Recording Code - Packet not sent within configured period Value After Reset:0x0
19	RO	0x0	PKTSCHED_SPDI_TIMEOUT_IRQ SPDI - Source Product Descriptor InfoFrame - Packet not sent within configured period Value After Reset:0x0
18	RO	0x0	PKTSCHED_ACP_TIMEOUT_IRQ ACP - Audio Content Protection - Packet not sent within configured period Value After Reset:0x0
17	RO	0x0	PKTSCHED_GHDMI2_SENT_IRQ GHDMI2 - Generic HDMI 2 - Packet has been sent Value After Reset:0x0
16	RO	0x0	PKTSCHED_GHDMI1_SENT_IRQ GHDMI1 - Generic HDMI 1 - Packet has been sent Value After Reset:0x0
15	RO	0x0	PKTSCHED_DRMI_SENT_IRQ DRMI - Dynamic Range and Mastering InfoFrame - Packet has been sent Value After Reset:0x0
14	RO	0x0	PKTSCHED_NVI_SENT_IRQ NVI - NTSC VBI InfoFrame - Packet has been sent Value After Reset:0x0
13	RO	0x0	PKTSCHED_AUDI_SENT_IRQ AUDI - Audio InfoFrame - Packet has been sent Value After Reset:0x0
12	RO	0x0	PKTSCHED_SPDI_SENT_IRQ SPDI - Source Product Descriptor InfoFrame - Packet has been sent Value After Reset:0x0
11	RO	0x0	PKTSCHED_AVI_SENT_IRQ AVI - Auxiliary Video InfoFrame - Packet has been sent Value After Reset:0x0

Bit	Attr	Reset Value	Description
10	RO	0x0	PKTSCHED_VSI_SENT_IRQ VSI - Vendor Specific InfoFrame - Packet has been sent Value After Reset:0x0
9	RO	0x0	PKTSCHED_EMP_SENT_IRQ EMP - Extended Metadata - Packet has been sent Value After Reset:0x0
8	RO	0x0	PKTSCHED_AMD_SENT_IRQ AMD - Audio Metadata - Packet has been sent Value After Reset:0x0
7	RO	0x0	PKTSCHED_GMD_SENT_IRQ GMD - Gamut Metadata - Packet has been sent Value After Reset:0x0
6	RO	0x0	PKTSCHED_ISRC2_SENT_IRQ ISRC2 - Intl Std Recording Code 2 - Packet has been sent Value After Reset:0x0
5	RO	0x0	PKTSCHED_ISRC1_SENT_IRQ ISRC1 - Intl Std Recording Code 1 - Packet has been sent Value After Reset:0x0
4	RO	0x0	PKTSCHED_ACP_SENT_IRQ ACP - Audio Content Protection - Packet has been sent Value After Reset:0x0
3	RO	0x0	PKTSCHED_GCP_SENT_IRQ GCP - General Control - Packet has been sent Value After Reset:0x0
2	RO	0x0	PKTSCHED_AUDS_SENT_IRQ AUDS - Audio Sample - Packet has been sent Value After Reset:0x0
1	RO	0x0	PKTSCHED_ACR_SENT_IRQ ACR - Audio Clock Recovery - Packet has been sent Value After Reset:0x0
0	RO	0x0	PKTSCHED_NULL_SENT_IRQ NULL - Null - Packet has been sent Value After Reset:0x0

HDMI TX Controller_AVP_2_INT_MASK_N

Address: Operational Base + offset (0x3834)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes
24	RW	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_MASK_N Mask for pktsched_gmd_p0pkt_unsent_vb_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_gmd_p0pkt_unsent_vb_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_gmd_p0pkt_unsent_vb_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
23	RW	0x0	PKTSCHED_GHDMI2_UNSENT_MASK_N Mask for pktsched_ghdmi2_unsent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi2_unsent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi2_unsent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
22	RW	0x0	PKTSCHED_GHDMI1_UNSENT_MASK_N Mask for pktsched_ghdmi1_unsent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi1_unsent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi1_unsent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
21	RW	0x0	PKTSCHED_ACR_TIMEOUT_MASK_N Mask for pktsched_acr_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acr_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acr_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
20	RW	0x0	PKTSCHED_ISRC_TIMEOUT_MASK_N Mask for pktsched_isrc_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_isrc_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_isrc_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19	RW	0x0	PKTSCHED_SPDI_TIMEOUT_MASK_N Mask for pktsched_spdi_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_spdi_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_spdi_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
18	RW	0x0	PKTSCHED_ACP_TIMEOUT_MASK_N Mask for pktsched_acp_timeout_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acp_timeout_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acp_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
17	RW	0x0	PKTSCHED_GHDMI2_SENT_MASK_N Mask for pktsched_ghdmi2_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi2_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi2_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
16	RW	0x0	PKTSCHED_GHDMI1_SENT_MASK_N Mask for pktsched_ghdmi1_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_ghdmi1_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_ghdmi1_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15	RW	0x0	PKTSCHED_DRMI_SENT_MASK_N Mask for pktsched_drmi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_drmi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_drmi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
14	RW	0x0	PKTSCHED_NVI_SENT_MASK_N Mask for pktsched_nvi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_nvi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_nvi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
13	RW	0x0	PKTSCHED_AUDI_SENT_MASK_N Mask for pktsched_audi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_audi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_audi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
12	RW	0x0	PKTSCHED_SPDI_SENT_MASK_N Mask for pktsched_spdi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_spdi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_spdi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	PKTSCHED_AVI_SENT_MASK_N Mask for pktsched_avi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_avi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_avi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	PKTSCHED_VSI_SENT_MASK_N Mask for pktsched_vsi_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_vsi_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_vsi_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
9	RW	0x0	PKTSCHED_EMP_SENT_MASK_N Mask for pktsched_emp_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_emp_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_emp_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	PKTSCHED_AMD_SENT_MASK_N Mask for pktsched_amd_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_amd_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_amd_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7	RW	0x0	PKTSCHED_GMD_SENT_MASK_N Mask for pktsched_gmd_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_gmd_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_gmd_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
6	RW	0x0	PKTSCHED_ISRC2_SENT_MASK_N Mask for pktsched_isrc2_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_isrc2_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_isrc2_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	PKTSCHED_ISRC1_SENT_MASK_N Mask for pktsched_isrc1_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_isrc1_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_isrc1_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	PKTSCHED_ACP_SENT_MASK_N Mask for pktsched_acp_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acp_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acp_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	PKTSCHED_GCP_SENT_MASK_N Mask for pktsched_gcp_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_gcp_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_gcp_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
2	RW	0x0	PKTSCHED_AUDS_SENT_MASK_N Mask for pktsched_auds_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_auds_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_auds_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	PKTSCHED_ACR_SENT_MASK_N Mask for pktsched_acr_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_acr_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_acr_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	PKTSCHED_NULL_SENT_MASK_N Mask for pktsched_null_sent_irq. Values: 0x0 (MASK): Write 0 to mask pktsched_null_sent_irq. 0x1 (UNMASK): Write 1 to unmask pktsched_null_sent_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_2_INT_CLEAR

Address: Operational Base + offset (0x3838)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes
24	WO	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_CLEAR Clear for pktsched_gmd_p0pkt_unsent_vb_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_gmd_p0pkt_unsent_vb_irq Value After Reset:0x0
23	WO	0x0	PKTSCHED_GHDMI2_UNSENT_CLEAR Clear for pktsched_ghdmi2_unsent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi2_unsent_irq Value After Reset:0x0
22	WO	0x0	PKTSCHED_GHDMI1_UNSENT_CLEAR Clear for pktsched_ghdmi1_unsent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi1_unsent_irq Value After Reset:0x0
21	WO	0x0	PKTSCHED_ACR_TIMEOUT_CLEAR Clear for pktsched_acr_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acr_timeout_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
20	WO	0x0	PKTSCHED_ISRC_TIMEOUT_CLEAR Clear for pktsched_isrc_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_isrc_timeout_irq Value After Reset:0x0
19	WO	0x0	PKTSCHED_SPDI_TIMEOUT_CLEAR Clear for pktsched_spdi_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_spdi_timeout_irq Value After Reset:0x0
18	WO	0x0	PKTSCHED_ACP_TIMEOUT_CLEAR Clear for pktsched_acp_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acp_timeout_irq Value After Reset:0x0
17	WO	0x0	PKTSCHED_GHDMI2_SENT_CLEAR Clear for pktsched_ghdmi2_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi2_sent_irq Value After Reset:0x0
16	WO	0x0	PKTSCHED_GHDMI1_SENT_CLEAR Clear for pktsched_ghdmi1_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_ghdmi1_sent_irq Value After Reset:0x0
15	WO	0x0	PKTSCHED_DRMI_SENT_CLEAR Clear for pktsched_drmi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_drmi_sent_irq Value After Reset:0x0
14	WO	0x0	PKTSCHED_NVI_SENT_CLEAR Clear for pktsched_nvi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_nvi_sent_irq Value After Reset:0x0
13	WO	0x0	PKTSCHED_AUDI_SENT_CLEAR Clear for pktsched_audi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_audi_sent_irq Value After Reset:0x0
12	WO	0x0	PKTSCHED_SPDI_SENT_CLEAR Clear for pktsched_spdi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_spdi_sent_irq Value After Reset:0x0
11	WO	0x0	PKTSCHED_AVI_SENT_CLEAR Clear for pktsched_avi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_avi_sent_irq Value After Reset:0x0
10	WO	0x0	PKTSCHED_VSI_SENT_CLEAR Clear for pktsched_vsi_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_vsi_sent_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
9	WO	0x0	PKTSCHED_EMP_SENT_CLEAR Clear for pktsched_emp_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_emp_sent_irq Value After Reset:0x0
8	WO	0x0	PKTSCHED_AMD_SENT_CLEAR Clear for pktsched_amd_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_amd_sent_irq Value After Reset:0x0
7	WO	0x0	PKTSCHED_GMD_SENT_CLEAR Clear for pktsched_gmd_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_gmd_sent_irq Value After Reset:0x0
6	WO	0x0	PKTSCHED_ISRC2_SENT_CLEAR Clear for pktsched_isrc2_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_isrc2_sent_irq Value After Reset:0x0
5	WO	0x0	PKTSCHED_ISRC1_SENT_CLEAR Clear for pktsched_isrc1_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_isrc1_sent_irq Value After Reset:0x0
4	WO	0x0	PKTSCHED_ACP_SENT_CLEAR Clear for pktsched_acp_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acp_sent_irq Value After Reset:0x0
3	WO	0x0	PKTSCHED_GCP_SENT_CLEAR Clear for pktsched_gcp_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_gcp_sent_irq Value After Reset:0x0
2	WO	0x0	PKTSCHED_AUDS_SENT_CLEAR Clear for pktsched_auds_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_auds_sent_irq Value After Reset:0x0
1	WO	0x0	PKTSCHED_ACR_SENT_CLEAR Clear for pktsched_acr_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_acr_sent_irq Value After Reset:0x0
0	WO	0x0	PKTSCHED_NULL_SENT_CLEAR Clear for pktsched_null_sent_irq Values: 0x1 (CLEAR): Write 1 to clear pktsched_null_sent_irq Value After Reset:0x0

HDMI TX Controller_AVP_2_INT_FORCE
Address: Operational Base + offset (0x383C)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved0 Reserved Field:Yes
24	WO	0x0	PKTSCHED_GMD_P0PKT_UNSENT_VB_FORCE Force for pktsched_gmd_p0pkt_unsent_vb_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_gmd_p0pkt_unsent_vb_irq Value After Reset:0x0
23	WO	0x0	PKTSCHED_GHDMI2_UNSENT_FORCE Force for pktsched_ghdmi2_unsent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi2_unsent_irq Value After Reset:0x0
22	WO	0x0	PKTSCHED_GHDMI1_UNSENT_FORCE Force for pktsched_ghdmi1_unsent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi1_unsent_irq Value After Reset:0x0
21	WO	0x0	PKTSCHED_ACR_TIMEOUT_FORCE Force for pktsched_acr_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acr_timeout_irq Value After Reset:0x0
20	WO	0x0	PKTSCHED_ISRC_TIMEOUT_FORCE Force for pktsched_isrc_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_isrc_timeout_irq Value After Reset:0x0
19	WO	0x0	PKTSCHED_SPDI_TIMEOUT_FORCE Force for pktsched_spdi_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_spdi_timeout_irq Value After Reset:0x0
18	WO	0x0	PKTSCHED_ACP_TIMEOUT_FORCE Force for pktsched_acp_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acp_timeout_irq Value After Reset:0x0
17	WO	0x0	PKTSCHED_GHDMI2_SENT_FORCE Force for pktsched_ghdmi2_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi2_sent_irq Value After Reset:0x0
16	WO	0x0	PKTSCHED_GHDMI1_SENT_FORCE Force for pktsched_ghdmi1_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_ghdmi1_sent_irq Value After Reset:0x0
15	WO	0x0	PKTSCHED_DRMI_SENT_FORCE Force for pktsched_drmi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_drmi_sent_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
14	WO	0x0	PKTSCHED_NVI_SENT_FORCE Force for pktsched_nvi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_nvi_sent_irq Value After Reset:0x0
13	WO	0x0	PKTSCHED_AUDI_SENT_FORCE Force for pktsched_audi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_audi_sent_irq Value After Reset:0x0
12	WO	0x0	PKTSCHED_SPDI_SENT_FORCE Force for pktsched_spdi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_spdi_sent_irq Value After Reset:0x0
11	WO	0x0	PKTSCHED_AVI_SENT_FORCE Force for pktsched_avi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_avi_sent_irq Value After Reset:0x0
10	WO	0x0	PKTSCHED_VSI_SENT_FORCE Force for pktsched_vsi_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_vsi_sent_irq Value After Reset:0x0
9	WO	0x0	PKTSCHED_EMP_SENT_FORCE Force for pktsched_emp_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_emp_sent_irq Value After Reset:0x0
8	WO	0x0	PKTSCHED_AMD_SENT_FORCE Force for pktsched_amd_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_amd_sent_irq Value After Reset:0x0
7	WO	0x0	PKTSCHED_GMD_SENT_FORCE Force for pktsched_gmd_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_gmd_sent_irq Value After Reset:0x0
6	WO	0x0	PKTSCHED_ISRC2_SENT_FORCE Force for pktsched_isrc2_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_isrc2_sent_irq Value After Reset:0x0
5	WO	0x0	PKTSCHED_ISRC1_SENT_FORCE Force for pktsched_isrc1_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_isrc1_sent_irq Value After Reset:0x0
4	WO	0x0	PKTSCHED_ACP_SENT_FORCE Force for pktsched_acp_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acp_sent_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
3	WO	0x0	PKTSCHED_GCP_SENT_FORCE Force for pktsched_gcp_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_gcp_sent_irq Value After Reset:0x0
2	WO	0x0	PKTSCHED_AUDS_SENT_FORCE Force for pktsched_auds_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_auds_sent_irq Value After Reset:0x0
1	WO	0x0	PKTSCHED_ACR_SENT_FORCE Force for pktsched_acr_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_acr_sent_irq Value After Reset:0x0
0	WO	0x0	PKTSCHED_NULL_SENT_FORCE Force for pktsched_null_sent_irq Values: 0x1 (FORCE): Write 1 to trigger pktsched_null_sent_irq Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_STATUS

Address: Operational Base + offset (0x3840)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[0] from ESM Module Value After Reset:0x0
18	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[1] from ESM Module Value After Reset:0x0
17	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[2] from ESM Module Value After Reset:0x0
16	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[3] from ESM Module Value After Reset:0x0
15	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[4] from ESM Module Value After Reset:0x0
14	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[5] from ESM Module Value After Reset:0x0
13	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[6] from ESM Module Value After Reset:0x0

Bit	Attr	Reset Value	Description
12	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[7] from ESM Module Value After Reset:0x0
11	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[8] from ESM Module Value After Reset:0x0
10	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[9] from ESM Module Value After Reset:0x0
9	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[10] from ESM Module Value After Reset:0x0
8	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[11] from ESM Module Value After Reset:0x0
7	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[12] from ESM Module Value After Reset:0x0
6	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[13] from ESM Module Value After Reset:0x0
5	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[14] from ESM Module Value After Reset:0x0
4	RO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_IRQ HDCP 2 Logic Port 0 Change interrupt for bit hdcp2_esm_p0_gpio_out[15] from ESM Module Value After Reset:0x0
3	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[0] from ESM Module Value After Reset:0x0
2	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[1] from ESM Module Value After Reset:0x0
1	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[2] from ESM Module Value After Reset:0x0
0	RO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_IRQ HDCP 2 Logic Global Change interrupt for bit hdcp2_esm_global_gpio_out[3] from ESM Module Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_MASK_N
Address: Operational Base + offset (0x3844)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_0_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_0_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_0_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
18	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_1_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_1_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_1_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
17	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_2_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_2_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_2_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
16	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_3_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_3_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_3_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_4_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_4_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_4_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
14	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_5_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_5_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_5_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
13	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_6_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_6_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_6_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
12	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_7_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_7_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_7_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_8_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_8_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_8_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_9_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_9_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_9_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
9	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_10_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_10_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_10_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_11_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_11_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_11_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
7	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_12_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_12_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_12_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
6	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_13_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_13_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_13_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
5	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_14_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_14_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_14_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_MASK_N Mask for hdcp2_esm_p0_gpio_out_15_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_p0_gpio_out_15_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_p0_gpio_out_15_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_0_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_0_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_0_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_1_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_1_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_1_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
1	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_2_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_2_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_2_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_MASK_N Mask for hdcp2_esm_global_gpio_out_3_chg_irq. Values: 0x0 (MASK): Write 0 to mask hdcp2_esm_global_gpio_out_3_chg_irq. 0x1 (UNMASK): Write 1 to unmask hdcp2_esm_global_gpio_out_3_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_CLEAR

Address: Operational Base + offset (0x3848)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_0_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_0_chg_irq Value After Reset:0x0
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_1_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_1_chg_irq Value After Reset:0x0
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_2_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_2_chg_irq Value After Reset:0x0
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_3_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_3_chg_irq Value After Reset:0x0
15	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_4_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_4_chg_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
14	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_5_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_5_chg_irq Value After Reset:0x0
13	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_6_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_6_chg_irq Value After Reset:0x0
12	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_7_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_7_chg_irq Value After Reset:0x0
11	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_8_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_8_chg_irq Value After Reset:0x0
10	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_9_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_9_chg_irq Value After Reset:0x0
9	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_10_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_10_chg_irq Value After Reset:0x0
8	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_11_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_11_chg_irq Value After Reset:0x0
7	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_12_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_12_chg_irq Value After Reset:0x0
6	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_13_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_13_chg_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
5	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_14_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_14_chg_irq Value After Reset:0x0
4	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_CLEAR Clear for hdcp2_esm_p0_gpio_out_15_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_p0_gpio_out_15_chg_irq Value After Reset:0x0
3	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_0_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_0_chg_irq Value After Reset:0x0
2	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_1_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_1_chg_irq Value After Reset:0x0
1	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_2_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_2_chg_irq Value After Reset:0x0
0	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_CLEAR Clear for hdcp2_esm_global_gpio_out_3_chg_irq Values: 0x1 (CLEAR): Write 1 to clear hdcp2_esm_global_gpio_out_3_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_3_INT_FORCE

Address: Operational Base + offset (0x384C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved0 Reserved Field:Yes
19	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_0_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_0_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_0_chg_irq Value After Reset:0x0
18	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_1_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_1_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_1_chg_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
17	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_2_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_2_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_2_chg_irq Value After Reset:0x0
16	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_3_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_3_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_3_chg_irq Value After Reset:0x0
15	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_4_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_4_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_4_chg_irq Value After Reset:0x0
14	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_5_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_5_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_5_chg_irq Value After Reset:0x0
13	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_6_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_6_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_6_chg_irq Value After Reset:0x0
12	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_7_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_7_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_7_chg_irq Value After Reset:0x0
11	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_8_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_8_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_8_chg_irq Value After Reset:0x0
10	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_9_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_9_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_9_chg_irq Value After Reset:0x0
9	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_10_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_10_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_10_chg_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
8	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_11_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_11_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_11_chg_irq Value After Reset:0x0
7	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_12_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_12_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_12_chg_irq Value After Reset:0x0
6	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_13_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_13_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_13_chg_irq Value After Reset:0x0
5	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_14_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_14_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_14_chg_irq Value After Reset:0x0
4	WO	0x0	HDCP2_ESM_P0_GPIO_OUT_15_CHG_FORCE Force for hdcp2_esm_p0_gpio_out_15_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_p0_gpio_out_15_chg_irq Value After Reset:0x0
3	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_0_CHG_FORCE Force for hdcp2_esm_global_gpio_out_0_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_0_chg_irq Value After Reset:0x0
2	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_1_CHG_FORCE Force for hdcp2_esm_global_gpio_out_1_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_1_chg_irq Value After Reset:0x0
1	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_2_CHG_FORCE Force for hdcp2_esm_global_gpio_out_2_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_2_chg_irq Value After Reset:0x0
0	WO	0x0	HDCP2_ESM_GLOBAL_GPIO_OUT_3_CHG_FORCE Force for hdcp2_esm_global_gpio_out_3_chg_irq Values: 0x1 (FORCE): Write 1 to trigger hdcp2_esm_global_gpio_out_3_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_STATUS
Address: Operational Base + offset (0x3850)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	RO	0x0	SPDIF_LINE3_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 3 interrupt Value After Reset:0x0
18	RO	0x0	SPDIF_LINE2_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 2 interrupt Value After Reset:0x0
17	RO	0x0	SPDIF_LINE1_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 1 interrupt Value After Reset:0x0
16	RO	0x0	SPDIF_LINE0_PROTOCOL_ERR_IRQ Audio SPDIF Protocol error in Lane 0 interrupt Value After Reset:0x0
15	RO	0x0	SPDIF_LINE3_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 3 interrupt Value After Reset:0x0
14	RO	0x0	SPDIF_LINE2_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 2 nterrupt Value After Reset:0x0
13	RO	0x0	SPDIF_LINE1_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 1 interrupt Value After Reset:0x0
12	RO	0x0	SPDIF_LINE0_PARITY_ERR_IRQ Audio SPDIF parity bit received incorrectly in Lane 0 interrupt Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RO	0x0	I2S_BBIT_ERR_IRQ Audio I2S error: disparity on received B bits interrupt Value After Reset:0x0
8	RO	0x0	I2S_WS_ERR_IRQ Audio I2S protocol error interrupt Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RO	0x0	AUDFIFO_OVF_IRQ Audio interface FIFO Overflow interrupt Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RO	0x0	PAI_FORMAT_CHG_IRQ Audio PAI interface format change interrupt Value After Reset:0x0
0	RO	0x0	PAI_PAIR_LAYOUT_CHG_IRQ Audio PAI pair layout chage interrupt Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_MASK_N
Address: Operational Base + offset (0x3854)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes

Bit	Attr	Reset Value	Description
19	RW	0x0	SPDIF_LINE3_PROTOCOL_ERR_MASK_N Mask for spdif_line3_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line3_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line3_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
18	RW	0x0	SPDIF_LINE2_PROTOCOL_ERR_MASK_N Mask for spdif_line2_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line2_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line2_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
17	RW	0x0	SPDIF_LINE1_PROTOCOL_ERR_MASK_N Mask for spdif_line1_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line1_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line1_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
16	RW	0x0	SPDIF_LINE0_PROTOCOL_ERR_MASK_N Mask for spdif_line0_protocol_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line0_protocol_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line0_protocol_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15	RW	0x0	SPDIF_LINE3_PARITY_ERR_MASK_N Mask for spdif_line3_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line3_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line3_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
14	RW	0x0	SPDIF_LINE2_PARITY_ERR_MASK_N Mask for spdif_line2_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line2_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line2_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
13	RW	0x0	SPDIF_LINE1_PARITY_ERR_MASK_N Mask for spdif_line1_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line1_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line1_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
12	RW	0x0	SPDIF_LINE0_PARITY_ERR_MASK_N Mask for spdif_line0_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask spdif_line0_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask spdif_line0_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	RW	0x0	I2S_BBIT_ERR_MASK_N Mask for i2s_bbit_err_irq. Values: 0x0 (MASK): Write 0 to mask i2s_bbit_err_irq. 0x1 (UNMASK): Write 1 to unmask i2s_bbit_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	I2S_WS_ERR_MASK_N Mask for i2s_ws_err_irq. Values: 0x0 (MASK): Write 0 to mask i2s_ws_err_irq. 0x1 (UNMASK): Write 1 to unmask i2s_ws_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x0	AUDFIFO_OVF_MASK_N Mask for audfifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask audfifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask audfifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	PAI_FORMAT_CHG_MASK_N Mask for pai_format_chg_irq. Values: 0x0 (MASK): Write 0 to mask pai_format_chg_irq. 0x1 (UNMASK): Write 1 to unmask pai_format_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	PAI_PAIR_LAYOUT_CHG_MASK_N Mask for pai_pair_layout_chg_irq. Values: 0x0 (MASK): Write 0 to mask pai_pair_layout_chg_irq. 0x1 (UNMASK): Write 1 to unmask pai_pair_layout_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_CLEAR

Address: Operational Base + offset (0x3858)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	WO	0x0	SPDIF_LINE3_PROTOCOL_ERR_CLEAR Clear for spdif_line3_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line3_protocol_err_irq Value After Reset:0x0
18	WO	0x0	SPDIF_LINE2_PROTOCOL_ERR_CLEAR Clear for spdif_line2_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line2_protocol_err_irq Value After Reset:0x0
17	WO	0x0	SPDIF_LINE1_PROTOCOL_ERR_CLEAR Clear for spdif_line1_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line1_protocol_err_irq Value After Reset:0x0
16	WO	0x0	SPDIF_LINE0_PROTOCOL_ERR_CLEAR Clear for spdif_line0_protocol_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line0_protocol_err_irq Value After Reset:0x0
15	WO	0x0	SPDIF_LINE3_PARITY_ERR_CLEAR Clear for spdif_line3_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line3_parity_err_irq Value After Reset:0x0
14	WO	0x0	SPDIF_LINE2_PARITY_ERR_CLEAR Clear for spdif_line2_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line2_parity_err_irq Value After Reset:0x0
13	WO	0x0	SPDIF_LINE1_PARITY_ERR_CLEAR Clear for spdif_line1_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line1_parity_err_irq Value After Reset:0x0
12	WO	0x0	SPDIF_LINE0_PARITY_ERR_CLEAR Clear for spdif_line0_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear spdif_line0_parity_err_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	WO	0x0	I2S_BBIT_ERR_CLEAR Clear for i2s_bbit_err_irq Values: 0x1 (CLEAR): Write 1 to clear i2s_bbit_err_irq Value After Reset:0x0
8	WO	0x0	I2S_WS_ERR_CLEAR Clear for i2s_ws_err_irq Values: 0x1 (CLEAR): Write 1 to clear i2s_ws_err_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	WO	0x0	AUDFIFO_OVF_CLEAR Clear for audfifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear audfifo_ovf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	PAI_FORMAT_CHG_CLEAR Clear for pai_format_chg_irq Values: 0x1 (CLEAR): Write 1 to clear pai_format_chg_irq Value After Reset:0x0
0	WO	0x0	PAI_PAIR_LAYOUT_CHG_CLEAR Clear for pai_pair_layout_chg_irq Values: 0x1 (CLEAR): Write 1 to clear pai_pair_layout_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_4_INT_FORCE

Address: Operational Base + offset (0x385C)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	Reserved3 Reserved Field:Yes
19	WO	0x0	SPDIF_LINE3_PROTOCOL_ERR_FORCE Force for spdif_line3_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line3_protocol_err_irq Value After Reset:0x0
18	WO	0x0	SPDIF_LINE2_PROTOCOL_ERR_FORCE Force for spdif_line2_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line2_protocol_err_irq Value After Reset:0x0
17	WO	0x0	SPDIF_LINE1_PROTOCOL_ERR_FORCE Force for spdif_line1_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line1_protocol_err_irq Value After Reset:0x0
16	WO	0x0	SPDIF_LINE0_PROTOCOL_ERR_FORCE Force for spdif_line0_protocol_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line0_protocol_err_irq Value After Reset:0x0
15	WO	0x0	SPDIF_LINE3_PARITY_ERR_FORCE Force for spdif_line3_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line3_parity_err_irq Value After Reset:0x0
14	WO	0x0	SPDIF_LINE2_PARITY_ERR_FORCE Force for spdif_line2_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line2_parity_err_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
13	WO	0x0	SPDIF_LINE1_PARITY_ERR_FORCE Force for spdif_line1_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line1_parity_err_irq Value After Reset:0x0
12	WO	0x0	SPDIF_LINE0_PARITY_ERR_FORCE Force for spdif_line0_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger spdif_line0_parity_err_irq Value After Reset:0x0
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9	WO	0x0	I2S_BBIT_ERR_FORCE Force for i2s_bbit_err_irq Values: 0x1 (FORCE): Write 1 to trigger i2s_bbit_err_irq Value After Reset:0x0
8	WO	0x0	I2S_WS_ERR_FORCE Force for i2s_ws_err_irq Values: 0x1 (FORCE): Write 1 to trigger i2s_ws_err_irq Value After Reset:0x0
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	WO	0x0	AUDFIFO_OVF_FORCE Force for audfifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger audfifo_ovf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	PAI_FORMAT_CHG_FORCE Force for pai_format_chg_irq Values: 0x1 (FORCE): Write 1 to trigger pai_format_chg_irq Value After Reset:0x0
0	WO	0x0	PAI_PAIR_LAYOUT_CHG_FORCE Force for pai_pair_layout_chg_irq Values: 0x1 (FORCE): Write 1 to trigger pai_pair_layout_chg_irq Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_STATUS

Address: Operational Base + offset (0x3860)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	RO	0x0	VID_FIFO_UDF_IRQ Video Interface FIFO Underflow Interrupt Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RO	0x0	VIDIF_VMON_VMEAS_IRQ Video Monitor vertical measures update interrupt Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	RO	0x0	VIDIF_VMON_HMEAS_IRQ Video Monitor horizontal measures update interrupt Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_MASK_N
Address: Operational Base + offset (0x3864)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	RW	0x0	VID_FIFO_UDF_MASK_N Mask for vid_fifo_udf_irq. Values: 0x0 (MASK): Write 0 to mask vid_fifo_udf_irq. 0x1 (UNMASK): Write 1 to unmask vid_fifo_udf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	VIDIF_VMON_VMEAS_MASK_N Mask for vidif_vmon_vmeas_irq. Values: 0x0 (MASK): Write 0 to mask vidif_vmon_vmeas_irq. 0x1 (UNMASK): Write 1 to unmask vidif_vmon_vmeas_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	VIDIF_VMON_HMEAS_MASK_N Mask for vidif_vmon_hmeas_irq. Values: 0x0 (MASK): Write 0 to mask vidif_vmon_hmeas_irq. 0x1 (UNMASK): Write 1 to unmask vidif_vmon_hmeas_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_CLEAR
Address: Operational Base + offset (0x3868)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	WO	0x0	VID_FIFO_UDF_CLEAR Clear for vid_fifo_udf_irq Values: 0x1 (CLEAR): Write 1 to clear vid_fifo_udf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	VIDIF_VMON_VMEAS_CLEAR Clear for vidif_vmon_vmeas_irq Values: 0x1 (CLEAR): Write 1 to clear vidif_vmon_vmeas_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	WO	0x0	VIDIF_VMON_HMEAS_CLEAR Clear for vidif_vmon_hmeas_irq Values: 0x1 (CLEAR): Write 1 to clear vidif_vmon_hmeas_irq Value After Reset:0x0

HDMI TX Controller_AVP_5_INT_FORCE
Address: Operational Base + offset (0x386C)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved1 Reserved Field:Yes
4	WO	0x0	VID_FIFO_UDF_FORCE Force for vid_fifo_udf_irq Values: 0x1 (FORCE): Write 1 to trigger vid_fifo_udf_irq Value After Reset:0x0
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	WO	0x0	VIDIF_VMON_VMEAS_FORCE Force for vidif_vmon_vmeas_irq Values: 0x1 (FORCE): Write 1 to trigger vidif_vmon_vmeas_irq Value After Reset:0x0
0	WO	0x0	VIDIF_VMON_HMEAS_FORCE Force for vidif_vmon_hmeas_irq Values: 0x1 (FORCE): Write 1 to trigger vidif_vmon_hmeas_irq Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_STATUS
Address: Operational Base + offset (0x3870)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	VID_FIFO_OVF_IRQ Video Interface FIFO Overflow Interrupt Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_MASK_N
Address: Operational Base + offset (0x3874)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	VID_FIFO_OVF_MASK_N Mask for vid_fifo_ovf_irq. Values: 0x0 (MASK): Write 0 to mask vid_fifo_ovf_irq. 0x1 (UNMASK): Write 1 to unmask vid_fifo_ovf_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_CLEAR
Address: Operational Base + offset (0x3878)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	VID_FIFO_OVF_CLEAR Clear for vid_fifo_ovf_irq Values: 0x1 (CLEAR): Write 1 to clear vid_fifo_ovf_irq Value After Reset:0x0

HDMI TX Controller_AVP_6_INT_FORCE
Address: Operational Base + offset (0x387C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	WO	0x0	VID_FIFO_OVF_FORCE Force for vid_fifo_ovf_irq Values: 0x1 (FORCE): Write 1 to trigger vid_fifo_ovf_irq Value After Reset:0x0

HDMI TX Controller_CEC_INT_STATUS
Address: Operational Base + offset (0x4000)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	RO	0x0	CECRX_NOTIFY_ERR_IRQ Follower - Bit timing error detected, Error Notification is being sent to Initiator, while rxbusy is set (for follower). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
11	RO	0x0	CECRX_EOM_IRQ Follower - Frame fully received after last data block with EOM=1 (for follower only). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
10	RO	0x0	CECTX_DRIVE_ERR_IRQ Drive 0 in the CEC output has not been seen in the CEC input interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
9	RO	0x0	CECRX_BUSY_IRQ Status bit cecrx_busy_st has changed value. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0

Bit	Attr	Reset Value	Description
8	RO	0x0	CECTX_BUSY_IRQ Status bit cectx_busy_st has changed value. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	RO	0x0	CECTX_FRAME_DISCARDED_IRQ Message to be sent has been discarded, since a new message has been received before the message is sent. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
4	RO	0x0	CECTX_NRETRANSMIT_FAIL_IRQ Last re- transmission fail. Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
3	RO	0x0	CECTX_LINE_ERR_IRQ Initiator - Line Error detected while transmitting a Frame (for initiator only). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
2	RO	0x0	CECTX_ARBLOST_IRQ Initiator - CEC line arbitration lost to a different Initiator when starting to transmit a Frame. (specification CEC 9). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
1	RO	0x0	CECTX_NACK_IRQ Initiator - Frame transmission stopped due to received NACK (direct address) or Negative ACK (broadcast) (for initiator only). Interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0
0	RO	0x0	CECTX_DONE_IRQ Initiator - Frame transmission is done successfully. (initiator only). interrupt flag status: Values: 0x0 (INACTIVE): inactive 0x1 (ACTIVE): active Value After Reset:0x0

HDMI TX Controller_CEC_INT_MASK_N
Address: Operational Base + offset (0x4004)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	RW	0x0	CECRX_NOTIFY_ERR_MASK_N Mask for cecrx_notify_err_irq. Values: 0x0 (MASK): Write 0 to mask cecrx_notify_err_irq. 0x1 (UNMASK): Write 1 to unmask cecrx_notify_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	CECRX_EOM_MASK_N Mask for cecrx_eom_irq. Values: 0x0 (MASK): Write 0 to mask cecrx_eom_irq. 0x1 (UNMASK): Write 1 to unmask cecrx_eom_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
10	RW	0x0	CECTX_DRIVE_ERR_MASK_N Mask for cectx_drive_err_irq. Values: 0x0 (MASK): Write 0 to mask cectx_drive_err_irq. 0x1 (UNMASK): Write 1 to unmask cectx_drive_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
9	RW	0x0	CECRX_BUSY_MASK_N Mask for cecrx_busy_irq. Values: 0x0 (MASK): Write 0 to mask cecrx_busy_irq. 0x1 (UNMASK): Write 1 to unmask cecrx_busy_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	CECTX_BUSY_MASK_N Mask for cectx_busy_irq. Values: 0x0 (MASK): Write 0 to mask cectx_busy_irq. 0x1 (UNMASK): Write 1 to unmask cectx_busy_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	RW	0x0	CECTX_FRAME_DISCARDED_MASK_N Mask for cectx_frame_discarded_irq. Values: 0x0 (MASK): Write 0 to mask cectx_frame_discarded_irq. 0x1 (UNMASK): Write 1 to unmask cectx_frame_discarded_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
4	RW	0x0	CECTX_NRETRANSMIT_FAIL_MASK_N Mask for cectx_nretransmit_fail_irq. Values: 0x0 (MASK): Write 0 to mask cectx_nretransmit_fail_irq. 0x1 (UNMASK): Write 1 to unmask cectx_nretransmit_fail_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	CECTX_LINE_ERR_MASK_N Mask for cectx_line_err_irq. Values: 0x0 (MASK): Write 0 to mask cectx_line_err_irq. 0x1 (UNMASK): Write 1 to unmask cectx_line_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	CECTX_ARBLOST_MASK_N Mask for cectx_arblost_irq. Values: 0x0 (MASK): Write 0 to mask cectx_arblost_irq. 0x1 (UNMASK): Write 1 to unmask cectx_arblost_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	CECTX_NACK_MASK_N Mask for cectx_nack_irq. Values: 0x0 (MASK): Write 0 to mask cectx_nack_irq. 0x1 (UNMASK): Write 1 to unmask cectx_nack_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	CECTX_DONE_MASK_N Mask for cectx_done_irq. Values: 0x0 (MASK): Write 0 to mask cectx_done_irq. 0x1 (UNMASK): Write 1 to unmask cectx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_CEC_INT_CLEAR

Address: Operational Base + offset (0x4008)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes
12	WO	0x0	CECRX_NOTIFY_ERR_CLEAR Clear for cecrx_notify_err_irq Values: 0x1 (CLEAR): Write 1 to clear cecrx_notify_err_irq Value After Reset:0x0
11	WO	0x0	CECRX_EOM_CLEAR Clear for cecrx_eom_irq Values: 0x1 (CLEAR): Write 1 to clear cecrx_eom_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
10	WO	0x0	CECTX_DRIVE_ERR_CLEAR Clear for cectx_drive_err_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_drive_err_irq Value After Reset:0x0
9	WO	0x0	CECRX_BUSY_CLEAR Clear for cecrx_busy_irq Values: 0x1 (CLEAR): Write 1 to clear cecrx_busy_irq Value After Reset:0x0
8	WO	0x0	CECTX_BUSY_CLEAR Clear for cectx_busy_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_busy_irq Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	WO	0x0	CECTX_FRAME_DISCARDED_CLEAR Clear for cectx_frame_discarded_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_frame_discarded_irq Value After Reset:0x0
4	WO	0x0	CECTX_NRETRANSMIT_FAIL_CLEAR Clear for cectx_nretransmit_fail_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_nretransmit_fail_irq Value After Reset:0x0
3	WO	0x0	CECTX_LINE_ERR_CLEAR Clear for cectx_line_err_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_line_err_irq Value After Reset:0x0
2	WO	0x0	CECTX_ARBLOST_CLEAR Clear for cectx_arblost_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_arblost_irq Value After Reset:0x0
1	WO	0x0	CECTX_NACK_CLEAR Clear for cectx_nack_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_nack_irq Value After Reset:0x0
0	WO	0x0	CECTX_DONE_CLEAR Clear for cectx_done_irq Values: 0x1 (CLEAR): Write 1 to clear cectx_done_irq Value After Reset:0x0

HDMI TX Controller_CEC_INT_FORCE

Address: Operational Base + offset (0x400C)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes

Bit	Attr	Reset Value	Description
12	WO	0x0	CECRX_NOTIFY_ERR_FORCE Force for cecrx_notify_err_irq Values: 0x1 (FORCE): Write 1 to trigger cecrx_notify_err_irq Value After Reset:0x0
11	WO	0x0	CECRX_EOM_FORCE Force for cecrx_eom_irq Values: 0x1 (FORCE): Write 1 to trigger cecrx_eom_irq Value After Reset:0x0
10	WO	0x0	CECTX_DRIVE_ERR_FORCE Force for cectx_drive_err_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_drive_err_irq Value After Reset:0x0
9	WO	0x0	CECRX_BUSY_FORCE Force for cecrx_busy_irq Values: 0x1 (FORCE): Write 1 to trigger cecrx_busy_irq Value After Reset:0x0
8	WO	0x0	CECTX_BUSY_FORCE Force for cectx_busy_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_busy_irq Value After Reset:0x0
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5	WO	0x0	CECTX_FRAME_DISCARDED_FORCE Force for cectx_frame_discarded_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_frame_discarded_irq Value After Reset:0x0
4	WO	0x0	CECTX_NRETRANSMIT_FAIL_FORCE Force for cectx_nretransmit_fail_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_nretransmit_fail_irq Value After Reset:0x0
3	WO	0x0	CECTX_LINE_ERR_FORCE Force for cectx_line_err_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_line_err_irq Value After Reset:0x0
2	WO	0x0	CECTX_ARBLOST_FORCE Force for cectx_arblost_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_arblost_irq Value After Reset:0x0
1	WO	0x0	CECTX_NACK_FORCE Force for cectx_nack_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_nack_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	WO	0x0	CECTX_DONE_FORCE Force for cectx_done_irq Values: 0x1 (FORCE): Write 1 to trigger cectx_done_irq Value After Reset:0x0

HDMI TX Controller_EARCRX_INTVEC_INDEX
Address: Operational Base + offset (0x4800)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RO	0x0	EARCRX_1_INTVEC eARC RX 1 Interrupt Vector triggered Value After Reset:0x0
0	RO	0x0	EARCRX_0_INTVEC eARC RX 0 Interrupt Vector triggered Value After Reset:0x0

HDMI TX Controller_EARCRX_0_INT_STATUS
Address: Operational Base + offset (0x4810)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved1 Reserved Field:Yes
21	RO	0x0	EARCRX_CMDC_HEARTBEAT_EARCVALID0_IRQ eARC RX CMDC - Bit EARC_TX_STAT.EARC_VALID=0 has been received while in Discovery state [RX eARC] (active eARC operation), causing the Discovery FSM to jump to state [RX DISC1]. Note: This interrupt is only triggered if configuration field earcrx_cmdc_dscvr_earcvalid0_to_disc1 is 1. Value After Reset:0x0
20	RO	0x0	EARCRX_CMDC_HEARTBEAT_EARCTXSTAT_UPD_IRQ eARC RX CMDC - The contents of EARC_TX_STAT register has been updated by the eARC TX device after a successful Heartbeat Transaction while in Discovery state [eARC RX]. Value After Reset:0x0
19	RO	0x0	EARCRX_CMDC_XACT_READ_DATA_IRQ eARC RX CMDC - A Read Transaction is ongoing, and the received Device ID and Offset are valid; SW shall now write the requested size and data into the respective earcrx_cmdc_xact_rd[X] registers Value After Reset:0x0
18	RO	0x0	EARCRX_CMDC_XACT_DONE_IRQ eARC RX CMDC - A transaction has finished, SW must check the result in register earcrx_cmdc_info and earcrx_cmdc_status. Value After Reset:0x0
17	RO	0x0	EARCRX_CMDC_RXPKT_BADPAR_IRQ eARC RX CMDC - A packet has been received with the wrong parity bit value. Information interrupt, no SW action needed. Note: If bit earcrx_cmdc_config: earcrx_cmdc_rxpkt_badpar_tolerant is set, the packet is received and the data used within the transaction. Value After Reset:0x0

Bit	Attr	Reset Value	Description
16	RO	0x0	EARCRX_CMDC_RXPKT_BADECC_IRQ eARC RX CMDC - A packet has been received with bit errors, and the ECC syndrome could not be used to correct the errors. Information interrupt, no SW action needed. Note: If bit earcrx_cmdc_config:earcrx_cmdc_rxpkt_badecc_tolerant is set, the packet is received and the data used within the transaction. Value After Reset:0x0
15	RO	0x0	EARCRX_CMDC_RXPKT_INCOMPLETE_IRQ eARC RX CMDC - A packet has been received with too few bits, packet was not received correctly. Value After Reset:0x0
14	RO	0x0	EARCRX_CMDC_RXPKT_BADSYNC_IRQ eARC RX CMDC - A packet has been received with a bad SYNC bit sequence, packet was not received correctly. Value After Reset:0x0
13	RO	0x0	EARCRX_CMDC_RXPKT_BADPREAMBLE_IRQ eARC RX CMDC - A packet has been received with a bad PREAMBLE bit sequence, packet was not received correctly. Value After Reset:0x0
12	RO	0x0	EARCRX_CMDC_HEARTBEAT_CAP_CHNG_IRQ eARC RX CMDC - The CAP_CHNG/CAP_CHNG_CONF handshake in Heartbeat transactions has finished successfully, after a SW request for a Capabilities Data Structure information change notification (earcrx_cmdc_heartbeat_rxstat_set:earcrx_cmdc_heartbeat_rxstat_cap_chng_set=1). Value After Reset:0x0
11	RO	0x0	EARCRX_CMDC_HEARTBEAT_STAT_CHNG_IRQ eARC RX CMDC - The STAT_CHNG/STAT_CHNG_CONF handshake in Heartbeat transactions has finished successfully, after a SW request for a audio latency information change notification (earcrx_cmdc_heartbeat_rxstat_set:earcrx_cmdc_heartbeat_rxstat_stat_chng_set=1). Value After Reset:0x0
10	RO	0x0	EARCRX_CMDC_HEARTBEAT_LOST_IRQ eARC RX CMDC - Heartbeat Lost while in [RX eARC] Discovery state (active eARC operation). This interrupt is triggered if a TeARC_LOST_HEARTBEAT timeout elapses while waiting for a successful Heartbeat transaction. Note: This interrupt is only triggered if configuration field earcrx_cmdc_heartbeat_loss_en is 1. Value After Reset:0x0
9	RO	0x0	EARCRX_CMDC_DISCOVERY_TIMEOUT_IRQ eARC RX CMDC - A TeARC_RX_TIMEOUT timeout has occurred waiting a Heartbeat sequence with EARC_TX_STAT.EARC_VALID=1 from eARC TX, during Discovery. The eARC Discovery is not attempted anymore, and the SW may now request an H14b ARC connection if needed. If H14b ARC mode is activated, bit earcrx_cmdc_control:earcrx_h14barc_active =1 shall be set. Value After Reset:0x0

Bit	Attr	Reset Value	Description
8	RO	0x0	EARCRX_CMDC_DISCOVERY_DONE_IRQ eARC RX CMDC - Discovery is completed successfully, reaching state [RX eARC]; Transactions can now be performed. Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_EARCRX_0_INT_MASK_N

Address: Operational Base + offset (0x4814)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved1 Reserved Field:Yes
21	RW	0x0	EARCRX_CMDC_HEARTBEAT_EARCVALID0_MASK_N Mask for earcrx_cmdc_heartbeat_earcvalid0_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_heartbeat_earcvalid0_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_heartbeat_earcvalid0_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
20	RW	0x0	EARCRX_CMDC_HEARTBEAT_EARCTXSTAT_UPD_MASK_N Mask for earcrx_cmdc_heartbeat_earctxstat_upd_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_heartbeat_earctxstat_upd_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_heartbeat_earctxstat_upd_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
19	RW	0x0	EARCRX_CMDC_XACT_READ_DATA_MASK_N Mask for earcrx_cmdc_xact_read_data_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_xact_read_data_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_xact_read_data_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
18	RW	0x0	EARCRX_CMDC_XACT_DONE_MASK_N Mask for earcrx_cmdc_xact_done_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_xact_done_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_xact_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
17	RW	0x0	EARCRX_CMDC_RXPKT_BADPAR_MASK_N Mask for earcrx_cmdc_rxpkt_badpar_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_rxpkt_badpar_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_rxpkt_badpar_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
16	RW	0x0	EARCRX_CMDC_RXPKT_BADECC_MASK_N Mask for earcrx_cmdc_rxpkt_badecc_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_rxpkt_badecc_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_rxpkt_badecc_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
15	RW	0x0	EARCRX_CMDC_RXPKT_INCOMPLETE_MASK_N Mask for earcrx_cmdc_rxpkt_incomplete_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_rxpkt_incomplete_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_rxpkt_incomplete_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
14	RW	0x0	EARCRX_CMDC_RXPKT_BADSYNC_MASK_N Mask for earcrx_cmdc_rxpkt_badsync_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_rxpkt_badsync_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_rxpkt_badsync_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
13	RW	0x0	EARCRX_CMDC_RXPKT_BADPREAMBLE_MASK_N Mask for earcrx_cmdc_rxpkt_badpreamble_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_rxpkt_badpreamble_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_rxpkt_badpreamble_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
12	RW	0x0	EARCRX_CMDC_HEARTBEAT_CAP_CHNG_MASK_N Mask for earcrx_cmdc_heartbeat_cap_chng_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_heartbeat_cap_chng_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_heartbeat_cap_chng_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
11	RW	0x0	EARCRX_CMDC_HEARTBEAT_STAT_CHNG_MASK_N Mask for earcrx_cmdc_heartbeat_stat_chng_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_heartbeat_stat_chng_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_heartbeat_stat_chng_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
10	RW	0x0	EARCRX_CMDC_HEARTBEAT_LOST_MASK_N Mask for earcrx_cmdc_heartbeat_lost_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_heartbeat_lost_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_heartbeat_lost_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
9	RW	0x0	EARCRX_CMDC_DISCOVERY_TIMEOUT_MASK_N Mask for earcrx_cmdc_discovery_timeout_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_discovery_timeout_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_discovery_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
8	RW	0x0	EARCRX_CMDC_DISCOVERY_DONE_MASK_N Mask for earcrx_cmdc_discovery_done_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_cmdc_discovery_done_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_cmdc_discovery_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_EARCRX_0_INT_CLEAR

Address: Operational Base + offset (0x4818)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved1 Reserved Field:Yes
21	WO	0x0	EARCRX_CMDC_HEARTBEAT_EARCVALID0_CLEAR Clear for earcrx_cmdc_heartbeat_earcvalid0_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_heartbeat_earcvalid0_irq Value After Reset:0x0
20	WO	0x0	EARCRX_CMDC_HEARTBEAT_EARCTXSTAT_UPD_CLEAR Clear for earcrx_cmdc_heartbeat_earctxstat_upd_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_heartbeat_earctxstat_upd_irq Value After Reset:0x0
19	WO	0x0	EARCRX_CMDC_XACT_READ_DATA_CLEAR Clear for earcrx_cmdc_xact_read_data_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_xact_read_data_irq Value After Reset:0x0
18	WO	0x0	EARCRX_CMDC_XACT_DONE_CLEAR Clear for earcrx_cmdc_xact_done_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_xact_done_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
17	WO	0x0	EARCRX_CMDC_RXPKT_BADPAR_CLEAR Clear for earcrx_cmdc_rxpkt_badpar_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_rxpkt_badpar_irq Value After Reset:0x0
16	WO	0x0	EARCRX_CMDC_RXPKT_BADECC_CLEAR Clear for earcrx_cmdc_rxpkt_badecc_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_rxpkt_badecc_irq Value After Reset:0x0
15	WO	0x0	EARCRX_CMDC_RXPKT_INCOMPLETE_CLEAR Clear for earcrx_cmdc_rxpkt_incomplete_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_rxpkt_incomplete_irq Value After Reset:0x0
14	WO	0x0	EARCRX_CMDC_RXPKT_BADSYNC_CLEAR Clear for earcrx_cmdc_rxpkt_badsync_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_rxpkt_badsync_irq Value After Reset:0x0
13	WO	0x0	EARCRX_CMDC_RXPKT_BADPREAMBLE_CLEAR Clear for earcrx_cmdc_rxpkt_badpreamble_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_rxpkt_badpreamble_irq Value After Reset:0x0
12	WO	0x0	EARCRX_CMDC_HEARTBEAT_CAP_CHNG_CLEAR Clear for earcrx_cmdc_heartbeat_cap_chng_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_heartbeat_cap_chng_irq Value After Reset:0x0
11	WO	0x0	EARCRX_CMDC_HEARTBEAT_STAT_CHNG_CLEAR Clear for earcrx_cmdc_heartbeat_stat_chng_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_heartbeat_stat_chng_irq Value After Reset:0x0
10	WO	0x0	EARCRX_CMDC_HEARTBEAT_LOST_CLEAR Clear for earcrx_cmdc_heartbeat_lost_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_heartbeat_lost_irq Value After Reset:0x0
9	WO	0x0	EARCRX_CMDC_DISCOVERY_TIMEOUT_CLEAR Clear for earcrx_cmdc_discovery_timeout_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_discovery_timeout_irq Value After Reset:0x0
8	WO	0x0	EARCRX_CMDC_DISCOVERY_DONE_CLEAR Clear for earcrx_cmdc_discovery_done_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_cmdc_discovery_done_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_EARCRX_0_INT_FORCE

Address: Operational Base + offset (0x481C)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved1 Reserved Field:Yes
21	WO	0x0	EARCRX_CMDC_HEARTBEAT_EARCVALID0_FORCE Force for earcrx_cmdc_heartbeat_earcvalid0_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_heartbeat_earcvalid0_irq Value After Reset:0x0
20	WO	0x0	EARCRX_CMDC_HEARTBEAT_EARCTXSTAT_UPD_FORCE Force for earcrx_cmdc_heartbeat_earctxstat_upd_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_heartbeat_earctxstat_upd_irq Value After Reset:0x0
19	WO	0x0	EARCRX_CMDC_XACT_READ_DATA_FORCE Force for earcrx_cmdc_xact_read_data_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_xact_read_data_irq Value After Reset:0x0
18	WO	0x0	EARCRX_CMDC_XACT_DONE_FORCE Force for earcrx_cmdc_xact_done_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_xact_done_irq Value After Reset:0x0
17	WO	0x0	EARCRX_CMDC_RXPKT_BADPAR_FORCE Force for earcrx_cmdc_rxpkt_badpar_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_rxpkt_badpar_irq Value After Reset:0x0
16	WO	0x0	EARCRX_CMDC_RXPKT_BADECC_FORCE Force for earcrx_cmdc_rxpkt_badecc_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_rxpkt_badecc_irq Value After Reset:0x0
15	WO	0x0	EARCRX_CMDC_RXPKT_INCOMPLETE_FORCE Force for earcrx_cmdc_rxpkt_incomplete_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_rxpkt_incomplete_irq Value After Reset:0x0
14	WO	0x0	EARCRX_CMDC_RXPKT_BADSYNC_FORCE Force for earcrx_cmdc_rxpkt_badsync_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_rxpkt_badsync_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
13	WO	0x0	EARCRX_CMDC_RXPKT_BADPREAMBLE_FORCE Force for earcrx_cmdc_rxpkt_badpreamble_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_rxpkt_badpreamble_irq Value After Reset:0x0
12	WO	0x0	EARCRX_CMDC_HEARTBEAT_CAP_CHNG_FORCE Force for earcrx_cmdc_heartbeat_cap_chng_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_heartbeat_cap_chng_irq Value After Reset:0x0
11	WO	0x0	EARCRX_CMDC_HEARTBEAT_STAT_CHNG_FORCE Force for earcrx_cmdc_heartbeat_stat_chng_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_heartbeat_stat_chng_irq Value After Reset:0x0
10	WO	0x0	EARCRX_CMDC_HEARTBEAT_LOST_FORCE Force for earcrx_cmdc_heartbeat_lost_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_heartbeat_lost_irq Value After Reset:0x0
9	WO	0x0	EARCRX_CMDC_DISCOVERY_TIMEOUT_FORCE Force for earcrx_cmdc_discovery_timeout_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_discovery_timeout_irq Value After Reset:0x0
8	WO	0x0	EARCRX_CMDC_DISCOVERY_DONE_FORCE Force for earcrx_cmdc_discovery_done_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_cmdc_discovery_done_irq Value After Reset:0x0
7:0	RW	0x00	Reserved0 Reserved Field:Yes

HDMI TX Controller_EARCRX_1_INT_STATUS

Address: Operational Base + offset (0x4820)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved0 Reserved Field:Yes
8	RO	0x0	EARCRX_DMAC_USRDATA_MSG_GENERIC_CHG_IRQ eARC RX DMAC User Data Generic Message payload change interrupt event Value After Reset:0x0
7	RO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_CHG_IRQ eARC RX DMAC User Data H14b ISRC2 Message payload change interrupt event Value After Reset:0x0
6	RO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_CHG_IRQ eARC RX DMAC User Data H14b ISRC1 Message payload change interrupt event Value After Reset:0x0

Bit	Attr	Reset Value	Description
5	RO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_CHG_IRQ eARC RX DMAC User Data H14b ACP Message payload change interrupt event Value After Reset:0x0
4	RO	0x0	EARCRX_DMAC_ECC_RX_CHECK_UNCERR_IRQ eARC RX DMAC Uncorrectable errors in the received Compressed Audio interrupt event Value After Reset:0x0
3	RO	0x0	EARCRX_DMAC_AUDIO_MUTE_CHG_IRQ eARC RX DMAC Audio mute status change interrupt event Value After Reset:0x0
2	RO	0x0	EARCRX_DMAC_AUDIO_TYPE_CHG_IRQ eARC RX DMAC Audio type status change interrupt event Value After Reset:0x0
1	RO	0x0	EARCRX_DMAC_CHSTATUS_BLOCK_CHG_IRQ eARC RX DMAC Channel Status block payload changed interrupt event Value After Reset:0x0
0	RO	0x0	EARCRX_DMAC_BPRXSAMPLER_PARITY_ERR_IRQ eARC RX DMAC Biphase-mark decoder IEC 60958 frame parity error in the received audio stream interrupt event Value After Reset:0x0

HDMI TX Controller_EARCRX_1_INT_MASK_N

Address: Operational Base + offset (0x4824)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved0 Reserved Field:Yes
8	RW	0x0	EARCRX_DMAC_USRDATA_MSG_GENERIC_CHG_MASK_N Mask for earcrx_dmac_usrdata_msg_generic_chg_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_usrdata_msg_generic_chg_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_usrdata_msg_generic_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
7	RW	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_CHG_MASK_N Mask for earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
6	RW	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_CHG_MASK_N Mask for earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

Bit	Attr	Reset Value	Description
5	RW	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_CHG_MASK_N Mask for earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
4	RW	0x0	EARCRX_DMAC_ECC_RX_CHECK_UNCERR_MASK_N Mask for earcrx_dmac_ecc_rx_check_uncerr_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_ecc_rx_check_uncerr_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_ecc_rx_check_uncerr_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
3	RW	0x0	EARCRX_DMAC_AUDIO_MUTE_CHG_MASK_N Mask for earcrx_dmac_audio_mute_chg_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_audio_mute_chg_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_audio_mute_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
2	RW	0x0	EARCRX_DMAC_AUDIO_TYPE_CHG_MASK_N Mask for earcrx_dmac_audio_type_chg_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_audio_type_chg_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_audio_type_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
1	RW	0x0	EARCRX_DMAC_CHSTATUS_BLOCK_CHG_MASK_N Mask for earcrx_dmac_chstatus_block_chg_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_chstatus_block_chg_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_chstatus_block_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0
0	RW	0x0	EARCRX_DMAC_BPRXSAMPLER_PARITY_ERR_MASK_N Mask for earcrx_dmac_bprxsampler_parity_err_irq. Values: 0x0 (MASK): Write 0 to mask earcrx_dmac_bprxsampler_parity_err_irq. 0x1 (UNMASK): Write 1 to unmask earcrx_dmac_bprxsampler_parity_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted. Value After Reset:0x0

HDMI TX Controller_EARCRX_1_INT_CLEAR

Address: Operational Base + offset (0x4828)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved0 Reserved Field:Yes
8	WO	0x0	EARCRX_DMAC_USRDATA_MSG_GENERIC_CHG_CLEAR Clear for earcrx_dmac_usrdata_msg_generic_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_usrdata_msg_generic_chg_irq Value After Reset:0x0
7	WO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_CHG_CLEAR Clear for earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq Value After Reset:0x0
6	WO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_CHG_CLEAR Clear for earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq Value After Reset:0x0
5	WO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_CHG_CLEAR Clear for earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq Value After Reset:0x0
4	WO	0x0	EARCRX_DMAC_ECC_RX_CHECK_UNCERR_CLEAR Clear for earcrx_dmac_ecc_rx_check_uncerr_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_ecc_rx_check_uncerr_irq Value After Reset:0x0
3	WO	0x0	EARCRX_DMAC_AUDIO_MUTE_CHG_CLEAR Clear for earcrx_dmac_audio_mute_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_audio_mute_chg_irq Value After Reset:0x0
2	WO	0x0	EARCRX_DMAC_AUDIO_TYPE_CHG_CLEAR Clear for earcrx_dmac_audio_type_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_audio_type_chg_irq Value After Reset:0x0
1	WO	0x0	EARCRX_DMAC_CHSTATUS_BLOCK_CHG_CLEAR Clear for earcrx_dmac_chstatus_block_chg_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_chstatus_block_chg_irq Value After Reset:0x0
0	WO	0x0	EARCRX_DMAC_BPRXSAMPLER_PARITY_ERR_CLEAR Clear for earcrx_dmac_bprxsampler_parity_err_irq Values: 0x1 (CLEAR): Write 1 to clear earcrx_dmac_bprxsampler_parity_err_irq Value After Reset:0x0

HDMI TX Controller_EARCRX_1_INT_FORCE

Address: Operational Base + offset (0x482C)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved0 Reserved Field:Yes
8	WO	0x0	EARCRX_DMAC_USRDATA_MSG_GENERIC_CHG_FORCE Force for earcrx_dmac_usrdata_msg_generic_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_usrdata_msg_generic_chg_irq Value After Reset:0x0
7	WO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC2_CHG_FORCE Force for earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq Value After Reset:0x0
6	WO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ISRC1_CHG_FORCE Force for earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq Value After Reset:0x0
5	WO	0x0	EARCRX_DMAC_USRDATA_MSG_HDMI_ACP_CHG_FORCE Force for earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq Value After Reset:0x0
4	WO	0x0	EARCRX_DMAC_ECC_RX_CHECK_UNCERR_FORCE Force for earcrx_dmac_ecc_rx_check_uncerr_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_ecc_rx_check_uncerr_irq Value After Reset:0x0
3	WO	0x0	EARCRX_DMAC_AUDIO_MUTE_CHG_FORCE Force for earcrx_dmac_audio_mute_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_audio_mute_chg_irq Value After Reset:0x0
2	WO	0x0	EARCRX_DMAC_AUDIO_TYPE_CHG_FORCE Force for earcrx_dmac_audio_type_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_audio_type_chg_irq Value After Reset:0x0
1	WO	0x0	EARCRX_DMAC_CHSTATUS_BLOCK_CHG_FORCE Force for earcrx_dmac_chstatus_block_chg_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_chstatus_block_chg_irq Value After Reset:0x0

Bit	Attr	Reset Value	Description
0	WO	0x0	EARCRX_DMAC_BPRXSAMPLER_PARITY_ERR_FORCE Force for earcrx_dmac_bprxsampler_parity_err_irq Values: 0x1 (FORCE): Write 1 to trigger earcrx_dmac_bprxsampler_parity_err_irq Value After Reset:0x0

24.5 Interface Description

Table 24-1 HDMI TX PHY0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
hdmitx0_ln0_txdp	O	HDMI_TX0_D0P/eDP_TX0_D0P	NS
hdmitx0_ln0_txdn	O	HDMI_TX0_D0N/eDP_TX0_D0N	NS
hdmitx0_ln1_txdp	O	HDMI_TX0_D1P/eDP_TX0_D1P	NS
hdmitx0_ln1_txdn	O	HDMI_TX0_D1N/eDP_TX0_D1N	NS
hdmitx0_ln2_txdp	O	HDMI_TX0_D2P/eDP_TX0_D2P	NS
hdmitx0_ln2_txdn	O	HDMI_TX0_D2N/eDP_TX0_D2N	NS
hdmitx0_ln3_txdp	O	HDMI_TX0_D3P/eDP_TX0_D3P	NS
hdmitx0_ln3_txdn	O	HDMI_TX0_D3N/eDP_TX0_D3N	NS
hdmitx0_sbdp	I/O	HDMI_TX0_SBDP/eDP_TX0_AUXP	NS
hdmitx0_sbdn	I/O	HDMI_TX0_SBDN/eDP_TX0_AUXN	NS
hdmitx0_cec_m0	I/O	BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d	BUS_IOC_GPIO4C_IOMUX_SEL_L[7:4]==5
hdmitx0_cec_m1	I/O	I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[7:4]==d
hdmitx0_hpd_m0	I/O	HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[7:4]==5
hdmitx0_hpd_m1	I/O	HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d	BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0]==3
hdmitx0_scl_m0	I/O	BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/DDRPHY_CH3_DTB3/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7_u	BUS_IOC_GPIO4B_IOMUX_SEL_H[15:12]==5
hdmitx0_scl_m1	I/O	I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u	BUS_IOC_GPIO0D_IOMUX_SEL_H[7:4]==b
hdmitx0_scl_m2	I/O	CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u	PMU2_IOC_GPIO0D_IOMUX_SEL_H[7:4]==8 BUS_IOC_GPIO3C_IOMUX_SEL_H[15:12]==5
hdmitx0_sda_m0	I/O	BT1120_D14/PCIE20X1_2_WAKEN_M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0_u	BUS_IOC_GPIO4C_IOMUX_SEL_L[3:0]==5
hdmitx0_sda_m1	I/O	I2S1_SDO2_M1/PDM0_SDI2_M1/P	BUS_IOC_GPIO

Module Pin	Direction	Pad Name	IOMUX Setting
		WM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u	0D_IOMUX_SEL_H[3:0]==b
hdmitx0_sda_m2	I/O	CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u	PMU2_IOC_GPIO0D_IOMUX_SEL_H[3:0]==8 BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0]==5

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 24-2 HDMI TX PHY1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
hdmitx1_ln0_txdp	O	HDMI_TX1_D0P/eDP_TX1_D0P	NS
hdmitx1_ln0_txdn	O	HDMI_TX1_D0N/eDP_TX1_D0N	NS
hdmitx1_ln1_txdp	O	HDMI_TX1_D1P/eDP_TX1_D1P	NS
hdmitx1_ln1_txdn	O	HDMI_TX1_D1N/eDP_TX1_D1N	NS
hdmitx1_ln2_txdp	O	HDMI_TX1_D2P/eDP_TX1_D2P	NS
hdmitx1_ln2_txdn	O	HDMI_TX1_D2N/eDP_TX1_D2N	NS
hdmitx1_ln3_txdp	O	HDMI_TX1_D3P/eDP_TX1_D3P	NS
hdmitx1_ln3_txdn	O	HDMI_TX1_D3N/eDP_TX1_D3N	NS
hdmitx1_sbdp	I/O	HDMI_TX1_SBDP/eDP_TX1_AUXP	NS
hdmitx1_sbdn	I/O	HDMI_TX1_SBDN/eDP_TX1_AUXN	NS
hdmitx1_cec_m0	I/O	GMAC0_PPSCLK/TEST_CLKOUT_M1/HDMI_TX1_CEC_M0/UART9_RX_M0/SPI1_CS1_M0/GPIO2_C4_d	PMU2_IOC_GPIO0D_IOMUX_SEL_L[7:4]==8 BUS_IOC_GPIO2C_IOMUX_SEL_H[3:0]==0
hdmitx1_cec_m1	I/O	I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[11:8]==d
hdmitx1_cec_m2	I/O	CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u	PMU2_IOC_GPIO0D_IOMUX_SEL_L[11:8]==8 BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0]==5
hdmitx1_hpd_m0	I/O	HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[11:8]==5
hdmitx1_hpd_m1	I/O	GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d	BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12]==5
hdmitx1_scl_m0	I/O	GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u	BUS_IOC_GPIO2B_IOMUX_SEL_H[7:4]==4
hdmitx1_scl_m1	I/O	CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[11:8]==5
hdmitx1_scl_m2	I/O	HDMI_TX1_SCL_M2/SPI2_MISO_M0/GPIO1_A4_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[3:0]==5
hdmitx1_sda_m0	I/O	GMAC0_PTP_REFCLK/FSPI_CS0N_	BUS_IOC_GPIO

Module Pin	Direction	Pad Name	IOMUX Setting
		M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u	2B_IOMUX_SEL_H[3:0]==4
hdmitx1_sda_m1	I/O	CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4]==5
hdmitx1_sda_m2	I/O	HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d	BUS_IOC_GPIO1A_IOMUX_SEL_L[15:12]==5

Notes: I=input, O=output, I/O=input/output, bidirectional

24.6 Application Notes

24.6.1 Controller Programming Model

Figure 24-6. shows the recommended programming sequence to build an HDMI-compliant system. The main operation mode is the HDMI TX Controller's configuration.

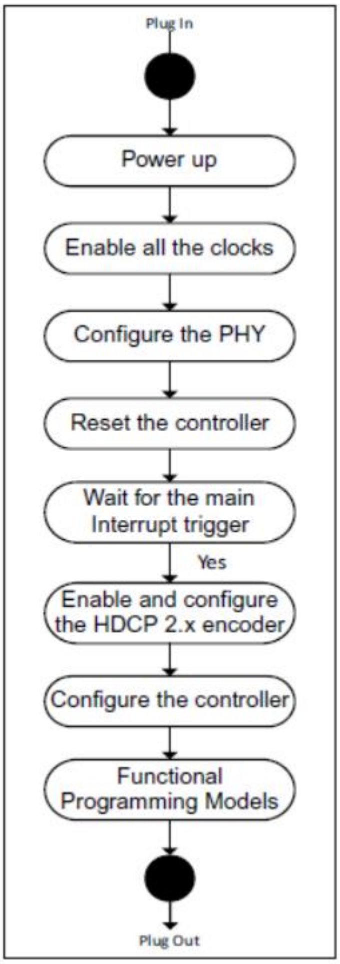

Fig. 24-6 Programming Sequence

24.6.1.1 Enabling the clocks

Enable all the clocks. The different clocks and their functions are the lists.

- apb_pclk: APB system interface clock.
- audclk: Audio interface clock.
- earc_bpclk: EARC RX audio interface biphase clock.
- ipi_clk: IPI interface clock.
- linkqpclk: Link quad-pixel clock.linkqpclk acts as TDMS clock in HDMI mode and as FRL clock in FRL mode. Synchronous to HDCP14 Encoder.
- refclk: Reference clock. Generates timer bases of different frequencies which can be used by counters of different timers. Synchronous to I2C master.
- vidqpclk: Video datapath clock.

24.6.1.2 Configuring the PHY
Configure the PHY as the HDMI eDP Combo PHY user guide (if applicable). Drive the required system and configuration clocks and pins with the required clock frequency.

24.6.1.3 Resetting the Controller
Reset the controller using the imainrst_n signal.

24.6.1.4 Triggering the Main Interrupt
Wait for the main interrupt line omain_int to be triggered. The apb_regbank_ready_irq is unmasked by default and notifies the software that the reset operation is complete and APB interface is online.

24.6.1.5 Configuring the HDCP 2.x Encoder
Enable and configure the HDCP2.x as per the HDCP2.x user guide (if applicable).

24.6.1.6 Configuring the Controller
This section describes the steps involved in configuring the HDMI TX Controller. Configure the timer_reference_base field of the timer_base_config0 register and wait for the timer_base_locked_irq interrupt to be triggered.

24.6.1.6.1 Configuring the Link
Configure the following components using the link_config0 register, DVI or HDMI, TMDS or FRL, FRL 3L or FRL 4L.

24.6.1.6.2 Configuring the Packets
Configure the following packet properties using the pktsched_* and pkt_<packet_type>* registers (if applicable), Packet contents - Register Writes, Scheduling options for the different packets.

24.6.1.6.3 Configuring the HDCP 1.4 Encoder
Configure the HDCP 1.4 using the hdcp14_* registers.

1. Write the hdcp14_an_value_high/low fields of the hdcp14_key_h/l registers.
2. Set HDCP 14 key encryption enable using the hdcp14_key_decrypt_en field of the hdcp14_config* registers if necessary.
3. Configure the decryption SEED using the hdcp14_key_decrypt_seed field of the hdcp14_key_seed register. Configure the HDCP An value, using the hdcp14_an_value_high/low fields of the hdcp14_an_h/l registers.
4. If the DKSET is stored in the register bank-(HDMI_QP_TX_HDCP14_DKSET_EXTERNAL=0) Write the HDCP keys in order, using the hdcp14_key_high/low fields of the hdcp14_key_h/l registers. For each HDCP Key, the MSB part (hdcp14_key_high), should be written first. Write the hdcp_aksv_high/low fields of the hdcp_aksv_h/l (40-bits for the hdcp_aksv_high) registers.
5. Initialize the HDCP Memories. Write the HDCP 1.4 KSV list in the revocation memory.
6. Update the HDCP HPD status using the hdcp14_hpd field of the hdcp14_config* registers.

24.6.1.6.4 Configuring the Audio Settings
Configure the audio settings, enable the interfaces, format status, pair layout, and so on using the audio_interface_[config/control/status]0 registers. Configuration of the number of active lanes and audio formats for the Serial Audio interface. Configure the related audio packet types-ACR, AMD, AUDI, ACP, ISRC BPCUV, user data, and others that can be overridden if they are not provided at audio interface input.

24.6.1.6.5 Configuring the Video Settings
Configure the pixel repetition factor using the vid_pr_factor [3:0] field of the video_interface_config1 register if required.

24.6.1.6.6 Configuring the SCDC
Configure the SCDC using the scdc_* and i2cm_* registers. You can configure the Scrambling, TMDS clock ratio, RR enable, FRL Rate, FFE levels, and so on.

24.6.1.6.7 Enabling Audio and Video Inputs
Provide data at the audio and video inputs.

24.6.1.6.8 Link Training
The Link Training procedure described in this section, requires the HDMI 2.1 TX Support parameter to be enabled. Otherwise, you should skip the Step 1.

1. Disable the video datapath of the AVP module by setting the

avp_datapath_video_swdisable field of the global_swdisable register. This enables the generation of GAPs only.
2. Update the scdc_config0 register to choose between. Polling by setting the scdc_upd_flags_poll_en field, or read request by setting the scdc_rr_en field. If you want to set an automatic clear after a read operation, set the scdc_upd_flags_audo_clr field.
3. Check if the update flag scdc_upd_flags_1/0 (Polling FLT_ready) has been changed by reading scdc_status0 register when the scdc_upd_flags_rd_irq interrupt of the mainunit_1_int_status register is triggered.
4. When the the FLT_ready is set, configure the FRL rate and the FFE levels on the Sink. To perform this write operation using the I2C, set the I2CM_write field of the I2CM_interface_control0 register. The FFE levels should also be set using the flt_ffe_levels field of the flt_config0 register.
5. Set the flt_start_p field of the flt_control0 register to start LTS:3. Hardware triggers the flt_exit_to_ltsp_irq interrupt of the mainunit_1_int_status register, after LTS:3 is complete. The hardware automatically completes all the LTS:3 operations.
6. Clear FLT_Update and monitor the scdc_upd_flags_clr_irq field of the mainunit_1_int_status register or the scdc_upd_flags_rd_p fields of the scdc_control0 register. Set the scdc_upd_flags_rd_p field of the scdc_control0 register to trigger an automatic read operation.
7. Check if the update flag scdc_upd_flags_1/0 has been set (Polling FRL_start) by reading the scdc_status0 register, when the scdc_upd_flags_rd_irq interrupt of the mainunit_1_int_status register is triggered. If scdc_upd_flags_* is set Link Training is complete.
8. Unset the avp_datapath_video_swdisable field of the global_swdisable register.

24.6.2 HDMI Audio and Video Programming Model

24.6.2.1 Audio Interface Programming Model

24.6.2.1.1 Audio Interfaces Configurations

The audio interface configurations can be performed using the audio_interface_config0 and audio_interface_config1 registers. Monitoring the audio interfaces can be performed using the audio_interface_status0 register and other interrupts. The required system configurations for the different audio interfaces are described in the following sections.

24.6.2.1.1.1 I2S Interface

The following section describes the system configurations for the I2S audio interface.
1. Select the I2S interface as the audio source, by setting the aud_if_sel[1:0] field of the audio_in-terface_config0 register to 2'h1.
2. Enable the active I2S lanes by configuring i2s_lines_en[3:0] field of the audio_interface_con-fig0 register. Each bit enables the respective data lane, i2s_lines_en[0] enables lane 0, i2s_lines_en[1] enables lane 1, i2s_lines_en[2] enables lane 2, i2s_lines_en[3] enables lane 3.
3. Enable the reception of the BPCUV bits (when transmitted), by setting i2s_bpcuv_en field of the audio_interface_config0 register to 1’b1.
4. Configure the audio format that is being received by writing the desired value to aud_format[2:0] field of the audio_interface_config0 register as shown in the list.
Audio Sample is Packet Type. Packet Type Value is 0x2, aud_format is 0x0.
HBR Audio Sample is Packet Type. Packet Type Value is 0x9, aud_format is 0x3.
Multi-Stream Audio Sample is Packet Type. Packet Type Value is 0xe, aud_format is 0x4.
5. When BPCUV bits reception is enabled, by default the B bit is extracted from the information received in the left channel. It is possible to force the receiver to extract the B bit from the right channel by setting the i2s_bbit_right field of the audio_interface_config0 register to 1’b1.
6. I2S operation can be monitored through the following interrupts, i2s_ws_err_irq interrupt indicates an illegal variation detected on iws_ws signal, i2s_bbit_err_irq interrupt indicates a mismatch between the B bits received in the left and right channels.

24.6.2.1.1.2 S/PDIF Interface

The following section describes the system configurations for the S/PDIF audio interface. 1.

Select the S/PDIF interface as the audio source, by setting aud_if_sel[1:0] field of the audio_interface_config0 register to 2'h2.
2. Enable the active S/PDIF lanes by configuring spdif_lines_en[3:0] field of the audio_interface_config0 register. Each bit enables the respective data lane, spdif_lines_en[0] enables lane 0, spdif_lines_en[1] enables lane 1, spdif_lines_en[2] enables lane 2, spdif_lines_en[3] enables lane 3.
3. Configure the audio format that is being received by writing the appropriate value to aud-format[2:0] field of the audio_interface_config0 register.
4. Data reception is done independently for each lane since there are four S/PDIF lanes.
5. It is possible to have a timing mismatch in the reception of the two different channels. By default, S/PDIF data is sampled using the timing of S/PDIF lane 0. This can be changed by configuring a different lane in spdif_pair_sel[1:0] field of the audio_interface_config0 register, 2’h0 selects lane 0, 2’h1 selects lane 1, 2’h2 selects lane 2, 2’h3 selects lane 3.
6. Monitor the S/PDIF reception through the following register bank entries. a. When data is being received correctly on the S/PDIF lines, the corresponding entries within the {spdif_line0_lock spdif_line1_lock spdif_line2_lock spdif_line3_lock} fields are enabled (set to 1’b1) b. Parity errors in the received data are signaled for the different S/PDIF lines through the spdif_line0_parity_err, spdif_line1_parity_err, spdif_line2_parity_err, and spdif_line3_parity_err interrupts c. Encoding errors in the received information are signaled for the different S/PDIF lines through the spdif_line0_protocol_err, spdif_line1_protocol_err, spdif_line2_proto-col_err, and spdif_line3_protocol_err interrupts.

24.6.2.1.2 Audio Storage

The received audio data may need to be stored before being transmitted; for example, audio received during an active video line can only be transmitted in the next blanking period. The audio storage can be configured and monitored through the following fields.
1. Overflows and underflows are signaled by the audfifo_ovf_irq and audfifo_udf_irq interrupts, respectively.
2. Audio FIFO can be cleared by setting the audfifo_clr_p field of the audio_interface_control0 register to 1’b1.
3. Audio FIFO can be configured to automatically clear itself, when an overflow occurs by setting the audfifo_init_on_ovf field of the audio_interface_config0 register to 1’b1.

24.6.2.2 Audio Packetizer Programming Model

24.6.2.2.1 Configure Audio Transmission

You should perform this process only if the HDMI TX Controller is configured in HDMI mode. In DVI mode, audio is not transmitted. The selected audio mode should be supported by the source (transmitter) and the sink (receiver) of the audio. The audio capabilities of the receiver are extracted from the E-EDID information. The steps to configure audio transmission are as follows.
1. Disable all audio sources.
2. Enable the audio data path of the AVP module by writing 1'b0 to the avp_datapath_packet_audio_swdisable field of the global_swdisable register.
3. Perform the reset of the audio data path of the AVP module by writing 1'b1 to the avp_datapath_packet_audio_swinit_p field of the global_swreset_request register.
4. Disable the transmission of the AUDS, ACR, AUDI, and AMD packets by writing 1'b0 to their corresponding fields as shown, AUDS: pktsched_auds_tx_en, ACR: pktsched_acr_tx_en. AUDI: pktsched_audi_tx_en, AMD: pktsched_amd_tx_en.
5. Select and configure the audio interfaces I2S, S/PDIF.
6. Configure the audio parameters. a. Audio Clock Regeneration.
i. Fix the audio at N factor for Audio Clock Regeneration. This factor depends on the audio sampling rate and video mode. For more information, see the *HDMI 2.1 Specification*.
ii. Write the audpkt_acr_n_value field of the audpkt_acr_control0 register.
iii. Set audio CTS factor for Audio Clock Regeneration.
7. Enable the transmission of the ACR, AUDI, and AMD packets by writing 1'b1 to their corresponding bit fields as shown, ACR: pktsched_acr_tx_en, AUDI: pktsched_audi_tx_en, AMD: pktsched_amd_tx_en.
8. Enable the transmission of the AUDS packet by writing 1'b1 to the pktsched_auds_tx_en field of the pktsched_pkt_en register.

9. Enable the audio sources according to the selected interface.
10.At this step, the software can continue to transmit the audio that it configured in the frames, or go back to Step 1 to reconfigure a new audio setup.

24.6.3 CEC Programming Model

24.6.3.1 Sending a Frame

The steps to send a CEC frame are as follows. 1. Write the frame message size (in bytes), to the cec_rxbuffer_cnt field of the cec_rx_count register.
2. Write the data to be transmitted, to the cec_rxbuffer_data_## (## represents 0 to 15).
a. The first cec_rxbuffer_data_0 byte is the header block and is mapped as cec_rxbuffer_data_0[7:0]={Initiator_address[3:0], Destination_address[3:0]}.
b. Fill the rest of the cec_rxbuffer_data_[15:1] fields with the data bytes to be transmitted (if necessary).
3. Order the CEC to send the frame by writing 1 to the frame_send_set_p field of the cec_tx_control register.
4. If the frame is: Successfully sent, then the cectx_done_irq field of the cec_int_status register is asserted. Not sent successfully, then one or more of the following interrupts can be triggered: cectx_nack_irq field of the cec_int_status register; cectx_arblost_irq field of the cec_int_status register; cectx_line_err_irq field of the cec_int_status register; cectx_nretransmit_fail_irq field of the cec_int_status register; cectx_frame_discarded_irq field of the cec_int_status register.

24.6.3.2 Read a Received Frame

The steps to read a received frame are as follows:
1. The software is informed that a frame is received successfully when the cecrx_eom_irq field of the cec_int_status register is triggered.
2. Read the cec_tx_count register to obtain information about: a. cec_txbuffer_cnt–number of bytes received (including header).
3. Read the necessary bytes from the TX buffer registers cec_txbuffer_data_## (0-15) accordingly with the information obtained in the cec_rx_count_status bit field.

24.6.3.3 Initial CEC Configuration

To use the CEC module, you must set up the following configuration registers.

24.6.3.3.1 CEC Configuration Register

The table shows the CEC configuration register cec_config and the different fields associated with the initial configuration.

Table 24-3 CEC Configuration Register

Field Name	Functionality
txreq_discard_if_rxbusy	Discards a transmit request (cec_ctrl.send=1) if receiver is busy
broadcast_nack	NACK to any received broadcast message by the CEC module. Message is not stored in the receiver registers.
cecfilter	Enable the CEC input filter.
frame_nretrans	Enable the CEC input filter.
rx_automatic_drive_acknowledge	Receiver automatic drive acknowledge.
signal_free_time	Selects the Signal Free time period that is to be respected before attempting to transmit or re-transmit a frame. If 0 is selected then the controller follows the HDMI specification in CEC 9.1 Signal free time.

24.6.3.3.2 CEC Address Register

The CEC address register-cec_addr should be set when the logical allocation is completed. You can define multiple addresses.

24.6.3.4 Cancel a TX Frame

You can cancel a TX frame by writing 1’b1 to the frame_send_clr field of the cec_tx_control register, if the frame to be transmitted is waiting for the end of an incoming frame (RX busy); the frame is set to be re-transmitted.
If the TX frame is already under transmission, then it is pushed to completion and not

cancelled.

24.6.3.5 Status Fields

The table shows the CEC status register cec_status and the different fields associated with the initial configuration.

Table 24-4 Status Fields

Field Name	Functionality
frame_send_pending_st	Frame is set to be transmitted. It is 1’b1 while a transmission is ongoing.
cecrx_busy_st	The CEC module is busy receiving a frame.
cectx_busy_st	The CEC module is busy transmitting a frame.

24.6.3.6 Interrupts

The table shows the CEC interrupts available in the cec_int_status register and conditions under which it is triggered.

Table 24-5 CEC Interrupts

Field Name	Functionality
cectx_done_irq	Frame transmission is completed successfully
cectx_nack_irq	NACK for direct address or broadcast is received while transmitting a frame
cectx_arblost_irq	CEC line arbitration is lost to another initiator
cectx_line_err_irq	Line error while transmitting a frame (detected a 0 instead of a 1)
cectx_nretransmit_fail_irq	All re-transmission attempts failed.
cectx_frame_discarded_irq	Frame to be sent was discarded since a new frame was received. Happens only when txreq_discard_if_rxbusy==1’b1.
cectx_busy_irq	The CEC TX FSM changes its busy state.
cecrx_busy_irq	The CEC RX FSM changes its busy state.
cectx_drive_err_irq	Drive zero in the CEC output is not seen in the CEC input.
cecrx_eom_irq	Frame is fully received with EOM after the last data block.
cecrx_notify_err_irq	Bit timing error is detected while cecrx_busy_irq is set. Error notification is sent to initiator.

24.6.3.7 CEC Bit Timing Fine Tuning

This is a debug-only feature that allows out-of-spec timings to be defined; to debug the CEC module. You can configure this feature by using the cec_rxqual_bittime_config register.

24.6.4 eARC Programming Model

The eARC RX controller enables simultaneous asynchronous operation of two different data channels. These data channels are operated independently and each has its own programming model.

24.6.4.1 Common Mode Data Channel Programming Model

Single read and write transactions, following an initial eARC Discovery process. Each read and write transactions can carry a payload of 1 to 255 bytes. The payload should have a defined payload size, device ID, and offset address. The hardware periodically performs a keep-alive mechanism called Heartbeat Sequence. The status and actions of the CMDC programming model are described in the following sections.

24.6.4.1.1 CMDC Configuration

You must configure the eARC RX CMDC controller before any operation. The registers used to configure the CMDC controller and their actions are as follows:

earcrx_cmdc_config0.

Handling of packet errors, ECC bit ordering, and parity errors.

Enabling device ID or offset whitelist enable.

Setting transaction timeout, restart, and data overflow.

Setting COMMA count for Discovery.

Loss enable for Heartbeat transactions.

earcrx_cmdc_config1.
Setting device ID or offset for the Heartbeat transactions
earcrx_cmdc_whitelist[0:3]_config.
Setting the allowed device ID or offset pairs, when whitelist is enabled.
earcrx_cmdc_sync_config.
Setting the pulse filter for eARC CMDC asynchronous inputs.
For more information on the field descriptions, see the "Register Description" chapter in the Databook.

24.6.4.1.2 Connect and Discovery

The CMDC Connect and Discovery steps are as follows:
1. Enable the eARC RX CMDC Discovery process by setting the earcrx_cmdc_discovery_en field of the earcrx_cmdc_control register.
2. The eARC TX device drives a logic-high-voltage-level pulse on the physical HPD connector pin, after at least 100 ms of low voltage level to start the eARC Discovery process. The software sets the earcrx_connector_hpd=1 field of the earcrx_cmdc_control register, when the correct voltage level is detected on physical HPD connector pin.
3. The hardware starts and performs the Discovery process by interacting with the eARC TX device after the HPD bit is asserted.
4. The hardware drives the COMMA sequences to the line and monitors the Heartbeat transactions from the eARC TX device, where the EARC_RX_STAT and EARC_TX_STAT status registers are exchanged between the two eARC devices.
5. The Discovery process is completed when the eARC TX device sets the EARC_VALID=1 field of the EARC_TX_STAT register. The next state is the [RX eARC].
6. There are two possible outcomes for the Discovery process that are communicated to software through the interrupts. earcrx_cmdc_discovery_done_irq: The eARC Discovery is complete and transactions can be executed. earcrx_cmdc_discovery_timeout_irq: A TeARC_RX_TIMEOUT timeout has occurred while waiting for a Heartbeat sequence with the EARC_TX_STAT.EARC_VALID=1 from the eARC TX device from [eARC TX], during Discovery. The eARC Discovery is not attempted again and the software can now request an H14b ARC connection if required. If the H14b ARC is used, earcrx_h14barc_active=1 field of the earcrx_cmdc_control register should be set. To perform eARC Discovery again, the H14b ARC mode must be disabled (earcrx- _h14barc_active=0). The eARC RX device waits for the opposing eARC TX device to set the HPD voltage low. When HPD low is detected, the software clears the HPD connector bit (earcrx_connector_hpd=0), and then returns to Step 2.
7. The eARC TX device can reset the eARC Discovery process to its initial state by setting the connector HPD voltage low. The software must always clear the respective earcrx_connector_hpd=0 field of the earcrx_cmdc_control register at this event, and then return to Step 2.
8. The Discovery state machine reverts to the state [RX DISC1] (Step 3), when in an active [RX eARC] state, if one of the following conditions occur: A Heartbeat Loss condition is detected; A valid Heartbeat is received with status bit EARC_TX_STAT:EARC_VALID=0 .
9. The current state of the Discovery state machine is available at earcrx_cmdc_discovery_state field of the earcrx_cmdc_status register. The state diagram follows the *HDMI 2.1 Specification*, as shown in Figure.

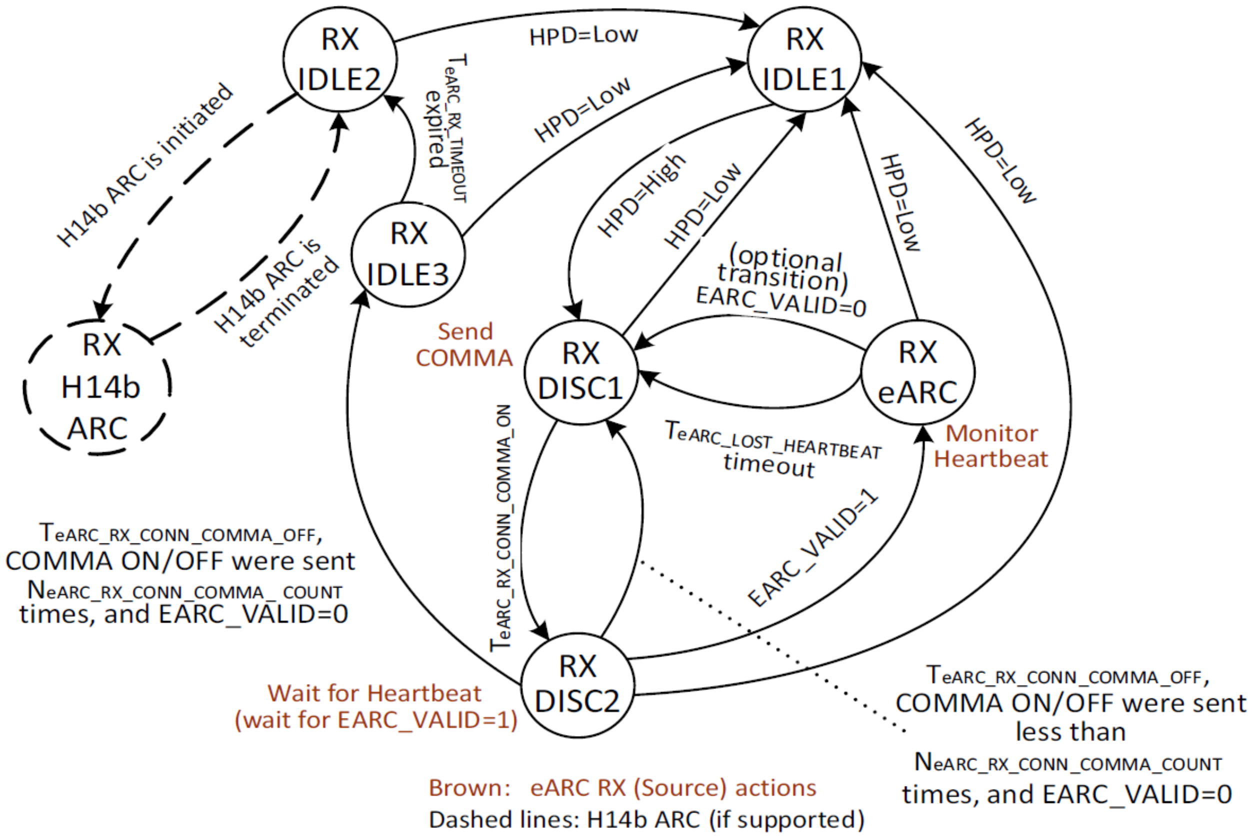

Fig. 24-6 HDMI2.1 Specification -eARC RX Discovery State Diagram

24.6.4.1.3 Heartbeat Sequence

The hardware automatically completes the Heartbeat sequence during the Discovery and regular Transaction operation, at time intervals TeARC_HEARTBEAT as initiated by the eARC TX device. The hardware performs a Heartbeat sequence as an uninterrupted read or write transaction pair, performed by reading EARC_RX_STAT status register from the eARC RX device, and writing the EARC_TX_STAT register into the eARC RX device. Each device manages the content of its status register. The software can verify the values of both status registers at any time. EARC_RX_STAT=earcrx_cmdc_status[7:0]; EARC_TX_STAT=earcrx_cmdc_status[15:8].

The bit values received by the EARC_TX_STAT register are cleared when exiting the Discovery state [RX eARC].

24.6.4.1.3.1 Configuration and Control

The software sets the expected device ID and offset values for the two Heartbeat transactions in each sequence in the earcrx_cmdc_config1 register. By default, the register values follow the *HDMI 2.1 Specification*. The values for EARC_RX_STATUS field is set by the software in the earcrx_cmdc_heartbeat_rxstat_set register.

24.6.4.1.3.2 Heartbeat Loss

A Heartbeat Loss condition is signaled during active eARC operation [RX eARC] state, if a Heartbeat sequence is not completed after TeARC_LOST_HEARTBEAT after the last successful Heartbeat. This triggers the earcrx_cmdc_heartbeat_lost_irq interrupt.

24.6.4.1.3.3 HPD Operation

During the eARC operation, the physical HPD wire is re-purposed, after the eARC discovery is complete, so that the eARC devices can utilize the status bit for the HPD signaling instead of the physical HPD. This is used, for example, to signal that the EDID has changed, without disabling the eARC communication. The eARC TX device sends the HPD value through the Heartbeat status bit EARC_TX_STAT[0]: HDMI_HPD.

24.6.4.1.3.4 eARC RX Capabilities Data Structure Change

1. When the eARC RX device changes the Capabilities Data Structure, it results in an

exchange of CAP_CHNG and CAP_CHNG_CONF status bits which are set to 1 and back to 0, in several Heartbeat trans-action sequences.
2. The software starts this event by setting the earcrx_cmdc_heartbeat_rxstat_cap_chng_set=1 field of the earcrx_cmdc_heartbeat_rxstat_set register.
3. This sets the EARC_RX_STAT:CAP_CHNG bit to be sent, as 1 during Heartbeat transactions. 4. The hardware reverts the EARC_RX_STAT:CAP_CHNG bit to 0, when the eARC TX device sends back the EARC_TX_STAT:CAP_CHNG_CONF=1 bit.
5. The earcrx_cmdc_heartbeat_cap_chng_irq interrupt is triggered to notify the software that the handshake is complete.
6. Then the eARC TX device reads the eARC RX Capabilities Data Structure using a read transaction.

24.6.4.1.3.5 eARC RX Audio Latency Change

1. When the eARC RX device changes to the audio latency information, the ERX_LATENCY register is updated.
2. The two eARC devices communicate this change by an exchange of the STAT_CHNG and STAT_CHNG_CONF bits being set to 1 and back to 0, in several Heartbeat transaction sequences.
3. The software starts this event by setting the earcrx_cmdc_heartbeat_rxstat_stat_chng_set=1 bit of the earcrx_cmdc_heartbeat_rxstat_set register.
4. This sets the EARC_RX_STAT: STAT_CHNG bit to be sent, as 1 during Heartbeat transactions.
5. The hardware reverts the EARC_RX_STAT:STAT_CHNG status bit to 0, when the eARC TX device sends back EARC_RX_STAT:STAT_CHNG_CONF=1 bit.
6. The earcrx_cmdc_heartbeat_stat_chng_irq interrupt is triggered to notify software that the handshake is complete. Then the eARC TX device performs the required transactions for Audio Latency change, according to the *HDMI2.1 Specification.*

24.6.4.1.4 eARC Transactions

The hardware receives and handles the read or write transaction that is initiated by the eARC TX device. The software handles the transaction only when required and it is signaled by the relevant interrupt.

24.6.4.1.4.1 Device ID and Offset Whitelist

1. The hardware automatically checks for a valid device ID and offset, sent by the eARC TX device for any transaction type. Any device ID or Offset can be accepted. They can also be accepted from a specific whitelist set.
2. If the whitelist function is disabled earcrx_cmdc_whitelist_en=0, any device ID and offset are accepted, and the transaction progresses to the data stage.
3. If the whitelist function is enabled earcrx_cmdc_whitelist_en=1, only the device ID and offset pairs defined in the earcrx_cmdc_whitelist[3:0]_config registers are accepted. Any value combinations outside of those defined in the registers results in a NACK packet response, ending the transaction.

24.6.4.1.4.2 Write Transactions

1. The hardware handles all the write transactions automatically.
2. When the write transaction is completed, the earcrx_cmdc_xact_done_irq interrupt is triggered and earcrx_cmdc_xact_successful=1 field of the earcrx_cmdc_status register is set. 3. The software can now obtain the received data in the earcrx_cmdc_xact_wr[64:0] register. 4. The hardware responds with a NACK to any new write transaction when the software is fetching the transaction information and data.
5. When the software completes the data fetching, it sets the earcrx_cmdc_xact_wrdata_stored=1 field of the earcrx_cmdc_xact_action register.
6. After this step, the hardware can accept a new write transaction from the eARC TX controller.

24.6.4.1.4.3 Read Transactions

1. The hardware handles the read transactions automatically.
2. After the device ID and offset are received and valid, earcrx_cmdc_xact_read_data_irq interrupt is triggered.
3. The software writes the requested read data into the respective registers. earcrx_cmdc_xact_rd0[7:0]: earcrx_cmdc_xact_rdsize Read transaction data size in bytes-1. earcrx_cmdc_xact_rd[X] Payload data.
4. The hardware responds to the CONT packets with NACK, while the software is loading data. 5. After payload size and data is loaded into registers, the software sets the earcrx_cmdc_xact_rd-data_avail=1 field of the earcrx_cmdc_xact_action register.
6. The hardware starts responding to CONT packets with the payload data, up to the size indicated in earcrx_cmdc_xact_rdsize field of the earcrx_cmdc_xact_rd0 register.
7. When the read transaction is finished, earcrx_cmdc_xact_done_irq interrupt is triggered.

24.6.4.1.4.4 Transaction Results

When a transaction is completed, regardless of success, failure, or transaction type (read or write), the earcrx_cmdc_xact_done_irq interrupt is triggered. The software checks the registers as shown in the table.

Table 24-6 earcrx_cmdc_status Register Fields

Field Name	Functionality
earcrx_cmdc_xact_finished	0: Transaction ongoing 1: Transaction completed
earcrx_cmdc_xact_successful	1: Transaction completed successfully
earcrx_cmdc_xact_failed_unexpcmd	1: Transaction failed due to Unexpected Command packet from eARC TX controller
earcrx_cmdc_xact_failed_uncorrecterr	1: Transaction failed due to Uncorrectable Error in received packet
earcrx_cmdc_xact_failed_stop	1: Transaction failed due to received STOP before the payload data stage
earcrx_cmdc_xact_failed_deviceid	1: Transaction failed due to rejected device ID
earcrx_cmdc_xact_failed_offset	1: Transaction failed due to rejected offset
earcrx_cmdc_xact_timeout	1: Timeout occurred during a transaction, waiting for a packet from eARC TX device (programmable time in field earcrx_cmdc_rx_xact_timeout)
earcrx_cmdc_xact_corrected_errnum	Accumulated number of ECC corrected single-bit errors in received packets, during a transaction
earcrx_cmdc_xact_restarted	1: Transaction restarted due to the received eARC_READ or eARC_WRITE command packet at an unexpected time
earcrx_cmdc_xact_data_overflow	1: The eARC TX device has sent or requested to receive more than 256 bytes of data during a write or read transaction

Table 24-7 earcrx_cmdc_xact_info Register

Field Name	Functionality
earcrx_cmdc_xact_info	Information on the received transaction type, device ID, offset, and the effectively transferred payload data size

If the eARC link becomes unresponsive, a possible state of eARC line stuck high can be checked in earcrx_cmdc_status:earcrx_cmdc_stuckhigh field.

24.6.4.1.4.5 eARC RX CMDC Interrupts

During eARC RX CMDC operation the interrupts described in Table in the earcrx_0_int_status register can be triggered.

Table 24-8 earcrx_cmdc Interrupts

Interrupt Name	Functionality
earcrx_cmdc_discovery_done_irq	Discovery is completed successfully, reaching the state [RX eARC]; transactions can now be performed

earcrx_cmdc_discovery_timeout_irq	A TeARC_RX_TIMEOUT timeout has occurred during the Discovery waiting for a Heartbeat sequence with EARC_TX_STAT.EARC_VALID=1 from the eARC TX device. The eARC Discovery is not attempted anymore, and the software can now request an H14b ARC connection if needed. If H14b ARC mode is activated, the software should set the bit earcrx_cmdc_control:earctx_h14barc_active=1
earcrx_cmdc_heartbeat_lost_irq	The Heartbeat is lost while in [RX eARC] state (active eARC operation). This interrupt is triggered when TeARC_LOST_HEARTBEAT timeout elapses while waiting for a successful Heartbeat transaction if the earcrx_cmdc_heartbeat_loss_en=1
earcrx_cmdc_heartbeat_stat_chng_i rq	The STAT_CHNG or STAT_CHNG_CONF status bits' handshake in the Heartbeat transactions is completed successfully, after a software request for a audio latency information change notification (earcrx_cmdc_heartbeat_rxstat_set:earcrx_cmdc_heartbeat_rxstat_stat_chng _set=1)
earcrx_cmdc_heartbeat_cap_chng_i rq	The CAP_CHNG or CAP_CHNG_CONF status bits' handshake in Heartbeat transactions is completed successfully, after a software request for a Capabilities Data Structure information change notification (earcrx_cmdc_heartbeat_rxstat_set:earcrx_cmdc_heartbeat_rxstat_cap_chng _set=1)
earcrx_cmdc_rxpkt_badpreamble_ir q	A packet is received with a bad PREAMBLE bit sequence, and so the packet received incorrectly. This is an information interrupt and no software action needed
earcrx_cmdc_rxpkt_badsync_irq	A packet is received with a bad SYNC bit sequence, and so the packet received incorrectly. This is an information interrupt and no software action needed
earcrx_cmdc_rxpkt_incomplete_irq	A packet is received with too few bits, and so the packet received incorrectly. This is an information interrupt and no software action needed
earcrx_cmdc_rxpkt_badecc_irq	A packet is received with bit errors, and the ECC syndrome cannot be used to correct the errors. This is an information interrupt and no software action needed If the earcrx_cmdc_config:earcrx_cmdc_rxpkt_badecc_tolerant bit is set, the packet is received and the data is used within the transaction.
earcrx_cmdc_rxpkt_badpar_irq	A packet is received with the wrong parity bit value. This is an information interrupt and no software action needed. If the earcrx_cmdc_config: earcrx_cmdc_rxpkt_badpar_tolerant bit is set, the packet is received and the data is used within the transaction
earcrx_cmdc_xact_done_irq	A transaction is completed and the software must check the result in the earcrx_cmdc_info and earcrx_cmdc_status register
earcrx_cmdc_xact_read_data_irq	A read transaction is ongoing, and the received device ID and offset are valid. The software now

	writes the requested size and data into the respective earcrx_cmdc_xact_rd[X] register where X is from 0 to 64
earcrx_cmdc_heartbeat_earctxstat_ upd_irq	eARC RX CMDC - The contents of the EARC_TX_STAT register is updated after a successful Heartbeat transaction while in the Discovery state [eARC RX]
earcrx_cmdc_heartbeat_earcvalid0_ irq	eARC RX CMDC - The EARC_TX_STAT.EARC_VALID=0 is received while in the [RX eARC] state (active eARC operation), causing the Discovery FSM to jump to the [RX DISC1] state. This interrupt is only triggered if the earcrx_cmdc_dscvr_earcvalid0_to_disc1 field is 1

24.6.4.2 Differential Mode Audio Channel Programming Model

The operation of the eARC device in DMAC programming model are described in the following sections.

24.6.4.2.1 eARC RX DMAC PHY Interface Timing

The timing relations between the each events and the signals, followed by the expected timing from the controller and requirements for the PHY are shown in the Figure.

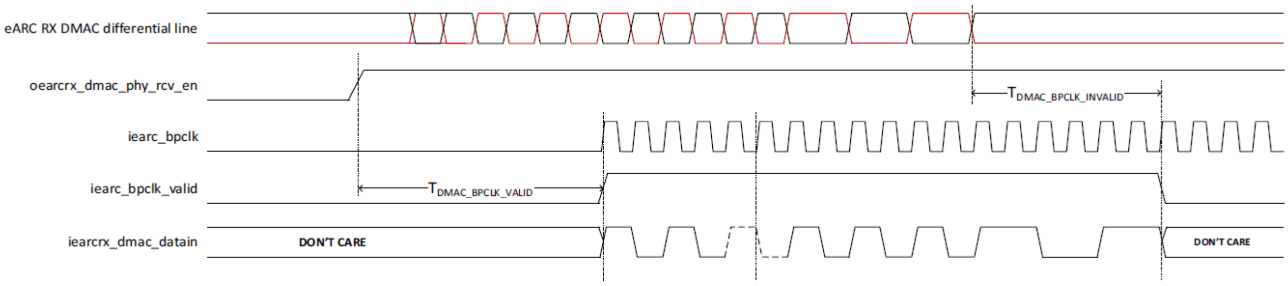

Fig. 24-6 eARC RX DMAC PHY Interface Timing

Table 24-9 eARC RX DMAC PHY Interface Timing Requirements

Timing	Description	Controller Event
TDMAC_BPCLK_VALID	The maximum time for the PHY DMAC receiver to be enabled and output biphase clock valid	NA
TDMAC BPCLK_INVALID	The time between no transitions coming on the eARC DMAC differential lines and the PHY notifying the eARC RX DMAC controller of the loss activity.	NA

24.6.4.2.2 eARC RX DMAC PHY Receiver Interface Description

The PHY receiver is enabled by the oearcrx_dmac_phy_rcv_en signal and is ready in TDMAC_BPCLK_VALID. The DMAC receiver on the PHY outputs the direct values from the line into iearcrx_dmac_datain signal, since the biphase decoding is done by the controller. The eARC RX DMAC PHY is configured in the earcrx_dmac_phy_config register.

24.6.4.2.3 Requirements

The eARC RX DMAC datapath is activated only after the eARC RX CMDC Discovery is completed successfully, and the Discovery state machine is in the [RX eARC] state. The software can verify if the eARC RX Discovery is completed successfully through the earcrx_0_int_status.earcrx_cmdc_discovery_done_irq interrupt; earcrx_cmdc_discovery_state=5 field of the earcrx_cmdc_status register (RX eARC).

24.6.4.2.4 Configuration

The eARC RX DMAC datapath and PHY are configured in the earcrx_dmac_config and earcrx_dmac_phy_config registers.

24.6.4.2.5 eARC RX DMAC Audio Reception

To start eARC RX audio reception the software must perform the following steps .

1. Enable the eARC RX PHY DMAC receiver by setting the earcrx_dmac_phy_rcv_en=1 field of the earcrx_dmac_phy_config register.

2. The software waits for the trigger of the following interrupts that indicate any activity in the eARC biphase clock iearc_bpclk, mainunit_0_int_status.earc_bpclk_off_chg_irq; mainunit_0_int_status.earc_bpclk_locked_chg_irq.
3. The software confirms that the eARC biphase clock is on and locked through the cmu_status.earc_bpclk_off_st=0 and cmu_status.earc_bpclk_locked_st=1 fields.
4. The software also confirms that the eARC biphase clock valid is through the mainunit_status0. earc_bpclk_valid_stable=1 field.
5. Enable the eARC RX DMAC audio datapath by setting the earcrx_dmac_en=1 field of the earcrx_dmac_control0 register.
6. The software waits for the earcrx_1_int_status. earcrx_dmac_chstatus_block_chg_irq interrupt, indicating the reception of a eARC audio Channel Status block.
7. The software reads the eARC audio Channel Status block received through the earcrx_dmac_chstatusX registers (where X is from 0 to 5) and analyzes their content (e.g. audio format, layout, channel allocation, and so on and so forth).
8. Configure the eARC RX DMAC audio channel enable using the earcrx_dmac_channel_alloc[31:0] field of the earcrx_dmac_control1 register for up to 32-channels (for example, bit 0: channel 1, and bit 31: channel 32).
9. Configure the eARC RX DMAC audio output interface using the earcrx_dmac_config register. Parallel Audio Output (up to 32 channels)-earcrx_dmac_config. earcrx_dmac_pao_en; S/PDIF IF (up to 8 channels)-earcrx_dmac_config.earcrx_dmac_sao_spdif_en; I2S IF (up to 8 channels) - earcrx_dmac_config.earcrx_dmac_sao_i2s_en.
10. Configure the IEC 60958-3 Channel Status information to be transmitted by the eARC RX audio output interfaces (PAO and SAO) through the earcrx_dmac_chstatus_streamer Y registers (where Y is from 0 to 14).
11. Configure the IEC 60958-3 user data information to be transmitted by the eARC RX audio output interfaces (SAO) through the earcrx_dmac_usrdata_streamer0 register.
12. Enable the eARC RX DMAC audio output interfaces by asserting the earctx_dmac_control0. earcrx_dmac_audio_en=1 field.

24.6.4.2.6 eARC DMAC Interrupts

During the eARC RX DMAC operation the interrupts from the earcrx_1_int_status, earcrx_intvec_index register can be triggered as shown in the table.

Table 24-10 eARC DMAC Interrupt

Interrupts	Functionality
earcrx_dmac_bprxsampler_parity_err_irq	Triggered when there is a eARC RX DMAC biphase-mark decoder IEC 60958 frame parity error in the received audio stream
earcrx_dmac_chstatus_block_chg_irq	Triggered when the eARC RX Channel Status block payload changes. Channel Status block is updated when every preamble B marker received (beginning of an IEC 60958 block)
earcrx_dmac_audio_type_chg_irq	eARC RX audio type status change interrupt. This interrupt is triggered whenever the earcrx_dmac_audio_type_st field changes state (regardless of the override enable)
earcrx_dmac_audio_mute_chg_irq	eARC RX audio MUTE status change interrupt. This interrupt is triggered whenever the earcrx_dmac_audio_mute_st field changes state (regardless of the override enable)
earcrx_dmac_ecc_rx_check_uncerr_irq	eARC RX DMAC uncorrectable errors in the received compressed audio
earcrx_dmac_usrdata_msg_hdmi_acp_chg_irq	eARC RX DMAC user data H14b ACP message payload change
earcrx_dmac_usrdata_msg_hdmi_isrc1_chg_irq	eARC RX DMAC user data H14b ISRC1 message payload change
earcrx_dmac_usrdata_msg_hdmi_isrc2_chg_irq	eARC RX DMAC user data H14b ISRC2 message payload change

earcrx_dmac_usrdata_msg_generic_chg_irq	eARC RX DMAC user data generic message payload change

Chapter 25 HDMI RX Controller

25.1 Overview

HDMIRX is fully compliant with HDMI1.4b and 2.0 specification. It offers a simple implementation for consumer electronics like DVD/player/recorder and camcorder. HDMIRX consists of one HDMI receiver controller and one HDMI receiver PHY.
HDMIRX supports the following features:

- Video formats:
  - HDMI 1.4b video formats
    - All CEA-861-E video formats up to 1080p@120Hz
    - HDMI 1.4b 4K x 2K video formats(3840x2160p@24Hz/25Hz/30Hz and 4096x2160p@24Hz)
    - HDMI 1.4b 3D video modes with up to 340 MHz (TMDS clock)
  - HDMI2.0 video formats
    - TMDS Scrambler to enable support for 2160p@60 Hz with RGB/YCbCr4:4:4 or YCbCr4:2:2
    - Supports YCbCr 4:2:0 to enable 2160p@60Hz at lower HDMI link speeds
- Colorimetry, 24-bit RGB 4:4:4, 24-bit YCbCr 4:4:4, 24/30-bit YCbCr 4:2:0, 24/30-bit YCbCr 4:2:2
- Pixel clock from 25 MHz up to 600 MHz
- Up to 192 kHz IEC60958 audio sampling rate
- S/PDIF 2channel output
- I2S 2/4/6/8channel output
- AMBA APB 3.0 register access
- SCDC I2C DDC access
- TMDS Scrambler to enable support for 2160p@60Hz with RGB/YCbCr 4:4:4
- Integrated CEC hardware engine
- Integrated HDCP1.4 key configuration
- Integrated E-EDID configuration
- AXI write DMA into DDR
  - Supports 64bit AXI bus width with 500M frequency
  - Burst8 alignment with the last burst length variable
  - Y and UV different store address
  - Supports virtual width

25.2 Block Diagram

HDMI_RX_WRAPPER: has two main sub_block: HDMI_QP_RX and HDMI_RX_DMA.
HDMIRXPHY lane3 is clock lane. Iextphy_tmdsdata0/iextphy_tmdsdata1/iextphy_tmdsdata2 just has low 40 valid bit, and it is corresponding to quad pixel rate. And itmdsqpclk is the 1/4 tmdsclk which corresponds to normal single pixel rate, for example, if the resolution is 1080p@60p, itmdsqpclk is 37.125M.

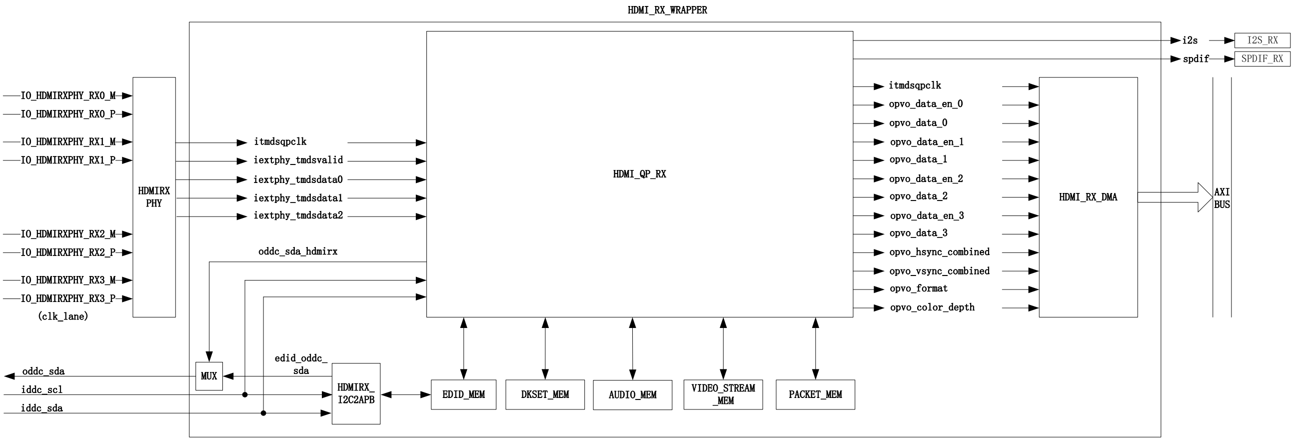

Fig. 25-1 HDMI_RX_WRAPPER Diagram

HDMI_QP_RX's block diagram is shown below.

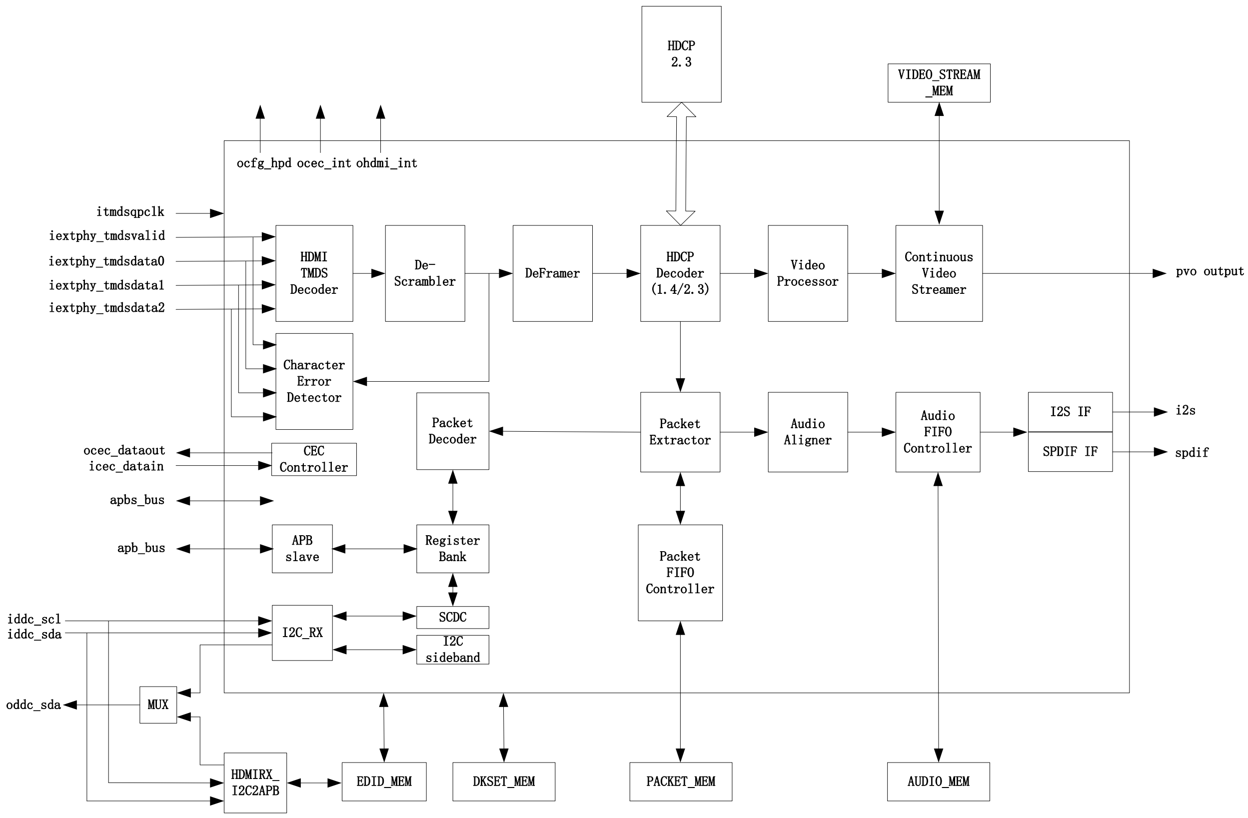

Fig. 25-2 HDMI_QP_RX Diagram

HDMI_RX_DMA's block diagram is shown below.

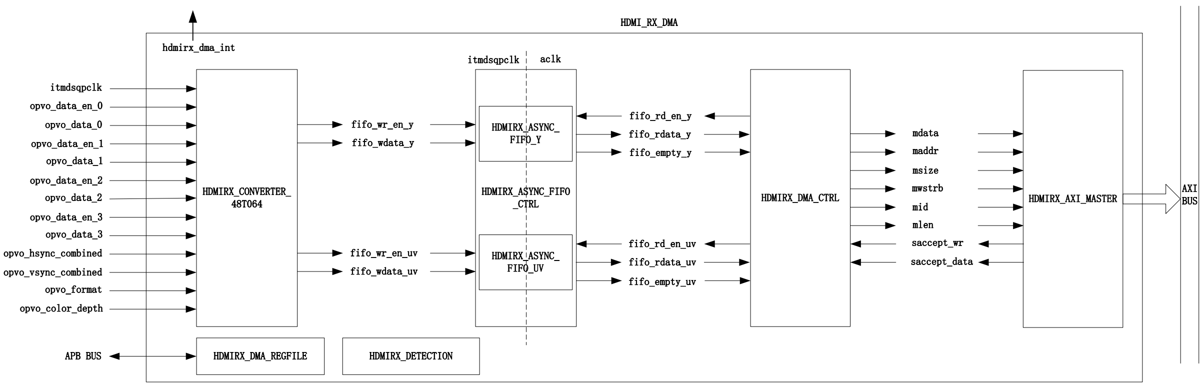

Fig. 25-3 HDMI_RX_DMA Diagram

25.3 Function Description

HDMIRX has two main sub-block: HDMI_QP_RX and HDMI_RX_DMA. HDMI_QP_RX receives three data channel lane, every data channel has 40bit valid data bit. HDMI_QP_RX video stream output quad data one cycle. And HDMI_RX_DMA will transform different data format into 64bit valid write data, and store them in the DDR through AXI bus with hdmirx_dma_ctrl.

25.3.1 HDMI TMDS Decoder

The HDMI TMDS Decoder module preforms TMDS decoding for each physical channel received from the PHY. In every itmdsqpclk cycle, input is four data buses, every data bus is 30bit with three physical channels. On each channel, data is received as 10bit TMDS symbols and decoded into either 8-bit video data, 4-bit Data Island data, or 2-bit Control Period data. The output is quad pixel rate with four parallel data stream. The input 40bit data is shown in diagram below.

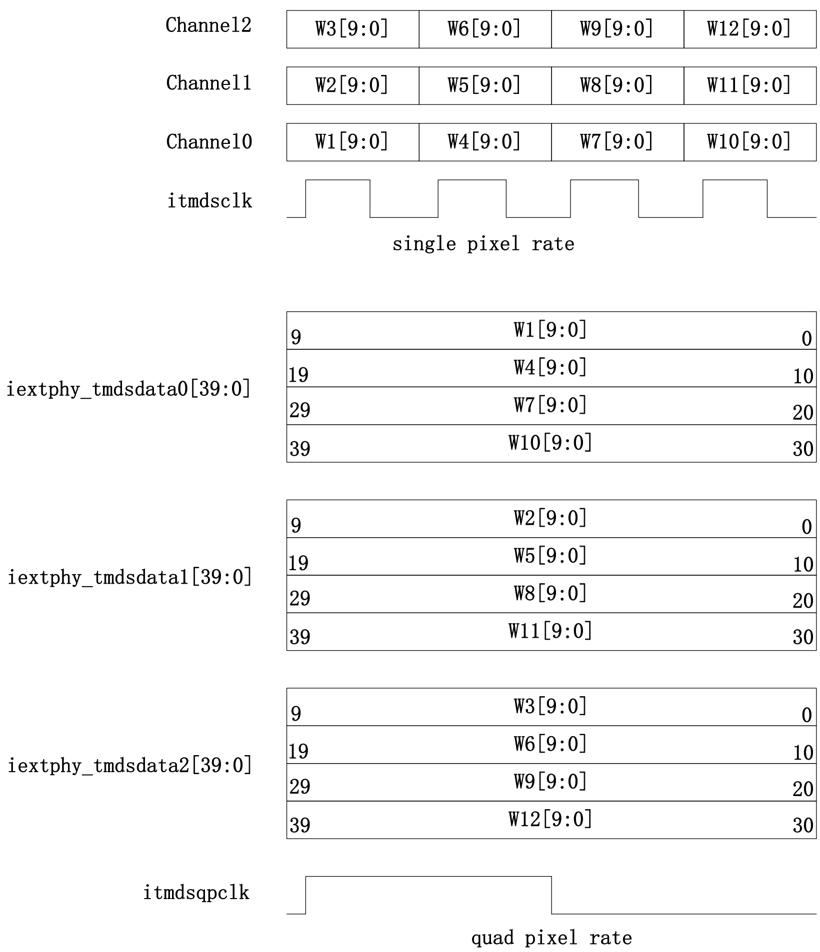

Fig. 25-4 HDMIRX input quad pixel rate Diagram

25.3.2 De-Scrambler

This module removes scrambling from source’s scrambled data. When the controller is operating in DVI, HDMI1.4b modes, this module behaves transparently.

25.3.3 Character Error Detection

This module provides a mechanism for the Sink side device to count and report(through SCDC channel) the Character Error number which it has detected. The Source uses this result to check the link quality by sampling the error counters at periodic intervals. The HDMI receiver implements character error detection, together with a character error counter for channel0, 1,
and 2. The receiver checks each incoming character as to whether it is valid in context. If the character is not valid, then the receiver increments a character error counter associated with each channel. If this character error counter is less than the threshold, this module will

output one important signal hdmirx_lock, this signal will be set 1'b1 to indicate that HDMIRX can output for hdmi_rx_dma module and the output data is valid data.

25.3.4 DeFramer

This module receives the HDMI data from the De-Scrambler and interprets its content. It extracts the Video and Data Island Data Enable from the data stream. Additionally, the block implements a glitch/spike filtering on Vertical and Horizontal Sync, the Guard Band, Preamble, Data Period, Video Period detection, and a Vertical Sync remap filtering.

25.3.5 HDCP Decoder

This module allows HDCP to decrypt the received content. It is capable of receiving any required key set using an external memory. The HDCP Decoder handles the data from the HDCP 1.4 engine and external HDCP2.3 engine, according to the incoming I2C Slave traffic.

25.3.6 Video Processor

This module is composed of the deep-color mode ungrouping, pixel de-repeater, video remapping, and video field detection functions. It assembles video data from the HDMI data stream in normal and deep color mode at any given HDMI specified format and representation.

If a Set-AVMUTE command is received from the HDMITX through the general control packet(GCP) for an automatic mute, you can program the mute value per component channel to allow usage across all color spaces. A manual force mode is also available to either control a video path mute through software or to test the subsequent connections.

25.3.7 Continuous Video Streamer

This module assembles a continuous video stream of only valid pixels during the video active period. This block also ensures video data period always begins in the bus0(opvo_data_0). The first line in the output, after a change in the video mode, can be ignored. The first line is used to measure video dimension parameters, necessary to generate output correctly as a continuous video stream in the subsequent lines. The Continuous Video Streamer uses an external memory to buffer the necessary video data in such a way that once the video output is enabled, there are enough buffered pixels to compensate for the subsequent invalid ones. This memory can store one 4k(4096) pixel line.

25.3.8 Packet Extractor

This module performs BCH decoding over received Data Island packets, establishing the Error Correction Code(ECC) feature. The generator polynomial related to this feature is defined in the HDMI specification and allows for one of the following configurable approaches over each BCH block:

- Correction of 1-bit error plus detection of 2-bits error
- Detection without correction of 1-bit error, 2-bits error and any odd n-bit error

Based on the ECC, the Packet Extractor provides filter configurability to discard packets that can't be corrected by the algorithm. Additionally, it calculates the Checksum of InfoFrame packets, and provides filter configurability to discard InfoFrames with errors detected through the Checksum.

Non-audio packets where errors are detected(but not corrected) can be discarded, depending on filter configuration. Audio packets are never discarded, regardless of error detection.

25.3.9 Packet Decoder

This module identifies Data Island packets extracted from HDMI link(TMDS) and separates them by Packet Type, redirecting their contents for storage in the Register Bank while also extracting the required information to control other blocks in the controller. The following packets are stored in a dedicated register set for direct software access.

Table 25-1 Packet type Mapping

Packet name	Packet Type value
Audio Clock Regeneration Packet(ACR)	0x01
General Control Packet(GCP)	0x03
Audio Content Protection Packet(ACP)	0x04
ISRC1 Packet	0x05
ISRC2 Packet	0x06
Gamut Metedata Packet(GMP)	0x0a

Audio Metedata Packet(AMP)	0x0d
Extended Metedata Packet(EMP)	0x7f
Vendor Specific InfoFrame Packet	0x81
Auxiliary Video Information InfoFrame Packet(AVI)	0x82
Source Product Description InfoFrame Packet	0x83
Audio InfoFrame Packet	0x84
NTSC VBI InfoFrame Packet	0x86
Dynamic Range and Mastering InfoFrame Packet(DRM)	0x87

When one of the dedicated packet registers changes value, the corresponding pkt_0_int_status. pktdec_*_chg_irq interrupt is triggered. Software must perform post-processing of the packet.

The registers that store the HDMI link packets have a snapshot feature that guarantees the data consistency during an APB read operation. This read operation starts in the lowest address of the corresponding packet. In this way, a snapshot of the packet being read is captured correctly and the APB read operation always returns consistent data. This flow is valid only when the pktdec_snapshot_bypass field is not enabled(set to 1'b0). Otherwise, there is no guaranteed consistency on the packets register when their contents are updated during the APB read operation.

25.3.10 Packet FIFO Controller

This module contains the logic to control the storage, by order of arrival, of non-audio type Data Island Packets through an external memory interface. This feature helps to reduce load from the application processor software, lowering real-time requirements of the system. The software is able to configure between free storing of every received packet or storing optional packets by individual packet type selection. The external packet memory is 448x64 size. Every packet type data will be stored in 4 memory 64bit unit.

ADDR	63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0
N	PB3 (SP0.3)	PB2 (SP0.2)	PB1 (SP0.1)	PB0 (SP0.0)	RSVD	PH2	PH1	PH0
N+1	PB11 (SP1.4)	PB10 (SP1.3)	PB9 (SP1.2)	PB8 (SP1.1)	PB7 (SP1.0)	PB6 (SP0.6)	PB5 (SP0.5)	PB4 (SP0.4)
N+2	PB19 (SP2.5)	PB18 (SP2.4)	PB17 (SP2.3)	PB16 (SP2.2)	PB15 (SP2.1)	PB14 (SP2.0)	PB13 (SP1.6)	PB12 (SP1.5)
N+3	PB27 (SP3.6)	PB26 (SP3.5)	PB25 (SP3.4)	PB24 (SP3.3)	PB23 (SP3.2)	PB22 (SP3.1)	PB21 (SP3.0)	PB20 (SP2.6)

PH:Packet Header PB:Packet Body SP:SubPacket

Fig. 25-5 Packet FIFO Storage Layout

25.3.11 Audio Aligner

Audio packets received from the Packet Extractor are aligned to be stored in an external audio FIFO. The audio format detection and audio channel status extraction are also implemented in this block. The audio channel status extraction to the register bank relies on the B.X bit, which indicates the start of a new block of 192 frames. If the B.X bit does not align with the 192 frames, the channel status will not be sampled into the register bank. Two audio interfaces are provided: I2S(2ch/4ch/6ch/8ch) and S/PDIF(2ch).

25.3.12 Audio FIFO Controller

The Audio FIFO Controller will control the audio packet write/read operation corresponding to the configuration. The audio memory is 896x60 size.

25.3.13 HDMIRX_CONVERTER_48TO64

This module converts different format to 64bit valid data. This module supports different format below.

Table 25-2 Store format

Input format	Store format
RGB888	RGB888

	ARGB8888/RGBA8888
YCbCr420_8bit	YCbCr420_8bit
YCbCr422_8bit	YCbCr422_8bit
YCbCr444_8bit	YCbCr444_8bit
YCbCr420_10bit	YCbCr420_10bit
	YCbCr420_16bit_align
YCbCr422_10bit	YCbCr422_10bit
	YCbCr422_16bit_align

In HDMI1.4 spec, YCbCr422 8/10/12bit are all transfered in 12bit mode. The different input format is shown below.

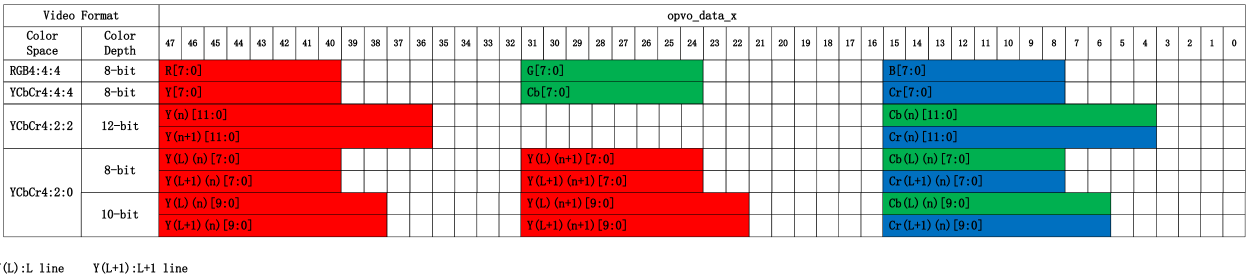

Fig. 25-6 HDMIRX input format map

(1)RGB888

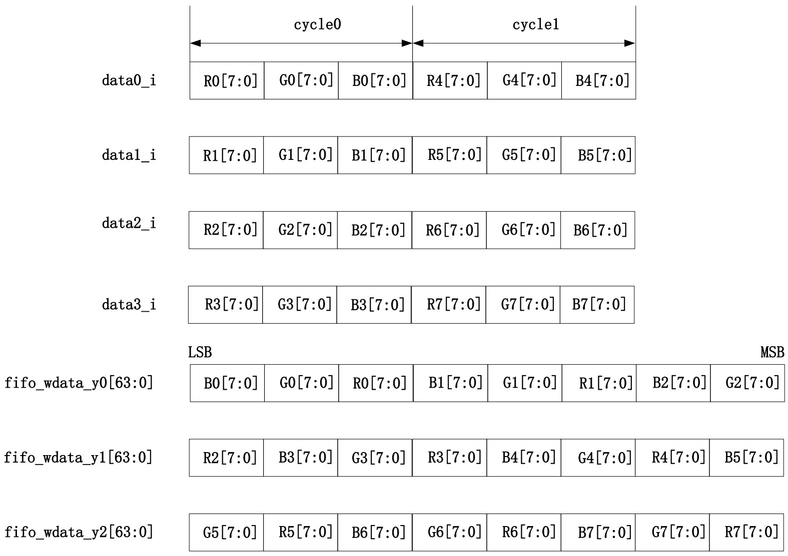

Fig. 25-7 RGB888 storage map

(2) ARGB8888/RGBA888

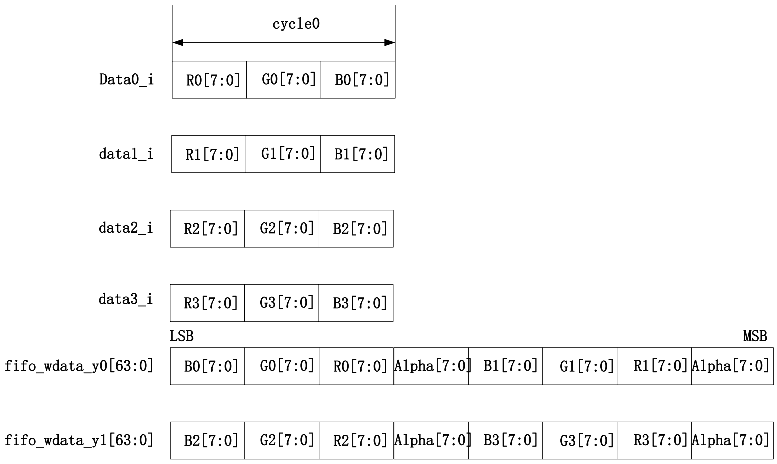

Fig. 25-8 ARGB8888 storage map

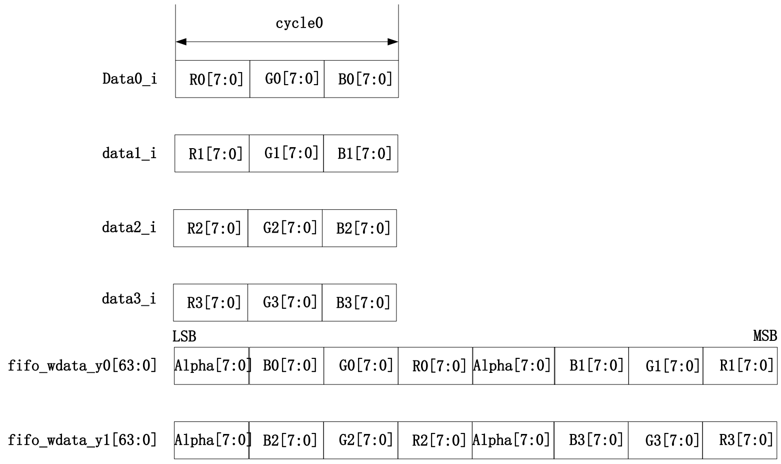

Fig. 25-9 RGBA8888 storage map

(3)YCbCr420_8bit

Odd line just store Y component, and Cb component will be stored in the Cb line buffer, and Cb will be read in the next line(even line).

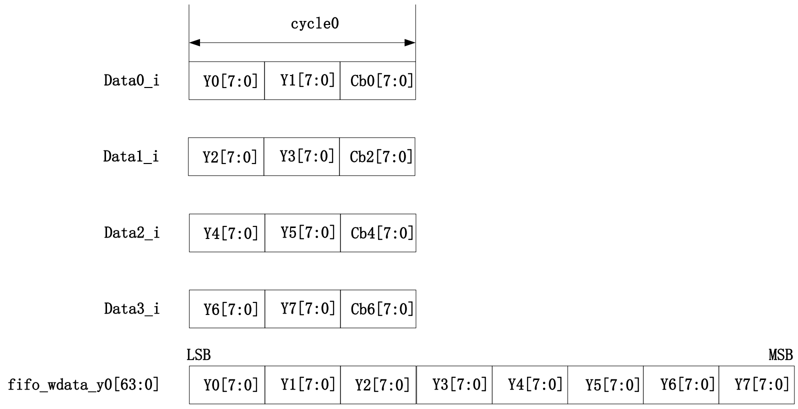

Fig. 25-10 YCbCr420_8bit odd line storage map

Even line will store Y and CbCr component.

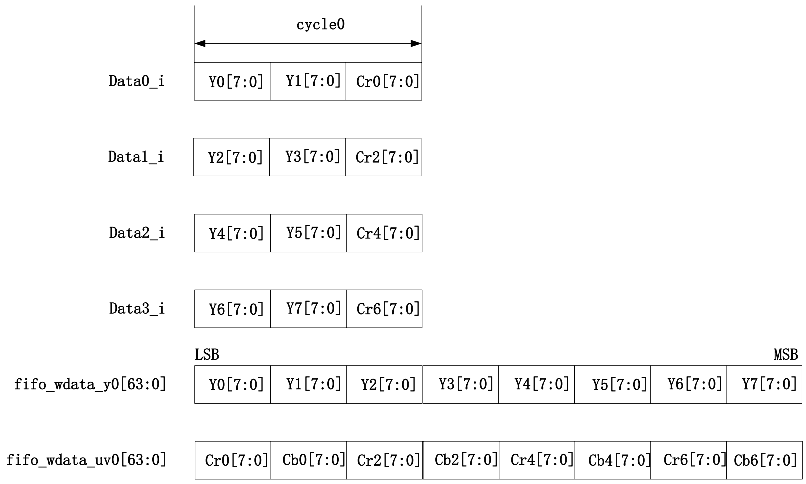

Fig. 25-11 YCbCr420_8bit even line storage map

(4)YCbCr422_8bit

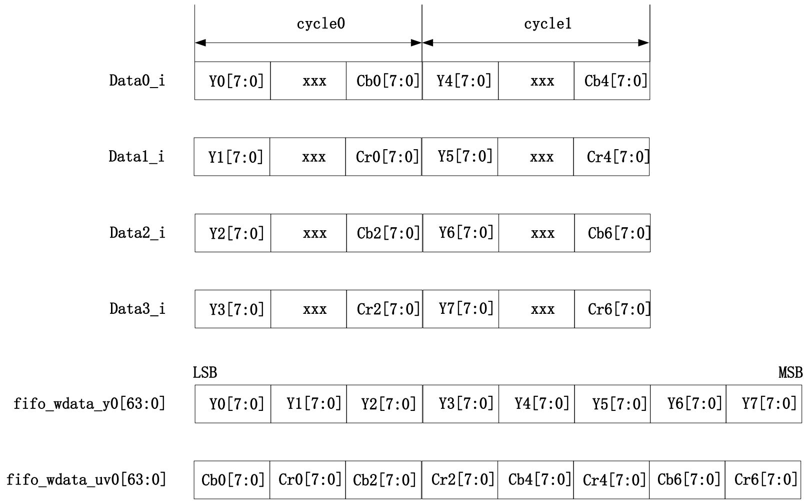

Fig. 25-12 YCbCr422_8bit storage map

(5)YCbCr444_8bit

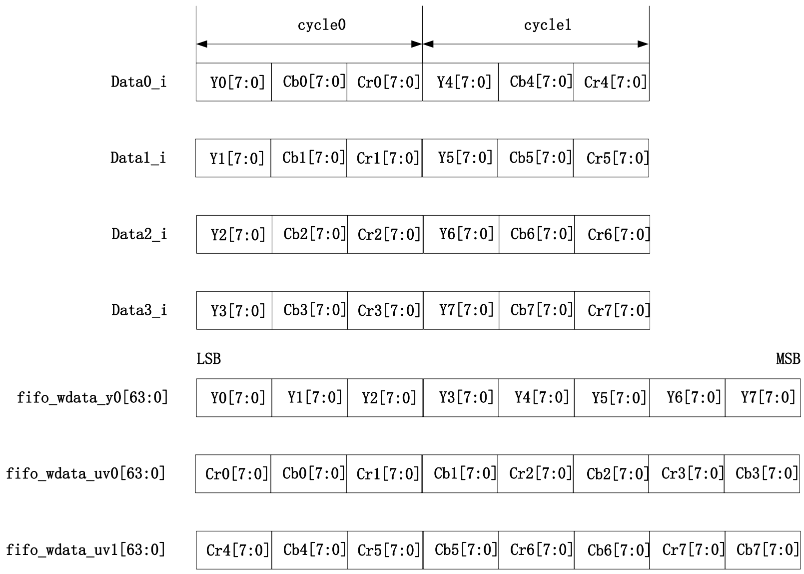

Fig. 25-13 YCbCr444_8bit storage map

(6)YCbCr420_10bit

Odd line just store Y component, and Cb component will be stored in the Cb line buffer, and Cb will be read in the next line(even line).

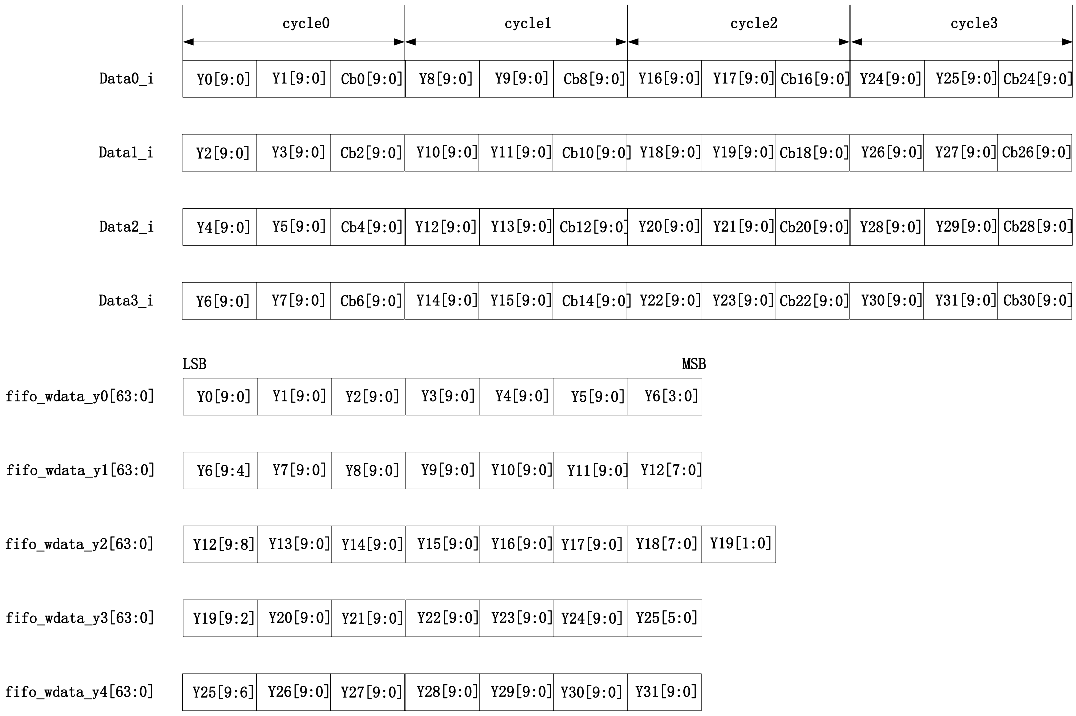

Fig. 25-14 YCbCr420_10bit odd line storage map

Even line will store Y and CbCr component.

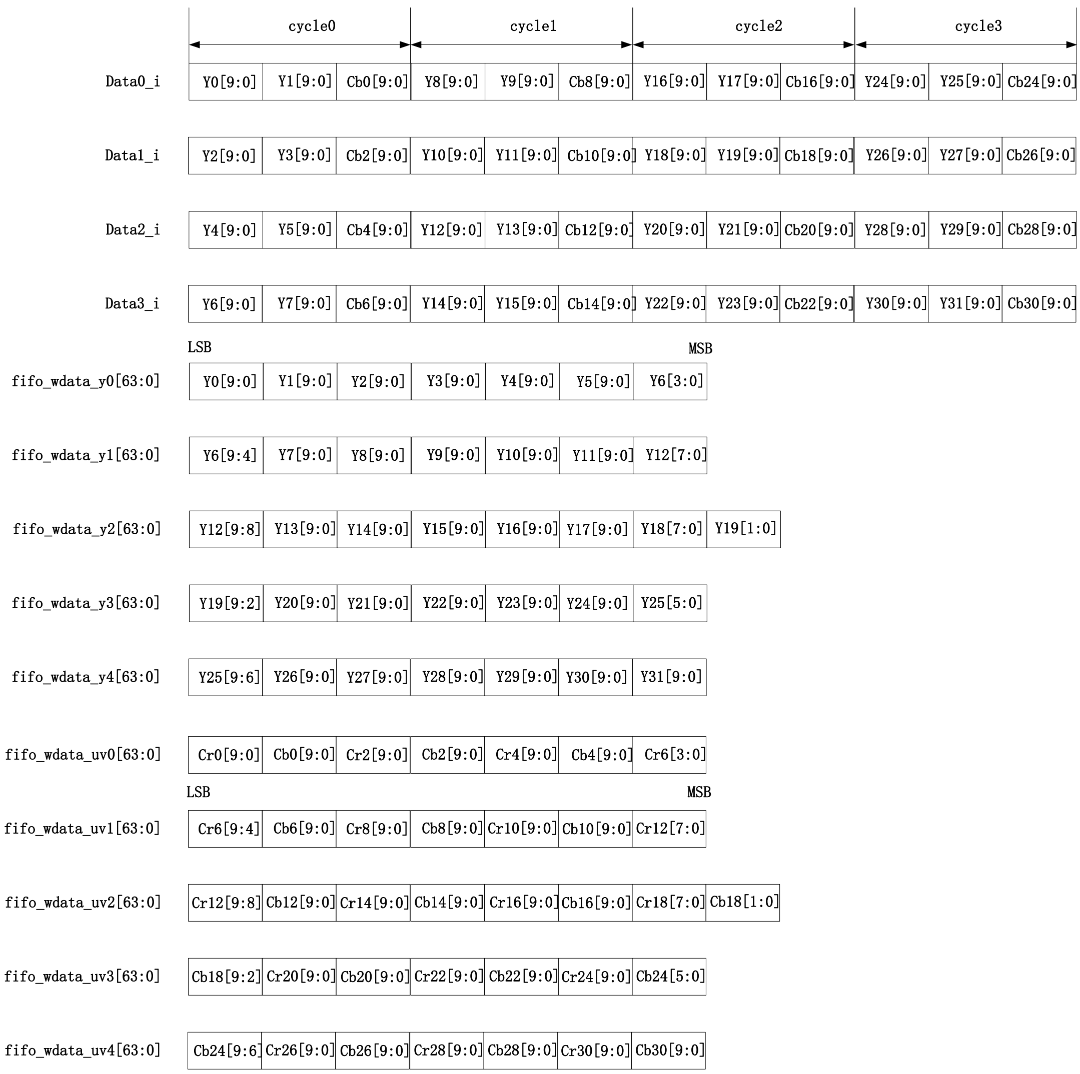

Fig. 25-15 YCbCr420_10bit even line storage map

(7)YCbCr420_16bit_align

Odd line just store Y component, and Cb component will be stored in the Cb line buffer, and Cb will be read in the next line(even line). Y10/CbCr10 can be padded 6bit dummy data in MSB or LSB, it is configurable.

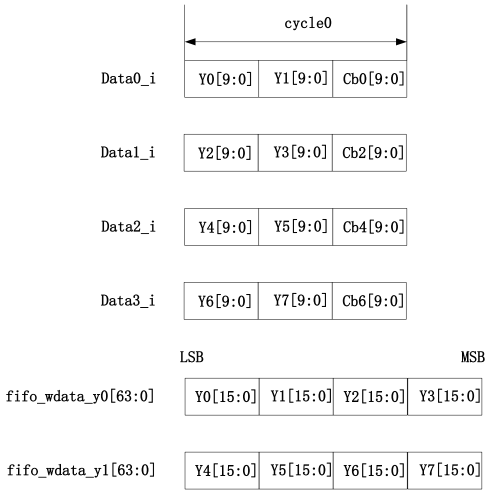

Fig. 25-16 YCbCr420_16bit_align odd line storage map

Even line will store Y and CbCr component.

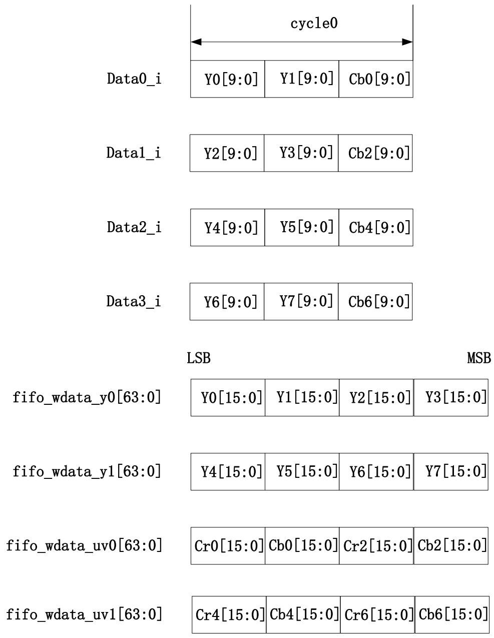

Fig. 25-17 YCbCr420_16bit_align even line storage map

(8)YCbCr422_10bit

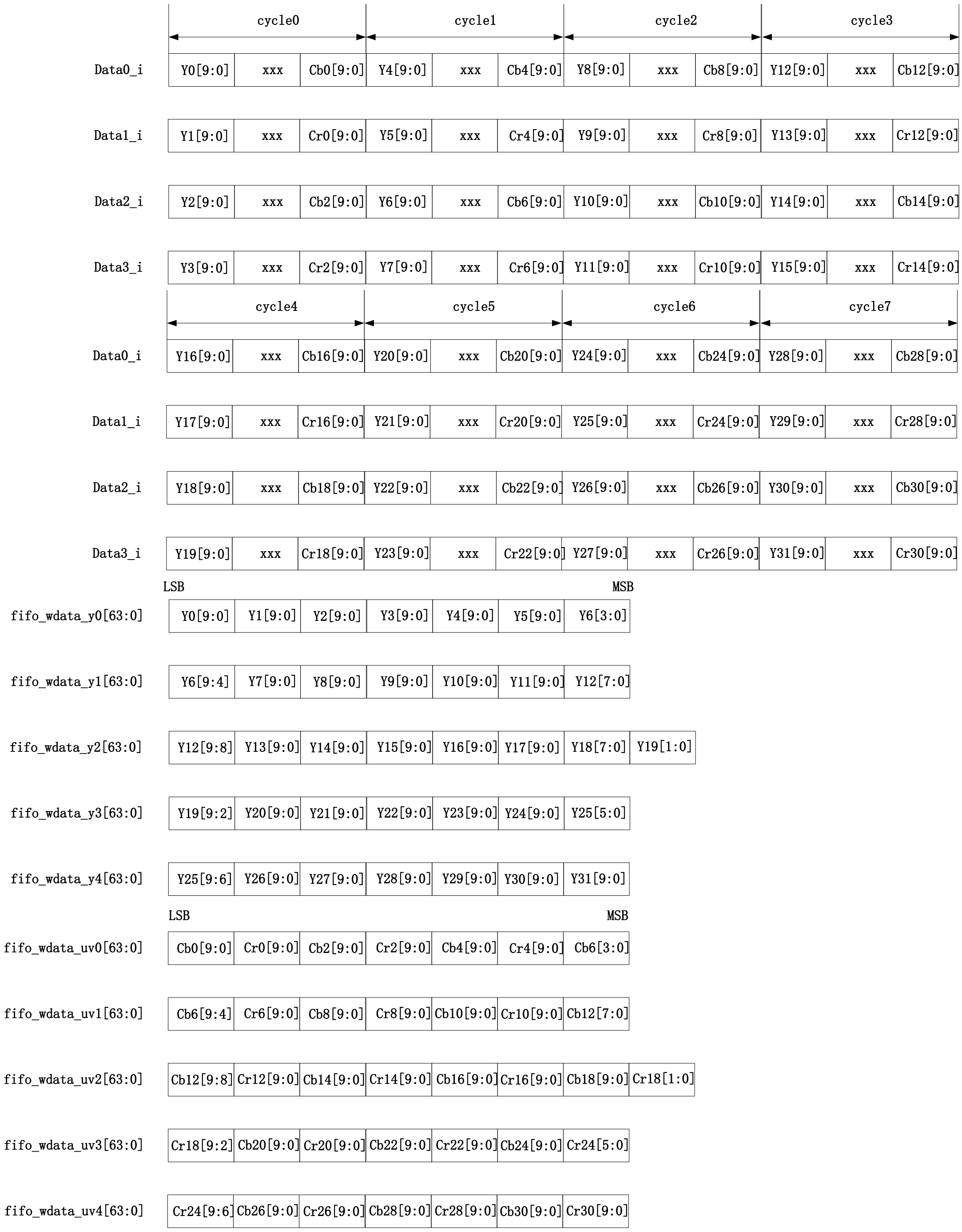

Fig. 25-18 YCbCr422_10bit storage map

(9) YCbCr422_16bit_align

Y10/CbCr10 can be padded 6bit dummy data in MSB or LSB, it is configurable.

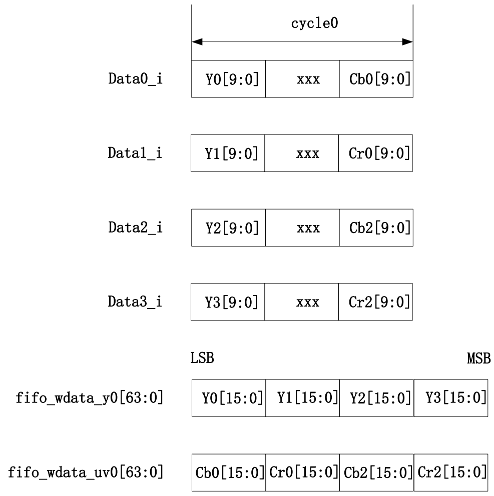

Fig. 25-19 YCbCr422_16bit_align storage map

25.3.14 HDMIRX_ASYNC_FIFO_CTRL

This module controls the HDMIRX asynchronous FIFO logic. Y_FIFO memory is 1024x64 size, UV_FIFO memory is 2048x64 size, it is enough for one 4k pixel line(max resolution 4096 pixel).

25.3.15 HDMIRX_DMA_CTRL

This module controls the HDMIRX AXI DMA awaddr/wdata logic. If input data stream is enough for burst8, and the hdmirx_dma_ctrl will send one burst8 command, and follow the wdata. Y component is priori to UV component, and they are send by polling mechanism.

25.4 Register Description

25.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

25.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CORE_ID	0x0000	W	0x00000000	Core Identification Register
VER_NUMBER	0x0004	W	0x00000000	IP Version Number Register
VER_TYPE	0x0008	W	0x00000000	IP Version Type Register
CONFIG_REG	0x000C	W	0x00000000	Core Configuration Identification Register
CORE_TIMESTAMP_HHMM	0x0014	W	0x00000000	Core Timestamp HHMM Register
CORE_TIMESTAMP_MMDD	0x0018	W	0x00000000	Core Timestamp MMDD Register
CORE_TIMESTAMP_YYYY	0x001C	W	0x00000000	Core Timestamp YYYY Register
GLOBAL_SWRESET_REQUEST	0x0020	W	0x00000000	Main Controller Software Reset Register
GLOBAL_SWENABLE	0x0024	W	0x00213F01	Main Controller Synchronous Enable Register
GLOBAL_TIMER_REF_BASE	0x0028	W	0x00000000	Timer Base ALU Register

Name	Offset	Size	Reset Value	Description
PMU_POWER_REQUEST	0x0040	W	0x00000000	PMU Power Up and Down Request Register
PMU_POWER_STATUS	0x0044	W	0x00001001	PMU Power and isolation Status Register
PMU_POWER_CONFIG	0x0048	W	0x00000000	PMU Configuration Register
CORE_CONFIG	0x0050	W	0x00000000	Core Configuration Register
CMU_CONFIG0	0x0060	W	0x00010001	CMU Configuration Register0
CMU_CONFIG3	0x006C	W	0x00000001	CMU Configuration Register3
CMU_CONFIG5	0x0074	W	0x00000001	CMU Configuration Register5
CMU_STATUS	0x007C	W	0x00000000	CMU Status Register
CMU_AUDCLK_FREQ	0x0080	W	0x00000000	Audio Clock Frequency Register
CMU_TMDSQPCLK_FREQ	0x0084	W	0x00000000	TMDS QP Clock Frequency Register
CMU_CR_PARA_CLK_FREQ	0x00AC	W	0x00000000	CR_PARA Clock Frequency Register
CMU_MAIN_CONFIG	0x00BC	W	0x00000001	CMU Main Configuration Register
PHY_CONFIG	0x00C0	W	0x00000103	PHY Configuration Register
PHY_STATUS	0x00C8	W	0x00000000	PHY_Status Register
PHY_JTAG_CONFIG	0x00CC	W	0x00000000	PHY Configuration JTAG Interface - Configuration Register
PHY_JTAG_TAP_TCLK	0x00D0	W	0x00000000	PHY configuration JTAG interface - Clock Control
PHY_JTAG_TAP_IN	0x00D4	W	0x00000000	PHY configuration JTAG interface - Tap IN to PHY
PHY_JTAG_TAP_OUT	0x00D8	W	0x00000000	PHY configuration JTAG interface - Tap Out from PHY
PHYCREG_CONFIG0	0x00E0	W	0x00000000	PHY CREG Configuration Register 0
PHYCREG_CONFIG1	0x00E4	W	0x00000000	PHY CREG Configuration Register 1
PHYCREG_CONFIG2	0x00E8	W	0x00000000	PHY CREG Configuration Register 2
PHYCREG_CONFIG3	0x00EC	W	0x00000000	PHY CREG Configuration Register 3
PHYCREG_CONTROL	0x00F0	W	0x00000000	PHY CREG Control Register
PHYCREG_STATUS	0x00F4	W	0x00000000	PHY CREG Status Register
PHYCREG_CONFIG4	0x00F8	W	0x00000100	PHY CREG Configuration Register 4
MAINUNIT_STATUS	0x0150	W	0x00000000	Main Unit Status
I2C_SLAVE_CONFIG0	0x0160	W	0x00050000	I2C Slave Configuration Register 0
I2C_SLAVE_CONFIG1	0x0164	W	0x00000000	I2C Slave Configuration Register 1

Name	Offset	Size	Reset Value	Description
DESCRAND_EN_CONTROL	0x0210	W	0x00000100	Descrambler Enable Control Register
DESCRAND_SYNC_CONTROL	0x0214	W	0x00000000	Descrambler Synchronization Control Register
DESCRAND_STATUS	0x0218	W	0x00000000	Descrambler Status Register
DESCRAND_SYNC_SEQ_CONFIG	0x022C	W	0x00000041	Descrambler Sync Sequence Error Threshold Control
DESCRAND_SYNC_SEQ_CLEAR	0x0230	W	0x00000000	Descrambler Sync Sequence Error Counter Clear Register
DESCRAND_SYNC_SEQ_STATUS	0x0234	W	0x00000000	Descrambler Sync Sequence Error Counter Status Register
DEFRAMER_CONFIG0	0x0270	W	0x00000000	De-Framer Configuration Register 0
DEFRAMER_CONFIG1	0x0274	W	0x021000F8	De-Framer Configuration Register 1
DEFRAMER_VSYNC_CNT_CLEAR	0x0278	W	0x00000000	De-Framer Vsync Counter Clear Register
DEFRAMER_STATUS	0x027C	W	0x00000000	De-Framer status Register
HDCP14_CONFIG	0x0290	W	0x000E0700	HDCP 1.4 Configuration Register
HDCP14_WOO_CONFIG	0x0294	W	0x021401FC	HDCP 1.4 WOO Configuration Register
HDCP14_KEY_H	0x02A4	W	0x00000000	HDCP 1.4 Key High Configuration Register
HDCP14_KEY_L	0x02A8	W	0x00000000	HDCP 1.4 Key Low Configuration Register
HDCP14_KEY_STATUS	0x02AC	W	0x00000000	HDCP 1.4 Key Status
HDCP14_BKSV_H	0x02B0	W	0x00000000	HDCP 1.4 BKSV High Configuration Register
HDCP14_BKSV_L	0x02B4	W	0x00000000	HDCP 1.4 BKSV Low Configuration Register
HDCP14_STATUS	0x02B8	W	0x00000000	HDCP 1.4 Status
HDCP14_BSTATUS	0x02BC	W	0x00000000	HDCP 1.4 Bstatus Configuration Register
HDCP14_DDC_STATUS0	0x02C0	W	0x00000000	HDCP 1.4 DDC Status Register 0
HDCP14_DDC_STATUS1	0x02C4	W	0x00000000	HDCP 1.4 DDC Status Register 1
HDCP14_DDC_STATUS2	0x02C8	W	0x00000000	HDCP 1.4 DDC Status Register 2
HDCP14_DDC_STATUS3	0x02CC	W	0x00000000	HDCP 1.4 DDC Status Register 3
HDCP14_DDC_STATUS4	0x02D0	W	0x00000000	HDCP 1.4 DDC Status Register 4
HDCP14_RPT_KSV_H	0x02D4	W	0x00000000	HDCP 1.4 Repeater KSV High Configuration Register
HDCP14_RPT_KSV_L	0x02D8	W	0x00000000	HDCP 1.4 Repeater KSV Low Configuration Register

Name	Offset	Size	Reset Value	Description
HDCP14_RPT_CONTROL	0x02DC	W	0x00000000	HDCP 1.4 Repeater Control Register
HDCP14_RPT_KSVFIFO	0x02E0	W	0x00000000	HDCP 1.4 Repeater KSV Index Register
HDCP14_RPT_STATUS	0x02E4	W	0x00000000	HDCP 1.4 Repeater Status Register
HDCP2_CONFIG	0x02F0	W	0x00001000	HDCP 2 Configuration Register
HDCP2_STATUS	0x02F4	W	0x00000000	HDCP 2 Status Register
HDCP2_ESM_GLOBAL_GPIO_IN	0x02F8	W	0x00000000	HDCP2 ESM - Global GPIO interface - Inputs to ESM
HDCP2_ESM_GLOBAL_GPIO_OUT	0x02FC	W	0x00000000	HDCP2 ESM - Global GPIO interface - Outputs from ESM
HDCP2_ESM_P0_GPIO_IN	0x0300	W	0x00000000	HDCP2 ESM - Port 0 GPIO interface - Inputs to ESM
HDCP2_ESM_P0_GPIO_OUT	0x0304	W	0x00000000	HDCP2 ESM - Port 0 GPIO interface - Outputs from ESM
VIDEO_SYNCGEN_CONFIG6	0x03D0	W	0x00000001	Video Synchronism Generation Configuration Register 6
VIDEO_SYNCGEN_CONFIG7	0x03D4	W	0x000000FC	Video Synchronism Generation Configuration Register 7
VIDEO_SYNCGEN_CONTROL	0x03E0	W	0x00000000	Video Synchronism Generation Control Register
VIDEO_SYNCGEN_STATUS1	0x03F0	W	0x00000000	Video Synchronism Generation Status Register 1
VIDEO_SYNCGEN_STATUS2	0x03F4	W	0x00000000	Video Synchronism Generation Status Register 2
VIDEO_SYNCGEN_STATUS3	0x03F8	W	0x00000000	Video Synchronism Generation Status Register 3
VIDEO_SYNCGEN_STATUS4	0x03FC	W	0x00000000	Video Synchronism Generation Status Register 4
VIDEO_SYNCGEN_STATUS5	0x0400	W	0x00000000	Video Synchronism Generation Status Register 5
VIDEO_SYNCGEN_STATUS6	0x0404	W	0x00000000	Video Synchronism Generation Status Register 6
VIDEO_SYNCGEN_STATUS7	0x0408	W	0x00000000	Video Synchronism Generation Status Register 7
VIDEO_SYNCGEN_STATUS8	0x040C	W	0x00000000	Video Synchronism Generation Status Register 8
VIDEO_SYNCGEN_STATUS9	0x0410	W	0x00000000	Video Synchronism Generation Status Register 9
VIDEO_CD_CONFIG	0x0420	W	0x00005040	Video Processor Color Depth Configuration Register

Name	Offset	Size	Reset Value	Description
VIDEO_PP_CONFIG	0x0424	W	0x00050000	Video Processor Packing Phase Configuration Register
VIDEO_CONFIG1	0x0428	W	0x00000000	Video Processor Configuration Register 1
VIDEO_CONFIG2	0x042C	W	0x00000000	Video Processor Configuration Register 2
VIDEO_MUTE_VALUE_H	0x0430	W	0x00000000	Video Processor Mute High Value Register
VIDEO_MUTE_VALUE_L	0x0434	W	0x00000000	Video Processor Mute Low Value Register
VIDEO_CONTROL	0x0438	W	0x00000000	Video Processor Control Register
VIDEO_STATUS	0x043C	W	0x00000000	Video Processor Status Register
VIDEO_FVA_VRR_CONFIG	0x0448	W	0x00000000	Video Processor FVA/VRR Configuration Register
VIDEO_STREAMER_CONFIG2	0x045C	W	0x00000000	Video Streamer Configuration Register 2
AUDIO_FIFO_CONFIG	0x0460	W	0x00000000	Audio Processor FIFO Configuration Register
AUDIO_FIFO_CONTROL	0x0464	W	0x00000000	Audio Processor FIFO Control Register
AUDIO_FIFO_THR_PASS	0x0468	W	0x00000090	Audio Processor FIFO Threshold Pass Configuration
AUDIO_FIFO_THR	0x046C	W	0x00200160	Audio Processor FIFO Threshold High and Low
AUDIO_FIFO_MUTE_THR	0x0470	W	0x00080178	Audio Processor FIFO Mute Threshold High and Low
AUDIO_FIFO_STATUS1	0x0474	W	0x0000FFFF	Audio Processor FIFO Status Register 1
AUDIO_FIFO_STATUS2	0x0478	W	0x00000000	Audio Processor FIFO Status Register 2
AUDIO_PROC_CONFIG0	0x0480	W	0x00000000	Audio Processor Configuration Register 0
AUDIO_PROC_CONFIG1	0x0484	W	0x00000000	Audio Processor Configuration Register 1
AUDIO_PROC_CONFIG2	0x0488	W	0x01F103F3	Audio Processor Configuration Register 2
AUDIO_PROC_CONFIG3	0x048C	W	0x00000000	Audio Processor Configuration Register 3
AUDIO_PROC_STATUS1	0x0490	W	0x00000100	Audio Processor Status Register 1
AUDIO_PROC_STATUS2	0x0494	W	0x00000000	Audio Processor Status Register 2
AUDIO_PROC_CHSTAT_SP0_L1	0x04A0	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Left Register 1

Name	Offset	Size	Reset Value	Description
AUDIO_PROC_CHSTAT_SP0_L2	0x04A4	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Left Register 2
AUDIO_PROC_CHSTAT_SP0_L3	0x04A8	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Left Register 3
AUDIO_PROC_CHSTAT_SP0_L4	0x04AC	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Left Register 4
AUDIO_PROC_CHSTAT_SP0_L5	0x04B0	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Left Register 5
AUDIO_PROC_CHSTAT_SP0_L6	0x04B4	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Left Register 6
AUDIO_PROC_CHSTAT_SP0_R1	0x04B8	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Right 1
AUDIO_PROC_CHSTAT_SP0_R2	0x04BC	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Right 2
AUDIO_PROC_CHSTAT_SP0_R3	0x04C0	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Right 3
AUDIO_PROC_CHSTAT_SP0_R4	0x04C4	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Right 4
AUDIO_PROC_CHSTAT_SP0_R5	0x04C8	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Right 5
AUDIO_PROC_CHSTAT_SP0_R6	0x04CC	W	0x00000000	Audio Processor Channel Status Sub Packet 0 Right 6
AUDIO_PROC_CHSTAT_SP1_L1	0x04D0	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Left Register 1
AUDIO_PROC_CHSTAT_SP1_L2	0x04D4	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Left Register 2
AUDIO_PROC_CHSTAT_SP1_L3	0x04D8	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Left Register 3
AUDIO_PROC_CHSTAT_SP1_L4	0x04DC	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Left Register 4
AUDIO_PROC_CHSTAT_SP1_L5	0x04E0	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Left Register 5
AUDIO_PROC_CHSTAT_SP1_L6	0x04E4	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Left Register 6
AUDIO_PROC_CHSTAT_SP1_R1	0x04E8	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Right 1
AUDIO_PROC_CHSTAT_SP1_R2	0x04EC	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Right 2
AUDIO_PROC_CHSTAT_SP1_R3	0x04F0	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Right 3
AUDIO_PROC_CHSTAT_SP1_R4	0x04F4	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Right 4

Name	Offset	Size	Reset Value	Description
AUDIO_PROC_CHSTAT_SP1_R5	0x04F8	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Right 5
AUDIO_PROC_CHSTAT_SP1_R6	0x04FC	W	0x00000000	Audio Processor Channel Status Sub Packet 1 Right 6
AUDIO_PROC_CHSTAT_SP2_L1	0x0500	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Left Register 1
AUDIO_PROC_CHSTAT_SP2_L2	0x0504	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Left Register 2
AUDIO_PROC_CHSTAT_SP2_L3	0x0508	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Left Register 3
AUDIO_PROC_CHSTAT_SP2_L4	0x050C	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Left Register 4
AUDIO_PROC_CHSTAT_SP2_L5	0x0510	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Left Register 5
AUDIO_PROC_CHSTAT_SP2_L6	0x0514	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Left Register 6
AUDIO_PROC_CHSTAT_SP2_R1	0x0518	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Right 1
AUDIO_PROC_CHSTAT_SP2_R2	0x051C	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Right 2
AUDIO_PROC_CHSTAT_SP2_R3	0x0520	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Right 3
AUDIO_PROC_CHSTAT_SP2_R4	0x0524	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Right 4
AUDIO_PROC_CHSTAT_SP2_R5	0x0528	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Right 5
AUDIO_PROC_CHSTAT_SP2_R6	0x052C	W	0x00000000	Audio Processor Channel Status Sub Packet 2 Right 6
AUDIO_PROC_CHSTAT_SP3_L1	0x0530	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Left Register 1
AUDIO_PROC_CHSTAT_SP3_L2	0x0534	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Left Register 2
AUDIO_PROC_CHSTAT_SP3_L3	0x0538	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Left Register 3
AUDIO_PROC_CHSTAT_SP3_L4	0x053C	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Left Register 4
AUDIO_PROC_CHSTAT_SP3_L5	0x0540	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Left Register 5
AUDIO_PROC_CHSTAT_SP3_L6	0x0544	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Left Register 6
AUDIO_PROC_CHSTAT_SP3_R1	0x0548	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Right 1

Name	Offset	Size	Reset Value	Description
AUDIO_PROC_CHSTAT_SP3_R2	0x054C	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Right 2
AUDIO_PROC_CHSTAT_SP3_R3	0x0550	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Right 3
AUDIO_PROC_CHSTAT_SP3_R4	0x0554	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Right 4
AUDIO_PROC_CHSTAT_SP3_R5	0x0558	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Right 5
AUDIO_PROC_CHSTAT_SP3_R6	0x055C	W	0x00000000	Audio Processor Channel Status Sub Packet 3 Right 6
SCDC_CONFIG	0x0580	W	0x00000000	SCDC Configuration Register
SCDC_CONTROL	0x0584	W	0x00000000	SCDC Control Register
SCDC_REGBANK_STATUS0	0x0588	W	0x00000000	SCDC Read Status Register 0
SCDC_REGBANK_STATUS1	0x058C	W	0x00000000	SCDC Read Status Register 1
SCDC_REGBANK_STATUS2	0x0590	W	0x00000000	SCDC Read Status Register 2
SCDC_REGBANK_STATUS3	0x0594	W	0x00000000	SCDC Read Status Register 3
SCDC_REGBANK_STATUS4	0x0598	W	0x00000000	SCDC Read Status Register 4
SCDC_REGBANK_STATUS5	0x059C	W	0x00000000	SCDC Read Status Register 5
SCDC_REGBANK_STATUS8	0x05A8	W	0x00000000	SCDC Read Status Register 8
SCDC_REGBANK_MS_STATUS0	0x05AC	W	0x00000000	SCDC Manufacturer Specific Write Data Status Register 0
SCDC_REGBANK_MS_STATUS1	0x05B0	W	0x00000000	SCDC Manufacturer Specific Write Data Status Register 1
SCDC_REGBANK_MS_STATUS2	0x05B4	W	0x00000000	SCDC Manufacturer Specific Write Data Status Register 2
SCDC_REGBANK_MS_STATUS3	0x05B8	W	0x00000000	SCDC Manufacturer Specific Write Data Status Register 3
SCDC_REGBANK_MS_STATUS4	0x05BC	W	0x00000000	SCDC Manufacturer Specific Write Data Status Register 4
SCDC_REGBANK_CONFIG0	0x05C0	W	0x00000000	SCDC Write Data Register 0
SCDC_REGBANK_CONFIG1	0x05C4	W	0x00000000	SCDC Write Data Register 1
SCDC_REGBANK_CONFIG2	0x05C8	W	0x00000000	SCDC Write Data Register 2

Name	Offset	Size	Reset Value	Description
SCDC_REGBANK_CONFIG3	0x05CC	W	0x00000000	SCDC Write Data Register 3
SCDC_REGBANK_CONFIG4	0x05D0	W	0x00000000	SCDC Write Data Register 4
SCDC_REGBANK_CONFIG5	0x05D4	W	0x00000000	SCDC Write Data Register 5
SCDC_REGBANK_CONFIG6	0x05D8	W	0x00000000	SCDC Write Data Register 6
SCDC_REGBANK_CONFIG7	0x05DC	W	0x00000000	SCDC Write Data Register 7
SCDC_REGBANK_CONFIG8	0x05E0	W	0x00000000	SCDC Write Data Register 8
VPG_CONFIG0	0x0700	W	0x00000010	Video Pattern Generator Configuration Register 0
VPG_CONFIG1	0x0704	W	0x00000000	Video Pattern Generator Configuration Register 1
VPG_HAHB_CONFIG	0x0708	W	0x00A00280	Video Pattern Generator Hactive and Hblank configuration Register
VPG_HDHW_CONFIG	0x070C	W	0x00600010	Video Pattern Generator Hfront and Hwidth Configuration Register
VPG_VAVB_CONFIG	0x0710	W	0x002D01E0	Video Pattern Generator Vactive and Vblank Configuration register
VPG_VDVW_CONFIG	0x0714	W	0x0002000A	Video Pattern Generator Vfront and Vwidth Configuration register
VPG_CB_LENGTH_CONFIG	0x0718	W	0x00000000	Chess board pattern tile length
VPG_CB_COLORA_L	0x071C	W	0x00000000	Chess board pattern tile color a 32 least significant bits
VPG_CB_COLORA_H	0x0720	W	0x00000000	Chess board pattern tile color a 16 most significant bits
VPG_CB_COLORB_L	0x0724	W	0x00000000	Chess board pattern tile color b 32 least significant bits
VPG_CB_COLORB_H	0x0728	W	0x00000000	Chess board pattern tile color b 16 most significant bits
AUDIO_GEN_CONFIG0	0x0740	W	0x00000000	Audio Generator Configuration Register 0
AUDIO_GEN_CONFIG1	0x0744	W	0x00000000	Audio Generator Configuration Register 1
AUDIO_GEN_CONFIG2	0x0748	W	0x00000000	Audio Generator Configuration Register 2
AUDIO_GEN_CONFIG3	0x074C	W	0x00000000	Audio Generator Configuration Register 3

Name	Offset	Size	Reset Value	Description
CED_CONFIG	0x0760	W	0x0F000000	Character Error Detection Configuration Register
CED_STATUS	0x0764	W	0x00000000	Character Error Detection Status Register
CED_DYN_CONFIG	0x0768	W	0x00000001	Character Error Detection Dynamic Counter Configuration
CED_DYN_CONTROL	0x076C	W	0x00000000	Character Error Detection Dynamic Counter Control Register
CED_DYN_STATUS1	0x0770	W	0x00000000	Character Error Detection Dynamic Counter Status Register 1
CED_DYN_STATUS2	0x0774	W	0x00000000	Character Error Detection Dynamic Counter Status Register 2
PKTEX_BCH_ERRCORR_CONFIG	0x07C0	W	0x00000003	Packet Extractor BCH Error Correction Control register
PKTEX_BCH_ERRFILT_CONFIG	0x07C4	W	0x00000000	Packet Extractor BCH Error Filter Control Register
PKTEX_CHKSUM_ERRFILT_CONFIG	0x07C8	W	0x00000000	Packet Extractor InfoFrame Checksum Error Filter Control
PKTEX_BCHERR_ACC_STATUS	0x07CC	W	0x00000000	Packet Extractor Accumulated Number of BCH Errors Status
PKTEX_FIELDS_BCHERR_STATUS	0x07D0	W	0xFFFFFFFF	Packet Extractor Number of Fields since last BCH Error
GENPKT_TYPE_CONFIG	0x07D4	W	0x00000000	Generic Packet Type Config Register
PKTEX_UPI_CONFIG	0x0800	W	0x00000000	Packet Extractor UPI Configuration Register When
PKTEX_UPI_EMDFILTER_CONFIG	0x0804	W	0x00000000	Packet Extractor UPI Extended Metadata Packet
GENEMD_EMDFILTER_CONFIG	0x0808	W	0x00000000	Generic Extended Metadata Packet Type Config Register
PKTDEC_ACR_CONFIG	0x1000	W	0x00000000	Packet Decoder ACR CTS/N Override Enable Control
PKTDEC_ACR_CTS_CONFIG	0x1004	W	0x00000000	Packet Decoder ACR CTS Override Value Register
PKTDEC_ACR_N_CONFIG	0x1008	W	0x00000000	Packet Decoder ACR N Override Value Register
PKTDEC_ACR_MAXMIN_CLEAR	0x100C	W	0x00000000	Packet Decoder ACR CTS/N Maximum/Minimum Tracking
PKTDEC_ACR_CTS_MAX_STATUS	0x1010	W	0x00000000	Packet Decoder ACR CTS Maximum Value Tracking

Name	Offset	Size	Reset Value	Description
PKTDEC_ACR_CTS_MIN_STATUS	0x1014	W	0x00000000	Packet Decoder ACR CTS Minimum Value Tracking Register
PKTDEC_ACR_N_MAX_STATUS	0x1018	W	0x00000000	Packet Decoder ACR N Maximum Value Tracking Register
PKTDEC_ACR_N_MIN_STATUS	0x101C	W	0x00000000	Packet Decoder ACR N Minimum Value Tracking Register
PKTDEC_SP_VALID_CONFIG	0x1020	W	0x00000000	Packet Decoder Subpacket 0 only Control Register
PKTDEC_GCP_AVMUTE_CONFIG	0x1024	W	0x00000000	Packet Decoder GCP/CMP AVMUTE Override Control
PKTDEC_AVMUTE_DIS_CONTROL	0x1028	W	0x00000000	Packet Decoder AVMUTE Disable Control Register
PKTDEC_EMD_CONTROL	0x102C	W	0x00000000	Packet Decoder EMD Control Register
PKTDEC_GCP_AVMUTE_STATUS	0x1030	W	0x00000000	Packet Decoder GCP/CMP AVMUTE Status Register
PKTDEC_EMD_STATUS	0x1034	W	0x00000000	Packet Decoder Extended Metadata Status Register
PKTDEC_SNAPSHOT_BYP_CONTROL	0x1040	W	0x00000000	Packet Decoder Snapshot Bypass Control Register
PKTDEC_ACR_PH2_1	0x1100	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Header Bytes 1-2
PKTDEC_ACR_PB3_0	0x1104	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Body Bytes 3-0
PKTDEC_ACR_PB7_4	0x1108	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Body Bytes 7-4
PKTDEC_ACR_PB11_8	0x110C	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Body Bytes 11-8
PKTDEC_ACR_PB15_12	0x1110	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Body Bytes 15-12
PKTDEC_ACR_PB19_16	0x1114	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Body Bytes 19-16
PKTDEC_ACR_PB23_20	0x1118	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Body Bytes 23-20

Name	Offset	Size	Reset Value	Description
PKTDEC_ACR_PB27_24	0x111C	W	0x00000000	Packet Decoder Audio Clock Regeneration Packet Body Bytes 27-24
PKTDEC_GCP_PH2_1	0x1120	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Header Bytes 1-2
PKTDEC_GCP_PB3_0	0x1124	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Body Bytes 3-0
PKTDEC_GCP_PB7_4	0x1128	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Body Bytes 7-4
PKTDEC_GCP_PB11_8	0x112C	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Body Bytes 11-8
PKTDEC_GCP_PB15_12	0x1130	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Body Bytes 15-12
PKTDEC_GCP_PB19_16	0x1134	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Body Bytes 19-16
PKTDEC_GCP_PB23_20	0x1138	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Body Bytes 23-20
PKTDEC_GCP_PB27_24	0x113C	W	0x00000000	Packet Decoder Generic Content/ Content Mute Packet Body Bytes 27-24
PKTDEC_ACP_PH2_1	0x1140	W	0x00000000	Packet Decoder Audio Content Protection Packet Header Bytes 1-2
PKTDEC_ACP_PB3_0	0x1144	W	0x00000000	Packet Decoder Audio Content Protection Packet Body Bytes 3-0
PKTDEC_ACP_PB7_4	0x1148	W	0x00000000	Packet Decoder Audio Content Protection Packet Body Bytes 7-4
PKTDEC_ACP_PB11_8	0x114C	W	0x00000000	Packet Decoder Audio Content Protection Packet Body Bytes 11-8
PKTDEC_ACP_PB15_12	0x1150	W	0x00000000	Packet Decoder Audio Content Protection Packet Body Bytes 15-12
PKTDEC_ACP_PB19_16	0x1154	W	0x00000000	Packet Decoder Audio Content Protection Packet Body Bytes 19-16

Name	Offset	Size	Reset Value	Description
PKTDEC_ACP_PB23_20	0x1158	W	0x00000000	Packet Decoder Audio Content Protection Packet Body Bytes 23-20
PKTDEC_ACP_PB27_24	0x115C	W	0x00000000	Packet Decoder Audio Content Protection Packet Body Bytes 27-24
PKTDEC_ISRC1_PH2_1	0x1160	W	0x00000000	Packet Decoder ISRC1 Packet Header Bytes 1-2
PKTDEC_ISRC1_PB3_0	0x1164	W	0x00000000	Packet Decoder ISRC1 Packet Body Bytes 3-0
PKTDEC_ISRC1_PB7_4	0x1168	W	0x00000000	Packet Decoder ISRC1 Packet Body Bytes 7-4
PKTDEC_ISRC1_PB11_8	0x116C	W	0x00000000	Packet Decoder ISRC1 Packet Body Bytes 11-8
PKTDEC_ISRC1_PB15_12	0x1170	W	0x00000000	Packet Decoder ISRC1 Packet Body Bytes 15-12
PKTDEC_ISRC1_PB19_16	0x1174	W	0x00000000	Packet Decoder ISRC1 Packet Body Bytes 19-16
PKTDEC_ISRC1_PB23_20	0x1178	W	0x00000000	Packet Decoder ISRC1 Packet Body Bytes 23-20
PKTDEC_ISRC1_PB27_24	0x117C	W	0x00000000	Packet Decoder ISRC1 Packet Body Bytes 27-24
PKTDEC_ISRC2_PH2_1	0x1180	W	0x00000000	Packet Decoder ISRC2 Packet Header Bytes 1-2
PKTDEC_ISRC2_PB3_0	0x1184	W	0x00000000	Packet Decoder ISRC2 Packet Body Bytes 3-0
PKTDEC_ISRC2_PB7_4	0x1188	W	0x00000000	Packet Decoder ISRC2 Packet Body Bytes 7-4
PKTDEC_ISRC2_PB11_8	0x118C	W	0x00000000	Packet Decoder ISRC2 Packet Body Bytes 11-8
PKTDEC_ISRC2_PB15_12	0x1190	W	0x00000000	Packet Decoder ISRC2 Packet Body Bytes 15-12
PKTDEC_ISRC2_PB19_16	0x1194	W	0x00000000	Packet Decoder ISRC2 Packet Body Bytes 19-16
PKTDEC_ISRC2_PB23_20	0x1198	W	0x00000000	Packet Decoder ISRC2 Packet Body Bytes 23-20
PKTDEC_ISRC2_PB27_24	0x119C	W	0x00000000	Packet Decoder ISRC2 Packet Body Bytes 27-24
PKTDEC_GMD_PH2_1	0x11A0	W	0x00000000	Packet Decoder Gamut Metadata Packet Header Bytes 1-2
PKTDEC_GMD_PB3_0	0x11A4	W	0x00000000	Packet Decoder Gamut Metadata Packet Body Bytes 3-0

Name	Offset	Size	Reset Value	Description
PKTDEC_GMD_PB7_4	0x11A8	W	0x00000000	Packet Decoder Gamut Metadata Packet Body Bytes 7-4
PKTDEC_GMD_PB11_8	0x11AC	W	0x00000000	Packet Decoder Gamut Metadata Packet Body Bytes 11-8
PKTDEC_GMD_PB15_12	0x11B0	W	0x00000000	Packet Decoder Gamut Metadata Packet Body Bytes 15-12
PKTDEC_GMD_PB19_16	0x11B4	W	0x00000000	Packet Decoder Gamut Metadata Packet Body Bytes 19-16
PKTDEC_GMD_PB23_20	0x11B8	W	0x00000000	Packet Decoder Gamut Metadata Packet Body Bytes 23-20
PKTDEC_GMD_PB27_24	0x11BC	W	0x00000000	Packet Decoder Gamut Metadata Packet Body Bytes 27-24
PKTDEC_AMD_PH2_1	0x11C0	W	0x00000000	Packet Decoder Audio Metadata Packet Header Bytes 1-2
PKTDEC_AMD_PB3_0	0x11C4	W	0x00000000	Packet Decoder Audio Metadata Packet Body Bytes 3-0
PKTDEC_AMD_PB7_4	0x11C8	W	0x00000000	Packet Decoder Audio Metadata Packet Body Bytes 7-4
PKTDEC_AMD_PB11_8	0x11CC	W	0x00000000	Packet Decoder Audio Metadata Packet Body Bytes 11-8
PKTDEC_AMD_PB15_12	0x11D0	W	0x00000000	Packet Decoder Audio Metadata Packet Body Bytes 15-12
PKTDEC_AMD_PB19_16	0x11D4	W	0x00000000	Packet Decoder Audio Metadata Packet Body Bytes 19-16
PKTDEC_AMD_PB23_20	0x11D8	W	0x00000000	Packet Decoder Audio Metadata Packet Body Bytes 23-20
PKTDEC_AMD_PB27_24	0x11DC	W	0x00000000	Packet Decoder Audio Metadata Packet Body Bytes 27-24
PKTDEC_VSIF_PH2_1	0x11E0	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Header Bytes 1-2
PKTDEC_VSIF_PB3_0	0x11E4	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Body Bytes 3-0
PKTDEC_VSIF_PB7_4	0x11E8	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Body Bytes 7-4
PKTDEC_VSIF_PB11_8	0x11EC	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Body Bytes 11-8
PKTDEC_VSIF_PB15_12	0x11F0	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Body Bytes 15-12

Name	Offset	Size	Reset Value	Description
PKTDEC_VSIF_PB19_16	0x11F4	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Body Bytes 19-16
PKTDEC_VSIF_PB23_20	0x11F8	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Body Bytes 23-20
PKTDEC_VSIF_PB27_24	0x11FC	W	0x00000000	Packet Decoder Vendor-Specific InfoFrame Packet Body Bytes 27-24
PKTDEC_AVIIF_PH2_1	0x1200	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Header Bytes 1-2
PKTDEC_AVIIF_PB3_0	0x1204	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Body Bytes 3-0
PKTDEC_AVIIF_PB7_4	0x1208	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Body Bytes 7-4
PKTDEC_AVIIF_PB11_8	0x120C	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Body Bytes 11-8
PKTDEC_AVIIF_PB15_12	0x1210	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Body Bytes 15-12
PKTDEC_AVIIF_PB19_16	0x1214	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Body Bytes 19-16
PKTDEC_AVIIF_PB23_20	0x1218	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Body Bytes 23-20
PKTDEC_AVIIF_PB27_24	0x121C	W	0x00000000	Packet Decoder Auxiliary Video Information InfoFrame Packet Body Bytes 27-24
PKTDEC_SRCPDIF_PH2_1	0x1220	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Header Bytes 1-2
PKTDEC_SRCPDIF_PB3_0	0x1224	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Body Bytes 3-0
PKTDEC_SRCPDIF_PB7_4	0x1228	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Body Bytes 7-4

Name	Offset	Size	Reset Value	Description
PKTDEC_SRCPDIF_PB11_8	0x122C	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Body Bytes 11-8
PKTDEC_SRCPDIF_PB15_12	0x1230	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Body Bytes 15-12
PKTDEC_SRCPDIF_PB19_16	0x1234	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Body Bytes 19-16
PKTDEC_SRCPDIF_PB23_20	0x1238	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Body Bytes 23-20
PKTDEC_SRCPDIF_PB27_24	0x123C	W	0x00000000	Packet Decoder Source Product Descriptor InfoFrame Packet Body Bytes 27-24
PKTDEC_AUDIF_PH2_1	0x1240	W	0x00000000	Packet Decoder Audio InfoFrame Packet Header Bytes 1-2
PKTDEC_AUDIF_PB3_0	0x1244	W	0x00000000	Packet Decoder Audio InfoFrame Packet Body Bytes 3-0
PKTDEC_AUDIF_PB7_4	0x1248	W	0x00000000	Packet Decoder Audio InfoFrame Packet Body Bytes 7-4
PKTDEC_AUDIF_PB11_8	0x124C	W	0x00000000	Packet Decoder Audio InfoFrame Packet Body Bytes 11-8
PKTDEC_AUDIF_PB15_12	0x1250	W	0x00000000	Packet Decoder Audio InfoFrame Packet Body Bytes 15-12
PKTDEC_AUDIF_PB19_16	0x1254	W	0x00000000	Packet Decoder Audio InfoFrame Packet Body Bytes 19-16
PKTDEC_AUDIF_PB23_20	0x1258	W	0x00000000	Packet Decoder Audio InfoFrame Packet Body Bytes 23-20
PKTDEC_AUDIF_PB27_24	0x125C	W	0x00000000	Packet Decoder Audio InfoFrame Packet Body Bytes 27-24
PKTDEC_NTSCVBIIF_PH2_1	0x1280	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Header Bytes 1-2
PKTDEC_NTSCVBIIF_PB3_0	0x1284	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Body Bytes 3-0
PKTDEC_NTSCVBIIF_PB7_4	0x1288	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Body Bytes 7-4
PKTDEC_NTSCVBIIF_PB11_8	0x128C	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Body Bytes 11-8

Name	Offset	Size	Reset Value	Description
PKTDEC_NTSCVBIIF_PB15_12	0x1290	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Body Bytes 15-12
PKTDEC_NTSCVBIIF_PB19_16	0x1294	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Body Bytes 19-16
PKTDEC_NTSCVBIIF_PB23_20	0x1298	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Body Bytes 23-20
PKTDEC_NTSCVBIIF_PB27_24	0x129C	W	0x00000000	Packet Decoder NTSC VBI InfoFrame Packet Body Bytes 27-24
PKTDEC_DRMIF_PH2_1	0x12A0	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Header Bytes 1-2
PKTDEC_DRMIF_PB3_0	0x12A4	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Body Bytes 3-0
PKTDEC_DRMIF_PB7_4	0x12A8	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Body Bytes 7-4
PKTDEC_DRMIF_PB11_8	0x12AC	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Body Bytes 11-8
PKTDEC_DRMIF_PB15_12	0x12B0	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Body Bytes 15-12
PKTDEC_DRMIF_PB19_16	0x12B4	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Body Bytes 19-16
PKTDEC_DRMIF_PB23_20	0x12B8	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Body Bytes 23-20
PKTDEC_DRMIF_PB27_24	0x12BC	W	0x00000000	Packet Decoder Dynamic Range and Mastering InfoFrame Packet Body Bytes 27-24
PKTDEC_EMD_PH2_1	0x12C0	W	0x00000000	Packet Decoder Extended Metadata Packet Header Bytes 1-2
PKTDEC_EMD_PB3_0	0x12C4	W	0x00000000	Packet Decoder Extended Metadata Packet Body Bytes 3-0
PKTDEC_EMD_PB7_4	0x12C8	W	0x00000000	Packet Decoder Extended Metadata Packet Body Bytes 7-4

Name	Offset	Size	Reset Value	Description
PKTDEC_EMD_PB11_8	0x12CC	W	0x00000000	Packet Decoder Extended Metadata Packet Body Bytes 11-8
PKTDEC_EMD_PB15_12	0x12D0	W	0x00000000	Packet Decoder Extended Metadata Packet Body Bytes 15-12
PKTDEC_EMD_PB19_16	0x12D4	W	0x00000000	Packet Decoder Extended Metadata Packet Body Bytes 19-16
PKTDEC_EMD_PB23_20	0x12D8	W	0x00000000	Packet Decoder Extended Metadata Packet Body Bytes 23-20
PKTDEC_EMD_PB27_24	0x12DC	W	0x00000000	Packet Decoder Extended Metadata Packet Body Bytes 27-24
PKTDEC_GENPKT0_PH2_1	0x1480	W	0x00000000	Packet Decoder Generic Packet 0 Packet Header Bytes 1-2
PKTDEC_GENPKT0_PB3_0	0x1484	W	0x00000000	Packet Decoder Generic Packet 0 Packet Body Bytes 3-0
PKTDEC_GENPKT0_PB7_4	0x1488	W	0x00000000	Packet Decoder Generic Packet 0 Packet Body Bytes 7-4
PKTDEC_GENPKT0_PB11_8	0x148C	W	0x00000000	Packet Decoder Generic Packet 0 Packet Body Bytes 11-8
PKTDEC_GENPKT0_PB15_12	0x1490	W	0x00000000	Packet Decoder Generic Packet 0 Packet Body Bytes 15-12
PKTDEC_GENPKT0_PB19_16	0x1494	W	0x00000000	Packet Decoder Generic Packet 0 Packet Body Bytes 19-16
PKTDEC_GENPKT0_PB23_20	0x1498	W	0x00000000	Packet Decoder Generic Packet 0 Packet Body Bytes 23-20
PKTDEC_GENPKT0_PB27_24	0x149C	W	0x00000000	Packet Decoder Generic Packet 0 Packet Body Bytes 27-24
PKTDEC_GENPKT1_PH2_1	0x14A0	W	0x00000000	Packet Decoder Generic Packet 1 Packet Header Bytes 1-2
PKTDEC_GENPKT1_PB3_0	0x14A4	W	0x00000000	Packet Decoder Generic Packet 1 Packet Body Bytes 3-0
PKTDEC_GENPKT1_PB7_4	0x14A8	W	0x00000000	Packet Decoder Generic Packet 1 Packet Body Bytes 7-4
PKTDEC_GENPKT1_PB11_8	0x14AC	W	0x00000000	Packet Decoder Generic Packet 1 Packet Body Bytes 11-8
PKTDEC_GENPKT1_PB15_12	0x14B0	W	0x00000000	Packet Decoder Generic Packet 1 Packet Body Bytes 15-12
PKTDEC_GENPKT1_PB19_16	0x14B4	W	0x00000000	Packet Decoder Generic Packet 1 Packet Body Bytes 19-16

Name	Offset	Size	Reset Value	Description
PKTDEC_GENPKT1_PB23_20	0x14B8	W	0x00000000	Packet Decoder Generic Packet 1 Packet Body Bytes 23-20
PKTDEC_GENPKT1_PB27_24	0x14BC	W	0x00000000	Packet Decoder Generic Packet 1 Packet Body Bytes 27-24
PKTFIFO_CONFIG	0x1500	W	0x00000000	Packet FIFO Configure Register
PKTFIFO_STORE_FILT_CONFIG	0x1504	W	0x00000000	Packet FIFO Store Filter Control Register
PKTFIFO_THR_CONFIG0	0x1508	W	0x00000032	Packet FIFO Threshold Configure Register 0
PKTFIFO_THR_CONFIG1	0x150C	W	0x00000008	Packet FIFO Threshold Configure Register 1
PKTFIFO_CONTROL	0x1510	W	0x00000000	Packet FIFO Control Register
PKTFIFO_FILL_STATUS	0x1514	W	0x00000000	Packet FIFO Fill Level Status Register
PKTFIFO_LTERM_FILL_STATUS	0x1518	W	0x00000000	Packet FIFO Long-term Fill Level Status Register
PKTFIFO_SKIP_PKT_CONTROL	0x151C	W	0x00000000	Packet FIFO Skip Packet Control Register
PKTFIFO_DATA	0x1520	W	0x00000000	Packet FIFO Data Register
VMON_CONTROL	0x1560	W	0x00000000	Video Monitor Control Register
VMON_CONTROL2	0x1564	W	0x00001F1F	Video Monitor Control Register 2
VMON_STATUS1	0x1580	W	0x00000000	Video Monitor Status Register 1
VMON_STATUS2	0x1584	W	0x00000000	Video Monitor Status Register 2
VMON_STATUS3	0x1588	W	0x00000000	Video Monitor Status Register 3
VMON_STATUS4	0x158C	W	0x00000000	Video Monitor Status Register 4
VMON_STATUS5	0x1590	W	0x00000000	Video Monitor Status Register 5
VMON_STATUS6	0x1594	W	0x00000000	Video Monitor Status Register 6
VMON_STATUS7	0x1598	W	0x00000000	Video Monitor Status Register 7
CEC_TX_CONTROL	0x2000	W	0x00000000	CEC Transmit Control Register This register handles the main control of the CEC initiator
CEC_STATUS	0x2004	W	0x00000000	CEC Status Register
CEC_CONFIG	0x2008	W	0x00000110	CEC Configuration Register
CEC_ADDR	0x200C	W	0x00000000	CEC Logical Address Register
CEC_TX_COUNT	0x2020	W	0x00000000	CEC Transmitter Buffer Counter Register
CEC_TX_DATA3_0	0x2024	W	0x00000000	CEC Byte 0-3 Transmitter Data Buffer Register
CEC_TX_DATA7_4	0x2028	W	0x00000000	CEC Byte 4-7 Transmitter Data Buffer Register
CEC_TX_DATA11_8	0x202C	W	0x00000000	CEC Byte 8-11 Transmitter Data Buffer Register

Name	Offset	Size	Reset Value	Description
CEC_TX_DATA15_12	0x2030	W	0x00000000	CEC Byte 12-15 Transmitter Data Buffer Register
CEC_RX_COUNT_STATUS	0x2040	W	0x00000000	CEC Receiver Buffer Counter and Lock Status Register
CEC_RX_DATA3_0	0x2044	W	0x00000000	CEC Byte 0-3 Receiver Data Buffer Register
CEC_RX_DATA7_4	0x2048	W	0x00000000	CEC Byte 4-7 Receiver Data Buffer Register
CEC_RX_DATA11_8	0x204C	W	0x00000000	CEC Byte 8-11 Receiver Data Buffer Register
CEC_RX_DATA15_12	0x2050	W	0x00000000	CEC Byte 12-15 Receiver Data Buffer Register
CEC_LOCK_CONTROL	0x2054	W	0x00000000	CEC Lock Control Register
CEC_RXQUAL_BITTIME_CONFIG	0x2060	W	0x00033333	CEC RX Bit Qualifier Timings Note: A change on these may cause out of specification CEC line timings
CEC_RX_BITTIME_CONFIG	0x2064	W	0x00333333	CEC RX Bit Qualifier Timings Note: A change on these may cause out of specification CEC line
CEC_TX_BITTIME_CONFIG	0x2068	W	0x63444444	CEC TX Bit Qualifier Timings Note: A change on these may cause out of specification CEC line
DMA_CONFIG1	0x4400	W	0x00000000	HDMIRX DMA control register1
DMA_CONFIG2	0x4404	W	0x00000000	HDMIRX DMA control register2
DMA_CONFIG3	0x4408	W	0x00000000	HDMIRX DMA control register3
DMA_CONFIG4	0x440C	W	0x00000000	HDMIRX DMA control register4
DMA_CONFIG5	0x4410	W	0x00000000	HDMIRX DMA control register5
DMA_CONFIG6	0x4414	W	0x00000000	HDMIRX DMA control register6
DMA_CONFIG7	0x4418	W	0x00000000	HDMIRX DMA control register7
DMA_CONFIG8	0x441C	W	0x00000000	HDMIRX DMA control register8
DMA_CONFIG9	0x4420	W	0x00000000	HDMIRX DMA control register9
DMA_CONFIG10	0x4424	W	0x00000000	HDMIRX DMA control register10
DMA_CONFIG11	0x4428	W	0x60010050	HDMIRX DMA control register11
DMA_STATUS1	0x4430	W	0x00000000	HDMIRX DMA status register1
DMA_STATUS2	0x4434	W	0x00000000	HDMIRX DMA status register2
DMA_STATUS3	0x4438	W	0x00000000	HDMIRX DMA status register3
DMA_STATUS4	0x443C	W	0x00000000	HDMIRX DMA status register4
DMA_STATUS5	0x4440	W	0x00000000	HDMIRX DMA status register5
DMA_STATUS6	0x4444	W	0x00000000	HDMIRX DMA status register6
DMA_STATUS7	0x4448	W	0x00000000	HDMIRX DMA status register7
DMA_STATUS8	0x444C	W	0x00000000	HDMIRX DMA status register8

Name	Offset	Size	Reset Value	Description
DMA_STATUS9	0x4450	W	0x00000000	HDMIRX DMA status register9
DMA_STATUS10	0x4454	W	0x00000000	HDMIRX DMA status register10
DMA_STATUS11	0x4458	W	0x00000000	HDMIRX DMA status register11
DMA_STATUS12	0x445C	W	0x00000000	HDMIRX DMA status register12
DMA_STATUS13	0x4460	W	0x00000000	HDMIRX DMA status register13
DMA_STATUS14	0x4464	W	0x00000000	HDMIRX DMA status register14
MAINUNIT_INTVEC_INDEX	0x5000	W	0x00000000	Main Unit Interrupt Vector Table Register
MAINUNIT_0_INT_STATUS	0x5010	W	0x00000000	Main Unit 0 Interrupt Status Register
MAINUNIT_0_INT_MASK_N	0x5014	W	0xC40000F3	Main Unit 0 Interrupt Mask Register
MAINUNIT_0_INT_CLEAR	0x5018	W	0x00000000	Main Unit 0 Interrupt Clear Register
MAINUNIT_0_INT_FORCE	0x501C	W	0x00000000	Main Unit 0 Interrupt Force Register
MAINUNIT_1_INT_STATUS	0x5020	W	0x00000000	Main Unit 1 Interrupt Status Register
MAINUNIT_1_INT_MASK_N	0x5024	W	0x00000000	Main Unit 1 Interrupt Mask Register
MAINUNIT_1_INT_CLEAR	0x5028	W	0x00000000	Main Unit 1 Interrupt Clear Register
MAINUNIT_1_INT_FORCE	0x502C	W	0x00000000	Main Unit 1 Interrupt Force Register
MAINUNIT_2_INT_STATUS	0x5030	W	0x00000000	Main Unit 2 Interrupt Status Register
MAINUNIT_2_INT_MASK_N	0x5034	W	0x00000000	Main Unit 2 Interrupt Mask Register
MAINUNIT_2_INT_CLEAR	0x5038	W	0x00000000	Main Unit 2 Interrupt Clear Register
MAINUNIT_2_INT_FORCE	0x503C	W	0x00000000	Main Unit 2 Interrupt Force Register
AVPUNIT_0_INT_STATUS	0x5040	W	0x00000000	AVPUNIT 0 Interrupt Status Register
AVPUNIT_0_INT_MASK_N	0x5044	W	0x00000000	AVPUNIT 0 Interrupt Mask Register
AVPUNIT_0_INT_CLEAR	0x5048	W	0x00000000	AVPUNIT 0 Interrupt Clear Register
AVPUNIT_0_INT_FORCE	0x504C	W	0x00000000	AVPUNIT 0 Interrupt Force Register
AVPUNIT_1_INT_STATUS	0x5050	W	0x00000000	AVPUNIT 1 Interrupt Status Register

Name	Offset	Size	Reset Value	Description
AVPUNIT_1_INT_MASK_N	0x5054	W	0x00000000	AVPUNIT 1 Interrupt Mask Register
AVPUNIT_1_INT_CLEAR	0x5058	W	0x00000000	AVPUNIT 1 Interrupt Clear Register
AVPUNIT_1_INT_FORCE	0x505C	W	0x00000000	AVPUNIT 1 Interrupt Force Register
PKT_0_INT_STATUS	0x5080	W	0x00000000	Packet Decoder, FIFO, and Extractor 0 Interrupt Status
PKT_0_INT_MASK_N	0x5084	W	0x00000000	Packet Decoder, FIFO, and Extractor 0 Interrupt Mask
PKT_0_INT_CLEAR	0x5088	W	0x00000000	Packet Decoder, FIFO, and Extractor 0 Interrupt Clear
PKT_0_INT_FORCE	0x508C	W	0x00000000	Packet Decoder, FIFO, and Extractor 0 Interrupt Force
PKT_1_INT_STATUS	0x5090	W	0x00000000	Packet Decoder, FIFO, and Extractor 1 Interrupt Status
PKT_1_INT_MASK_N	0x5094	W	0x00000000	Packet Decoder, FIFO, and Extractor 1 Interrupt Mask
PKT_1_INT_CLEAR	0x5098	W	0x00000000	Packet Decoder, FIFO, and Extractor 1 Interrupt Clear
PKT_1_INT_FORCE	0x509C	W	0x00000000	Packet Decoder, FIFO, and Extractor 1 Interrupt Force
PKT_2_INT_STATUS	0x50A0	W	0x00000000	Packet Decoder, FIFO, and Extractor 2 Interrupt Status
PKT_2_INT_MASK_N	0x50A4	W	0x00000000	Packet Decoder, FIFO, and Extractor 2 Interrupt Mask
PKT_2_INT_CLEAR	0x50A8	W	0x00000000	Packet Decoder, FIFO, and Extractor 2 Interrupt Clear
PKT_2_INT_FORCE	0x50AC	W	0x00000000	Packet Decoder, FIFO, and Extractor 2 Interrupt Force
SCDC_INT_STATUS	0x50C0	W	0x00000000	SCDC Interrupt Status Register
SCDC_INT_MASK_N	0x50C4	W	0x00000000	SCDC Interrupt Mask Register
SCDC_INT_CLEAR	0x50C8	W	0x00000000	SCDC Interrupt Clear Register
SCDC_INT_FORCE	0x50CC	W	0x00000000	SCDC Interrupt Force Register
HDCP_INT_STATUS	0x50D0	W	0x00000000	HDCP Interrupt Status Register
HDCP_INT_MASK_N	0x50D4	W	0x00000000	HDCP Interrupt Mask Register
HDCP_INT_CLEAR	0x50D8	W	0x00000000	HDCP Interrupt Clear Register
HDCP_INT_FORCE	0x50DC	W	0x00000000	HDCP Interrupt Force Register
HDCP_1_INT_STATUS	0x50E0	W	0x00000000	HDCP Interrupt Status Register 1
HDCP_1_INT_MASK_N	0x50E4	W	0x00000000	HDCP Interrupt Mask Register 1
HDCP_1_INT_CLEAR	0x50E8	W	0x00000000	HDCP Interrupt Clear Register 1
HDCP_1_INT_FORCE	0x50EC	W	0x00000000	HDCP Interrupt Force Register 1

Name	Offset	Size	Reset Value	Description
CEC_INT_STATUS	0x5100	W	0x00000000	CEC Interrupt Status Register
CEC_INT_MASK_N	0x5104	W	0x00000000	CEC Interrupt Mask Register
CEC_INT_CLEAR	0x5108	W	0x00000000	CEC Interrupt Clear Register
CEC_INT_FORCE	0x510C	W	0x00000000	CEC Interrupt Force Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.3 Detail Registers Description

CORE_ID
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	core_id This register is ASCII encoded per byte: 31:24-8'h48=H ASCII Character 23:16-8'h51=Q ASCII Character 15:8-8'h52=R ASCII Character 7:0-8'h58=X ASCII Character ASCII representation of this register content is HQRX

VER_NUMBER
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ver_number This register represents the ASCII value of current IP version, for example: 31:24-8'h31=1 ASCII Character 23:16-8'h30=0 ASCII Character 15:8-8'h30=0 ASCII Character 7:0-8'h61=a ASCII Character For the above example, ASCII representation of this register content is 1.00a

VER_TYPE
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ver_type This register represents the ASCII value of the current release type, for example: 31:24-8'h65=e ASCII Character 23:16-8'h61=a ASCII Character 15:8-8'h30=0 ASCII Character 7:0-8'h30=0 ASCII Character For the above example, ASCII representation of this register content is ea00

CONFIG_REG

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	earctx Indicates that Enhanced Audio Return Channel(eARC)TX interface is present on IP core hardware
27:25	RO	0x0	reserved
24	RO	0x0	phy_external Indicates that PHY external interface is present on IP core hardware
23:13	RO	0x000	reserved
12	RO	0x0	frl Indicates that hdmi2.1 features, including Fixed Rate Link(FRL)are present on IP core hardware
11:10	RO	0x0	reserved
9	RO	0x0	cec Indicates that CEC interface is present on IP core hardware
8	RO	0x0	pmu Indicates that Power Management Unit(PMU)is present on IP core hardware
7:6	RO	0x0	reserved
5	RO	0x0	hdcp2_interface Indicates that HDCP2 ESM is present on IP core hardware
4	RO	0x0	hdcp14_external_dkset Indicates that HDCP1.4 external device key set(DPK and Bksv) memory interface is present on IP core hardware
3:2	RO	0x0	reserved
1	RO	0x0	snps_audio_pll Indicates that Audio PLL interface is present on IP core hardware
0	RO	0x0	audio_sample_output Indicates that Audio Sample Output interface is present on IP core hardware

CORE_TIMESTAMP_HHMM

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	core_timestamp_hhmm This register represents the ASCII value of the timestamp for the Hours/Minutes(HHMM format)at the generation of the IP.

CORE_TIMESTAMP_MMDD

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	core_timestamp_mmdd This register represents the ASCII value of the timestamp for the Month/Day(MMDD format)at the generation of the IP.

CORE_TIMESTAMP_YYYY

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	core_timestamp_yyyy This register represents the ASCII value of the timestamp for the Year(YYYY format)at the generation of the IP

GLOBAL_SWRESET_REQUEST

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	phyctrl_swresetreq PHY control register parallel interface software reset request. Reading this register always returns zero. 1'b0: No effect 1'b1: This will generate the following synchronized reset that acts as an asynchronous reset in the RTL code: ophyctrl_refrst_n, ophyctrl_cr_pararst_n.
20:18	RO	0x0	reserved
17	WO	0x0	apb_swresetreq APB interface software reset request. Reading this register always returns zero. 1'b0: No effect 1'b1: Reset the APB interface logic This does not clear any register in any functional unit. This acts over the following internal reset signals: APB interface reset: oapb_ apbrst_n and oapb_refrst_n.
16	WO	0x0	cec_swresetreq CEC unit software reset request. 1'b0: No effect 1'b1: Reset the CEC unit Reading this register always returns zero. This acts over the following internal reset signals: CEC reset: ocec_refrst_n
15:13	RO	0x0	reserved
12	WO	0x0	datapath_swresetreq AVPUNIT datapath software reset request. 1'b0: No effect 1'b1: Reset the AVPUNIT logic Reading this register always returns zero. This does not reset the AVPUNIT registers neither reset the HDCP1.4 DPK keys stored in the HDCP1.4 engine, nor reset the SCDC module or I2C Slave module. This acts over the following internal reset signals: AVPUNIT datapath resets: odatapath_refrst_n, odatapath_tmdsqprst_n, oaud_audrst_n, oaud_tmdsqprst_n, oaud_refrst_n, ohdcp_refrst_n, ohdcp_tmdsqprst_n, opktfifo_ tmdsqprst_n, opktfifo_apbrst_n, and opktfifo_refrst_n
11	WO	0x0	pktfifo_swresetreq Packet FIFO functional unit software reset request. 1'b0: No effect 1'b1: Reset the packet FIFO related configuration registers. Reading this register always return zero. This acts over the following internal reset signals: Audio logic resets: opktfifo_tmdsqprst_n, opktfifo_apbrst_n, and opktfifo_ refrst_n.

Bit	Attr	Reset Value	Description
10	WO	0x0	hdcp_swresetreq HDCP functional unit software reset request. 1'b0: No effect 1'b1: Reset the HDCP logic in the AVPUNIT Reading this register always returns zero. This acts over the following internal reset signals: HDCP logic resets: ohdcp_refrst_n, ohdcpkey_refrst_n, and ohdcp_tmdsqprst_ n.
9	WO	0x0	audio_swresetreq Audio functional unit software reset request. Reading this register always returns zero. 1'b0: No effect 1'b1: Reset the audio logic in the AVPUNIT. This acts over the following internal reset signals: Audio logic resets: oaud_audrst_n, oaud_tmdsqprst_n, and oaud_refrst_n.
8	WO	0x0	avpunit_swresetreq avpunit software reset request: 1'b0: No effect 1'b1: Reset all the avpunit logic Reading this register always returns zero. This acts over the following internal reset signals: oavpunit_refrst_n, oavpunit_tmdsqprst_n, odatapath_refrst_n, odatapath_tmdsqprst_n, oaud_audrst_n, oaud_tmdsqprst_n, oaud_refrst_n, oscdc_refrst_n, oi2c_refrst_n, ohdcp_refrst_n, ohdcpkey_refrst_n, ohdcp_tmdsqprst_n, opktfifo_tmdsqprst_n, opktfifo_apbrst_n, and opktfifo_refrst_n.
7:1	RO	0x00	reserved
0	WO	0x0	main_swresetreq Main reset control field that when activated resets all configuration and status bits and resets all functional units. 1’b0: No action 1’b1: Start reset This acts over the following internal reset signals: (1)Main Unit reset: omain_refrst_n (2)AVPUNIT resets: oavpunit_refrst_n, oavpunit_tmdsqprst_n, odatapath_refrst_n, odatapath_tmdsqprst_n, oaud_audrst_n, oaud_tmdsqprst_n, oaud_refrst_n, oscdc_refrst_n, oi2c_refrst_n, ohdcp_refrst_n, ohdcpkey_refrst_n, ohdcp_tmdsqprst_n, opktfifo_tmdsqprst_n, opktfifo_apbrst_n, and opktfifo_refrst_n (3)CEC reset: ocec_refrst_n (4)APB interface reset: oapb_apbrst_n, oapb_refrst_n (5)PHY controller reset: ophyctrl_refrst_n, ophyctrl_cr_pararst_n This bit is self clearing.

GLOBAL_SWENABLE

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x1	phyctrl_enable PHY Control Register Parallel interface synchronous enable. 1'b0: It disables the following synchronous enable bits: CREG synchronous enables: wphyctrl_ref_en, wphyctrl_cr_para_en. 1'b1: It enables the corresponding synchronous enable bit.
20:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x1	cec_enable CEC synchronous enable. 1'b0: It disables the following synchronous enable bits: CEC synchronous enables: ocec_ref_en. 1'b1: It enables the corresponding synchronous enable bit. Attention: CEC associated registers are cleared.
15:14	RO	0x0	reserved
13	RW	0x1	tmds_enable TMDS datapath synchronous enable. 1'b0: It disables the following synchronous enable bits: TMDS datapath synchronous enables: otmds_ref_en, otmds_tmdsqp_en. 1'b1: It enables the corresponding synchronous enable bit.
12	RW	0x1	datapath_enable AVPUNIT datapath synchronous enable: 1'b0: It disables the following synchronous enable bits: AVPUNIT datapath synchronous enable: odatapath_ref_en, odatapath_ tmdsqp_en, otmds_ref_en, otmds_tmdsqp_en, oaud_aud_en, oaud_tmdsqp_en, oaud_ref_en, ohdcp_ref_en, ohdcp_tmdsqp_en, opktfifo_apb_en, opktfifo_tmdsqp_en, opktfifo_ref_en 1'b1: It enables the corresponding synchronous enable bit. Attention: This does not clear AVPUNIT registers neither the HDCP1.4 DPK keys stored in the HDCP1.4 engine.
11	RW	0x1	pktfifo_enable Packet FIFO synchronous enable: 1'b0: It disables the following synchronous enable bits: Packet FIFO synchronous enables: opktfifo_apb_en, opktfifo_tmdsqp_en, opktfifo_ref_en. 1'b1: It enables the corresponding synchronous enable bit. Attention: Packet FIFO associated registers are cleared.
10	RW	0x1	hdcp_enable HDCP 1.4 synchronous enable. 1'b0: It disables the following synchronous enable bits. HDCP synchronous enables: ohdcp_ref_en, ohdcpkey_ref_en, ohdcp_ tmdsqp_en. 1'b1: It enables the corresponding synchronous enable bit. Attention: HDCP associated configuration registers are not cleared but HDCP1.4 keys stored inside HDCP1.4 engine are cleared. Attention: When HDCP1.4 is disabled(global_swenable: hdcp_enable == 0) and HDCP type selection is HDCP1.4 (hdcp2_status: hdcp2_type_sel_sts==0), video and audio are not available in downstream blocks. In this condition, no video and audio are provided on the respective output interfaces.
9	RW	0x1	audio_enable Audio synchronous enable. 1'b0: It disables the following synchronous enable bits: Audio synchronous enables: oaud_aud_en, oaud_tmdsqp_en, oaud_ref_ en. 1'b1: It enables the corresponding synchronous enable bit. Attention: Audio associated registers are not cleared.

Bit	Attr	Reset Value	Description
8	RW	0x1	avpunit_enable AVPUNIT synchronous enable. 1'b0: It disables the following synchronous enable bits. AVPUNIT synchronous enable: oavpunit_ref_en, oavpunit_tmdsqp_en, odatapath_ref_en, odatapath_tmdsqp_en, otmds_ref_en, otmds_tmdsqp_en, oaud_aud_en, oaud_tmdsqp_en, oaud_ref_en, oscdc_ ref_en, oi2c_ref_en, ohdcp_ref_en, ohdcpkey_ref_en, ohdcp_tmdsqp_en, opktfifo_apb_en, opktfifo_tmdsqp_en, opktfifo_ref_en. 1'b1: It enables the corresponding synchronous enable bit. Attention: After this bit field is successfully released, the mainunit_0_int_status.regbank_ready_irq interrupt is triggered raising the ohdmi_int signal. This interrupt is automatically triggered by the main unit to warn the software that the AVPUNIT register bank is ready to be accessed.
7:1	RO	0x00	reserved
0	RW	0x1	main_enable Main synchronous enable. 1'b0: It disables the following synchronous enable bits. (1)Main unit synchronous enable: omain_ref_en (2)AVPUNIT synchronous enable: oavpunit_ref_en, oavpunit_tmdsqp_en, odatapath_ ref_en, odatapath_tmdsqp_en, otmds_ref_en, otmds_tmdsqp_en, oaud_aud_en, oaud_tmdsqp_en, oaud_ref_en, oscdc_ref_en, oi2c_ref_en, ohdcp_ref_en, ohdcpkey_ref_en, ohdcp_tmdsqp_en, opktfifo_apb_en, opktfifo_tmdsqp_en, opktfifo_ ref_en. (3)CEC synchronous enable: ocec_ref_en. 1'b1: The control of the synchronous enables is performed by its individual bits. Attention: After this bit field is successfully released, the mainunit_0_int_status.apb_if_ready_irq and mainunit_0_int_status.regbank_ready_irq interrupts are triggered raising the ohdmi_int signal. This interrupt is automatically triggered by the main unit to warn the software that the register bank is ready to be accessed.

GLOBAL_TIMER_REF_BASE

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	timer_reference_base Timer reference base, this represents the number of irefclk cycles in 1 second. This is the frequency of the irefclk. Attention: This register is always consistent with input irefclk clock frequency. Example of configured value for irefclk of 200MHz is 29'd200000000.

PMU_POWER_REQUEST

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13	WO	0x0	cec_power_up_req_p CEC Power Up Request. 1'b0: No action 1'b1: The CEC power region receives a power-up request and is reconnected to the rest of the controller. The interrupt mainunit_1_int_status.cec_powered_up_irq=1'b1 indicates that CEC region has completed the power on sequence. Note: Before powering up this region the CEC must be disabled (cec_enable set to 0).
12	WO	0x0	cec_power_down_req_p CEC Power Down Request. 1'b0: No action 1'b1: The CEC power region receives a power-down request and is isolated for the rest of the controller. The interrupt mainunit_1_int_status.cec_powered_down_irq=1'b1 indicates that the CEC region has completed the power-down sequence.
11:2	RO	0x000	reserved
1	WO	0x0	avpunit_power_up_req_p AVPUNIT Power Up Request. 1'b0: No action 1'b1: The AVPUNIT power region receives a power-up request and it is reconnected to the rest of the controller. The interrupt mainunit_1_int_status.avpunit_powered_up_irq=1'b1 indicates that the AVPUNIT region has completed the power on sequence. Before powering up this region, the avpunit must be disabled (avpunit_enable set to 0).
0	WO	0x0	avpunit_power_down_req_p AVPUNIT Power Down Request: 1'b0: No action 1'b1: The AVPUNIT power region receives a power-down request and is isolated from the rest of the controller. The interrupt mainunit_1_int_status.avpunit_powered_down_irq=1'b1 indicates that the AVPUNIT region has completed the power down sequence.

PMU_POWER_STATUS

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	cec_isolation_st CEC Isolation Status. 1'b0: ISOLATION is OFF in the CEC power domain. 1'b1: ISOLATION is ON in the CEC power domain(the domain is isolated).
12	RO	0x1	cec_power_st CEC Power Status. 1'b0: Power is OFF in the CEC power domain. 1'b1: Power is ON in the CEC power domain(the domain is powered).
11:2	RO	0x000	reserved
1	RO	0x0	avpunit_isolation_st AVPUNIT Isolation Status. 1'b0: ISOLATION is OFF in the AVPUNIT power domain. 1'b1: ISOLATION is ON in the AVPUNIT power domain.(the domain is isolated)

Bit	Attr	Reset Value	Description
0	RO	0x1	avpunit_power_st AVPUNIT Power Status. 1'b0: Power is OFF in the AVPUNIT power domain. 1'b1: Power is ON in the AVPUNIT power domain(the domain is powered).

PMU_POWER_CONFIG

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	isolation_to_power_gap Time gap between the setting the isolation and switching off the power. The time is counted in irefclk cycles and that gap can be configured with the following values: 3'b000: 2 3'b001: 65 3'b010: 129 3'b011: 257 3'b100: 513 3'b101: 1025 3'b110: 2049 3'b111: 4096

CORE_CONFIG

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	hpd HPD plug detect for HDMI source input.

CMU_CONFIG0

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0001	tmdsqpclk_stable_freq_margin TMDS QP Clock-Allowed frequency variation(in kHz) for clock lock. This field cannot exceed 7% of the nominal clock frequency.
15	RO	0x0	reserved
14:0	RW	0x0001	audclk_stable_freq_margin Audio clock-Allowed frequency variation(in kHz) for clock lock. This field cannot exceed 7% of the nominal clock frequency.

CMU_CONFIG3

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0001	frlclk_stable_freq_margin FRL Clock-Allowed frequency variation(in kHz) for clock lock. This field cannot exceed 7% of the nominal clock frequency.

CMU_CONFIG5

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0001	cr_para_clk_stable_freq_margin CR_PARA Clock-Allowed frequency variation(in kHz) for clock lock. This field cannot exceed 7% of the nominal clock frequency.

CMU_STATUS

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	timer_base_locked_st Timer base locked status flag. 1'b0: Timer Base calculations in progress and not locked. 1'b1: Timer Base calculations completed and locked. Note: Writing a new Timer Reference Base to the register global_timer_ref_base initiates new Timer Base calculations. While these are in progress, this status is expected to fall momentaneously and when the calculations are finally done it is expected to rise, together with corresponding interrupt request time_base_locked_irq.
27:8	RO	0x00000	reserved
7	RO	0x0	cr_para_clk_off_st CR_PARA Clock off(not running)status flag. This signal is set to 1 whenever there is not CR_PARA Clock activity during two consecutive evaluation time periods.
6	RO	0x0	cr_para_clk_locked_st CR_PARA Clock measure locked status flag. 1'b0: Clock is not locked 1'b1: Clock is locked(is within the configured stable frequency margin)
5	RO	0x0	tmdsqpclk_off_st TMDSQP Clock off(not running)status flag. This signal is set to 1 whenever there is no TMDS QP Clock activity during two consecutive evaluation time periods.
4	RO	0x0	tmdsqpclk_locked_st TMDSQP Clock measure locked status flag. 1'b0: Clock is not locked. 1'b1: Clock is locked(is within the configured stable frequency margin)
3:2	RO	0x0	reserved
1	RO	0x0	audclk_off_st Audio Clock off(not running) status flag. This signal is set to 1 whenever there is no Audio Clock activity during two consecutive evaluation time periods.
0	RO	0x0	audclk_locked_st Audio Clock measure locked status flag. 1'b0: Clock is not locked 1'b1: Clock is locked(is within the configured stable frequency margin)

CMU_AUDCLK_FREQ

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RO	0x00000	audclk_freq Audio Clock frequency in kHz.

CMU_TMDSQPCLK_FREQ

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	tmdsqpclk_freq TMDS QP Clock frequency in kHz.

CMU_CR_PARA_CLK_FREQ

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	cr_para_clk_freq CR_PARA Clock frequency in kHz.

CMU_MAIN_CONFIG

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	cmu_en Enable CMU 0: Disable 1: Enable

PHY_CONFIG

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	ldo_earc_bleed_en LDO Configuration.
27:26	RW	0x0	ldo_earc_prog LDO Configuration.
25	RW	0x0	ldo_afe_bleed_en LDO Configuration.
24:23	RW	0x0	ldo_afe_prog LDO Configuration.
22	RW	0x0	ldo_bypass LDO Configuration.
21	RW	0x0	ldo_pwrdn LDO Configuration.
20	RW	0x0	ldo_earc_pwrdn LDO Configuration
19:17	RO	0x0	reserved
16	RW	0x0	tmds_clock_ratio This signal defines the TMDS clock ratio to the bit rate for TMDS modes. 1'b0: TMDS clock = 1/10 of bit rate 1'b1: TMDS clock = 1/40 of bit rate. If the bit rate > 3.4Gbps, it will be configured 1'b1.

Bit	Attr	Reset Value	Description
15	RW	0x0	rxdata_width PHY data channel width selection. 1'b0: 20-bit valid data on rxdata_X[53:0] (X=0, 1, 2) 1'b1: 40-bit valid data on rxdata_X[53:0] (X=0, 1, 2) In current usage, it will be configured 1'b1 for 40bit valid.
14	RW	0x0	test_stop_clk_en PHY Test interface-test_stop_clk_en.
13	RW	0x0	test_powerdown PHY Test interface-test_powerdown.
12	RW	0x0	test_burnin PHY Test interface-test_burnin.
11:9	RW	0x0	reffreq_sel Frequency selection for cr_para_clk PHY clock input. It indicates the current frequency of the cr_para_clk. Value-Reference clock Frequency(MHz) 3'b000: 24 3'b001: 25 3'b010: 27 3'b011: 48 3'b100: 50 3'b101: 54 3'b110: 100 3'b111: Reserved
8	RW	0x1	hdmi_disable Disable/Restart PHY
7:2	RO	0x00	reserved
1	RW	0x1	phy_pddq PHY pddq control.
0	RW	0x1	phy_reset PHY Reset control. 1'b1: Reset the HDMIRX phy 1'b0: Reset release

PHY_STATUS

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	hdmi_disable_ack HDMI Disable Acknowledge
0	RO	0x0	pddq_ack PDDQ Acknowledge

PHY_JTAG_CONFIG

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	earctx_jtag_trst_n JTAG interface reset output to the eARC TX PHY. This is no useful.
3:1	RO	0x0	reserved
0	RW	0x0	jtag_trst_n JTAG interface reset output to PHY 1'b0: Reset enabled 1'b1: Reset disabled

PHY_JTAG_TAP_TCLK

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	earctx_jtag_tck JTAG interface clock output to eARC TX PHY. This is no useful.
3:1	RO	0x0	reserved
0	RW	0x0	jtag_tck JTAG interface clock output to PHY.

PHY_JTAG_TAP_IN

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	jtag_tms JTAG interface Test Mode Select(TMS) output to PHY.
3:1	RO	0x0	reserved
0	RW	0x0	jtag_tdi JTAG interface data in, output to PHY.

PHY_JTAG_TAP_OUT

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	jtag_tdo_en JTAG interface data output enable from PHY.
3:1	RO	0x0	reserved
0	RO	0x0	jtag_tdo JTAG interface data output from PHY

PHYCREG_CONFIG0

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	phycreg_cr_para_selection_mode PHYCR Selection Mode: This field control the selection between the PHY JTAG and CR interfaces, and also to control the clock gating of the internal CR bus. The possible modes are as follows: 2'b00: JTAG selected and clock not available on internal CR bus(if internally blocked) 2'b01: JTAG selected and clock available on internal CR bus (irrespective of internally blocked or not) 2'b10: Control Register(CR) selected and clock not available on internal CR bus (if internally blocked) 2'b11: Control Register(CR)selected and clock available on internal CR bus (irrespective of internally blocked or not)

PHYCREG_CONFIG1

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phycreg_cr_para_addr CR address

PHYCREG_CONFIG2
Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phycreg_cr_para_wr_data CR write data

PHYCREG_CONFIG3
Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	earctx_phycreg_selector It selects between the PHY CR interface of the HDMI PHY and the EARCTX PHY. 1'b0: HDMI PHY interface selected 1'b1: EARCTX PHY interface selected

PHYCREG_CONTROL
Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	phycreg_cr_para_write_p CR write enable function: Writes the data on cr_para_wr_data [15:0] to the referenced address on cr_para_addr[15:0].
0	WO	0x0	phycreg_cr_para_read_p CR read enable function: Reads from the referenced address on cr_para_addr[15:0] and provides the data on cr_para_rd_data [15:0].

PHYCREG_STATUS
Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	phycreg_cr_para_datavalid CR read data is valid
23:16	RO	0x00	reserved
15:0	RO	0x0000	phycreg_cr_para_rd_data CR read data

PHYCREG_CONFIG4
Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x100	phycreg_cr_para_timeout CR timeout value in cr_para_clk cycles. The timeout counter is restarted with a read/write operation and counts until receiving an ack from the PHY(ocfg_phycreq_cr_write/read_done_irq) or when the specified timeout value is reached (ocfg_phycreg_cr_timeout_irq).

MAINUNIT_STATUS
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	tmdsvalid_stable_st TMDS valid stable change interrupt status.
0	RO	0x0	audpll_lock_stable_st Audio PLL lock stable change interrupt status.

I2C_SLAVE_CONFIG0

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	i2c_reply_nack I2C reply with NACK
19:12	RW	0x50	i2c_h2_sel_addr_qst Debug register that controls I2C HDCP port address used to switch between HDCP2 versus HDCP1.4 operation. Attention: By HDCP2 specification it should be 0x50 and should not be changed since it may cause improper HDCP operation.
11:10	RO	0x0	reserved
9:8	RW	0x0	i2c_spike_suppr_qst SCDC I2C select spike suppression mode 2'b00: 2 out of 2 2'b01: 2 out of 3(majority selection) 2'b10: 3 out of 3 2'b11: 4 out of 4
7:5	RO	0x0	reserved
4	RW	0x0	i2c_timeout_en_qst I2C timeout enable 1'b0: Disable timeout 1'b1: Enable timeout
3	RO	0x0	reserved
2:0	RW	0x0	i2c_timeout_cnt_qst I2C timeout window value. When the timeout window elapses, a reset is applied to the I2C slave. Timeout counter starts when SCL line is asserted high. 3'b000: Timeout 1ms 3'b001: Timeout 2ms 3'b010: Timeout 3ms 3'b011: Timeout 4ms 3'b100: Timeout 5ms 3'b101: Timeout 6ms 3'b110: Timeout 7ms 3'b111: Timeout 7ms

I2C_SLAVE_CONFIG1

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	i2c_sda_out_hold_value_qst I2C SDA_OUT hold time value(expressed in number of irefclk cycles). Valid range is 8'd0, ..., 8'd255. Attention: When I2C_SDA_OUT hold time is disabled(equal to 8'd0), the hold time must be ensured externally by SDA I/O.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	i2c_sda_in_hold_value_qst I2C SDA_IN hold time value(expressed in number of irefclk cycles). Valid range is 8'd0, ..., 8'd255. Attention: When I2C_SDA_IN hold time is disabled(equal to 8'd0), the hold time must be ensured externally by SDA I/O.

DESCRAND_EN_CONTROL

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x1	frl_descramb_en_qst FRL Descrambler Enable. It is no useful.
7:2	RO	0x00	reserved
1:0	RW	0x0	scramb_en_sel_qst HDMI2.0 Scrambling Enable selector. 2'b00: SCDC control(default). The SCDC Scrambling_Enable value controls Descrambler disable/enable. 2'b01: Auto-detect. Enable Descrambling when scrambled data is detected. 2'b10: Forces Descrambling disable. 2'b11: Forces Descrambling enable.

DESCRAND_SYNC_CONTROL

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:1	RW	0x0	min_ucp_char_qst Minimum number of followed Unscrambled Control Characters required for an Unscrambled Control Period to be considered for applying reset to the Descrambler LFSRs. 2'b00: A complete Unscrambled Control Period is considered if the number of received Unscrambled Control characters resides between 5 and 8. 2'b01: A complete Unscrambled Control Period is considered if the number of received Unscrambled Control characters resides between 6 and 8. 2'b10: A complete Unscrambled Control Period is considered if the number of received Unscrambled Control characters resides between 7 and 8. 2'b11: Only a complete received Unscrambled Control Period is considered (8 out of 8 Unscrambled Control characters received).
0	RW	0x0	recover_unsync_stream_qst Recover unsynched HDMI stream. Until the first Descrambler synchronization character sequence(Unscrambled Control Period)is received, the Descrambler LFSRs are not synchronized, and therefore data combined with their output values is considered invalid. With this debug field configured high, the unsynchronized stream is forwarded as valid data to datapath blocks that succeed the Descrambler.

DESCRAND_STATUS

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RO	0x0	scramb_det_sts Scrambling detected(scrambling detected even with auto detection control disabled, that is, scramben_sel_qst != 1). This status signal is driven high when a Scrambled Control Code is received. If a Control Period with more than eight Unscrambled Control Characters is received, this status signal is driven low.
3:1	RO	0x0	reserved
0	RO	0x0	descrand_sync_st Descrambler synchronization status. 1'b0: Descrambler is not synchronized 1'b1: Unscrambled Control Period synchronization symbols have been received and Descrambler is synchronized

DESCRAND_SYNC_SEQ_CONFIG

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x4	descrand_sync_seq_err_cnt_thr Interrupt counter threshold for sync sequence(Unscrambled Control Period)errors. 3'b000: 2 3'b001: 4 3'b010: 8 3'b011: 16 3'b100: 32 3'b101: 64 3'b110: 128 3'b111: 256
3:1	RO	0x0	reserved
0	RW	0x1	descrand_sync_seq_err_cnt_en Interrupt counter enable for Sync Sequence(Unscrambled Control Period) errors. 1'b0: The interrupt is set every time the related event occurs. 1'b1: The interrupt is set when the counter is a multiple of the value set by the threshold.

DESCRAND_SYNC_SEQ_CLEAR

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	descrand_sync_seq_err_cnt_clr_p Clear sync_seq_err interrupt counter 1'b0: No action 1'b1: Clear counter to 0 Note: This register is auto-clear. Reading this register always reads zero.

DESCRAND_SYNC_SEQ_STATUS

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	descrand_sync_seq_err_cnt_sts Interrupt counter for sync_seq_err events. This register reflects the number of incomplete Descrambler Synchronization Character sequences received, in case of errors in the TMDS stream. The HDMI2.0 Specification dictates that the Unscrambled Control Period corresponds exactly to eight consecutive Unscrambled Control Characters. If this sequence is received with less than the defined number of characters and therefore is considered incomplete, this counter is incremented.

DEFRAMER_CONFIG0

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	vs_cnt_thr_qst Vertical Sync counter threshold 8'd0: Reserved 8'd1-8'd255: When Vsync counter reach this value, the avpunit_1_int_status.vsync_thr_reached_irq interrupt is asserted. Software can also clear and restart the Vsync counter threshold by writing in vsync_cnt_clr_p field.
19:18	RW	0x0	hs_pol_qst Horizontal Sync Polarity mechanism control. 2'b00: Automatic 2'b01: Manual, inverted HSYNC 2'b10: Manual, no HSYNC inversion 2'b11: Same as 0, automatic
17:16	RW	0x0	vs_pol_qst Vertical Sync Polarity mechanism control. 2'b00: Automatic 2'b01: Manual, inverted VSYNC 2'b10: Manual, no VSYNC inversion 2'b11: Same as 0, automatic
15:13	RO	0x0	reserved
12	RW	0x0	ctl_spikefilter_en_qst CTL spike filter enable 1'b0: No filtering is applied to control channels. 1'b1: Single cycle spike filtering applied in the control channels CTL0, CTL1, CTL2, CTL3 in Control Period indication.
11:9	RO	0x0	reserved
8	RW	0x0	vs_remapfilter_en_qst Vertical Sync remap filter enable 1'b0: No filtering is applied to Vsync 1'b1: Vsync format filter active. Vsync format correction filter is activated and the reformatted Vsync is forwarded.
7:4	RO	0x0	reserved
3:2	RW	0x0	hs_filter_order_qst Horizontal Sync glitch filter order 2'b00: Filter is disabled 2'b01/2'b10/2'b11: Configures the duration(number of pixel fragments)of the glitch to be filter in the correspondent sync signal(in a pixel clocked stream a fragment corresponds to one pixel clock cycle)

Bit	Attr	Reset Value	Description
1:0	RW	0x0	vs_filter_order_qst Vertical Sync glitch filter order 2'b00: Filter is disabled 2'b01/2'b10/2'b11: Configures the duration(number of pixel fragments)of the glitch to be filter in the correspondent sync signal(in a pixel clocked stream a fragment corresponds to one pixel clock cycle)

DEFRAMER_CONFIG1

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	opmode_hdmi_type_qst HDMI Operation type(only valid if opmode_hdmi_qst is set to value 2 and HDMI QP RX controller is configured with HDMI2.1 FRL support) 2'b00: HDMI Legacy Mode(for HDMI2.0 and 1.X specifications) 2'b01: HDMI FRL 3L 2'b10: HDMI FRL 4L 2'b11: Reserved
27	RO	0x0	reserved
26:24	RW	0x2	hdmi2dvi_thr_qst HDMI to DVI threshold Configures the number of consecutive fields(determined by Vsync active edge rise), with no detected Data Islands, needed to change from HDMI to DVI mode. 3'd0: Reserved 3'd1-3'd7: 1 to 7 fields
23	RO	0x0	reserved
22:20	RW	0x1	dvi2hdmi_thr_qst DVI to HDMI threshold Configures the number of consecutive fields(determined by Vsync active edge rise), with detected Data Islands, needed to change from DVI to HDMI mode. 3'd0: Reserved 3'd1-3'd7: 1 to 7 fields
19:18	RO	0x0	reserved
17:16	RW	0x0	opmode_hdmi_qst HDMI Operation mode. 2'b00: HDMI automatic detection 2'b01: Forces DVI operation 2'b10: Forces HDMI operation 2'b11: Reserved
15:8	RW	0x00	gb_err_thr_qst Guard Band errors threshold. 8'd0: Interrupt gbdet_err_irq triggered when on Guard Band error occurs. 8'd1-8'd255: The Guard Band check mechanism implements a counter that accumulates the Guard Band errors occurred in last last_frame_gb_check_qst fields. When this counter reaches the value defined in threshold gb_err_thr_qst, the Guard Band errors gbdet_err_irq is triggered.

Bit	Attr	Reset Value	Description
7:4	RW	0xf	last_frame_gb_check_qst Number of fields to accumulate Guard Band errors. This accumulated value is then be compared against gb_err_thr_qst. If accumulated errors are greater than configured threshold, the gbdet_err_irq is triggered. 4'd0: Guard Band errors in one filed. 4'd1-4'd15: Guard Band errors in 2 up to 16 fields correspondingly.
3:0	RW	0x8	num_preamble_lock_qst Number of preambles needed to lock. 8'd0-8'd4: Reserved 8'd5-8'd8: This is the minimum number of preambles required to transact from Control Period to Data Island Period or Video Data Period (depending preamble type) 8'd9-8'd15: Reserved

DEFRAMER_VSYNC_CNT_CLEAR

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	vsync_cnt_clr_p Vertical sync counter clear Vertical sync counter is cleared when this bit is asserted high.

DEFRAMER_STATUS

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RO	0x0	opmode_sts Operation mode status 3'b000: DVI mode 3'b001: HDMI2.0 or 1.X mode 3'b010: Reserved 3'b011: Reserved 3'b100: HDMI2.1 FRL 3L mode 3'b101: HDMI2.1 FRL 4L mode 3'b110: Reserved 3'b111: Reserved
3:1	RO	0x0	reserved
0	RO	0x0	autohdmidvi_sts Automatic HDMI/DVI mode detection

HDCP14_CONFIG

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	hdcp14_delay_qst HDCP1.4 delay-delays in HDCP1.4 data path. The HDCP1.4 path is balanced, so this is configured to be zero(used for debug purposes).
29	RO	0x0	reserved
28	RW	0x0	repeater_qst HDCP repeater capability value 1'b0: HDCP1.4 repeater disable 1'b1: HDCP1.4 repeater enable

Bit	Attr	Reset Value	Description
27	RW	0x0	fastreauth_qst Bcaps Fast Re-authentication value. When asserted high, the HDCP receiver is capable of receiving (unencrypted)video signals during the session re-authentication.
26	RW	0x0	features_1dot1_qst HDCP1.4 1.1 Features capability. When asserted high, the HDCP receiver supports Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options.
25	RW	0x0	fasti2c_qst Bcaps Fast I2C value 1'b0: 100kHz is the maximum transfer rate supported 1'b1: Device supports 400kHz transfers
24	RW	0x0	hdmi_rsvd_qst Bcaps HDMI reserved value(is zero)
23:20	RO	0x0	reserved
19:16	RW	0xe	eess_ctl_thr_qst EESS number of CTL=1001 threshold to consider ENC_EN on EESS. This field configures the number (minus one)of HDMI clocks that CTL3..0 is equal to 4'b1001, during the Window Of Opportunity, to be considered as active encryption enable. 4'd0-4'd10: Reserved 4'd11-4'd15: 12 to 16 CTL=1001 values to consider ENC:EN on EESS.
15:12	RO	0x0	reserved
11:8	RW	0x7	oess_ctl3_thr_qst OESS number of CTL3=1 threshold to consider ENC_EN on OESS. This field configures the number of HDMI clocks that CTL3 must be asserted high to be considered as active encryption enable. 4'd0: Reserved 4'd1-4'd8: 1 up to 8 CTL3 at 1 4'd9-4'd15: Reserved
7:6	RO	0x0	reserved
5:4	RW	0x0	eess_oess_sel_qst EESS/OESS selection 2'b00: Automatic mode 1(operation is HDMI mode or 1.1 features is enabled) 2'b01: Forces OESS 2'b10: Forces EESS 2'b11: Automatic mode 2
3:1	RO	0x0	reserved
0	RW	0x0	key_decrypt_en_qst HDCP Key Encryption enable 1'b0: HDCP key is not encrypted 1'b1: HDCP key is encrypted

HDCP14_WOO_CONFIG

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x214	hdcp_woo_end_qst HDCP WOO end position(used only in EESS). Number of pixels after the Vertical Sync active edge where the Window Of Opportunity ends. This value should take into account WOO definition on HDCP1.4 Specification and desired range of receiver adaptability to uncompliant sources. This value is always higher than hdcp_woo_start_qst and is primarily intended for debug purposes(for that reason it is not advisable to change it from its default value).
15:10	RO	0x00	reserved
9:0	RW	0x1fc	hdcp_woo_start_qst HDCP WOO start position(used only in EESS). Number of pixels after the Vertical Sync active edge where the Window Of Opportunity starts. This value should take into account WOO definition on HDCP1.4 Specification and desired range of receiver adaptability to uncompliant sources. This value is always lower than hdcp_woo_end_qst and is primarily intended for debug purposes(for that reason it is not advisable to change it from its default value).

HDCP14_KEY_H

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	WO	0x000000	hdcp_key_high HDCP Encrypted Key[55:32] portion Encrypted secret key, only for external storage of encrypted HDCP keys. A key is written by first writing the high part of hdcpkey[55:32] in hdcp_key_high register and then the low hdcpkey[31:0] to hdcp_ key_low register. Writing hdcp_key_low triggers decryption and storage in the key table, as well as auto incrementing of the hdcp_ key_index.

HDCP14_KEY_L

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	hdcp_key_low HDCP Encrypted Key[31:0] portion Encrypted secret key, only for external storage of encrypted HDCP keys. A key is written by first writing the high part of hdcpkey[55:32] in hdcp_key_high register and then the low hdcpkey[31:0] to hdcp_ key_low register. Writing hdcp_key_low triggers decryption and storage in the key table, as well as auto incrementing of the hdcp_key_index.

HDCP14_KEY_STATUS

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RO	0x0	hdcp_key_wr_ok HDCP Key write ok. Status flag to indicate whether key set writing is allowed. 1'b0: Not allowed. 1'b1: Allowed.
7:6	RO	0x0	reserved
5:0	RO	0x00	hdcp_key_index HDCP Key index. Valid range is 6'h00-6'h27.

HDCP14_BKSV_H
Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	hdcp_bksv_high_qst DDC Bksv register content(bits 39:32)

HDCP14_BKSV_L
Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hdcp_bksv_low_qst DDC Bksv register content(bit31:0)

HDCP14_STATUS
Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	hdcp14_decrypt_on HDCP1.4 decryption on. 1'b0: HDCP1.4 decryption is off. 1'b1: HDCP1.4 decryption is on.
7:6	RO	0x0	reserved
5	RO	0x0	hdcp14_oess_eess_chg_st HDCP1.4 OESS/EESS change interrupt status
4	RO	0x0	hdcp14_auth_st HDCP1.4 authentication interrupt status
3:2	RO	0x0	reserved
1:0	RO	0x0	auth_curstate HDCP1.4 Authentication FSM State. 2'b00: B0_UNAUTHENTICATED 2'b01: B1_COMPUTATION 2'b10: B2_AUTHENTICATED 2'b11: B3_UPDATE_RI

HDCP14_BSTATUS
Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	hdcp_bstatus HDCP1.4 Bstatus Content. [15:14]: Reserved [13]: Reserved for future possible HDMI use [12]: HDMI_MODE [11]: MAX_CASCADE_EXCEEDED [10:8]: DEPTH [7]: MAX_DEVS_EXCEEDED [6:0]: DEVICE_COUNT

HDCP14_DDC_STATUS0

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	hdcp_ri HDCP1.4 Ri value
15:9	RO	0x00	reserved
8	RO	0x0	hdcp_ainfo HDCP1.4 Ainfo enable 1.1 features flag
7:0	RO	0x00	hdcp_pj HDCP1.4 Pj value

HDCP14_DDC_STATUS1

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdcp_an_high HDCP1.4 An[63:32] value

HDCP14_DDC_STATUS2

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdcp_an_low HDCP1.4 An[31:0] value

HDCP14_DDC_STATUS3

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	hdcp_aksv_high HDCP1.4 Aksv[39:0] value

HDCP14_DDC_STATUS4

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdcp_aksv_low HDCP1.4 Aksv[31:0] value

HDCP14_RPT_KSV_H

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	rpt_ksv_high HDCP Repeater KSV[39:32] portion

HDCP14_RPT_KSV_L

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rpt_ksv_low HDCP Repeater KSV[31:0] portion

HDCP14_RPT_CONTROL
Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	rpt_lostauth Detected the lost of authentication by a downstream device.Auto-clearing.
1	WO	0x0	rpt_timeout A timeout or a topology error as occurred when gathering the KSV list from the downstream devices. Auto-clearing.
0	WO	0x0	rpt_ksvlistready Indicates that software has completed the KSV memory write process. Auto-clearing.

HDCP14_RPT_KSVFIFO
Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	rpt_ksv_index KSV list index pointer. Set index of KSV to be written in rpt_ksv_high and rpt_ksv_low registers

HDCP14_RPT_STATUS
Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	rpt_waitingksv Indicates that the HDCP hardware has completed the first part of the authentication and is currently waiting for the KSV FIFO to be written, and rpt_ksvlist_ready is to be set.
7:5	RO	0x0	reserved
4	RO	0x0	rpt_ksvhold Status flag to indicate whether key set writing is. 1'b0: Allowed 1'b1: Not allowed
3:1	RO	0x0	reserved
0	RO	0x0	rpt_ready KSV FIFO ready. Status flag to indicate that the HDCP hardware has completed the second part of the authentication process (KSV FIFO ready) and has computed the verification value V. It requires no software action and is useful in the debug process.

HDCP2_CONFIG
Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	hdcp2_cd_ovr_value HDCP2 color depth override value
19:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	hdcp2_cd_ovr_en HDCP2 color depth override enable 1'b0: Color Depth value is taken from received GCP packet 1'b1: Color Depth value is controlled by hdcp2_cd_ovr_value
15:13	RO	0x0	reserved
12	RW	0x1	hdcp2_connected HDCP2 connected value
11:10	RO	0x0	reserved
9	RW	0x0	hdcp2_pkt_err_ovr_value HDCP2 AVMUTE packet error override value 1'b0: No packet error 1'b1: Packet error
8	RW	0x0	hdcp2_pkt_err_ovr_en HDCP2 AVMUTE packet error override enable 1'b0: Packet error is determine by BCH error code analysis for each received packet. 1'b1: Packet error is controlled by hdcp2_pkt_err_ovr_value for each received packet.
7:6	RO	0x0	reserved
5	RW	0x0	hdcp2_avmute_ovr_value HDCP2 AVMUTE override value. 1'b0: Not AVMUTE 1'b1: AVMUTE
4	RW	0x0	hdcp2_avmute_ovr_en HDCP2 AVMUTE override enable(debug intended): 1'b0: AVMUTE value is taken from received GCP packet 1'b1: AVMUTE value is controlled by hdcp2_avmute_ovr_value
3	RO	0x0	reserved
2	RW	0x0	hdcp2_switch_ovr_value HDCP2 switch override value 1'b0: HDCP1.4 1'b1: HDCP2
1	RW	0x0	hdcp2_switch_ovr_en HDCP2 switch override enable. 1'b0: HDCP2 versus 1.4 switch controlled automatically by I2C slave received transactions(if previous transaction is for HDCP2 address space then switch points to HDCP2, if previous transaction points to HDCP1.4 address space then switch points to HDCP1.4, by default switch starts in HDCP2) 1'b1: HDCP2 versus 1.4 switch value is controlled by hdcp2_switch_ovr_value.
0	RW	0x0	hdcp2_switch_lck HDCP2 switch lock. 1'b0: Enables you to change the direction of the HDCP2 versus 1.4 switch by using the hdcp2_switch_ovr_en and hdcp2_switch_ ovr _value 1'b1: You can still write to hdcp2_switch_ovr_en and hdcp2_ switch_ovr_value but has no effect over the HDCP2 versus 1.4 switch, that keeps as it has been configured by hdcp2_switch_ ovr_ en and hdcp2_switch_ovr_value at the time, the 1 is write to this bit field. Once you set the value to 1, you can change the value back to 0 only by issuing a main, avpunit,or HDCP sw reset.

HDCP2_STATUS

Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	hdcp2_cd_sts HDCP2 color depth status
11:9	RO	0x0	reserved
8	RO	0x0	hdcp2_avmute_sts HDCP2 AVMUTE status
7	RO	0x0	hdcp2_switch_lck_sts HDCP2 switch lock status
6	RO	0x0	hdcp2_ovr_en_sts HDCP2 override enable status
5	RO	0x0	hdcp2_ovr_val_sts HDCP2 override value status 1'b0: HDCP1.4 1'b1: HDCP2
4	RO	0x0	hdcp2_type_sel_sts HDCP type selection 1'b0: HDCP1.4 1'b1: HDCP2
3:2	RO	0x0	reserved
1	RO	0x0	hdcp2_in_avmute HDCP2 in AVMUTE
0	RO	0x0	hdcp2_decrypted HDCP2 decrypted

HDCP2_ESM_GLOBAL_GPIO_IN

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	hdcp2_esm_global_gpio_in Global General-Purpose inputs to the HDCP2 ESM block.

HDCP2_ESM_GLOBAL_GPIO_OUT

Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	hdcp2_esm_global_gpio_out Global General-Purpose outputs from the HDCP2 ESM block. [0]: Asserted when the ESM has successfully booted and is ready to accept commands. [3:1]: Reserved.

HDCP2_ESM_P0_GPIO_IN

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:1	RW	0x0	hdcp2_esm_p0_gpio_in Port0 General-Purpose inputs to the HDCP2 ESM block.
0	RO	0x0	reserved

HDCP2_ESM_P0_GPIO_OUT

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	hdcp2_esm_p0_gpio_out Global General-Purpose outputs from the HDCP2 ESM block. [0]: Capable [1]: Not_capable [2]: Authenticated [3]: Authentication failed [4]: Link Error(authentication lost) [5]: CSM, Only valid if port is configured as a repeater [6]: Reserved for rx [7]: AKE Init or SKE done [15:8]: Reserved

VIDEO_SYNCGEN_CONFIG6

Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	vproc_frl_syncgen_auto_restart Automatically restart Video Streamer SyncGen algorithm and FIFO clear, after a reconfiguration of horizontal widths has occurred or an underflow/overflow condition.

VIDEO_SYNCGEN_CONFIG7

Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x00fc	vproc_frl_syncgen_fifo_thr_pass Number of additional Video Tri-Bytes, divided by 4, required to buffer after generating Hblank, to cope with Data Flow Metering variations and avoid underflow.

VIDEO_SYNCGEN_CONTROL

Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	vproc_frl_syncgen_fifo_clr_min_p Clear the minimum level reached in Video Streamer FIFO at the time it starts to output a video line.
1	WO	0x0	vproc_frl_syncgen_fifo_clr_max_p Clear the maximum level reached in Video Streamer FIFO at the time it starts to output a video line.
0	WO	0x0	vproc_frl_syncgen_fifo_init_p Clear Video Streamer FIFO and reinitialize Synchronism Generation algorithms.

VIDEO_SYNCGEN_STATUS1

Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vproc_frl_syncgen_sts_fifo_min_lvl Minimum level reached in Video Streamer FIFO at the time it starts to output a video line.
15:0	RO	0x0000	vproc_frl_syncgen_sts_fifo_max_lvl Maximum level reached in Video Streamer FIFO at the time it starts to output a video line.

VIDEO_SYNCGEN_STATUS2

Address: Operational Base + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	vproc_frl_syncgen_sts_hfront_width Hfront width

VIDEO_SYNCGEN_STATUS3
Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	vproc_frl_syncgen_sts_hsync_width Hsync width

VIDEO_SYNCGEN_STATUS4
Address: Operational Base + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	vproc_frl_syncgen_sts_hback_width Hback width

VIDEO_SYNCGEN_STATUS5
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	vproc_frl_syncgen_sts_avg_line_len_diff Average line length difference between calculations.

VIDEO_SYNCGEN_STATUS6
Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	vproc_frl_syncgen_sts_pop_wrd_count_thr Pop word count threshold

VIDEO_SYNCGEN_STATUS7
Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	vproc_frl_syncgen_sts_syncgen_delay Syncgen delay

VIDEO_SYNCGEN_STATUS8
Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vproc_frl_syncgen_sts_vsync_width Vsync width
15:0	RO	0x0000	vproc_frl_syncgen_sts_vfront_width Vfront width

VIDEO_SYNCGEN_STATUS9
Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	vproc_frl_syncgen_sts_vback_width Vback width

VIDEO_CD_CONFIG

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	vproc_cd_delay_nstd_qst Enable color depth reset delay count only when non-reserved CD values are received. 1'b0: Any non-zero Color Depth GCP value counts as valid 1'b1: Only 24, 30, 36, 48bits Color Depth GCP values are counted as valid.
15:12	RW	0x5	vproc_cd_delay_thr Number of GCP packets received before internal color depth value is reset when override mode is enabled. 4'd0: Reserved 4'd1-4'd15: 1 up to 15 GCP packets received
11:9	RO	0x0	reserved
8	RW	0x0	vproc_cd_delay_ovr_en Color Depth timeout value override mode. 1'b0: Reset to 24bits color depth after receiving 5 video fields without color information. 1'b1: Use configured threshold value as the count of video fields to determine color depth timeout state.
7:4	RW	0x4	vproc_cd_ovr_value Color Depth override value 4'b0000-4'b0011: Reserved 4'b0100: 24bits per pixel 4'b0101: 30bits per pixel 4'b0110: 36bits per pixel 4'b0111: 48bits per pixel 4'b1000-4'b1111: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	vproc_cd_ovr_en Enable Color Depth override mode 1'b0: Use automatically detected Color Depth 1'b1: Force Color Depth to configured value

VIDEO_PP_CONFIG

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x05	vproc_pp_diff_thr Pixel Packing Phase discrepancy counter interrupt threshold. Raises interrupt when the discrepancy counter is greater than the value configured in this field. Note: 0xff is not valid configuration and value 0x00 causes interrupt to be triggered in every mismatch.
15:9	RO	0x00	reserved
8	RW	0x0	vproc_pp_diff_on_valid_qst Only count Pixel Packing Phase discrepancies when valid PP values are received.

Bit	Attr	Reset Value	Description
7:4	RW	0x0	vproc_pp_ovr_value Last Packing Phase override value 4'b0000: Pixel Packing Phase 4 4'b0001: Pixel Packing Phase 1 4'b0010: Pixel Packing Phase 2 4'b0011: Pixel Packing Phase 3 4'b0100-4'b1111: Reserved, it is treated as 4'b0000.
3:1	RO	0x0	reserved
0	RW	0x0	vproc_pp_ovr_en Enable Pixel Packing Phase override mode 1'b0: Use the value received in the GCP packet as the last Packing Phase. 1'b1: Use the Pixel Packing Phase override value as the last Packing Phase.

VIDEO_CONFIG1

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	vproc_frl_syncgen_vb_const Enable use of vproc_h*_width register field values to configure a constant Htotal to be used during vblank.
26	RW	0x0	vproc_bypass_48b_mode Enable 48bit mode when video processing is bypassed. 1'b0: 24bits of compressed data sent per-bus 1'b1: 48bits of compressed data sent per-bus
25	RW	0x0	vproc_bypass Enable Video Processing bypass. Note: Must be enabled when Compressed Video Transport is enabled.
24	RW	0x0	vproc_frl_syncgen_dis Disable synchronization signal generation in FRL mode. 1'b0: Synchronization signal generation is enabled when operating in FRL mode 1'b1: Synchronization signal generation is disabled when operating in FRL mode
23	RO	0x0	reserved
22	RW	0x0	vproc_field_vblank_osc_dis Disable vblank oscillation calculation in field status(when receiving Frame Packing and Field Alternative 3D video) and synchronism generation. 1'b0: Assumes non-integer vblank width and accounts for different lengths of active space(or vertical blank) areas. 1'b1: Assumes integer vblank width and that active space(or vertical blank) areas have the same length. Note: Should be set to 1 in VIC 39.
21	RW	0x0	vproc_field_interlaced_en Assume interlaced mode during field status generation in Frame Packing 3D structures. 1'b0: Video is assumed to be progressive 1'b1: Video is assumed to be interlaced
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:17	RW	0x0	vproc_field_pol PVO field polarity control. In normal(positive)polarity mode, the output field indication is as follows. 3'b000: Odd Left frame 3'b001: Odd Right frame 3'b010: Even Left frame 3'b011: Even Right frame When in negative polarity mode the above values are inverted. This field can take the following values 3'b000: Use automatically detected polarity value(positive polarity) 3'b001: Invert automatically detected polarity value(negative polarity) 3'b010: Force output field value to 0 3'b011: Force output field value to 1 3'b100: Force output field value to 2 3'b101: Force output field value to 3 3'b110: Reserved 3'b111: Reserved
16	RW	0x0	vproc_vmute_en Enable video mute mode 1'b0: Video mute is disabled 1'b1: Video mute is enabled and the video output is set to the value configured in vproc_vmute_value_low/high fields
15:14	RO	0x0	reserved
13:12	RW	0x0	vproc_type_ovr_value Video type override value 2'b00: Progressive 2'b01: Interlaced 2'b10: Progressive 3D 2'b11: Interlaced 3D
11:9	RO	0x0	reserved
8	RW	0x0	vproc_type_ovr_en Enable video type override mode
7:4	RW	0x0	vproc_pr_manual_value Pixel Repetition value used in manual mode 4'b0000: No repetition 4'b0001: Pixel data sent 2 times 4'b0010: Pixel data sent 3 times 4'b0011: Pixel data sent 4 times 4'b0100: Pixel data sent 5 times 4'b0101: Pixel data sent 6 times 4'b0110: Pixel data sent 7 times 4'b0111: Pixel data sent 8 times 4'b1000: Pixel data sent 9 times 4'b1001: Pixel data sent 10 times 4'b1010-4'b1111: Reserved, it is treated as 0 value.
3:2	RO	0x0	reserved
1	RW	0x0	vproc_avmute_ignore Ignore AVMUTE control received in GCP 1'b0: AVMUTE value in GCP controls video mute mode 1'b1: AVMUTE value in GCP does not force video mute mode

Bit	Attr	Reset Value	Description
0	RW	0x0	vproc_pr_auto_en Enable Pixel Repetition automatic mode. 1'b0: Use the Pixel Repetition manual value as the valid Pixel Repetition 1'b1: Use the value received in the AVI InfoFrame packet as the valid Pixel Repetition.

VIDEO_CONFIG2

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	vproc_vsync_pol_ovr_value Vertical synchronism polarity override value 1'b0: Negative polarity 1'b1: Positive polarity
18	RW	0x0	vproc_vsync_pol_ovr_en Enable vertical synchronism polarity override.
17	RW	0x0	vproc_hsync_pol_ovr_value Horizontal synchronism polarity override value 1'b0: Negative polarity 1'b1: Positive polarity
16	RW	0x0	vproc_hsync_pol_ovr_en Enable horizontal synchronism polarity override.
15:12	RW	0x0	vproc_3d_fmt_ovr_value 3D video format override value 4'b0000: Frame Packing 4'b0001: Top-and-Bottom 4'b0010: Side-by-Side(half) 4'b0011: Field Alternative 4'b0100: Line Alternative 4'b0101: Side-by-Side(full) 4'b0110: L+depth 4'b0111: L+depth+graphics+graphics-depth 4'b1000: Frame sequential 4'b1001: Dual 3D-Frame sequential combined with Top-and-Bottom 4'b1010: Dual 3D-Frame sequential combined with Side-by-Side(full) 4'b1011: Dual 3D-Top-and-Bottom combined with Side-by-Side(full) 4'b1100-4'b1111: Reserved
11:9	RO	0x0	reserved
8	RW	0x0	vproc_3d_fmt_ovr_en Enable override of 3D video format 1'b0: Video format is automatically detected 1'b1: Video format is overridden
7	RO	0x0	reserved
6:4	RW	0x0	vproc_fmt_ovr_value Video format override value. 3'b000: RGB 4:4:4 3'b001: YCbCr 4:2:2 3'b010: YCbCr 4:4:4 3'b011: YCbCr 4:2:0 3'b100-3'b111: Reserved, it is treated as 3'b000
3:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	vproc_fmt_ovr_en Enable override of video format. 1'b0: Video format is automatically detected 1'b1: Video format is overridden

VIDEO_MUTE_VALUE_H

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	vproc_vmute_value_high_qst Video output value when Video Mute is enabled(most significant [47:32] bits)

VIDEO_MUTE_VALUE_L

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vproc_vmute_value_low_qst Video output value when Video Mute is enabled(least significant [31:0] bits) Note: This configuration is only valid after vproc_vmute_value_high is written.

VIDEO_CONTROL

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	vproc_pp_diff_clr_p Clear Pixel Packing Phase discrepancy counter.

VIDEO_STATUS

Address: Operational Base + offset (0x043C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	vproc_pp_diff_cnt Pixel Packing Phase discrepancy counter value. Reflects the number of times the deep color mode internal last Packing Phase value does not match the corresponding value contained in a received GCP packet.
7	RO	0x0	reserved
6:4	RO	0x0	vproc_pp_current Pixel Packing Phase value of last pixel of last Video Data Period.
3:0	RO	0x0	vproc_cd_current Current active Color Depth value.

VIDEO_FVA_VRR_CONFIG

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	vproc_active_space_qst Number of lines in Active Space when FVA and/or VRR are enabled. Field detection uses the measured Vblank value when this field is zero. This field must be configured when VRR_EN and/or FVA_EN of Video Timing Extended Metadata Data Set are enabled for the field detection mechanism to work correctly in all 3D modes.

VIDEO_STREAMER_CONFIG2

Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	vstream_fifo_almost_full_thr Video Streamer FIFO almost full threshold configuration.
15:0	RW	0x0000	vstream_fifo_almost_empty_thr Video Streamer FIFO almost empty threshold configuration.

AUDIO_FIFO_CONFIG

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	afifo_bypass_en When enabled, audio samples from the Audio Generator do not pass through the external FIFO memory. 1'b0: Audio samples from the Audio Generator are stored in FIFO before being used. 1'b1: Audio samples from the Audio Generator are used directly by the audio interfaces without passing through the FIFO. This field should only be enabled when there is no tmdsqpclk available.
1	RW	0x0	afifo_fill_stop When enabled, the Audio FIFO does not push any new audio samples into memory 1'b0: Audio samples are stored as they are received 1'b1: Received audio samples are ignored
0	RW	0x0	afifo_fill_restart Automatically restart Audio FIFO filling mode after it becomes empty, following a FIFO underflow event. 1'b0: After an underflow event, the FIFO needs to be restarted using afifo_init_p field. 1'b1: After an underflow event, the FIFO automatically restarts storing new audio samples as they are received. Note:After an overflow event is triggered, the FIFO must be restarted using afifo_init_p field even after underflow condition is met.

AUDIO_FIFO_CONTROL

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	afifo_clr_max_p Clear long term audio FIFO maximum fill status.
1	WO	0x0	afifo_clr_min_p Clear long term audio FIFO minimum fill status.
0	WO	0x0	afifo_init_p Audio FIFO initialization pulse When asserted, the Audio FIFO address pointers are reset and any internal blocks that receive data from the Audio FIFO are restarted.

AUDIO_FIFO_THR_PASS

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x090	afifo_thr_pass_qst Audio FIFO pass threshold level(real FIFO threshold is configured value x4)

AUDIO_FIFO_THR

Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x020	afifo_thr_low_qst Audio FIFO low threshold level(real FIFO threshold is configured value x4).
15:10	RO	0x00	reserved
9:0	RW	0x160	afifo_thr_high_qst Audio FIFO high threshold level(real FIFO threshold is configured value x4).

AUDIO_FIFO_MUTE_THR

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x008	afifo_thr_mute_low_qst Audio FIFO mute low threshold level(real FIFO threshold is configured value x4).
15:10	RO	0x00	reserved
9:0	RW	0x178	afifo_thr_mute_high_qst Audio FIFO mute high threshold level(real FIFO threshold is configured value x4).

AUDIO_FIFO_STATUS1

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	afifo_fill_state_max Minimum fill level reached by Audio FIFO after pass threshold is reached.
15:0	RO	0xffff	afifo_fill_state_min Maximum fill level reached by Audio FIFO after pass threshold is reached.

AUDIO_FIFO_STATUS2

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	afifo_underflow_st Indicates that Audio FIFO is in underflow
24	RO	0x0	afifo_overflow_st Indicates that Audio FIFO is in overflow
23:16	RO	0x00	reserved
15:0	RO	0x0000	afifo_fill_state Current Audio FIFO fill level

AUDIO_PROC_CONFIG0

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	speaker_alloc_ovr_en Audio speaker/channel allocation override enable
15:14	RO	0x0	reserved
13	RW	0x0	aud_mute_ovr_value Audio mute flag override value
12	RW	0x0	aud_mute_ovr_en Audio mute flag override enable.
11:10	RO	0x0	reserved
9	RW	0x0	pao_rate_ovr_value Parallel Audio Output rate mode override value. 1'b0: Output rate is equal to sampling frequency(fs) 1'b1: Output rate is 128/56 of the sampling frequency(fs*128/56)
8	RW	0x0	pao_rate_ovr_en Parallel Audio Output rate mode override enable.
7:6	RO	0x0	reserved
5	RW	0x0	aud_chan_spread_en Enable using the four output channels simultaneously to transmit audio samples from a single channel. 1'b0: Audio samples sent in a single channel 1'b1: Audio samples sent in the four channels Only applicable in the following scenarios: (1)DST and HBR audio streams (2)Audio Sample Packet-Layout 0 (3)One Bit Audio-Layout 0
4	RW	0x0	i2s_bpcuv_en Enable I2S bpcuv mode
3	RO	0x0	reserved
2	RW	0x0	spdif_en Enable S/PDIF serial audio output
1	RW	0x0	i2s_en Enable I2S serial audio output
0	RW	0x0	pao_en Enable parallel audio output

AUDIO_PROC_CONFIG1

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	aud_force_pll4x_en Force PLL 4x multiplication output control signal 1'b0: Value not forced 1'b1: Oaud_pll4x force to value 1'b1
12	RO	0x0	reserved
11:10	RW	0x0	chstatus_select Channel Status Packet Selector for 3D Audio. If 3D Audio is received, the Channel Status Register save the 8 Channels of the corresponding Packet. 2'b00: Packet1 2'b01: Packet2 2'b10: Packet3 2'b11: Packet4
9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8:4	RW	0x00	auddet_thr Audio type detection is only valid after the number of consecutive received audio packets is at least the value configured in this field. 5'b0000: Reserved 5'b0001-5'b11111: Number of consecutive audio packets received, required to consider audio type valid.
3:2	RO	0x0	reserved
1	RW	0x0	aud_layout_ovr_value Audio layout override value
0	RW	0x0	aud_layout_ovr_en Audio layout override enable

AUDIO_PROC_CONFIG2

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x1	afifo_thr_pass_demutemask_n Audio FIFO pass threshold demute mask 1'b0: Audio FIFO pass threshold does not contribute for de-asserting the mute signal 1'b1: Audio FIFO pass threshold contributes for de-asserting the mute signal

Bit	Attr	Reset Value	Description
23:20	RW	0xf	sample_flat_demutemask_n Sample Flat demute mask 4'b0000: Sample Flat does not contribute for de-asserting the mute signal 4'b0001: Sample Flat of channel 0 contributes for de-asserting the mute signal 4'b0010: Sample Flat of channel 1 contributes for de-asserting the mute signal 4'b0011: Sample Flat of channel 0 and 1 contributes for de-asserting the mute signal 4'b0100: Sample Flat of channel 2 contributes for de-asserting the mute signal 4'b0101: Sample Flat of channel 0 and 2 contributes for de-asserting the mute signal 4'b0110: Sample Flat of channel 1 and 2 contributes for de-asserting the mute signal 4'b0111: Sample Flat of channel 0, 1, and 2 contributes for de-asserting the mute signal 4'b1000: Sample Flat of channel 3 contributes for de-asserting the mute signal 4'b1001: Sample Flat of channel 0 and 3 contributes for de-asserting the mute signal 4'b1010: Sample Flat of channel 1 and 3 contributes for de-asserting the mute signal 4'b1011: Sample Flat of channel 0, 1, and 3 contributes for de-asserting the mute signal 4'b1100: Sample Flat of channel 2 and 3 contributes for de-asserting the mute signal 4'b1101: Sample Flat of channel 0, 2, and 3 contributes for de-asserting the mute signal 4'b1110: Sample Flat of channel 1, 2, and 3 contributes for de-asserting the mute signal 4'b1111: Sample Flat of channel 0, 1, 2, and 3 contributes for de-asserting the mute signal
19:17	RO	0x0	reserved
16	RW	0x1	avmute_demutemask_n AVMUTE demute mask 1'b0: AVMUTE does not contribute for de-asserting the mute signal 1'b1: AVMUTE contributes for de-asserting the mute signal
15:10	RO	0x00	reserved
9	RW	0x1	afifo_thr_mute_low_mutemask_n Audio FIFO mute low threshold mute mask 1'b0: Audio FIFO mute low threshold does not contribute for de-asserting the mute signal 1'b1: Audio FIFO mute low threshold contributes for de-asserting the mute signal
8	RW	0x1	afifo_thr_mute_high_mutemask_n Audio FIFO mute high threshold mute mask 1'b0: Audio FIFO mute high threshold does not contribute for asserting the mute signal 1'b1: Audio FIFO mute high threshold contributes for asserting the mute signal

Bit	Attr	Reset Value	Description
7:4	RW	0xf	sample_flat_mutemask_n Sample Flat mute mask 4'b0000: Sample Flat does not contribute for asserting the mute signal 4'b0001: Sample Flat of channel 0 contributes for asserting the mute signal 4'b0010: Sample Flat of channel 1 contributes for asserting the mute signal 4'b0011: Sample Flat of channel 0 and 1 contributes for asserting the mute signal 4'b0100: Sample Flat of channel 2 contributes for asserting the mute signal 4'b0101: Sample Flat of channel 0 and 2 contributes for asserting the mute signal 4'b0110: Sample Flat of channel 1 and 2 contributes for asserting the mute signal 4'b0111: Sample Flat of channel 0, 1, and 2 contributes for asserting the mute signal 4'b1000: Sample Flat of channel 3 contributes for asserting the mute signal 4'b1001: Sample Flat of channel 0 and 3 contributes for asserting the mute signal 4'b1010: Sample Flat of channel 1 and 3 contributes for asserting the mute signal 4'b1011: Sample Flat of channel 0, 1, and 3 contributes for asserting the mute signal 4'b1100: Sample Flat of channel 2 and 3 contributes for asserting the mute signal 4'b1101: Sample Flat of channel 0, 2, and 3 contributes for asserting the mute signal 4'b1110: Sample Flat of channel 1, 2, and 3 contributes for asserting the mute signal 4'b1111: Sample Flat of channel 0, 1, 2, and 3 contributes for asserting the mute signal
3:2	RO	0x0	reserved
1	RW	0x1	aud_fmt_chg_mutemask_n Audio format change mute mask 1'b0: Audio format change detection does not contribute for asserting the mute signal 1'b1: Audio format change detection contributes for asserting the mute signal
0	RW	0x1	avmute_mutemask_n AVMUTE mute mask 1'b0: AVMUTE does not contribute for asserting the mute signal 1'b1: AVMUTE contributes for asserting the mute signal

AUDIO_PROC_CONFIG3

Address: Operational Base + offset (0x048C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	speaker_alloc_ovr_value Speaker Allocation Override Value. Each bit defines one channel to be outputed. (1)If Audio Packets received are 3D Audio Packets then the 32bit are used to define up to 32 channels (2)If Audio Packets received are not 3D Audio Packets then the only the 8 LSB are used to override the Speaker Allocation

AUDIO_PROC_STATUS1

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	aud_speaker_alloc Currently active audio Speaker Allocation value
23:21	RO	0x0	reserved
20:17	RO	0x0	aud_sample_present Contains the sample_present value of AS, OBA, MSAS, MSOBA audio packets. Note: On remaining audio packet types this field is set to 4'b1111.
16:13	RO	0x0	aud_sample_flat Contains the sample_flat(or samples_invalid) value of AS, OBA, MSAS, MSOBA, and DST audio packets. Note1: In DST audio packets, the sample_invalid value is replicated in the 4bits of this field. Note2: On remaining audio packet types this field is set to 4'b0000 Note3: If the Audio Generator is used when the HDMI_QP_RX_ASO interface is defined, this register is set with the sample_flat that is defined on the agen_sample_flat field.
12:9	RO	0x0	reserved
8	RO	0x1	aud_mute_st Indicates current audio mute status 1'b0: Mute disabled 1'b1: Mute enabled
7:4	RO	0x0	reserved
3	RO	0x0	aud_layout Currently active layout(when applicable) 1'b0: Layout 0 1'b1: Layout 1
2:0	RO	0x0	aud_fmt_st Currently active Audio Packet Format value 3'b000: Audio Sample Packet 3'b001: One Bit Audio Sample Packet 3'b010: DST Audio Packet 3'b011: High-Bitrate(HBR) Audio Stream Packet 3'b100: Multi-Stream Audio Sample Packet 3'b101: One Bit Multi-Stream Audio Sample Packet 3'b110: 3D Audio Sample Packet 3'b111: 3D One Bit Audio

AUDIO_PROC_STATUS2

Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_32ch_alloc Currently active Speaker Allocation received for 3D Audio(up to 32 channels) (1)If the Audio InfoFrame is received then the Speaker Allocation is defined by Speaker Mask or Channel Index, respectively. (2)If the Audio Metadata Packet is received then the Speaker Allocation is defined as {20'd0, ACAT, CA}.

AUDIO_PROC_CHSTAT_SP0_L1

Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_left_3_0 Channel Status bytes 3 to 0 from Sub Packet 0, Left channel.

AUDIO_PROC_CHSTAT_SP0_L2
Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_left_7_4 Channel Status bytes 7 to 4 from Sub Packet 0, Left channel.

AUDIO_PROC_CHSTAT_SP0_L3
Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_left_11_8 Channel Status bytes 11 to 8 from Sub Packet 0, Left channel.

AUDIO_PROC_CHSTAT_SP0_L4
Address: Operational Base + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_left_15_12 Channel Status bytes 15 to 12 from Sub Packet 0, Left channel.

AUDIO_PROC_CHSTAT_SP0_L5
Address: Operational Base + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_left_19_16 Channel Status bytes 19 to 16 from Sub Packet 0, Left channel.

AUDIO_PROC_CHSTAT_SP0_L6
Address: Operational Base + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_left_23_20 Channel Status bytes 23 to 20 from Sub Packet 0, Left channel.

AUDIO_PROC_CHSTAT_SP0_R1
Address: Operational Base + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_right_3_0 Channel Status bytes 3 to 0 from Sub Packet 0, Right channel.

AUDIO_PROC_CHSTAT_SP0_R2
Address: Operational Base + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_right_7_4 Channel Status bytes 7 to 4 from Sub Packet 0, Right channel.

AUDIO_PROC_CHSTAT_SP0_R3
Address: Operational Base + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_right_11_8 Channel Status bytes 11 to 8 from Sub Packet 0, Right channel.

AUDIO_PROC_CHSTAT_SP0_R4
Address: Operational Base + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_right_15_12 Channel Status bytes 15 to 12 from Sub Packet 0, Right channel.

AUDIO_PROC_CHSTAT_SP0_R5
Address: Operational Base + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_right_19_16 Channel Status bytes 19 to 16 from Sub Packet 0, Right channel.

AUDIO_PROC_CHSTAT_SP0_R6
Address: Operational Base + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp0_right_23_20 Channel Status bytes 23 to 20 from Sub Packet 0, Right channel.

AUDIO_PROC_CHSTAT_SP1_L1
Address: Operational Base + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_left_3_0 Channel Status bytes 3 to 0 from Sub Packet 1, Left channel.

AUDIO_PROC_CHSTAT_SP1_L2
Address: Operational Base + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_left_7_4 Channel Status bytes 7 to 4 from Sub Packet 1, Left channel.

AUDIO_PROC_CHSTAT_SP1_L3
Address: Operational Base + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_left_11_8 Channel Status bytes 11 to 8 from Sub Packet 1, Left channel.

AUDIO_PROC_CHSTAT_SP1_L4
Address: Operational Base + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_left_15_12 Channel Status bytes 15 to 12 from Sub Packet 1, Left channel.

AUDIO_PROC_CHSTAT_SP1_L5
Address: Operational Base + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_left_19_16 Channel Status bytes 19 to 16 from Sub Packet 1, Left channel.

AUDIO_PROC_CHSTAT_SP1_L6
Address: Operational Base + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_left_23_20 Channel Status bytes 23 to 20 from Sub Packet 1, Left channel.

AUDIO_PROC_CHSTAT_SP1_R1
Address: Operational Base + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_right_3_0 Channel Status bytes 3 to 0 from Sub Packet 1, Right channel.

AUDIO_PROC_CHSTAT_SP1_R2
Address: Operational Base + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_right_7_4 Channel Status bytes 7 to 4 from Sub Packet 1, Right channel.

AUDIO_PROC_CHSTAT_SP1_R3
Address: Operational Base + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_right_11_8 Channel Status bytes 11 to 8 from Sub Packet 1, Right channel.

AUDIO_PROC_CHSTAT_SP1_R4
Address: Operational Base + offset (0x04F4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_right_15_12 Channel Status bytes 15 to 12 from Sub Packet 1, Right channel.

AUDIO_PROC_CHSTAT_SP1_R5
Address: Operational Base + offset (0x04F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_right_19_16 Channel Status bytes 19 to 16 from Sub Packet 1, Right channel.

AUDIO_PROC_CHSTAT_SP1_R6
Address: Operational Base + offset (0x04FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp1_right_23_20 Channel Status bytes 23 to 20 from Sub Packet 1, Right channel.

AUDIO_PROC_CHSTAT_SP2_L1
Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_left_3_0 Channel Status bytes 3 to 0 from Sub Packet 2, Left channel.

AUDIO_PROC_CHSTAT_SP2_L2
Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_left_7_4 Channel Status bytes 7 to 4 from Sub Packet 2, Left channel.

AUDIO_PROC_CHSTAT_SP2_L3
Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_left_11_8 Channel Status bytes 11 to 8 from Sub Packet 2, Left channel.

AUDIO_PROC_CHSTAT_SP2_L4
Address: Operational Base + offset (0x050C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_left_15_12 Channel Status bytes 15 to 12 from Sub Packet 2, Left channel.

AUDIO_PROC_CHSTAT_SP2_L5
Address: Operational Base + offset (0x0510)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_left_19_16 Channel Status bytes 19 to 16 from Sub Packet 2, Left channel.

AUDIO_PROC_CHSTAT_SP2_L6
Address: Operational Base + offset (0x0514)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_left_23_20 Channel Status bytes 23 to 20 from Sub Packet 2, Left channel.

AUDIO_PROC_CHSTAT_SP2_R1
Address: Operational Base + offset (0x0518)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_right_3_0 Channel Status bytes 3 to 0 from Sub Packet 2, Right channel.

AUDIO_PROC_CHSTAT_SP2_R2
Address: Operational Base + offset (0x051C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_right_7_4 Channel Status bytes 7 to 4 from Sub Packet 2, Right channel.

AUDIO_PROC_CHSTAT_SP2_R3
Address: Operational Base + offset (0x0520)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_right_11_8 Channel Status bytes 11 to 8 from Sub Packet 2, Right channel.

AUDIO_PROC_CHSTAT_SP2_R4
Address: Operational Base + offset (0x0524)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_right_15_12 Channel Status bytes 15 to 12 from Sub Packet 2, Right channel.

AUDIO_PROC_CHSTAT_SP2_R5
Address: Operational Base + offset (0x0528)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_right_19_16 Channel Status bytes 19 to 16 from Sub Packet 2, Right channel.

AUDIO_PROC_CHSTAT_SP2_R6
Address: Operational Base + offset (0x052C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp2_right_23_20 Channel Status bytes 23 to 20 from Sub Packet 2, Right channel.

AUDIO_PROC_CHSTAT_SP3_L1
Address: Operational Base + offset (0x0530)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_left_3_0 Channel Status bytes 3 to 0 from Sub Packet 3, Left channel.

AUDIO_PROC_CHSTAT_SP3_L2
Address: Operational Base + offset (0x0534)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_left_7_4 Channel Status bytes 7 to 4 from Sub Packet 3, Left channel.

AUDIO_PROC_CHSTAT_SP3_L3
Address: Operational Base + offset (0x0538)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_left_11_8 Channel Status bytes 11 to 8 from Sub Packet 3, Left channel.

AUDIO_PROC_CHSTAT_SP3_L4
Address: Operational Base + offset (0x053C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_left_15_12 Channel Status bytes 15 to 12 from Sub Packet 3, Left channel.

AUDIO_PROC_CHSTAT_SP3_L5
Address: Operational Base + offset (0x0540)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_left_19_16 Channel Status bytes 19 to 16 from Sub Packet 3, Left channel.

AUDIO_PROC_CHSTAT_SP3_L6
Address: Operational Base + offset (0x0544)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_left_23_20 Channel Status bytes 23 to 20 from Sub Packet 3, Left channel.

AUDIO_PROC_CHSTAT_SP3_R1
Address: Operational Base + offset (0x0548)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_right_3_0 Channel Status bytes 3 to 0 from Sub Packet 3, Right channel.

AUDIO_PROC_CHSTAT_SP3_R2
Address: Operational Base + offset (0x054C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_right_7_4 Channel Status bytes 7 to 4 from Sub Packet 3, Right channel.

AUDIO_PROC_CHSTAT_SP3_R3
Address: Operational Base + offset (0x0550)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_right_11_8 Channel Status bytes 11 to 8 from Sub Packet 3, Right channel.

AUDIO_PROC_CHSTAT_SP3_R4
Address: Operational Base + offset (0x0554)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_right_15_12 Channel Status bytes 15 to 12 from Sub Packet 3, Right channel.

AUDIO_PROC_CHSTAT_SP3_R5

Address: Operational Base + offset (0x0558)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_right_19_16 Channel Status bytes 19 to 16 from Sub Packet 3, Right channel.

AUDIO_PROC_CHSTAT_SP3_R6

Address: Operational Base + offset (0x055C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aud_chstatus_sp3_right_23_20 Channel Status bytes 23 to 20 from Sub Packet 3, Right channel.

SCDC_CONFIG

Address: Operational Base + offset (0x0580)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rr_ifflags_alreadyset Read Request sent if RR_Enable bit is set with any of the Update Flags already. 1'b1: Read Request sent when RR_Enable bit is set and any of the Update Flags is already. 1'b0: Read Request sent only when RR_Enable is previous active and any of the Update Flags transitions from 0 to 1.
4:3	RO	0x0	reserved
2	RW	0x0	standby Sink is placed into standby or is unpowered.
1	RW	0x0	hpdlow Hot Plug Detect pin has voltage = low for 100ms or more
0	RW	0x0	powerprovided Power provided 1'b1: +5V Power Signal is provided by the Source 1'b0: +5V Power Signal is not provided by the Source

SCDC_CONTROL

Address: Operational Base + offset (0x0584)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	frl_start_ovr_p SCDC FRL Link Training-FRL_start override

SCDC_REGBANK_STATUS0

Address: Operational Base + offset (0x0588)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	frl_start_sts FRL_start Update Flag status. Remains set(=1) until a new Link Training process occurs-unlike scdc_frl_start, this register field is not cleared by Source.
27:15	RO	0x0000	reserved
14	RO	0x0	scdc_rsed_update SCDC Update Flags register-RSED_Update

Bit	Attr	Reset Value	Description
13	RO	0x0	scdc_flt_update SCDC Update Flags register-FLT_update
12	RO	0x0	scdc_frl_start SCDC Update Flags register-FRL_start
11	RO	0x0	scdc_source_test_update SCDC Update Flags register-Source_Test_Update
10	RO	0x0	scdc_rrtest SCDC Update Flags register-RR Test
9	RO	0x0	scdc_cedupdate SCDC Update Flags register-CED_Update
8	RO	0x0	scdc_statusupdate SCDC Update Flags register-Status_Update
7:0	RO	0x00	scdc_sourceversion SCDC Source Version/Revision register-Source Version

SCDC_REGBANK_STATUS1

Address: Operational Base + offset (0x058C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	scdc_scramb_status SCDC Status register-Scrambling_Status
7:2	RO	0x00	reserved
1	RO	0x0	scdc_tmdsbitclkratio SCDC_TMDS Configuration register-TMDS_Bit_Clock_ratio
0	RO	0x0	scdc_scramb_en SCDC TMDS Configuration register-Scrambling_Enable

SCDC_REGBANK_STATUS2

Address: Operational Base + offset (0x0590)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	scdc_ffe_levels SCDC Configuration register-FFE_Levels
11:8	RO	0x0	scdc_frl_rate SCDC configuration register-FRL_Rate
7:2	RO	0x00	reserved
1	RO	0x0	scdc_flt_no_retrain SCDC Configuration register-FLT_no_retrain
0	RO	0x0	scdc_rrenable SCDC Configuration register-RR_Enable

SCDC_REGBANK_STATUS3

Address: Operational Base + offset (0x0594)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	scdc_ch2locked SCDC Status Flags register-Ch2_Locked
2	RO	0x0	scdc_ch1locked SCDC Status Flags register-Ch1_Locked
1	RO	0x0	scdc_ch0locked SCDC Status Flags register-Ch0_Locked
0	RO	0x0	scdc_clockdetected SCDC Status Flags register-Clock_Detected

SCDC_REGBANK_STATUS4

Address: Operational Base + offset (0x0598)

Bit	Attr	Reset Value	Description
31	RO	0x0	scdc_err_det1_valid SCDC CED registers-Channel 1 Character Error Valid
30:16	RO	0x0000	scdc_err_det1 SCDC CED registers-Channel 1 Character Error Count
15	RO	0x0	scdc_err_det0_valid SCDC CED registers-Channel 0 Character Error Valid
14:0	RO	0x0000	scdc_err_det0 SCDC CED registers-Channel 0 Character Error Count

SCDC_REGBANK_STATUS5

Address: Operational Base + offset (0x059C)

Bit	Attr	Reset Value	Description
31	RO	0x0	scdc_erdet_lane0_valid SCDC CED registers-Lane 0 Character Error valid
30:16	RO	0x0000	scdc_erdet_lane0 SCDC CED registers-Lane 0 Character Error Count
15	RO	0x0	scdc_err_det2_valid SCDC CED registers-Channel 2 Character Error Valid
14:0	RO	0x0000	scdc_err_det2 SCDC CED registers-Channel 2 Character Error Count

SCDC_REGBANK_STATUS8

Address: Operational Base + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	scdc_testreadreq SCDC Test Configuration register-TestReadRequest
6:0	RO	0x00	scdc_testreadreqdelay SCDC Test Configuration register-TestReadRequestDelay

SCDC_REGBANK_MS_STATUS0

Address: Operational Base + offset (0x05AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	manufacturspecificwr0 SCDC Manufacturer Specific Registers-ManufacturerSpecific_Wr[31:0]

SCDC_REGBANK_MS_STATUS1

Address: Operational Base + offset (0x05B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	manufacturspecificwr1 SCDC Manufacturer Specific Registers-ManufacturerSpecific_Wr[63:32]

SCDC_REGBANK_MS_STATUS2

Address: Operational Base + offset (0x05B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	manufacturspecificwr2 SCDC Manufacturer Specific Registers-ManufacturerSpecific_Wr[95:64]

SCDC_REGBANK_MS_STATUS3

Address: Operational Base + offset (0x05B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	manufacturspecificwr3 SCDC Manufacturer Specific Registers-ManufacturerSpecific_Wr[127:96]

SCDC_REGBANK_MS_STATUS4

Address: Operational Base + offset (0x05BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	manufacturspecificwr4 SCDC Manufacturer Specific Registers-ManufacturerSpecific_Wr[143:128]

SCDC_REGBANK_CONFIG0

Address: Operational Base + offset (0x05C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	scdc_sinkversion_qst SCDC Sink Version register - Sink Version

SCDC_REGBANK_CONFIG1

Address: Operational Base + offset (0x05C4)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	manufacturer_oui_qst SCDC Manufacturer Specific registers-Manufacturer_OUI
7:0	RO	0x00	reserved

SCDC_REGBANK_CONFIG2

Address: Operational Base + offset (0x05C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	deviceid_string0_qst SCDC Manufacturer Specific registers-Device ID_String LSBytes.

SCDC_REGBANK_CONFIG3

Address: Operational Base + offset (0x05CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	deviceid_string1_qst SCDC Manufacturer Specific registers-Device ID_String MSBytes.

SCDC_REGBANK_CONFIG4

Address: Operational Base + offset (0x05D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	deviceid_sw_minorrev_qst SCDC Manufacturer Specific registers-Device ID Software Minor Revision.
15:8	RW	0x00	deviceid_sw_majorrev_qst SCDC Manufacturer Specific registers-Device ID Software Major Revision.
7:4	RW	0x0	deviceid_majorrev_qst SCDC Manufacturer Specific registers-Device ID Hardware Major Revision.
3:0	RW	0x0	deviceid_minorrev_qst SCDC Manufacturer Specific registers-Device ID Hardware Minor Revision.

SCDC_REGBANK_CONFIG5

Address: Operational Base + offset (0x05D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	manufacturspecific0_qst SCDC Manufacturer Specific registers-ManufacturerSpecific_Rd[31:0].

SCDC_REGBANK_CONFIG6

Address: Operational Base + offset (0x05D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	manufacturspecific1_qst SCDC Manufacturer Specific registers-ManufacturerSpecific_Rd[63:32].

SCDC_REGBANK_CONFIG7

Address: Operational Base + offset (0x05DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	manufacturspecific2_qst SCDC Manufacturer Specific registers-ManufacturerSpecific_Rd[95:64].

SCDC_REGBANK_CONFIG8

Address: Operational Base + offset (0x05E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	manufacturspecific3_qst SCDC Manufacturer Specific registers-ManufacturerSpecific_Rd[127:96].

VPG_CONFIG0

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	vpg_connection_sel_qst VPG output connection selection 2'b00: Disconnected 2'b01: Connected to HDCP 2'b10: Connected to Video Processor 2'b11: Connected to PVO Interface Note: When connected to HDCP or Video Processor, the vpg is configured to 8bit(without deep color mode).
27:25	RO	0x0	reserved
24	RW	0x0	vpg_colorrange_qst Color range 1'b0: Full range 1'b1: Limited range
23:20	RW	0x0	vpg_colordepth_qst Video color depth 4'b0000-4'b0011: Reserved, 24bits color depth if selected 4'b0100: 24bits(8 per component) 4'b0101: 30bits(10 per component) 4'b0110: 36bits(12 per component) 4'b0111: 48bits(16 per component) 4'b1000-4'b1111: Reserved, 24bits color depth if selected

Bit	Attr	Reset Value	Description
19:16	RW	0x0	vpg_prepetition_qst Pixel repetition support 4'b0000: No pixel repetition 4'b0001-4'b1001: pixel send 1 + vpg_prepetition
15	RO	0x0	reserved
14:12	RW	0x0	vpg_colorimetry_qst Video colorimetry 3'b000: RGB 4:4:4 3'b001: YCC 4:2:2 3'b010: YCC 4:4:4 3'b011: YCC 4:2:0 3'b100-3'b111: Reserved, RGB 4:4:4 if selected
11:10	RO	0x0	reserved
9	RW	0x0	vpg_vblankosc_qst Vertical blank length oscillation
8	RW	0x0	vpg_ilace_qst Interlaced/Progressive video 1'b0: Progressive 1'b1: Interlaced
7	RO	0x0	reserved
6	RW	0x0	vpg_vs_pol_qst Vertical sync signal polarity 1'b0: Negative polarity 1'b1: Positive polarity
5	RW	0x0	vpg_hs_pol_qst Horizontal sync signal polarity 1'b0: Negative polarity 1'b1: Positive polarity
4	RW	0x1	vpg_de_pol_qst Debug field, data enable signal polarity 1'b0: Negative polarity 1'b1: Positive polarity
3:1	RO	0x0	reserved
0	RW	0x0	vpg_en Enable video pattern generator 1'b0: Disable 1'b1: Enable

VPG_CONFIG1

Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	vpg_patt_mode_qst Video generator pattern mode 2'b00: Color spectrum 2'b01: Gray ramp 2'b10: Chess board 2'b11: Chess board
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	vpg_3d_struct_qst 3D Structure 4'b0000: Reserved, video in 2D mode if selected 4'b0001: Frame packing mode 4'b0010: Field alternative mode 4'b0011: Line alternative mode 4'b0100: Side-by-side full mode 4'b0101: L+depth mode 4'b0110: L+depth+GFX+G-depth mode 4'b0111: Top-and-Bottom 4'b1000: Side-by-side half mode 4'b1001-4'b1111: Reserved, video in 2D mode if selected.
3:2	RO	0x0	reserved
1	RW	0x0	vpg_3d_frameseq_qst Signals video generator that the 3D frame sequential is the configured 3D video mode.
0	RW	0x0	vpg_3d_en_qst 3D video mode enable

VPG_HAHB_CONFIG

Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00a0	vpg_hblank_qst Horizontal blank length
15:14	RO	0x0	reserved
13:0	RW	0x0280	vpg_hactive_qst Horizontal active length

VPG_HDHW_CONFIG

Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x060	vpg_hwidth_qst Horizontal sync width
15:13	RO	0x0	reserved
12:0	RW	0x0010	vpg_hfront_qst Horizontal sync front

VPG_VAVB_CONFIG

Address: Operational Base + offset (0x0710)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x02d	vpg_vblank_qst Vertical blank length
15:13	RO	0x0	reserved
12:0	RW	0x01e0	vpg_vactive_qst Vertical active length

VPG_VDVW_CONFIG

Address: Operational Base + offset (0x0714)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

Bit	Attr	Reset Value	Description
22:16	RW	0x02	vpg_vwidth_qst Vertical sync width
15:9	RO	0x00	reserved
8:0	RW	0x00a	vpg_vfront_qst Vertical sync front

VPG_CB_LENGTH_CONFIG

Address: Operational Base + offset (0x0718)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	vpg_cb_height_qst Chess board pattern tile height
15:10	RO	0x00	reserved
9:0	RW	0x000	vpg_cb_width_qst Chess board pattern tile width

VPG_CB_COLORA_L

Address: Operational Base + offset (0x071C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vpg_cb_colora_low_qst Chess board pattern tile color a 32 least significant bits

VPG_CB_COLORA_H

Address: Operational Base + offset (0x0720)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	vpg_cb_colora_high_qst Chess board pattern tile color a 16 most significant bits

VPG_CB_COLORB_L

Address: Operational Base + offset (0x0724)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vpg_cb_colorb_low_qst Chess board pattern tile color b 32 least significant bits

VPG_CB_COLORB_H

Address: Operational Base + offset (0x0728)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	vpg_cb_colorb_high_qst Chess board pattern tile color b 16 most significant bits

AUDIO_GEN_CONFIG0

Address: Operational Base + offset (0x0740)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	agen_speaker_alloc Audio generator speaker/channel allocation
7:6	RO	0x0	reserved
5	RW	0x0	agen_sample_flat Audio generator Sample Flat value

Bit	Attr	Reset Value	Description
4	RW	0x0	agen_layout Audio generator layout 1'b0: Layout 0 1'b1: Layout 1
3:1	RO	0x0	reserved
0	RW	0x0	agen_en Enable audio generator

AUDIO_GEN_CONFIG1

Address: Operational Base + offset (0x0744)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	agen_freq_fs Audio sample frequency(Hz) Supported values 5'b00000: 32000 5'b00001: 44100 5'b00010: 48000 5'b00011: 64000 5'b00100: 88200 5'b00101: 96000 5'b00110: 128000 5'b00111: 176400 5'b01000: 192000 5'b01001: 256000 5'b01010: 352800 5'b01011: 384000 5'b01100: 512000 5'b01101: 705600 5'b01110: 768000 5'b01111: 1024000 5'b10000: 1411200 5'b10001: 1536000 5'b10010-5'b11111: Reserved

AUDIO_GEN_CONFIG2

Address: Operational Base + offset (0x0748)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	iec_chsts_categorycode_qst Audio Generator Channel Status Category Code value
7	RO	0x0	reserved
6:4	RW	0x0	iec_chsts_lpcmmode_qst Audio Generator Channel Status Linear PCM Audio Mode
3	RO	0x0	reserved
2	RW	0x0	iec_chsts_copyright_qst Audio Generator Channel Status Copyright value
1	RW	0x0	iec_udata_right_qst Audio Generator Right channel user data
0	RW	0x0	iec_udata_left_qst Audio Generator Left channel user data

AUDIO_GEN_CONFIG3

Address: Operational Base + offset (0x074C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	iec_chsts_cgmsa_qst Audio Generator Channel Status CGMS-A value
29:28	RW	0x0	iec_chsts_clkaccuracy_qst Audio Generator Channel Status Clock Accuracy value
27:24	RW	0x0	iec_chsts_origsampfreq_qst Audio Generator Channel Status Original Sample Frequency value
23:20	RW	0x0	iec_chsts_wordlength_qst Audio Generator Channel Status Sample Word Length value
19:16	RW	0x0	iec_chsts_sampfreq_qst Audio Generator Channel Status Sampling Frequency value
15:8	RO	0x00	reserved
7:4	RW	0x0	iec_chsts_channelnumber_qst Audio Generator Channel Status Channel Number value
3:0	RW	0x0	iec_chsts_sourcenumber_qst Audio Generator Channel Status Source Number value

CED_CONFIG

Address: Operational Base + offset (0x0760)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x1	ced_viddatachecken_qst Enable Character Error Checking during Video data
26	RW	0x1	ced_dataischecken_qst Enable Character Error Checking during Data Island
25	RW	0x1	ced_gbchecken_qst Enable Character Error Checking during Guard Bands
24	RW	0x1	ced_ctrlchecken_qst Enable Character Error Checking during Control Period
23:15	RO	0x000	reserved
14:0	RW	0x0000	ced_chlockmaxer_qst Maximum errors detected within q period of 10ms to consider that the channel is locked

CED_STATUS

Address: Operational Base + offset (0x0764)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:6	RO	0x0	ced_decstate_ch2 Current Character Error Detection Decode State for channel 2 3'b000: Unknown 3'b001: Control Period 3'b010: Data Island 3'b011: Video Data 3'b100: Guard Band1 3'b101: Guard Band2 3'b110: Video Data to Control Period transition state 3'b111: Data Island to Control Period transition state

Bit	Attr	Reset Value	Description
5:3	RO	0x0	ced_decstate_ch1 Current Character Error Detection Decode State for channel 1 3'b000: Unknown 3'b001: Control Period 3'b010: Data Island 3'b011: Video Data 3'b100: Guard Band1 3'b101: Guard Band2 3'b110: Video Data to Control Period transition state 3'b111: Data Island to Control Period transition state
2:0	RO	0x0	ced_decstate_ch0 Current Character Error Detection Decode State for channel 0 3'b000: Unknown 3'b001: Control Period 3'b010: Data Island 3'b011: Video Data 3'b100: Guard Band1 3'b101: Guard Band2 3'b110: Video Data to Control Period transition state 3'b111: Data Island to Control Period transition state

CED_DYN_CONFIG
Address: Operational Base + offset (0x0768)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0001	ced_dyn_thr_qst Dynamic Character Error Detection counters interrupt threshold. Interrupt is generated when error counter is equal or bigger than the configured value.

CED_DYN_CONTROL
Address: Operational Base + offset (0x076C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	ced_dyn_clr_p Clear dynamic Character Error Detection counters

CED_DYN_STATUS1
Address: Operational Base + offset (0x0770)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RO	0x0000	ced_dyn_cnt_ch1_st Dynamic Character Error Detection counter value for channel 1
15	RO	0x0	reserved
14:0	RO	0x0000	ced_dyn_cnt_ch0_st Dynamic Character Error Detection counter value for channel 0

CED_DYN_STATUS2
Address: Operational Base + offset (0x0774)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	ced_dyn_cnt_ch2_st Dynamic Character Error Detection counter value for channel 2

PKTEX_BCH_ERRCORR_CONFIG

Address: Operational Base + offset (0x07C0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x1	bch_aud_errcorr_en_qst BCH Error correction enable, applicable to audio packets only. The BCH Error Correction Code implementation in the controller is according to what is defined in the HDMI1.4b specification. Depending on if the BCH Error Correction is enabled, one of the following approach is taken: bch_aud_errcorr_en_qst=1: Detection and correction of Subpackets containing 1bit error, plus detection of Subpackets containing 2bit errors.(no action is performed in this case) bch_aud_errcorr_en_qst=0: Detection(but no correction) of Subpackets containing 1bit, 2bit and any odd-n bit errors. Note: Although the Error Correction Code mechanism is able to detect errors in audio Subpackets(as described above), filtering is not applied. In that sense, switching off bch_aud_errcorr_en_qst performs no action over the incoming Subpackets.
0	RW	0x1	bch_errcorr_en_qst BCH Error correction enable, applicable to non-audio packets only. The BCH Error Correction Code implementation in the controller is according to what is defined in the HDMI1.4b specification. Depending on if the BCH Error Correction is enabled, one of the following approach is taken: bch_errcorr_en_qst=1: Detection and correction of Subpackets containing 1bit error, plus detection of Subpackets containing 2bit errors. bch_errcorr_en_qst=0: Detection(but no correction) of Subpackets containing 1bit, 2bit and any odd-n bit errors. Note: Packets with detected(but not corrected)errors are filtered depending on pktex_bch_errfilt_config individual field configuration.

PKTEX_BCH_ERRFILT_CONFIG

Address: Operational Base + offset (0x07C4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	bchsp_genpkt1_errfilt_qst BCH Generic Packet1 Subpacket error filter
28	RW	0x0	bchsp_genpkt0_errfilt_qst BCH Generic Packet0 Subpacket error filter
27:15	RO	0x0000	reserved
14	RW	0x0	bchsp_emd_errfilt_qst BCH EMD Subpacket error filter
13	RW	0x0	bchsp_drmif_errfilt_qst BCH DRM InfoFrame Subpacket error filter
12	RW	0x0	bchsp_ntscvbiif_errfilt_qst BCH NTSC VBI InfoFrame Subpacket error filter
11	RO	0x0	reserved
10	RW	0x0	bchsp_audif_errfilt_qst BCH AUD InfoFrame Subpacket error filter
9	RW	0x0	bchsp_srcpdif_errfilt_qst BCH SPD InfoFrame Subpacket error filter
8	RW	0x0	bchsp_avif_errfilt_qst BCH AVI InfoFrame Subpacket error filter

Bit	Attr	Reset Value	Description
7	RW	0x0	bchsp_vsif_errfilt_qst BCH VS InfoFrame Subpacket error filter
6	RW	0x0	bchsp_amd_errfilt_qst BCH AMD Subpacket error filter
5	RW	0x0	bchsp_gmd_errfilt_qst BCH GMD Subpacket error filter
4	RW	0x0	bchsp_isrc_errfilt_qst BCH ISRC1/ISRC2 Subpacket error filter
3	RW	0x0	bchsp_acp_errfilt_qst BCH ACP Subpacket error filter
2	RW	0x0	bchsp_gcp_errfilt_qst BCH GCP Subpacket error filter
1	RW	0x0	bchsp_acr_errfilt_qst BCH ACR Subpacket error filter
0	RW	0x0	bchph_errfilt_qst BCH Packet Header error filter

PKTEX_CHKSUM_ERRFILT_CONFIG

Address: Operational Base + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	chksum_genpkt1_errfilt_qst Generic Packet 1 Checksum error filter Note: This filter only takes effect if the configured Generic Packet 1 Type is an InfoFrame, such as PKT_TYPE[7]=1
28	RW	0x0	chksum_genpkt0_errfilt_qst Generic Packet 0 Checksum error filter Note: This filter only takes effect if the configured Generic Packet 0 Type is an InfoFrame, such as PKT_TYPE[7]=1
27:7	RO	0x000000	reserved
6	RW	0x0	chksum_drmif_errfilt_qst DRM InfoFrame Packet Checksum error filter
5	RW	0x0	chksum_ntscvbiif_errfilt_qst NTSC VBI InfoFrame Packet Checksum error filter
4	RO	0x0	reserved
3	RW	0x0	chksum_audif_errfilt_qst AUD InfoFrame Packet Checksum error filter
2	RW	0x0	chksum_srcpdif_errfilt_qst SPD InfoFrame Packet Checksum error filter
1	RW	0x0	chksum_aviif_errfilt_qst AVI InfoFrame Packet Checksum error filter
0	RW	0x0	chksum_vsif_errfilt_qst VS InfoFrame Packet Checksum error filter

PKTEX_BCHERR_ACC_STATUS

Address: Operational Base + offset (0x07CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	bchauderr_acc_sts Accumulated number of BCH Errors in audio packets. When read, this field is cleared. Note: This field considers errors regardless of the error correction mechanism.

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	bcherr_acc_sts Accumulated number of BCH Errors in non-audio packets. When read, this field is cleared. Note: This field considers errors regardless of the error correction mechanism.

PKTEX_FIELDS_BCHERR_STATUS

Address: Operational Base + offset (0x07D0)

Bit	Attr	Reset Value	Description
31:16	RO	0xffff	fields_since_bchauderr_sts Number of Fields since last BCH Error in audio packets. Note: This field considers errors regardless of the error correction mechanism.
15:0	RO	0xffff	fields_since_bcherr_sts Number of Fields since last BCH Error in non-audio packets. Note: This field considers errors regardless of the error correction mechanism.

GENPKT_TYPE_CONFIG

Address: Operational Base + offset (0x07D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	genpkt1_type Generic Packet 1 Type Attention: This feature does not support the following packet types (1)Audio Sample Packet (2)One Bit Audio Sample Packet (3)DST Audio Packet (4)High Bitrate Audio Stream Packet (5)3D Audio Sample Packet (6)One Bit 3D Audio Sample Packet (7)Multi-Stream Audio Sample Packet (8)One Bit Multi-Stream Audio Sample Packet
15:8	RO	0x00	reserved
7:0	RW	0x00	genpkt0_type Generic Packet 0 Type Attention: This feature does not support the following packet types (1)Audio Sample Packet (2)One Bit Audio Sample Packet (3)DST Audio Packet (4)High Bitrate Audio Stream Packet (5)3D Audio Sample Packet (6)One Bit 3D Audio Sample Packet (7)Multi-Stream Audio Sample Packet (8)One Bit Multi-Stream Audio Sample Packet

PKTEX_UPI_CONFIG

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	upi_genpkt1_type_en_output Generic Packet 1 enable UPI output

Bit	Attr	Reset Value	Description
28	RW	0x0	upi_genpkt0_type_en_output Generic Packet 0 enable UPI output
27:22	RO	0x00	reserved
21	RW	0x0	upi_emd_en_output Extended Metadata Packet enable UPI output
20	RW	0x0	upi_drmif_en_output Dynamic Range and Mastering(DRM) InfoFrame Packet enable UPI output
19	RW	0x0	upi_ntscvbiif_en_output NTSC VBI InfoFrame Packet enable UPI output
18	RO	0x0	reserved
17	RW	0x0	upi_audif_en_output AUD(Audio) InfoFrame Packet enable UPI output
16	RW	0x0	upi_srcpdif_en_output Source Product Descriptor(SPD) InfoFrame Packet enable UPI output
15	RW	0x0	upi_aviif_en_output AVI InfoFrame Packet enable UPI output
14	RW	0x0	upi_vsif_en_output Vendor Specific (VS) InfoFrame Packet enable UPI output
13	RW	0x0	upi_msoba_en_output One Bit Multi-Stream Audio Sample Packet enable UPI output
12	RW	0x0	upi_msa_en_output Multi-Stream Audio Sample Packet enable UPI output
11	RW	0x0	upi_amd_en_output Audio Metadata (AMD) Packet enable UPI output
10	RW	0x0	upi_3doba_en_output One bit 3D Audio Sample Packet enable UPI output
9	RW	0x0	upi_3da_en_output 3D Audio Sample Packet(L-PCM format only) enable UPI output
8	RW	0x0	upi_gmd_en_output GMD Packet enable UPI output
7	RW	0x0	upi_hbr_en_output High Bitrate(HBR) Audio Stream Packet(IEC61937) enable UPI output
6	RW	0x0	upi_dst_en_output DST Audio Sample Packet enable UPI output
5	RW	0x0	upi_oba_en_output One Bit Audio Sample Packet enable UPI output
4	RW	0x0	upi_isrc_en_output ISRC1/ISRC2 Packet enable UPI output
3	RW	0x0	upi_acp_en_output ACP Packet enable UPI output
2	RW	0x0	upi_gcp_en_output General Control Packet(GCP) enable UPI output
1	RW	0x0	upi_as_en_output Audio Sample(L-PCM and IEC 61937 compressed formats) enable UPI output
0	RW	0x0	upi_acr_en_output Audio Clock Regeneration(ACR) Packet enable UPI output

PKTEX_UPI_EMDFILTER_CONFIG
Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	upi_emdfilter_genemd_output Generic EMP type When this bit field is high the packets with Organization_id and Data_Set_Tag as defined in register genemd_emdfilter_config is outputed.
11:9	RO	0x0	reserved
8	RW	0x0	upi_emdfilter_vesa_output VESA defined Data Set When this bit field is high the packets with Organization_id == 3 is outputed
7	RW	0x0	upi_emdfilter_vtem_output Video Timing Extended Metadata When this bit field is high the packets with Organization_id == 1 and Data_Set_Tag == 1 is outputed
6	RW	0x0	upi_emdfilter_ctahdr_output CTA-861-G HDR Dynamic Metadata Extended InfoFrame When this bit field is high the packets with Organization_id == 2 is outputed
5	RW	0x0	upi_emdfilter_cvtem_output Compressed Video Transport Extended Metadata When this bit field is high the packets with Organization_id == 1 and Data_Set_Tag == 2 is outputed
4	RW	0x0	upi_emdfilter_vsem_output Vendor Specific EM Data Sets When this bit field is high the packets with Organization_id == 0 is outputed
3:1	RO	0x0	reserved
0	RW	0x0	upi_emdfilter_en UPI Extended Metadata Packet[EMP] filter by type enable 1'b0: All EMPs received are outouted, regardless of the type 1'b1: Only the EMPs with specific type(organization_id, and data_set_tag) set are outputed

GENEMD_EMDFILTER_CONFIG

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	genemd_dataset Data_Set_Tag for the generic EMP type
15:13	RO	0x0	reserved
12	RW	0x0	genemd_datasetfilter_en UPI Extended Metadata Packet[EMP] filter by Data_Set _Tag enable 1'b0: All EMPs with the Organization_ID = genemd_organization_id are outputed, regardless of the Data_Set_Tag value 1'b1: Only the EMPs with the Organization_ID = genemd_ organization_id and Data_Set_Tag = genemd_dataset are outputed
11:8	RO	0x0	reserved
7:0	RW	0x00	genemd_organization_id Organization_ID for the generic EMP type

PKTDEC_ACR_CONFIG

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	pktdec_acr_cts_offset_value ACR CTS offset value. This register field can be configured with a positive or negative value that is added to the CTS received in the ACR packet. Note: The register must be configured with a value represented in 2's complement
7	RO	0x0	reserved
6:4	RW	0x0	pktdec_acr_deltacts_thr_qst ACR Delta CTS Threshold. This field configures the minimum ACR CTS variation between two consecutive values in order for the interrupt request acr_cts_chg_irq to be triggered. (1)3'b000: Minimum Delta CTS = 1 (2)3'b001: Minimum Delta CTS = 2 (3)3'b010: Minimum Delta CTS = 4 (4)3'b011: Minimum Delta CTS = 8 (5)3'b100: Minimum Delta CTS = 16 (6)3'b101: Minimum Delta CTS = 32 (7)3'b110-3'b111: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	pktdec_acr_cts_n_over_en ACR CTS/N Override enable 1'b0: Override disabled 1'b1: Override enabled. The controller outputs 'ocfg_audpll_mux_cts' and 'ocfg_audpll_mux_n' takes their values from register fields 'pktdec_acr_cts_ovr_value' and 'pktdec_acr_ n_ovr_value', instead of the values from the received ACR Subpackets. If the override values are different from the last received ACR Subpacket, interrupt 'pktdec_acr_cts_chg_irq' is triggered once.

PKTDEC_ACR_CTS_CONFIG

Address: Operational Base + offset (0x1004)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	pktdec_acr_cts_ovr_value ACR CTS Override value

PKTDEC_ACR_N_CONFIG

Address: Operational Base + offset (0x1008)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	pktdec_acr_n_ovr_value ACR N Override value

PKTDEC_ACR_MAXMIN_CLEAR

Address: Operational Base + offset (0x100C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	pktdec_clear_avmute_p Writing 1 to this register clears the AVMUTE
0	WO	0x0	pktdec_acr_cts_n_maxmin_clr_p Writing 1 to this register clears the values of pkdec_acr_cts_max_ sts and pkdec_acr_n_max_sts to 0, while clearing the values of pkdec_acr_cts_min_cts and pkdec_acr_n_min_sts to 20'hfffff.

PKTDEC_ACR_CTS_MAX_STATUS

Address: Operational Base + offset (0x1010)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	pktdec_acr_cts_max_sts Maximum ACR CTS value

PKTDEC_ACR_CTS_MIN_STATUS

Address: Operational Base + offset (0x1014)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	pktdec_acr_cts_min_sts Minimum ACR CTS value

PKTDEC_ACR_N_MAX_STATUS

Address: Operational Base + offset (0x1018)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	pktdec_acr_n_max_sts Maximum ACR N value

PKTDEC_ACR_N_MIN_STATUS

Address: Operational Base + offset (0x101C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	pktdec_acr_n_min_sts Minimum ACR N value

PKTDEC_SP_VALID_CONFIG

Address: Operational Base + offset (0x1020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	pktdec_gcp_sp0_only_qst GCP/CMP Subpacket 0 only control register 1'b0: A majority algorithm to check equality of GCP/CMP Subpackets applied, filtering GCP/CMP packets that are not considered valid. 1'b1: GCP/CMP Subpacket 0 is considered always valid not attending to the other Subpacket values.
0	RW	0x0	pktdec_acr_sp0_only_qst ACR Subpacket 0 only control register 1'b0: A majority algorithm to check equality of ACR Subpackets is applied, filtering ACR packets that are not considered valid. 1'b1: ACR Subpacket 0 is considered always valid not attending to the other Subpacket values.

PKTDEC_GCP_AVMUTE_CONFIG

Address: Operational Base + offset (0x1024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:13	RW	0x0	pkdec_auto_clear_avmute_sel Auto Clear AVMUTE time selection 3'b000: 5s 3'b001: 2s 3'b010: 1s 3'b011: 500ms 3'b100: 250ms 3'b101-3'b111: Reserved(not to be used)
12	RW	0x0	pktdec_auto_clear_avmute_en Auto Clear AVMUTE enable 1'b0: Disable(no automatic clear AVMUTE) 1'b1: Enable
11:9	RO	0x0	reserved
8	RW	0x0	pktdec_gcp_clr_avmute_ovr_value GCP Clear_AVMUTE/CMP UNMUTE override value
7:5	RO	0x0	reserved
4	RW	0x0	pktdec_gcp_set_avmute_ovr_value GCP Set_AVMUTE/CMP MUTE override value
3:1	RO	0x0	reserved
0	RW	0x0	pktdec_gcp_avmute_ovr_en GCP/CMP Set_AVMUTE override enable

PKTDEC_AVMUTE_DIS_CONTROL

Address: Operational Base + offset (0x1028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pktdec_avmute_disable AVMUTE Disable

PKTDEC_EMD_CONTROL

Address: Operational Base + offset (0x102C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	pktdec_vtem_fva_en_ovr_value VTEM VRR_EN override value
2	RW	0x0	pktdec_vtem_fva_en_ovr_en VTEM VRR_EN override enable
1	RW	0x0	pktdec_vtem_vrr_en_ovr_value Internal VTEM FVA_EN override value
0	RW	0x0	pktdec_vtem_vrr_en_ovr_en Enable override of internal FVA_EN generation from VTEM FVA_Factor_M1 field.

PKTDEC_GCP_AVMUTE_STATUS

Address: Operational Base + offset (0x1030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	pktdec_gcp_clr_avmute_sts GCP Clear_AVMUTE/CMP MUTE status(shows overridden value if pkdec_gcp_avmute_ovr_en=1)
3:1	RO	0x0	reserved
0	RO	0x0	pktdec_gcp_set_avmute_sts GCP Set_AVMUTE/CMP MUTE status(shows overridden value if pkdec_gcp_avmute_ovr_en=1)

PKTDEC_EMD_STATUS

Address: Operational Base + offset (0x1034)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	pktdec_emd_vtem_sts Video Timing Extended Metadata Data Set active status 1'b0: Video Timing data set is invalid 1'b1: Video Timing data set is valid
0	RO	0x0	pktdec_emd_cvtem_sts Compressed Video Transport Extended Metadata Data Set active status 1'b0: Compressed Video Transport is not active 1'b1: Compressed Video Transport is active

PKTDEC_SNAPSHOT_BYP_CONTROL

Address: Operational Base + offset (0x1040)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pktdec_snapshot_bypass Snapshot bypass 1'b0: Snapshot mechanism is used 1'b1: Snapshot mechanism is bypassed The Packet Decoder relies on a snapshot mechanism used to guarantee consistency of Data Island packet data during the read process of register in the 0x1100-0x14ff address range.

PKTDEC_ACR_PH2_1

Address: Operational Base + offset (0x1100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_acr_ph2_1 Audio Clock Regeneration Packet Header Bytes 1-2

PKTDEC_ACR_PB3_0

Address: Operational Base + offset (0x1104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acr_pb3_0 Audio Clock Regeneration Packet Body Bytes 3-0

PKTDEC_ACR_PB7_4

Address: Operational Base + offset (0x1108)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acr_pb7_4 Audio Clock Regeneration Packet Body Bytes 7-4

PKTDEC_ACR_PB11_8

Address: Operational Base + offset (0x110C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acr_pb11_8 Audio Clock Regeneration Packet Body Bytes 11-8

PKTDEC_ACR_PB15_12

Address: Operational Base + offset (0x1110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acr_pb15_12 Audio Clock Regeneration Packet Body Bytes 15-12

PKTDEC_ACR_PB19_16

Address: Operational Base + offset (0x1114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acr_pb19_16 Audio Clock Regeneration Packet Body Bytes 19-16

PKTDEC_ACR_PB23_20

Address: Operational Base + offset (0x1118)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acr_pb23_20 Audio Clock Regeneration Packet Body Bytes 23-20

PKTDEC_ACR_PB27_24

Address: Operational Base + offset (0x111C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acr_pb27_24 Audio Clock Regeneration Packet Body Bytes 27-24

PKTDEC_GCP_PH2_1

Address: Operational Base + offset (0x1120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_gcp_ph2_1 Generic Content/Content Mute Packet Header Bytes 1-2

PKTDEC_GCP_PB3_0

Address: Operational Base + offset (0x1124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gcp_pb3_0 Generic Content/Content Mute Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_gcp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GCP_PB7_4

Address: Operational Base + offset (0x1128)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gcp_pb7_4 Generic Content/Content Mute Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_gcp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GCP_PB11_8

Address: Operational Base + offset (0x112C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gcp_pb11_8 Generic Content/Content Mute Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_gcp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GCP_PB15_12

Address: Operational Base + offset (0x1130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gcp_pb15_12 Generic Content/Content Mute Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_gcp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GCP_PB19_16

Address: Operational Base + offset (0x1134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gcp_pb19_16 Generic Content/Content Mute Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_gcp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GCP_PB23_20

Address: Operational Base + offset (0x1138)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gcp_pb23_20 Generic Content/Content Mute Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_gcp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GCP_PB27_24

Address: Operational Base + offset (0x113C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gcp_pb27_24 Generic Content/Content Mute Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_gcp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ACP_PH2_1

Address: Operational Base + offset (0x1140)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_acp_ph2_1 Audio Content Protection Packet Header Bytes 1-2

PKTDEC_ACP_PB3_0

Address: Operational Base + offset (0x1144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acp_pb3_0 Audio Content Protection Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_acp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ACP_PB7_4

Address: Operational Base + offset (0x1148)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acp_pb7_4 Audio Content Protection Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_acp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ACP_PB11_8

Address: Operational Base + offset (0x114C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acp_pb11_8 Audio Content Protection Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_acp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ACP_PB15_12

Address: Operational Base + offset (0x1150)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acp_pb15_12 Audio Content Protection Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_acp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ACP_PB19_16

Address: Operational Base + offset (0x1154)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acp_pb19_16 Audio Content Protection Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_acp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ACP_PB23_20

Address: Operational Base + offset (0x1158)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acp_pb23_20 Audio Content Protection Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_acp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ACP_PB27_24

Address: Operational Base + offset (0x115C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_acp_pb27_24 Audio Content Protection Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_acp_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC1_PH2_1

Address: Operational Base + offset (0x1160)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	pktdec_isrc1_ph2_1 ISRC1 Packet Header Bytes 1-2

PKTDEC_ISRC1_PB3_0

Address: Operational Base + offset (0x1164)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc1_pb3_0 ISRC1 Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_isrc1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC1_PB7_4

Address: Operational Base + offset (0x1168)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc1_pb7_4 ISRC1 Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_isrc1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC1_PB11_8

Address: Operational Base + offset (0x116C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc1_pb11_8 ISRC1 Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_isrc1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC1_PB15_12

Address: Operational Base + offset (0x1170)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc1_pb15_12 ISRC1 Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_isrc1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC1_PB19_16

Address: Operational Base + offset (0x1174)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc1_pb19_16 ISRC1 Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_isrc1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC1_PB23_20

Address: Operational Base + offset (0x1178)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc1_pb23_20 ISRC1 Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_isrc1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC1_PB27_24

Address: Operational Base + offset (0x117C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc1_pb27_24 ISRC1 Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_isrc1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC2_PH2_1

Address: Operational Base + offset (0x1180)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_isrc2_ph2_1 ISRC2 Packet Header Bytes 1-2

PKTDEC_ISRC2_PB3_0

Address: Operational Base + offset (0x1184)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc2_pb3_0 ISRC2 Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_isrc2_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC2_PB7_4

Address: Operational Base + offset (0x1188)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc2_pb7_4 ISRC2 Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_isrc2_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC2_PB11_8

Address: Operational Base + offset (0x118C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc2_pb11_8 ISRC2 Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_isrc2_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC2_PB15_12

Address: Operational Base + offset (0x1190)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc2_pb15_12 ISRC2 Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_isrc2_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC2_PB19_16

Address: Operational Base + offset (0x1194)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc2_pb19_16 ISRC2 Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_isrc2_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC2_PB23_20

Address: Operational Base + offset (0x1198)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc2_pb23_20 ISRC2 Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_isrc2_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_ISRC2_PB27_24

Address: Operational Base + offset (0x119C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_isrc2_pb27_24 ISRC2 Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_isrc2_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GMD_PH2_1

Address: Operational Base + offset (0x11A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_gmd_ph2_1 Gamut Metadata Packet Header Bytes 1-2

PKTDEC_GMD_PB3_0

Address: Operational Base + offset (0x11A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gmd_pb3_0 Gamut Metadata Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_gmd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GMD_PB7_4

Address: Operational Base + offset (0x11A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gmd_pb7_4 Gamut Metadata Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_gmd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GMD_PB11_8

Address: Operational Base + offset (0x11AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gmd_pb11_8 Gamut Metadata Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_gmd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GMD_PB15_12

Address: Operational Base + offset (0x11B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gmd_pb15_12 Gamut Metadata Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_gmd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GMD_PB19_16

Address: Operational Base + offset (0x11B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gmd_pb19_16 Gamut Metadata Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_gmd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GMD_PB23_20

Address: Operational Base + offset (0x11B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gmd_pb23_20 Gamut Metadata Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_gmd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_GMD_PB27_24

Address: Operational Base + offset (0x11BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_gmd_pb27_24 Gamut Metadata Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_gmd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass.

PKTDEC_AMD_PH2_1

Address: Operational Base + offset (0x11C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	pktdec_amd_ph2_1 Audio Metadata Packet Header Bytes 1-2

PKTDEC_AMD_PB3_0

Address: Operational Base + offset (0x11C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_amd_pb3_0 Audio Metadata Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_amd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AMD_PB7_4

Address: Operational Base + offset (0x11C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_amd_pb7_4 Audio Metadata Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_amd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AMD_PB11_8

Address: Operational Base + offset (0x11CC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_amd_pb11_8 Audio Metadata Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_amd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AMD_PB15_12

Address: Operational Base + offset (0x11D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_amd_pb15_12 Audio Metadata Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_amd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AMD_PB19_16

Address: Operational Base + offset (0x11D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_amd_pb19_16 Audio Metadata Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_amd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AMD_PB23_20

Address: Operational Base + offset (0x11D8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_amd_pb23_20 Audio Metadata Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_amd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AMD_PB27_24

Address: Operational Base + offset (0x11DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_amd_pb27_24 Audio Metadata Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_amd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_VSIF_PH2_1

Address: Operational Base + offset (0x11E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_vsif_ph2_1 Vendor-Specific InfoFrame Packet Header Bytes 1-2

PKTDEC_VSIF_PB3_0

Address: Operational Base + offset (0x11E4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_vsif_pb3_0 Vendor-Specific InfoFrame Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_vsif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_VSIF_PB7_4

Address: Operational Base + offset (0x11E8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_vsif_pb7_4 Vendor-Specific InfoFrame Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_vsif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_VSIF_PB11_8

Address: Operational Base + offset (0x11EC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_vsif_pb11_8 Vendor-Specific InfoFrame Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_vsif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_VSIF_PB15_12

Address: Operational Base + offset (0x11F0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_vsif_pb15_12 Vendor-Specific InfoFrame Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_vsif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_VSIF_PB19_16

Address: Operational Base + offset (0x11F4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_vsif_pb19_16 Vendor-Specific InfoFrame Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_vsif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_VSIF_PB23_20

Address: Operational Base + offset (0x11F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_vsif_pb23_20 Vendor-Specific InfoFrame Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_vsif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_VSIF_PB27_24

Address: Operational Base + offset (0x11FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_vsif_pb27_24 Vendor-Specific InfoFrame Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_vsif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AVIIF_PH2_1

Address: Operational Base + offset (0x1200)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_aviif_ph2_1 Auxiliary Video Information Packet Header Bytes 1-2

PKTDEC_AVIIF_PB3_0

Address: Operational Base + offset (0x1204)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_aviif_pb3_0 Auxiliary Video Information Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_aviif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AVIIF_PB7_4

Address: Operational Base + offset (0x1208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_aviif_pb7_4 Auxiliary Video Information Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_aviif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AVIIF_PB11_8

Address: Operational Base + offset (0x120C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_aviif_pb11_8 Auxiliary Video Information Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_aviif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AVIIF_PB15_12

Address: Operational Base + offset (0x1210)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_aviif_pb15_12 Auxiliary Video Information Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_aviif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AVIIF_PB19_16

Address: Operational Base + offset (0x1214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_aviif_pb19_16 Auxiliary Video Information Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_aviif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AVIIF_PB23_20

Address: Operational Base + offset (0x1218)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_aviif_pb23_20 Auxiliary Video Information Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_aviif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AVIIF_PB27_24

Address: Operational Base + offset (0x121C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_aviif_pb27_24 Auxiliary Video Information Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_aviif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_SRCPDIF_PH2_1

Address: Operational Base + offset (0x1220)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	pktdec_srcpdif_ph2_1 Source Product Descriptor InfoFrame Packet Header Bytes 1-2

PKTDEC_SRCPDIF_PB3_0

Address: Operational Base + offset (0x1224)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_srcpdif_pb3_0 Source Product Descriptor InfoFrame Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_srcpdif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_SRCPDIF_PB7_4

Address: Operational Base + offset (0x1228)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_srcpdif_pb7_4 Source Product Descriptor InfoFrame Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_srcpdif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_SRCPDIF_PB11_8

Address: Operational Base + offset (0x122C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_srcpdif_pb11_8 Source Product Descriptor InfoFrame Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_srcpdif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_SRCPDIF_PB15_12

Address: Operational Base + offset (0x1230)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_srcpdif_pb15_12 Source Product Descriptor InfoFrame Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_srcpdif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_SRCPDIF_PB19_16

Address: Operational Base + offset (0x1234)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_srcpdif_pb19_16 Source Product Descriptor InfoFrame Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_srcpdif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_SRCPDIF_PB23_20

Address: Operational Base + offset (0x1238)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_srcpdif_pb23_20 Source Product Descriptor InfoFrame Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_srcpdif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_SRCPDIF_PB27_24
Address: Operational Base + offset (0x123C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_srcpdif_pb27_24 Source Product Descriptor InfoFrame Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_srcpdif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AUDIF_PH2_1
Address: Operational Base + offset (0x1240)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_audif_ph2_1 Audio InfoFrame Packet Header Bytes 1-2

PKTDEC_AUDIF_PB3_0
Address: Operational Base + offset (0x1244)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_audif_pb3_0 Audio InfoFrame Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_audif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AUDIF_PB7_4
Address: Operational Base + offset (0x1248)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_audif_pb7_4 Audio InfoFrame Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_audif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AUDIF_PB11_8
Address: Operational Base + offset (0x124C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_audif_pb11_8 Audio InfoFrame Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_audif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AUDIF_PB15_12
Address: Operational Base + offset (0x1250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_audif_pb15_12 Audio InfoFrame Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_audif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AUDIF_PB19_16

Address: Operational Base + offset (0x1254)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_audif_pb19_16 Audio InfoFrame Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_audif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AUDIF_PB23_20

Address: Operational Base + offset (0x1258)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_audif_pb23_20 Audio InfoFrame Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_audif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_AUDIF_PB27_24

Address: Operational Base + offset (0x125C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_audif_pb27_24 Audio InfoFrame Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_audif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_NTSCVBIIF_PH2_1

Address: Operational Base + offset (0x1280)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_ntscvbiif_ph2_1 NTSC VBI InfoFrame Packet Header Bytes 1-2

PKTDEC_NTSCVBIIF_PB3_0

Address: Operational Base + offset (0x1284)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_ntscvbiif_pb3_0 NTSC VBI InfoFrame Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_ntscvbiif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_NTSCVBIIF_PB7_4

Address: Operational Base + offset (0x1288)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_ntscvbiif_pb7_4 NTSC VBI InfoFrame Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_ntscvbiif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_NTSCVBIIF_PB11_8

Address: Operational Base + offset (0x128C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_ntscvbiif_pb11_8 NTSC VBI InfoFrame Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_ntscvbiif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_NTSCVBIIF_PB15_12

Address: Operational Base + offset (0x1290)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_ntscvbiif_pb15_12 NTSC VBI InfoFrame Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_ntscvbiif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_NTSCVBIIF_PB19_16

Address: Operational Base + offset (0x1294)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_ntscvbiif_pb19_16 NTSC VBI InfoFrame Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_ntscvbiif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_NTSCVBIIF_PB23_20

Address: Operational Base + offset (0x1298)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_ntscvbiif_pb23_20 NTSC VBI InfoFrame Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_ntscvbiif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_NTSCVBIIF_PB27_24

Address: Operational Base + offset (0x129C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_ntscvbiif_pb27_24 NTSC VBI InfoFrame Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_ntscvbiif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_DRMIF_PH2_1

Address: Operational Base + offset (0x12A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	pktdec_drmif_ph2_1 Dynamic Range and Mastering InfoFrame Packet Header Bytes 1-2

PKTDEC_DRMIF_PB3_0
Address: Operational Base + offset (0x12A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_drmif_pb3_0 Dynamic Range and Mastering InfoFrame Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_drmif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_DRMIF_PB7_4
Address: Operational Base + offset (0x12A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_drmif_pb7_4 Dynamic Range and Mastering InfoFrame Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_drmif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_DRMIF_PB11_8
Address: Operational Base + offset (0x12AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_drmif_pb11_8 Dynamic Range and Mastering InfoFrame Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_drmif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_DRMIF_PB15_12
Address: Operational Base + offset (0x12B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_drmif_pb15_12 Dynamic Range and Mastering InfoFrame Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_drmif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_DRMIF_PB19_16
Address: Operational Base + offset (0x12B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_drmif_pb19_16 Dynamic Range and Mastering InfoFrame Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_drmif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_DRMIF_PB23_20
Address: Operational Base + offset (0x12B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_drmif_pb23_20 Dynamic Range and Mastering InfoFrame Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_drmif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_DRMIF_PB27_24

Address: Operational Base + offset (0x12BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_drmif_pb27_24 Dynamic Range and Mastering InfoFrame Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_drmif_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_EMD_PH2_1

Address: Operational Base + offset (0x12C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_emd_ph2_1 Extended Metadata Packet Header Bytes 1-2

PKTDEC_EMD_PB3_0

Address: Operational Base + offset (0x12C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_emd_pb3_0 Extended Metadata Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_emd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_EMD_PB7_4

Address: Operational Base + offset (0x12C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_emd_pb7_4 Extended Metadata Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_emd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_EMD_PB11_8

Address: Operational Base + offset (0x12CC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_emd_pb11_8 Extended Metadata Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_emd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_EMD_PB15_12

Address: Operational Base + offset (0x12D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_emd_pb15_12 Extended Metadata Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_emd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_EMD_PB19_16

Address: Operational Base + offset (0x12D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_emd_pb19_16 Extended Metadata Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_emd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_EMD_PB23_20

Address: Operational Base + offset (0x12D8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_emd_pb23_20 Extended Metadata Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_emd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_EMD_PB27_24

Address: Operational Base + offset (0x12DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_emd_pb27_24 Extended Metadata Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_emd_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT0_PH2_1

Address: Operational Base + offset (0x1480)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pktdec_genpkt0_ph2_1 Generic Packet 0 Packet Header Bytes 1-2

PKTDEC_GENPKT0_PB3_0

Address: Operational Base + offset (0x1484)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt0_pb3_0 Generic Packet 0 Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_genpkt0_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT0_PB7_4

Address: Operational Base + offset (0x1488)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt0_pb7_4 Generic Packet 0 Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_genpkt0_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT0_PB11_8

Address: Operational Base + offset (0x148C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt0_pb11_8 Generic Packet 0 Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_genpkt0_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT0_PB15_12

Address: Operational Base + offset (0x1490)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt0_pb15_12 Generic Packet 0 Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_genpkt0_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT0_PB19_16

Address: Operational Base + offset (0x1494)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt0_pb19_16 Generic Packet 0 Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_genpkt0_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT0_PB23_20

Address: Operational Base + offset (0x1498)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt0_pb23_20 Generic Packet 0 Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_genpkt0_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT0_PB27_24

Address: Operational Base + offset (0x149C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt0_pb27_24 Generic Packet 0 Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_genpkt0_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT1_PH2_1

Address: Operational Base + offset (0x14A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	pktdec_genpkt1_ph2_1 Generic Packet 1 Packet Header Bytes 1-2

PKTDEC_GENPKT1_PB3_0

Address: Operational Base + offset (0x14A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt1_pb3_0 Generic Packet 1 Packet Body Bytes 3-0 Note: contents only updated after reading pktdec_genpkt1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT1_PB7_4

Address: Operational Base + offset (0x14A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt1_pb7_4 Generic Packet 1 Packet Body Bytes 7-4 Note: contents only updated after reading pktdec_genpkt1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT1_PB11_8

Address: Operational Base + offset (0x14AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt1_pb11_8 Generic Packet 1 Packet Body Bytes 11-8 Note: contents only updated after reading pktdec_genpkt1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT1_PB15_12

Address: Operational Base + offset (0x14B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt1_pb15_12 Generic Packet 1 Packet Body Bytes 15-12 Note: contents only updated after reading pktdec_genpkt1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT1_PB19_16

Address: Operational Base + offset (0x14B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt1_pb19_16 Generic Packet 1 Packet Body Bytes 19-16 Note: contents only updated after reading pktdec_genpkt1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT1_PB23_20

Address: Operational Base + offset (0x14B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt1_pb23_20 Generic Packet 1 Packet Body Bytes 23-20 Note: contents only updated after reading pktdec_genpkt1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTDEC_GENPKT1_PB27_24

Address: Operational Base + offset (0x14BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktdec_genpkt1_pb27_24 Generic Packet 1 Packet Body Bytes 27-24 Note: contents only updated after reading pktdec_genpkt1_ph2_1, unless snapshot feature is disabled using pktdec_snapshot_bypass

PKTFIFO_CONFIG

Address: Operational Base + offset (0x1500)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pktfifo_write_en Packet FIFO write enable 1'b0: Inhibit write to Packet FIFO 1'b1: Allow write to Packet FIFO

PKTFIFO_STORE_FILT_CONFIG

Address: Operational Base + offset (0x1504)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	pktfifo_store_genpkt1 Store Generic Packet 1 packets
28	RW	0x0	pktfifo_store_genpkt0 Store Generic Packet 0 packets
27:15	RO	0x0000	reserved
14	RW	0x0	pktfifo_store_emd Store Extended Metadata packets
13	RW	0x0	pktfifo_store_drmif Store Dynamic Range and Mastering InfoFrame packets
12	RW	0x0	pktfifo_store_ntscvbiif Store NTSC VBI InfoFrame packets
11	RO	0x0	reserved
10	RW	0x0	pktfifo_store_audif Store Audio InfoFrame packets
9	RW	0x0	pktfifo_store_srcpdif Store Source Product Descriptor InfoFrame packets
8	RW	0x0	pktfifo_store_aviif Store Auxiliary Video Information InfoFrame packets
7	RW	0x0	pktfifo_store_vsif Store Vendor-Specific InfoFrame packets
6	RW	0x0	pktfifo_store_amd Store Audio Metadata packets
5	RW	0x0	pktfifo_store_gmd Store Gamut Metadata packets
4	RW	0x0	pktfifo_store_isrc Store ISRC1/ISRC2 packets

Bit	Attr	Reset Value	Description
3	RW	0x0	pktfifo_store_acp Store Audio Content Protection packets
2	RW	0x0	pktfifo_store_gcp Store General Control/Content Mute packets
1	RW	0x0	pktfifo_store_acr Store Audio Clock Regeneration packets
0	RW	0x0	pktfifo_store_filt_en Store filter enable

PKTFIFO_THR_CONFIG0
Address: Operational Base + offset (0x1508)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x032	pktfifo_thr_pass_qst Packet FIFO pass threshold level(real FIFO threshold is configured value x4)

PKTFIFO_THR_CONFIG1
Address: Operational Base + offset (0x150C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	pktfifo_thr_high_qst Packet FIFO high threshold level(real FIFO threshold is configured value x4)
15:11	RO	0x00	reserved
10:1	RW	0x004	pktfifo_thr_low_qst Packet FIFO low threshold level(real FIFO threshold is configured value x4)
0	RO	0x0	reserved

PKTFIFO_CONTROL
Address: Operational Base + offset (0x1510)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	WO	0x0	pktfifo_ltfill_clr_p Clear Long-term Packet FIFO fill status When asserted, the values that drive register fields pktfifo_ltfill_min_st and pktfifo_ltfill_max_ sts are cleared.
7:1	RO	0x00	reserved
0	WO	0x0	pktfifo_init_p Packet FIFO initialization pulse When asserted, the Packet FIFO address pointers are reset.

PKTFIFO_FILL_STATUS
Address: Operational Base + offset (0x1514)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	pktfifo_thr_high_st Packet FIFO above high threshold status
27:25	RO	0x0	reserved
24	RO	0x0	pktfifo_thr_pass_st Packet FIFO above pass threshold status
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RO	0x0	pktfifo_thr_low_st Packet FIFO below low threshold status
19:17	RO	0x0	reserved
16	RO	0x0	pktfifo_new_entry_st Packet FIFO New Entry status
15:0	RO	0x0000	pktfifo_fill_sts Packet FIFO Fill Level status(number of packets in the FIFO)

PKTFIFO_LTERM_FILL_STATUS

Address: Operational Base + offset (0x1518)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pktfifo_ltfill_max_sts Packet FIFO Long-term fill maximum status
15:0	RO	0x0000	pktfifo_ltfill_min_sts Packet FIFO Long-term fill minimum status

PKTFIFO_SKIP_PKT_CONTROL

Address: Operational Base + offset (0x151C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	pktfifo_skip_pkt_p Write 1 to skip the packet currently at the top of the FIFO. If some of the packet words have already been read from pktfifo_data, the remaining words are discarded.

PKTFIFO_DATA

Address: Operational Base + offset (0x1520)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pktfifo_data Read this register to read the top of the Packet FIFO and pop the next value.

VMON_CONTROL

Address: Operational Base + offset (0x1560)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	vmon_source_sel Video Monitor source selection 3'b000: PVO output 3'b001: HDCP output 3'b010: Deframer output 3'b011: VPG output 3'b100: VPROC internal 3'b101-3'b111: Reserved
27:25	RO	0x0	reserved
24	RW	0x0	vmon_irq_thr_mode Video monitor measurement interrupt threshold mode 1'b0: A change bigger than 1 in a front, syncwidth, back, or active measurement generates an interrupt. 1'b1: Any change in a front, syncwidth, back, or active measurement generates an interrupt.
23:19	RO	0x00	reserved

Bit	Attr	Reset Value	Description
18:16	RW	0x0	vmon_dataen_diph_sel Data enable diphase selection 3'b000: Do not delay data enable 3'b001: Delay data enable by one TMDS cycle 3'b010: Delay data enable by two TMDS cycle 3'b011: Delay data enable by three TMDS cycle 3'b100-3'b111: Reserved, no delay
15:11	RO	0x00	reserved
10:8	RW	0x0	vmon_vsync_diph_sel Vsync diphase selection 3'b000: Do not delay vertical sync 3'b001: Delay vertical sync by one TMDS cycle 3'b010: Delay vertical sync by two TMDS cycle 3'b011: Delay vertical sync by three TMDS cycle 3'b100-3'b111: Reserved, no delay
7:3	RO	0x00	reserved
2:0	RW	0x0	vmon_hsync_diph_sel Hsync diphase selection 3'b000: Do not delay horizontal sync 3'b001: Delay horizontal sync by one TMDS cycle 3'b010: Delay horizontal sync by two TMDS cycle 3'b011: Delay horizontal sync by three TMDS cycle 3'b100-3'b111: Reserved, no delay

VMON_CONTROL2

Address: Operational Base + offset (0x1564)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x1	vmon_irq_vactive_en Video Monitor interrupt enable when Vactive changes. 1'b0: Changes in Vactive doesn't generate an interrupt 1'b1: Changes in Vactive generates an interrupt
11	RW	0x1	vmon_irq_vback_en Video Monitor interrupt enable when Vback changes. 1'b0: Changes in Vback doesn't generate an interrupt 1'b1: Changes in Vback generates an interrupt
10	RW	0x1	vmon_irq_vsyncwidth_en Video Monitor interrupt enable when Vsyncwidth changes. 1'b0: Changes in Vsyncwidth doesn't generate an interrupt 1'b1: Changes in Vsyncwidth generates an interrupt
9	RW	0x1	vmon_irq_vfront_en Video Monitor interrupt enable when Vfront changes. 1'b0: Changes in Vfront doesn't generate an interrupt 1'b1: Changes in Vfront generates an interrupt
8	RW	0x1	vmon_irq_vtotal_en Video Monitor interrupt enable when Vtotal changes. 1'b0: Changes in Vtotal doesn't generate an interrupt 1'b1: Changes in Vtotal generates an interrupt
7:5	RO	0x0	reserved
4	RW	0x1	vmon_irq_hactive_en Video Monitor interrupt enable when Hactive changes. 1'b0: Changes in Hactive doesn't generate an interrupt 1'b1: Changes in Hactive generates an interrupt

Bit	Attr	Reset Value	Description
3	RW	0x1	vmon_irq_hback_en Video Monitor interrupt enable when Hback changes. 1'b0: Changes in Hback doesn't generate an interrupt 1'b1: Changes in Hback generates an interrupt
2	RW	0x1	vmon_irq_hsyncwidth_en Video Monitor interrupt enable when Hsyncwidth changes. 1'b0: Changes in Hsyncwidth doesn't generate an interrupt 1'b1: Changes in Hsyncwidth generates an interrupt
1	RW	0x1	vmon_irq_hfront_en Video Monitor interrupt enable when Hfront changes. 1'b0: Changes in Hfront doesn't generate an interrupt 1'b1: Changes in Hfront generates an interrupt
0	RW	0x1	vmon_irq_htotal_en Video Monitor interrupt enable when Htotal changes. 1'b0: Changes in Htotal doesn't generate an interrupt 1'b1: Changes in Htotal generates an interrupt

VMON_STATUS1

Address: Operational Base + offset (0x1580)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vmon_hsyncwidth Horizontal sync width measure
15:0	RO	0x0000	vmon_hfront Horizontal front measure

VMON_STATUS2

Address: Operational Base + offset (0x1584)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vmon_hblank Horizontal blank measure
15:0	RO	0x0000	vmon_hback Horizontal back measure

VMON_STATUS3

Address: Operational Base + offset (0x1588)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vmon_htotal Horizontal total measure
15:0	RO	0x0000	vmon_hactive Horizontal active measure

VMON_STATUS4

Address: Operational Base + offset (0x158C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vmon_vsyncwidth Vertical sync width measure
15:0	RO	0x0000	vmon_vfront Vertical front measure

VMON_STATUS5

Address: Operational Base + offset (0x1590)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vmon_vblank Vertical blank measure

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	vmon_vback Vertical back measure

VMON_STATUS6

Address: Operational Base + offset (0x1594)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	vmon_vtotal Vertical total measure
15:0	RO	0x0000	vmon_vactive Vertical active measure

VMON_STATUS7

Address: Operational Base + offset (0x1598)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	vmon_alt_detect Alternative video detection 1'b0: Odd frame detected-Vsync fall edge aligned with Hsync rise edge 1'b1: Even frame detected-Vsync fall edge misaligned with Hsync rise edge Note: Alternative video detection is only enabled when preceding Vsync rise edge is aligned with Hsync rise edge.
7:5	RO	0x0	reserved
4	RO	0x0	vmon_ilace_detect Interlaced video detection 1'b0: Progressive video format 1'b1: Interlaced video format Video format is consider interlaced if either field or alternative detections are asserted at least once every two Vsync cycles.
3:1	RO	0x0	reserved
0	RO	0x0	vmon_field_detect Field detection 1'b0: Odd field-Vsync rise edge aligned with Hsync rise edge 1'b1: Even field-Vsync rise edge misaligned with Hsync rise edge

CEC_TX_CONTROL

Address: Operational Base + offset (0x2000)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	frame_send_clr_p Prevents further re-transmissions. If the transmission is ongoing, it is attempted to completion.
0	WO	0x0	frame_send_set_p Set by software to trigger CEC sending a frame as an initiator. If cec_cfg.txreq_discad_ifrxbusy == 0, the frame is transmitted even after receiving a frame in between. Otherwise, the frame to be sent is discarded as soon as a new incoming frame arrives(before being able to transmit)

CEC_STATUS

Address: Operational Base + offset (0x2004)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RO	0x0	cectx_busy_st Hardware is busy transmitting a frame When this bit change, It generates the cectx_busy_irq interrupt.
7:5	RO	0x0	reserved
4	RO	0x0	cecrx_busy_st Hardware is busy receiving a message frame. If 'send' is asserted for a new TX message to be sent, it is delayed until the ongoing RX message is done. When this bit changes, it generates the cecrx_ busy_irq interrupt.
3:1	RO	0x0	reserved
0	RO	0x0	frame_send_pending_st Frame send pending status 1'b1: A frame is set to be transmitted(waiting for the end of an incoming message or to have access to the line). This bit keeps at 1 while the transmission is going on. 1'b0: CEC transmission is done(no matter successful or failed)

CEC_CONFIG

Address: Operational Base + offset (0x2008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	rx_automatic_drive_acknowledge RX automatic drive acknowledge 1'b0: Wait for initiator to drive logic "1" at ACK/NACK bit position for follower to reply with ACK/NACK bit 1'b1: Automatically drive ACK/NACK bit at 2.65ms of EOM initiator bit
8	RW	0x1	cecfilter Filter enable. Active high 1'b1: CEC filter is active and filters spurious signals in the CEC line (filter pulses < 0.1ms) 1'b0: CEC filter inactive
7:6	RO	0x0	reserved
5:4	RW	0x1	frame_nretrans Select number of re-transmission the hardware attempts as initiator after an arbitration loss(cectx_arblost_irq) or line error detection(cectx_lineerror_irq)
3:2	RO	0x0	reserved
1	RW	0x0	broadcast_nack Broadcast State 1'b1: Respond with Negative ACK to any received broadcast message. Message not stored in RX registers 1'b0: Receive broadcast messages
0	RW	0x0	txreq_discard_if_rxbusy Transmit request(cec_ctrl.send=1)is discarded if a RX transfer is ongoing. 1'b1: The transmit request is cancelled if there is an ongoing RX transfer on the CEC line, raising the RX busy interrupt. 1'b0: The transmit request is always recorded by the TX FIFO for immediate or later transmission, depending on the CEC line status. For instance, the transmit is performed as soon as possible.

CEC_ADDR

Address: Operational Base + offset (0x200C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	cec_follower_addr Logical address allocated to the CEC device. Each bit selects a specific address, multiple bits can be selected (1)Logical address 0 - Device TV (2)Logical address 1 - Recording Device 1 (3)Logical address 2 - Recording Device 2 (4)Logical address 3 - Tuner 1 (5)Logical address 4 - Playback Device 1 (6)Logical address 5 - Audio System (7)Logical address 6 - Tuner 2 (8)Logical address 7 - Tuner 3 (9)Logical address 8 - Playback Device 2 (10)Logical address 9 - Playback Device 3 (11)Logical address 10 - Tuner 4 (12)Logical address 11 - Playback Device 3 (13)Logical address 12 - Backup 1 (14)Logical address 13 - Backup 2 (15)Logical address 14 - Specific use The CEC always answers to broadcast messages unless the broadcast_nack field of the cec_config register is set to 1'b1.

CEC_TX_COUNT

Address: Operational Base + offset (0x2020)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	cec_txbuffer_cnt Frame message size in bytes to be transmitted, including Header and Data blocks 4'b0000: Send 1 byte 4'b0001: Send 2 bytes 4'b0010: Send 3 bytes 4'b0011: Send 4 bytes 4'b0100: Send 5 bytes 4'b0101: Send 6 bytes 4'b0110: Send 7 bytes 4'b0111: Send 8 bytes 4'b1000: Send 9 bytes 4'b1001: Send 10 bytes 4'b1010: Send 11 bytes 4'b1011: Send 12 bytes 4'b1100: Send 13 bytes 4'b1101: Send 14 bytes 4'b1110: Send 15 bytes 4'b1111: Send 16 bytes

CEC_TX_DATA3_0

Address: Operational Base + offset (0x2024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cec_txbuffer_data_3 CEC Transmitter Buffer - Byte 3
23:16	RW	0x00	cec_txbuffer_data_2 CEC Transmitter Buffer - Byte 2
15:8	RW	0x00	cec_txbuffer_data_1 CEC Transmitter Buffer - Byte 1

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_txbuffer_data_0 CEC Transmitter Buffer - Byte 0

CEC_TX_DATA7_4
Address: Operational Base + offset (0x2028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cec_txbuffer_data_7 CEC Transmitter Buffer - Byte 7
23:16	RW	0x00	cec_txbuffer_data_6 CEC Transmitter Buffer - Byte 6
15:8	RW	0x00	cec_txbuffer_data_5 CEC Transmitter Buffer - Byte 5
7:0	RW	0x00	cec_txbuffer_data_4 CEC Transmitter Buffer - Byte 4

CEC_TX_DATA11_8
Address: Operational Base + offset (0x202C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cec_txbuffer_data_11 CEC Transmitter Buffer - Byte 11
23:16	RW	0x00	cec_txbuffer_data_10 CEC Transmitter Buffer - Byte 10
15:8	RW	0x00	cec_txbuffer_data_9 CEC Transmitter Buffer - Byte 9
7:0	RW	0x00	cec_txbuffer_data_8 CEC Transmitter Buffer - Byte 8

CEC_TX_DATA15_12
Address: Operational Base + offset (0x2030)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cec_txbuffer_data_15 CEC Transmitter Buffer - Byte 15
23:16	RW	0x00	cec_txbuffer_data_14 CEC Transmitter Buffer - Byte 14
15:8	RW	0x00	cec_txbuffer_data_13 CEC Transmitter Buffer - Byte 13
7:0	RW	0x00	cec_txbuffer_data_12 CEC Transmitter Buffer - Byte 12

CEC_RX_COUNT_STATUS
Address: Operational Base + offset (0x2040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RO	0x0	cec_rxbuffer_cnt Received frame message size in bytes, including Header and Data blocks 4'b0000: 1 byte received 4'b0001: 2 bytes received 4'b0010: 3 bytes received 4'b0011: 4 bytes received 4'b0100: 5 bytes received 4'b0101: 6 bytes received 4'b0110: 7 bytes received 4'b0111: 8 bytes received 4'b1000: 9 bytes received 4'b1001: 10 bytes received 4'b1010: 11 bytes received 4'b1011: 12 bytes received 4'b1100: 13 bytes received 4'b1101: 14 bytes received 4'b1110: 15 bytes received 4'b1111: 16 bytes received

CEC_RX_DATA3_0

Address: Operational Base + offset (0x2044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cec_rxbuffer_data_3 CEC Receiver Buffer - Byte 3
23:16	RO	0x00	cec_rxbuffer_data_2 CEC Receiver Buffer - Byte 2
15:8	RO	0x00	cec_rxbuffer_data_1 CEC Receiver Buffer - Byte 1
7:0	RO	0x00	cec_rxbuffer_data_0 CEC Receiver Buffer - Byte 0

CEC_RX_DATA7_4

Address: Operational Base + offset (0x2048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cec_rxbuffer_data_7 CEC Receiver Buffer - Byte7
23:16	RO	0x00	cec_rxbuffer_data_6 CEC Receiver Buffer - Byte6
15:8	RO	0x00	cec_rxbuffer_data_5 CEC Receiver Buffer - Byte5
7:0	RO	0x00	cec_rxbuffer_data_4 CEC Receiver Buffer - Byte 4

CEC_RX_DATA11_8

Address: Operational Base + offset (0x204C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cec_rxbuffer_data_11 CEC Receiver Buffer - Byte11
23:16	RO	0x00	cec_rxbuffer_data_10 CEC Receiver Buffer - Byte10
15:8	RO	0x00	cec_rxbuffer_data_9 CEC Receiver Buffer - Byte9
7:0	RO	0x00	cec_rxbuffer_data_8 CEC Receiver Buffer - Byte8

CEC_RX_DATA15_12

Address: Operational Base + offset (0x2050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cec_rxbuffer_data_15 CEC Receiver Buffer - Byte15
23:16	RO	0x00	cec_rxbuffer_data_14 CEC Receiver Buffer - Byte14
15:8	RO	0x00	cec_rxbuffer_data_13 CEC Receiver Buffer - Byte13
7:0	RO	0x00	cec_rxbuffer_data_12 CEC Receiver Buffer - Byte12

CEC_LOCK_CONTROL

Address: Operational Base + offset (0x2054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	locked_rxbuffer_clr_p Write 1 to this bit to unlock the RX buffer and allow the controller to receive a new incoming message

CEC_RXQUAL_BITTIME_CONFIG

Address: Operational Base + offset (0x2060)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x3	rxqual_follbit_timet8_earlstart RX qualifier bit time for T8, the earliest time of the start of a new bit. Any fall edge before this time puts the bit qualifier FSM in abort state. 3'b000: 1.90ms 3'b001: 1.95ms 3'b010: 2.00ms 3'b011: 2.04ms 3'b100: 2.10ms 3'b101: 2.15ms 3'b110: 2.20ms 3'b111: 2.25ms
15	RO	0x0	reserved
14:12	RW	0x3	rxqual_follbit_timet7_laterethigh RX qualifier bit time for T7, the latest return to high time. Any edge after this time puts the bit qualifier FSM in abort state. 3'b000: 1.55ms 3'b001: 1.60ms 3'b010: 1.65ms 3'b011: 1.71ms 3'b100: 1.75ms 3'b101: 1.80ms 3'b110: 1.85ms 3'b111: 1.90ms
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x3	rxqual_follbit_timet6_earlrethigh RX qualifier bit time for T6, the earliest return to high time. Any edge before this time puts the bit qualifier FSM in abort state. 3'b000: 1.15ms 3'b001: 1.20ms 3'b010: 1.25ms 3'b011: 1.29ms 3'b100: 1.35ms 3'b101: 1.40ms 3'b110: 1.45ms 3'b111: 1.50ms
7	RO	0x0	reserved
6:4	RW	0x3	rxqual_follbit_timet3_laterethigh RX qualifier bit time for T3, the latest return to high time. Any edge after this time puts the bit qualifier FSM in abort state. 3'b000: 0.65ms 3'b001: 0.7ms 3'b010: 0.75ms 3'b011: 0.81ms 3'b100: 0.85ms 3'b101: 0.90ms 3'b110: 0.95ms 3'b111: 1.00ms
3	RO	0x0	reserved
2:0	RW	0x3	rxqual_follbit_timet2_earlrethigh RX qualifier bit time for T2, the earliest return to high time. Any edge before this time puts the bit qualifier FSM in abort state. 3'b000: 0.25ms 3'b001: 0.30ms 3'b010: 0.35ms 3'b011: 0.39ms 3'b100: 0.45ms 3'b101: 0.50ms 3'b110: 0.55ms 3'b111: 0.6ms

CEC_RX_BITTIME_CONFIG

Address: Operational Base + offset (0x2064)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

Bit	Attr	Reset Value	Description
22:20	RW	0x3	rx_follbit_timet9_auto_ack When RX automatic ACK bit is enabled(rx_automatic_drive_acknowledge = 1) and current bit is EOM, the follower drives CEC line to zero thus starting the NACK/ ACK bit time. This correspond to the end of a bit(time T9) 3'b000: 2.50ms 3'b001: 2.55ms 3'b010: 2.60ms 3'b011: 2.65ms 3'b100: 2.70ms 3'b101: 2.75ms 3'b110: 2.80ms 3'b111: 2.85ms When RX automatic ACK bit is disabled (rx_automatic_drive_acknowledge = 0), the maximum bit time is defined by rx_follbit_timet9_endframe field register
19	RO	0x0	reserved
18:16	RW	0x3	rx_startbit_timet4_latend RX start bit time for T4, the latest time of the start of a new bit. If a fall edge is not detected before this time, the maximum width of a start bit has been exceeded and so the start bit is aborted. 3'b000: 4.55ms 3'b001: 4.60ms 3'b010: 4.65ms 3'b011: 4.71ms 3'b100: 4.75ms 3'b101: 4.80ms 3'b110: 4.85ms 3'b111: 4.9ms
15	RO	0x0	reserved
14:12	RW	0x3	rx_startbit_timet3_earlend RX start bit time for T3, the earliest end of a start bit. Any edge before this time aborts the start bit. 3'b000: 4.15ms 3'b001: 4.20ms 3'b010: 4.25ms 3'b011: 4.29ms 3'b100: 4.35ms 3'b101: 4.40ms 3'b110: 4.45ms 3'b111: 4.50ms
11	RO	0x0	reserved
10:8	RW	0x3	rx_startbit_timet2_laterethigh RX start bit time for T2, the earliest return to high time. A fall edge after this time aborts the start bit. 3'b000: 3.75ms 3'b001: 3.80ms 3'b010: 3.85ms 3'b011: 3.91ms 3'b100: 3.95ms 3'b101: 4.00ms 3'b110: 4.05ms 3'b111: 4.10ms
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x3	rx_startbit_timet1_earlrethigh RX start bit time for T1, the earliest return to high time. Any edge before this time aborts the start bit. 3'b000: 3.35ms 3'b001: 3.40ms 3'b010: 3.45ms 3'b011: 3.49ms 3'b100: 3.55ms 3'b101: 3.60ms 3'b110: 3.65ms 3'b111: 3.7ms
3	RO	0x0	reserved
2:0	RW	0x3	rx_follbit_timet9_endframe RX follower bit time for T9, the end of a frame. An edge after this time is considered as part of n new frame. 3'b000: 2.60ms 3'b001: 2.65ms 3'b010: 2.70ms 3'b011: 2.76ms 3'b100: 2.80ms 3'b101: 2.85ms 3'b110: 2.90ms 3'b111: 2.95ms

CEC_TX_BITTIME_CONFIG

Address: Operational Base + offset (0x2068)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x6	tx_round_trip_delay TX round trip delay. The CEC input line is sampled after this delay to check if the drive zero of the CEC output is in fact in the line. This value is greater than the fall edge output delay of the CEC line output. 3'b000: 0.02ms 3'b001: 0.04ms 3'b010: 0.06ms 3'b011: 0.08ms 3'b100: 0.10ms 3'b101: 0.13ms 3'b110: 0.16ms 3'b111: 0.20ms Note:With the filter ON, the value below 0.1ms works as the interrupt, drive_err_irq triggers since the delay caused by the filter is already greater than the specified value.
27	RO	0x0	reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x3	tx_startbit_time_risesample TX start bit rise sample. This is the time(counted from the fall edge of the startbit)when the CEC input line is sampled to check if the line is zero. 3'b000: 3.75ms 3'b001: 3.80ms 3'b010: 3.85ms 3'b011: 3.91ms 3'b100: 3.95ms 3'b101: 4.00ms 3'b110: 4.05ms 3'b111: 4.10ms From this time on (and until the next bit fall edge), if the CEC line is zero the arbitration lost interrupt is triggered.
23	RO	0x0	reserved
22:20	RW	0x4	tx_startbit_time_totalduration TX start bit total duration. This is the time when the next bit starts 3'b000: 4.30ms(or 4.40ms when CEC Filter is enabled) 3'b001: 4.35ms(or 4.40ms when CEC Filter is enabled) 3'b010: 4.40ms 3'b011: 4.45ms 3'b100: 4.50ms 3'b101: 4.55ms 3'b110: 4.60ms 3'b111: 4.65ms
19	RO	0x0	reserved
18:16	RW	0x4	tx_startbit_time_lh_trans TX start bit low to high transition time. This is the duration of the low period of the start bit 3'b000: 3.50ms 3'b001: 3.55ms 3'b010: 3.60ms 3'b011: 3.65ms 3'b100: 3.70ms 3'b101: 3.75ms 3'b110: 3.80ms 3'b111: 3.85ms
15	RO	0x0	reserved
14:12	RW	0x4	tx_err_notify_time TX error notify time. This is the duration of the low logic value of the CEC line for an error notification 3'b000: 3.40ms 3'b001: 3.45ms 3'b010: 3.50ms 3'b011: 3.55ms 3'b100: 3.60ms 3'b101: 3.65ms 3'b110: 3.70ms 3'b111: 3.75ms
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x4	tx_bit_time_period TX initiator data bit period. The time when a new consecutive bit starts. 3'b000: 2.20ms 3'b001: 2.25ms 3'b010: 2.30ms 3'b011: 2.35ms 3'b100: 2.40ms 3'b101: 2.45ms 3'b110: 2.50ms 3'b111: 2.55ms
7	RO	0x0	reserved
6:4	RW	0x4	tx_bit_time_rethigh TX initiator return to high data bit time when indicating a logic bit 0(zero) 3'b000: 1.30ms 3'b001: 1.35ms 3'b010: 1.40ms 3'b011: 1.45ms 3'b100: 1.50ms 3'b101: 1.55ms 3'b110: 1.60ms 3'b111: 1.65ms
3	RO	0x0	reserved
2:0	RW	0x4	tx_bit_time_lh_trans TX initiator low to high data bit transition time when indicating a logical 1(one) 3'b000: 0.40ms 3'b001: 0.45ms 3'b010: 0.50ms 3'b011: 0.55ms 3'b100: 0.60ms 3'b101: 0.65ms 3'b110: 0.70ms 3'b111: 0.75ms

DMA_CONFIG1

Address: Operational Base + offset (0x4400)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	uv_wid AXI DMA UV component id
27:24	RW	0x0	y_wid AXI DMA Y component id
23:16	RW	0x00	dummy_value If input format is yuv420_10bit/yuv422_10bit, and store format is yuv420_16bit/yuv422_16bit, dummy_value is the 6bit padding value.

Bit	Attr	Reset Value	Description
15:12	RW	0x0	ddr_store_format DDR store format. 4'b0000: RGB888 4'b0001: RGBA8888/ARGB8888(input rgb888) 4'b0010: YUV420_8BIT 4'b0011: YUV420_10BIT 4'b0100: YUV422_8BIT 4'b0101: YUV422_10BIT 4'b0110: YUV444_8BIT 4'b0111: Reserved 4'b1000: YUV420_16BIT(input yuv420_10bit) 4'b1001: YUV422_16BIT(input yuv422_10bit) 4'b1010-4'b1111: Reserved
11:4	RW	0x00	alpha_value If input format is rgb888, and store format in DDR is argb8888/ rgba8888, it must be configured 8bit alpha component.
3	RW	0x0	padding_position_en This signal will enable padding position. If input format is rgb888, and store format in DDR is argb8888/ rgba8888, it must pad 8bit alpha component. If input format is yuv420_10bit/yuv422_10bit and store format in DDR is yuv420_ 16bit/yuv422_16bit, it must pad 6bit. 1'b0: Pad in MSB 1'b1: Pad in LSB
2:1	RO	0x0	reserved
0	RW	0x0	abandon_en If HDMIRX lock, this signal enable DMA 1'b0: DMA will store the data, even hdmirx_lock is disable 1'b1: DMA will store the data after hdmirx_lock enable, if hdmirx_ lock is disable the input will be treated as unvalid data, and input data will be abandoned

DMA_CONFIG2
Address: Operational Base + offset (0x4404)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frame_addr_y DMA Y component store starting address

DMA_CONFIG3
Address: Operational Base + offset (0x4408)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frame_addr_uv DMA UV component store starting address

DMA_CONFIG4
Address: Operational Base + offset (0x440C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	line_flag_int_en Line flag interrupt enable
7	RW	0x0	hdmirx_dma_idle_int_en HDMIRX DMA idle interrupt enable
6	RW	0x0	hdmirx_lock_disable_int_en HDMIRX lock disable interrupt enable

Bit	Attr	Reset Value	Description
5	RW	0x0	last_frame_axi_unfinish_int_en Last frame AXI unfinish interrupt enable
4	RW	0x0	false_frame_end_int_en False frame end interrupt enable
3	RW	0x0	timing_mismatch_int_en Timing mismatch interrupt enable
2	RW	0x0	fifo_overflow_int_en HDMIRX DMA FIFO overflow interrupt enable
1	RW	0x0	fifo_underflow_int_en HDMIRX DMA FIFO underflow interrupt enable
0	RW	0x0	hdmirx_axi_error_int_en HDMIRX DMA AXI error interrupt enable

DMA_CONFIG5

Address: Operational Base + offset (0x4410)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	W1C	0x0	line_flag_int_clear_en Enable to clear line flag interrupt
7	W1C	0x0	hdmirx_dma_idle_int_clear_en Enable to clear HDMIRX DMA idle interrupt
6	W1C	0x0	hdmirx_lock_disable_int_clear_en Enable to clear HDMIRX lock disable interrupt
5	W1C	0x0	last_frame_axi_unfinish_int_clear_en Enable to clear last frame AXI unfinish interrupt
4	W1C	0x0	false_frame_end_int_clear_en Enable to clear false frame end interrupt
3	W1C	0x0	timing_mismatch_int_clear_en Enable to clear timing mismatch interrupt
2	RW	0x0	fifo_overflow_int_clear_en Enable to clear HDMIRX DMA FIFO overflow interrupt
1	W1C	0x0	fifo_underflow_int_clear_en Enable to clear HDMIRX DMA FIFO underflow interrupt
0	W1C	0x0	hdmirx_axi_error_int_clear_en Enable to clear HDMIRX DMA AXI error interrupt

DMA_CONFIG6

Address: Operational Base + offset (0x4414)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:14	RW	0x0000	pixel_blank_threshold Pixel blank threshold. When pixel blank count greater than pixel_blank_threshold in active line, it will be treated as a false line end, which is used for generate false_frame_end signal.
13	RW	0x0	hdmirx_lock_mode HDMIRX lock mode 1'b0: If HDMIRX lock drive "0" in half frame, the HDMIRX lock detection will output directly, and the input data will be discarded right now. 1'b1: If HDMIRX lock drive "0" in half frame, the HDMIRX lock detection will record this event , and the input data will be received until current whole frame finish, and next frame will be discarded.

Bit	Attr	Reset Value	Description
12	RW	0x0	axi_unfinish_disable last frame AXI unfinish detection enable 1'b0: Last_frame_axi_unfinish will be detection in every frame 1'b1: Last_frame_axi_unfinish will not be detection
11	RW	0x0	axi_unfinish_state_clear_en 1'b0: If last_frame_axi_unfinish has been detected, last_frame_axi_unfinish will not be set 0 manually 1'b1: If last_frame_axi_unfinish has been detected, last_frame_axi_unfinish will be set 0 manually
10	RW	0x0	fifo_overflow_flag_disable FIFO overflow flag disable enable 1'b0: FIFO_overflow_flag will not be set 0 until next new start 1'b1: FIFO_overflow_flag will be set 0 manually
9	RW	0x0	uv_swap_en Input data uv swap enable 1'b0: Input data will not be uv swap 1'b1: Input data will be uv swap
8	RW	0x0	last_frame_axi_unfinish_num_clear_en Last frame AXI unfinish number clear enable. 1'b0: Last frame AXI unfinish number will not be set 0 1'b1: Last frame AXI unfinish number will be set 0, and will be sum from 0 again
7	RW	0x0	timing_mismatch_int_mode Timing detection mode selection 1'b0: The detection width/height will compare with the last frame width/height 1'b1: The detection width/height will compare with the last frame width/height and The detection width/height will compare with width/height corresponding to VIC value
6	RW	0x0	field_toggle_en FIELD signal inversion enable 1'b0: FIELD will not be inverted 1'b1: FIELD will be inverted
5	RW	0x0	hsync_toggle_en HSYNC signal inversion enable 1'b0: HSYNC will not be inverted 1'b1: HSYNC will be inverted
4	RW	0x0	vsync_toggle_en VSYNC signal inversion enable 1'b0: VSYNC will not be inverted 1'b1: VSYNC will be inverted
3	RW	0x0	pic_height_pick_vid_value_en When detect false frame end, the line count will compare the picture height 1'b0: Line count will compare with the picture height corresponding to vic value 1'b1: Line count will compare with the last frame's picture height
2	RW	0x0	timing_mismatch_int_detection_en HDMIRX timing detection enable
1	RW	0x0	hdmirx_dma_en HDMIRX DMA output enable 1'b0: The input from HDMIRX controller will be discarded 1'b1: The input from HDMIRX controller will be received

Bit	Attr	Reset Value	Description
0	RW	0x0	false_frame_end_en 1'b0: The false frame end will be discarded 1'b1: The false frame end will be treated valid frame end

DMA_CONFIG7

Address: Operational Base + offset (0x4418)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	line_flag_num If line count greater than line_flag_num, will trigger line_flag_int interrupt.
15:12	RO	0x0	reserved
11:0	RW	0x000	lock_frame_num HDMIRX DMA will detect hdmirx_lock signal, if hdmirx_lock has been driven "1" with continuous lock_frame_num frame, the input data stream will be treated as valid data, and HDMIRX DMA will receive input data stream.

DMA_CONFIG8

Address: Operational Base + offset (0x441C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	reg_mirror_en HDMIRX DMA register configuration mode 1'b0: HDMIRX DMA register will be in function directly after configuration 1'b1: HDMIRX DMA register will be in function in next frame

DMA_CONFIG9

Address: Operational Base + offset (0x4420)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	vic_value Vic value

DMA_CONFIG10

Address: Operational Base + offset (0x4424)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	edid_wdata EDID wdata

DMA_CONFIG11

Address: Operational Base + offset (0x4428)

Bit	Attr	Reset Value	Description
31:16	RW	0x6001	segment_pointer_addr Before HDMITX read EDID 256-511 address section, DDC will send segment pointer address(0x60) and CMD(0x01). If it is matched, DDC bus will read the EDID 256-511 address section.
15:12	RO	0x0	reserved
11	RW	0x0	edid_read_block1_en 1'b0: Reading EDID block1 segment with slave address 1'b1: Reading EDID block1 segment manually even though slave address mismatch

Bit	Attr	Reset Value	Description
10	RW	0x0	edid_i2c_arbiter_disable 1'b0: DDC bus will arbiter for HDMIRX controller for SCDC/HDCP manually even though EDID slave address match 1'b1: DDC bus will arbiter based on slave address match
9	RW	0x0	edid_i2c_arbiter_en 1'b0: Read the EDID SRAM through DDC bus just in I2C slave address match 1'b1: Read the EDID SRAM through DDC bus even though I2C slave address mismatch
8	RW	0x0	edid_read_en EDID read enable through APB bus
7	RW	0x0	edid_write_en EDID write enable through APB bus
6:0	RW	0x50	edid_slave_addr EDID slave address

DMA_STATUS1
Address: Operational Base + offset (0x4430)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	line_flag_int Line flag interrupt status
7	RO	0x0	hdmirx_dma_idle_int HDMIRX DMA idle interrupt status
6	RO	0x0	hdmirx_lock_disable_int HDMIRX lock disable interrupt status
5	RO	0x0	last_frame_axi_unfinish_int Last frame AXI unfinish interrupt status
4	RO	0x0	false_frame_end_int False frame end interrupt status
3	RO	0x0	timing_mismatch_int Timing mismatch interrupt status
2	RO	0x0	fifo_overflow_int FIFO overflow interrupt status
1	RO	0x0	fifo_underflow_int FIFO underflow interrupt status
0	RO	0x0	hdmirx_axi_error_int HDMIRX AXI error interrupt status

DMA_STATUS2
Address: Operational Base + offset (0x4434)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pic_width Picture width
15:0	RO	0x0000	pic_height Picture height

DMA_STATUS3
Address: Operational Base + offset (0x4438)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pic_width_total Picture total width
15:0	RO	0x0000	pic_height_total Picture total height

DMA_STATUS4
Address: Operational Base + offset (0x443C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	picture_width_sync HSYNC cycle number
15:0	RO	0x0000	pic_height_sync VSYNC cycle number

DMA_STATUS5
Address: Operational Base + offset (0x4440)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pic_width_back HBACK cycle number
15:0	RO	0x0000	pic_height_back VBACK cycle number

DMA_STATUS6
Address: Operational Base + offset (0x4444)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdmirx_error_axi_cmd1 The last AXI CMD when AXI error interrupt. This CMD is awaddr [31:0].

DMA_STATUS7
Address: Operational Base + offset (0x4448)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdmirx_error_axi_cmd2 The last AXI CMD when AXI error interrupt. [0]: Awready [1]: Awvalid [2:3]: Awlock [4:6]: Awprot [7:10]: Awcache [11:12]: Awburst [13:15]: Awsize [16:19]: Awid [20:23]: Awlen [24:25]: Bresp [26:31]: Reserved

DMA_STATUS8
Address: Operational Base + offset (0x444C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdmirx_error_axi_last_second_cmd1 The last second AXI CMD when AXI error interrupt. This CMD is awaddr[31:0].

DMA_STATUS9
Address: Operational Base + offset (0x4450)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hdmirx_error_axi_last_second_cmd2 The last second AXI CMD when AXI error interrupt. [0]: Awready [1]: Awvalid [2:3]: Awlock [4:6]: Awprot [7:10]: Awcache [11:12]: Awburst [13:15]: Awsize [16:19]: Awid [20:23]: Awlen [24:25]: Bresp [26:31]: Reserved

DMA_STATUS10

Address: Operational Base + offset (0x4454)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	line_flag_raw_int Line flag raw interrupt status
16	RO	0x0	hdmi_int HDMIRX controller interrupt status
15:6	RO	0x000	axi_unfinish_frame_num AXI unfinish frame number
5	RO	0x0	interlace_en HDMIRX interlace status
4	RO	0x0	hdmirx_dma_idle hdmirx_dma_idle status
3	RO	0x0	hdmirx_lock hdmirx_lock status
2	RO	0x0	timing_mismatch_raw_int Timing mismatch raw interrupt status
1	RO	0x0	fifo_overflow_raw_int FIFO overflow raw interrupt status
0	RO	0x0	fifo_underflow_raw_int FIFO underflow raw interrupt status

DMA_STATUS11

Address: Operational Base + offset (0x4458)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	avmute HDMIRX avmute status

Bit	Attr	Reset Value	Description
24:9	RO	0x0000	decodemode [3:0]: Busd_decodemode [7:4]: Busc decodemode [11:8]: Busb_decodemode [15:12]: Busa_decodemode busX_decodemode[3:0] map 4'b0000: Unknown 4'b0001: Control 4'b0010: Data island preamble 4'b0011: Video preamble 4'b0100: Data island leading guard band 4'b0101: Data island trailing guard band 4'b0110: Video leading guard band 4'b0111: Data island 4'b1000: Video 4'b10001-4'b1111: Reserved
8:7	RO	0x0	hdmirx_type HDMIRX type 2’b00: Progressive 2’b01: Interlaced 2’b10: 3D Progressive 2’b11: 3D Interlaced
6:3	RO	0x0	hdmirx_color_depth HDMIRX color_depth 4’b0100: 24bits 4’b0101: 30bits 4’b0110: 36bits 4’b0111: 48bits Others: Reserved
2:0	RO	0x0	hdmirx_format HDMIRX format 3’b000: RGB 3’b001: YCbCr 4:2:2 3’b010: YCbCr 4:4:4 3’b011: YCbCr 4:2:0 Others: Reserved

DMA_STATUS12

Address: Operational Base + offset (0x445C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	line_cnt_debug [15:0]: UV CMD line count for debug [31:16]: CMD line count for debug

DMA_STATUS13

Address: Operational Base + offset (0x4460)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	line_cnt_valid HDMIRX controller valid line count

DMA_STATUS14

Address: Operational Base + offset (0x4464)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	RO	0x0	edid_read_block1_flag1 EDID I2C has receive the CMD 0x60, that is 0x60 is segment pointer address
26	RO	0x0	edid_read_block1_flag2 EDID I2C has receive the CMD 0x01
25	RO	0x0	edid_read_block1_flag EDID I2C has receive the whole CMD 0x6001, that is 0x60 is segment pointer address, 0x01 is the specific I2C CMD
24:17	RO	0x00	edid_i2c_raddr EDID I2C read address
16	RO	0x0	edid_read_flag 1'b0: HDMIRX has the DDC access authority for SCDC/HDCP 1'b1: It indicates EDID has been granted DDC access authority
15:8	RO	0x00	reserved
7:0	RO	0x00	edid_rdata EDID rdata

MAINUNIT_INTVEC_INDEX

Address: Operational Base + offset (0x5000)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RO	0x0	hdcp_1_intvec HDCP 1 interrupt Vector triggered
13	RO	0x0	hdcp_intvec HDCP interrupt Vector triggered
12	RO	0x0	scdc_intvec SCDC Interrupt Vector triggered
11	RO	0x0	reserved
10	RO	0x0	pkt_2_intvec Packet 2 Interrupt Vector triggered
9	RO	0x0	pkt_1_intvec Packet 1 Interrupt Vector triggered
8	RO	0x0	pkt_0_intvec Packet 0 Interrupt Vector triggered
7	RO	0x0	reserved
6	RO	0x0	avpunit_2_intvec AVPUNIT 2 interrupt Vector triggered
5	RO	0x0	avpunit_1_intvec AVPUNIT 1 interrupt Vector triggered
4	RO	0x0	avpunit_0_intvec AVPUNIT 0 interrupt Vector triggered
3	RO	0x0	reserved
2	RO	0x0	mainunit_2_intvec Main unit 2 interrupt Vector triggered
1	RO	0x0	mainunit_1_intvec Main unit 1 interrupt Vector triggered
0	RO	0x0	mainunit_0_intvec Main unit 0 interrupt Vector triggered

MAINUNIT_0_INT_STATUS

Address: Operational Base + offset (0x5010)

Bit	Attr	Reset Value	Description
31	RO	0x0	regbank_ready_irq Register Bank ready interrupt. Indicates all non-powered off units between AVPUNIT, PKTFIFO, and CEC are ready.
30	RO	0x0	apb_if_ready_irq APB interface ready interrupt
29:27	RO	0x0	reserved
26	RO	0x0	timer_base_locked_irq Timer Base locked interrupt
25:8	RO	0x00000	reserved
7	RO	0x0	cr_para_clk_off_chg_irq CR_PARA Clock(icr_para_clk) is off(not running)change interrupt
6	RO	0x0	cr_para_clk_locked_chg_irq CR_PARA Clock(icr_para_clk)locked change interrupt
5	RO	0x0	tmdsqpclk_off_chg_irq TMDS QP Clock(itmdsqpclk) is off(not running) change interrupt
4	RO	0x0	tmdsqpclk_locked_chg_irq TMDS QP Clock(itmdsqpclk) locked change interrupt
3:2	RO	0x0	reserved
1	RO	0x0	audclk_off_chg_irq Audio Clock(iaudclk) is off(not running) change interrupt
0	RO	0x0	audclk_locked_chg_irq Audio clock(iaudclk)locked change interrupt

MAINUNIT_0_INT_MASK_N

Address: Operational Base + offset (0x5014)

Bit	Attr	Reset Value	Description
31	RW	0x1	regbank_ready_mask_n Write 1 to unmask regbank_ready_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
30	RW	0x1	apb_if_ready_mask_n Write 1 to unmask apb_if_ready_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
29:27	RO	0x0	reserved
26	RW	0x0	timer_base_locked_mask_n Write 1 to unmask timer_base_locked_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
25:8	RO	0x00000	reserved
7	RW	0x0	cr_para_clk_off_chg_mask_n Write 1 to unmask cr_para_clk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
6	RW	0x0	cr_para_clk_locked_chg_mask_n Write 1 to unmask cr_para_clk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
5	RW	0x0	tmdsqpclk_off_chg_mask_n Write 1 to unmask tmdsqpclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
4	RW	0x0	tmdsqpclk_locked_chg_mask_n Write 1 to unmask tmdsqpclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
3:2	RO	0x0	reserved
1	RW	0x0	audclk_off_chg_mask_n Write 1 to unmask audclk_off_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
0	RW	0x0	audclk_locked_chg_mask_n Write 1 to unmask audclk_locked_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

MAINUNIT_0_INT_CLEAR

Address: Operational Base + offset (0x5018)

Bit	Attr	Reset Value	Description
31	WO	0x0	regbank_ready_clear Write 1 to reset regbank_ready_irq
30	WO	0x0	apb_if_ready_clear Write 1 to reset apb_if_ready_irq
29:27	RO	0x0	reserved
26	WO	0x0	timer_base_locked_clear Write 1 to reset timer_base_locked_irq
25:8	RO	0x00000	reserved
7	WO	0x0	cr_para_clk_off_chg_clear Write 1 to reset cr_para_clk_off_chg_irq
6	WO	0x0	cr_para_clk_locked_chg_clear Write 1 to reset cr_para_clk_locked_chg_irq
5	WO	0x0	tmdsqpclk_off_chg_clear Write 1 to reset tmdsqpclk_off_chg_irq
4	WO	0x0	tmdsqpclk_locked_chg_clear Write 1 to reset tmdsqpclk_locked_chg_irq
3:2	RO	0x0	reserved
1	WO	0x0	audclk_off_chg_clear Write 1 to reset audclk_off_chg_irq
0	WO	0x0	audclk_locked_chg_clear Write 1 to reset audclk_locked_chg_irq

MAINUNIT_0_INT_FORCE

Address: Operational Base + offset (0x501C)

Bit	Attr	Reset Value	Description
31	WO	0x0	regbank_ready_force Write 1 to trigger regbank_ready_irq
30	WO	0x0	apb_if_ready_force Write 1 to trigger apb_if_ready_irq
29:27	RO	0x0	reserved
26	WO	0x0	timer_base_locked_force Write 1 to trigger timer_base_locked_irq
25:8	RO	0x00000	reserved
7	WO	0x0	cr_para_clk_off_chg_force Write 1 to trigger cr_para_clk_off_chg_irq
6	WO	0x0	cr_para_clk_locked_chg_force Write 1 to trigger cr_para_clk_locked_chg_irq
5	WO	0x0	tmdsqpclk_off_chg_force Write 1 to trigger tmdsqpclk_off_chg_irq
4	WO	0x0	tmdsqpclk_locked_chg_force Write 1 to trigger tmdsqpclk_locked_chg_irq
3:2	RO	0x0	reserved
1	WO	0x0	audclk_off_chg_force Write 1 to trigger audclk_off_chg_irq
0	WO	0x0	audclk_locked_chg_force Write 1 to trigger audclk_locked_chg_irq

MAINUNIT_1_INT_STATUS

Address: Operational Base + offset (0x5020)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	ddc_scdc_activity_irq Indicates DDC(I2C) activity addressing SCDC
20	RO	0x0	ddc_hdcp_activity_irq Indicates DDC(I2C) activity addressing HDCP
19:14	RO	0x00	reserved
13	RO	0x0	cec_powered_down_irq Indicates that the CEC has reached the power down status
12	RO	0x0	cec_powered_up_irq Indicates that the CEC has reached the power up status
11:2	RO	0x000	reserved
1	RO	0x0	avpunit_powered_down_irq Indicates that the AVPUNIT has reached the power down status
0	RO	0x0	avpunit_powered_up_irq Indicates that the AVPUNIT has reached the power up status

MAINUNIT_1_INT_MASK_N

Address: Operational Base + offset (0x5024)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	ddc_scdc_activity_mask_n Write 1 to unmask ddc_scdc_activity_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
20	RW	0x0	ddc_hdcp_activity_mask_n Write 1 to unmask ddc_hdcp_activity_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
19:14	RO	0x00	reserved
13	RW	0x0	cec_powered_down_mask_n Write 1 to unmask cec_powered_down_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
12	RW	0x0	cec_powered_up_mask_n Write 1 to unmask cec_powered_up_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
11:2	RO	0x000	reserved
1	RW	0x0	avpunit_powered_down_mask_n Write 1 to unmask avpunit_powered_down_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
0	RW	0x0	avpunit_pwoered_up_mask_n Write 1 to unmask avpunit_powered_up_irq. The interrupt line is asserted if the corresponding interrupt is asserted

MAINUNIT_1_INT_CLEAR

Address: Operational Base + offset (0x5028)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	ddc_scdc_activity_clear Write 1 to reset ddc_scdc_activity_irq
20	WO	0x0	ddc_hdcp_activity_clear Write 1 to reset ddc_hdcp_activity_irq
19:14	RO	0x00	reserved
13	WO	0x0	cec_powered_down_clear Write 1 to reset cec_powered_down_irq

Bit	Attr	Reset Value	Description
12	WO	0x0	cec_powered_up_clear Write 1 to reset cec_powered_up_irq
11:2	RO	0x000	reserved
1	WO	0x0	avpunit_powered_down_clear Write 1 to reset avpunit_powered_down_irq
0	WO	0x0	avpunit_powered_up_clear Write 1 to reset avpunit_powered_up_irq

MAINUNIT_1_INT_FORCE

Address: Operational Base + offset (0x502C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	ddc_scdc_activity_force Write 1 to trigger ddc_scdc_activity_irq
20	WO	0x0	ddc_hdcp_activity_force Write 1 to trigger ddc_hdcp_activity_irq
19:14	RO	0x00	reserved
13	WO	0x0	cec_powered_down_force Write 1 to trigger cec_powered_down_irq
12	WO	0x0	cec_powered_up_force Write 1 to trigger cec_powered_up_irq
11:2	RO	0x000	reserved
1	WO	0x0	avpunit_powered_down_force Write 1 to trigger avpunit_powered_down_irq
0	WO	0x0	avpunit_powered_up_force Write 1 to trigger avpunit_powered_up_irq

MAINUNIT_2_INT_STATUS

Address: Operational Base + offset (0x5030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	phycreg_cr_timeout_irq PHYCREG acknowledge timeout interrupt status.
11	RO	0x0	phycreg_cr_read_done_irq PHYCREG read done interrupt status
10	RO	0x0	phycreg_cr_write_done_irq PHYCREG write done interrupt status
9	RO	0x0	phycreg_cr_selector_done_irq PHYCREG selector mode interrupt status
8	RO	0x0	phycreg_cr_selectionmode_done_irq PHYCREG selection mode done interrupt status
7:2	RO	0x00	reserved
1	RO	0x0	tmdsvalid_stable_chg_irq TMDS valid stable change interrupt status
0	RO	0x0	audpll_lock_stable_chg_irq Audio PLL lock stable change interrupt status

MAINUNIT_2_INT_MASK_N

Address: Operational Base + offset (0x5034)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	phycreg_cr_timeout_mask_n Write 1 to unmask phycreg_cr_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
11	RW	0x0	phycreg_cr_read_done_mask_n Write 1 to unmask phycreg_cr_read_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
10	RW	0x0	phycreg_cr_write_done_mask_n Write 1 to unmask phycreg_cr_write_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
9	RW	0x0	phycreg_cr_selector_done_mask_n write 1 to unmask phycreg_cr_selector_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
8	RW	0x0	phycreg_cr_selectionmode_done_mask_n Write 1 to unmask phycreg_cr_selectionmode_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
7:2	RO	0x00	reserved
1	RW	0x0	tmdsvalid_stable_chg_mask_n Write 1 to unmask tmdsvalid_stable_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
0	RW	0x0	audpll_lock_stable_chg_mask_n Write 1 to unmask audpll_lock_stable_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted

MAINUNIT_2_INT_CLEAR

Address: Operational Base + offset (0x5038)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	WO	0x0	phycreg_cr_timeout_clear Write 1 to reset phycreg_cr_timeout_irq
11	WO	0x0	phycreg_cr_read_done_clear Write 1 to reset phycreg_cr_read_done_irq
10	WO	0x0	phycreg_cr_write_done_clear Write 1 to reset phycreg_cr_write_done_irq
9	WO	0x0	phycreg_cr_selector_done_clear Write 1 to reset phycreg_cr_selector_done_irq
8	WO	0x0	phycreg_cr_selectionmode_done_clear Write 1 to reset phycreg_cr_selectionmode_done_irq
7:2	RO	0x00	reserved
1	WO	0x0	tmdsvalid_stable_chg_clear Write 1 to reset tmdsvalid_stable_chg_irq
0	WO	0x0	audpll_lock_stable_chg_clear Write 1 to reset audpll_lock_stable_chg_irq

MAINUNIT_2_INT_FORCE

Address: Operational Base + offset (0x503C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	WO	0x0	phycreg_cr_timeout_force Write 1 to trigger phycreg_cr_timeout_irq
11	WO	0x0	phycreg_cr_read_done_force Write 1 to trigger phycreg_cr_read_done_irq
10	WO	0x0	phycreg_cr_write_done_force Write 1 to trigger phycreg_cr_write_done_irq
9	WO	0x0	phycreg_cr_selector_done_force Write 1 to trigger phycreg_cr_selector_done_irq

Bit	Attr	Reset Value	Description
8	WO	0x0	phycreg_cr_selectionmode_done_force Write 1 to trigger phycreg_cr_selectionmode_done_irq
7:2	RO	0x00	reserved
1	WO	0x0	tmdsvalid_stable_chg_force Write 1 to trigger tmdsvalid_stable_chg_irq
0	WO	0x0	audpll_lock_stable_chg_force Write 1 to trigger audpll_lock_stable_chg_irq

AVPUNIT_0_INT_STATUS

Address: Operational Base + offset (0x5040)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RO	0x0	ced_dyn_cnt_ch2_irq Dynamic Character Error Detection counter in channel2 reached configured threshold.
21	RO	0x0	ced_dyn_cnt_ch1_irq Dynamic Character Error Detection counter in channel1 reached configured threshold.
20	RO	0x0	ced_dyn_cnt_ch0_irq Dynamic Character Error Detection counter in channel0 reached configured threshold.
19:8	RO	0x000	reserved
7	RO	0x0	descrand_sync_seq_err_irq Descrambler and De-randomizer Synchronization sequence (Unscrambled Control Period)error interrupt flag status.
6:5	RO	0x0	reserved
4	RO	0x0	descrand_sync_irq Descrambler and De-randomizer Synchronization interrupt flag status. Triggered upon rise of descrand_sync_st.
3:0	RO	0x0	reserved

AVPUNIT_0_INT_MASK_N

Address: Operational Base + offset (0x5044)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	ced_dyn_cnt_ch2_mask_n Write 1 to unmask ced_dyn_cnt_ch2_irq. The interrupt is asserted if the corresponding interrupt is asserted.
21	RW	0x0	ced_dyn_cnt_ch1_mask_n Write 1 to unmask ced_dyn_cnt_ch1_irq. The interrupt is asserted if the corresponding interrupt is asserted.
20	RW	0x0	ced_dyn_cnt_ch0_mask_n Write 1 to unmask ced_dyn_cnt_ch0_irq. The interrupt is asserted if the corresponding interrupt is asserted.
19:8	RO	0x000	reserved
7	RW	0x0	descrand_sync_seq_err_mask_n Write 1 to unmask descrand_sync_seq_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
6:5	RO	0x0	reserved
4	RW	0x0	descrand_sync_mask_n Write 1 to unmask descrand_sync_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
3:0	RO	0x0	reserved

AVPUNIT_0_INT_CLEAR

Address: Operational Base + offset (0x5048)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	WO	0x0	ced_dyn_cnt_ch2_clear Write 1 to reset ced_dyn_cnt_ch2_irq
21	WO	0x0	ced_dyn_cnt_ch1_clear Write 1 to reset ced_dyn_cnt_ch1_irq
20	WO	0x0	ced_dyn_cnt_ch0_clear Write 1 to reset ced_dyn_cnt_ch0_irq
19:8	RO	0x000	reserved
7	WO	0x0	descrand_sync_seq_err_clear Write 1 to reset descrand_sync_seq_err_irq
6:5	RO	0x0	reserved
4	WO	0x0	descrand_sync_clear Write 1 to reset descrand_sync_irq
3:0	RO	0x0	reserved

AVPUNIT_0_INT_FORCE

Address: Operational Base + offset (0x504C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	WO	0x0	ced_dyn_cnt_ch2_force Write 1 to trigger ced_dyn_cnt_ch2_irq
21	WO	0x0	ced_dyn_cnt_ch1_force Write 1 to trigger ced_dyn_cnt_ch1_irq
20	WO	0x0	ced_dyn_cnt_ch0_force Write 1 to trigger ced_dyn_cnt_ch0_irq
19:8	RO	0x000	reserved
7	WO	0x0	descrand_sync_seq_err_force Write 1 to trigger descrand_sync_seq_err_irq
6:5	RO	0x0	reserved
4	WO	0x0	descrand_sync_force Write 1 to trigger descrand_sync_irq
3:0	RO	0x0	reserved

AVPUNIT_1_INT_STATUS

Address: Operational Base + offset (0x5050)

Bit	Attr	Reset Value	Description
31	RO	0x0	vmon_vmeas_irq Video monitor vertical measures update
30	RO	0x0	vmon_hmeas_irq Video Monitor horizontal measures update
29	RO	0x0	vstream_fifo_init_irq Video streamer - pixel FIFO init interrupt
28:25	RO	0x0	reserved
24	RO	0x0	aud_chstatus_sp3_irq Audio processor - sub-packet 3 Channel Status value updated
23	RO	0x0	aud_chstatus_sp2_irq Audio processor - sub-packet 2 Channel Status value updated
22	RO	0x0	aud_chstatus_sp1_irq Audio processor - sub-packet 1 Channel Status value updated
21	RO	0x0	aud_chstatus_sp0_irq Audio processor - sub-packet 0 Channel Status value updated

Bit	Attr	Reset Value	Description
20	RO	0x0	aud_mute_irq Audio processor - mute control changed
19	RO	0x0	afifo_underflow_irq Audio FIFO - memory empty when trying to read audio
18	RO	0x0	afifo_overflow_irq Audio FIFO - memory full when trying to write audio sample
17	RO	0x0	afifo_thr_mute_low_irq Audio FIFO - mute low threshold reached
16	RO	0x0	afifo_thr_mute_high_irq Audio FIFO - mute high threshold reached
15	RO	0x0	afifo_thr_low_irq Audio FIFO - low threshold reached
14	RO	0x0	afifo_thr_high_irq Audio FIFO - high threshold reached
13	RO	0x0	afifo_thr_pass_irq Audio FIFO - pass threshold reached
12	RO	0x0	aud_fmt_chg_irq Audio Processor - Audio packet format changed. This interrupt is triggered by the following events: (1)When audio_proc_config1.auddet_thr audio packets are received of a different type than what is currently active (2)When audio_proc_config1.auddet_thr packets of the same type are received after an Audio FIFO initialization
11	RO	0x0	vproc_syncgen_irq Video processor synchronism generator sync signal toggled during active video
10	RO	0x0	vproc_pp_diff_irq Video processor packing phase discrepancy counter
9	RO	0x0	vproc_cd_timeout_irq Video processor GCP Color Depth information has timed out
8	RO	0x0	vproc_cd_chg_irq Video processor color depth value changed
7	RO	0x0	vstream_fifo_overflow_irq Video streamer pixel FIFO overflow interrupt
6	RO	0x0	vstream_fifo_underflow_irq Video streamer pixel FIFO underflow interrupt
5	RO	0x0	vstream_fifo_almost_full_irq Video streamer pixel FIFO almost full interrupt
4	RO	0x0	vstream_fifo_almost_empty_irq Video Streamer pixel FIFO almost empty interrupt
3	RO	0x0	deframer_dvihdmi_chg_irq Change in automatic DVI/HDMI mode interrupt
2	RO	0x0	deframer_gbdet_err_irq De-Framer errors detected in Guard Band interrupt
1	RO	0x0	deframer_vsync_thr_reached_irq De-Framer Vertical Sync threshold reached interrupt
0	RO	0x0	deframer_vsync_irq De-Framer Vertical Sync interrupt

AVPUNIT_1_INT_MASK_N

Address: Operational Base + offset (0x5054)

Bit	Attr	Reset Value	Description
31	RW	0x0	vmon_vmeas_mask_n Write 1 to unmask vmon_vmeas_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
30	RW	0x0	vmon_hmeas_mask_n Write 1 to unmask vmon_hmeas_irq. The interrupt line is asserted if the corresponding interrupt is asserted
29	RW	0x0	vstream_fifo_init_mask_n Write 1 to unmask vstream_fifo_init_irq. The interrupt line is asserted if the corresponding interrupt is asserted
28:25	RO	0x0	reserved
24	RW	0x0	aud_chstatus_sp3_mask_n Write 1 to unmask aud_chstatus_sp3_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
23	RW	0x0	aud_chstatus_sp2_mask_n Write 1 to unmask aud_chstatus_sp2_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
22	RW	0x0	aud_chstatus_sp1_mask_n Write 1 to unmask aud_chstatus_sp1_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
21	RW	0x0	aud_chstatus_sp0_mask_n Write 1 to unmask aud_chstatus_sp0_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
20	RW	0x0	aud_mute_mask_n Write 1 to unmask aud_mute_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
19	RW	0x0	afifo_underflow_mask_n Write 1 to unmask afifo_underflow_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
18	RW	0x0	afifo_overflow_mask_n Write 1 to unmask afifo_overflow_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
17	RW	0x0	afifo_thr_mute_low_mask_n Write 1 to unmask afifo_thr_mute_low_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
16	RW	0x0	afifo_thr_mute_high_mask_n Write 1 to unmask afifo_thr_mute_high_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
15	RW	0x0	afifo_thr_low_mask_n Write 1 to unmask afifo_thr_low_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
14	RW	0x0	afifo_thr_high_mask_n Write 1 to unmask afifo_thr_high_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
13	RW	0x0	afifo_thr_pass_mask_n Write 1 to unmask afifo_thr_pass_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
12	RW	0x0	aud_fmt_chg_mask_n Write 1 to unmask aud_fmt_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
11	RW	0x0	vproc_syncgen_mask_n Write 1 to unmask vproc_syncgen_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
10	RW	0x0	vproc_pp_diff_mask_n Write 1 to unmask vproc_pp_diff_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
9	RW	0x0	vproc_cd_timeout_mask_n Write 1 to unmask vproc_cd_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
8	RW	0x0	vproc_cd_chg_mask_n Write 1 to unmask vproc_cd_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
7	RW	0x0	vstream_fifo_overflow_mask_n Write 1 to unmask vstream_fifo_overflow_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
6	RW	0x0	vstream_fifo_underflow_mask_n Write 1 to unmask vstream_fifo_underflow_irq. The interrupt line is asserted if the corresponding interrupt is asserted
5	RW	0x0	vstream_fifo_almost_full_mask_n Write 1 to unmask vstream_fifo_almost_full_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
4	RW	0x0	vstream_fifo_almost_empty_mask_n Write 1 to unmask vstream_fifo_almost_empty_irq. The interrupt line is asserted if the corresponding interrupt is asserted
3	RW	0x0	deframer_dvihdmi_chg_mask_n Write 1 to unmask deframer_dvihdmi_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
2	RW	0x0	deframer_gbdet_err_mask_n Write 1 to unmask deframer_gbdet_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
1	RW	0x0	deframer_vsync_thr_reached_mask_n Write 1 to unmask deframer_vsync_thr_reached_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
0	RW	0x0	deframer_vsync_mask_n Write 1 to unmask deframer_vsync_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

AVPUNIT_1_INT_CLEAR

Address: Operational Base + offset (0x5058)

Bit	Attr	Reset Value	Description
31	WO	0x0	vmon_vmeas_clear Write 1 to reset vmon_vmeas_irq
30	WO	0x0	vmon_hmeas_clear Write 1 to reset vmon_hmeas_irq
29	WO	0x0	vstream_fifo_init_clear Write 1 to reset vstream_fifo_init_irq
28:25	RO	0x0	reserved
24	WO	0x0	aud_chstatus_sp3_clear Write 1 to reset aud_chstatus_sp3_irq
23	WO	0x0	aud_chstatus_sp2_clear Write 1 to reset aud_chstatus_sp2_irq
22	WO	0x0	aud_chstatus_sp1_clear Write 1 to reset aud_chstatus_sp1_irq
21	WO	0x0	aud_chstatus_sp0_clear Write 1 to reset aud_chstatus_sp0_irq
20	WO	0x0	aud_mute_clear Write 1 to reset aud_mute_irq
19	WO	0x0	afifo_underflow_clear Write 1 to reset afifo_underflow_irq
18	WO	0x0	afifo_overflow_clear Write 1 to reset afifo_overflow_irq
17	WO	0x0	afifo_thr_mute_low_clear Write 1 to reset afifo_thr_mute_low_irq

Bit	Attr	Reset Value	Description
16	WO	0x0	afifo_thr_mute_high_clear Write 1 to reset afifo_thr_mute_high_irq
15	WO	0x0	afifo_thr_low_clear Write 1 to reset afifo_thr_low_irq
14	WO	0x0	afifo_thr_high_clear Write 1 to reset afifo_thr_high_irq
13	WO	0x0	afifo_thr_pass_clear Write 1 to reset afifo_thr_pass_irq
12	WO	0x0	aud_fmt_chg_clear Write 1 to reset aud_fmt_chg_irq
11	WO	0x0	vproc_syncgen_clear Write 1 to reset vproc_syncgen_irq
10	WO	0x0	vproc_pp_diff_clear Write 1 to reset vproc_pp_diff_irq
9	WO	0x0	vproc_cd_timeout_clear Write 1 to reset vproc_cd_timeout_irq
8	WO	0x0	vproc_cd_chg_clear Write 1 to reset vproc_cd_chg_irq
7	WO	0x0	vstream_fifo_overflow_clear Write 1 to reset vstream_fifo_overflow_irq
6	WO	0x0	vstream_fifo_underflow_clear Write 1 to reset vstream_fifo_underflow_irq
5	WO	0x0	vstream_fifo_almost_full_clear Write 1 to reset vstream_fifo_almost_full_irq
4	WO	0x0	vstream_fifo_almost_empty_clear Write 1 to reset vstream_fifo_almost_empty_irq
3	WO	0x0	deframer_dvihdmi_chg_clear Write 1 to reset deframer_dvihdmi_chg_irq
2	WO	0x0	deframer_gbdet_err_clear Write 1 to reset deframer_gbdet_err_irq
1	WO	0x0	deframer_vsync_thr_reached_clear Write 1 to reset deframer_vsync_thr_reached_irq
0	WO	0x0	deframer_vsync_clear Write 1 to reset deframer_vsync_irq

AVPUNIT_1_INT_FORCE

Address: Operational Base + offset (0x505C)

Bit	Attr	Reset Value	Description
31	WO	0x0	vmon_vmeas_force Write 1 to trigger vmon_vmeas_irq
30	WO	0x0	vmon_hmeas_force Write 1 to trigger vmon_hmeas_irq
29	WO	0x0	vstream_fifo_init_force Write 1 to trigger vstream_fifo_init_irq
28:25	RO	0x0	reserved
24	WO	0x0	aud_chstatus_sp3_force Write 1 to trigger aud_chstatus_sp3_irq
23	WO	0x0	aud_chstatus_sp2_force Write 1 to trigger aud_chstatus_sp2_irq
22	WO	0x0	aud_chstatus_sp1_force Write 1 to trigger aud_chstatus_sp1_irq
21	WO	0x0	aud_chstatus_sp0_force Write 1 to trigger aud_chstatus_sp0_irq

Bit	Attr	Reset Value	Description
20	WO	0x0	aud_mute_force Write 1 to trigger aud_mute_irq
19	WO	0x0	afifo_underflow_force Write 1 to trigger afifo_underflow_irq
18	WO	0x0	afifo_overflow_force Write 1 to trigger afifo_overflow_irq
17	WO	0x0	afifo_thr_mute_low_force Write 1 to trigger afifo_thr_mute_low_irq
16	WO	0x0	afifo_thr_mute_high_force Write 1 to trigger afifo_thr_mute_high_irq
15	WO	0x0	afifo_thr_low_force Write 1 to trigger afifo_thr_low_irq
14	WO	0x0	afifo_thr_high_force Write 1 to trigger afifo_thr_high_irq
13	WO	0x0	afifo_thr_pass_force Write 1 to trigger afifo_thr_pass_irq
12	WO	0x0	aud_fmt_chg_force Write 1 to trigger aud_fmt_chg_irq
11	WO	0x0	vproc_syncgen_force Write 1 to trigger vproc_syncgen_irq
10	WO	0x0	vproc_pp_diff_force Write 1 to trigger vproc_pp_diff_irq
9	WO	0x0	vproc_cd_timeout_force Write 1 to trigger vproc_cd_timeout_irq
8	WO	0x0	vproc_cd_chg_force Write 1 to trigger vproc_cd_chg_irq
7	WO	0x0	vstream_fifo_overflow_force Write 1 to trigger vstream_fifo_overflow_irq
6	WO	0x0	vstream_fifo_underflow_force Write 1 to trigger vstream_fifo_underflow_irq
5	WO	0x0	vstream_fifo_almost_full_force Write 1 to trigger vstream_fifo_almost_full_irq
4	WO	0x0	vstream_fifo_almost_empty_force Write 1 to trigger vstream_fifo_almost_empty_irq
3	WO	0x0	deframer_dvihdmi_chg_force Write 1 to trigger deframer_dvihdmi_chg_irq
2	WO	0x0	deframer_gbdet_err_force Write 1 to trigger deframer_gbdet_err_irq
1	WO	0x0	deframer_vsync_thr_reached_force Write 1 to trigger deframer_vsync_thr_reached_irq
0	WO	0x0	deframer_vsync_force Write 1 to trigger deframer_vsync_irq

PKT_0_INT_STATUS

Address: Operational Base + offset (0x5080)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	pktdec_emd_chg_irq Extended Metadata Packet change interrupt flag status.
20	RO	0x0	reserved
19	RO	0x0	pktdec_clear_avmute_timeout_irq Clear AVMUTE timeout (the time between the AVMUTE rise and the configured time in pktdec_auto_clear_avmute_sel has been reached)

Bit	Attr	Reset Value	Description
18	RO	0x0	pktdec_genpkt1_chg_irq Generic Packet 1 change interrupt flag status.
17	RO	0x0	pktdec_genpkt0_chg_irq Generic Packet 0 change interrupt flag status.
16	RO	0x0	pktdec_drmif_chg_irq Dynamic Range and Mastering InfoFrame Packet change interrupt flag status
15	RO	0x0	pktdec_ntscvbiif_chg_irq NTSC VBI InfoFrame Packet change interrupt flag status
14	RO	0x0	reserved
13	RO	0x0	pktdec_audif_chg_irq Audio InfoFrame Packet change interrupt flag status.
12	RO	0x0	pktdec_srcpdif_chg_irq Source Product Descriptor InfoFrame Packet change interrupt flag status
11	RO	0x0	pktdec_aviif_chg_irq Auxiliary Video Information InfoFrame Packet change interrupt flag status
10	RO	0x0	pktdec_vsif_chg_irq Vendor-Specific InfoFrame Packet change interrupt flag status
9	RO	0x0	pktdec_amd_chg_irq Audio Metadata Packet change interrupt flag status
8	RO	0x0	pktdec_gmd_chg_irq Gamut Metadata Packet change interrupt flag status
7	RO	0x0	pktdec_isrc2_chg_irq ISRC2 Packet change interrupt flag status.
6	RO	0x0	pktdec_isrc1_chg_irq ISRC1 Packet change interrupt flag status.
5	RO	0x0	pktdec_acp_chg_irq Audio Content Protection Packet change interrupt flag status.
4	RO	0x0	pktdec_gcp_chg_irq Generic Content/Content Mute Packet change interrupt flag status
3	RO	0x0	pktdec_acr_chg_irq Audio Clock Regeneration Packet change interrupt flag status
2	RO	0x0	pktdec_acp_timeout_irq Audio Content Protection Packet 600ms timeout interrupt flag status.
1	RO	0x0	pktdec_acr_n_chg_irq Audio Clock Regeneration N change interrupt flag status
0	RO	0x0	pktdec_acr_cts_chg_irq Audio Clock Regeneration CTS change interrupt flag status

PKT_0_INT_MASK_N

Address: Operational Base + offset (0x5084)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	pktdec_emd_chg_mask_n Write 1 to unmask pktdec_emd_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
20	RO	0x0	reserved
19	RW	0x0	pktdec_clear_avmute_timeout_mask_n Write 1 to unmask pktdec_clear_avmute_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
18	RW	0x0	pktdec_genpkt1_chg_mask_n Write 1 to unmask pktdec_genpkt1_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
17	RW	0x0	pktdec_genpkt0_chg_mask_n Write 1 to unmask pktdec_genpkt0_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
16	RW	0x0	pktdec_drmif_chg_mask_n Write 1 to unmask pktdec_drmif_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
15	RW	0x0	pktdec_ntscvbiif_chg_mask_n Write 1 to unmask pktdec_ntscvbiif_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
14	RO	0x0	reserved
13	RW	0x0	pktdec_audif_chg_mask_n Write 1 to unmask pktdec_audif_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
12	RW	0x0	pktdec_srcpdif_chg_mask_n Write 1 to unmask pktdec_srcpdif_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
11	RW	0x0	pktdec_aviif_chg_mask_n Write 1 to unmask pktdec_aviif_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
10	RW	0x0	pktdec_vsif_chg_mask_n Write 1 to unmask pktdec_vsif_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
9	RW	0x0	pktdec_amd_chg_mask_n Write 1 to unmask pktdec_amd_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
8	RW	0x0	pktdec_gmd_chg_mask_n Write 1 to unmask pktdec_gmd_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
7	RW	0x0	pktdec_isrc2_chg_mask_n Write 1 to unmask pktdec_isrc2_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
6	RW	0x0	pktdec_isrc1_chg_mask_n Write 1 to unmask pktdec_isrc1_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
5	RW	0x0	pktdec_acp_chg_mask_n Write 1 to unmask pktdec_acp_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
4	RW	0x0	pktdec_gcp_chg_mask_n Write 1 to unmask pktdec_gcp_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
3	RW	0x0	pktdec_acr_chg_mask_n Write 1 to unmask pktdec_acr_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
2	RW	0x0	pktdec_acp_timeout_mask_n Write 1 to unmask pktdec_acp_timeout_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
1	RW	0x0	pkdec_acr_n_chg_mask_n Write 1 to unmask pktdec_acr_n_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
0	RW	0x0	pktdec_acr_cts_chg_mask_n Write 1 to unmask pktdec_acr_cts_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

PKT_0_INT_CLEAR

Address: Operational Base + offset (0x5088)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	pktdec_emd_chg_clear Write 1 to reset pktdec_emd_chg_irq
20	RO	0x0	reserved
19	WO	0x0	pktdec_clear_avmute_timeout_clear Write 1 to reset pktdec_clear_avmute_timeout_irq
18	WO	0x0	pktdec_genpkt1_chg_clear Write 1 to reset pktdec_genpkt1_chg_irq
17	WO	0x0	pktdec_genpkt0_chg_clear Write 1 to reset pktdec_genpkt0_chg_irq
16	WO	0x0	pktdec_drmif_chg_clear Write 1 to reset pktdec_drmif_chg_irq
15	WO	0x0	pktdec_ntscvbiif_chg_clear Write 1 to reset pktdec_ntscvbiif_chg_irq
14	RO	0x0	reserved
13	WO	0x0	pktdec_audif_chg_clear Write 1 to reset pktdec_audif_chg_irq
12	WO	0x0	pktdec_srcpdif_chg_clear Write 1 to reset pktdec_srcpdif_chg_irq
11	WO	0x0	pktdec_aviif_chg_clear Write 1 to reset pktdec_aviif_chg_irq
10	WO	0x0	pktdec_vsif_chg_clear Write 1 to reset pktdec_vsif_chg_irq
9	WO	0x0	pktdec_amd_chg_clear Write 1 to reset pktdec_amd_chg_irq
8	WO	0x0	pktdec_gmd_chg_clear Write 1 to reset pktdec_gmd_chg_irq
7	WO	0x0	pktdec_isrc2_chg_clear Write 1 to reset pktdec_isrc2_chg_irq
6	WO	0x0	pktdec_isrc1_chg_clear Write 1 to reset pktdec_isrc1_chg_irq
5	WO	0x0	pktdec_acp_chg_clear Write 1 to reset pktdec_acp_chg_irq
4	WO	0x0	pktdec_gcp_chg_clear Write 1 to reset pktdec_gcp_chg_irq
3	WO	0x0	pktdec_acr_chg_clear Write 1 to reset pktdec_acr_chg_irq
2	WO	0x0	pktdec_acp_timeout_clear Write 1 to reset pktdec_acp_timeout_irq
1	WO	0x0	pktdec_acr_n_chg_clear Write 1 to reset pktdec_acr_n_chg_irq
0	WO	0x0	pktdec_acr_cts_chg_clear Write 1 to reset pktdec_acr_cts_chg_irq

PKT_0_INT_FORCE

Address: Operational Base + offset (0x508C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	pktdec_emd_chg_force Write 1 to trigger pktdec_emd_chg_irq
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19	WO	0x0	pktdec_clear_avmute_timeout_force Write 1 to trigger pktdec_clear_avmute_timeout_irq
18	WO	0x0	pktdec_genpkt1_chg_force Write 1 to trigger pktdec_genpkt1_chg_irq
17	WO	0x0	pktdec_genpkt0_chg_force Write 1 to trigger pktdec_genpkt0_chg_irq
16	WO	0x0	pktdec_drmif_chg_force Write 1 to trigger pktdec_drmif_chg_irq
15	WO	0x0	pktdec_ntscvbiif_chg_force Write 1 to trigger pktdec_ntscvbiif_chg_irq
14	RO	0x0	reserved
13	WO	0x0	pktdec_audif_chg_force Write 1 to trigger pktdec_audif_chg_irq
12	WO	0x0	pktdec_srcpdif_chg_force Write 1 to trigger pktdec_srcpdif_chg_irq
11	WO	0x0	pktdec_aviif_chg_force Write 1 to trigger pktdec_aviif_chg_irq
10	WO	0x0	pktdec_vsif_chg_force Write 1 to trigger pktdec_vsif_chg_irq
9	WO	0x0	pktdec_amd_chg_force Write 1 to trigger pktdec_amd_chg_irq
8	WO	0x0	pktdec_gmd_chg_force Write 1 to trigger pktdec_gmd_chg_irq
7	WO	0x0	pktdec_isrc2_chg_force Write 1 to trigger pktdec_isrc2_chg_irq
6	WO	0x0	pktdec_isrc1_chg_force Write 1 to trigger pktdec_isrc1_chg_irq
5	WO	0x0	pktdec_acp_chg_force Write 1 to trigger pktdec_acp_chg_irq
4	WO	0x0	pktdec_gcp_chg_force Write 1 to trigger pktdec_gcp_chg_irq
3	WO	0x0	pktdec_acr_chg_force Write 1 to trigger pktdec_acr_chg_irq
2	WO	0x0	pktdec_acp_timeout_force Write 1 to trigger pktdec_acp_timeout_irq
1	WO	0x0	pktdec_acr_n_chg_force Write 1 to trigger pktdec_acr_n_chg_irq
0	WO	0x0	pktdec_acr_cts_chg_force Write 1 to trigger pktdec_acr_cts_chg_irq

PKT_1_INT_STATUS

Address: Operational Base + offset (0x5090)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x0	pktfifo_new_entry_irq Packet FIFO new entry interrupt flag status.
5	RO	0x0	pktfifo_overflow_irq Packet FIFO overflow interrupt flag status.
4	RO	0x0	pktfifo_underflow_irq Packet FIFO underflow interrupt flag status
3	RO	0x0	reserved
2	RO	0x0	pktfifo_thr_high_irq Packet FIFO high threshold interrupt flag status

Bit	Attr	Reset Value	Description
1	RO	0x0	pktfifo_thr_pass_irq Packet FIFO pass threshold interrupt flag status.
0	RO	0x0	pktfifo_thr_low_irq Packet FIFO low threshold interrupt flag status

PKT_1_INT_MASK_N

Address: Operational Base + offset (0x5094)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	pktfifo_new_entry_mask_n Write 1 to unmask pktfifo_new_entry_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
5	RW	0x0	pktfifo_overflow_mask_n Write 1 to unmask pktfifo_overflow_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
4	RW	0x0	pktfifo_underflow_mask_n Write 1 to unmask pktfifo_underflow_irq. The interrupt line is asserted if the corresponding interrupt is asserted
3	RO	0x0	reserved
2	RW	0x0	pktfifo_thr_high_mask_n Write 1 to unmask pktfifo_thr_high_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
1	RW	0x0	pktfifo_thr_pass_mask_n Write 1 to unmask pktfifo_thr_pass_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
0	RW	0x0	pktfifo_thr_low_mask_n Write 1 to unmask pktfifo_thr_low_irq. The interrupt line is asserted if the corresponding interrupt is asserted

PKT_1_INT_CLEAR

Address: Operational Base + offset (0x5098)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	WO	0x0	pktfifo_new_entry_clear Write 1 to reset pktfifo_new_entry_irq
5	WO	0x0	pktfifo_overflow_clear Write 1 to reset pktfifo_overflow_irq
4	WO	0x0	pktfifo_underflow_clear Write 1 to reset pktfifo_underflow_irq
3	RO	0x0	reserved
2	WO	0x0	pktfifo_thr_high_clear Write 1 to reset pktfifo_thr_high_irq
1	WO	0x0	pktfifo_thr_pass_clear Write 1 to reset pktfifo_thr_pass_irq
0	WO	0x0	pktfifo_thr_low_clear Write 1 to reset pktfifo_thr_low_irq

PKT_1_INT_FORCE

Address: Operational Base + offset (0x509C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	WO	0x0	pktfifo_new_entry_force Write 1 to trigger pktfifo_new_entry_irq

Bit	Attr	Reset Value	Description
5	WO	0x0	pktfifo_overflow_force Write 1 to trigger pktfifo_overflow_irq
4	WO	0x0	pktfifo_underflow_force Write 1 to trigger pktfifo_underflow_irq
3	RO	0x0	reserved
2	WO	0x0	pktfifo_thr_high_force Write 1 to trigger pktfifo_thr_high_irq
1	WO	0x0	pktfifo_thr_pass_force Write 1 to trigger pktfifo_thr_pass_irq
0	WO	0x0	pktfifo_thr_low_force Write 1 to trigger pktfifo_thr_low_irq

PKT_2_INT_STATUS

Address: Operational Base + offset (0x50A0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	pktdec_emd_rcv_irq Extended Metadata Packet received interrupt flag status.
20:19	RO	0x0	reserved
18	RO	0x0	pktdec_genpkt1_rcv_irq Generic Packet 1 received interrupt flag status
17	RO	0x0	pktdec_genpkt0_rcv_irq Generic Packet 0 received interrupt flag status
16	RO	0x0	pktdec_drmif_rcv_irq Dynamic Range and Mastering InfoFrame Packet received interrupt flag status
15	RO	0x0	pktdec_ntscvbiif_rcv_irq NTSC VBI InfoFrame Packet received interrupt flag status
14	RO	0x0	reserved
13	RO	0x0	pktdec_audif_rcv_irq Audio InfoFrame Packet received interrupt flag status.
12	RO	0x0	pktdec_srcpdif_rcv_irq Source Product Descriptor InfoFrame Packet received interrupt flag status
11	RO	0x0	pktdec_aviif_rcv_irq Auxiliary Video Information InfoFrame Packet received interrupt flag status.
10	RO	0x0	pktdec_vsif_rcv_irq Vendor-Specific InfoFrame Packet received interrupt flag status.
9	RO	0x0	pktdec_amd_rcv_irq Audio Metadata Packet received interrupt flag status
8	RO	0x0	pktdec_gmd_rcv_irq Gamut Metadata Packet received interrupt flag status
7	RO	0x0	pktdec_isrc2_rcv_irq ISRC2 Packet received interrupt flag status.
6	RO	0x0	pktdec_isrc1_rcv_irq ISRC1 Packet received interrupt flag status.
5	RO	0x0	pktdec_acp_rcv_irq Audio Content Protection Packet received interrupt flag status.
4	RO	0x0	pktdec_gcp_rcv_irq Generic Content/Content Mute Packet received interrupt flag status.
3	RO	0x0	pktdec_acr_rcv_irq Audio Clock Regeneration Packet received interrupt flag status

Bit	Attr	Reset Value	Description
2:0	RO	0x0	reserved

PKT_2_INT_MASK_N

Address: Operational Base + offset (0x50A4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	pktdec_emd_rcv_mask_n Write 1 to unmask pktdec_emd_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
20:19	RO	0x0	reserved
18	RW	0x0	pktdec_genpkt1_rcv_mask_n Write 1 to unmask pktdec_genpkt1_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
17	RW	0x0	pktdec_genpkt0_rcv_mask_n Write 1 to unmask pktdec_genpkt0_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
16	RW	0x0	pktdec_drmif_rcv_mask_n Write 1 to unmask pktdec_drmif_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted
15	RW	0x0	pktdec_ntscvbiif_rcv_mask_n Write 1 to unmask pktdec_ntscvbiif_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
14	RO	0x0	reserved
13	RW	0x0	pktdec_audif_rcv_mask_n Write 1 to unmask pktdec_audif_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted
12	RW	0x0	pktdec_srcpdif_rcv_mask_n Write 1 to unmask pktdec_srcpdif_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
11	RW	0x0	pktdec_aviif_rcv_mask_n Write 1 to unmask pktdec_aviif_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted
10	RW	0x0	pktdec_vsif_rcv_mask_n Write 1 to unmask pktdec_vsif_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted
9	RW	0x0	pktdec_amd_rcv_mask_n Write 1 to unmask pktdec_amd_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
8	RW	0x0	pktdec_gmd_rcv_mask_n Write 1 to unmask pktdec_gmd_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
7	RW	0x0	pktdec_isrc2_rcv_mask_n Write 1 to unmask pktdec_isrc2_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted
6	RW	0x0	pktdec_isrc1_rcv_mask_n Write 1 to unmask pktdec_isrc1_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
5	RW	0x0	pktdec_acp_rcv_mask_n Write 1 to unmask pktdec_acp_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
4	RW	0x0	pktdec_gcp_rcv_mask_n Write 1 to unmask pktdec_gcp_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted

Bit	Attr	Reset Value	Description
3	RW	0x0	pktdec_acr_rcv_mask_n Write 1 to unmask pktdec_acr_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
2:0	RO	0x0	reserved

PKT_2_INT_CLEAR

Address: Operational Base + offset (0x50A8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	pktdec_emd_rcv_clear Write 1 to reset pktdec_emd_rcv_irq
20:19	RO	0x0	reserved
18	WO	0x0	pktdec_genpkt1_rcv_clear Write 1 to reset pktdec_genpkt1_rcv_irq
17	WO	0x0	pktdec_genpkt0_rcv_clear Write 1 to reset pktdec_genpkt0_rcv_irq
16	WO	0x0	pktdec_drmif_rcv_clear Write 1 to reset pktdec_drmif_rcv_irq
15	WO	0x0	pktdec_ntscvbiif_rcv_clear Write 1 to reset pktdec_ntscvbiif_rcv_irq
14	RO	0x0	reserved
13	WO	0x0	pktdec_audif_rcv_clear Write 1 to reset pktdec_audif_rcv_irq
12	WO	0x0	pktdec_srcpdif_rcv_clear Write 1 to reset pktdec_srcpdif_rcv_irq
11	WO	0x0	pktdec_aviif_rcv_clear Write 1 to reset pktdec_aviif_rcv_irq
10	WO	0x0	pktdec_vsif_rcv_clear Write 1 to reset pktdec_vsif_rcv_irq
9	WO	0x0	pktdec_amd_rcv_clear Write 1 to reset pktdec_amd_rcv_irq
8	WO	0x0	pktdec_gmd_rcv_clear Write 1 to reset pktdec_gmd_rcv_irq
7	WO	0x0	pktdec_isrc2_rcv_clear Write 1 to reset pktdec_isrc2_rcv_irq
6	WO	0x0	pktdec_isrc1_rcv_clear Write 1 to reset pktdec_isrc1_rcv_irq
5	WO	0x0	pktdec_acp_rcv_clear Write 1 to reset pktdec_acp_rcv_irq
4	WO	0x0	pktdec_gcp_rcv_clear Write 1 to reset pktdec_gcp_rcv_irq
3	WO	0x0	pktdec_acr_rcv_clear Write 1 to reset pktdec_acr_rcv_irq
2:0	RO	0x0	reserved

PKT_2_INT_FORCE

Address: Operational Base + offset (0x50AC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	pktdec_emd_rcv_force Write 1 to trigger pktdec_emd_rcv_irq
20:19	RO	0x0	reserved
18	WO	0x0	pktdec_genpkt1_rcv_force Write 1 to trigger pktdec_genpkt1_rcv_irq

Bit	Attr	Reset Value	Description
17	WO	0x0	pktdec_genpkt0_rcv_force Write 1 to trigger pktdec_genpkt0_rcv_irq
16	WO	0x0	pktdec_drmif_rcv_force Write 1 to trigger pktdec_drmif_rcv_irq
15	WO	0x0	pktdec_ntscvbiif_rcv_force Write 1 to trigger pktdec_ntscvbiif_rcv_irq
14	RO	0x0	reserved
13	WO	0x0	pktdec_audif_rcv_force Write 1 to trigger pktdec_audif_rcv_irq
12	WO	0x0	pktdec_srcpdif_rcv_force Write 1 to trigger pktdec_srcpdif_rcv_irq
11	WO	0x0	pktdec_aviif_rcv_force Write 1 to trigger pktdec_aviif_rcv_irq
10	WO	0x0	pktdec_vsif_rcv_force Write 1 to trigger pktdec_vsif_rcv_irq
9	WO	0x0	pktdec_amd_rcv_force Write 1 to trigger pktdec_amd_rcv_irq
8	WO	0x0	pktdec_gmd_rcv_force Write 1 to trigger pktdec_gmd_rcv_irq
7	WO	0x0	pktdec_isrc2_rcv_force Write 1 to trigger pktdec_isrc2_rcv_irq
6	WO	0x0	pktdec_isrc1_rcv_force Write 1 to trigger pktdec_isrc1_rcv_irq
5	WO	0x0	pktdec_acp_rcv_force Write 1 to trigger pktdec_acp_rcv_irq
4	WO	0x0	pktdec_gcp_rcv_force Write 1 to trigger pktdec_gcp_rcv_irq
3	WO	0x0	pktdec_acr_rcv_force Write 1 to trigger pktdec_acr_rcv_irq
2:0	RO	0x0	reserved

SCDC_INT_STATUS

Address: Operational Base + offset (0x50C0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	scdctmdsccfg_chg_irq SCDC TMDS Configuration register change interrupt flag status: 1'b0: Inactive 1'b1: Active
1	RO	0x0	scdcscstatus_chg_irq SCDC Status flag change interrupt status: 1'b0: Inactive 1'b1: Active
0	RO	0x0	scdccfg_chg_irq SCDC Configuration register change interrupt flag status: 1'b0: Inactive 1'b1: Active

SCDC_INT_MASK_N

Address: Operational Base + offset (0x50C4)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	scdctmdsccfg_chg_mask_n Write 1 to unmask scdctmdsccfg_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
1	RW	0x0	scdcscstatus_chg_mask_n Write 1 to unmask scdcscstatus_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted
0	RW	0x0	scdccfg_chg_mask_n Write 1 to unmask scdccfg_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

SCDC_INT_CLEAR

Address: Operational Base + offset (0x50C8)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	scdctmdsccfg_chg_clear Write 1 to reset scdctmdsccfg_chg_irq
1	WO	0x0	scdcscstatus_chg_clear Write 1 to reset scdcscstatus_chg_irq
0	WO	0x0	scdccfg_chg_clear Write 1 to reset scdccfg_chg_irq

SCDC_INT_FORCE

Address: Operational Base + offset (0x50CC)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	scdctmdsccfg_chg_force Write 1 to trigger scdctmdsccfg_chg_irq
1	WO	0x0	scdcscstatus_chg_force Write 1 to trigger scdcscstatus_chg_irq
0	WO	0x0	scdccfg_chg_force Write 1 to trigger scdccfg_chg_irq

HDCP_INT_STATUS

Address: Operational Base + offset (0x50D0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	hdcp2_decrypted_chg_irq HDCP 2 decrypted interrupt flag status
20	RO	0x0	hdcp2_authentication_fail_irq HDCP 2 authentication fail interrupt flag status
19	RO	0x0	hdcp2_authenticated_irq HDCP 2 authenticated interrupt flag status
18	RO	0x0	hdcp2_authentication_lost_irq HDCP 2 authentication lost interrupt flag status
17	RO	0x0	hdcp2_not_capable_irq HDCP 2 not capable interrupt flag status
16	RO	0x0	hdcp2_capable_irq HDCP 2 capable interrupt flag status
15:11	RO	0x00	reserved
10	RO	0x0	hdcp_dkset_done_irq HDCP1.4 Device Key Set read operation done interrupt status
9	RO	0x0	hdcp14_oess_eess_chg_irq HDCP1.4 OESS and EESS change interrupt status

Bit	Attr	Reset Value	Description
8	RO	0x0	hdcp14_encdis_irq HDCP1.4 Encryption Disable interrupt status
7	RO	0x0	hdcp14_encen_irq HDCP1.4 Encryption Enable interrupt status
6	RO	0x0	hdcp14_auth_irq HDCP1.4 Authenticated interrupt status
5	RO	0x0	hdcp14_bstatus_read_irq HDCP1.4 BSTATUS read request received interrupt status
4	RO	0x0	hdcp14_bcaps_read_irq HDCP1.4 BCAPS read request received interrupt status
3	RO	0x0	reserved
2	RO	0x0	hdcp14_ri_read_irq HDCP1.4 Ri read request received interrupt status
1	RO	0x0	hdcp14_bksv_read_irq HDCP1.4 BKSV read request received interrupt status
0	RO	0x0	hdpc14_aksv_rcv_irq HDCP1.4 AKSV received interrupt status

HDCP_INT_MASK_N

Address: Operational Base + offset (0x50D4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	hdcp2_decrypted_chg_mask_n Write 1 to unmask hdcp2_decrypted_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
20	RW	0x0	hdcp2_authentication_fail_mask_n Write 1 to unmask hdcp2_authentication_fail_irq. The interrupt line is asserted if the corresponding interrupt is asserted
19	RW	0x0	hdcp2_authenticated_mask_n Write 1 to unmask hdcp2_authenticated_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
18	RW	0x0	hdcp2_authentication_lost_mask_n Write 1 to unmask hdcp2_authentication_lost_irq. The interrupt line is asserted if the corresponding interrupt is asserted
17	RW	0x0	hdcp2_not_capable_mask_n Write 1 to unmask hdcp2_not_capable_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
16	RW	0x0	hdcp2_capable_mask_n Write 1 to unmask hdcp2_capable_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
15:11	RO	0x00	reserved
10	RW	0x0	hdcp_dkset_done_mask_n Write 1 to unmask hdcp_dkset_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
9	RW	0x0	hdcp14_oess_eess_chg_mask_n Write 1 to unmask hdcp14_oess_eess_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
8	RW	0x0	hdcp14_encdis_mask_n Write 1 to unmask hdcp14_encdis_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
7	RW	0x0	hdcp14_encen_mask_n Write 1 to unmask hdcp14_encen_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
6	RW	0x0	hdcp14_auth_mask_n Write 1 to unmask hdcp14_auth_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
5	RW	0x0	hdcp14_bstatus_read_mask_n Write 1 to unmask hdcp14_bstatus_read_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
4	RW	0x0	hdcp14_bcaps_read_mask_n Write 1 to unmask hdcp14_bcaps_read_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
3	RO	0x0	reserved
2	RW	0x0	hdcp14_ri_read_mask_n Write 1 to unmask hdcp14_ri_read_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
1	RW	0x0	hdcp14_bksv_read_mask_n Write 1 to unmask hdcp14_bksv_read_irq. The interrupt line is asserted if the corresponding interrupt is asserted
0	RW	0x0	hdcp14_aksv_rcv_mask_n Write 1 to unmask hdcp14_aksv_rcv_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

HDCP_INT_CLEAR

Address: Operational Base + offset (0x50D8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	hdcp2_decrypted_chg_clear Write 1 to reset hdcp2_decrypted_chg_irq
20	WO	0x0	hdcp2_authentication_fail_clear Write 1 to reset hdcp2_authentication_fail_irq
19	WO	0x0	hdcp2_authenticated_clear Write 1 to reset hdcp2_authenticated_irq
18	WO	0x0	hdcp2_authentication_lost_clear Write 1 to reset hdcp2_authentication_lost_irq
17	WO	0x0	hdcp2_not_capable_clear Write 1 to reset hdcp2_not_capable_irq
16	WO	0x0	hdcp2_capable_clear Write 1 to reset hdcp2_capable_irq
15:11	RO	0x00	reserved
10	WO	0x0	hdcp_dkset_done_clear Write 1 to reset hdcp_dkset_done_irq
9	WO	0x0	hdcp14_oess_eess_chg_clear Write 1 to reset hdcp14_oess_eess_chg_irq
8	WO	0x0	hdcp14_encdis_clear Write 1 to reset hdcp14_encdis_irq
7	WO	0x0	hdcp14_encen_clear Write 1 to reset hdcp14_encen_irq
6	WO	0x0	hdcp14_auth_clear Write 1 to reset hdcp14_auth_irq
5	WO	0x0	hdcp14_bstatus_read_clear Write 1 to reset hdcp14_bstatus_read_irq
4	WO	0x0	hdcp14_bcaps_read_clear Write 1 to reset hdcp14_bcaps_read_irq
3	RO	0x0	reserved
2	WO	0x0	hdcp14_ri_read_clear Write 1 to reset hdcp14_ri_read_irq

Bit	Attr	Reset Value	Description
1	WO	0x0	hdcp14_bksv_read_clear Write 1 to reset hdcp14_bksv_read_irq
0	WO	0x0	hdcp14_aksv_rcv_clear Write 1 to reset hdcp14_aksv_rcv_irq

HDCP_INT_FORCE

Address: Operational Base + offset (0x50DC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	WO	0x0	hdcp2_decrypted_chg_force Write 1 to trigger hdcp2_decrypted_chg_irq
20	WO	0x0	hdcp2_authentication_fail_force Write 1 to trigger hdcp2_authentication_fail_irq
19	WO	0x0	hdcp2_authenticated_force Write 1 to trigger hdcp2_authenticated_irq
18	WO	0x0	hdcp2_authentication_lost_force Write 1 to trigger hdcp2_authentication_lost_irq
17	WO	0x0	hdcp2_not_capable_force Write 1 to trigger hdcp2_not_capable_irq
16	WO	0x0	hdcp2_capable_force Write 1 to trigger hdcp2_capable_irq
15:11	RO	0x00	reserved
10	WO	0x0	hdcp_dkset_done_force Write 1 to trigger hdcp_dkset_done_irq
9	WO	0x0	hdcp14_oess_eess_chg_force Write 1 to trigger hdcp14_oess_eess_chg_irq
8	WO	0x0	hdcp14_encdis_force Write 1 to trigger hdcp14_encdis_irq
7	WO	0x0	hdcp14_encen_force Write 1 to trigger hdcp14_encen_irq
6	WO	0x0	hdcp14_auth_force Write 1 to trigger hdcp14_auth_irq
5	WO	0x0	hdcp14_bstatus_read_force Write 1 to trigger hdcp14_bstatus_read_irq
4	WO	0x0	hdcp14_bcaps_read_force Write 1 to trigger hdcp14_bcaps_read_irq
3	RO	0x0	reserved
2	WO	0x0	hdcp14_ri_read_force Write 1 to trigger hdcp14_ri_read_irq
1	WO	0x0	hdcp14_bksv_read_force Write 1 to trigger hdcp14_bksv_read_irq
0	WO	0x0	hdcp14_aksv_rcv_force Write 1 to trigger hdcp14_aksv_rcv_irq

HDCP_1_INT_STATUS

Address: Operational Base + offset (0x50E0)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RO	0x0	hdcp2_esm_p0_gpio_out_15_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[15] - interrupt flag status

Bit	Attr	Reset Value	Description
9	RO	0x0	hdcp2_esm_p0_gpio_out_14_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[14] - interrupt flag status
8	RO	0x0	hdcp2_esm_p0_gpio_out_13_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[13] - interrupt flag status
7	RO	0x0	hdcp2_esm_p0_gpio_out_12_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[12] - interrupt flag status
6	RO	0x0	hdcp2_esm_p0_gpio_out_11_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[11] - interrupt flag status
5	RO	0x0	hdcp2_esm_p0_gpio_out_10_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[10] - interrupt flag status
4	RO	0x0	hdcp2_esm_p0_gpio_out_9_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[9] - interrupt flag status
3	RO	0x0	hdcp2_esm_p0_gpio_out_8_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[8] - interrupt flag status
2	RO	0x0	hdcp2_esm_p0_gpio_out_7_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[7] - interrupt flag status
1	RO	0x0	hdcp2_esm_p0_gpio_out_6_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[6] - interrupt flag status
0	RO	0x0	hdcp2_esm_p0_gpio_out_5_chg_irq Port 0 General-Purpose outputs from the HDCP2 ESM block Change interrupt for bit hdcp2_esm_p0_gpio_out[5] - interrupt flag status

HDCP_1_INT_MASK_N

Address: Operational Base + offset (0x50E4)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	hdcp2_esm_p0_gpio_out_15_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_15_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
9	RW	0x0	hdcp2_esm_p0_gpio_out_14_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_14_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
8	RW	0x0	hdcp2_esm_p0_gpio_out_13_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_13_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
7	RW	0x0	hdcp2_esm_p0_gpio_out_12_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_12_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
6	RW	0x0	hdcp2_esm_p0_gpio_out_11_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_11_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
5	RW	0x0	hdcp2_esm_p0_gpio_out_10_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_10_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
4	RW	0x0	hdcp2_esm_p0_gpio_out_9_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_9_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
3	RW	0x0	hdcp2_esm_p0_gpio_out_8_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_8_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
2	RW	0x0	hdcp2_esm_p0_gpio_out_7_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_7_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
1	RW	0x0	hdcp2_esm_p0_gpio_out_6_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_6_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
0	RW	0x0	hdcp2_esm_p0_gpio_out_5_chg_mask_n Write 1 to unmask hdcp2_esm_p0_gpio_out_5_chg_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

HDCP_1_INT_CLEAR

Address: Operational Base + offset (0x50E8)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	WO	0x0	hdcp2_esm_p0_gpio_out_15_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_15_chg_irq
9	WO	0x0	hdcp2_esm_p0_gpio_out_14_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_14_chg_irq
8	WO	0x0	hdcp2_esm_p0_gpio_out_13_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_13_chg_irq
7	WO	0x0	hdcp2_esm_p0_gpio_out_12_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_12_chg_irq
6	WO	0x0	hdcp2_esm_p0_gpio_out_11_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_11_chg_irq
5	WO	0x0	hdcp2_esm_p0_gpio_out_10_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_10_chg_irq
4	WO	0x0	hdcp2_esm_p0_gpio_out_9_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_9_chg_irq

Bit	Attr	Reset Value	Description
3	WO	0x0	hdcp2_esm_p0_gpio_out_8_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_8_chg_irq
2	WO	0x0	hdcp2_esm_p0_gpio_out_7_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_7_chg_irq
1	WO	0x0	hdcp2_esm_p0_gpio_out_6_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_6_chg_irq
0	WO	0x0	hdcp2_esm_p0_gpio_out_5_chg_clear Write 1 to reset hdcp2_esm_p0_gpio_out_5_chg_irq

HDCP_1_INT_FORCE

Address: Operational Base + offset (0x50EC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	WO	0x0	hdcp2_esm_p0_gpio_out_15_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_15_chg_irq
9	WO	0x0	hdcp2_esm_p0_gpio_out_14_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_14_chg_irq
8	WO	0x0	hdcp2_esm_p0_gpio_out_13_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_13_chg_irq
7	WO	0x0	hdcp2_esm_p0_gpio_out_12_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_12_chg_irq
6	WO	0x0	hdcp2_esm_p0_gpio_out_11_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_11_chg_irq
5	WO	0x0	hdcp2_esm_p0_gpio_out_10_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_10_chg_irq
4	WO	0x0	hdcp2_esm_p0_gpio_out_9_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_9_chg_irq
3	WO	0x0	hdcp2_esm_p0_gpio_out_8_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_8_chg_irq
2	WO	0x0	hdcp2_esm_p0_gpio_out_7_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_7_chg_irq
1	WO	0x0	hdcp2_esm_p0_gpio_out_6_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_6_chg_irq
0	WO	0x0	hdcp2_esm_p0_gpio_out_5_chg_force Write 1 to trigger hdcp2_esm_p0_gpio_out_5_chg_irq

CEC_INT_STATUS

Address: Operational Base + offset (0x5100)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	cecrx_notify_err_irq Follower - Bit timing error detected, Error Notification is being sent to Initiator, while rxbusy is set (for follower). Interrupt flag status: 1'b0: Inactive 1'b1: Active
11	RO	0x0	cecrx_eom_irq Follower - Frame fully received after last data block with EOM=1 (for follower only). Interrupt flag status: 1'b0: Inactive 1'b1: Active

Bit	Attr	Reset Value	Description
10	RO	0x0	cectx_drive_err_irq Drive 0 in the CEC output has not been seen in the CEC input interrupt flag status: 1'b0: Inactive 1'b1: Active
9	RO	0x0	cecrx_busy_irq Status bit cecrx_busy_st has changed value. Interrupt flag status: 1'b0: Inactive 1'b1: Active
8	RO	0x0	cectx_busy_irq Status bit cectx_busy_st has changed value. Interrupt flag status: 1'b0: Inactive 1'b1: Active
7:6	RO	0x0	reserved
5	RO	0x0	cectx_frame_discarded_irq Message to be sent has been discarded, since a new message has been received before the message is sent. Interrupt flag status: 1'b0: Inactive 1'b1: Active
4	RO	0x0	cectx_nretransmit_fail_irq Last re- transmission fail. Interrupt flag status: 1'b0: Inactive 1'b1: Active
3	RO	0x0	cectx_line_err_irq Initiator - Line Error detected while transmitting a Frame (for initiator only). Interrupt flag status: 1'b0: Inactive 1'b1: Active
2	RO	0x0	cectx_arblost_irq Initiator - CEC line arbitration lost to a different Initiator when starting to transmit a Frame. (specification CEC 9). Interrupt flag status: 1'b0: Inactive 1'b1: Active
1	RO	0x0	cectx_nack_irq Initiator - Frame transmission stopped due to received NACK (direct address) or Negative ACK (broadcast) (for initiator only). Interrupt flag status: 1'b0: Inactive 1'b1: Active
0	RO	0x0	cectx_done_irq Initiator - Frame transmission is done successfully. (initiator only). Interrupt flag status: 1'b0: Inactive 1'b1: Active

CEC_INT_MASK_N

Address: Operational Base + offset (0x5104)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	cecrx_notify_err_mask_n Write 1 to unmask cecrx_notify_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

Bit	Attr	Reset Value	Description
11	RW	0x0	cecrx_eom_mask_n Write 1 to unmask cecrx_eom_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
10	RW	0x0	cectx_drive_err_mask_n Write 1 to unmask cectx_drive_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
9	RW	0x0	cecrx_busy_mask_n Write 1 to unmask cecrx_busy_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
8	RW	0x0	cectx_busy_mask_n Write 1 to unmask cectx_busy_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
7:6	RO	0x0	reserved
5	RW	0x0	cectx_frame_discarded_mask_n Write 1 to unmask cectx_frame_discarded_irq. The interrupt line is asserted if the corresponding interrupt is asserted
4	RW	0x0	cectx_nretransmit_fail_mask_n Write 1 to unmask cectx_nretransmit_fail_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
3	RW	0x0	cectx_line_err_mask_n Write 1 to unmask cectx_line_err_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
2	RW	0x0	cectx_arblost_mask_n Write 1 to unmask cectx_arblost_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
1	RW	0x0	cectx_nack_mask_n Write 1 to unmask cectx_nack_irq. The interrupt line is asserted if the corresponding interrupt is asserted.
0	RW	0x0	cectx_done_mask_n Write 1 to unmask cectx_done_irq. The interrupt line is asserted if the corresponding interrupt is asserted.

CEC_INT_CLEAR

Address: Operational Base + offset (0x5108)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	WO	0x0	cecrx_notify_err_clear Write 1 to reset cecrx_notify_err_irq
11	WO	0x0	cecrx_eom_clear Write 1 to reset cecrx_eom_irq
10	WO	0x0	cectx_drive_err_clear Write 1 to reset cectx_drive_err_irq
9	WO	0x0	cecrx_busy_clear Write 1 to reset cecrx_busy_irq
8	WO	0x0	cectx_busy_clear Write 1 to reset cectx_busy_irq
7:6	RO	0x0	reserved
5	WO	0x0	cectx_frame_discarded_clear Write 1 to reset cectx_frame_discarded_irq
4	WO	0x0	cectx_nretransmit_fail_clear Write 1 to reset cectx_nretransmit_fail_irq
3	WO	0x0	cectx_line_err_clear Write 1 to reset cectx_line_err_irq
2	WO	0x0	cectx_arblost_clear Write 1 to reset cectx_arblost_irq

Bit	Attr	Reset Value	Description
1	WO	0x0	cectx_nack_clear Write 1 to reset cectx_nack_irq
0	WO	0x0	cectx_done_clear Write 1 to reset cectx_done_irq

CEC_INT_FORCE

Address: Operational Base + offset (0x510C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	WO	0x0	cecrx_notify_err_force Write 1 to trigger cecrx_notify_err_irq
11	WO	0x0	cecrx_eom_force Write 1 to trigger cecrx_eom_irq
10	WO	0x0	cectx_drive_err_force Write 1 to trigger cectx_drive_err_irq
9	WO	0x0	cecrx_busy_force Write 1 to trigger cecrx_busy_irq
8	WO	0x0	cectx_busy_force Write 1 to trigger cectx_busy_irq
7:6	RO	0x0	reserved
5	WO	0x0	cectx_frame_discarded_force Write 1 to trigger cectx_frame_discarded_irq
4	WO	0x0	cectx_nretransmit_fail_force Write 1 to trigger cectx_nretransmit_fail_irq
3	WO	0x0	cectx_line_err_force Write 1 to trigger cectx_line_err_irq
2	WO	0x0	cectx_arblost_force Write 1 to trigger cectx_arblost_irq
1	WO	0x0	cectx_nack_force Write 1 to trigger cectx_nack_irq
0	WO	0x0	cectx_done_force Write 1 to trigger cectx_done_irq

25.5 Interface Description

Table 25-3 HDMIRX_WRAPPER Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
IO_HDMIRXPHY_RX0_M	I/O	HDMI_RX_D0N	NA
IO_HDMIRXPHY_RX0_P	I/O	HDMI_RX_D0P	NA
IO_HDMIRXPHY_RX1_M	I/O	HDMI_RX_D1N	NA
IO_HDMIRXPHY_RX1_P	I/O	HDMI_RX_D1P	NA
IO_HDMIRXPHY_RX2_M	I/O	HDMI_RX_D2N	NA
IO_HDMIRXPHY_RX2_P	I/O	HDMI_RX_D2P	NA
IO_HDMIRXPHY_RX3_M	I/O	HDMI_RX_CLKN	NA
IO_HDMIRXPHY_RX3_P	I/O	HDMI_RX_CLKP	NA

Module Pin	Direction	Pad Name	IOMUX Setting
IO_HDMIRXPHY_RESREF	I/O	HDMI_RX_REXT	NA
ocfg_hpd	I/O	MIPI_CAMERA1_CLK_M0/SPDIF0_TX_M0/PCIE30X2_WAKEN_M3/HDMI_RX_HPDIN_M2/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6_u	BUS_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'h5
		HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDIN_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d	BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h5
		BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDIN_M0/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d	BUS_IOC_GPIO4B_IOMUX_SEL_H[11:8] = 4'h5
icec_datain/ ocec_dataout	I/O	MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u	BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12]= 4'h5
		CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d	BUS_IOC_GPIO3D_IOMUX_SEL_L[7:4]= 4'h5
		BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d	BUS_IOC_GPIO4B_IOMUX_SEL_H[7:4]= 4'h5
iddc_sda/ oddc_sda	I/O	MIPI_CAMERA4_CLK_M0/PCIE30X2_CLKREQN_M3/HDMI_RX_SDA_M2/I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7_u	BUS_IOC_GPIO1D_IOMUX_SEL_H[15:12]= 4'h5
		CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d	BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12]= 4'h5
		I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[7:4]=4'hb && PMU2_IOC_GPIO0D_IOMUX_SEL_L[7:4] = 4'h8
iddc_scl	I/O	MIPI_CAMERA3_CLK_M0/HDMI_RX_SCL_M2/I2C8_SCL_M2/UART1_RTSN_M1/PWM14_M2/GPIO1_D6_u	BUS_IOC_GPIO1D_IOMUX_SEL_H[11:8]= 4'h5
		CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d	BUS_IOC_GPIO3D_IOMUX_SEL_L[11:8]= 4'h5
		I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[11:8]=4'hb && PMU2_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 4'h8

Notes: I=input, O=output, I/O=input/output, bidirectional

25.6 Application Notes

25.6.1 HDMIRX Application

The figure below shows the recommended programming sequence to build an HDMIRX system.

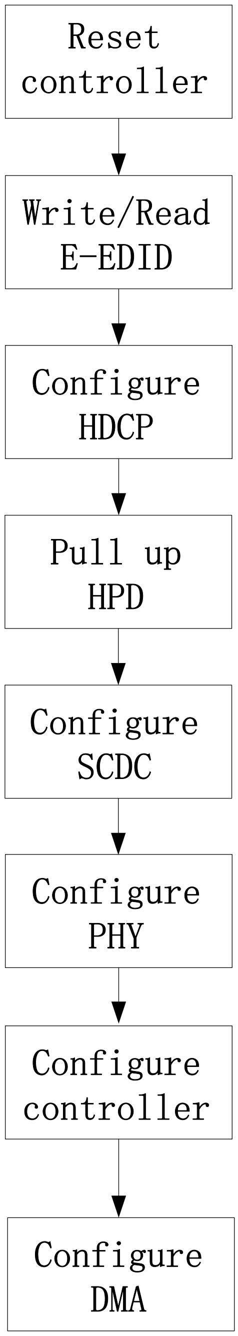

Fig. 25-20 HDMIRX configuration flow

25.6.1.1 Reset controller

HDMIRX controller main reset signal imain_rst_n is from CRU module, the CRU register base address is 0XFD7C0000. The register 0xaf4 below is the CRU register.

Table 25-4 Reset controller operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0xaf4[11]	resetn_hdmirx_ref_req	0x0	0x1	Configure HDMIRX controller main reset signal imain_rst_n to reset the whole HDMIRX controller
Wait for 100us at least				
0xaf4[11]	resetn_hdmirx_ref_req	0x0	0x0	Release the HDMIRX controller main reset signal

SFR Address	SFR Name	Default Value	Setting Value	Description
0x24[31:0]	global_swenable	0x0021 3f01	0x0	Configure all the sub-block enable 1'b0
0x24[31:0]	global_swenable	0x0021 3f01	0x0021 3f01	Configure all the sub-block enable 1'b1. [0]bit: main_enable [8]bit: avpunit_enable [9]bit: audio_enable [10]bit: hdcp_enable [11]bit: pktfifo_enable [12]bit: datapath_enable [13]bit: tmds_enable [16]bit: cec_enable [21]bit: phyctrl_enable

25.6.1.2 Write/Read E-EDID

Table 25-5 E-EDID operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x4428[6:0]	edid_slave_ addr	0x0	0x50	Configure EDID slave address, the common value is 0x50
0x4428[7]	edid_write_en	0x0	0x1	Configure EDID write enable
0x4424[7:0]	edid_wdata	0x0		Configure the first EDID write data
0x4424[7:0]	edid_wdata	0x0		Configure the second EDID write data
...(continue configure 0x4424)				
0x4424[7:0]	edid_wdata	0x0		Configure the 512th EDID write data
The driver will configure 512 EDID write data, and next can read the EDID data through APB bus for debug purpose				
0x4428[7]	edid_write_en	0x0	0x0	Disable EDID write enable
0x4428[8]	edid_read_en	0x0	0x1	Configure EDID read enable
0x4464[7:0]	edid_rdata	0x0		Read the first EDID data
0x4464[7:0]	edid_rdata	0x0		Read the second EDID data
...(continue read 0x4464)				
0x4464[7:0]	edid_rdata	0x0		Read the 512th EDID data
0xfd5a8008[2]	grf_con_hdmirx_sdain_msk	0x0	0x1	Unmask hdmirx ddc sda channel,if not, hdmirx ddc sda will always be 1
0xfd5a8008[1]	grf_con_hdmirx_sclin_msk	0x0	0x1	Unmask hdmirx ddc scl channel,if not, hdmirx ddc scl will always be 1

The user can read the EDID through APB bus just for debug purpose, and HDMITX will read the EDID through DDC bus.

25.6.1.3 Configure HDCP

1. configure HDCP1.4
(1)configure HDCP1.4 key

The driver configures the HDCP1.4 key through HDMIRX APB secure bus firstly, which is different from HDMIRX APB bus. The HDMIRX apb_secure bus has the base address 0XFDF10000(hdmirx_s_addr_offset).

Table 25-6 HDCP1.4 key configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x24[10]	hdcp enable	0x0	0x0	Disable hdmirx hdcp1.4
0xFD586054[14]	sgrf_con_hdmirx_apbs_sel	0x0	0x0	Mux hdcp1.4 sram write enable for secure apb bus
0xFDF10000+0*4	hdmirx_hdcp14_key0[7:0]	0x0		Configure HDCP1.4 key0
0xFDF10000+1*4	hdmirx_hdcp14_key1[7:0]	0x0		Configure HDCP1.4 key1
...(continue configure HDCP1.4 key through address 0xFDF10000+i*4)				
0xFDF10000+288*4	hdmirx_hdcp14_key288[7:0]	0x0		Configure HDCP1.4 key288
0XFD586054[14]	sgrf_con_hdmirx_apbs_sel	0x0	0x1	Enable hdmirx hdcp1.4
0x24[10]	hdcp_enable	0x0	0x1	Mux hdcp1.4 sram read enable for hdmirx internal interface

The driver can read the HDCP1.4 key use the same address as write address. HDCP1.4 key SRAM is 289 byte size, so the offset address must multiply 4.

(2)configure decrypt_seed_en and decrypt_seed

Table 25-7 HDCP1.4 configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x2f0[2:1]	[1]: hdcp_ovr_en [2]: hdcp_ovr_value	0x0	0x1	hdcp_ovr_value is 1'b0 means HDCP1.4
0x24[10]	hdcp_enable	0x0	0x1	Configure HDCP enable
0x290[0]	key_decrypt_en_qst	0x0	0x1	Configure key_decrypt_seed_en for decrypt seed
0x290[5:4]	eess_oess_sel_qst	0x0	0x2	EESS/OESS selection
0x290[11:8]	oess_ctl3_thr_qst	0x7	0x7	OESS number of CTL3=1 threshold to consider ENC_EN on OESS, it may be changed.
0x290[19:16]	eess_ctl_thr_qst	0xe	0xe	EESS number of CTL=1001 threshold to consider ENC_EN on EESS, it may be changed.
0x290[25]	fasti2c_qst	0x0	0x0	If fasti2c_qst is configured 1'b1, it means that the DDC bus support 400KHz transfers. If fasti2c_qst configure 1'b0, it means that the DDC bus just support 100KHz transfers.

SFR Address	SFR Name	Default Value	Setting Value	Description
0x290[26]	features_1dot1_qst	0x0	0x0	HDCP1.4 1.1 Features capability. It is disable.
0x290[27]	fastreauth_qst	0x0	0x0	Bcaps Fast Re-authentication value. It is disable.
0x290[28]	repeater_qst	0x0	0x0	HDCP Repeater capability value. It is disable.

When configure key_decrypt_seed, HDMIRX will read HDCP1.4 key SRAM and decrypt the HDCP1.4 encrypted key with the seed.
(3)configure HDCP2

Table 25-8 HDCP2 configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x2f0[2:1]	[1]: hdcp_ovr_en [2]: hdcp_ovr_value	0x0	0x3	hdcp_ovr_value is 1’b1 means HDCP2

It is simple for HDMIRX controller configuration when in HDCP2 operation.

25.6.1.4 Pull up HPD

Table 25-9 HPD operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x50[0]	hpd	0x0	0x1	Pull up the HPD signal for HDMITX reading EDID and sending video

25.6.1.5 Configure SCDC

Table 25-10 Configure SCDC operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x580[0]	powerprovided	0x0	0x1	+5V power provided for SCDC operation
0x5c0[7:0]	scdc_sinkversion_qst	0x0	0x1	Configure SCDC sink version
0x164[7:0]	i2c_sda_in_hold_value_qst	0x0	0x15	Configure I2C SDA_IN hold time value(expressed in number of irefclk cycle)
0x164[15:8]	i2c_sda_out_hold_value_qst	0x0	0x80	Configure I2C SDA_OUT hold time value(expressed in number of irefclk cycle)

25.6.1.6 Configure PHY

HDMIRX controller has one cr_para interface to configure HDMIRX phy, and driver can configure the HDMIRX controller register to configure HDMIRX phy.

Table 25-11 HDMIRX phy configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0xc0[0]	phy_reset	0x1	0x1	Reset HDMIRX phy
Wait for 100us				
0xc0[0]	phy_reset	0x1	0x0	Release HDMIRX phy reset
0xe0[1:0]	phycreg_cr_para_selection_mode	0x0	0x3	This signal control the selection between the PHY JTAG and cr_para interface. The driver select the cr_para interface here.
Read the [10]bit of SYS_GRF_SOC_STATUS1(0x384, The GRF base address is 0XFD58C000), until this bit is 1'b1. This signal sram_init_done indicates the HDMIRX phy SRAM initial done.				
Write the [1]bit of SYS_GRF_SOC_CON1(0x304), configure 1'b1. This signal is HDMIRX phy sram_ext_ld_done signal, it is the handshake signal with sram_init_done signal				
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x20c7	Configure the first write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x0	Configure the first write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the first wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the second write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the second write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the second wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the third write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x3	Configure the third write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)

SFR Address	SFR Name	Default Value	Setting Value	Description
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the third wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 4th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the 4th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 4th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 5th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the 5th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 5th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 6th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x3	Configure the 6th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 6th wdata finish

SFR Address	SFR Name	Default Value	Setting Value	Description
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 7th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the 7th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 7th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 8th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x0	Configure the 8th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 8th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 9th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x1	Configure the 9th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 9th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 10th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x0	Configure the 10th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)

SFR Address	SFR Name	Default Value	Setting Value	Description
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 10th wdata finish
0xc0[1]	phy_pddq	0x1	0x0	Configure phy pddq 1'b0, and HDMIRX phy begins to enable its reference voltage generator and performs termination calibration.
Read 0xc8[0] bit, it is pddq_ack, read this register bit, wait and until it is 1'b0. It indicates pddq finish.				
0xc0[8]	phy_hdmi_disable	0x1	0x0	Configure phy hdmi_disable 1'b0, and HDMIRX phy begins to enter initialization sequence, and phy begins to power up circuit calibrations.
Read 0xc8[1] bit, it is hdmi_disable_ack, read this register bit, wait and until it is 1'b0. It indicates power up finish.				
0xc0[11:9]	reffreq_sel	0x0	0x0	Select HDMIRX phy cr_para_clk frequency. Default value is 24M. 3'b000: 24M 3'b001: 25M 3'b010: 27M 3'b011: 48M 3'b100: 50M 3'b101: 54M 3'b110: 100M
0xc0[15]	rxdata_width	0x0	0x1	Configure the rxdata width. 1'b0 is 20bit valid, 1'b1 is 40bit valid. And this version is quad pixel, so it is 40bit valid.
Read 0x58c[1] bit, it is scdc_tmdsbitclkratio, before the HDMITX sends >= 3.4Gbps channel video, and it will be configured 1'b1 by the DDC bus.				
0xc0[16]	tmds_clk_ratio	0x0	0x0	If the HDMIRX phy channel bit rate is >= 3.4Gbps, for example 4k resolution, tmds_clk_ration must be configured 1'b1.

25.6.1.7 Configure controller

After HDMIRX phy power up, and has recovered the clock, and next the driver should

configure the video process, audio process, and CEC process.
(1)video process

Table 25-12 video process configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x5018[31:0]	mainunit_0_int_clear	0x0	0xffffffff	Clear all the mainunit0 interrupt
0x5014[31:0]	mainunit_0_int_mask_n	0x0	0xffffffff	Enable all the mainunit0 interrupt
0x28[31:0]	global_timer_ref_base	0x198b7b25	0x198b7b25	It is irefclk frequency value. The default value is 428571429Hz(428.57MHz), there is another frequency 396MHz. The irefclk will count for 1ms/10ms/100s/1s, and will generate the corresponding pulse for many logic.
Wait for timer_base_locked_irq, which is the [26]bit of mainunit_0_int, and clear this interrupt status.				
0x60[14:0]	audclk_stable_freq_margin	0x1	0x1	Configure the audio clock allowed frequency variation(in kHz) for clock lock (audclk_locked_st), this field can’t exceed 7% of the nominal clock frequency.
0x60[30:16]	tmdsqpclk_stable_freq_margin	0x1	0x2	Configure the tmdsqpclk clock allowed frequency variation(in kHz) for clock lock(tmdsqpclk_locked_st), this field can’t exceed 7% of the nominal clock frequency.
0x5018[31:0]	mainunit_0_int_clear	0x0	0xffffffff	Clear all the mainunit0 interrupt
0x5014[31:0]	mainunit_0_int_mask_n	0x0	0xffffffff	Enable all the mainunit0 interrupt
0x5028[31:0]	mainunit_1_int_clear	0x0	0xffffffff	Clear all the mainunit1 interrupt
0x5024[31:0]	mainunit_1_int_mask_n	0x0	0xffffffff	Enable all the mainunit1 interrupt
0x5038[31:0]	mainunit_2_int_clear	0x0	0xffffffff	Clear all the mainunit2 interrupt
0x5034[31:0]	mainunit_2_int_mask_n	0x0	0xffffffff	Enable all the mainunit2 interrupt
0x5048[31:0]	avpunit_0_int_clear	0x0	0xffffffff	Clear all the avpunit0 interrupt

SFR Address	SFR Name	Default Value	Setting Value	Description
0x5044[31:0]	avpunit_0_int_mask_n	0x0	0xffffffff	Enable all the avpunit0 interrupt
0x5058[31:0]	avpunit_1_int_clear	0x0	0xffffffff	Clear all the avpunit1 interrupt
0x5054[31:0]	avpunit_1_int_mask_n	0x0	0xffffffff	Enable all the avpunit1 interrupt
0x5088[31:0]	pkt_0_int_clear	0x0	0xffffffff	Clear all the pkt0 interrupt
0x5084[31:0]	pkt_0_int_mask_n	0x0	0xffffffff	Enable all the pkt0 interrupt
0x5098[31:0]	pkt_1_int_clear	0x0	0xffffffff	Clear all the pkt1 interrupt
0x5094[31:0]	pkt_1_int_mask_n	0x0	0xffffffff	Enable all the pkt1 interrupt
0x50a8[31:0]	pkt_2_int_clear	0x0	0xffffffff	Clear all the pkt2 interrupt
0x50a4[31:0]	pkt_2_int_mask_n	0x0	0xffffffff	Enable all the pkt2 interrupt
0x50c8[31:0]	scdc_int_clear	0x0	0xffffffff	Clear all the SCDC interrupt
0x50c4[31:0]	scdc_int_mask_n	0x0	0xffffffff	Enable all the SCDC interrupt
0x50d8[31:0]	hdcp_int_clear	0x0	0xffffffff	Clear all the HDCP interrupt
0x50d4[31:0]	hdcp_int_mask_n	0x0	0xffffffff	Enable all the HDCP interrupt
0x5108[31:0]	cec_int_clear	0x0	0xffffffff	Clear all the CEC interrupt
0x5104[31:0]	cec_int_mask_n	0x0	0xffffffff	Enable all the CEC interrupt
0x210[1:0]	scramble_en_sel_qst	0x0	0x1	HDMI2.0 Scrambling Enable selector. 2’b00: SCDC control(default) 2’b01: Auto-detect. Enable descrambling when scrambled data is detected. 2’b10: Forces descrambling disable 2’b11: Forces descrambling enable
0x760[14:0]	ced_chlockmaxer_qst	0x0		Maximum errors detected within a period of 10ms to consider that the channel is locked. A channel shall be deemed to be locked if it accumulates a maximum of one error per Mcsc over the 10ms period.For example,if itmdsqpclk is 148.5M(4pixel rate),it is 594,if itmdsqpclk is 37.125M(4pixel rate),it is 149.
0x760[24]	ced_ctrlchecken_qst	0x1	0x1	Enable Character Error Checking during Control Period

SFR Address	SFR Name	Default Value	Setting Value	Description
0x760[25]	ced_gbchecken_qst	0x1	0x1	Enable Character Error Checking during Guard Bands
0x760[26]	ced_dataischecken_qst	0x1	0x1	Enable Character Error Checking during Data Island
0x760[27]	ced_viddatachecken_qst	0x1	0x1	Enable Character Error Checking during Video Data

(2)audio process

Table 25-13 audio process configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x480[1]	i2s_en	0x0	0x0	Disable I2S enable
0x480[2]	spdif_en	0x0	0x0	Disable S/PDIF enable
0x5054[12]	aud_fmt_chg_mask_n	0x0	0x0	Mask audio format change interrupt
0x24[9]	audio_enable	0x0	0x0	Disable audio enable
Wait pktdec_acr_rcv_irq interrupt([3]bit of 0x50a0, pkt_2_int_status register), and read acr_packet(0x1100~0x111c).				
Extract cts[19:0] = {acr_sub_packet1[3:0], acr_sub_packet2[7:0], acr_sub_packet3[7:0]}. Extract n[19:0] = {acr_sub_packet4[3:0], acr_sub_packet5[7:0], acr_sub_packet6[7:0]}. reg 0x1104 is {acr_sub_packet3[7:0],acr_sub_packet2[7:0],acr_sub_packet1[7:0], acr_sub_packet0[7:0]},that cts[19:0] = {0x1104[11:8],0x1104[23:16],0x1104[31:24]}; reg 0x1108 is {acr_sub_packet7[7:0],acr_sub_packet6[7:0],acr_sub_packet5[7:0], acr_sub_packet4[7:0]},that n[19:0] = {0x1108[3:0],0x1108[15:8],0x1108[23:16]};				
Read tmdsqpclk value. Read 0x84[19:0], it is tmdsqpclk, it is tmdsclk/4(tmdsclk is the TMDS clock frequency of the single pixel rate , for example if the input resolution is 1080p, the tmdsclk is 148.5M, and tmdsqpclk is 148.5M/4=37.125M)				
Calculate audio clock frequency. Iaudclk = (tmdsqpclk*4)*n/cts. Calculate audio sample frequency fs = iaudclk/128.				
0x140[0](CRU_CLKSEL_CON140)	clk_hdmirx_aud_sel	0x0	0x1	Audio clock selection, select clk_hdmirx_aud_frac.
0x139[31:0](CRU_CLKSEL_CON139)	hdmirx_aud_frac_div	0x0		Configure iaudclk frequency fractional division coefficient. The audio clock source is 1188M, if the iaudclk is 6.144M, 1188/6.144 = 193.36. and 1/193.359 = 100/19336, so [31:16] = 0x64(100), [15:0] = 0x4b88(19336)
Wait pktdec_audif_rcv_irq interrupt([13]bit of 0x50a0, pkt_2_int_status register), and read audif_packet(0x1240~0x125c).				

SFR Address	SFR Name	Default Value	Setting Value	Description
Wait pktdec_amd_rcv_irq interrupt([9]bit of 0x50a0, pkt_2_int_status register), and read audio_metadata_packet(0x11c0~0x11dc).				
Extract channel count = audif_sub_packet1[2:0]. And driver can also extract other information from this audio_infoframe packet.				
0x24[9]	audio_enable	0x0	0x1	Configure audio enable
0x480[1]	i2s_en	0x0	0x0/0x1	If audio format is I2S, and enable i2s_en, configure 1'b1
0x480[2]	spdif_en	0x0	0x0/0x1	If audio format is S/PDIF, and enable spdif_en, configure 1'b1
0x468[9:0]	afifo_thr_pass_qst	0x0		Configure audio FIFO pass threshold level. For example, driver configures afifo_thr_pass_qst[9:0] = 10'd4, if The HDMIRX receives 16 audio packet, and will begin to read the HDMIRX audio FIFO, and begin to output the I2S/S/PDIF.
0x46c[25:16]	afifo_thr_low_qst	0x0		Configure audio FIFO low threshold level. For example, driver configures afifo_thr_low_qst[9:0] = 10'd2, if The HDMIRX audio FIFO has left 8 audio packet, and it will indicate HDMIRX audio FIFO is almost read empty, and we must adjust audio clock, or HDMIRX has lost the audio sample.
0x46c[9:0]	afifo_thr_high_qst	0x0		Configure audio FIFO high threshold level. For example, driver configures afifo_thr_low_qst[9:0] = 10'd64, if The HDMIRX audio FIFO has 256 audio packet, and HDMIRX has received too many audio packet, driver should adjust audio clock.
0x470[25:16]	afifo_thr_mute_low_qst	0x0		Configure audio FIFO mute low threshold level. For

SFR Address	SFR Name	Default Value	Setting Value	Description
				example, driver configures afifo_thr_low_qst[9:0] = 10’d1, if The HDMIRX audio FIFO has left 4 audio packet, and it will mute audio output.
0x470[9:0]	afifo_thr_mute_high_qst	0x0		Configure audio FIFO mute high threshold level. For example, driver configures afifo_thr_high_qst[9:0] = 10’d100, if The HDMIRX audio FIFO has received 400 audio packet, and it will mute audio output.
0x464[0]	afifo_init_p	1’b0	1’b1	Configure audio FIFO initialization pulse, and audio FIFO address pointers will be reset, and restart to receive audio data. If aud_fifo_overflow/aud_fifo_underflow, driver should also configure this bit.
0x5054[12]	aud_fmt_chg_mask_n	0x0	0x1	unmask audio format change interrupt

Driver should adjust iaudclk frequency in an interval of time, because HDMITX source audio clock frequency may be different from HDMIRX sink audio clock frequency. If driver ignores this audio clock difference, the audio FIFO may be read empty or write full. So driver must adjust iaudclk frequency in a fixed time intervals.

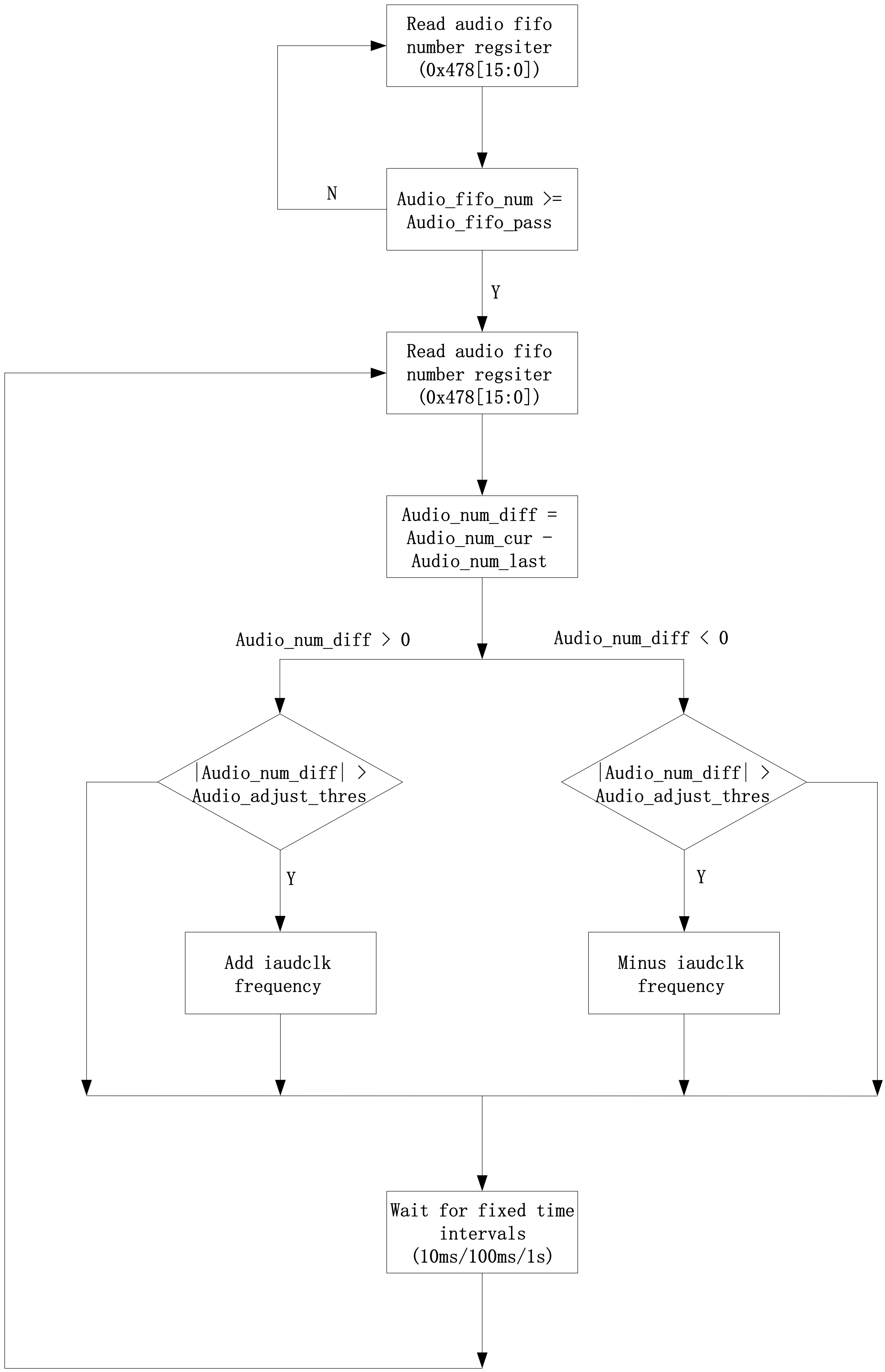

Fig. 25-21 audio clock adjust flow

(3)video resolution change process
If HDMITX changes the video resolution, and HDMIRX phy will lock again, and driver should detect this change event.

Table 25-14 video resolution change operation

SFR Address	SFR Name	Default Value	Setting Value	Description
wait tmdsqpclk_off_chg_irq interrupt(0x5010[5]), if this interrupt happens, it indicates that tmdsqpclk has been changed.				
Read the 0x84[19:0], it is tmdsqpclk_freq, it indicates the tmdsqpclk frequency.				
wait tmdsvalid_stable_chg_irq(0x5030[1]), It indicates that TMDS valid has been changed.				
Configure HDMIRX phy process and HDMIRX controller process again.				

(4)CEC operation
After CEC IOMUX configuration, driver can perform CEC operation, include sending process and receiving process.

Table 25-15 CEC sending operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x2020[3:0]	cec_tx_count	0x0		Configure the frame message size in bytes.
0x2024[31:0]	cec_tx_data3_0	0x0		Configure CEC tx data byte0-byte3. cec_tx_data byte0 is header block: {Initiator_address[3:0],Destination_address[3:0]}
0x2028[31:0]	cec_tx_data7_4	0x0		Configure CEC tx data byte4-byte7
0x202c[31:0]	cec_tx_data11_8	0x0		Configure CEC tx data byte8-byte11
0x2030[31:0]	cec_tx_data15_12	0x0		Configure CEC tx data byte12-byte15
0x2000[0]	frame_send_set_p	0x0	0x1	Configure to trigger CEC sending a frame as an initiator
Wait cectx_done_irq(0x5100[0]), If this interrupt triggers, it indicates that one frame has been send successfully. Or the driver will receive one or more of these interrupt below. cectx_nack_irq(0x5100[1]) cectx_arblost_irq(0x5100[2]) cectx_line_err_irq(0x5100[3]) cectx_nretransmit_fail_irq(0x5100[4]) cectx_frame_discarded_irq(0x5100[5])				

The following sequence describes the process of CEC receiving one frame.

Table 25-16 CEC receiving operation

SFR Address	SFR Name	Default Value	Setting Value	Description
Wait the interrupt cecrx_eom_irq(0x5100[11]bit), and if this interrupt triggers, it indicates that CEC has received one frame.				

SFR Address	SFR Name	Default Value	Setting Value	Description
Read the cec_rxbuffer_cnt(0x2040[3:0]), it is the received frame message size in bytes, including Header and Data blocks.				
Read the cec_rx_data3_0(0x2044). Read the cec_rx_data7_4(0x2048). Read the cec_rx_data11_8(0x204c). Read the cec_rx_data15_12(0x2050).				
0x2054[0]	locked_rxbuffer_clr_p	0x0	0x1	Configure this bit to allow the controller to receive a new incoming message.

25.6.1.8 Configure DMA

The following sequence describes the process of DMA.

Table 25-17 HDMIRX DMA operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x4410[0]	hdmirx_axi_error_int_clear_en	0x0	0x1	Clear hdmirx_axi_error_int
0x4410[1]	fifo_underflow_int_clear_en	0x0	0x1	Clear fifo_underflow_int
0x4410[2]	fifo_overflow_int_cleare_en	0x0	0x1	Clear fifo_overflow_int
0x4410[3]	timing_mismatch_int_clear_en	0x0	0x1	Clear timing_mismatch_int
0x4410[4]	false_frame_end_int_clear_en	0x0	0x1	Clear false_frame_end_int
0x4410[5]	last_frame_axi_unfinish_int_clear_en	0x0	0x1	Clear last_frame_axi_unfinish_int
0x4410[6]	hdmirx_lock_disable_int_clear_en	0x0	0x1	Clear hdmirx_lock_disable_int
0x4410[7]	hdmirx_dma_idle_int_clear_en	0x0	0x1	Clear hdmirx_dma_idle_int
0x4410[8]	line_flag_int_clear_en	0x0	0x1	Clear line_flag_int
0x440c[8:0]	int_enable	0x0	0x1ff	Enable all the interrupt
Read the video information. Read 0x4434 register for hdmirx_width/hdmirx_height, Read 0x4458 register for HDMIRX color_depth/format.				
0x441c[0]	reg_mirror_en	0x0	0x1	Register mirror enable. It make the register act in next frame start
0x4400[15:12]	ddr_store_format	0x0		Configure the DDR store format corresponding to format. The driver may have to configure alpha_value/

SFR Address	SFR Name	Default Value	Setting Value	Description
				dummy_value/padding_position_en
0x4404[31:0]	frame_addr_y	0x0		Configure RGB/Y component store address
0x4408[31:0]	frame_addr_uv	0x0		Configure UV component store address
0x4414[9]	uv_swap_en	0x0	0x1/0x0	If the format is YCbCr422, it should be configured 1’b0, or it is 1’b1.
0x4414[4]	vsync_toggle_en	0x0	0x1	Invert vsync polarity (optional)
0x4414[5]	hsync_toggle_en	0x0	0x1	Invert hsync polarity (optional)
0x4420[6:0]	vic_value	0x0		Configure vic_value for timing mismatch detection
0x4414[2]	timing_mismatch_int_detection_en	0x0	0x1	Enable timing mismatch detection
0x4418[11:0]	lock_frame_num	0x0	0x2	After hdmirx_lock pull up, and the first two frame will be abandoned as unvalid frame for timing detection and other information detection such as format, color_depth, vic_value.
0x4400[0]	abandon_en	0x0	0x1	When abandon_en enable, if hdmirx_lock is 1’b0, this frame will be treated as unvalid frame and will be abandoned.
Read 0x4454[3]bit(hdmirx_lock), if it is 1’b1, it indicates that HDMIRX three channel have been locked and the input TMDS data is valid.				
0x4414[1]	hdmirx_dma_en	1’b0	1’b1	DMA begins to receive data from HDMIRX controller and begins to store FIFO
0x4418[31:16]	line_flag_num	0x0		If HDMIRX has received line_flag_num lines, and it will trigger line_flag_int interrupt, and It indicates there is almost line_flag_num lines in DDR.
Wait line_flag_int interrupt(0x4410[8]bit), and driver begins to read HDMI data from DDR.				

Chapter 26 HDCP2.3 Controller

26.1 Overview

The HDCP2.3 controller is an Embedded Security Module (ESM). This module is a self-contained module that can be integrated with HDMI and DP cores to ensure DCP robustness rules for HDCP.
The ESM has a small MCU inside. It reads ESM Image for operation through the AXI interface.
The HDCP2.3 Controller supports following features:

- Supports HDCP Revision 2.3
- Bus Interface Features:
  - An AXI port for instruction fetch and shared R/W memory
  - An Identity Interface for secret keys used to secure the ESM
  - An Entropy Interface to a True Random Number Generator(TRNG)
  - A Host Port Interface (APB Interface) for an external host processor to send commands and get status from the ESM.
- Support configurable multi-port, up to six ports, each port can be configurable for HDMI or DP.
- Support configurable Transmitter/Receiver, it can be individually configured for HDMI and/or DP operation
- The HDMI portion of the port supports the following features:
  - HDMI video data and associated control
  - I2C sideband interface connected with the local HDMI I2C interface (shared with DDC) for access to the remote end of the HDCP link
  - A GPIO interface for direct hardware signaling between the ESM and the controller
  - Support HDMI streams up to 48Gbps (maximum data cipher throughput of 42.7Gbps for HDMI operation)
- The DP portion of the port contains the following features:
  - TX and RX AUX FIFO interfaces for access to the remote end of the HDCP link
  - AES keystream FIFO interface
  - A GPIO interface for direct hardware signaling between the ESM and the controller
  - State interface to indicate to the controller the ESM state, and to ensure the controller is synchronized to the ESM regarding its state
  - A Debug interface to allow user-defined controller signals to be captured and logged by the ESM
  - Support DP data rates up to 32.4Gbps (maximum data cipher throughput of 25.92Gbps for DP operation)
- MMU:
  - 4k/64k page size
  - TLB pre-fetch

26.2 Block Diagram

The ESM executes firmware from system memory external to the ESM which must be processed with the supplied tools as the firmware image is encrypted to the keys you created to present on the ID Interface. A host library (supplied in source code) is compiled with your application software running on the host processor to send commands to the ESM and monitor its status for results. The ESM has two types of instantiations, one instantiation has one HDMIRX interface and two HDMITX interface, and another instantiation has two DPTX interface. The following figure illustrates the HDMI controller’s connection with external interfaces.

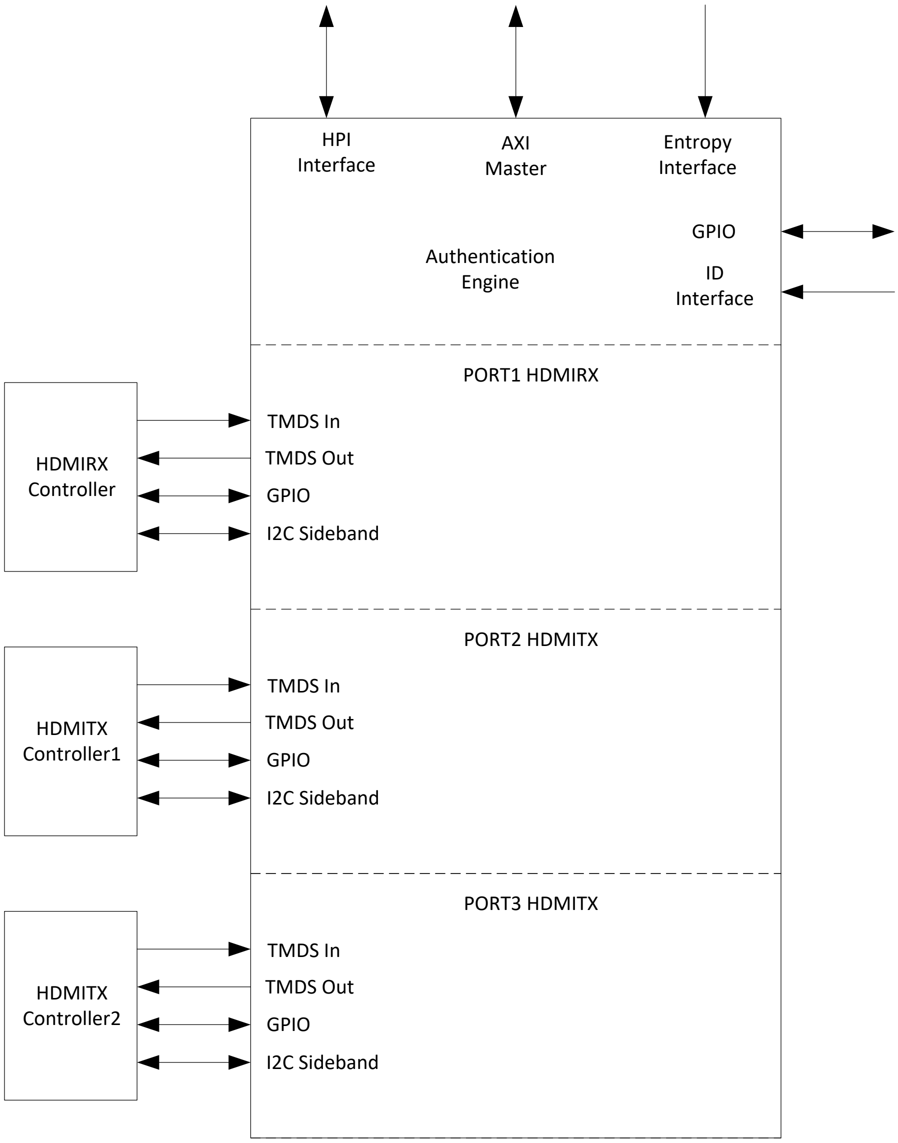

Fig. 26-1 HDCP2.3 with HDMI Block Diagram

The following figure illustrates the DP controller’s connection with external interfaces.

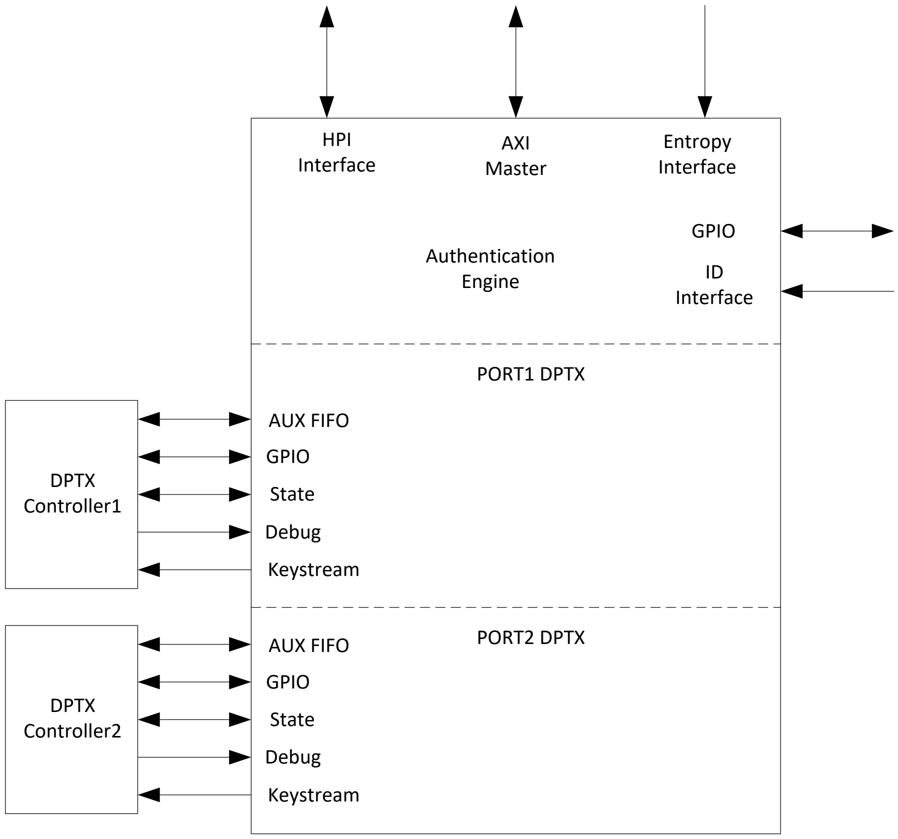

Fig. 26-2 HDCP2.3 with DP Block Diagram

The Embedded Security Module (ESM) is composed of two parts:

- The Authentication Engine (AE) contains a controller that runs the HDCP authentication process.
- The Content Encryption Engine (CEE) is an ESM component that encrypts data for the HDCP transmitter.

The following figure represents how the ESM is typically integrated in SOC.

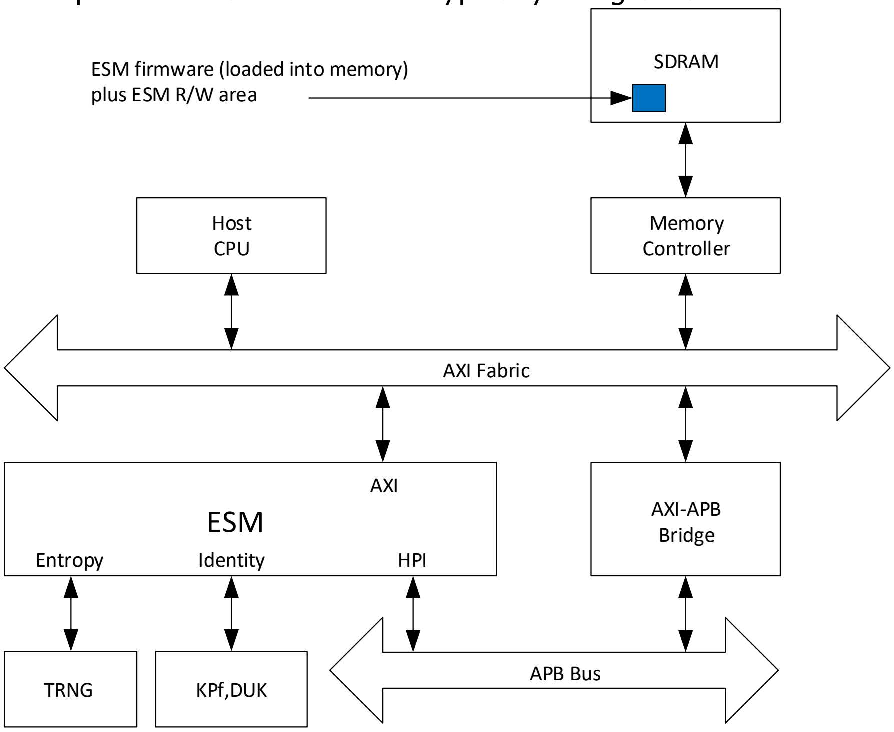

Fig. 26-3 Typical ESM Integration in SOC

26.3 Function Description

26.3.1 AXI interface

The ESM requires continuous access to its firmware for operation, which is accessed through the AXI interface and usually placed a reserved portion of SDRAM. It also uses this interface for communicating messages with the external host processor to pass content such as SRM data, pairing information, and debug/log information.

The ESM requires access to relatively fast and low latency external memory as it randomly accesses its firmware periodically to perform operations. For AXI transactions the average initial access latency may be up to 1000ns.

Note: *The ESM still functions in higher latency systems; however, the ESM may experience intermittent errors, such as failing to authenticate, as there are fixed timeout requirements during the authentication process which must be met. A system with persistent high latency memory accesses may prevent the ESM from fetching its firmware in a timely fashion resulting in protocol timeouts. Following Table summarizes the various requirements the ESM places on the memory, assuming an AXI interface clock of 428(396) MHz and an average latency of 1000 ns.*

Table 26-1 ESM Memory Access

Phase	**Duration (ms)**	**Appropriate Badwidth (Mbytes/sec)**	**Description**
Bootup	100(maximum)	5.0	Initial startup of ESM to Idle state.
TX Authentication	525ms	1.5	ESM transmitter authentication phase including capability check.
RX Authentication	525ms	1.0	ESM receiver authentication phase.
Idle, authenticated	n/a	< 1.0, 4.0	ESM is either in the Idle state waiting to start authentication or in the authenticated state. The second number is when the ESM has debug logging enabled.

The external host memory required by the ESM must be physically contiguous and allocated before the ESM can be started. The ESM Image and R/W memory buffer addresses must be 4K aligned otherwise the ESM cannot properly access the memory. Following table describes the requirements.

Table 26-2 ESM host memory requirements

Size (bytes)	**ESM Access**	**Purpose**
~256K	Read Only	Contains the ESM firmware. This size varies depending on the particular configuration of the ESM you are using.
20K + p*n*256 (TX) (p is the number of transmitters and n is the number of paired devices supported)	Read / Write	Bidirectional communication buffer to exchange data with the Host. Messages such as SRM updates, pairing data, and logging information are placed in this area by the host and the ESM. The number of pairs supported by this parameter is defined in the configuration file.

The provided ESM host application library allocates a small amount of the processor's memory space, which is accessible by the ESM. Communication with this interface is provided by the ESM host application library.

26.3.2 HPI Interface

The external host issues commands to the ESM through the HPI which supports a limited set of commands such as:

- Enabling and disabling of security on the link
- Enabling debugging/logging
- Retrieving pairing information

- Updating the SRM
- ESM status

Communication with this interface is provided by the ESM host application library.

26.3.3 APB interface (HPI)

The external host issues commands to the ESM through the HPI. The ESM supports a limited set of commands such as:

- Enabling and disabling of content security on the link
- Enabling debugging/logging
- Retrieving pairing information
- Updating the SRM
- ESM status

The external host must issue a SRM list to the ESM when one is available, according to the requirements of DCP LLC.
Communication with this interface is provided by the ESM host application library.

26.3.4 Identity Interface

This interface contains the secret keys the ESM requires to implement its security. The KPf and
DUK signals on this interface must be secure from tampering and external user observation as it is used by the ESM to create session keys and other cryptographic secrets required for operation.
When integrating the ESM into your design, you must take to ensure that these requirements are met otherwise the operation of the ESM can be compromised.

Table 26-3 Secure Key for ESM

Description	Purpose
Platform Key (KPf)	A customer created secret random key used to decrypt the ESM firmware. The KPf is intended to be common across a deployed model of a product.
Device Unique Key (DUK)	A customer created secret random key used to decrypt the DCP key data and to encrypt and decrypt content unique to the ESM such as the pairing message content. It is strongly recommended this value should be unique for every unit.
Device Number (Devnum)	This is a non-secret device number and is currently not used.

Note: *The KPf and DUK must be kept confidential as exposing either one compromises the security of the ESM.*

26.3.5 Entropy Interface

This interface connects to a True Random Number Generator (TRNG). The nonce data on this interface must be secure from tampering and external user observation as it is used by the ESM to create session keys and other cryptographic secrets required for secure operation.

Table 26-4 Entropy Interface

Signal	Description
I_ent_val[127:0]	This is the nonce data from the TRNG. The value is used to seed the ESM's PRNG which is used to generate keys for the authentication process and session keys. The value must be truly random and not generated by another PRNG, as per the HDCP for HDMI specification, Section 2.13 (Random Number Generation). Note the requirements for DP are the same.
O_ent_gen	If the ESM pull up this signal and will make TRNG generate n new I_ent_val[127:0].
I_ent_vld	I_ent_val valid signal, if it is 1'b1, it indicates that I_ent_val[127:0] is valid for ESM.

The ESM may request the generation of a new nonce by asserting the O_ent_gen signal. This signal involves an automatic handshake between the two cores and normally remains asserted until the TRNG for ESM responds lowering the I_ent_vld signal. At this point the

ESM normally acknowledges that the new request is underway by withdrawing the O_ent_gen signal. At this point the TRNG for ESM is generating a new nonce. When the nonce is stable, the TRNG for ESM raises the I_ent_vld signal indicating that the ESM can safely read the nonce value from the I_ent_val port. The ESM nonce interface waveform is in the figure below.

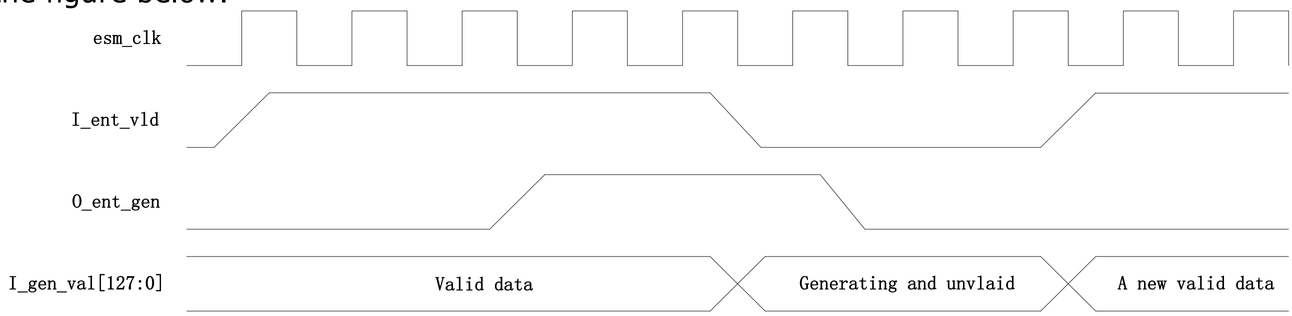

Fig. 26-4 ESM nonce interface

26.3.6 GPIO Interface

This interface contains a number of general purpose inputs and outputs which can be used by the host to monitor the status of the ESM.

26.3.7 HDMI Interface

The HDMI interface contains logic to apply content protection to the Data and Video Islands as the TMDS data passes through the ESM.

Table 26-5 HDMI Interface

Description	**Purpose**
I2C sideband	I2C sideband interface connected with HDMIRX/HDMITX I2C controller, and use the HDMIRX/HDMITX DDC interface for HDCP protocol communication with the remote device. It is mapped by the controller onto the DDC interface.
GPIO	Direct signals between the controller and the ESM to indicate the status of the ESM to the controller, and to signal the ESM
TMDS In	TMDS data output from the controller. For TX this is the unencrypted data, for the RX this is the encrypted data.
TMDS Out	TMDS data input to the controller. For a TX this is the encrypted data, for the RX this is the decrypted data.

The DP interface provides a cipher key stream to the controller which is responsible for XORing it onto the appropriate data symbols as identified in the HDCP for DP Specification, Section 3 (HDCP Encryption).

Table 26-6 DP Interface

Description	**Purpose**
AUX FIFO	Separate Ingress and Egress FIFOs for HDCP protocol communication with the remote device, mapped by the controller onto the AUX channel.
GPIO	Direct signals between the controller and the ESM to indicate the status of the ESM to the controller, and to signal the ESM
State	Signals from the ESM to the controller to indicate its state, with signals reflected back from the controller to the ESM to ensure the controller's state is synchronized with the ESM.
Debug	A general purpose debug port which allows the ESM to capture arbitrary signals from the controller for logging.
Keystream	A stream of AES keys used to decrypt the content data.

26.3.8 HDCP2.3 Controller Behavior

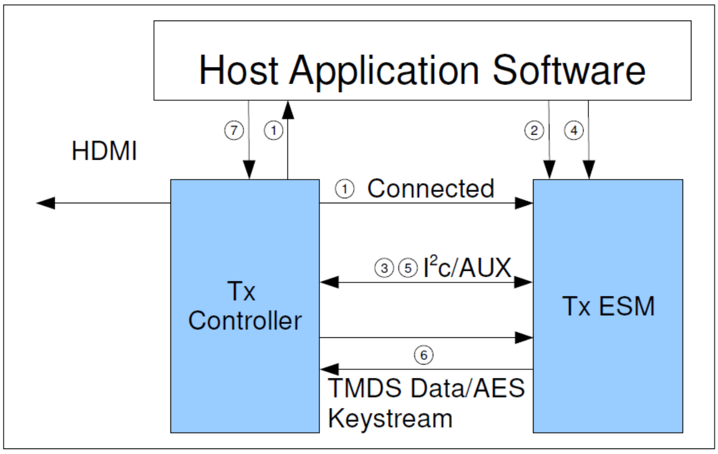

Fig. 26-5 Transmitter Authentication

If HDCP2.3 controller is a transmitter, it works as following steps:

1. The controller asserts the connected signal to the ESM. The application software receives the notification from the controller. For HDMI operation the ESM outputs a fixed pattern (the BSOD value) on the TMDS data output.
2. The application software issues the command HLC_HDCPTX_SetCapability which causes the ESM to perform a capability check with the receiver. Before this point in time the ESM does not know the capability of the RX so the port's capable GPIO output signal is not asserted.
3. The ESM queries the receiver. If the receiver does not support HDCP2.3 then the port's not_capable GPIO output is asserted. The application software should then check if the receiver supports HDCP1.4 (or no link protection) and take appropriate action; the ESM is no longer required. If the receiver supports HDCP2.3 then the capable GPIO output is asserted and the ESM transitions to a pre-authorized state. For HDMI operation this means unencrypted low value content is permitted on the video path (TMDS interface).
4. If the receiver supports HDCP2.3 the application software issues the command HLC_HDCP_Authenticate to the ESM. As a security feature the ESM enforces a timeout (set in the configuration file) after the receiver indicates it is HDCP2.3 capable to the time the command HLC_HDCP_Authenticate must be issued. If you exceed this time out you must repeat the process from step #2. (When the port is configured for HDMI it will switch its TMDS output back to the fixed pattern output).
5. The ESM initiates authentication with the receiver and successfully completes authentication (or not). The application software and the HDMI controller are appropriately notified (authenticated and authentication_failed outputs asserted accordingly).
6. If authentication is successful the ESM starts to encrypt the TMDS data (HDMI).
7. The application software can now send high value content securely on the link.

Following successful authentication the ESM periodically checks the status of the connected receiver. If a response is not received, or the receiver requests re-authentication the ESM immediately outputs a fixed pattern on the TMDS output (HDMI), asserts the outputs authentication_failed along with a reath_req, and returns to the Idle state. To re-authenticate you must call the function HLC_HDCP_Authenticate to drop authentication and then call the function again to start authentication.

26.3.9 HDCP2.3 Software Initialization

An external host controller (ARM Core or MCU) allocates memory, initializes the ESM, and enables the ESM controller. The general reset and startup sequence is:

a. Configure clocks for HDCP controller.

b. Load KPf & DUK from effuse to gasket.
c. The ESM reset is de-asserted and the ESM enters a reset state.
d. The host allocates contiguous memory for the firmware and R/W areas. The buffers are 4K aligned.
e. The host configures the ESM's HPI interface, defining the physical memory pointer for the
ESM firmware.
f. The host copies the ESM firmware from persistent storage to the firmware memory location.
g. The host enables the ESM controller, putting it in a running state. At this point the ESM initiates transactions on the AXI bus to fetch its firmware.
h. ESM asserts a GPIO to indicate it is booted to indicate it can accept commands. The status can also be monitored from the HPI interface.

The ESM host application library provides the startup sequence from step d through h.

26.3.10 Autostart

The autostart feature is an option which permits a transmitter or receiver port (configurable per port) on the ESM to autonomously take over the detection of a connection and run through the authentication process without intervention from the external host. In the event of an error the port automatically retries up to a specified number of attempts (configuration based) before idling requiring intervention from the host.

For a transmitter this feature automates the capability checking and authentication along with any re-authentication which may be required due to link errors. For a receiver this feature enables the port to immediately respond to authentication requests without host intervention.

26.3.11 Key Usage

There are two secrets, 128 bit keys you are responsible for creating for use by the ESM.

The Platform Key (KPf) is used by the ESM to decrypt its firmware. It is recommended this key be common for all ESMs deployed for a particular product as it permits a common (encrypted) firmware image to be deployed.

The Device Unique Key (DUK) is used by the ESM to protect secrets unique to the device such as HDCP receiver keys and locally generated data such as pairing information. Although it is not required, it is strongly recommended this key be unique for every different unit deployed in a product so that if the KPf is and DUK are compromised, device specific secrets for only that unit are exposed. Using a common DUK for all devices could permit device specific secrets for all devices to be exposed.

As shipped from the factory, the firmware cannot be used as-is and must be processed with tools that are provided with the ESM software package. Figure below illustrates the tools and the flow that are required to produce encrypted ESM firmware. You edit the firmware.aic file supplied with the firmware image and replace the factory test/simulation values with your secret KPf and DUK keys.

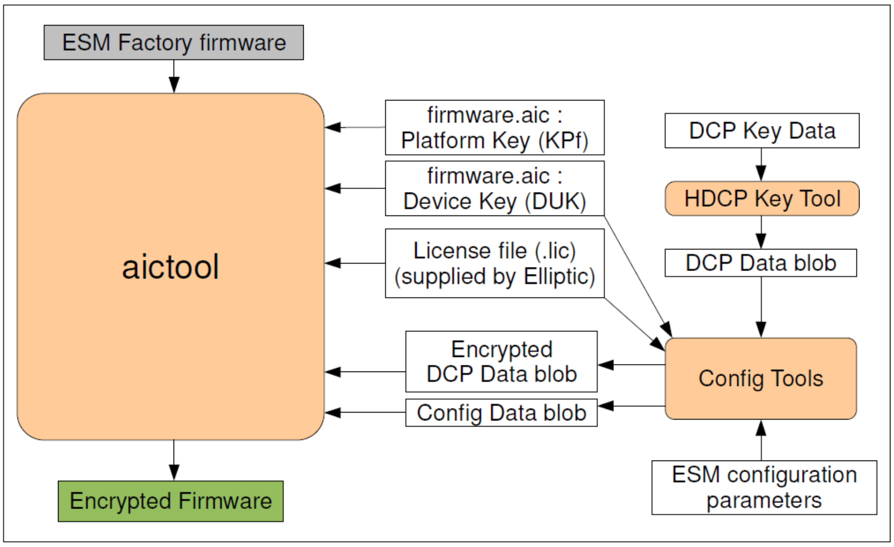

Fig. 26-6 ESM Image tool flow

The DCP TX key data is common for all transmitter ports whereas the DCP RX key data is unique for each receiver port.

To facilitate manufacturing it is highly desirable to build and deploy a common software image for all units. If ESM only contains transmitter ports then it is possible to do this, however if you also have receiver ports you are required by DCP to have a unique receiver key for each receiver in your design.

26.4 Register Description

26.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

26.4.2 HDCP2.3 Registers Summary

Name	Offset	Size	Reset Value	Description
FW_INFO_0	0x0008	W	0x00000000	Firmware Information 0
FW_INFO_1	0x000C	W	0x00000000	Firmware Information 1
HOST_IRQ_EN	0x0010	W	0x00000000	Interrupt enables
HOST_IRQ_STAT	0x0014	W	0x00000000	Interrupt Status
FW_ADDR	0x0020	W	0x00000000	Firmware Address
HOST_CTRL	0x002C	W	0x00000000	Host Control
HOST_MB_P0	0x0030	W	0x00000000	Host Mailbox Parameter 0
HOST_MB_P1	0x0034	W	0x00000000	Host Mailbox Parameter 1
HOST_MB_CTRL	0x0038	W	0x00000000	Host Mailbox Control
HOST_MB_OWN	0x003C	W	0x00000000	Host Mailbox Ownership
CPU_MB_P0	0x0040	W	0x00000000	CPU Mailbox Parameter 0
CPU_MB_P1	0x0044	W	0x00000000	CPU Mailbox Parameter 1
CPU_MB_CTRL	0x0048	W	0x00000000	CPU Mailbox Control
CPU_MB_OWN	0x004C	W	0x00000000	CPU Mailbox Ownership
OOB_STAT	0x005C	W	0x00000000	Out-of-band Status
ERR_STAT	0x0060	W	0x00000000	Error Status
USER_NOTIFY	0x0064	W	0x00000000	User Notification
VERSION_0	0x0070	W	0x00000000	Version Information 0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.3 HDCP2.3 Detail Registers Description

FW_INFO_0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	info Firmware version/info

FW_INFO_1
Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	info Firmware version/info

HOST_IRQ_EN
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	glbl Global IRQ enable 1'b0: Disable irq enable 1'b1: Enable irq
30:22	RO	0x000	reserved
21	RW	0x0	err Error IRQ enable 1'b0: Disable irq enable 1'b1: Enable irq
20	RW	0x0	oob OOB IRQ enable 1'b0: Disable irq enable 1'b1: Enable irq
19:18	RO	0x0	reserved
17	RW	0x0	mb_rtn Mailbox return IRQ enable 1'b0: Disable irq enable 1'b1: Enable irq
16	RW	0x0	mb_msg Mailbox message IRQ enable 1'b0: Disable irq enable 1'b1: Enable irq
15:0	RW	0x0000	user User IRQ enable 16’h0: Disable irq enable 16’h1: Enable irq

HOST_IRQ_STAT
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	W1C	0x0	err Indicates the error status register has been written 1'b0: Inactive 1'b1: Active
20	W1C	0x0	oob Indicates the out-of-band status register has been written. 1'b0: Inactive 1'b1: Active
19:18	RO	0x0	reserved

Bit	Attr	Reset Value	Description
17	W1C	0x0	mb_rtn Indicates that the ESM has returned host mailbox ownership 1'b0: Inactive 1'b1: Active
16	W1C	0x0	mb_msg Indicates that the ESM has written a message to the mailbox 1'b0: Inactive 1'b1: Active
15:0	W1C	0x0000	user User defined interrupts triggered by writing to the USER_NOTIFY register. 16'h0: Inactive 16'h1: Active

FW_ADDR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	ptr Pointer that controls the base address of the firmware image. This pointer is 4KB aligned. The pointer becomes RO and may not be modified after the HOST_CTRL/FW_VLD is written.
11:0	RO	0x000	reserved

HOST_CTRL

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	fw_vld The host may write this field with a "1" to start the ESM. All identity information must be available on the identity interface, the FW_ADDR register must be setup and the firmware must be loaded in the external memory prior to writing this register. 1'b0: Inactive 1'b1: Active

HOST_MB_P0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	param This is the lower 32 bits of the 64 bit arbitrary information corresponding to the current command to be passed through the host mailbox.

HOST_MB_P1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	param This is the upper 32 bits of the 64 bit arbitrary information corresponding to the current command to be passed through the host mailbox.

HOST_MB_CTRL

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	cmd Writing this register sends a mailbox command to the ESM

HOST_MB_OWN

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	own This indicates ownership of the host mailbox. It is set by a write to the HOST_MB_CTRL register. It is cleared by the ESM after the mailbox command has been processed. The host mailbox registers must not be modified while the ESM owns the mailbox. When the ESM clears the bit, an MB_RTN interrupt is generated. 1'b0: Not-owned 1'b1: Owned

CPU_MB_P0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	param This is the lower 32 bits of the 64 bit arbitrary information corresponding to the current command passed through the cpu mailbox

CPU_MB_P1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	param This is the upper 32 bits of the 64 bit arbitrary information corresponding to the current command passed through the cpu mailbox

CPU_MB_CTRL

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	cmd This register contains the cpu mailbox command from the ESM. When the ESM writes this register the host receives an MB_MSG interrupt

CPU_MB_OWN

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	own This indicates the ownership of the CPU mailbox. It is set when the ESM writes a mailbox command to the CPU_MB_CTRL register. It is cleared by the host writing a "1" to this register 1'b0: Not-owned 1'b1: Owned

OOB_STAT

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	stat This register communicates out-of-band information to the host. When the register is written by the ESM, an OOB interrupt is generated.

ERR_STAT

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	stat This register communicates back to the host that a serious error condition has occured. When the register is written by the ESM, an ERR interrupt is generated. An update on the hardware diagnostic port is also triggered.

USER_NOTIFY

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	idx A write of this register with a "1" in any bit position will cause the corresponding USER_x interrupt to be sent to the other processor. A write value of zero is not permitted. 16'h0: Inactive 16'h1: Active

VERSION_0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	epn Project Number encoded in BCD
15:8	RO	0x00	reserved
7:4	RO	0x0	major Major release version number
3:0	RO	0x0	minor Minor release version number

26.4.4 TRNG Registers Summary

Name	Offset	Size	Reset Value	Description
CTRL	0x0000	W	0x00000000	This register causes the TRNG to execute one of a number of actions. There are 3 commands available
STAT	0x0004	W	0x00070000	The NONCE_MODE field indicates that the engine is currently waiting for the host to load a nonce
MODE	0x0008	W	0x00000000	This register is used to set the length of the PRNG output register
SMODE	0x000C	W	0x000A0000	This register is used to enable or disable certain mission-mode run-time features within the core

Name	Offset	Size	Reset Value	Description
IE	0x0010	W	0x00000000	This register is used to enable or disable interrupts within the TRNG
ISTAT	0x0014	W	0x00000000	This register allows the user to monitor the interrupt and/or status contributions of the TRNG
COREKIT_REL	0x0018	W	0x00000000	Contains the coreKit release information
FEATURES	0x001C	W	0x00000000	Contains the build-time parameter enumerations
RAND0	0x0020	W	0x00000000	The RAND0 register is part of the RANDx register set
RAND1	0x0024	W	0x00000000	The RAND1 register is part of the RANDx register set
RAND2	0x0028	W	0x00000000	The RAND2 register is part of the RANDx register set
RAND3	0x002C	W	0x00000000	The RAND3 register is part of the RANDx register set
RAND4	0x0030	W	0x00000000	The RAND4 register is part of the RANDx register set
RAND5	0x0034	W	0x00000000	The RAND5 register is part of the RANDx register set
RAND6	0x0038	W	0x00000000	The RAND6 register is part of the RANDx register set
RAND7	0x003C	W	0x00000000	The RAND7 register is part of the RANDx register set
SEED0	0x0040	W	0x00000000	The SEED0 register is part of the SEEDx register set
SEED1	0x0044	W	0x00000000	The SEED1 register is part of the SEEDx register set
SEED2	0x0048	W	0x00000000	The SEED2 register is part of the SEEDx register set
SEED3	0x004C	W	0x00000000	The SEED3 register is part of the SEEDx register set
SEED4	0x0050	W	0x00000000	The SEED4 register is part of the SEEDx register set
SEED5	0x0054	W	0x00000000	The SEED5 register is part of the SEEDx register set
SEED6	0x0058	W	0x00000000	The SEED6 register is part of the SEEDx register set
SEED7	0x005C	W	0x00000000	The SEED7 register is part of the SEEDx register set
AUTO_RQSTS	0x0060	W	0x00000000	This register allows the TRNG to generate a reseed reminder alarm
AUTO_AGE	0x0064	W	0x00000000	This register allows the TRNG to generate a reseed reminder alarm
TIME_TO_SEED	0x006C	W	0x00000000	This register contains the number of clock cycles taken to generate the last new random seed
BUILD_CFG0	0x00F0	W	0x00000000	Contains the build-time parameter settings

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.5 TRNG Detail Registers Description

CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	cmd Execute a command 3'b000: (CMD_NOP) Execute a NOP 3'b001: (CMD_GEN_RAND) Generate a random number 3'b010: (CMD_RAND_RESEED) Execute a random reseed 3'b011: (CMD_NONCE_RESEED) Execute a nonce reseed Others: Reserved

STAT

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	rand_reseeding Current state of random seed generation operations 1'b0: (NO_RAND_RESEED_IN_PRGRS) No random reseed generation process in progress 1'b1: (RAND_RESEED_IN_PRGRS) Random reseed generation process in progress
30	RO	0x0	rand_generating Current state of random number generation operations 1'b0: (NO_RAND_GEN_IN_PRGRS) No random number generation process in progress 1'b1: (RAND_GEN_IN_PRGRS) Random number generation process in progress
29:28	RO	0x0	reserved
27	RO	0x0	srvc_rqst Current state of unacknowledged request indicator 1'b0: (NO_UNACK_RQST) No unacknowledged service request 1'b1: (UNACK_RQST) Unacknowledged service request
26:19	RO	0x00	reserved
18:16	RO	0x7	last_reseed Action which loaded current seed 3'b000: (SEEDED_BY_CMD) Reseeded by host random reseed command 3'b001: Reserved 3'b010: Reserved 3'b011: (SEEDED_BY_NONCE) Reseeded by nonce 3'b100: (SEEDED_BY_PIN) Reseeded by I_ctrl_reseed driven to 1 or internal auto-reseed 3'b101: Reserved 3'b110: Reserved 3'b111: (UNSEEDED) Unseeded (zeroized state)
15:10	RO	0x00	reserved
9	RO	0x0	seeded Current SEEDED state 1'b0: (NOT_SEEDED) PRNG core is not seeded 1'b1: (SEEDED) PRNG core is seeded
8	RO	0x0	mission_mode Reflects state of SMODE. MISSION_MODE
7:4	RO	0x0	reserved
3	RO	0x0	r256 Reflects state of MODE. R256

Bit	Attr	Reset Value	Description
2	RO	0x0	nonce_mode Current state of NONCE mode 1'b0: (NONCE_DISABLED) Nonce mode disabled 1'b1: (NONCE_ENABLED) Nonce mode enabled
1:0	RO	0x0	reserved

MODE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	r256 Current length for PRNG RANDx registers 1'b0: (PRNG_128bit) PRNG set up for 128-bit maximum 1'b1: (PRNG_256bit) PRNG set up for 256-bit maximum
2:0	RO	0x0	reserved

SMODE

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x0a	max_rejects Maximum number of consecutive bit rejections before issuing ring tweak.
15:9	RO	0x00	reserved
8	RW	0x0	mission_mode Sets the operating mode to TEST or MISSION 1'b0: (EN_TEST_MODE) Test mode (access to internal state and test fields) 1'b1: (EN_MISSION_MODE) Mission mode (no access to internal state) NOTE: Any change to the state of this field (1 to 0 or 0 to 1) causes the TRNG to zeroize itself.
7:3	RO	0x00	reserved
2	RW	0x0	nonce_mode Sets the reseed mode to nonce or random 1'b0: (EN_NONCE_RESEED) Disable nonce mode 1'b1: (EN_RANDON_RESEED) Enable nonce mode
1:0	RO	0x0	reserved

IE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	glbl_en Global interrupt enable 1'b0: (LFSR_LOCKUP_EXC) Globally disable interrupts 1'b1: (LFSR_LOCKUP_INC) Globally enable interrupts
30:5	RO	0x0000000	reserved
4	RW	0x0	lfsr_lockup_en Include or exclude lfsr_lockup interrupt contribution 1'b0: (LFSR_LOCKUP_EXC) Disable lfsr_lockup interrupt contribution 1'b1: (LFSR_LOCKUP_INC) Enable lfsr_lockup interrupt contribution

Bit	Attr	Reset Value	Description
3	RW	0x0	rqst_alarm_en Include or exclude rqst_alarm interrupt contribution. 1'b0: (RQST_ALARM_EXC) Disable rqst_alarm interrupt contribution 1'b1: (RQST_ALARM_INC) Enable rqst_alarm interrupt contribution
2	RW	0x0	age_alarm_en Include or exclude age_alarm interrupt contribution 1'b0: (AGE_ALARM_EXC) Disable age_alarm interrupt contribution 1'b1: (AGE_ALARM_INC) Enable age_alarm interrupt contribution
1	RW	0x0	seed_done_en Include or exclude seed_done interrupt contribution. 1'b0: (SEED_DONE_EXC) Disable seed_done interrupt contribution 1'b1: (SEED_DONE_INC) Enable seed_done interrupt contribution
0	RW	0x0	rand_rdy_en Include or exclude rand_rdy interrupt contribution. 1'b0: (RAND_RDY_EXC) Disable rand_rdy interrupt contribution 1'b1: (RAND_RDY_INC) Enable rand_rdy interrupt contribution

ISTAT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	lfsr_lockup Status and acknowledgment (clearing) of lfsr_lockup indicator When read this bit 1'b0: (LFSR_LOCKUP_R0) No unacknowledged lfsr_lockup indicator 1'b1: (LFSR_LOCKUP_R1) Unacknowledged lfsr_lockup indicator When write this bit 1'b0: (LFSR_LOCKUP_W0) NOP 1'b1: (LFSR_LOCKUP_W1) Acknowledge lfsr_lockup indicator
3	W1C	0x0	rqst_alarm Status and acknowledgment (clearing) of rqst_alarm indicator When read this bit 1'b0: (RQST_ALARM_R0) No unacknowledged rqst_alarm indicator 1'b1: (RQST_ALARM_R1) Unacknowledged rqst_alarm indicator When write this bit 1'b0: (RQST_ALARM_W0) NOP 1'b1: (RQST_ALARM_W1) Acknowledge rqst_alarm indicator
2	W1C	0x0	age_alarm Status and acknowledgment (clearing) of age_alarm indicator. When read this bit 1'b0: (AGE_ALARM_R0) No unacknowledged AGE_ALARM indicator 1'b1: (AGE_ALARM_R1) Unacknowledged AGE_ALARM indicator When write this bit 1'b0: (AGE_ALARM_W0) NOP 1'b1: (AGE_ALARM_W1) Acknowledge AGE_ALARM indicator

Bit	Attr	Reset Value	Description
1	W1C	0x0	seed_done Status and acknowledgment (clearing) of seed_done indicator When read this bit 1'b0: (SEED_DONE_R0) No unacknowledged seed_done indicator 1'b1: (SEED_DONE_R1) Unacknowledged seed_done indicator When write this bit 1'b0: (SEED_DONE_W0) NOP 1'b1: (SEED_DONE_W1) Acknowledge seed_done indicator
0	W1C	0x0	rand_rdy Status and acknowledgment (clearing) of rand_rdy indicator. When read this bit 1'b0: (RAND_RDY_R0) No unacknowledged rand_rdy indicator 1'b1: (RAND_RDY_R1) Unacknowledged rand_rdy indicator When write this bit 1'b0: (RAND_RDY_W0) NOP 1'b1: (RAND_RDY_W1) Acknowledge rand_rdy indicator

COREKIT_REL

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	ext_enum Indicates the coreKit release extension type. For example, release '2.35e-lca04' is encoded as 0x1. 4'b0000: (EXT_ENUM_GA) GA release 4'b0001: (EXT_ENUM_LCA) LCA release 4'b0010: (EXT_ENUM_EA) EA release 4'b0011: (EXT_ENUM_LP) LP release 4'b0100: (EXT_ENUM_LPC) LPC release 4'b0101: (EXT_ENUM_SOW) SOW release Others: Reserved
27:24	RO	0x0	reserved
23:16	RO	0x00	ext_ver Indicates the coreKit release extension version number. For example, release '2.35e-lp04' is encoded as 0x4. GA releases have a value of 0.
15:0	RO	0x0000	rel_num Indicates the coreKit release version in pseudo-BCD. For example, release '2.35e-lca04' is encoded as 0x235e.

FEATURES

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	bg8 If 1'b1, indicates the seed generator has 8 ring oscillator pairs. If 1'b0, indicates the seed generator has 6 ring oscillator pairs. This build-time configuration parameter is not customermodifiable. 1'b0: (SIX_BGS) 6 Bit Generators present 1'b1: (EIGHT_BGS) 8 Bit Generators present
23:4	RO	0x00000	reserved
3	RO	0x0	mission_mode_reset_state Indicates state of SMODE. MISSION_MODE reset state 1'b0: (RST_TEST_MODE) Resets to TEST_MODE 1'b1: (RST_MISSION_MODE) Resets to MISSION_MODE

Bit	Attr	Reset Value	Description
2	RO	0x0	rand_seed_avail Indicates the ring-oscillator sub-section is present. This build-time configuration parameter is not customermodifiable. 1'b0: (NO_RING_OSC) No ring-oscillator seed generator present 1'b1: (RING_OSC) Ring-oscillator seed generator present
1:0	RO	0x0	max_rand_length Maximum length of the PRNG RANDx register set. 1'b0: (PRNG_128bit) PRNG set up for 128-bit maximum 1'b1: (PRNG_256bit) PRNG set up for 256-bit maximum

RAND0
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 0

RAND1
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 1

RAND2
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 2

RAND3
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 3

RAND4
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 4

RAND5
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 5

RAND6
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 6

RAND7

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rand Random data word 7

SEED0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 0

SEED1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 1

SEED2

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 2

SEED3

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 3

SEED4

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 4

SEED5

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 5

SEED6

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 6

SEED7

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	seed Seed data word 7

AUTO_RQSTS

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rqsts 16'h0: Disable the AUTO_RQSTS alarm feature. 16'h1-16'hffff: Reload value for internal AUTO_RQSTS counter.

AUTO_AGE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	age 16'h0: Disable the AUTO_AGE alarm feature. 16'h1-16'hffff: Reload value for internal AUTO_AGE counter.

TIME_TO_SEED

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	tts Shows the number of system clock cycles taken to generate the last random seed.

BUILD_CFG0

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RO	0x0	cdc_sync_depth Depth of the CDC resynchronizer chains 2'b10: (CDC_RESYNC_2) CDC re-synchronization depth 2 2'b11: (CDC_RESYNC_3) CDC re-synchronization depth 3 2'b00: (CDC_RESYNC_4) CDC re-synchronization depth 4 2'b01: Reserved
7	RO	0x0	rand_rings_avail Indicates if ring-oscillator sub-section is present 1'b0: (NO_RING_OSC) No ring-oscillator seed generator present 1'b1: (RING_OSC) Ring-oscillator seed generator present
6	RO	0x0	bg8 Indicates how many bit generators are present 1'b0: (SIX_BGS) 6 Bit Generators present 1'b1: (EIGHT_BGS) 8 Bit Generators present
5	RO	0x0	auto_reseed_loopback Indicates auto-reseed configuration setting 1'b0: (NO_AUTO_RESEED) No auto-reseed loopback 1'b1: (AUTO_RESEED) Auto-reseed loopback present
4	RO	0x0	mode_after_rst Indicates state of SMODE. MISSION_MODE reset state 1'b0: (RST_TEST_MODE) Resets to TEST_MODE 1'b1: (RST_MISSION_MODE) Resets to MISSION_MODE
3	RO	0x0	prng_len_after_rst State of MODE. R256 after reset 1'b0: (RST_PRNG_128bit) PRNG length set to 128-bit after reset 1'b1: (RST_PRNG_256bit): PRNG length set to 256-bit after reset
2	RO	0x0	max_prng_len Maximum length of the PRNG RANDx register set 1'b0: (PRNG_128bit) PRNG set up for 128-bit maximum 1'b1: (PRNG_256bit) PRNG set up for 256-bit maximum

Bit	Attr	Reset Value	Description
1:0	RO	0x0	core_type Core type 2'b00: (CORE_TYPE_BASE_TRNG) TRNG 2'b01: (CORE_TYPE_BASE_WITH_ESM_NONCE) TRNG with ESM nonce I/O 2'b10: (CORE_TYPE_NIST_TRNG) TRNG NIST 2'b11: (CORE_TYPE_NIST_WITH_EDU) TRNG NIST with EDU

26.4.6 HDCP2.3 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
DTE_ADDR	0x0000	W	0x00000000	MMU current page Table addressIt is only can be written when MMU state is disable or page fault or mmu enable stall state
STATUS	0x0004	W	0x00000018	MMU status register
COMMAND	0x0008	W	0x00000000	MMU command register
PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault
ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
INT_MASK	0x001C	W	0x00000000	MMU raw interrupt status register
INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.7 HDCP2.3 MMU Detail Registers Description

DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr mmu dte base addr , the address must be 4kb aligned

STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master reponsible for last page fault
5	RO	0x0	page_fault_is_write The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	replay_buffer_empty The MMU replay buffer is empty
3	RO	0x1	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command.

Bit	Attr	Reset Value	Description
0	RO	0x0	paging_enabled Paging is enabled

COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

PAGE_FAULT_ADDR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	page_fault_addr address of last page fault

ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	mmu_zap_one_line address to be invalidated from the page table cache

INT_RAWSTAT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error read bus error
0	RW	0x0	page_fault page fault

INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error read bus error
0	WO	0x0	page_fault page fault

INT_MASK

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	read_bus_error read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	page_fault page fault enable an interrupt source if the corresponding mask bit is set to 1

INT_STATUS
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error read bus error
0	RO	0x0	page_fault page fault

AUTO_GATING
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_auto_gating when it is 1'b1, the mmu will auto gating itself.

26.5 Interface Description

There is no Interface signal Description.

26.6 Application Notes

26.6.1 Host Application Software

The ESM package contains a series of tools and a run-time library as bellow:

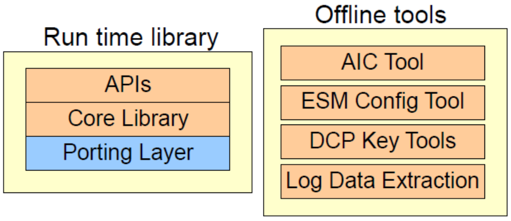

Fig. 26-7 ESM software

26.6.2 Run Time Library

This library is provided as source code and is used by the host application processor to control the ESM.
Setting the configurable options of the ESM is not provided through APIs for security reasons. It is instead embedded into the ESM’s Image as part of the process of building a deployable image.
The APIs provide a minimal interface to the ESM, which include the following:

- Load/Initialize firmware image
- Start authentication to secure a link
- Terminate an authenticated link
- Collect logging data
- Get/Set pairing information
- Update SRM data
- Status updates

Sample code is provided and demonstrates how to use the various APIs. In addition, a software API reference guide is included and provides details on the API calls and their parameters.

26.6.3 Offline Tools

There are three separate offline tools that are required to build a deployable image for the ESM as shown in Figure ESM Image tool flow and one tool for logging information. All of these tools are developed to run on a 32 bit Linux system.

26.6.4 Configuration Tool

The troot_base_config_interface tool is used to convert the various configuration files into a data blob to be used by the aictool which creates the encrypted ESM firmware. There are a number of different configuration files which the tools reads, with each configuration file containing a mix of factory configured parameters, and user-adjustable parameters.

This tool also requires the firmware.aic file in order to generate the data blob.

User Parameters for Configuration Files

The following table indicates which parameters in the configuration files are user-adjustable and other non-described parameters should not be changed. A basic description of the parameter is included below, see the configuration file's comments for a more complete description.

Table 26-7 Configuration files

File Name	Parameter	Description
troot_base_config.cfg	[LOGGING_MODE]	Logging on/off
	[LOGGING_LEVEL]	Sets the verbosity of the output log messages.
	[RESEED_TIMEOUT]	Specifies the time the ESM will wait for the TRNG to supply a new nonce before reporting an error
	[RESEED_AUTO_INTERVAL]	By default the ESM will periodically query the TRNG for a new nonce at the period specified.
	[CPU_FREQ]	Sets the frequency of the esm_clk input. Mandatory to change.
troot_HDCPmgr_TX.cfg	[SRM_VERSION]	Denotes whether the SRM is to be checked or not and the minimum version number permitted.
troot_HDCPTX.cfg	[I2C_FREQ]	(HDMI) Sets the default I2C frequency.can be changed via an API.
	[I2C_USE_SHORT_READ]	(HDMI) Sets whether the interface uses short reads for status requests.can be changed via an API.
	[CEE_BSOD]	(HDMI) Sets the 24 bit fixed pattern value output by the ESM. See the description following this table for more details.
	[AUTO_START]	Sets the default startup state of the Autostart feature
	[HDCP_TIMEOUTS]	Sets whether the ESM enforces the HDCP timeout periods. Should be enabled only for testing and/or debugging.
	[CEE_FRAME_CNT_DEBUG]	(HDMI) The ESM emits periodic log

File Name	Parameter	Description
		messages once authenticated, based on the number of VSYNC pulses counted by this parameter.
	[PAIRING_ENABLED]	Sets whether pairing will be enabled or not
	[MAX_PAIRING_DEVICES]	Sets the maximum number of paired devices supported per port. Note the external R/W memory requirements increase based on this setting, and the number of TX ports in your design.
	[MEM_PAIRING_SIZE]	Sets the amount of R/W memory the pairing data will occupy.
	[CAPABLE_BYPASS_TIME]	(HDMI) Sets the maximum amount of time the ESM will enable low value content after a capability check before switching back to a fixed pattern output. See HLC_HDCPTX_SetCapability in the API guide.
	[LVC_TIMEOUT]	(HDMI) Sets the maximum amount of time the ESM will enable low value content without a capability check. See HLC_HDCPTX_EnableLowValueContent in the API guide.
	[LVC_EXPIRED_CNT]	(HDMI) Sets the maximum number of LVC timeouts permitted.

The [CEE_BSOD] is a 32 bit decimal value which parameter represents fixed data output on the TMDS data bus if the ESM encounters an authentication issue or detects attempts have been made to tamper with it. The value is only relevant for ports configured for HDMI. This 32 bit value is output as follows:

Table 26-8 ESM BSOD Output Mapping

BSOD Bit Positions	HDMI Controller TMDS Data Channel
[7:0]	O_tmds_ch0 [7:0]
[15:8]	O_tmds_ch1 [7:0]
[23:16]	O_tmds_ch2 [7:0]
[32:24]	Not used

26.6.5 HDCP Key Tools

This tool (HDCP keys) is used to create a DCP key data file, which is required to build the encrypted DCP data blob needed for creating the encrypted ESM firmware. The tool reads a configuration file that contains the RX or TX key information from DCP in clear text and outputs a structured data file for the configuration interface tool to encrypt with the appropriate secret keys.

The tools can also accept the DCP published key files themselves.

26.6.6 AIC Tool

The tool is used to create the encrypted ESM firmware. To build the encrypted firmware, you must first create the data files for the DCP keys and the configuration. These files, along with an input configuration file for this tool are used to build an image that can be used by the ESM. In addition to specifying the Platform and Device Unique Keys in the configuration file, there are additional keys that also must be specified as noted below.

Content Randomization

There are two separate values in the firmware.aic file, IK and IVc (128 bits and 96 bits respectively), which you must randomly generate to create a new encrypted ESM firmware image. Failure to do this puts secret data in the ESM firmware at risk of being compromised.

26.6.7 Log Data Extraction

The logging information from the ESM is output in a proprietary format. This tool is used to produce readable output of captured logging data content.

The Host Library contains a core library component which includes all the functions necessary to use the ESM. The library is built using portable C code and uses various abstraction functions to allow for migration to different platforms. Before using the ESM in your system you must properly implement the abstraction components specific to your platform.

There are two distinct abstraction components used by the Host Library, the System Abstraction Layer and the Host Library Driver (HLD) component. The System Abstraction Layer (or Common Component) defines system level functions used by the Host Library, such as malloc, memcpy, etc.

These functions are linked into the Host Library when it is built.

The Host Library Driver (HLD) component establishes a communication between the library and the physical ESM hardware, including managing the memory required for the ESM Image and the read/write area. This is a run-time plug-in module that is defined in your application and specified as a parameter to the ESM initialization function.

The figure below illustrates the abstraction components used by the Host Library package. This figure demonstrates one example where there are three separate ESMs in the system, requiring (typically) three separate HLD instantiations.consult the ESM Host Library API guide for more details on the HLD implementation.

26.6.8 Host Library

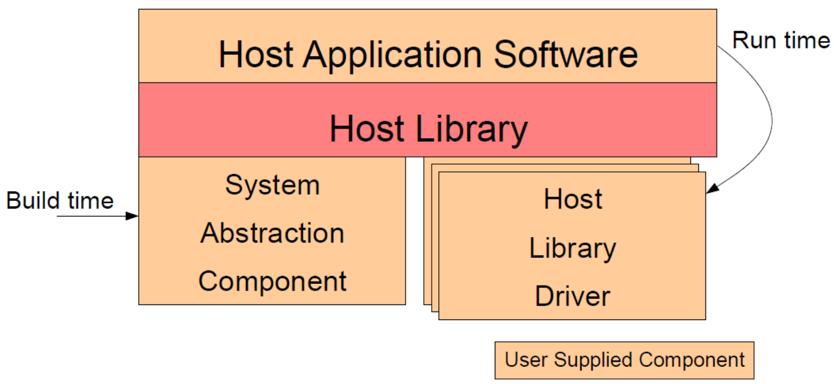

Fig. 26-8 Host Library Layers

The Host Library provides a number of sample applications using the ESM with the library. The applications demonstrate using the library in a User Space Linux application:

- Repeater/Converter (Linux) [Planned in later releases – not currently available]
- Transmitter (Linux)

All the sample applications demonstrate API usage, loading the ESM firmware, and running a specific ESM application.
The sample applications provided as a Linux User Space application communicate to the ESM hardware through a Linux Kernel driver which is implemented as a Host Library Driver (HLD) plug-in.

```
elliptic
├── doc             Host Library Documentation
├── host_library    Host Library source code and includes
└── samples         Sample applications and driver applications
```

Fig. 26-9 Development Tree Overview

Transmitter
There is a sample transmitter applications provided in the samples folder:
HDCP_TX.c is a Linux based example and utilizes file IO and threads.
Linux OS
Sample applications are targeted for a Linux User Space application environment. In order to use them a custom kernel driver is used and the HLD plug-in for the host library was made to call IOCTLs which mapped to the appropriate interfaces in the kernel driver module to access the ESM.
To build for this platform run the makefile from the esm_host_lib folder:

    make samples

The implementation of the platform specific APIs (for the Linux example) are in the following files:
./host_library/cal/system/sample_platform/elliptic_common.c
./host_library/cal/system/sample_platform/elliptic_log.c
./host_library/include/elliptic_platform_specific_system_type.h
./host_library/include/elliptic_platform_specific_system.h
You can change these implementations as needed for your specific platform.
Debugging Suggestions
The host library driver interface is relatively straightforward to implement as the host library itself takes care of the required protocols to communicate with the ESM. The detailed HPI interface and command protocols are considered proprietary information, however, the information presented below can be followed if you are having difficulty getting the ESM operating in your environment.

26.6.9 TRNG operation

The TRNG is a self-seeding True Random Number Generator. It generates random data that is statistically equivalent to a uniformly distributed random data stream. The circuit includes a seed generator which creates a non-deterministic random value to seed an internal Pseudo Random Number Generator (PRNG). The output is the random number.
The TRNG generates random data that is statistically equivalent to a uniformly distributed random data stream. The circuit includes an oscillating rings based seed generator which creates non-deterministic random noise to seed a noise whitener circuit. The output of the noise whitener is a random number. The TRNG block is shown in the figure below.

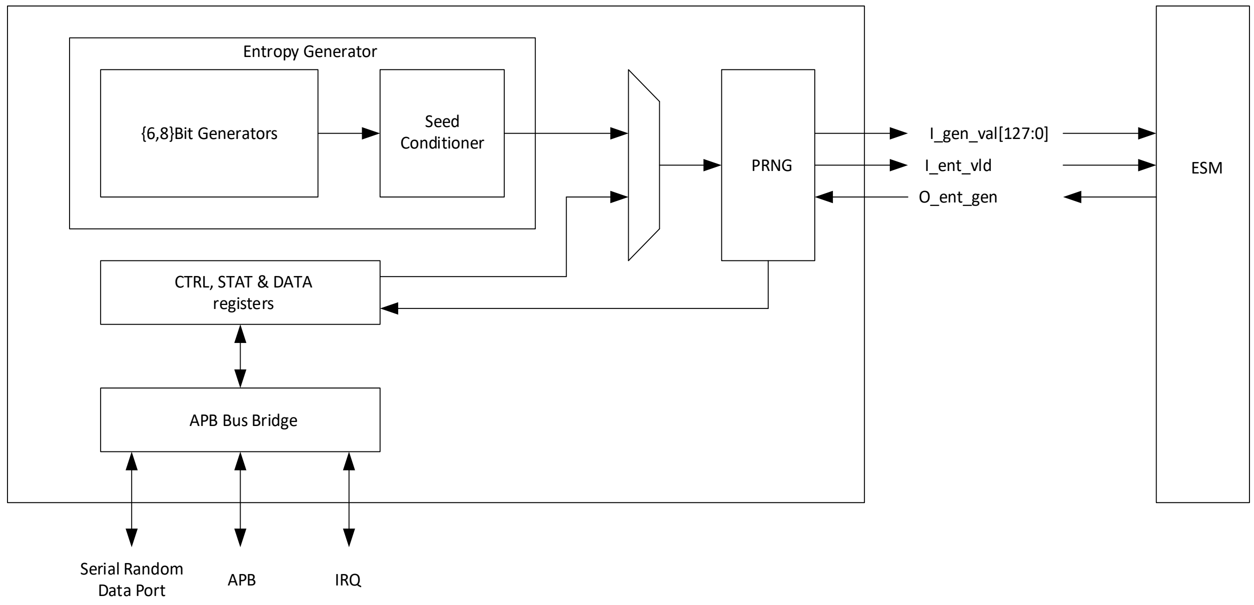

Fig. 26-10 Simplified block diagram of TRNG

(1)Reseed operations

The TRNG can be reseeded using its internal random seed generator or through a host-supplied nonce seed.

Whenever any of the reseed operations is executed, the reseed reminder alarm counters are automatically reinitialized from their respective reload registers (if they are non-zero). In addition, the O_ctrl_reminder alarm signal is also cleared as well. There are different ways to initiate the random seed.

Table 26-9 Polling mode cmd for random seed initial operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0[2:0]	cmd	0x0	0x2	start the random reseed sequence running
Wait 0x14[1]bit is 1'b1. This bit is seed_done indication signal.				
0x14[1]	seed_done	0x0	0x1	Configure to acknowledge and clear the flag

The second mode for random seed initial operation is interrupt mode.

Table 26-10 Interrupt mode cmd for random seed initial operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x10[31]	glbl_en	0x0	0x1	Configure global interrupt enable
0x10[1]	seed_done_en	0x0	0x1	Enable seed_done interrupt
0x0[2:0]	cmd	0x0	0x2	start the random reseed sequence running
Wait 0x14[1]bit is 1'b1. This bit is seed_done indication signal.				
0x14[1]	seed_done	0x0	0x1	Configure to acknowledge and clear the flag

The third mode for random seed initial operation is through I_ctrl_reseed port.

Table 26-11 I_ctrl_reseed port for random seed initial operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0xfd5a8000+ 0x8[9]	I_ctrl_seed	0x0	0x1	start the random reseed sequence running

SFR Address	SFR Name	Default Value	Setting Value	Description
Read the O_ctrl_reseeding(0xfd5a8000+0x34[22]), if it is 1'b1, it indicates that the TRNG has completed the reseeding operation.				

The I_ctrl_reseed port is primarily intended to be used in instantiations where there is no host register interface to manage the internal TRNG workings. It is not typically recommended that both the I_ctrl_reseed port and the host register interface be used in the same design.
The host must wait until any on-going rand_generation operation has completed before issuing a nonce seed operation. This can be monitored through the STAT register. In detail, execute the following sequence to load a nonce seed.

Table 26-12 TRNG nonce reseed operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0xc[2]	nonce_mode	0x0	0x1	Set the reseed mode to nonce
Wait 0x4[2]bit is 1'b1. This bit is nonce_mode indication signal.				
0x40[31:0]	seed0	0x0		Configure seed0 register
0x44[31:0]	seed1	0x0		Configure seed1 register
0x48[31:0]	seed2	0x0		Configure seed2 register
0x4c[31:0]	seed3	0x0		Configure seed3 register
0x50[31:0]	seed4	0x0		Configure seed4 register
0x54[31:0]	seed5	0x0		Configure seed5 register
0x58[31:0]	seed6	0x0		Configure seed6 register
0x5c[31:0]	seed7	0x0		Configure seed7 register
0x0[2:0]	cmd	0x0	0x3	Execute the load nonce sequence
0xc[2]	nonce_mode	0x0	0x0	Configure to return the core to normal operation

(2)Random number generation operations
To request the TRNG to generate a new random number, the host must write a 1 to the CMD field in the CTRL register(0x0[2:0]). The TRNG must have been seeded by one of the seed mechanisms before executing these sequences.
This is polling mode for random number generation operations.

Table 26-13 Polling mode for random number generation operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0[2:0]	cmd	0x0	0x1	start the random number generation process
Wait 0x14[0]bit is 1'b1. This bit is rand_rdy signal, it indicates has finished random number generation.				
0x14[0]	rand_rdy	0x0	0x1	Configure to acknowledge and clear the flag
Read the random data from RAND0 (0x20) through RAND3 (0x2c).				

This is interrupt mode for random number generation operations.

Table 26-14 Interrupt mode for random number generation operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x10[31]	glbl_en	0x0	0x1	Configure global interrupt enable

SFR Address	SFR Name	Default Value	Setting Value	Description
0x10[0]	rand_rdy_en	0x0	0x1	Configure rand_rdy interrupt enable
0x0[2:0]	cmd	0x0	0x1	start the random number generation process
Wait 0x14[0]bit is 1'b1. This bit is rand_rdy signal, it indicates has finish random number generation.				
0x14[0]	rand_rdy	0x0	0x1	Configure to acknowledge and clear the flag
Read the random data from RAND0 (0x20) through RAND3(0x2c).				

(3)ESM cmd for generating new random data operations
The cmd of ESM for generating a new random data I_gen_val[127:0] is shown below.
step1.clear all the irq state

```
address =
ELP_ESM_ENT_ADDR_BASE(0x80020900)+ELP_PROT_ENT_IRQ_STAT_REG(0x4);
wr_data = 0xffffffff;
_mailbox_poke(address, wr_data);
```

step2. set up irq enable

```
address = ELP_ESM_ENT_ADDR_BASE(0x80020900)+ELP_PROT_ENT_IRQ_EN_REG(0x0);
wr_data = 0x1;
_mailbox_poke(address, wr_data);
```

step3. register the IRQ with the firmware

```
irq_bit_num = TROOT_TB_CMD_CPU_ENT_IRQ;//22
address=
ELP_ESM_ENT_ADDR_BASE(0x80020900) + ELP_PROT_ENT_IRQ_STAT_REG(0x4);
_mailbox_put(TROOT_TB_CMD_IRQ_REGISTER, irq_bit_num, address);
_mailbox_get(TROOT_TB_CMD_IRQ_REGISTER_RESP, 0, 0, chk_data, chk1_data, 1, 1);
//TROOT_TB_CMD_IRQ_REGISTER = 131
//TROOT_TB_CMD_IRQ_REGISTER_RESP = 131
```

step4. make sure we can request a nonce

```
address = ELP_ESM_ENT_ADDR_BASE(0x80020900)+ELP_PROT_ENT_STAT_REG(0x14);
chk_data = 0x1;
_mailbox_peek(address, chk_data, rd_data, 1);
```

step5. request the nonce

```
address = ELP_ESM_ENT_ADDR_BASE(0x80020900)+ELP_PROT_ENT_CTRL_REG(0x10);
wr_data = 0x1;
_mailbox_poke(address, wr_data);
```

Chapter 27 HDMI TX/eDP Combo PHY

27.1 Overview

This chapter describes an overview of HDMI TX/eDP Combo PHY. HDMI TX/eDP Combo PHY is a PHY hard macro to support HDMI TX and eDP interfaces. Combo transmit-PHY for HDMI2.1 TMDS Link, FRL Link, eDP Link.Maximum data rate of 12Gbps (HDMI2.1 FRL) and minimum data rate of 250Mbps (HDMI2.1 TMDS). For the convenience of writing, we also name HDMI TX/eDP Combo PHY as HDPTX PHY.

- HDMI2.1
  - AC coupled voltage mode drivers for HDMI2.1 TMDS links
  - Supports all the data rates in FRL: 3, 6, 8, 10 and 12Gbps
  - Supports Single Ref-clock input and multiple TMDS/Pixel clock frequencies
  - Supports Pixel clock input (25MHz to 594MHz) with TMDS multiplication
  - Supports 3 TAP FFE support for FRL mode
  - Single ended and common mode ARC support
  - Supports 20/40 bits parallel data interface for HDMI 2.0 operation
  - Supports 18/36 bits parallel data interface for HDMI 2.1 operation
  - Supports symbol clock output with configurable divider option for link operation
  - Supports Pixel clock output for link operation
  - Supports 4 lane Fixed Rate Link operation with 3Gbps, 6Gbps, 8Gbps, 10Gbps and 12Gbps rates
  - Supports 24MHz reference clock
  - Supports channel swap function for HDMI 2.0 back compatible operation
- eDP
  - Supports RBR (1.62Gbps per lane), HBR (2.7Gbps per lane) and HBR2 (5.4Gbps per lane) data rates
  - Supports training table with swing-level 0-3 and pre-emphasis-level 0-3
  - Supports AUX function as required by DP PHY implementing TX main link
  - Supports x1, x2 and x4 configurations
  - Supports 24MHz reference clock

27.2 Block Diagram

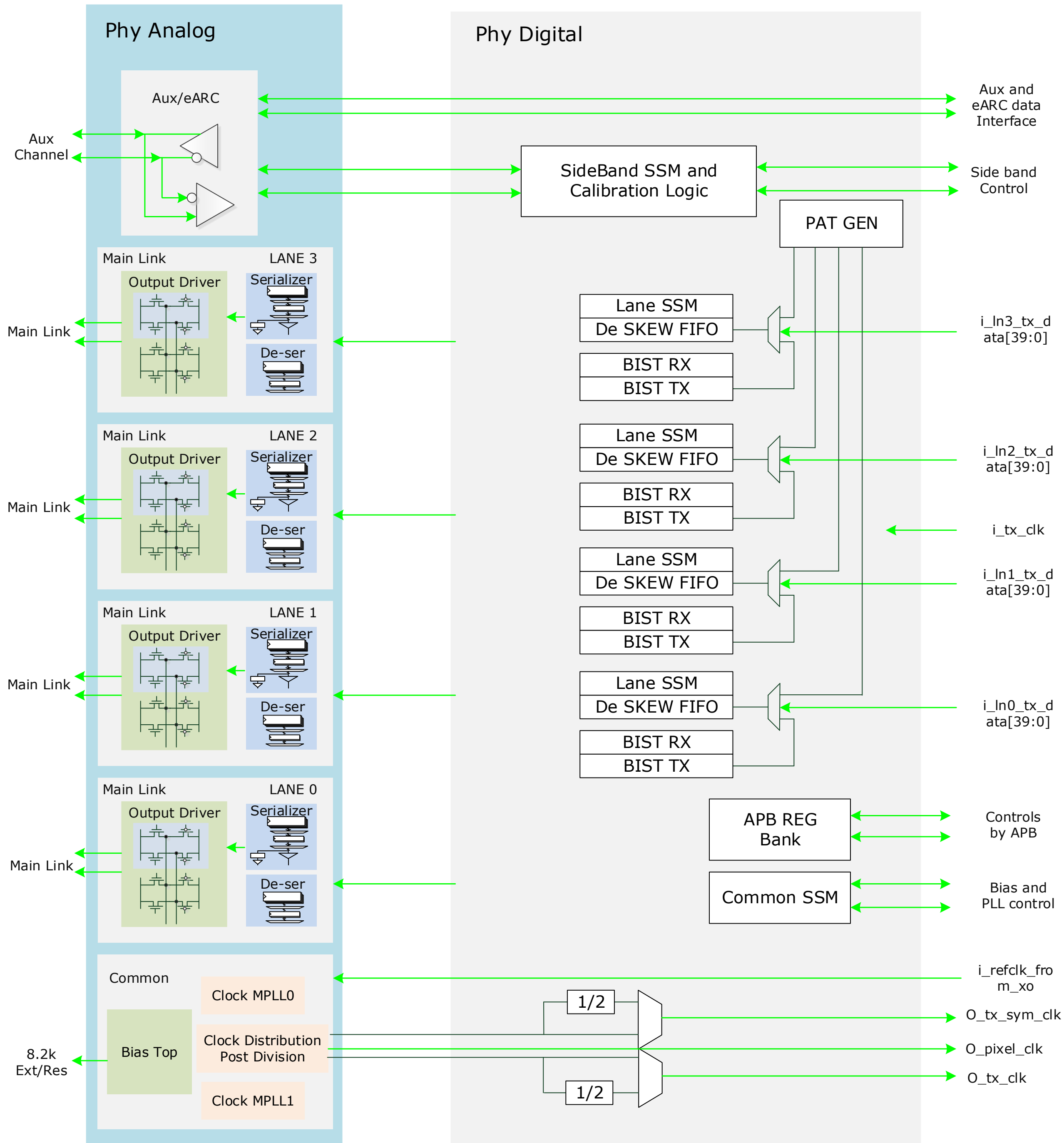

Fig. 27-1 Block diagram of HDMI TX/eDP Combo PHY

Above figure shows the block diagram of HDMI TX/eDP Combo PHY. It comprises of one CMN, four lanes of transmitter, one sideband that supports AUX channel for eDP and one PHY digital. The common block consists of one Band Gap, one Bias generation block and one PLL.

27.3 Function Description

27.3.1 PHY Analog

HDMI TX/eDP Combo PHY comprises of a PHY analog and PHY digital. The PHY consists of: One CMN block, a sideband block to support AUX for DP and ARC HDMI and Four Transmit lanes.

27.3.1.1 CMN

The CMN consists of a band-gap reference (BGR), bias generator and PLL. The BGR circuit generates high-accuracy reference voltage of 820mV across PVT variation. A bias generator makes two kinds of current, external-and internal-resistor (RMRES)-referred current, and these currents are distributed to each block in CMN and lanes. The external resistor-referred (REXT) current is generated using an 8.2KΩ resistor which is connected between the rext

pad and ground outside the chip. On the other hand, the internal resistor-referred current is generated using internally integrated replica resistor to compensate resistance error across PVT variation. The PLL in the CMN synthesizes high-speed clock, which is used for TX serializer, from a reference clock. The reference clock can be selected from three clock sources; crystal oscillator, SoC PLL's output reference clock.
The following are the main features of the PLL:
Supports LC PLL for 5 ~ 6GHz clock.
Supports sigma-delta modulated fractional divider.
Automatic Frequency Calibrated (AFC) oscillator setting for the desired frequency of operation Programmable charge pump current and loop filter resistance allowing for wide range of programmable loop bandwidth and peaking.

27.3.1.2 TRANSMITTER

The TX comprises serializer, driver, common-mode (CM). The driver generates baud-rate voltage waveform on TX output pads, ln01/1/2/3_txdp/n, with 3-tap FIR filter function. The main driver has hybrid structure, by combining voltage-and current-mode driver in parallel, to achieve both a small power consumption and large voltage swing. The voltage-mode driver is activated in default, but the current mode driver is optional to improve the TX output swing.
The driver also supports 3-tap FIR filter to suppress one pre and one post-cursor according to the HDMI2.1 FRL specification. The driver has the resolution of 1/36 in controlling amplitude and filter ratio, and maximum ratio of pre-shoot and de-emphasis are 15/36 and 8/36, respectively.

27.3.1.3 Side Band block

The side block consists of a termination block, a push-pull voltage buffer, a lower speed receiver and a PWM receiver. These blocks work in AC coupled AUX-RXTX.

27.3.1.3.1 Push Pull Voltage buffer (AUX Driver)

A push voltage buffer has been used to have very slow slew (5 to 30ns) on the line during transmission. The transmitter can be configured to drive wither common mode data or differential mode data on the line. During reception mode the buffer hold the line in common mode. This driver is also responsible for boundary scan driver.

27.3.1.3.2 Termination

The side-band is always terminated to 50 Ohms internally. The common mode of the termination is set by the push-pull voltage buffer described above. The termination block is designed such that same calibration code of main link transmitter can be used.

27.3.1.3.3 A lower speed receiver (AUX Receiver)

The lower speed receiver is responsible to receive 1Mbps differential AUX data. In ARC mode this listens to only sbdp line. This receiver has a pad interface which practically works as differential line to common mode voltage generation just by adding the voltage waveforms at sbdp and sbdn line. The following figure depicts the usage of pad interface and data multiplexing.

27.3.2 HDMI/eDP Combo PHY Source Power States

This section describes the PHY power states. It describes the four power states for PHY. ON state is the normal operational state or mission mode for the PHY. The allowed power state transitions are described in the following figure. For all power state transitions, ensure that the MAC/SoC does not initiate any operational sequence or further power state transition until the PHY indicates that the initial state transition is completed.

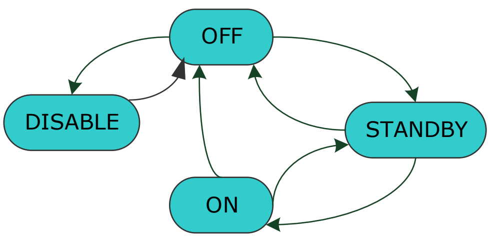

Fig. 27-2 PHY Power state transition flow diagram

Table 27-1 HDMI TX/eDP Combo PHY Power States

State	Description	Exit Latency Duration
OFF	***Reset state of PHY. All the blocks will be in power down mode.*** This is PHY reset mode but serial lines are weakly held to common mode to provide a current path during transient if SINK is connected to high voltage termination (HDMI) or board pull up (eDP) supply is coming up. Reference clock supplied to PHY may be turned off.	-
DISABLE	***Low power saving mode with low recovery time latency*** This is lowest power modes of PHY-Analog. When reduced or no lanes are used by SoC by APB configuration the PHY-Analog can be set to.	-
STANDBY	***Clock ready state*** The common block is brought and calibration for all required analog blocks are completed in this state. Some LANES can be in DISABLE state. Remaining active LANES are waiting for the LINK Layer/SoC to send parallel data. All the interface clock is ready and o_phy_rdy, o_phy_clk_rdy and o_sb_rdy is asserted high. The serial lines are held in common mode. This state is very important for the AC coupled system to charge the common mode of the line.	>200us
ON	***Normal operation mode***	-

27.4 Register Description

27.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

27.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
HDPTXPHY_CMN_REG0000	0x0000	W	0x00000004	CMN Register
HDPTXPHY_CMN_REG0008	0x0020	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0009	0x0024	W	0x0000000C	CMN Register
HDPTXPHY_CMN_REG000A	0x0028	W	0x00000083	CMN Register
HDPTXPHY_CMN_REG000B	0x002C	W	0x00000006	CMN Register
HDPTXPHY_CMN_REG0020	0x0080	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0021	0x0084	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0025	0x0094	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0028	0x00A0	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG002D	0x00B4	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG002E	0x00B8	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG002F	0x00BC	W	0x00000004	CMN Register
HDPTXPHY_CMN_REG003C	0x00F0	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG003D	0x00F4	W	0x00000040	CMN Register
HDPTXPHY_CMN_REG004E	0x0138	W	0x00000034	CMN Register
HDPTXPHY_CMN_REG0051	0x0144	W	0x0000007D	CMN Register
HDPTXPHY_CMN_REG0053	0x014C	W	0x0000007D	CMN Register
HDPTXPHY_CMN_REG0055	0x0154	W	0x0000007D	CMN Register

Name	Offset	Size	Reset Value	Description
HDPTXPHY_CMN_REG005A	0x0168	W	0x00000033	CMN Register
HDPTXPHY_CMN_REG005C	0x0170	W	0x00000025	CMN Register
HDPTXPHY_CMN_REG005E	0x0178	W	0x0000004F	CMN Register
HDPTXPHY_CMN_REG0060	0x0180	W	0x0000004E	CMN Register
HDPTXPHY_CMN_REG0063	0x018C	W	0x0000004E	CMN Register
HDPTXPHY_CMN_REG0064	0x0190	W	0x0000000F	CMN Register
HDPTXPHY_CMN_REG0065	0x0194	W	0x00000014	CMN Register
HDPTXPHY_CMN_REG0069	0x01A4	W	0x00000002	CMN Register
HDPTXPHY_CMN_REG006C	0x01B0	W	0x00000013	CMN Register
HDPTXPHY_CMN_REG0070	0x01C0	W	0x00000018	CMN Register
HDPTXPHY_CMN_REG0074	0x01D0	W	0x00000005	CMN Register
HDPTXPHY_CMN_REG0081	0x0204	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0082	0x0208	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0083	0x020C	W	0x00000024	CMN Register
HDPTXPHY_CMN_REG0084	0x0210	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0085	0x0214	W	0x00000002	CMN Register
HDPTXPHY_CMN_REG0086	0x0218	W	0x00000010	CMN Register
HDPTXPHY_CMN_REG0087	0x021C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0089	0x0224	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0095	0x0254	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0097	0x025C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG0099	0x0264	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009A	0x0268	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009B	0x026C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009E	0x0278	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG009F	0x027C	W	0x00000000	CMN Register
HDPTXPHY_CMN_REG00A0	0x0280	W	0x00000000	CMN Register
HDPTXPHY_SB_REG0102	0x0408	W	0x00000003	Sideband Register
HDPTXPHY_SB_REG0103	0x040C	W	0x00000018	Sideband Register
HDPTXPHY_SB_REG0104	0x0410	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0105	0x0414	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0106	0x0418	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0109	0x0424	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG010D	0x0434	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG010F	0x043C	W	0x00000001	Sideband Register
HDPTXPHY_SB_REG0110	0x0440	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0113	0x044C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0114	0x0450	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0115	0x0454	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0116	0x0458	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0117	0x045C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0118	0x0460	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0119	0x0464	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011A	0x0468	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011B	0x046C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011C	0x0470	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011D	0x0474	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011E	0x0478	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG011F	0x047C	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0120	0x0480	W	0x00000000	Sideband Register
HDPTXPHY_SB_REG0123	0x048C	W	0x00000000	Sideband Register

Name	Offset	Size	Reset Value	Description
HDPTXPHY_INTOP_REG0200	0x0800	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0201	0x0804	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0203	0x080C	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0204	0x0810	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0205	0x0814	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0206	0x0818	W	0x00000000	Lane Top Register
HDPTXPHY_INTOP_REG0207	0x081C	W	0x00000000	Lane Top Register
HDPTXPHY_LANE_REG0303	0x0C0C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0307	0x0C1C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030A	0x0C28	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030B	0x0C2C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030C	0x0C30	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030D	0x0C34	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030E	0x0C38	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG030F	0x0C3C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0310	0x0C40	W	0x00000002	Lane 0 Register
HDPTXPHY_LANE_REG0311	0x0C44	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0312	0x0C48	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG0316	0x0C58	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG031B	0x0C6C	W	0x00000000	Lane 0 Register
HDPTXPHY_LANE_REG031F	0x0C7C	W	0x00000014	Lane 0 Register
HDPTXPHY_LANE_REG0320	0x0C80	W	0x000000A0	Lane 0 Register
HDPTXPHY_LANE_REG0403	0x100C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0407	0x101C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040A	0x1028	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040B	0x102C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040C	0x1030	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040D	0x1034	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG040E	0x1038	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0410	0x1040	W	0x00000002	Lane 1 Register
HDPTXPHY_LANE_REG0411	0x1044	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0412	0x1048	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG0416	0x1058	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG041B	0x106C	W	0x00000000	Lane 1 Register
HDPTXPHY_LANE_REG041F	0x107C	W	0x00000014	Lane 1 Register
HDPTXPHY_LANE_REG0503	0x140C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG0507	0x141C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050A	0x1428	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050B	0x142C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050C	0x1430	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050D	0x1434	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG050E	0x1438	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG0510	0x1440	W	0x00000002	Lane 2 Register
HDPTXPHY_LANE_REG0511	0x1444	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG0512	0x1448	W	0x00000000	Lane 2 Register

Name	Offset	Size	Reset Value	Description
HDPTXPHY_LANE_REG0516	0x1458	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG051B	0x146C	W	0x00000000	Lane 2 Register
HDPTXPHY_LANE_REG051F	0x147C	W	0x00000014	Lane 2 Register
HDPTXPHY_LANE_REG0520	0x1480	W	0x000000A0	Lane 2 Register
HDPTXPHY_LANE_REG0521	0x1484	W	0x00000014	Lane 2 Register
HDPTXPHY_LANE_REG0603	0x180C	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0607	0x181C	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060A	0x1828	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060B	0x182C	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060C	0x1830	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060D	0x1834	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG060E	0x1838	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0610	0x1840	W	0x00000002	Lane 3 Register
HDPTXPHY_LANE_REG0611	0x1844	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0612	0x1848	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG0616	0x1858	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG061B	0x186C	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG061E	0x1878	W	0x00000000	Lane 3 Register
HDPTXPHY_LANE_REG061F	0x187C	W	0x00000014	Lane 3 Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

27.4.3 Detail Registers Description

HDPTXPHY_CMN_REG0000

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_bgr_en Override enable for bgr_en.
6	RW	0x0	bgr_en BGR enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_bgr_lpf_bypass Override enable for bgr_lpf_bypass.
4	RW	0x0	bgr_lpf_bypass BGR LPF bypass to reduce BGR settle time 1'b0: LPF enable 1'b1: LPF bypass
3:2	RW	0x1	ana_bgr_820m_sel BGR 820mV selection (for current bias) 2'b00: 780mV 2'b01: 820mV 2'b10: 860mV 2'b11: 900mV
1	RW	0x0	ana_bgr_clk_en BGR chopper clock enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ana_bgr_ladder_en BGR output voltage selection 1'b0: BGR output 1'b1: Resistor ladder output

HDPTXPHY_CMN_REG0008

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_lcpll_en Override enable for lcpll_en.
6	RW	0x0	lcpll_en LC PLL enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ana_lcpll_bea_con_clk_out_en Enable LCPLL beacon clock output
4	RW	0x0	ana_lcpll_lcv_co_mode_en Enable LCVCO mode
3	RW	0x0	ovrd_lcpll_afc_init_rstn Override enable for lcpll_afc_init_rstn
2	RW	0x0	lcpll_afc_init_rstn PLL AFC initial reset. When initial reset is asserted, the previous AFC result is reset. When initial reset is released, AFC starts from the initial AFC code given in i_rx_cdr_afc_sel_logic [3:0]. 1'b0: Reset 1'b1: Released
1	RW	0x0	ovrd_lcpll_afc_rstn Override enable for lcpll_afc_rstn
0	RW	0x0	lcpll_afc_rstn PLL AFC reset. When AFC reset is asserted, the previous AFC result is held. When AFC reset is released, AFC starts from the previous AFC code stored in internal memory. 1'b0: Reset 1'b1: Released

HDPTXPHY_CMN_REG0009

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_lcpll_pi_afc_clk_div2_en PLL AFC clock frequency selection 1'b0: fVCO 1'b1: fVCO/2
4	RW	0x0	ana_lcpll_afc_bsel PLL AFC code manual selection enables 1'b0: AFC result 1'b1: Manual selection
3	RW	0x1	ana_lcpll_afc_en PLL AFC enable; if enabled, VCO frequency is automatically calibrated. If disabled, VCO starts to oscillate with fixed AFC code of i_pll_man_bsel_m and _l. 1'b0: Disable 1'b1: Enable
2	RW	0x1	ana_lcpll_afc_from_pre_code PLL AFC option in restart case 1'b0: Restart from initial AFC code 1'b1: Restart from previous AFC code

Bit	Attr	Reset Value	Description
1:0	RW	0x0	ana_lcpll_afc_man_bsel_l Manual PLL AFC code selection (LSB)

HDPTXPHY_CMN_REG000A
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x8	ana_lcpll_afc_man_bsel_m Manual PLL AFC code selection (MSB)
3:0	RW	0x3	ana_lcpll_afc_stb_num Number of reference clock cycle to check VCO stabilization during PLL AFC start

HDPTXPHY_CMN_REG000B
Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:1	RW	0x3	ana_lcpll_afc_tol_num PLL VCO stabilization tolerance; VCO is considered as settled-down if |counter difference|<i_pll_afc_tol during i_pll_afc_stb_num
0	RW	0x0	ana_lcpll_afc_vci_force PLL control voltage force for open-loop test purpose 1'b0: Released 1'b1: Forced

HDPTXPHY_CMN_REG0020
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ana_lcpll_pms_mdiv PLL main divider setting Divider value = Setting code

HDPTXPHY_CMN_REG0021
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ana_lcpll_pms_mdiv_afc PLL main divider setting for AFC counter Divider value = Setting code

HDPTXPHY_CMN_REG0025
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ana_lcpll_iqdiv_bypass VCO clock bypass IQ divider enable.
5	RW	0x0	ovrd_lcpll_pms_iqdiv_rstn Override enable for lcpll_pms_iqdiv_rstn
4	RW	0x0	lcpll_pms_iqdiv_rstn IQ divider resetn
3	RW	0x0	ovrd_lcpll_ref_chopper_clk_div_rstn Override enable for lcpll_ref_chopper_clk_div_rstn

Bit	Attr	Reset Value	Description
2	RW	0x0	lcpll_ref_chopper_clk_div_rstn Chopper clk divider reset 1'b0: Reset 1'b1: Released
1:0	RW	0x0	ana_lcpll_ref_bypass_clk_sel PLL Bypass clock selection 2'b00: XO 2'b01: IO 2'b10: PIXEL or LC_OUT_CLK 2'b11: System PLL clock

HDPTXPHY_CMN_REG0028

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ovrd_lcpll_sdm_rstn ovrd_lcpll_sdm_rstn
3	RW	0x0	lcpll_sdm_rstn PLL SDM reset 1'b0: Reset 1'b1: Released
2	RW	0x0	ana_lcpll_sdc_fractional_en Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
1	RW	0x0	ovrd_lcpll_sdc_rstn Override enable for lcpll_sdc_rstn
0	RW	0x0	lcpll_sdc_rstn PLL SDM clock generation (SDC) reset 1'b0: Reset 1'b1: Release

HDPTXPHY_CMN_REG002D

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ana_lcpll_sdm_ph_num_sel PLL PI input clock phase number 1'b0: 8-phase 1'b1: 4-phase
5:4	RW	0x0	ana_lcpll_sdm_pi_step PLL phase interpolstor step 2'b00: 1-step (16-phase) 2'b01: 2-step (8-phase) 2'b1x: 0.5-step
3:1	RW	0x0	ana_lcpll_sdc_n PLL SDC divide-ratio selection (MC_val=0 N, MC_val=1 N-1) 3'b000: /4/3 3'b001: /5/4 3'b010: /6/5 3'b100: /7/6 3'b101: /8/7 3'b110: /9/8

Bit	Attr	Reset Value	Description
0	RW	0x0	ana_lcpll_sdc_n2 PLL SDC divide-ratio selection 1'b0: No additional/2 1'b1: Additional/2

HDPTXPHY_CMN_REG002E

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	ana_lcpll_sdc_numerator Numerator of SDC (Max 65)

HDPTXPHY_CMN_REG002F

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x01	ana_lcpll_sdc_denominator Denominator of SDC (Max 65)
1	RW	0x0	ovrd_lcpll_sdc_ndiv_rstn Override enable for lcpll_sdc_ndiv_rstn
0	RW	0x0	lcpll_sdc_ndiv_rstn SDC NDIV Resetn.

HDPTXPHY_CMN_REG003C

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ana_lcpll_reserved PLL Reserved pins

HDPTXPHY_CMN_REG003D

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ropll_en Override enable for ropll_en.
6	RW	0x1	ropll_en RO PLL enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ana_ropll_beacon_clk_out_en Enable ROPLL beacon clock output.
4	RW	0x0	ana_ropll_lcvco_mode_en Enable LCVCO mode.
3	RW	0x0	ovrd_ropll_afc_init_rstn Override enable for ropll_afc_init_rstn.
2	RW	0x0	ropll_afc_init_rstn PLL AFC initial reset. When initial reset is asserted, the previous AFC result is reset. When initial reset is released. AFC starts from the initial AFC code given in i_rx_cdr_afc_sel_logic[3:0]. 1'b0: Reset 1'b1: Released
1	RW	0x0	ovrd_ropll_afc_rstn Override enable for ropll_afc_rstn.

Bit	Attr	Reset Value	Description
0	RW	0x0	ropll_afc_rstn PLL AFC reset. When AFC reset is asserted, the previous AFC result is held. When AFC reset is released, AFC starts from the previous AFC code stored in internal memory. 1'b0: Reset 1'b1: Released

HDPTXPHY_CMN_REG004E

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ana_ropll_fld_non_continuous_mode Check frequency lock detection of PLL 1'b0: Once 1'b1: Continuously
6	RW	0x0	ana_ropll_fld_slow_bypass PLL slow frequency lock detection bypass 1'b0: No bypass 1'b1: Bypass
5	RW	0x1	ana_ropll_pi_en PLL phase interpolator enable 1'b0: Disable 1'b1: Enable
4:1	RW	0xa	ana_ropll_pi_str PLL phase interpolator input buffer strength control for Gen3 and Gen4 (for 8GHz VCO) 4'b0000: Min. strength .... 4'b1111: Max. strength
0	RW	0x0	ana_ropll_100m_clk_en Enable 100M clock.

HDPTXPHY_CMN_REG0051

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x7d	ropll_pms_mdiv_rbr [rbr] PLL main divider setting Divider value = Setting code

HDPTXPHY_CMN_REG0053

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x7d	ropll_pms_mdiv_hbr2 [hbr2] PLL main divider setting Divider value = Setting code

HDPTXPHY_CMN_REG0055

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x7d	ropll_pms_mdiv_afc_rbr [rbr] PLL main divider setting for AFC counter Divider value = Setting code

HDPTXPHY_CMN_REG005A
Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x3	ropll_pms_sdiv_rbr [rbr] PLL post divider setting (N-1, except /7) 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8
3:0	RW	0x3	ropll_pms_sdiv_hbr [hbr]PLL post divider setting (N-1, except /7) 3'b000: /1 3'b001: /2 3'b010: /3 3'b011: /4 3'b100: /5 3'b101: /6 3'b110: X 3'b111: /8

HDPTXPHY_CMN_REG005C
Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ana_ropll_iqdiv_bypass VCO clock bypass IQ divider enable.
6	RW	0x0	ovrd_ropll_pms_iqdiv_rstn Override enable for ropll_pms_iqdiv_rstn.
5	RW	0x1	ropll_pms_iqdiv_rstn IO divider resetn.
4:3	RW	0x0	ana_ropll_ref_bypass_clk_sel PLL Bypass clock selection. 2'b00: X0 2'b01: IO 2'b10: PIXEL or LC_OUT_CLK 2'b11: System PLL clock
2	RW	0x1	ana_ropll_ref_chopper_clk_en Chopper clk enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	ovrd_ropll_ref_chopper_clk_div_rstn Override enable for ropll_ref_chopper_clk_div_rstn.
0	RW	0x1	ropll_ref_chopper_clk_div_rstn Chopper clk divider reset 1'b0: Reset 1'b1: Released

HDPTXPHY_CMN_REG005E

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	ana_ropll_sdm_en PLL SDM enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_ropll_sdm_rstn Override enable for ropll_sdm_rstn.
4	RW	0x0	ropll_sdm_rstn PLL SDM reset 1'b0: Reset 1'b1: Released
3	RW	0x1	ropll_sdc_fractional_en_rbr [rbr]Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
2	RW	0x1	ropll_sdc_fractional_en_hbr [hbr]Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
1	RW	0x1	ropll_sdc_fractional_en_hbr2 [hbr2] Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division
0	RW	0x1	ropll_sdc_fractional_en_hbr3 [hbr3] Fractional clock divide in SDM clock generation 1'b0: Integer division 1'b1: Fractional division

HDPTXPHY_CMN_REG0060

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_sdm_denominator_rbr [rbr] Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signed i_pll_sdm_ki_pll_ssc_fm_deviationi_pll_ssc_fm_freq-14

HDPTXPHY_CMN_REG0063

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x4e	ropll_sdm_denominator_hbr3 [hbr3] Denominator of SDM (Max. 255) Constraint: i_pll_sdm_lc > |signed i_pll_sdm_ki_pll_ssc_fm_deviation - i_pll_ssc_fm_freq-1|

HDPTXPHY_CMN_REG0064

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RW	0x1	ropll_sdm_numerator_sign_rbr [rbr] Sign of SDM numerator 1'b0: Positive 1'b1: Negative
2	RW	0x1	ropll_sdm_numerator_sign_hbr [hbr]Sign of SDM numerator 1'b0: Positive 1'b1: Negative
1	RW	0x1	ropll_sdm_numerator_sign_hbr2 [hbr2] Sign of SDM numerator 1'b0: Positive 1'b1: Negative
0	RW	0x1	ropll_sdm_numerator_sign_hbr3 [hbr3] Sign of SDM numerator 1'b0: Positive 1'b1: Negative

HDPTXPHY_CMN_REG0065
Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x14	ropll_sdm_numerator_rbr [rbr] Numerator of SDM with i_pll_sdm_k_sign (-255~255).

HDPTXPHY_CMN_REG0069
Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_ropll_sdm_ph_num_sel PLL PI input clock phase number 1'b0: 8-phase 1'b1: 4-phase
4:3	RW	0x0	ana_ropll_sdm_pi_step PLL phase interpolstor step 2'b00: 1-step (16-phase) 2'b01: 2-step (8-phase) 2'b1x: 0.5-step
2:0	RW	0x2	ropll_sdc_n_rbr [rbr] PLL SDC divide-ratio selection 3'b000: /3 3'b001: /4 3'b010: /5 3'b011: /6 3'b100: /7 3'b101: /8

HDPTXPHY_CMN_REG006C
Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x13	ropll_sdc_numerator_rbr [rbr] Numerator of SDC (Max 65)

HDPTXPHY_CMN_REG0070
Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x18	ropll_sdc_denominator_rbr [rbr] Denominator of SDC (Max 65)

HDPTXPHY_CMN_REG0074

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ovrd_ropll_sdc_ndiv_rstn Override enable for ropll_sdc_ndiv_rstn
2	RW	0x1	ropll_sdc_ndiv_rstn ROPLL SDC ndiv reset
1	RW	0x0	ovrd_ropll_ssc_en Override enable for ropll_ssc_en
0	RW	0x1	ropll_ssc_en PLL SSC enable 1'b0: Disable 1'b1: Enable

HDPTXPHY_CMN_REG0081

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_pll_cd_clk_en Override enable for pll_cd_clk_en
6	RW	0x0	pll_cd_clk_en CD enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_pll_cd_tx_ser_rstn Override enable for pll_cd_tx_ser_rstn
4	RW	0x0	pll_cd_tx_ser_rstn TX_SER resetn
3	RW	0x0	ana_pll_cd_tx_ser_rate_sel NA
2	RW	0x0	ana_pll_cd_hsclk_inv CD output clock polarity inversion 1'b0: No swap 1'b1: P/N swap
1	RW	0x0	ana_pll_cd_hsclk_west_en CD driver nmos strength control N/A
0	RW	0x0	ana_pll_cd_hsclk_east_en CD driver pmos strength control N/A

HDPTXPHY_CMN_REG0082

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_pll_cd_vreg_en Override enable for pll_cd_vreg_en
6	RW	0x0	pll_cd_vreg_en Controls Regulator Enable 1'b0: Disable regulator (Bypass VDD PMOS switch turns ON) 1'b1: Regulator Enable (Bypass path disables)

Bit	Attr	Reset Value	Description
5	RW	0x0	ovrd_pll_cd_vreg_lpf_bypass Override enable for pll_cd_vreg_lpf_bypass
4	RW	0x0	pll_cd_vreg_lpf_bypass Controls Regulator input voltage reference noise reduction Low pass filter (BW <5MHz) 1'b0: Regulator reference Low pass filter Mode 1'b1: Bypass Low pass filter (Fast charging)
3:0	RW	0x0	ana_pll_cd_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_CMN_REG0083

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x1	ana_pll_cd_vreg_ictrl Regulator Opamp tail current control 2'b00: -25% 2'b01: Default 2'b10: +50% 2'b11: +100%
4	RW	0x0	ana_pll_cd_vreg_out_sel Force Bypass Regulator.Regulator and VDD is connected to Regulator node using pass gate 1'b0: Regulator mode 1'b1: Bypass
3	RW	0x0	ana_pll_cd_vreg_ref_sel Regulator Opamp Reference voltage selection 1'b0: VDD (as reference) 1'b1: VDDH Ladder as reference
2:0	RW	0x4	ana_pll_cd_vreg_ladder_sel Choose vref based on VDDH ladder tap points. For VDDH=1.8, Vref= 3'b000: 0.749 3'b001: 0.776 3'b010: 0.804 3'b011: 0.831 3'b100: 0.859 3'b101: 0.886 3'b110: 0.914 3'b111: 0.941

HDPTXPHY_CMN_REG0084

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	ovrd_pll_lcro_clk_sel Override enable for pll_lcro_clk_sel
5	RW	0x0	pll_lcro_clk_sel Slects between LC vs RO PLL clock.
4	RW	0x0	ana_pll_bist_en Enables the BIST clock path in BIST mode.
3	RW	0x0	ana_pll_cd_bistclk_west_en Enables the BIST clock path twoards Lane2 and Lane 3
2	RW	0x0	ana_pll_cd_bistclk_east_en Enables the BIST clock path twoards Lane0 and Lane 1
1:0	RW	0x0	ana_pll_bist_clk_sel Selects BIST clock among 1, IB, Q and QB phases.

HDPTXPHY_CMN_REG0085
Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_pll_sync_loss_det_en Override enable for pll_sync_loss_det_en
4	RW	0x0	pll_sync_loss_det_en Enables the sync loss detection pulse generator.
3	RW	0x0	ovrd_pll_sync_loss_det_clk_en Override enable for pll_sync_loss_det_clk_en
2	RW	0x0	pll_sync_loss_det_clk_en Enables the clock for the sync loss detection pulse generator.
1:0	RW	0x2	ana_pll_sync_loss_det_mode Slects the sync loss detection mode from the followin table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_CMN_REG0086
Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	ana_pll_pcg_postdiv_sel Same as output divider settings of the PLL
3:1	RW	0x0	ana_pll_pcg_clk_sel 3'b000: 8-bit color depth 3'b001: 10-bit color depth 3'b010: 12-bit color depth 3'b100: 16-bit color depth
0	RW	0x0	ana_pll_pcg_clk_en Enables the Pixel clock generator.

HDPTXPHY_CMN_REG0087
Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ana_pll_frl_mode_en FRL Mode enable = 1 for HDMI 2.1 mode
2	RW	0x0	ana_pll_tx_hs_clk_en Enables the DP mode symbol clock for PMA_D

Bit	Attr	Reset Value	Description
1:0	RW	0x0	ana_pll_atb_sel ATB select lines for CD.

HDPTXPHY_CMN_REG0089

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ovrd_lcpll_fine_tune_start Override enable for lcpll_fine_tune_start
4	RW	0x0	lcpll_fine_tune_start LCPLL fine tune start override value
3	RW	0x0	ovrd_ropll_fine_tune_start Override enable for ropll_fine_tune_start
2	RW	0x0	ropll_fine_tune_start ROPLL fine tune start override value
1	RW	0x0	cmn_lcpll_alone_mode LCPLL alone mode.
0	RW	0x0	cmn_timer_sel CMN timer selection

HDPTXPHY_CMN_REG0095

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:2	RW	0x0	lane_mux_sel_dp TX Lane LC/RO Clock Select Bit 0: Lane 0, ..., Bit3: Lane 3
1:0	RW	0x0	dp_tx_link_bw 2'b00: Picks PLL setting from RBR register set 2'b01: Picks PLL setting from HBR register set 2'b10: Picks PLL setting from HBR2 register set 2'b11: Picks PLL setting from HBR3 register set

HDPTXPHY_CMN_REG0097

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	aux_dtb_out_en Used to select one of the DTB signals from lane CMN and SB module to drive sbp and sbn line at top
1	RW	0x0	dig_clk_sel 1'b1: Selects the LCPLL output reference clock for refence clock of PMA digital and o_dig_ref_clk 1'b0: Selects the ROPLL output reference clock for refence clock of PMA digital and o_dig_ref_clk
0	RW	0x0	hs_clk_mask_en Unused

HDPTXPHY_CMN_REG0099

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	ssc_en Synchronize SSC enable Bit 0: LCPLL SSC Enable Bit 1: ROPLL SSC Enable
5:3	RW	0x0	vcoclk_mon_sel Tx monitor clock select 3'b000: clk/4 3'b001: clk/2 3'b100: Lane 0 read pointer clk 3'b101: Lane 1 read pointer clk 3'b110: Lane 2 read pointer clk 3'b111: Lane 3 read pointer clk
2	RW	0x0	cmn_ropll_alone_mode 1'b0: Cascaded PLL operation 1'b1: ROPLL alone operation
1:0	RW	0x0	ovrd_pcs_rate Override enable for pcs_rate

HDPTXPHY_CMN_REG009A
Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pcs_rate Not used.
5	RW	0x0	bypass_sync_loss_det Bypass sync loss detection
4:2	RW	0x0	tg_sync_loss_mon_time Programmable delay for sync
1	RW	0x0	mon_afc_code_sel Monitor AFC code
0	RW	0x0	hs_speed_sel Tx high speed clock speed select 1'b0: Scan Tx clock / 2 1'b1: Scan Tx clock

HDPTXPHY_CMN_REG009B
Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ls_speed_sel Link symbol clock select 1'b0: Link symbol clock /2 1'b1: Link symbol clock
3	RW	0x0	phy_ready Indicates the PHY is ready for transmission
2	RW	0x0	phy_clk_ready Indicates the PHY output clocks are stable
1	RW	0x0	aux_tx_data_inv Inverts auxiliary transmission data when set to 1
0	RW	0x0	aux_rx_data_inv Inverts auxiliary reception data when set to 1

HDPTXPHY_CMN_REG009E
Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	cmn_dtb_digout_sel Select one of the digout in CMN module
1	RW	0x0	ovrd_pcs_bgr_en Override enable for pcs_bgr_en RW
0	RW	0x0	pcs_bgr_en Enable Bandgap reference.

HDPTXPHY_CMN_REG009F
Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_pcs_bias_en Override enable for pcs_bias_en
6	RW	0x0	pcs_bias_en Enable biases.
5	RW	0x0	ovrd_pcs_cmn_rstn Override enable for pcs_cmn_rstn
4	RW	0x0	pcs_cmn_rstn Reset for common logics
3	RW	0x0	ovrd_pcs_init_rstn Override enable for pcs_init_rstn
2	RW	0x0	pcs_init_rstn Initial POR reset
1	RW	0x0	ovrd_pcs_lane_rstn Override enable for pcs_lane_rstn
0	RW	0x0	pcs_lane_rstn Lane reset

HDPTXPHY_CMN_REG00A0
Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_pcs_pll_en Override enable for pcs_pll_en
5	RW	0x0	pcs_pll_en Enable PLL.
4:2	RW	0x0	pcs_ref_freq_sel Reference clock selection 2'b00: Ref clk from XO 2'b01: Ref clk from IO 2'b10: Ref clk from Pixel clk in 2'b11: Ref clk from Sys pll
1	RW	0x0	ovrd_pcs_dp_pll_lock_done Override enable for pcs_dp_pll_lock_done
0	RW	0x0	pcs_dp_pll_lock_done PLL lock completion indicator

HDPTXPHY_SB_REG0102
Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	ana_sb_mon_tx_ref_clk_sel Not used for HDPTX

Bit	Attr	Reset Value	Description
5	RW	0x0	ovrd_sb_rxterm_en Override enable for sb_rxterm_en
4	RW	0x0	sb_rxterm_en Enable rx termination or source termination; this should go high after bias enable and calibration sequence in functional protocols.
3:0	RW	0x3	ana_sb_rxterm_offsp For i_sb_rescal_tune<2:0> = 3, the table for both Offset P and N looks like 4'b0000: 50 Ohms 4'b0001: 48.4 Ohms 4'b0011: 46.9 Ohms 4'b0111: 45.5 Ohms 4'b1111: 44.2 Ohms

HDPTXPHY_SB_REG0103

Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x3	ana_sb_rxterm_offsn For i_sb_rescal_tune<2:0> = 3, the table for both Offset P and N looks like 4'b0000: 50 Ohms 4'b0001: 48.4 Ohms 4'b0011: 46.9 Ohms 4'b0111: 45.5 Ohms 4'b1111: 44.2 Ohms
2	RW	0x0	ana_sb_rx_term_gnd_en External reference clock I/O termination to ground 1'b0: Disable termination to GND 1'b1: Enable termination to GND
1	RW	0x0	ovrd_sb_rx_rescal_done Override enable for sb_rx_rescal_done
0	RW	0x0	sb_rx_rescal_done Not used for HDPTX

HDPTXPHY_SB_REG0104

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_sb_rx_rescal_en Override enable for sb_rx_rescal_en
6	RW	0x0	sb_rx_rescal_en Not used for HDPTX
5	RW	0x0	ovrd_sb_en Override enable for sb_en
4	RW	0x0	sb_en Enables the common bias block for side band. This needs to be enabled only after BG_OK.
3	RW	0x0	ovrd_sb_arc_en Override enable for sb_arc_en
2	RW	0x0	sb_arc_en ARC Enable
1	RW	0x0	ovrd_sb_aux_en Override enable for sb_aux_en

Bit	Attr	Reset Value	Description
0	RW	0x0	sb_aux_en AUX Enable 1'b0: Disable 1'b1: Enable

HDPTXPHY_SB_REG0105
Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ovrd_sb_earc_cmdc_en Override enable for sb_earc_cmdc_en
5	RW	0x0	sb_earc_cmdc_en External reference clock I/O AC-coupling capacitor bypass enable 1'b0: Use AC coupling cap 1'b1: Bypass AC coupling cap
4	RW	0x0	ovrd_sb_earc_cmtx_en Override enable for sb_earc_cmtx_en
3	RW	0x0	sb_earc_cmtx_en Enables the voltage buffers for slewing rate controlle transmission.
2:0	RW	0x0	ana_sb_tx_hlvl_prog This controls the voltage buffer in/out high value. 3'b000: 480mV 3'b001: 490mV 3'b010: 515mV 3'b011: 535mV 3'b100: 560mV 3'b101: 580mV 3'b110: 600mV 3'b111: 623mV

HDPTXPHY_SB_REG0106
Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	ana_sb_tx_llvl_prog This controls the voltage buffer in/out low value. 3'b000: 320mV 3'b001: 310mV 3'b010: 285mV 3'b011: 260mV 3'b100: 240mV 3'b101: 220mV 3'b110: 200mV 3'b111: 180mV

Bit	Attr	Reset Value	Description
3:0	RW	0x0	ana_sb_tx_bias_ctrl <1:0> controls the slew Rate and <3:2> controls output stage current of buffer. Slew rate current 2'b00: (75uA) 2'b01: (100uA) 2'b10: (150uA) 2'b11: (200uA) Output stage current 2'b00: 8.0mA 2'b01: 4.0mA 2'b10: 4.0mA 2'b11: 2.0mA

HDPTXPHY_SB_REG0109

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	ana_sb_rx_vcm_n_ctrl SB RX VCM control
5	RW	0x0	ana_sb_aux_rx_vcm_sel Not used for HDPTX
4	RW	0x0	ovrd_sb_earc_dmrx_afc_done Override enable for sb_earc_dmrx_afc_done
3	RW	0x0	sb_earc_dmrx_afc_done After AFC calibration of PWM sampling oscillator this signal goes high. Using this AFC related signals are shut down.
2:0	RW	0x0	ana_sb_dmrx_afc_div_ratio This controls the post division after oscillator. 0, 6 and 7 are not valid codes. 3'b001: divide by 16 3'b010: divide by 8 3'b011: divide by 4 3'b100: divide by 2 3'b101: divide by 1 (default)

HDPTXPHY_SB_REG010D

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ana_sb_dmrx_lpbk_en This enables the loopback path for PWM detector; it bypasses the sampler.
4	RW	0x0	ana_sb_dmrx_lpbk_data The loopback data from register; the duty cycle of the data has to be more than 53% or less than 47%.
3:2	RW	0x0	ana_sb_dmrx_ref_prog SB DMRX reference programming
1:0	RW	0x0	ana_sb_dmrx_hyst_prog SB DMRX hysteresis programming

HDPTXPHY_SB_REG010F

Address: Operational Base + offset (0x043C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	ovrd_sb_vreg_en Override enable for sb_vreg_en
6	RW	0x0	sb_vreg_en Enables Regulator for PWM Detector.
5	RW	0x0	ovrd_sb_vreg_lpf_bypass Override enable for sb_vreg_lpf_bypass
4	RW	0x0	sb_vreg_lpf_bypass Bypasses the LPF during LDO bring up
3:0	RW	0x1	ana_sb_vreg_gain_ctrl Controls the feedback gain of the LDO. 4'b0000: 1.00 4'b0001: 1.03 4'b0010: 1.04 4'b0011: 1.05 4'b0100: 1.06 4'b0101: 1.09 4'b0110: 1.12 4'b0111: 1.15

HDPTXPHY_SB_REG0110

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	ana_sb_vreg_ictrl Controls the error amplifier tail current 0: 250uA 1: 500uA 2: 750uA 3: 1.00mA
4:2	RW	0x0	ana_sb_vreg_ladder_sel Controls the regulated output voltage. 3'b000: 700mV 3'b001: 725mV 3'b010: 750mV 3'b011: 775mV 3'b100: 800mV 3'b101: 825mV 3'b110: 850mV 3'b111: 875mV
1	RW	0x0	ana_sb_vreg_out_sel It bypasses the LDO with VDD.
0	RW	0x0	ana_sb_vreg_ref_sel Used as power saving mode.

HDPTXPHY_SB_REG0113

Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	sb_rx_rcal_opt_code This is use to select finale rcal code after rcal enable goes low and rcal done goes high 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code + i_sfr_rcal_code(i_sfr_sb_rx_rterm_ctrl) 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code(i_sfr_sb_rx_rterm_ctrl)
3:0	RW	0x0	sb_rx_rterm_ctrl This is the code to be added in the tune code to generate finale rcal code depends on the value of i_sfr_sb_rx_rcal_opt_code

HDPTXPHY_SB_REG0114

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

5:3	RW	0x0	sb_tg_sb_en_delay_time
			This sfr is the select line to set count wrt refclock cycle to set sb enable after rcal done goes high
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

2:0	RW	0x0	sb_tg_rxterm_en_delay_time
			This sfr is the select line to set count wrt refclock cycle to set sb rxterm enable signal after sb en goes high
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

HDPTXPHY_SB_REG0115

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description

5:3	RW	0x0	sb_ready_delay_time
			This sfr is the select line to set count count wrt refclock cycle to set sb ready signal after all calibration completed
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

2:0	RW	0x0	sb_tg_osc_en_delay_time
			This sfr is the select line to set count count wrt refclock cycle to set oscillator enable after vreg sequence completed
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

HDPTXPHY_SB_REG0116

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

6:4	RW	0x0	sb_tg_osc_en_to_afc_rstn_delay_time
			This sfr is the select line to set count wrt refclock cycle to release reset to afc calibration module after oscillator osc enable signal set.
			3'b000: delay_time = 9'd0; // 0
			3'b001: delay_time = 9'd13; // 0.5us for 25MHz refclk
			3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
			3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
			3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
			3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
			3'b110: delay_time = 9'd250; // 10us for 25MHz refclk
			3'b111: delay_time = 9'd500; // 20us for 25MHz refclk
			default: delay_time = 9'd25; // 1us for 25MHz refclk

3:2	RW	0x0	sb_pwm_start_code
			This is the sfr select line to set initial pwm code to start pwm calibration
			2'b00: pwm_start_code = 5'b0_1111; //-15
			2'b01: pwm_start_code = 5'b0_1010; //-10
			2'b10: pwm_start_code = 5'b0_0101; //-5
			2'b11: pwm_start_code = 5'b0_0000; // 0
			default: pwm_start_code = 5'b0_1111; //-15

Bit	Attr	Reset Value	Description
1:0	RW	0x0	sb_oc_settle_time This is the count which is use to select refclock cycle count to settle comparator output for latest calibration code 2'b00: settle_time = 5'd6; 2'b01: settle_time = 5'd12; 2'b10: settle_time = 5'd18; 2'b11: settle_time = 5'd24; default: settle_time = 5'd6;

HDPTXPHY_SB_REG0117

Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	sb_oc_num_of_sample This is use to select number of times oc comparator output to be sampled for applied cal code to make sure cal code matches reuired specifiction 2'b00: sample_cnt = 4'd2; 2'b01: sample_cnt = 4'd6; 2'b10: sample_cnt = 4'd10; 2'b11: sample_cnt = 4'd14; default: sample_cnt = 4'd2;
5	RW	0x0	sb_oc_en This sfr enable offset calibration
4	RW	0x0	sb_oc_bypass_pwm Bypass enable for PWM

3:0	RW	0x0	sb_tg_pll_cd_vreg_fast_pulse_time
			This sfr is the select line to set number of clock cycle for which vreg bypass signal go high
			4'b0000: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd25;//1us
			4'b0001: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd50;//2us
			4'b0010: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd75;//3us
			4'b0011: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd100;//4us
			4'b0100: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd125;//5us
			4'b0101: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;//10us
			4'b0110: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd500;//20us
			4'b0111: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd750;//30us
			4'b1000: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1000;//40us
			4'b1001: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1250;//50us
			4'b1010: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd2500;//100us
			4'b1011: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd3750;//150us
			4'b1100: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd5000;//200us
			4'b1101: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd7500;//300us
			4'b1110: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd10000;//400us
			4'b1111: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd12500;//500us
			default: tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;

HDPTXPHY_SB_REG0118

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_earc_dmrx_recvrd_clk_cnt This is the target count the rec clk should give for specifide refclock cycle This count should be 10, 20 or 40 (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)

HDPTXPHY_SB_REG0119

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	sb_tg_cnt_run_no__9_8 This is the refclock count cycle during which rec clock counter run. This count should be such that time duration with refclock good enough to get requird rec clock count (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)

HDPTXPHY_SB_REG011A

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_cnt_run_no__7_0 This is the refclock count cycle during which rec clock counter run This count should be such that time duration with refclock good enough to get requird rec clock count (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)

HDPTXPHY_SB_REG011B

Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sb_earc_sig_det_bypass This sfr use to bypass signal detect logic
3:0	RW	0x0	sb_afc_tol OSC stable tolerance. This is the tolarance for vco count that can be taken to make sure vco generating stable frequency

HDPTXPHY_SB_REG011C

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sb_afc_stb_num OSC stable number for initial time. it uses to configure number of time vco generate stable count to go for stable frequency comparison state

HDPTXPHY_SB_REG011D

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_osc_cnt_min This is the minimum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock. Refclock: count required 24MHz: 103 25MHz: 99 26MHz: 95 27MHz: 92 45MHz: 55 54MHz: 46

HDPTXPHY_SB_REG011E

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sb_tg_osc_cnt_max This is the maximum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock. Refclock: count required 24MHz: 106 25MHz: 101 26MHz: 98 27MHz: 94 45MHz: 57 54MHz: 48

HDPTXPHY_SB_REG011F

Address: Operational Base + offset (0x047C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sb_pwm_afc_ctrl This is the sfr which use for selecting pwm afc calibration code depending on its MSB MSB = 1 then MSB from -1 to 0 bits value taken as calibration code for pwm afc MSB = 0 then afc code is internally generated from afc module logic if AFC _EN =1
5:2	RO	0x0	reserved
1	RW	0x0	sb_rcal_rstn Sideband resister calibration enable signal 1'b0: Resister calibration disable 1'b1: Resister calibration enable
0	RW	0x0	sb_arc_en_in Sideband arc enable signal 1'b0: ARC disable 1'b1: ARC enable

HDPTXPHY_SB_REG0120

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	sb_aux_en_in Sideband aux enable signal 1'b0: AUX disable 1'b1: AUX enable
6	RW	0x0	sb_rx_term_sel Sideband rx term sel 1'b1: Code taken from lane rcal 1'b0: Code taken from rcal module in sideband
5:4	RW	0x0	sb_rcal_term_sel Not used
3:2	RW	0x0	sb_rcal_lane_sel Select rcal code to sideband from lane 0,1,2,3. 2'b00: Lane0 code to sideband from lane 2'b01: Lane1 code to sideband from lane 2'b10: Lane2 code to sideband from lane 2'b11: Lane3 code to sideband from lane
1	RW	0x0	sb_eARC_en Enable eARC mode for HDMI
0	RW	0x0	sb_eARC_afc_en 1'b0: AFC disable 1'b1: AFC enable

HDPTXPHY_SB_REG0123

Address: Operational Base + offset (0x048C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_sb_earc_rx_mode Override enable for sb_earc_rx_mode
6	RW	0x0	sb_earc_rx_mode PHY input to eARC in cmrx mode
5	RW	0x0	ovrd_sb_ready Override enable for sb_ready
4	RW	0x0	sb_ready Showing sideband ready signal to analog
3	RW	0x0	ovrd_sb_sig_det_done Override enable for sb_sig_det_done
2	RW	0x0	sb_sig_det_done Show signal detect done in dmac rx mode
1	RW	0x0	ovrd_sb_earc_dmac_en Override enable for sb_earc_dmac_en
0	RW	0x0	sb_earc_dmac_en Input enabling from digital module for signal detect module

HDPTXPHY_INTOP_REG0200

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	dck_master_lane Select master read pointer clock source 2'b00: Lane 0 2'b01: Lane 1 2'b10: Lane 2 2'b11: Lane 3

Bit	Attr	Reset Value	Description
4:3	RW	0x0	master_lane_sel TX control interface of one source lane is driven to all lanes in align mode. Sources - 2'b00: Lane 0 2'b01: Lane 1 2'b10: Lane 2 2'b11: Lane 3
2	RW	0x0	protocol_sel Mux select on input data to data path CTS pattern generator gives 20 bit which the data path converts to 40 bits. In all other cases, input data connects to data path
1	RW	0x0	hdmi_tmds_frl_sel Mux selects on input data to data path In HDMI TMDS mode, one of the lanes needs to generate clock which is achieved using SFR clock user pattern. In all other cases, input data connects to data path
0	RW	0x0	cts_mode Transmits 20-bit CTS data when set to 1

HDPTXPHY_INTOP_REG0201

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__39_32 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0203

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__23_16 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0204

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__15_8 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0205

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_user_pat__7_0 40-bit clock signal generated for HDMI TMDS mode

HDPTXPHY_INTOP_REG0206

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ctrl_align_mode TX control interface mux based on master lane selection is valid only if ctrl_align_mode is set to 1

Bit	Attr	Reset Value	Description
6:5	RW	0x0	deskew_ptr_master_lane_sel Deskew pointer control based on master lane
4:3	RW	0x0	lane_swap_sel Selects one of four lane swap combinations (xx: o/p lane - i/p lane) 2'b00: 0 - 0, 1 - 1, 2 - 2, 3 - 3 2'b01: 0 - 1, 1 - 0, 2 - 2, 3 - 3 2'b10: 0 - 0, 1 - 1, 2 - 3, 3 - 2 2'b11: 0 - 3, 1 - 2, 2 - 1, 3 - 0
2:1	RW	0x0	data_bus_width Used for data bus width conversion 1'b0: Converts the 20-bit data in 20b clock domain to 40-bit data in tbc domain 1'b1: Conversion happends based on CTS mode value
0	RW	0x0	bus_width_sel 1'b1: Sets 36/40 bits data bus operation 1'b0: Sets 18/20 bits data bus operation

HDPTXPHY_INTOP_REG0207

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	lane_en Lane enabling for sync pulse and sync loss signals

HDPTXPHY_LANE_REG0303

Address: Operational Base + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln0_ana_tx_drv_eien_fb_en tx common mode feedback when eien is enable 1'b0: Disable 1'b1: Enable (feedback is enable)
5	RW	0x0	ovrd_ln0_tx_drv_lvl_ctrl Override enable for ln0_tx_drv_lvl_ctrl
4:0	RW	0x00	ln0_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap-level (max swing) ... 5'b00000: min main-tap-level (min swing) Others: N/A

HDPTXPHY_LANE_REG0307

Address: Operational Base + offset (0x0C1C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln0_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement) 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln0_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement

Bit	Attr	Reset Value	Description
2	RW	0x0	ln0_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
1	RW	0x0	ln0_ana_tx_d ln0_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln0_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG030A

Address: Operational Base + offset (0x0C28)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln0_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln0_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG030B

Address: Operational Base + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln0_tx_jeq_even_ctrl_hbr [hbr]TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln0_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG030C

Address: Operational Base + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln0_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln0_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG030D

Address: Operational Base + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln0_tx_jeq_odd_ctrl_hbr [hbr]TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln0_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG030E

Address: Operational Base + offset (0x0C38)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln0_tx_jeq_odd_ctrl_hbr3 [hbr3] TX jitter EQ driver (odd) strength control same as even control
2	RW	0x0	ovrd_ln0_tx_rcal_en Override enable for ln0_tx_rcal_en
1	RW	0x0	ln0_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln0_ana_tx_rterm_42p5_en TX 42.5 ohms termination enable 1'b0: Disable (50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG030F

Address: Operational Base + offset (0x0C3C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	ovrd_ln0_tx_rxd_comp_en Override enable for ln0_tx_rxd_comp_en
6	RW	0x0	ln0_tx_rxd_comp_en TX receiver detector comparator enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	ovrd_ln0_tx_rxd_en Override enable for ln0_tx_rxd_en
4	RW	0x0	ln0_tx_rxd_en TX receiver detector enable. Drives a transition on the serial data and measures the charge time of the line in order to determine whether a receiver is connected. 1'b0: normal operation 1'b1: initiate a receiver detect sequence
3	RW	0x0	ln0_ana_tx_rxd_comp_i_ctrl TX receiver detector comparator bias control 1'b0: 1x 1'b1: 3x
2	RW	0x0	ln0_ana_tx_bist_en Enables BIST for serial nodes.
1:0	RW	0x0	ln0_ana_tx_bist_clkdel_prog Phase shifting delay in BIST clock path.

HDPTXPHY_LANE_REG0310
Address: Operational Base + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	ln0_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln0_ana_tx_sync_loss_det_mode Selects the sync loss detection mode from the following table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0311
Address: Operational Base + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln0_tx_sync_pulse_det_clk_en Override enable for ln0_tx_sync_pulse_det_clk_en
6	RW	0x0	ln0_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln0_tx_sync_pulse_det_en Override enable for ln0_tx_sync_pulse_det_en

Bit	Attr	Reset Value	Description
4	RW	0x0	ln0_tx_sync_pulse_det_en Enables the sync loss detector
3	RW	0x0	ln0_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
2	RW	0x0	ln0_tx_ser_40bit_en_hbr [hbr]TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln0_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
0	RW	0x0	ln0_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0312

Address: Operational Base + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln0_tx_ser_data_rstn Override enable for ln0_tx_ser_data_rstn
6	RW	0x0	ln0_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released
5	RW	0x0	ln0_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln0_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln0_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln0_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln0_tx_ser_clk_rstn Override enable for ln0_tx_ser_clk_rstn
0	RW	0x0	ln0_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

HDPTXPHY_LANE_REG0316

Address: Operational Base + offset (0x0C58)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	ln0_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG031B

Address: Operational Base + offset (0x0C6C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ln0_ana_tx_reserved Reserved port

HDPTXPHY_LANE_REG031F

Address: Operational Base + offset (0x0C7C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ln0_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion
4:2	RW	0x5	ln0_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln0_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

HDPTXPHY_LANE_REG0320

Address: Operational Base + offset (0x0C80)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x5	ln0_tg_ser_vreg_fast_pulse_time 3'b000: 1us 3'b001: 2us 3'b010: 3us 3'b011: 4us 3'b100: 5us 3'b101: 10us 3'b110: 20us 3'b111: 30us
4	RW	0x0	ln0_ovrd_txd_deskew_rstn Override enable for ln0_txd_deskew_rstn
3	RW	0x0	ln0_txd_deskew_rstn Active low reset for the lane data path
2	RW	0x0	ln0_txd_deskew_bypass_err_chk Counter relation check bypass
1	RW	0x0	ln0_txd_deskew_fix_da Fix the latch phase
0	RW	0x0	ln0_txd_deskew_fix_db Fix the latch phase

HDPTXPHY_LANE_REG0403

Address: Operational Base + offset (0x100C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln1_ana_tx_drv_eien_fb_en Tx common mode feedback when EIEN is enable 1'b0: Disable 1'b1: Enable (feedback is enable)
5	RW	0x0	ovrd_ln1_tx_drv_lvl_ctrl Override enable for ln1_tx_drv_lvl_ctrl
4:0	RW	0x00	ln1_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap-level (max swing) ... 5'b00000: min main-tap-level (min swing) Others: N/A

HDPTXPHY_LANE_REG0407

Address: Operational Base + offset (0x101C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln1_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement) 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln1_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement
2	RW	0x0	ln1_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1	RW	0x0	ln1_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln1_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG040A

Address: Operational Base + offset (0x1028)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln1_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln1_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG040B

Address: Operational Base + offset (0x102C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln1_tx_jeq_even_ctrl_hbr [hbr]TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln1_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG040C

Address: Operational Base + offset (0x1030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln1_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln1_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG040D

Address: Operational Base + offset (0x1034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln1_tx_jeq_odd_ctrl_hbr [hbr] TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln1_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG040E

Address: Operational Base + offset (0x1038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln1_tx_jeq_odd_ctrl_hbr3 [hbr3] TX jitter EQ driver (odd) strength control same as even control
2	RW	0x0	ovrd_ln1_tx_rcal_en Override enable for ln1_tx_rcal_en
1	RW	0x0	ln1_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln1_ana_tx_rterm_42p5_en TX 42.5 ohms termination enable 1'b0: Disable (50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG0410

Address: Operational Base + offset (0x1040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:2	RW	0x00	ln1_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln1_ana_tx_sync_loss_det_mode Slects the sync loss detection mode from the followin table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0411

Address: Operational Base + offset (0x1044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln1_tx_sync_pulse_det_clk_en Override enable for ln1_tx_sync_pulse_det_clk_en
6	RW	0x0	ln1_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln1_tx_sync_pulse_det_en Override enable for ln1_tx_sync_pulse_det_en
4	RW	0x0	ln1_tx_sync_pulse_det_en Enables the sync loss detector.
3	RW	0x0	ln1_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
2	RW	0x0	ln1_tx_ser_40bit_en_hbr [hbr]TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln1_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
0	RW	0x0	ln1_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0412

Address: Operational Base + offset (0x1048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln1_tx_ser_data_rstn Override enable for ln1_tx_ser_data_rstn

Bit	Attr	Reset Value	Description
6	RW	0x0	ln1_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released
5	RW	0x0	ln1_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln1_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln1_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln1_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln1_tx_ser_clk_rstn Override enable for ln1_tx_ser_clk_rstn
0	RW	0x0	ln1_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

HDPTXPHY_LANE_REG0416

Address: Operational Base + offset (0x1058)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	ln1_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG041B

Address: Operational Base + offset (0x106C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ln1_ana_tx_reserved Reserved port

HDPTXPHY_LANE_REG041F
Address: Operational Base + offset (0x107C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ln1_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion
4:2	RW	0x5	ln1_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln1_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

HDPTXPHY_LANE_REG0503
Address: Operational Base + offset (0x140C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln2_ana_tx_drv_eien_fb_en Tx common mode feedback when eien is enable 1'b0: Disable 1'b1: Enable (feedback is enable)
5	RW	0x0	ovrd_ln2_tx_drv_lvl_ctrl Override enable for ln2_tx_drv_lvl_ctrl
4:0	RW	0x00	ln2_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap level (max swing) ... 5'b00000: min main-tap level (min swing) Others: N/A

HDPTXPHY_LANE_REG0507
Address: Operational Base + offset (0x141C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln2_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement), 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln2_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement

Bit	Attr	Reset Value	Description
2	RW	0x0	ln2_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
1	RW	0x0	ln2_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln2_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG050A

Address: Operational Base + offset (0x1428)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln2_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln2_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG050B

Address: Operational Base + offset (0x142C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln2_tx_jeq_even_ctrl_hbr [hbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln2_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG050C

Address: Operational Base + offset (0x1430)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ln2_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln2_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG050D

Address: Operational Base + offset (0x1434)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ln2_tx_jeq_odd_ctrl_hbr [hbr] TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln2_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG050E

Address: Operational Base + offset (0x1438)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln2_tx_jeq_odd_ctrl_hbr3 [hbr3] TX jitter EQ driver (odd) strength control same as even control
2	RW	0x0	ovrd_ln2_tx_rcal_en Override enable for ln2_tx_rcal_en
1	RW	0x0	ln2_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln2_ana_tx_rterm_42p5_en TX 42.5 ohms termination enable 1'b0: Disable (50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG0510

Address: Operational Base + offset (0x1440)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:2	RW	0x00	ln2_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln2_ana_tx_sync_loss_det_mode Selects the sync loss detection mode from the following table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0511

Address: Operational Base + offset (0x1444)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln2_tx_sync_pulse_det_clk_en Override enable for ln2_tx_sync_pulse_det_clk_en
6	RW	0x0	ln2_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln2_tx_sync_pulse_det_en Override enable for ln2_tx_sync_pulse_det_en
4	RW	0x0	ln2_tx_sync_pulse_det_en Enables the sync loss detector.
3	RW	0x0	ln2_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
2	RW	0x0	ln2_tx_ser_40bit_en_hbr [hbr]TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln2_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width
0	RW	0x0	ln2_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0512

Address: Operational Base + offset (0x1448)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln2_tx_ser_data_rstn Override enable for ln2_tx_ser_data_rstn
6	RW	0x0	ln2_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released

Bit	Attr	Reset Value	Description
5	RW	0x0	ln2_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln2_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln2_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln2_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln2_tx_ser_clk_rstn Override enable for ln2_tx_ser_clk_rstn
0	RW	0x0	ln2_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

HDPTXPHY_LANE_REG0516

Address: Operational Base + offset (0x1458)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	ln2_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG051B

Address: Operational Base + offset (0x146C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ln2_ana_tx_reserved Reserved port

HDPTXPHY_LANE_REG051F

Address: Operational Base + offset (0x147C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	ln2_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion
4:2	RW	0x5	ln2_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln2_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

HDPTXPHY_LANE_REG0520

Address: Operational Base + offset (0x1480)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x5	ln2_tg_ser_vreg_fast_pulse_time 3'b000: 1us 3'b001: 2us 3'b010: 3us 3'b011: 4us 3'b100: 5us 3'b101: 10us 3'b110: 20us 3'b111: 30us
4	RW	0x0	ln2_ovrd_txd_deskew_rstn Override enable for ln2_txd_deskew_rstn
3	RW	0x0	ln2_txd_deskew_rstn Active low reset for the lane data path
2	RW	0x0	ln2_txd_deskew_bypass_err_chk Counter relation check bypass
1	RW	0x0	ln2_txd_deskew_fix_da Fix the latch phase
0	RW	0x0	ln2_txd_deskew_fix_db Fix the latch phase

HDPTXPHY_LANE_REG0521

Address: Operational Base + offset (0x1484)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln2_txd_deskew_bypass Enable Tx data bypass
6	RW	0x0	ln2_txd_data_clk_type_man_en Unused
5:4	RW	0x1	ln2_txd_clk_type Unused

Bit	Attr	Reset Value	Description
3:2	RW	0x1	ln2_txd_data_type Unused
1	RW	0x0	ln2_nearlb_en 1'b1: Enables nearend loopback mode 1'b0: Disables nearend loopback mode
0	RW	0x0	ln2_bist_auto_run Auto BIST start and errinj

HDPTXPHY_LANE_REG0603

Address: Operational Base + offset (0x180C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln3_ana_tx_drv_eien_fb_en tx common mode feedback when eien is enable 1'b0: Disable 1'b1: Enable (feedback is enable)
5	RW	0x0	ovrd_ln3_tx_drv_lvl_ctrl Override enable for ln3_tx_drv_lvl_ctrl
4:0	RW	0x00	ln3_tx_drv_lvl_ctrl TX driver main-tap level (TX_AMP<10:0>) 5'b01010: max main-tap-level (max swing) ... 5'b00000: min main-tap-level (min swing) Others: N/A

HDPTXPHY_LANE_REG0607

Address: Operational Base + offset (0x181C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln3_ana_tx_drv_accdrv_pol_sel TX edge-enhancement AC coupled driver sign selection 1'b0: Polarity change, data P/N is switched (deenhancement) 1'b1: Polarity non-change(enhancement)
5:3	RW	0x0	ln3_ana_tx_drv_accdrv_ctrl TX edge-enhancement AC coupled driver strength control 3'b000: No enhancement ... 3'b111: Max enhancement
2	RW	0x0	ln3_ana_tx_drv_hsclk_mon_en Enable of high-speed clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
1	RW	0x0	ln3_ana_tx_drv_pll_ref_mon_en Enable of PLL reference clock monitor through Tx driver 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln3_ana_tx_drv_pll_ref_mon_sel Select PLL reference clock monitor through Tx driver 1'b0: LCPLL 1'b1: ROPLL (MPHY do not need this pin, always LCPLL)

HDPTXPHY_LANE_REG060A

Address: Operational Base + offset (0x1828)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ln3_ana_tx_jeq_en TX jitter EQ enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ln3_tx_jeq_even_ctrl_rbr [rbr] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG060B
Address: Operational Base + offset (0x182C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln3_tx_jeq_even_ctrl_hbr [hbr]TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

Bit	Attr	Reset Value	Description
3:0	RW	0x0	ln3_tx_jeq_even_ctrl_hbr2 [hbr2] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on

HDPTXPHY_LANE_REG060C
Address: Operational Base + offset (0x1830)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln3_tx_jeq_even_ctrl_hbr3 [hbr3] TX jitter EQ driver (even) strength control 4'b0000: 0 legs on (jitter EQ driver off) 4'b0001: 2 legs on 4'b0010: 2 legs on 4'b0011: 4 legs on 4'b0100: 3 legs on 4'b0101: 5 legs on 4'b0110: 5 legs on 4'b0111: 7 legs on 4'b1000: 3 legs on 4'b1001: 5 legs on 4'b1010: 5 legs on 4'b1011: 7 legs on 4'b1100: 6 legs on 4'b1101: 8 legs on 4'b1110: 8 legs on 4'b1111: 10 legs on
3:0	RW	0x0	ln3_tx_jeq_odd_ctrl_rbr [rbr] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG060D
Address: Operational Base + offset (0x1834)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ln3_tx_jeq_odd_ctrl_hbr [hbr] TX jitter EQ driver (odd) strength control same as even control
3:0	RW	0x0	ln3_tx_jeq_odd_ctrl_hbr2 [hbr2] TX jitter EQ driver (odd) strength control same as even control

HDPTXPHY_LANE_REG060E

Address: Operational Base + offset (0x1838)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:3	RW	0x0	ln3_tx_jeq_odd_ctrl_hbr3 [hbr3] TX jitter EQ driver (odd) strength control Same as even control
2	RW	0x0	ovrd_ln3_tx_rcal_en Override enable for ln3_tx_rcal_en
1	RW	0x0	ln3_tx_rcal_en TX RCAL enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	ln3_ana_tx_rterm_42p5_en TX 42.5 ohms termination enable 1'b0: Disable (50 ohm) 1'b1: Enable (42.5 ohm)

HDPTXPHY_LANE_REG0610

Address: Operational Base + offset (0x1840)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:2	RW	0x00	ln3_ana_tx_bist_mode This defines the BIST paths and modes as follows: <0> enables the serializer data output. <1> flips the serializer data output <3:2> defines the line sampling input 2'b00: txp-txn 2'b01: txn-vdd/2 2'b10: txp-vdd/2 2'b11: off <4> inverts the byte clock <5> enables the SA bist clock in LANE CD
1:0	RW	0x2	ln3_ana_tx_sync_loss_det_mode Slects the sync loss detection mode from the followin table: 2'b00: 2UI pulse from div10 clock 2'b01: 4UI pulse from div10 clock 2'b10: 2UI pulse from div40 clock 2'b11: 4UI pulse from div40 clock

HDPTXPHY_LANE_REG0611

Address: Operational Base + offset (0x1844)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln3_tx_sync_pulse_det_clk_en Override enable for ln3_tx_sync_pulse_det_clk_en
6	RW	0x0	ln3_tx_sync_pulse_det_clk_en Enables the clock path for sync loss detector.
5	RW	0x0	ovrd_ln3_tx_sync_pulse_det_en Override enable for ln3_tx_sync_pulse_det_en.
4	RW	0x0	ln3_tx_sync_pulse_det_en Enables the sync loss detector.

Bit	Attr	Reset Value	Description
3	RW	0x0	ln3_tx_ser_40bit_en_rbr [rbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
2	RW	0x0	ln3_tx_ser_40bit_en_hbr [hbr] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
1	RW	0x0	ln3_tx_ser_40bit_en_hbr2 [hbr2] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit
0	RW	0x0	ln3_tx_ser_40bit_en_hbr3 [hbr3] TX serializer data width selection 1'b0: 20/16-bit 1'b1: 40/32-bit

HDPTXPHY_LANE_REG0612
Address: Operational Base + offset (0x1848)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ovrd_ln3_tx_ser_data_rstn Override enable for ln3_tx_ser_data_rstn
6	RW	0x0	ln3_tx_ser_data_rstn TX serializer data-path resetn 1'b0: Reset 1'b1: Released
5	RW	0x0	ln3_tx_ser_rate_sel_rbr [rbr] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
4	RW	0x0	ln3_tx_ser_rate_sel_hbr [hbr]TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
3	RW	0x0	ln3_tx_ser_rate_sel_hbr2 [hbr2] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
2	RW	0x0	ln3_tx_ser_rate_sel_hbr3 [hbr3] TX serializer data rate selection for Gen4 (Need to be controlled with i_tx_en_40bit) 1'b0: 20/40-bit 1'b1: 16/32-bit
1	RW	0x0	ovrd_ln3_tx_ser_clk_rstn Override enable for ln3_tx_ser_clk_rstn
0	RW	0x0	ln3_tx_ser_clk_rstn TX serializer clock-path resetn 1'b0: Reset 1'b1: Released

HDPTXPHY_LANE_REG0616

Address: Operational Base + offset (0x1858)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	ln3_ana_tx_ser_vreg_gain_ctrl Control regulator feedback gain--> <3>: No connect, <2:0>: Gain--> 3'b000: 1 3'b001: 1.03 3'b010: 1.035 3'b011: 1.043 3'b100: 1.059 3'b101: 1.094 3'b110: 1.118 3'b111: 1.155 Output regulator voltage: Gain*VDD

HDPTXPHY_LANE_REG061B

Address: Operational Base + offset (0x186C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	ln3_ana_tx_reserved Reserved port

HDPTXPHY_LANE_REG061E

Address: Operational Base + offset (0x1878)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ln3_ovrd_tx_rcal_done Override enable for ln3_tx_rcal_done
6	RW	0x0	ln3_tx_rcal_done Monitoring for TX RCAL done
5	RW	0x0	ln3_drv_lvl_deskew_bypass Unused
4	RW	0x0	ln3_eien_deskew_bypass Unused
3	RW	0x0	ln3_hdmi_tmds_clk_lane_sel Selects clock user pattern or 40-bit tx data depending on protocol select and HDMI TMDS FRL select signals
2	RW	0x0	ln3_polarity_inv Polarity inversion of data when set to 1
1	RW	0x0	ln3_lane_mode 1'b1: The deskew FIFO works on shared pointer 1'b0: The deskew FIFO works on its own pointers
0	RW	0x0	ln3_lane_timer_sel 1'b1: Updates the lane timer value on monitoring interface even if Lane SSM did not complete 1'b0: Lets the lane timer updated on monitoring interface only when Lane SSM completes

HDPTXPHY_LANE_REG061F

Address: Operational Base + offset (0x187C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	ln3_rx_clk_inv 1'b1: Inverts the BIST recovered clock before feeding to PMA digital BIST RX path 1'b0: Passes the BIST recovered clock to PMA digital BIST RX path without inversion
4:2	RW	0x5	ln3_tg_rcal_rstn_delay_time Rx Rcal reset delay time after PLL AFC done 3'b000: 0 3'b001: 0.5us 3'b010: 1us 3'b011: 2us 3'b100: 3us 3'b101: 5us 3'b110: 10us 3'b111: 20us
1:0	RW	0x0	ln3_tg_tx_dcc_en_delay_time 2'b00: 3'd4 2'b01: 3'd5 2'b10: 3'd6 2'b11: 3'd7

27.5 Interface Description

Table 27-2 HDMI TX PHY0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
hdmitx0_ln0_txdp	O	HDMI_TX0_D0P/eDP_TX0_D0P	NS
hdmitx0_ln0_txdn	O	HDMI_TX0_D0N/eDP_TX0_D0N	NS
hdmitx0_ln1_txdp	O	HDMI_TX0_D1P/eDP_TX0_D1P	NS
hdmitx0_ln1_txdn	O	HDMI_TX0_D1N/eDP_TX0_D1N	NS
hdmitx0_ln2_txdp	O	HDMI_TX0_D2P/eDP_TX0_D2P	NS
hdmitx0_ln2_txdn	O	HDMI_TX0_D2N/eDP_TX0_D2N	NS
hdmitx0_ln3_txdp	O	HDMI_TX0_D3P/eDP_TX0_D3P	NS
hdmitx0_ln3_txdn	O	HDMI_TX0_D3N/eDP_TX0_D3N	NS
hdmitx0_sbdp	I/O	HDMI_TX0_SBDP/eDP_TX0_AUXP	NS
hdmitx0_sbdn	I/O	HDMI_TX0_SBDN/eDP_TX0_AUXN	NS
hdmitx0_cec_m0	I/O	BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d	BUS_IOC_GPIO4C_IOMUX_SEL_L[7:4]==5
hdmitx0_cec_m1	I/O	I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[7:4]==d
hdmitx0_hpd_m0	I/O	HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[7:4]==5
hdmitx0_hpd_m1	I/O	HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d	BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0]==3
hdmitx0_scl_m0	I/O	BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/DDRPHY_CH3_DTB3/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7_u	BUS_IOC_GPIO4B_IOMUX_SEL_H[15:12]==5
hdmitx0_scl_m1	I/O	I2S1_SDO3_M1/CPU_BIG1_AVS/I	BUS_IOC_GPIO

Module Pin	Direction	Pad Name	IOMUX Setting
		2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u	0D_IOMUX_SEL_H[7:4]==b
hdmitx0_scl_m2	I/O	CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u	PMU2_IOC_GPIO0D_IOMUX_SEL_H[7:4]==8 BUS_IOC_GPIO3C_IOMUX_SEL_H[15:12]==5
hdmitx0_sda_m0	I/O	BT1120_D14/PCIE20X1_2_WAKEN_M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0_u	BUS_IOC_GPIO4C_IOMUX_SEL_L[3:0]==5
hdmitx0_sda_m1	I/O	I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u	BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0]==b
hdmitx0_sda_m2	I/O	CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u	PMU2_IOC_GPIO0D_IOMUX_SEL_H[3:0]==8 BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0]==5

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 27-3 HDMI TX PHY1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
hdmitx1_ln0_txdp	O	HDMI_TX1_D0P/eDP_TX1_D0P	NS
hdmitx1_ln0_txdn	O	HDMI_TX1_D0N/eDP_TX1_D0N	NS
hdmitx1_ln1_txdp	O	HDMI_TX1_D1P/eDP_TX1_D1P	NS
hdmitx1_ln1_txdn	O	HDMI_TX1_D1N/eDP_TX1_D1N	NS
hdmitx1_ln2_txdp	O	HDMI_TX1_D2P/eDP_TX1_D2P	NS
hdmitx1_ln2_txdn	O	HDMI_TX1_D2N/eDP_TX1_D2N	NS
hdmitx1_ln3_txdp	O	HDMI_TX1_D3P/eDP_TX1_D3P	NS
hdmitx1_ln3_txdn	O	HDMI_TX1_D3N/eDP_TX1_D3N	NS
hdmitx1_sbdp	I/O	HDMI_TX1_SBDP/eDP_TX1_AUXP	NS
hdmitx1_sbdn	I/O	HDMI_TX1_SBDN/eDP_TX1_AUXN	NS
hdmitx1_cec_m0	I/O	GMAC0_PPSCLK/TEST_CLKOUT_M1/HDMI_TX1_CEC_M0/UART9_RX_M0/SPI1_CS1_M0/GPIO2_C4_d	PMU2_IOC_GPIO0D_IOMUX_SEL_L[7:4]==8 BUS_IOC_GPIO2C_IOMUX_SEL_H[3:0]==0
hdmitx1_cec_m1	I/O	I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u	BUS_IOC_GPIO0D_IOMUX_SEL_L[11:8]==d
hdmitx1_cec_m2	I/O	CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u	PMU2_IOC_GPIO0D_IOMUX_SEL_L[11:8]==8 BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0]==5
hdmitx1_hpd_m0	I/O	HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6_d	BUS_IOC_GPIO1A_IOMUX_SEL

Module Pin	Direction	Pad Name	IOMUX Setting
			_H[11:8]==5
hdmitx1_hpd_m1	I/O	GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d	BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12]==5
hdmitx1_scl_m0	I/O	GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u	BUS_IOC_GPIO2B_IOMUX_SEL_H[7:4]==4
hdmitx1_scl_m1	I/O	CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[11:8]==5
hdmitx1_scl_m2	I/O	HDMI_TX1_SCL_M2/SPI2_MISO_M0/GPIO1_A4_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[3:0]==5
hdmitx1_sda_m0	I/O	GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u	BUS_IOC_GPIO2B_IOMUX_SEL_H[3:0]==4
hdmitx1_sda_m1	I/O	CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u	BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4]==5
hdmitx1_sda_m2	I/O	HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d	BUS_IOC_GPIO1A_IOMUX_SEL_L[15:12]==5

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 27-4 EDP Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
edptx0_ln0_txdp	O	HDMI_TX0_D0P/eDP_TX0_D0P	NS
edptx0_ln0_txdn	O	HDMI_TX0_D0N/eDP_TX0_D0N	NS
edptx0_ln1_txdp	O	HDMI_TX0_D1P/eDP_TX0_D1P	NS
edptx0_ln1_txdn	O	HDMI_TX0_D1N/eDP_TX0_D1N	NS
edptx0_ln2_txdp	O	HDMI_TX0_D2P/eDP_TX0_D2P	NS
edptx0_ln2_txdn	O	HDMI_TX0_D2N/eDP_TX0_D2N	NS
edptx0_ln3_txdp	O	HDMI_TX0_D3P/eDP_TX0_D3P	NS
edptx0_ln3_txdn	O	HDMI_TX0_D3N/eDP_TX0_D3N	NS
edptx0_sbdp	I/O	HDMI_TX0_SBDP/eDP_TX0_AUXP	NS
edptx0_sbdn	I/O	HDMI_TX0_SBDN/eDP_TX0_AUXN	NS
edptx1_ln0_txdp	O	HDMI_TX1_D0P/eDP_TX1_D0P	NS
edptx1_ln0_txdn	O	HDMI_TX1_D0N/eDP_TX1_D0N	NS
edptx1_ln1_txdp	O	HDMI_TX1_D1P/eDP_TX1_D1P	NS
edptx1_ln1_txdn	O	HDMI_TX1_D1N/eDP_TX1_D1N	NS
edptx1_ln2_txdp	O	HDMI_TX1_D2P/eDP_TX1_	NS

Module Pin	Direction	Pad Name	IOMUX Setting
		D2P	
edptx1_ln2_txdn	O	HDMI_TX1_D2N/eDP_TX1_D2N	NS
edptx1_ln3_txdp	O	HDMI_TX1_D3P/eDP_TX1_D3P	NS
edptx1_ln3_txdn	O	HDMI_TX1_D3N/eDP_TX1_D3N	NS
edptx1_sbdp	I/O	HDMI_TX1_SBDP/eDP_TX1_AUXP	NS
edptx1_sbdn	I/O	HDMI_TX1_SBDN/eDP_TX1_AUXN	NS
edptx0_hpd_m0	I	HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[7:4]==4'h5
edptx0_hpd_m1	I	HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d	BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0]==4'h3
edptx1_hpd_m0	I	HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6_d	BUS_IOC_GPIO1A_IOMUX_SEL_H[11:8]==4'h5
edptx1_hpd_m1	I	GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d	BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12]==4'h5

Notes: I=input, O=output, I/O=input/output, bidirectional

27.6 Application Notes

27.6.1 SFR Settings for HDMI mode

This table shows how to set SFR in HDMI mode. The "Setting Value" column has settings for TMDS 40 bits mode with lane 3 as clock lane. Please follow the description column to set for 18/20/36 bits mode, FRL mode and clock lane change.

Table 27-5 DP 40bit mode with RBR rate SFR Setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0800[2]	protocol_sel	0x0	0x1	0: DP mode 1: HDMI mode
0x025C[1]	dig_clk_sel	0x0	0x1	1'b0: Select LCPLL reference clock mux output (LCPLL alone mode and Cascade mode) 1'b1: Select ROPLL reference clock mux output (ROPLL alone mode)
0x0C28[4]	ln0_ana_tx_jeq_en	0x0	0x1	Transmitter setting
0x1028[4]	ln1_ana_tx_jeq_en	0x0	0x1	Transmitter setting
0x1428[4]	ln2_ana_tx_jeq_en	0x0	0x1	Transmitter setting
0x1828[4]	ln3_ana_tx_jeq_en	0x0	0x1	Transmitter setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0C28[3:0]	ln0_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x0C2C[7:4]	ln0_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x0C2C[3:0]	ln0_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x0C30[7:4]	ln0_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1028[3:0]	ln1_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x102C[7:4]	ln1_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x102C[3:0]	ln1_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x130C[7:4]	ln1_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1428[3:0]	ln2_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x142C[7:4]	ln2_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x142C[3:0]	ln2_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1430[7:4]	ln2_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1828[3:0]	ln3_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter setting
0x182C[7:4]	ln3_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter setting
0x182C[3:0]	ln3_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1830[7:4]	ln3_tx_jeq_even_ctrl_hbr3	0x0	0x7	Transmitter setting
0x0C30[3:0]	ln0_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x0C34[7:4]	ln0_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0C34[3:0]	ln0_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x0C38[7:4]	ln0_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1030[3:0]	ln1_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x1034[7:4]	ln1_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting
0x1034[3:0]	ln1_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1038[7:4]	ln1_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1430[3:0]	ln2_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x1434[7:4]	ln2_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting
0x1434[3:0]	ln2_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1438[7:4]	ln2_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x1830[3:0]	ln3_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter setting
0x1834[7:4]	ln3_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter setting
0x1834[3:0]	ln3_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter setting
0x1838[3:0]	ln3_tx_jeq_odd_ctrl_hbr3	0x0	0x7	Transmitter setting
0x0C0C[4:0]	ln0_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x100C[4:0]	ln1_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x140C[4:0]	ln2_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x180C[4:0]	ln3_tx_drv_lvl_ctrl	0x0	0xC	Transmitter setting
0x0C1C[6]	ln0_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting
0x101C[6]	ln1_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x141C[6]	ln2_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting
0x181C[6]	ln3_ana_tx_drv_accdrv_pol_sel	0x0	0x0	Transmitter setting
0x0C1C[5:3]	ln0_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x101C[5:3]	ln1_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x141C[5:3]	ln2_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x181C[5:3]	ln3_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter setting
0x021C[2]	ana_pll_tx_hs_clk_en	0x0	0x1	PLL setting
0x0204[0]	ana_pll_cd_hsclk_east_en	0x0	0x1	PLL setting
0x0204[1]	ana_pll_cd_hsclk_west_en	0x0	0x0	PLL setting
0x0818[2:1]	data_bus_width	0x0	0x3	0x0: 18 bits data bus (for HDMI FRL mode only) 0x1: 20 bits data bus 0x2: 36 bits data bus (for HDMI FRL mode only) 0x3: 40 bits data bus
0x0818[0]	bus_width_sel	0x0	0x1	0x0: 18/20 bits data bus 0x1: 36/40 bits data bus
0x0254[1:0]	dp_tx_link_bw	0x0	0x0	Multiplexes the register settings for analog blocks. 0x0: RBR register settings applied to analog (*_rbr registers) 0x1: HBR register settings applied to analog (*_hbr registers) 0x2: HBR2 register settings applied to analog (*_hbr2 registers) 0x3: HBR3 register settings applied to analog (*_hbr3 registers)

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0264[2]	cmn_ropll_alone_mode	0x0	0x1	0x0: Cascade mode/LCPLL mode 0x1: ROPLL alone mode. For HDMI TMDS rates ROPLL alone mode should be used. For FRL 8Gbps rate, cascade mode needs to be used.
0x0224[1]	cmn_lcpll_alone_mode	0x0	0x0	0x0: Cascade mode/ROPLL mode 0x1: LCPLL alone mode. For FRL 8Gbps rate, cascade mode needs to be used. For FRL 10Gbps and 12Gbps, LCPLL alone mode should be used.
0x0204[3]	ana_pll_cd_tx_ser_rate_sel	0x0	0x0	0x0: For TMDS mode 0x1: For FRL mode
0x021C[3]	ana_pll_frl_mode_en	0x0	0x0	0x0: For TMDS mode 0x1: For FRL mode
0x0C6C[7:0]	ln0_ana_tx_reserved	0x0	0x1	Transmitter setting
0x106C[7:0]	ln1_ana_tx_reserved	0x0	0x1	Transmitter setting
0x014C[7:0]	ln2_ana_tx_reserved	0x0	0x1	Transmitter setting
0x018C[7:0]	ln3_ana_tx_reserved	0x0	0x1	Transmitter setting
0x0C58[3:0]	ln0_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1058[3:0]	ln1_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1458[3:0]	ln2_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1858[3:0]	ln3_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x0C40[1:0]	ln0_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1040[1:0]	ln1_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x1440[1:0]	ln2_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1840[1:0]	ln3_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x0208[3:0]	ana_pll_cd_vreg_gain_ctrl	0x0	0x4	PLL setting
0x00F0[7]	ana_lcpll_reserved[7]	0x0	0x1	PLL setting
0x020C[6:5]	ana_pll_cd_vreg_ictrl	0x1	0x1	PLL setting
0x0214[1:0]	ana_pll_sync_loss_det_mode	0x0	0x3	PLL setting
0x0210[5]	pll_lcro_clk_sel	0x0	0x1	PLL setting
0x0268[0]	hs_speed_sel	0x0	0x1	Clock setting of o_tx_hs_clk 0x0: Div20 clock output 0x1: Div10 clock output
0x026C[4]	ls_speed_sel	0x0	0x0	Clock setting of o_tx_link_sym_clk 0x0: Div40/Div36 clock output 0x1: Div20/Div18 clock output
0x0C44[3]	ln0_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x0C44[2]	ln0_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x0C44[1]	ln0_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x0C44[0]	ln0_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x1044[3]	ln1_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1044[2]	ln1_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1044[1]	ln1_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1044[0]	ln1_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x1444[3]	ln2_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1444[2]	ln2_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x1444[1]	ln2_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1444[0]	ln2_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x1844[3]	ln3_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1844[2]	ln3_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1844[1]	ln3_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1844[0]	ln3_tx_ser_40bit_en_hbr3	0x0	0x1	Transmitter setting
0x0C48[5]	ln0_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x0C48[4]	ln0_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x0C48[3]	ln0_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x0C48[2]	ln0_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[5]	ln1_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[4]	ln1_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[3]	ln1_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1048[2]	ln1_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[5]	ln2_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[4]	ln2_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[3]	ln2_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1448[2]	ln2_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[5]	ln3_tx_ser_rate_sel_rbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[4]	ln3_tx_ser_rate_sel_hbr	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[3]	ln3_tx_ser_rate_sel_hbr2	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode
0x1848[2]	ln3_tx_ser_rate_sel_hbr3	0x0	0x0	0x0: HDMI TMDS mode 0x1: HDMI FRL mode

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0804[7:0]	clk_user_pat_39_32	0x0	0x0	Clock pattern to be driven on the clock serial lanes. Bit 40 to 32.
0x0808[7:0]	clk_user_pat_31_24	0x0	0x0	Clock pattern to be driven on the clock serial lanes. Bit 31 to 24.
0x080C[7:0]	clk_user_pat_23_16	0x0	0x0F	Clock pattern to be driven on the clock serial lanes. Bit 23 to 16.
0x0810[7:0]	clk_user_pat_15_8	0x0	0xFF	Clock pattern to be driven on the clock serial lanes. Bit 15 to 8.
0x0814[7:0]	clk_user_pat_7_0	0x0	0xFF	Clock pattern to be driven on the clock serial lanes. Bit 7 to 0.
0x0C78[3]	ln0_hdmi_tmds_clk_lane_sel	0x0	0x0	0x0: Lane 0 drives the serial data 0x1: Lane 0 drives the clock pattern on serial lanes This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x1078[3]	ln1_hdmi_tmds_clk_lane_sel	0x0	0x0	0x0: Lane 1 drives the serial data 0x1: Lane 1 drives the clock pattern on serial lanes. This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x1478[3]	ln2_hdmi_tmds_clk_lane_sel	0x0	0x0	0x0: Lane 2 drives the serial data 0x1: Lane 2 drives the clock pattern on serial lanes This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x1878[3]	ln3_hdmi_tmds_clk_lane_sel	0x0	0x1	0x0: Lane 3 drives the serial data 0x1: Lane 3 drives the clock pattern on serial lanes This register should be set for only HDMI TMDS mode basing clock lane requirement.
0x0800[1]	hdmi_tmds_frl_sel	0x0	0x1	0x0: HDMI FRL mode 0x1: HDMI TMDS mode
0x0218[7:4]	ana_pll_pcg_postdiv_sel	0x1	0x1	PLL Setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0218[3:1]	ana_pll_pcg_clk_sel	0x0	0x0	PLL Setting
0x0218[0]	ana_pll_pcg_clk_en	0x0	0x1	0x0: Disables pixel clock generation 0x1: Enables pixel clock generation
0x081C[3:0]	lane_en	0x0	0xF	lane_en bit0: 0x0 – Disables the lane 0 0x1 – Enables the lane 0 lane_en bit1: 0x0 – Disables the lane 1 0x1 – Enables the lane 1 lane_en bit2: 0x0 – Disables the lane 2 0x1 – Enables the lane 2 lane_en bit3: 0x0 – Disables the lane 3 0x1 – Enables the lane 3 Only one lane can be disabled based on HDMI protocol, that too in FRL 3Gbps and 6Gbps rates only.

27.6.2 Programming Sequence for HDMI eARC mode operation

Below are the list registers to be configured to keep the sideband in eARC mode. The differential mode receive clk is available on o_earc_dmac_rxclk and data is availabel on o_earc_dmac_rxdata. The enable for differential mode receiver is i_earc_dmac_en. The common mode transmits enable is i_earc_tx_mode and receive enable i_earc_rx_mode. The input data for common mode transmit is i_aux_earc_txdata. The output data of common mode receivee is o_earc_cmdc_rxdata.

Table 27-6 Programming Sequence for HDMI eARC mode operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x025C[1]	dig_clk_sel	0x0	As Required	1'b0: Select LCPLL reference clock mux output (LCPLL alone mode and Cascade mode) 1'b1: Select ROPLL reference clock mux output (ROPLL alone mode)
0x044C[5:4]	sb_rx_rcal_opt_code	0x0	0x1	This is use to select finale rcal code after rcal enable goes low and rcal done goes high 00: o_rcal_code = tune_code 01: o_rcal_code = i_sfr_rcal_code 10: o_rcal_code = tune_code + i_sfr_rcal_code (i_sfr_sb_rx_rterm_ctrl) 11: o_rcal_code = tune_code i_sfr_rcal_code (i_sfr_sb_rx_rterm_ctrl)

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0470[3:0]	sb_afc_stb_num	0x0	0x4	OSC stable number for initial time... it use to configure number of times vco generate stable count to go for stable frequency comparison state
0x046C[3:0]	sb_afc_tol	0x0	0x3	OSC stable tolerance… This is the tolarance for vco count that can be taken to make sure vco generating stable frequency
0x0424[3:0]	ana_sb_dmrx_afc_div_ratio	0x0	0x5	This controls the post division after oscillator. 0, 6 and 7 are not valid codes. 1: divide by 16 2: divide by 8 3: divide by 4 4: divide by 2 5: divide by 1 (default)
0x0480[0]	sb_eARC_afc_en	0x0	0x1	0: AFC disable, 1: AFC enable
0x0480[1]	sb_eARC_en	0x0	0x1	Enable eARC mode for HDMI
0x046C[4]	sb_earc_sig_det_bypass	0x0	0x1	This sfr use to bypass signal detect logic
0x047C[7:2]	sb_pwm_afc_ctrl	0x0	0xC	This is the sfr which use for selecting pwm afc calibration code depending on its MSB MSB = 1 then MSB -1 to 0 bits value taken as calibration code for pwm afc MSB=0 then afc code is internally generated from afc module logic if AFC _EN =1
0x047C[1]	sb_rcal_rstn	0x0	0x1	Sideband resister calibration enable signal If 1'b0 resister calibration disable If 1'b1 resister calibration enable

0x0454[5:3]	sb_ready_delay_time	0x0	0x2	This sfr is the select line to set count count wrt refclock cycle to set sb ready signal after all calibration completed
				3'b000: delay_time = 9'd0; // 0
				3'b001: delay_time = 9'd13; // 0.5us
				for 25MHz refclk

SFR Address	SFR Name	Default Value	Setting Value	Description

				3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
				3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
				3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
				3'b101: delay_time = 9'd125; // 5us for 25MHz refclk
				3'b110: delay_time = 9'd250; // 10us
				for 25MHz refclk
				3'b111: delay_time = 9'd500; // 20us
				for 25MHz refclk
				default: delay_time = 9'd25; // 1us for 25MHz refclk

0x044C[3:0]	sb_rx_rterm_ctrl	0x0	0x3	This is the code to be added in the tune code to generate finale rcal code depends on the value of i_sfr_sb_rx_rcal_opt_code
0x0408[3:0]	ana_sb_rxterm_offsp	0x0	0x3	For i_sb_rescal_tune<2:0> = 3, the table for both OffsetP and N looks like 0000: 50 Ohms 0001: 48.4 Ohms 0011: 46.9 Ohms 0111: 45.5 Ohms 1111: 44.2 Ohms
0x040C[6:3]	ana_sb_rxterm_offsn	0x0	0x3	For i_sb_rescal_tune<2:0> = 3, the table for both OffsetP and N looks like 0000: 50 Ohms 0001: 48.4 Ohms 0011: 46.9 Ohms 0111: 45.5 Ohms 1111: 44.2 Ohms
0x0464[7:0]	sb_tg_cnt_run_no_7_0	0x0	0x3	This is the refclock count cycle during which rec clock counter run This count should be such that time duration with refclock good enough to get requird rec clock count (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <=

SFR Address	SFR Name	Default Value	Setting Value	Description
				(i_sfr_sb_tg_earc_dmrx_recvrd_clk_cn t* recover clock period)
0x0460[7:0]	sb_tg_earc_dmrx_recvrd_clk_cnt	0x0	0xA	This is the target count the rec clk should give for specifide refclock cycle This count should be 10, 20 or 40 (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cn t* recover clock period)
0x0478[7:0]	sb_tg_osc_cnt_max	0x0	0x5	This is the maximum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock Refclock: count required 24MHz: 8’d106 25MHz: 8’d 101 26MHz: 8’d 98 27MHz: 8’d 94 45MHz: 8’d 57 54MHz: 8’d 48
0x0474[7:0]	sb_tg_osc_cnt_min	0x0	0x3	This is the minimum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock Refclock: count required 24MHz: 8’d 103 25MHz: 8’d 99 26MHz: 8’d 95 27MHz: 8’d 92 45MHz: 8’d 55 54MHz: 8’d 46

0x045C[3:0]	sb_tg_pll_cd_vreg_fast_pulse_time	0x0	0x4	This sfr is the select line to set number of clock cycle for which vreg bypass signal going high
				4'b0000:tg_sb_pll_cd_vreg_fast_pulse_time =14'd25; // 1us 4'b0000:
				4'b0001:tg_sb_pll_cd_vreg_fast_pulse_time =14'd50; // 2us
				4'b0010:tg_sb_pll_cd_vreg_fast_pulse_time =14'd75; // 3us
				4'b0011:tg_sb_pll_cd_vreg_fast_pul

SFR Address	SFR Name	Default Value	Setting Value	Description

				se_time =14'd100; // 4us
				4'b0100:tg_sb_pll_cd_vreg_fast_pulse_time =14'd125; // 5us
				4'b0101:tg_sb_pll_cd_vreg_fast_pulse_time =14'd250; // 10us
				4'b0110:tg_sb_pll_cd_vreg_fast_pulse_time =14'd500; // 20us
				4'b0111:tg_sb_pll_cd_vreg_fast_pulse_time =14'd750; // 30us
				4'b1000:tg_sb_pll_cd_vreg_fast_pulse_time =14'd1000; // 40us
				4'b1001:tg_sb_pll_cd_vreg_fast_pulse_time =14'd1250; // 50us
				4'b1010:tg_sb_pll_cd_vreg_fast_pulse_time =14'd2500; // 100us
				4'b1011:tg_sb_pll_cd_vreg_fast_pulse_time =14'd3750; // 150us
				4'b1100:tg_sb_pll_cd_vreg_fast_pulse_time =14'd5000; // 200us
				4'b1101:tg_sb_pll_cd_vreg_fast_pulse_time =14'd7500; // 300us
				4'b1110:tg_sb_pll_cd_vreg_fast_pulse_time =14'd10000; // 400us
				4'b1111:tg_sb_pll_cd_vreg_fast_pulse_time =14'd12500; // 500us
				default:tg_sb_pll_cd_vreg_fast_pulse_time =14'd250;

0x0450[2:0]	sb_tg_rxterm_en_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to set rxterm
				enable after sb enable goes high
				3'b000: delay_time = 9'd0; // 0
				3'b001: delay_time = 9'd13; // 0.5us
				for 25MHz refclk
				3'b010: delay_time = 9'd25; // 1us
				for 25MHz refclk
				3'b011: delay_time = 9'd50; // 2us
				for 25MHz refclk
				3'b100: delay_time = 9'd75; // 3us
				for 25MHz refclk
				3'b101: delay_time = 9'd125; // 5us
				for 25MHz refclk
				3'b110: delay_time = 9'd250; // 10us

SFR Address	SFR Name	Default Value	Setting Value	Description

				for 25MHz refclk
				3'b111: delay_time = 9'd500; // 20us
				for 25MHz refclk
				default: delay_time = 9'd25; // 1us
				for 25MHz refclk

0x0450[5:3]	sb_tg_sb_en_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to set sb enable after rcal done goes high
				3'b000: delay_time = 9'd0; // 0
				3'b001: delay_time = 9'd13; // 0.5us
				for 25MHz refclk
				3'b010: delay_time = 9'd25; // 1us
				for 25MHz refclk
				3'b011: delay_time = 9'd50; // 2us
				for 25MHz refclk
				3'b100: delay_time = 9'd75; // 3us
				for 25MHz refclk
				3'b101: delay_time = 9'd125; // 5us
				for 25MHz refclk
				3'b110: delay_time = 9'd250; // 10us
				for 25MHz refclk
				3'b111: delay_time = 9'd500; // 20us
				for 25MHz refclk
				default: delay_time = 9'd25; // 1us
				for 25MHz refclk

0x0414[2:0]	ana_sb_tx_hlvl_prog	0x0	0x7	This controls the voltage buffer in/out high value. 000: 480mV 001: 490mV 010: 515mV 011: 535mV 100: 560mV 101: 580mV 110: 600mV 111:623mV
0x0418[6:4]	ana_sb_tx_llvl_prog	0x0	0x7	This controls the voltage buffer in/out low value. 000: 320mV 001: 310mV

SFR Address	SFR Name	Default Value	Setting Value	Description
				010: 285mV 011: 260mV 100: 240mV 101: 220mV 110: 200mV 111: 180mV
0x043C[3:0]	ana_sb_vreg_gain_ctrl	0x1	0x0	Controls the feedback gain of the LDO. 0: 1.00 1: 1.03 2: 1.04 3: 1.05 4: 1.06 5: 1.09 6. 1.12 7: 1.15
0x0440[0]	ana_sb_vreg_ref_sel	0x0	0x1	Used as power saving mode

0x0454[2:0]	sb_tg_osc_en_delay_time	0x0	0x2	This sfr is the select line to set count count wrt refclock cycle to set oscillator enable after vreg sequence completed
				3'b000: delay_time = 9'd0; // 0
				3'b001: delay_time = 9'd13; // 0.5us
				for 25MHz refclk
				3'b010: delay_time = 9'd25; // 1us
				for 25MHz refclk
				3'b011: delay_time = 9'd50; // 2us
				for 25MHz refclk
				3'b100: delay_time = 9'd75; // 3us
				for 25MHz refclk
				3'b101: delay_time = 9'd125; // 5us
				for 25MHz refclk
				3'b110: delay_time = 9'd250; // 10us
				for 25MHz refclk
				3'b111: delay_time = 9'd500; // 20us
				for 25MHz refclk
				default: delay_time = 9'd25; // 1us
				for 25MHz refclk

0x0458[6:4]	sb_tg_osc_en_to_afc_rstn_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to release reset to afc calibration module after oscillator

SFR Address	SFR Name	Default Value	Setting Value	Description

				osc enable signal seting.
				3'b000: delay_time = 9'd0; // 0
				3'b001: delay_time = 9'd13; // 0.5us
				for 25MHz refclk
				3'b010: delay_time = 9'd25; // 1us for 25MHz refclk
				3'b011: delay_time = 9'd50; // 2us for 25MHz refclk
				3'b100: delay_time = 9'd75; // 3us for 25MHz refclk
				3'b101: delay_time = 9'd125; // 5us forc25MHz refclk
				3'b110: delay_time = 9'd250; // 10us
				for 25MHz refclk
				3'b111: delay_time = 9'd500; // 20us
				for 25MHz refclk
				default: delay_time = 9'd25; // 1us for 25MHz refclk

0x0424[3:0]	ana_sb_dmrx_afc_div_ratio	0x0	0x5	This controls the post division after oscillator. 0, 6 and 7 are not valid codes. 1: divide by 16 2: divide by 8 3: divide by 4 4: divide by 2 5: divide by 1 (default)
0x040C[1]	ovrd_sb_rx_rescal_done	0x0	0x1	Enable SFR override for rescal done
0x0410[5]	ovrd_sb_en	0x0	0x1	Enable SFR override for sideband enable
0x0408[5]	ovrd_sb_rxter_en	0x0	0x1	Enable SFR override for sideband rx termination enable
0x0414[6]	ovrd_sb_earc_cmdc_en	0x0	0x1	Enable SFR override for sideband eARC CMDC mode enable
0x043C[7]	ovrd_sb_vreg_en	0x0	0x1	Enable SFR override for sideband vreg enable
0x043C[5]	ovrd_sb_vreg_lpf_bypass	0x0	0x1	Enable SFR override for sideband vreg LPF bypass pulse
0x043C[5]	ovrd_sb_vreg_lpf_bypass	0x0	0x1	Enable SFR override for sideband vreg LPF bypass pulse
0x048C[5]	ovrd_sb_ready	0x0	0x1	Enable SFR override for sideband ready

SFR Address	SFR Name	Default Value	Setting Value	Description
Bring up Bias/BGR, deassert init_rstn, cmn_rstn if not done already and wait for 1000us				
0x040C[0]	sb_rx_rescal_done	0x0	0x1	SFR override value for rescal done
Wait for 50us				
0x0410[4]	sb_rxterm_en	0x0	0x1	SFR override value for sideband rx termination enable
Wait for 50us				
0x0408[4]	sb_rxterm_en	0x0	0x1	SFR override value for sideband rx termination enable
Wait for 50us				
0x0414[5]	sb_earc_cmdc_en	0x0	0x1	SFR override value for sideband eARC CMDC mode enable
0x043C[6]	sb_vreg_en	0x0	0x1	SFR override value for sideband vreg enable
Wait for 50us				
0x043C[4]	sb_vreg_lpf_bypass	0x0	0x1	SFR override value for sideband vreg LPF bypass pulse
Wait for 250us				
0x043C[4]	sb_vreg_lpf_bypass	0x0	0x0	SFR override value for sideband vreg LPF bypass pulse
Wait for 100us				
0x048C[4]	sb_ready	0x0	0x1	SFR override value for sideband ready

27.6.3 EDP TX PHY Application

"SFR Address" in the tables below means that Comb TX PHY's address.

27.6.3.1 Start-Up Sequence for PHY

The Power-Up sequence as the table below.

Table 27-7 Programming Sequence for DP Start-Up operation

Power-Up Sequence
Power up and clock is valid
Reset PHY and reset init_rstn, cmn_rstn and lane_rstn by writing PMU1CRU_SOFTRST_CON03[15]=1'b1, PMU1CRU_SOFTRST_CON04[0]=1'b1, PMU1CRU_SOFTRST_CON04[1]=1'b1
Release APB reset of PHY
Write internal registers thought APB. Configure AUX and Main Link register in this stage. Detail configuration can be found in the following chapters.
Write HDPTXPHY_GRF_CON0[6:5]=2'b11, bias_en=1, bgr_en=1
Wait 10us
Write PMU1CRU_SOFTRST_CON03[15]=1'b0, release init_rstn
Wait 10us
Write HDPTXPHY_GRF_CON0[7]=1'b1, pll_en=1
Wait 10us
PMU1CRU_SOFTRST_CON04[0]=1'b0, release cmn_rstn

Power-Up Sequence
Wait o_pll_lock_done, read <HDPTXPHY_GRF_STATUS0> (Please see HDPTXPHY_GRF for base and offset address) until bit3 o_pll_lock_done=1.
Wait 10us
PMU1CRU_SOFTRST_CON04[1]=1'b0, release lane_rstn
Wait o_phy_rdy, read <HDPTXPHY_GRF_STATUS0> until bit1 o_phy_rdy=1.
The PHY's configuration is ready, the controller can send data.

27.6.3.2 PHY AUX Setting

Below are the registers to be configured to bring up sideband in aux mode. Please set AUX as the sequence in the table below.

Table 27-8 Programming Sequence for DP AUX mode operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0x044C[5:4]	sb_rx_rcal_opt_code	0x0	0x1	This is use to select finale rcal code after rcal enable goes low and rcal done goes high 2'b00: o_rcal_code = tune_code 2'b01: o_rcal_code = i_sfr_rcal_code 2'b10: o_rcal_code = tune_code + i_sfr_rcal_code (i_sfr_sb_rx_rterm_ctrl) 2'b11: o_rcal_code = tune_code - i_sfr_rcal_code (i_sfr_sb_rx_rterm_ctrl)
0x044C[3:0]	sb_rx_rterm_ctrl	0x0	0x3	This is the code to be added in the tune code to generate finale rcal code depends on the value of i_sfr_sb_rx_rcal_opt_code
0x0450[5:3]	sb_tg_sb_en_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to set sb enable after rcal done goes high 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500;

SFR Address	SFR Name	Default Value	Setting Value	Description
				20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x0450[2:0]	sb_tg_rxterm_en_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to set rxterm enable after sb enable goes high 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x0454[5:3]	sb_ready_delay_time	0x0	0x2	This sfr is the select line to set count count wrt refclock cycle to set sb ready signal after all calibration completed 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25;

SFR Address	SFR Name	Default Value	Setting Value	Description
				1us for 25MHz refclk
0x0454[2:0]	sb_tg_osc_en_delay_time	0x0	0x2	This sfr is the select line to set count count wrt refclock cycle to set oscillator enable after vreg sequence completed 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk
0x0458[6:4]	sb_tg_osc_en_to_afc_rstn_delay_time	0x0	0x2	This sfr is the select line to set count wrt refclock cycle to release reset to afc calibration module after oscillator osc enable signal set. 3'b000: delay_time = 9'd0; 0us for 25MHz refclk 3'b001: delay_time = 9'd13; 0.5us for 25MHz refclk 3'b010: delay_time = 9'd25; 1us for 25MHz refclk 3'b011: delay_time = 9'd50; 2us for 25MHz refclk 3'b100: delay_time = 9'd75; 3us for 25MHz refclk 3'b101: delay_time = 9'd125; 5us for 25MHz refclk 3'b110: delay_time = 9'd250; 10us for 25MHz refclk 3'b111: delay_time = 9'd500; 20us for 25MHz refclk default: delay_time = 9'd25; 1us for 25MHz refclk

SFR Address	SFR Name	Default Value	Setting Value	Description

0x045C[3:0]	sb_tg_pll_cd_vreg_fast_pulse_time	0x0	0x4	This sfr is the select line to set number of clock cycle for which vreg bypass signal go high
				4'b0000:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd25;
				1us for 25MHz refclk
				4'b0001:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd50;
				2us for 25MHz refclk
				4'b0010:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd75;
				3us for 25MHz refclk
				4'b0011:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd100;
				4us for 25MHz refclk
				4'b0100:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd125;
				5us for 25MHz refclk
				4'b0101:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;
				10us for 25MHz refclk
				4'b0110:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd500;
				20us for 25MHz refclk
				4'b0111:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd750;
				30us for 25MHz refclk
				4'b1000:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1000;
				40us for 25MHz refclk
				4'b1001:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd1250;
				50us for 25MHz refclk
				4'b1010:

SFR Address	SFR Name	Default Value	Setting Value	Description

				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd2500;
				100us for 25MHz refclk
				4'b1011:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd3750;
				150us for 25MHz refclk
				4'b1100:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd5000;
				200us for 25MHz refclk
				4'b1101:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd7500;
				300us for 25MHz refclk
				4'b1110:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd10000;
				400us for 25MHz refclk
				4'b1111:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd12500;
				500us for 25MHz refclk
				default:
				tg_sb_pll_cd_vreg_fast_pulse_time = 14'd250;

0x0460[7:0]	sb_tg_earc_dmrx_recvrd_clk_cnt	0x0	0xA	This is the target count the rec clk should give for specifide refclock cycle This count should be 10, 20 or 40 (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period
0x0464[7:0]	sb_tg_cnt_run_no_7_0	0x0	0x3	This is the refclock count cycle during which rec clock counter run This count should be such that time duration with refclock good enough to get requird rec clock count (i_sfr_sb_tg_cnt_run_no * reference clock cycle period) <= (i_sfr_sb_tg_earc_dmrx_recvrd_clk_cnt* recover clock period)

SFR Address	SFR Name	Default Value	Setting Value	Description
0x046C[4]	sb_earc_sig_det_bypass	0x0	0x1	This sfr use to bypass signal detect logic
0x046C[3:0]	sb_afc_tol	0x0	0x3	OSC stable tolerance. This is the tolarance for vco count that can be taken to make sure vco generating stable frequency
0x0470[3:0]	sb_afc_stb_num	0x0	0x4	OSC stable number for initial time.it use to configure number of times vco generate stable count to go for stable frequency comparison state
0x0474[7:0]	sb_tg_osc_cnt_min	0x0	0x67	This is the minimum target count from vco to be received for one ref clock cycle to to get 2.5GHz PLL clock Refclock: count required 24MHz: 8’d103 25MHz: 8’d99 26MHz: 8’d95 27MHz: 8’d92 45MHz: 8’d55 54MHz: 8’d46
0x0478[7:0]	sb_tg_osc_cnt_max	0x0	0x6A	This is the maximum target count from vco to be received for one ref clock cycle to to get 2.5GHz pll clock Refclock: count required 24MHz: 8’d106 25MHz: 8’d101 26MHz: 8’d98 27MHz: 8’d94 45MHz: 8’d57 54MHz: 8’d48
0x047C[7:2]	sb_pwm_afc_ctrl	0x0	0x5	This is the sfr which use for selecting pwm afc calibration code depending on its MSB MSB = 1 then MSB-1 to 0 bits value taken as calibration code for pwm afc MSB = 0 then afc code is internally generated from afc module logic if AFC _EN =1
0x0434[4]	ana_sb_dmrx_lpbk_data	0x0	0x1	The loopback data from register; the duty cycle of the data have to be more than 53% or less than 47%.

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0440[1]	ana_sb_vreg_out_sel	0x0	0x1	It bypasses the LDO with VDD.
0x0440[0]	ana_sb_vreg_ref_sel	0x0	0x1	Used as power saving mode
0x043C[3:0]	ana_sb_vreg_gain_ctrl	0x1	0x0	Controls the feedback gain of the LDO. 4’b0000: 1.00 4’b0001: 1.03 4’b0010: 1.04 4’b0011: 1.05 4’b0100: 1.06 4’b0101: 1.09 4’b0110: 1.12 4’b0111: 1.15
0x0408[3:0]	ana_sb_rxterm_offsp	0x0	0x3	For i_sb_rescal_tune<2:0> = 3, the table for both OffsetP and N looks like 4’b0000: 50 Ohms 4’b0001: 48.4 Ohms 4’b0011: 46.9 Ohms 4’b0111: 45.5 Ohms 4’b1111: 44.2 Ohms
0x040C[6:3]	ana_sb_rxterm_offsn	0x0	0x3	For i_sb_rescal_tune<2:0> = 3, the table for both OffsetP and N looks like 4’b0000: 50 Ohms 4’b0001: 48.4 Ohms 4’b0011: 46.9 Ohms 4’b0111: 45.5 Ohms 4’b1111: 44.2 Ohms
0x047C[1]	sb_rcal_rstn	0x0	0x1	Sideband resister calibration enable signal If 1'b0 resister calibration disable If 1'b1 resister calibration enable
0x0410[0]	sb_aux_en	0x0	0x1	AUX Enable This is ovrd for sb_aux_en_in 1’b0: Disable 1’b1: Enable
0x0480[7]	sb_aux_en_in	0x0	0x1	AUX Enable 1’b0: Disable 1’b1: Enable
0x040C[1]	ovrd_sb_rx_rescal_done	0x0	0x1	Enable SFR override for rescal done
0x0410[5]	ovrd_sb_en	0x0	0x1	Enable SFR override for sideband enable

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0408[5]	ovrd_sb_rxterm_en	0x0	0x1	Enable SFR override for sideband rx termination enable
0x043C[7]	ovrd_sb_vreg_en	0x0	0x1	Enable SFR override for sideband vreg enable
0x0410[1]	ovrd_sb_aux_en	0x0	0x1	Enable SFR override for sideband aux enable
0x048C[5]	ovrd_sb_ready	0x0	0x1	Enable SFR override for sideband ready
Bring up Bias/BGR, deassert init_rstn, cmn_rstn if not done already and wait for 1000us				
0x040C[0]	sb_rx_rescal_done	0x0	0x1	SFR override value for rescal done
Wat for 100us				
0x0410[4]	sb_en	0x0	0x1	SFR override value for sideband enable
Wait for 100us				
0x0408[4]	sb_rxterm_en	0x0	0x1	SFR override value for sideband rx termination enable
Wait for 10us				
0x043C[6]	sb_vreg_en	0x0	0x1	SFR override value for sideband vreg enable
Wait for 10us				
0x0410[0]	sb_aux_en	0x0	0x1	SFR override value for sideband aux enable
Wait for 100us				
0x048C[4]	sb_ready	0x0	0x1	

27.6.3.3 PHY Main Link Setting

Below are the registers to be configured to set RBR/HBR/HBR2 rates. Please set link rate as the sequence in the table below. For the different setting of RBR/HBR/HBR2 rates and 1/2/4 lane, please see the table below.

Table 27-9 DP mode Setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0800[2]	protocol_sel	0x0	0x0	DP mode
0x025C[1]	dig_clk_sel	0x0	0x1	1'b0: Select LCPLL reference clock mux output (LCPLL alone mode and Cascade mode) 1'b1: Select ROPLL reference clock mux output (ROPLL alone mode)

if RBR:
<0x0144> = 0x87, <0x0154>=0x87, <0x0168>=0x33
<0x0180> = 0x21, <0x0190>=0x07, <0x0194> = 0x00
<0x01b0> = 0x03, <0x01c0>=0x08
else if HBR:
<0x0148> = 0x71, <0x0158>=0x71, <0x0168> = 0x31				

SFR Address	SFR Name	Default Value	Setting Value	Description
<0x0184> = 0x27, <0x0190>=0x0f, <0x0198> = 0x0d <0x01b4> = 0x07, <0x01c4>=0x18 else if HBR2: <0x014c> = 0x71, <0x015c> = 0x71, <0x016c> = 0x03 <0x0188> = 0x27, <0x0190> = 0x0f, <0x019c> = 0x0d <0x01b8> = 0x07, <0x01c8> = 0x18				
0x0C28[4]	ln0_ana_tx_jeq_en	0x0	0x1	Transmitter Setting
0x1028[4]	ln1_ana_tx_jeq_en	0x0	0x1	Transmitter Setting
0x1428[4]	ln2_ana_tx_jeq_en	0x0	0x1	Transmitter Setting
0x1828[4]	ln3_ana_tx_jeq_en	0x0	0x1	Transmitter Setting
0x0C28[3:0]	ln0_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x0C2C[7:4]	ln0_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x0C2C[3:0]	ln0_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1028[3:0]	ln1_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x102C[7:4]	ln1_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x102C[3:0]	ln1_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1428[3:0]	ln2_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x142C[7:4]	ln2_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x142C[3:0]	ln2_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1828[3:0]	ln3_tx_jeq_even_ctrl_rbr	0x0	0x7	Transmitter Setting
0x182C[7:4]	ln3_tx_jeq_even_ctrl_hbr	0x0	0x7	Transmitter Setting
0x182C[3:0]	ln3_tx_jeq_even_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x0C30[3:0]	ln0_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0C34[7:4]	ln0_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x0C34[3:0]	ln0_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1030[3:0]	ln1_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting
0x1034[7:4]	ln1_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x1034[3:0]	ln1_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1430[3:0]	ln2_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting
0x1434[7:4]	ln2_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x1434[3:0]	ln2_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x1830[3:0]	ln3_tx_jeq_odd_ctrl_rbr	0x0	0x7	Transmitter Setting
0x1834[7:4]	ln3_tx_jeq_odd_ctrl_hbr	0x0	0x7	Transmitter Setting
0x1834[3:0]	ln3_tx_jeq_odd_ctrl_hbr2	0x0	0x7	Transmitter Setting
0x0C0C[4:0]	ln0_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x100C[4:0]	ln1_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x140C[4:0]	ln2_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x180C[4:0]	ln3_tx_drv_lvl_ctrl	0x0	0xC	Transmitter Setting
0x0C1C[6]	ln0_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting
0x101C[6]	ln1_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting
0x141C[6]	ln2_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting
0x181C[6]	ln3_ana_tx_drv_accdrv_pol_sel	0x0	0x1	Transmitter Setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x0C1C[5:3]	ln0_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x101C[5:3]	ln1_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x141C[5:3]	ln2_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x181C[5:3]	ln3_ana_tx_drv_accdrv_ctrl	0x0	0x4	Transmitter Setting
0x021C[2]	ana_pll_tx_hs_clk_en	0x0	0x1	PLL setting
0x0204[0]	ana_pll_cd_hsclk_east_en	0x0	0x1	PLL setting
0x0204[1]	ana_pll_cd_hsclk_west_en	0x0	0x0	PLL setting
0x0818[2:1]	data_bus_width	0x0	0x1	2’b00: 18 bit data bus (for HDMI FRL mode only) 2’b01: 20 bit data bus 2’b10: 36 bit data bus (for HDMI FRL mode only) 2’b11: 40 bit data bus
0x0818[0]	bus_width_sel	0x0	0x0	1’b0: 20 bit data bus 1’b1: 40 bit data bus
0x0254[1:0]	dp_tx_link_bw	0x0	0x0 or 0x1 or 0x2	Multiplexes the register settings for analog blocks. 2’b00: RBR register settings applied to analog (*_rbr registers) 2’b01: HBR register settings applied to analog (*_hbr registers) 2’b10: HBR2 register settings applied to analog (*_hbr2 registers) This register is set differently when work in different rates.
0x0264[2]	cmn_ropll_alone_mode	0x0	0x1	1’b0: Cascade mode/LCPLL mode 1’b1: ROPLL alone mode ROPLL alone mode should be used for RBR, HBR and HBR2 modes.
0x0C6C[7:0]	ln0_ana_tx_reserved	0x0	0x1	Transmitter setting
0x106C[7:0]	ln1_ana_tx_reserved	0x0	0x1	Transmitter setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x014C[7:0]	ln2_ana_tx_reserved	0x0	0x1	Transmitter setting
0x018C[7:0]	ln3_ana_tx_reserved	0x0	0x1	Transmitter setting
0x0C58[3:0]	ln0_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1058[3:0]	ln1_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1458[3:0]	ln2_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x1858[3:0]	ln3_ana_tx_ser_vreg_gain_ctrl	0x0	0x2	Transmitter setting
0x0C40[1:0]	ln0_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1040[1:0]	ln1_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1440[1:0]	ln2_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x1840[1:0]	ln3_ana_tx_sync_loss_det_mode	0x0	0x3	Transmitter setting
0x0208[3:0]	ana_pll_cd_vreg_gain_ctrl	0x0	0x4	PLL setting
0x00F0[7]	ana_lcpll_reserved[7]	0x0	0x1	PLL setting
0x020C[6:5]	ana_pll_cd_vreg_ictrl	0x1	0x1	PLL setting
0x0214[1:0]	ana_pll_sync_loss_det_mode	0x0	0x3	PLL setting
0x0210[5]	pll_lcro_clk_sel	0x0	0x1	PLL setting
0x0268[0]	hs_speed_sel	0x0	0x1	Clock setting of o_tx_hs_clk 1’b0: Div20 clock output 1’b1: Div10 clock output
0x026C[4]	ls_speed_sel	0x0	0x1	Clock setting of o_tx_link_sym_clk 1’b0: Div40/Div36 clock output

SFR Address	SFR Name	Default Value	Setting Value	Description
				1'b1: Div20/Div18 clock output
0x0C44[3]	ln0_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x0C44[2]	ln0_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x0C44[1]	ln0_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1044[3]	ln1_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1044[2]	ln1_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1044[1]	ln1_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1444[3]	ln2_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1444[2]	ln2_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1444[1]	ln2_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x1844[3]	ln3_tx_ser_40bit_en_rbr	0x0	0x1	Transmitter setting
0x1844[2]	ln3_tx_ser_40bit_en_hbr	0x0	0x1	Transmitter setting
0x1844[1]	ln3_tx_ser_40bit_en_hbr2	0x0	0x1	Transmitter setting
0x0264[7:6]	ssc_en	0x0	0x2	PLL Setting
0x081C[3:0]	lane_en	0x0	0xF or 0x3 or 0x1	lane_en[0]: 1'b0: Disables lane 0 1'b1: Enables lane 0 lane_en[1]: 1'b0: Disables lane 1 1'b1: Enables lane 1 lane_en[2]: 1'b0: Disables lane 2 1'b1: Enables lane 2 lane_en[3]: 1'b0: Disables lane 3 1'b1: Enables lane 3

27.6.3.4 PHY Power-Off Setting

Bring down all the PHY enables and assert the PHY resets.

Table 27-10 Power-Off setting

SFR Address	SFR Name	Default Value	Setting Value	Description
0x081C[3:0]	lane_en	0x0	0x0	lane_en[0]:

SFR Address	SFR Name	Default Value	Setting Value	Description
				1'b0: Disables lane 0 1'b1: Enables lane 0 lane_en[1]: 1'b0: Disables lane 1 1'b1: Enables lane 1 lane_en[2]: 1'b0: Disables lane 2 1'b1: Enables lane 2 lane_en[3]: 1'b0: Disables lane 3 1'b1: Enables lane 3
0x027C[7:6]	pcs_bias_en pcs_init_rstn pcs_cmn_rstn pcs_lane_rstn	0x0	0xaa	Disable bias, init, cmn and lane rstn
0x0280[6:5]	pcs_pll_en	0x0	0x2	Disable PLL
Assert APB reset				

27.6.3.5 PHY Change Setting Flow

For RBR/HBR/HBR2 rates, the registers 0x0254[1:0], 0x0144, 0x0148, 0x014c, 0x0154, 0x0158, 0x015c, 0x0168, 0x016c, 0x0180, 0x0184, 0x0188, 0x0190, 0x0194, 0x0198, 0x019c, 0x01b0, 0x01b4, 0x01b8, 0x01c0, 0x01c4, 0x01c8 should be set correctly. For 1/2/4 lane, the registers 0x081C[3:0] should be set correctly. All the register above can be seen in chapter PHY Main Link Setting. Please look for it for the details.

If want to change PHY's setting, please power down the PHY according to chapter PHY Power-Off Setting. After PHY is power-off, change the SFR settings and bring up PHY as chapter Start-Up Sequence for PHY.

27.6.3.6 PHY Voltage-Swing and Pre-Emphasis setting

The Voltage-Swing and Pre-Emphasis can be adjusted in this table.

Table 27-11 Voltage Swing and Pre-emphasis Level

	Pre-emphasis level 0	**Pre-emphasis level1**	**Pre-emphasis level 2**	**Pre-emphasis level 3**
Voltage swing level 0	lane_reg0303=0x22 lane_reg0304=0x10	lane_reg0303=0x25 lane_reg0304=0x13	lane_reg0303=0x29 lane_reg0304=0x17	lane_reg0303=0x2d lane_reg0304=0x1c
Voltage swing level 1	lane_reg0303=0x25 lane_reg0304=0x10	lane_reg0303=0x2a lane_reg0304=0x15	lane_reg0303=0x2d lane_reg0304=0x19	Not supported
Voltage swing level 2	lane_reg0303=0x28 lane_reg0304=0x10	lane_reg0303=0x2d lane_reg0304=0x16	Not supported	Not supported
Voltage swing level 3	lane_reg0303=0x2d lane_reg0304=0x10	Not supported	Not supported	Not supported

Chapter 28 HDMI RX PHY

28.1 Overview

HDMI RX PHY supports the following features:

- Single-port HDMI 2.0 RX PHY, 4 lanes, no sideband channels
- Data rate support in HDMI 2.0 mode
  - 6Gbps down to 3.4Gbps
- Data rate support in HDMI 1.4 mode
  - 3.4Gbps down to 250Mbps
- True-color (24 bit) and deep-color (30) color resolution modes
- Up to 4k at 30/50/60/120 Hz HDTV display resolutions
- Input clock
  - Wide range of discrete input reference clock (100, 54, 50, 48, 27, 25, 24MHz)
  - 85-150MHz input clock from TMDSCLK lane for HDMI 2.0 operation
  - 25-340MHz input clock from TMDSCLK lane for HDMI 1.4 operation
- Custom LDO: 3.3V to 1.8V
- Flip-chip package support
- Poly-orientation: North-South Orientation
- Internal Built-in Self-Test (BIST) for production testing
- JTAG interface for configuration
- IO continuity test included
- Includes analog embedded IO
- 3.3V termination included internally on HDMI 2.0 RX PHY
- No 5V stress support targeted
- Adaptive and configurable RX CTLE and DFE
  - Automatic equalization
- Support to HDMI 2.0 CTS

28.2 Block Diagram

HDMI_RX PHY has two main sub_block: Protocol Coding Sublayer (PCS) and Physical Media Attachment (PMA). HDMI_RX PHY block diagram is shown below.

Each lane module (raw_pcs_lane) contains Finite State Machines (FSM) to execute the power-up calibration and run-time adaptation algorithms. The algorithms are stored in a register bank located in a common module (raw_pcs_cmn). The design includes two register access arbiters. The memory arbiter is used for accessing the register bank whereas the control register arbiter is used to access all other registers in the PCS and the PMA. This mechanism provides efficient use of the registers and state machines within each lane where each lane can independently execute a different portion of the algorithm while reducing the register access bottleneck. All control registers in the PCS and PMA can be externally accessed using JTAG or CR parallel interfaces, with only one interface at any given time.

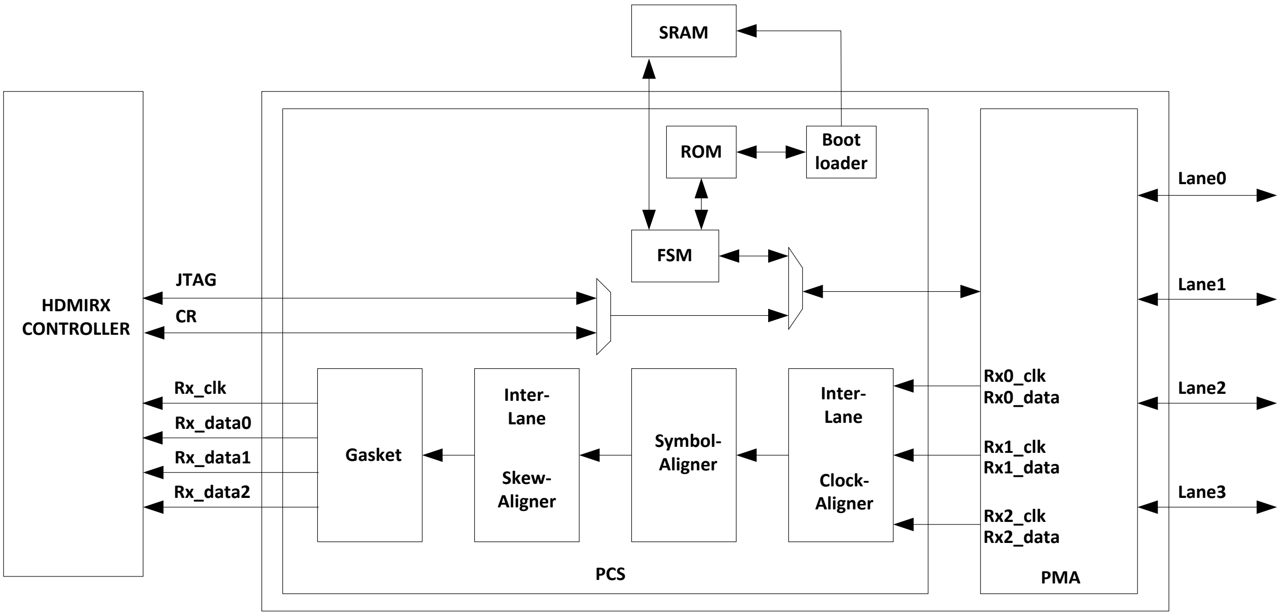

Fig. 28-1 HDMI_RX PHY diagram

HDMI_RX PHY PMA block diagram is shown below.

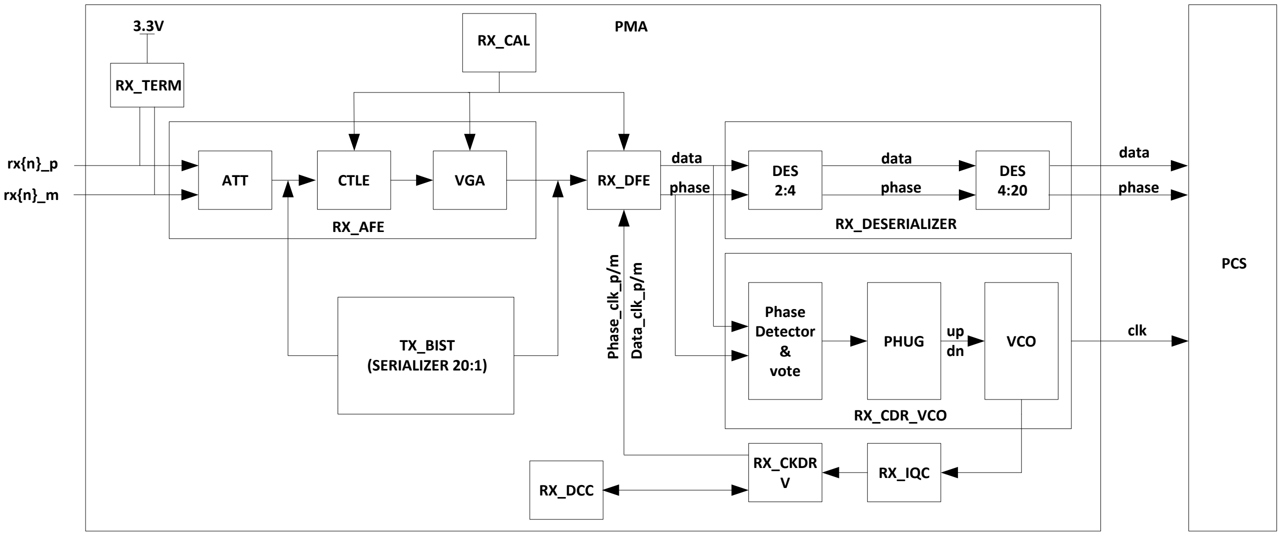

Fig. 28-2 HDMI_RX PHY single lane PMA diagram

The PMA receives differential serial data from a pair of external pads. Receiver characteristics, such as equalization and termination, are user-controllable. A continuous-time linear equalizer (CTLE) is first used to compensate for channel loss. A decision feedback equalizer (DFE) is also implemented after the CTLE to further equalize the signal for high-speed data rates. A clock and data recovery (CDR) circuit is implemented, which recovers the clock from the data. A dedicated VCO is implemented as the source of the recovering clock. The CDR loop adjusts the VCO clock frequency and phase until the frequency matches incoming data and the phase is aligned with incoming data. This recovered clock is used to retime received data and send it to the deserializer, which produces parallel data and a parallel data clock for the relevant PCS lane.

28.3 Function Description

HDMI_RX PHY has two main sub_block: Protocol Coding Sublayer (PCS) and Physical Media Attachment (PMA).

28.3.1 RX AFE

The analog front end (AFE) circuitry receives and terminates off-chip data signal, controls the signal level, and equalizes the signal by way of a linear equalizer. The AFE comprises three major blocks: the termination, an attenuator, and a CTLE VGA. The termination block is a programmable resistance that provides a constant 50 Ω termination over corners. The attenuator and VGA is responsible for attenuating the incoming signal to acceptable levels so the CTLE and DFE can maintain linearity in the case of short link. The CTLE provides high-

frequency signal boosting from 0dB to 12dB, along with programmable gain.
(1) Termination(TERM)
The TERM block is tuned to 50 Ω by the PHY using an off-chip reference resistor. The termination is fixed to AC coupled mode termination, and in this mode there is a single-ended 50 Ω termination to ground on each of RXP and RXM.
(2) Attenuator(ATT)
The ATT block is responsible for attenuating the incoming signal to acceptable levels in order that the subsequent CTLE and DFE circuits maintain linearity over all channels. Attenuation is controlled by the two MSBs of rxX_eq_afe_gain[3:0](X=0, 1, 2, 3).
(3) Continuous time-linear equalizer(CTLE)
The CTLE block provides high-frequency boost used to equalize the frequency dependent loss in a channel. The CTLE block has programmable boost level and gain provided by rxX_eq_ctle_boost[4:0] and the two LSBs of rxX_eq_afe_gain[3:0](X=0, 1, 2, 3).

28.3.2 RX DFE

The second equalizer in the RX is the Decision Feedback Equalizer (DFE). The output of the AFE is sent to a 2-tap adaptive DFE, which incorporates offset-compensated samplers. The output of the DFE is deserialized and sent to the core along with the recovered clock.
The DFE can be disabled by the following control signals:
(1) The rxX_ana_adaptation_en signal
(2) The LANEN_DIG_ANA_RX_CTL_OVRD_OUT.RX_ANA_ADAPTATION_EN register bit can be de-asserted to disable DFE adaptation. In this case, the DFE error-sampling path and related clock path are all disabled to save power.
(3) The LANEN_DIG_ANA_RX_CTL_OVRD_OUT.RX_ANA_DFE_TAPS_EN register bit can be used to reset the DFE taps to 1’b0 and, therefore, disable the DFE functionality.

28.3.3 RX CDR

The clock and data recovery (CDR) circuit is implemented as a second-order digital loop. The loop includes a proportional path and an integral path. To reduce proportional path latency, the proportional path is implemented separately from the integral path, with much higher speed. The proportional path and integral path outputs control a dedicated voltage-controlled oscillator (VCO), which generates an RX clock aligned with incoming data. CDR is shown in figure below.

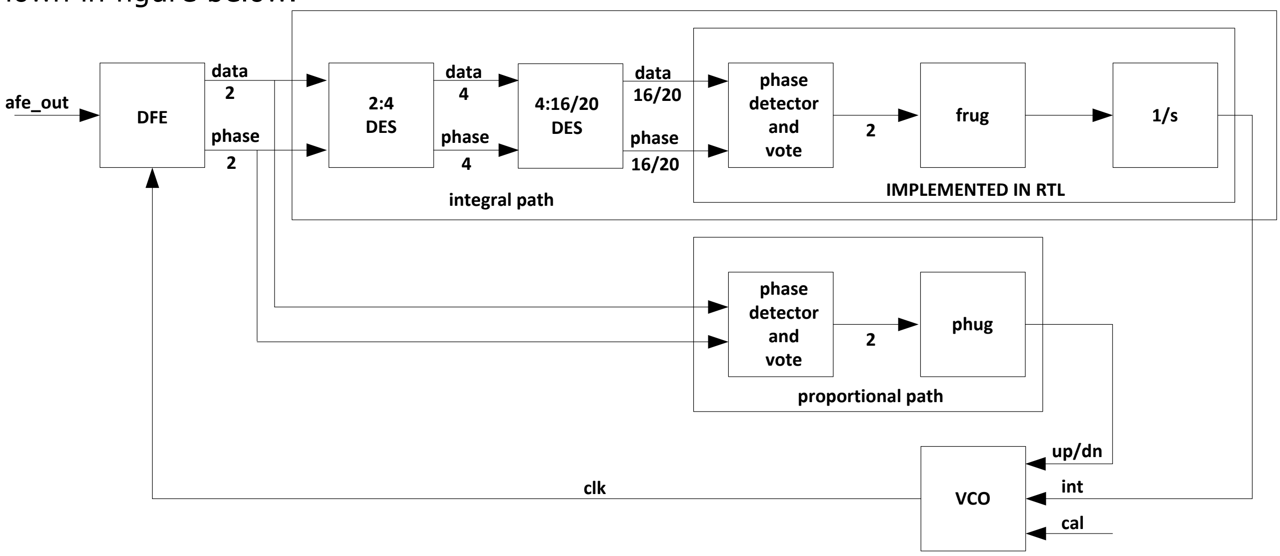

Fig. 28-3 HDMI_RX PHY CDR diagram

28.3.4 RX Deserialization

The deserializer converts serial data from RX and sends the data to the Soft IP as parallel data. The deserializer qualifies serial input data from the AFE using the high-speed serial recovered clock, and deserializes the data using the low-speed parallel recovered clock. The deserializer forwards the deserialized data to the receiver's Soft IP channel. The deserializer supports a 20 bit interface.

28.3.5 RX Internal Eye Monitor

Provided with the PHY is an internal eye monitor, which can provide data to produce a plot of time and voltage axis using internal DFT hooks built into the AFE. The eye monitor is non-destructive and can be run in parallel with live traffic. This procedure can be used to characterize the input RX eye margin as seen after the ATT and CTLE.

28.3.6 RX Equalization and Adaptation

The PHY supports receiver equalization, adaptation of receiver equalization parameters, and requests for updating Source side TxFFE settings. The PHY adapts RX AFE parameters, DFE coefficients, and remote TX equalization in two steps—startup adaptation and mission mode adaptation.

(1) startup adaptation

Startup adaptation starts when the RX is powered up with data received and with CDR locked. First, AFE gain, including ATT and GAIN parameters, are adapted based on a measurement of the average eye opening. Then, the CTLE BOOST is adapted using correlations. After CTLE is adapted, DFE tap coefficients are adapted using correlations.

(2) mission mode adaptation

The goal of mission mode adaptation is to continuously fine-tune the system. For AFE parameters (such as gain control) during mission mode adaptation, CTLE boosting is not changed unless the eye opening exceeds some preset range. Also during mission mode adaptation, DFE coefficients are adapted continuously by the least mean squares (LMS) algorithm.

28.3.7 Test Transmitter

This IP contains a test transmitter for at-speed testing of the RX data-path. This test TX contains a serializer that runs on a reference clock from the VCO of the adjacent lane and serializes the parallel data generated from a pattern generator.

28.3.8 RX Inter Lane Clock Aligner

HDMIRX PHY PMA will output 3 independent lane data stream, every data stream with its lane clock. In inter lane clock aligner module, every lane data stream will write into one data_fifo reg which is 160 bit with its lane clock. And it will use the lane0 clock to read this data_fifo reg, so all these three lane data stream will align to lane0 clock.

28.3.9 RX Symbol Aligner

This module aligns each data lane in 10 bit unit. In the PMA may sample the data bit which is not alignment with 10 bit, but in fixed data phase, so this module will extract 10 bit boundary and align it in 10 bit unit.

In the first stage, the HDMITX will send
10'h2ab: 10'b1010101011(channel0),
10'h0ab: 10'b0010101011(channel1),
10'h354: 10'b1101010100(channel2),
and it is send in LSB first, so RX will receive
10'b1101010101(10'h355, channel0),
10'b1101010100(10'h354, channel1),
10'b0010101011(10'h0ab, channel2).

The first 9 MSB bit is 9'b110101010 or 9'b001010101, and 9'b001010101 is the inversion of 9'b110101010. So the detection comma is 9'b001010101 and its inversion. If the RX extract these detection comma in lane data stream and it will record this pointer in the lane data stream, and output the 10 bit unit with this boundary.

28.3.10 Inter Lane Skew Aligner

This module will align different data lane, which is based on lane0. HDMITX will send 10'h2ab(channel0), 10'h0ab(channel1), 10'h354(channel2), and this module will find these three channel boundary with these comma's inversion, and align them across these three channels.

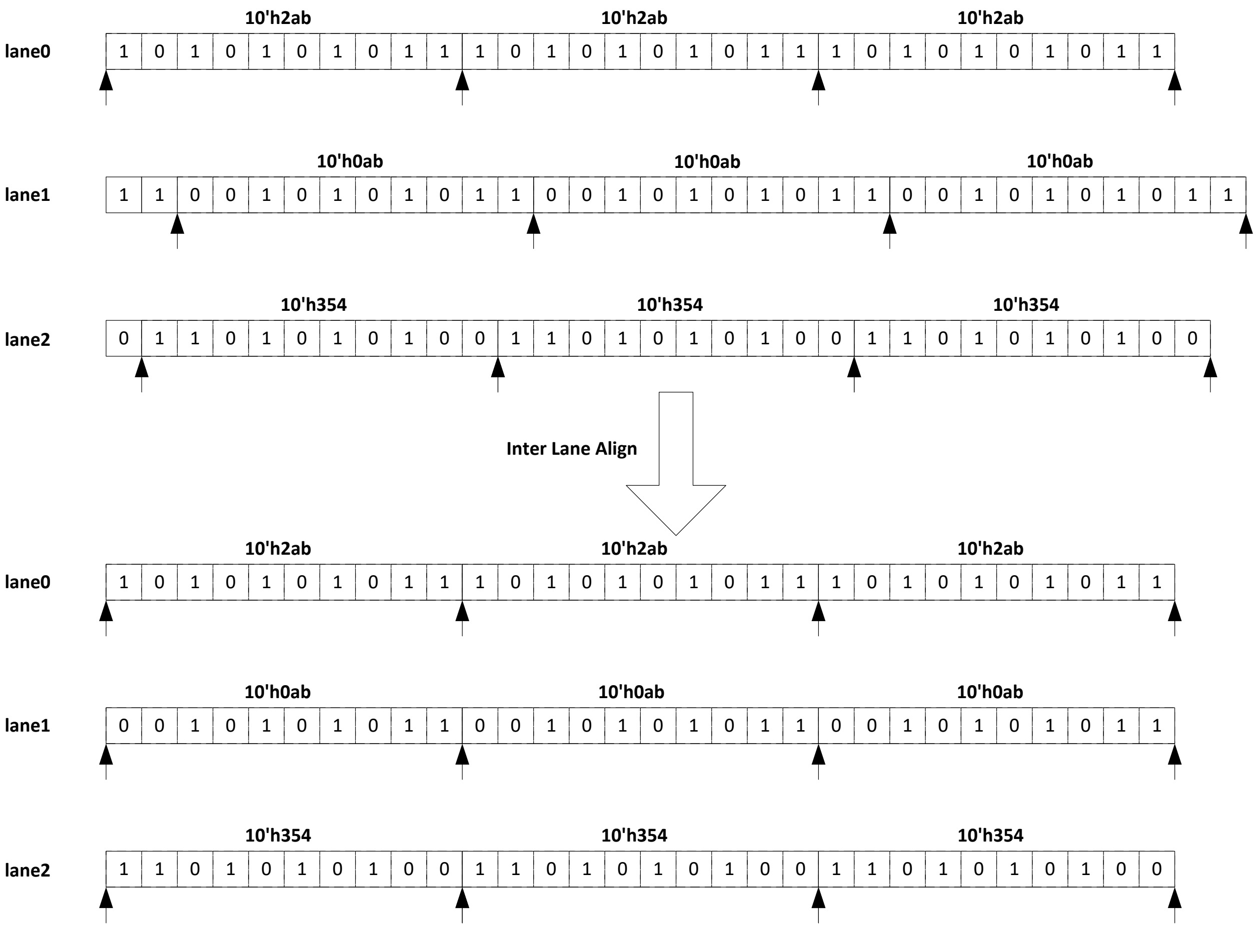

Fig. 28-4 Inter lane skew aligner

28.3.11 RX Gasket

This module will invert each lane data, and pad two 20 bit data into one 40 bit data and output.

The clock will be divided by two and output as the final clock corresponding 40 bit valid data.

28.4 Register Description

28.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

28.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SUP_DIG_IDCODE_LO	0x0000	W	0x000034CD	Low 16 bits of IDCODE
SUP_DIG_IDCODE_HI	0x0001	W	0x00003C42	High 16 bits of IDCODE
SUP_DIG_REFCLK_OVRD_IN	0x0002	W	0x00000700	Override values for incoming REFCLK and RESET controls from ASIC
SUP_DIG_RX_TERM_ACDC_EN_OVRD_IN	0x0003	W	0x00000000	Override values for incoming RX controls from ASIC
SUP_DIG_TMDSCLK_CTRL_OVRD_IN	0x0004	W	0x00000004	Override values for incoming TMDSCLK controls from ASIC
SUP_DIG_SUP_OVRD_IN	0x000D	W	0x00000008	Override values for support block ASIC inputs
SUP_DIG_SUP_OVRD_OUT	0x000E	W	0x00000010	Override values for support block ASIC outputs
SUP_DIG_LVL_OVRD_IN	0x000F	W	0x00000010	Override values for level settings
SUP_DIG_DEBUG	0x0010	W	0x00000000	Debug controls

Name	Offset	Size	Reset Value	Description
SUP_DIG_RX_TERM_EN_ACDC_IN	0x0018	W	0x00000000	Current value for RX_TERM_EN and RX_TERM_ACDC
SUP_DIG_ASIC_IN	0x0019	W	0x00000000	Current values for incoming SUP control signals from ASIC
SUP_DIG_LVL_ASIC_IN	0x001A	W	0x00000000	Current values for incoming level controls from ASIC
SUP_DIG_BANDGAP_ASIC_IN	0x001B	W	0x00000000	Current values for incoming bandgap control from ASIC
SUP_DIG_CLK_RST_BG_PWRUP_TIME_0	0x0038	W	0x00000082	BG Power UP Time Register #0
SUP_DIG_CLK_RST_BG_PWRUP_TIME_1	0x0039	W	0x00000208	BG Power UP Time Register #1
SUP_DIG_ANA_CREGS_ANA_RTUNE_OVRD_IN	0x004A	W	0x00000000	Values for analog rtune block
SUP_DIG_ANA_CREGS_ANA_ATB_IN	0x004B	W	0x00000000	Values for analog atb switch
SUP_DIG_ANA_CREGS_ANA_BG_IN	0x004D	W	0x0000050A	Override values for analog bandgap block
SUP_DIG_ANA_CREGS_TMDS_CLK_SETTING	0x004E	W	0x00000000	Settings for TMDS clock reception and sense detection
SUP_DIG_ANA_CREGS_SUP_ANA_NC	0x004F	W	0x00000000	Reserve values for sup analog block
SUP_DIG_RTUNE_DEBUG	0x0060	W	0x00000000	Resistor tuning debug controls
SUP_DIG_RTUNE_CONFIG	0x0061	W	0x00000014	Configure rtune Operation
SUP_DIG_RTUNE_STAT	0x0062	W	0x00000000	Resistor tuning register status
SUP_DIG_RTUNE_EARC_SET_VAL	0x0064	W	0x00000000	Set value of EARC Resistor
SUP_DIG_RTUNE_RX21_SET_VAL	0x0065	W	0x00000000	Set value of RX21 Resistor
SUP_DIG_RTUNE_EARC_STAT	0x0067	W	0x00000000	EARC Resistor tuning register status
SUP_DIG_RTUNE_RX21_STAT	0x0068	W	0x00000000	RX21 Resistor tuning register status
SUP_DIG_ANA_RX_OVERLOAD_PROT_EN_OVRD_OUT	0x0069	W	0x00000000	Override value for rx_ana_det0Vp_en_i and and rx_ana_det0Vn_en_i
SUP_DIG_ANA_TMDSCLK_EN_OVRD_OUT	0x006A	W	0x00000000	Override value for tmdsclk_an_en signal going to ANA
SUP_DIG_ANA_EARC_TERM_CODE_OVRD_OUT	0x006B	W	0x00000000	Override value for EARC term code
SUP_DIG_ANA_RX_TERM_CODE_OVRD_OUT	0x006C	W	0x00000000	Override value for RX term code
SUP_DIG_ANA_RTUNE_OVRD_OUT	0x006D	W	0x00000000	Override value for rtune signals going to ANA
SUP_DIG_ANA_STAT	0x006E	W	0x00000000	SUP input status register for SUP ANA outputs
SUP_DIG_ANA_ANA_OVRD_OUT	0x006F	W	0x00000000	Override values for ana_async_rst and bandgap signals going to ANA
LANE0_DIG_ASIC_LANE_OVRD_IN	0x1000	W	0x00000000	Override values for incoming LANE controls from ASIC
LANE0_DIG_ASIC_RX_ASIC_LOS	0x1001	W	0x00000000	LOS Related signals

Name	Offset	Size	Reset Value	Description
LANE0_DIG_ASIC_LOS_OVRD_IN	0x1002	W	0x00000010	Override values for LOS signal at ASIC side
LANE0_DIG_ASIC_LOS_OVRD_IN_1	0x1003	W	0x0000005A	Override values for LOS signal at ASIC side
LANE0_DIG_ASIC_CDR_CONTROL_OVRD_IN	0x1006	W	0x00000000	Override values for incoming CDR settings controls from ASIC
LANE0_DIG_ASIC_RX_OVRD_IN_0	0x1007	W	0x00000000	Override values for incoming RX controls from ASIC, register #0
LANE0_DIG_ASIC_RX_OVRD_IN_1	0x1008	W	0x00000014	Override values for incoming RX controls from ASIC, register #1
LANE0_DIG_ASIC_RX_OVRD_IN_2	0x1009	W	0x000003E8	Override values for incoming RX controls from ASIC, register #2
LANE0_DIG_ASIC_RX_OVRD_IN_3	0x100A	W	0x00000000	Override values for incoming RX controls from ASIC, register #3
LANE0_DIG_ASIC_RX_OVRD_IN_4	0x100B	W	0x00000000	Override values for incoming RX controls from ASIC, register #4
LANE0_DIG_ASIC_RX_OVRD_IN_5	0x100C	W	0x00000000	Override values for incoming RX controls from ASIC, register #5
LANE0_DIG_ASIC_RX_OVRD_EQ_IN_0	0x100D	W	0x00003078	Override values for incoming RX EQ controls from ASIC, register #0
LANE0_DIG_ASIC_RX_OVRD_EQ_IN_1	0x100E	W	0x00004040	Override values for incoming RX EQ controls from ASIC, register #1
LANE0_DIG_ASIC_RX_OVRD_OUT_0	0x100F	W	0x00000000	Override values for outgoing RX controls to ASIC, register #0
LANE0_DIG_ASIC_RX_ASIC_IN_0	0x1015	W	0x00000000	Current values for incoming RX controls from ASIC, register #0
LANE0_DIG_ASIC_RX_ASIC_IN_1	0x1016	W	0x00000000	Current values for incoming RX controls from ASIC, register #1
LANE0_DIG_ASIC_RX_EQ_ASIC_IN_0	0x1017	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #0
LANE0_DIG_ASIC_RX_EQ_ASIC_IN_1	0x1018	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #1
LANE0_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0	0x1019	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #0
LANE0_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1	0x101A	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #1
LANE0_DIG_ASIC_RX_ASIC_OUT_0	0x101B	W	0x00000000	Current values for outgoing RX status controls from PHY, register #0
LANE0_DIG_LBERT_CTL	0x1020	W	0x00000000	Pattern Generator controls
LANE0_DIG_RX_CDR_CDR_CTL_0	0x1024	W	0x0000000F	Control bits for receiver in recovered domain
LANE0_DIG_RX_CDR_CDR_CTL_1	0x1025	W	0x00007039	CDR Control Register #1
LANE0_DIG_RX_CDR_CDR_CTL_2	0x1026	W	0x00004ABB	CDR Control Register #2
LANE0_DIG_RX_CDR_CDR_CTL_3	0x1027	W	0x0000099B	CDR Control Register #3

Name	Offset	Size	Reset Value	Description
LANE0_DIG_RX_CDR_CDR_CTL_4	0x1028	W	0x00000003	CDR Control Register #4
LANE0_DIG_RX_CDR_CDR_CTL_5	0x1029	W	0x00000649	CDR Control Register #5
LANE0_DIG_RX_CDR_CDR_CTL_6	0x102A	W	0x000006DB	CDR Control Register #6
LANE0_DIG_RX_CDR_CDR_CTL_7	0x102B	W	0x00008766	CDR Control Register #7
LANE0_DIG_RX_CDR_CDR_CTL_8	0x102C	W	0x0000ECCA	CDR Control Register #8
LANE0_DIG_RX_CDR_CDR_CTL_9	0x102D	W	0x00006432	CDR Control Register #9
LANE0_DIG_RX_CDR_CDR_CTL_10	0x102E	W	0x0000ECA8	CDR Control Register #10
LANE0_DIG_RX_CDR_STAT	0x102F	W	0x00000000	Current output values to dpll (phug, frug)
LANE0_DIG_RX_PWRCTL_RX_PSTATE_P0	0x1040	W	0x00000CF7	RX Power State Control Register for P0
LANE0_DIG_RX_PWRCTL_RX_PSTATE_P0S	0x1041	W	0x00000407	RX Power State Control Register for P0S
LANE0_DIG_RX_PWRCTL_RX_PSTATE_P1	0x1042	W	0x00000307	RX Power State Control Register for P1
LANE0_DIG_RX_PWRCTL_RX_PSTATE_P2	0x1043	W	0x00000301	RX Power State Control Register for P2
LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_0	0x1044	W	0x000001E6	RX Power UP Time Register #0
LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_1	0x1045	W	0x0000069A	RX Power UP Time Register #1
LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_2	0x1046	W	0x0000001A	RX Power UP Time Register #2
LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_3	0x1047	W	0x00000000	RX Power UP Time Register #3
LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0	0x1048	W	0x00000400	RX VCO calibration controls register #0
LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1	0x1049	W	0x00000100	RX VCO calibration controls register #1
LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2	0x104A	W	0x00002600	RX VCO calibration controls register #2
LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0	0x104B	W	0x00003319	RX Power UP Time Register #0
LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1	0x104C	W	0x00000003	RX Power UP Time Register #1
LANE0_DIG_RX_VCOCAL_RX_VCO_STAT_0	0x104D	W	0x00000000	RX VCO status register #0
LANE0_DIG_RX_VCOCAL_RX_VCO_STAT_1	0x104E	W	0x00000000	RX VCO status register #1
LANE0_DIG_RX_VCOCAL_RX_VCO_STAT_2	0x104F	W	0x00000000	RX VCO status register #2
LANE0_DIG_RX_RX_ALIGN_XAUI_COMM_MASK	0x1050	W	0x000003FF	XAUI_COMMA mask
LANE0_DIG_RX_LBERT_CTL	0x1051	W	0x00000000	Pattern Matcher controls

Name	Offset	Size	Reset Value	Description
LANE0_DIG_RX_LBERT_ERR	0x1052	W	0x00000000	Pattern match error counter
LANE0_DIG_RX_RX_LOS_LOS_0	0x1053	W	0x00000062	LOS Control Register #1
LANE0_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS	0x1055	W	0x00000000	Status of rx_pwrsm_state
LANE0_DIG_RX_DPLL_FREQ	0x105C	W	0x00002000	Current frequency integrator value.
LANE0_DIG_RX_DPLL_FREQ_BOUND_0	0x105D	W	0x000004C8	Frequency Bounds for incoming data stream #0
LANE0_DIG_RX_DPLL_FREQ_BOUND_1	0x105E	W	0x0000019C	Frequency Bounds for incoming data stream #1
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_0	0x1060	W	0x00000C10	Adaptation Configuration Register #0
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_1	0x1061	W	0x00000009	Adaptation Configuration Register #1
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_2	0x1062	W	0x000000C2	Adaptation Configuration Register #2
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_3	0x1063	W	0x00000000	Adaptation Configuration Register #3
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_4	0x1064	W	0x00000000	Adaptation Configuration Register #4
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_5	0x1065	W	0x00000000	Adaptation Configuration Register #5
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_6	0x1066	W	0x0000792B	Adaptation Configuration Register #6
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_7	0x1067	W	0x00004342	Adaptation Configuration Register #7
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_8	0x1068	W	0x00004925	Adaptation Configuration Register #8
LANE0_DIG_RX_ADPTCTL_ADPT_CFG_9	0x1069	W	0x00000000	Adaptation Configuration Register #9
LANE0_DIG_RX_ADPTCTL_RST_ADPT_CFG	0x106A	W	0x0000001F	Reset adaptation Configuration Register
LANE0_DIG_RX_ADPTCTL_ATT_STATUS	0x106B	W	0x00000000	Value of ATT adaptation code
LANE0_DIG_RX_ADPTCTL_VGA_STATUS	0x106C	W	0x00000000	Value of VGA adaptation code
LANE0_DIG_RX_ADPTCTL_CTLE_STATUS	0x106D	W	0x00000000	Value of CTLE adaptation code
LANE0_DIG_RX_ADPTCTL_DFE_TAP1_STATUS	0x106E	W	0x00000000	Value of DFE Tap1 adaptation code
LANE0_DIG_RX_ADPTCTL_DFE_TAP2_STATUS	0x106F	W	0x00000000	Value of DFE Tap2 adaptation code
LANE0_DIG_RX_ADPTCTL_DFE_TAP3_STATUS	0x1070	W	0x00000000	Value of DFE Tap3 adaptation code
LANE0_DIG_RX_ADPTCTL_DFE_TAP4_STATUS	0x1071	W	0x00000000	Value of DFE Tap4 adaptation code
LANE0_DIG_RX_ADPTCTL_DFE_TAP5_STATUS	0x1072	W	0x00000000	Value of DFE Tap5 adaptation code

Name	Offset	Size	Reset Value	Description
LANE0_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST	0x1073	W	0x00000080	Offset values for RX DFE data even vDAC
LANE0_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST	0x1074	W	0x00000080	Offset values for RX DFE data odd vDAC
LANE0_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN	0x1075	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
LANE0_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD	0x1076	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
LANE0_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST	0x1077	W	0x00000080	Offset values for RX DFE error even vDAC
LANE0_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST	0x1078	W	0x00000080	Offset values for RX DFE error odd vDAC
LANE0_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL	0x1079	W	0x00000000	Value of error slicer level
LANE0_DIG_RX_ADPTCTL_ADPT_RESET	0x107A	W	0x00000000	Adaptation reset register
LANE0_DIG_RX_STAT_LD_VAL_1	0x1080	W	0x00000040	Stat load value for the sample counter #1
LANE0_DIG_RX_STAT_DATA_MSK	0x1081	W	0x0000FFFF	Stat data mask bits [15:0]
LANE0_DIG_RX_STAT_MATCH_CTL0	0x1082	W	0x00003C06	Stat match controls register #0
LANE0_DIG_RX_STAT_MATCH_CTL1	0x1083	W	0x00000800	Stat match controls register #1
LANE0_DIG_RX_STAT_STAT_CTL0	0x1084	W	0x00004000	Stat controls register #0
LANE0_DIG_RX_STAT_STAT_CTL1	0x1085	W	0x00000008	Stat controls register #1
LANE0_DIG_RX_STAT_SMPL_CNT1	0x1086	W	0x00000000	Sample counter #1 Status
LANE0_DIG_RX_STAT_STAT_CNT_0	0x1087	W	0x00000000	Stat counter 0 Status
LANE0_DIG_RX_STAT_STAT_CNT_1	0x1088	W	0x00000000	Stat counter 1 Status
LANE0_DIG_RX_STAT_STAT_CNT_2	0x1089	W	0x00000000	Stat counter 2 Status
LANE0_DIG_RX_STAT_STAT_CNT_3	0x108A	W	0x00000000	Stat counter 3 Status
LANE0_DIG_RX_STAT_STAT_CNT_4	0x108B	W	0x00000000	Stat counter 4 Status
LANE0_DIG_RX_STAT_STAT_CNT_5	0x108C	W	0x00000000	Stat counter 5 Status
LANE0_DIG_RX_STAT_STAT_CNT_6	0x108D	W	0x00000000	Stat counter 6 Status
LANE0_DIG_RX_STAT_CAL_COMP_CLK_CTL	0x108E	W	0x00000019	Calibration Comparator Control
LANE0_DIG_RX_STAT_MATCH_CTL2	0x108F	W	0x00000000	Stat match controls register #2

Name	Offset	Size	Reset Value	Description
LANE0_DIG_RX_STAT_MATCH_CTL3	0x1090	W	0x00000000	Stat match controls register #3
LANE0_DIG_RX_STAT_MATCH_CTL4	0x1091	W	0x00000000	Stat match controls register #4
LANE0_DIG_RX_STAT_MATCH_CTL5	0x1092	W	0x00000000	Stat match controls register #5
LANE0_DIG_RX_STAT_STAT_CTL2	0x1093	W	0x00000000	Stat controls register #2
LANE0_DIG_RX_STAT_STAT_STOP	0x1094	W	0x00000000	Stat stop register
LANE0_DIG_ANA_TX_OVRD_OUT	0x10A0	W	0x00000000	Override values for TX signals going to ANA
LANE0_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT	0x10A1	W	0x00000000	Feature enable for tx_ana_lpbk_dfe_mode
LANE0_DIG_ANA_RX_DIV_OVRD_OUT	0x10A6	W	0x00000000	Override values for RX control signals going to ANA
LANE0_DIG_ANA_RX_CTL_OVRD_OUT	0x10A7	W	0x00000000	Override values for RX control signals going to ANA
LANE0_DIG_ANA_RX_PWR_OVRD_OUT	0x10A8	W	0x00000000	Override values for RX PWR UP/DN signals going to ANA
LANE0_DIG_ANA_RX_VCO_OVRD_OUT_0	0x10A9	W	0x00000000	Override values for RX VCO signals going to ANA #0
LANE0_DIG_ANA_RX_VCO_OVRD_OUT_1	0x10AA	W	0x00000002	Override values for RX VCO signals going to ANA #1
LANE0_DIG_ANA_RX_VCO_OVRD_OUT_2	0x10AB	W	0x00000000	Override values for RX VCO signals going to ANA #2
LANE0_DIG_ANA_RX_CAL	0x10AC	W	0x00000000	Sets values for RX CAL signals going to ANA register
LANE0_DIG_ANA_RX_DAC_CTRL	0x10AD	W	0x00000080	Sets values for RX DAC CTRL value going to ANA
LANE0_DIG_ANA_RX_DAC_CTRL_OVRD	0x10AE	W	0x00000000	Overrides RX DAC CTRL bus (en/val/sel) going to ANA
LANE0_DIG_ANA_RX_DAC_CTRL_SEL	0x10AF	W	0x00000000	Sets values for RX DAC CTRL Select signal going to ANA
LANE0_DIG_ANA_RX_AFE_ATT_VGA	0x10B0	W	0x00003000	Value for RX AFE ATT & VGA signals going to ANA
LANE0_DIG_ANA_RX_AFE_CTLE	0x10B1	W	0x00000000	Values for RX AFE CTLE signals going to ANA
LANE0_DIG_ANA_RX_SCOPE	0x10B2	W	0x00000000	Values for RX SCOPE signals going to ANA
LANE0_DIG_ANA_RX_SLICER_CTRL	0x10B3	W	0x00000077	Sets values for RX slicer ctrl signals going to ANA register
LANE0_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST	0x10B4	W	0x00000007	Sets values for RX ANA IQ phase adjust signal going to ANA register
LANE0_DIG_ANA_RX_ANA_IQ_SENSE_EN	0x10B5	W	0x00000000	Sets values for RX ANA IQ SENSE signal
LANE0_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN	0x10B6	W	0x00000000	DAC CTRL enable signal
LANE0_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE	0x10B7	W	0x00000000	Afe update enable signal

Name	Offset	Size	Reset Value	Description
LANE0_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK	0x10B8	W	0x00000000	PHASE adjust clock signal
LANE0_DIG_ANA_STATUS_0	0x10B9	W	0x00000000	Lane input status register #0
LANE0_DIG_ANA_STATUS_1	0x10BA	W	0x00000000	Lane input status register #1
LANE0_DIG_ANA_STATUS_LOS	0x10BB	W	0x00000000	LOS status at ana interface
LANE0_DIG_ANA_CREGS_TX_ANA_ATB_REG	0x10C0	W	0x00000000	TX ANA ATB measurement control register
LANE0_DIG_ANA_CREGS_RX_ANA_EQ_CTRL	0x10C4	W	0x00000034	RX ANA EQ control register
LANE0_DIG_ANA_CREGS_RX_ANA_VCO_CTRL	0x10C5	W	0x00000004	RX ANA VCO control register
LANE0_DIG_ANA_CREGS_RX_ANA_VREG_CTRL	0x10C6	W	0x00000001	RX ANA VREG control register
LANE0_DIG_ANA_CREGS_RX_ANA_DISCONNECT	0x10C7	W	0x00000000	RX ANA disconnect control
LANE0_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL	0x10C8	W	0x00000000	RX ANA reserved control register
LANE0_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1	0x10C9	W	0x00000000	RX ANA ATB control register 1
LANE0_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2	0x10CA	W	0x00000000	RX ANA ATB control register 2
LANE1_DIG_ASIC_LANE_OVRD_IN	0x1100	W	0x00000000	Override values for incoming LANE controls from ASIC
LANE1_DIG_ASIC_RX_ASIC_LOS	0x1101	W	0x00000000	LOS Related signals
LANE1_DIG_ASIC_LOS_OVRD_IN	0x1102	W	0x00000010	Override values for LOS signal at ASIC side
LANE1_DIG_ASIC_LOS_OVRD_IN_1	0x1103	W	0x0000005A	Override values for LOS signal at ASIC side
LANE1_DIG_ASIC_CDR_CONTROL_OVRD_IN	0x1106	W	0x00000000	Override values for incoming CDR settings controls from ASIC
LANE1_DIG_ASIC_RX_OVRD_IN_0	0x1107	W	0x00000000	Override values for incoming RX controls from ASIC, register #0
LANE1_DIG_ASIC_RX_OVRD_IN_1	0x1108	W	0x00000014	Override values for incoming RX controls from ASIC, register #1
LANE1_DIG_ASIC_RX_OVRD_IN_2	0x1109	W	0x000003E8	Override values for incoming RX controls from ASIC, register #2
LANE1_DIG_ASIC_RX_OVRD_IN_3	0x110A	W	0x00000000	Override values for incoming RX controls from ASIC, register #3
LANE1_DIG_ASIC_RX_OVRD_IN_4	0x110B	W	0x00000000	Override values for incoming RX controls from ASIC, register #4
LANE1_DIG_ASIC_RX_OVRD_IN_5	0x110C	W	0x00000000	Override values for incoming RX controls from ASIC, register #5
LANE1_DIG_ASIC_RX_OVRD_EQ_IN_0	0x110D	W	0x00003078	Override values for incoming RX EQ controls from ASIC, register #0
LANE1_DIG_ASIC_RX_OVRD_EQ_IN_1	0x110E	W	0x00004040	Override values for incoming RX EQ controls from ASIC, register #1

Name	Offset	Size	Reset Value	Description
LANE1_DIG_ASIC_RX_OVRD_OUT_0	0x110F	W	0x00000000	Override values for outgoing RX controls to ASIC, register #0
LANE1_DIG_ASIC_RX_ASIC_IN_0	0x1115	W	0x00000000	Current values for incoming RX controls from ASIC, register #0
LANE1_DIG_ASIC_RX_ASIC_IN_1	0x1116	W	0x00000000	Current values for incoming RX controls from ASIC, register #1
LANE1_DIG_ASIC_RX_EQ_ASIC_IN_0	0x1117	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #0
LANE1_DIG_ASIC_RX_EQ_ASIC_IN_1	0x1118	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #1
LANE1_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0	0x1119	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #0
LANE1_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1	0x111A	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #1
LANE1_DIG_ASIC_RX_ASIC_OUT_0	0x111B	W	0x00000000	Current values for outgoing RX status controls from PHY, register #0
LANE1_DIG_LBERT_CTL	0x1120	W	0x00000000	Pattern Generator controls
LANE1_DIG_RX_CDR_CDR_CTL_0	0x1124	W	0x0000000F	Control bits for receiver in recovered domain
LANE1_DIG_RX_CDR_CDR_CTL_1	0x1125	W	0x00007039	CDR Control Register #1
LANE1_DIG_RX_CDR_CDR_CTL_2	0x1126	W	0x00004ABB	CDR Control Register #2
LANE1_DIG_RX_CDR_CDR_CTL_3	0x1127	W	0x0000099B	CDR Control Register #3
LANE1_DIG_RX_CDR_CDR_CTL_4	0x1128	W	0x00000003	CDR Control Register #4
LANE1_DIG_RX_CDR_CDR_CTL_5	0x1129	W	0x00000649	CDR Control Register #5
LANE1_DIG_RX_CDR_CDR_CTL_6	0x112A	W	0x000006DB	CDR Control Register #6
LANE1_DIG_RX_CDR_CDR_CTL_7	0x112B	W	0x00008766	CDR Control Register #7
LANE1_DIG_RX_CDR_CDR_CTL_8	0x112C	W	0x0000ECCA	CDR Control Register #8
LANE1_DIG_RX_CDR_CDR_CTL_9	0x112D	W	0x00006432	CDR Control Register #9
LANE1_DIG_RX_CDR_CDR_CTL_10	0x112E	W	0x0000ECA8	CDR Control Register #10
LANE1_DIG_RX_CDR_STAT	0x112F	W	0x00000000	Current output values to dpll (phug, frug)
LANE1_DIG_RX_PWRCTL_RX_PSTATE_P0	0x1140	W	0x00000CF7	RX Power State Control Register for P0
LANE1_DIG_RX_PWRCTL_RX_PSTATE_P0S	0x1141	W	0x00000407	RX Power State Control Register for P0S
LANE1_DIG_RX_PWRCTL_RX_PSTATE_P1	0x1142	W	0x00000307	RX Power State Control Register for P1

Name	Offset	Size	Reset Value	Description
LANE1_DIG_RX_PWRCTL_RX_PSTATE_P2	0x1143	W	0x00000301	RX Power State Control Register for P2
LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_0	0x1144	W	0x000001E6	RX Power UP Time Register #0
LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_1	0x1145	W	0x0000069A	RX Power UP Time Register #1
LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_2	0x1146	W	0x0000001A	RX Power UP Time Register #2
LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_3	0x1147	W	0x00000000	RX Power UP Time Register #3
LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0	0x1148	W	0x00000400	RX VCO calibration controls register #0
LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1	0x1149	W	0x00000100	RX VCO calibration controls register #1
LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2	0x114A	W	0x00002600	RX VCO calibration controls register #2
LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0	0x114B	W	0x00003319	RX Power UP Time Register #0
LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1	0x114C	W	0x00000003	RX Power UP Time Register #1
LANE1_DIG_RX_VCOCAL_RX_VCO_STAT_0	0x114D	W	0x00000000	RX VCO status register #0
LANE1_DIG_RX_VCOCAL_RX_VCO_STAT_1	0x114E	W	0x00000000	RX VCO status register #1
LANE1_DIG_RX_VCOCAL_RX_VCO_STAT_2	0x114F	W	0x00000000	RX VCO status register #2
LANE1_DIG_RX_RX_ALIGN_XAUI_COMM_MASK	0x1150	W	0x000003FF	XAUI_COMMA mask
LANE1_DIG_RX_LBERT_CTL	0x1151	W	0x00000000	Pattern Matcher controls
LANE1_DIG_RX_LBERT_ERR	0x1152	W	0x00000000	Pattern match error counter
LANE1_DIG_RX_RX_LOS_LOS_0	0x1153	W	0x00000062	LOS Control Register #1
LANE1_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS	0x1155	W	0x00000000	Status of rx_pwrsm_state
LANE1_DIG_RX_DPLL_FREQ	0x115C	W	0x00002000	Current frequency integrator value.
LANE1_DIG_RX_DPLL_FREQ_BOUND_0	0x115D	W	0x000004C8	Frequency Bounds for incoming data stream #0
LANE1_DIG_RX_DPLL_FREQ_BOUND_1	0x115E	W	0x0000019C	Frequency Bounds for incoming data stream #1
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_0	0x1160	W	0x00000C10	Adaptation Configuration Register #0
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_1	0x1161	W	0x00000009	Adaptation Configuration Register #1
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_2	0x1162	W	0x000000C2	Adaptation Configuration Register #2
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_3	0x1163	W	0x00000000	Adaptation Configuration Register #3
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_4	0x1164	W	0x00000000	Adaptation Configuration Register #4

Name	Offset	Size	Reset Value	Description
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_5	0x1165	W	0x00000000	Adaptation Configuration Register #5
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_6	0x1166	W	0x0000792B	Adaptation Configuration Register #6
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_7	0x1167	W	0x00004342	Adaptation Configuration Register #7
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_8	0x1168	W	0x00004925	Adaptation Configuration Register #8
LANE1_DIG_RX_ADPTCTL_ADPT_CFG_9	0x1169	W	0x00000000	Adaptation Configuration Register #9
LANE1_DIG_RX_ADPTCTL_RST_ADPT_CFG	0x116A	W	0x0000001F	Reset adaptation Configuration Register
LANE1_DIG_RX_ADPTCTL_ATT_STATUS	0x116B	W	0x00000000	Value of ATT adaptation code
LANE1_DIG_RX_ADPTCTL_VGA_STATUS	0x116C	W	0x00000000	Value of VGA adaptation code
LANE1_DIG_RX_ADPTCTL_CTLE_STATUS	0x116D	W	0x00000000	Value of CTLE adaptation code
LANE1_DIG_RX_ADPTCTL_DFE_TAP1_STATUS	0x116E	W	0x00000000	Value of DFE Tap1 adaptation code
LANE1_DIG_RX_ADPTCTL_DFE_TAP2_STATUS	0x116F	W	0x00000000	Value of DFE Tap2 adaptation code
LANE1_DIG_RX_ADPTCTL_DFE_TAP3_STATUS	0x1170	W	0x00000000	Value of DFE Tap3 adaptation code
LANE1_DIG_RX_ADPTCTL_DFE_TAP4_STATUS	0x1171	W	0x00000000	Value of DFE Tap4 adaptation code
LANE1_DIG_RX_ADPTCTL_DFE_TAP5_STATUS	0x1172	W	0x00000000	Value of DFE Tap5 adaptation code
LANE1_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST	0x1173	W	0x00000080	Offset values for RX DFE data even vDAC
LANE1_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST	0x1174	W	0x00000080	Offset values for RX DFE data odd vDAC
LANE1_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN	0x1175	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
LANE1_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD	0x1176	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
LANE1_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST	0x1177	W	0x00000080	Offset values for RX DFE error even vDAC
LANE1_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST	0x1178	W	0x00000080	Offset values for RX DFE error odd vDAC
LANE1_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL	0x1179	W	0x00000000	Value of error slicer level
LANE1_DIG_RX_ADPTCTL_ADPT_RESET	0x117A	W	0x00000000	Adaptation reset register
LANE1_DIG_RX_STAT_LD_VAL_1	0x1180	W	0x00000040	Stat load value for the sample counter #1
LANE1_DIG_RX_STAT_DATA_MSK	0x1181	W	0x0000FFFF	Stat data mask bits [15:0]

Name	Offset	Size	Reset Value	Description
LANE1_DIG_RX_STAT_MATCH_CTL0	0x1182	W	0x00003C06	Stat match controls register #0
LANE1_DIG_RX_STAT_MATCH_CTL1	0x1183	W	0x00000800	Stat match controls register #1
LANE1_DIG_RX_STAT_STAT_CTL0	0x1184	W	0x00004000	Stat controls register #0
LANE1_DIG_RX_STAT_STAT_CTL1	0x1185	W	0x00000008	Stat controls register #1
LANE1_DIG_RX_STAT_SMPL_CNT1	0x1186	W	0x00000000	Sample counter #1 Status
LANE1_DIG_RX_STAT_STAT_CNT_0	0x1187	W	0x00000000	Stat counter 0 Status
LANE1_DIG_RX_STAT_STAT_CNT_1	0x1188	W	0x00000000	Stat counter 1 Status
LANE1_DIG_RX_STAT_STAT_CNT_2	0x1189	W	0x00000000	Stat counter 2 Status
LANE1_DIG_RX_STAT_STAT_CNT_3	0x118A	W	0x00000000	Stat counter 3 Status
LANE1_DIG_RX_STAT_STAT_CNT_4	0x118B	W	0x00000000	Stat counter 4 Status
LANE1_DIG_RX_STAT_STAT_CNT_5	0x118C	W	0x00000000	Stat counter 5 Status
LANE1_DIG_RX_STAT_STAT_CNT_6	0x118D	W	0x00000000	Stat counter 6 Status
LANE1_DIG_RX_STAT_CAL_COMP_CLK_CTL	0x118E	W	0x00000019	Calibration Comparator Control
LANE1_DIG_RX_STAT_MATCH_CTL2	0x118F	W	0x00000000	Stat match controls register #2
LANE1_DIG_RX_STAT_MATCH_CTL3	0x1190	W	0x00000000	Stat match controls register #3
LANE1_DIG_RX_STAT_MATCH_CTL4	0x1191	W	0x00000000	Stat match controls register #4
LANE1_DIG_RX_STAT_MATCH_CTL5	0x1192	W	0x00000000	Stat match controls register #5
LANE1_DIG_RX_STAT_STAT_CTL2	0x1193	W	0x00000000	Stat controls register #2
LANE1_DIG_RX_STAT_STAT_STOP	0x1194	W	0x00000000	Stat stop register
LANE1_DIG_ANA_TX_OVRD_OUT	0x11A0	W	0x00000000	Override values for TX signals going to ANA
LANE1_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT	0x11A1	W	0x00000000	Feature enable for tx_ana_lpbk_dfe_mode
LANE1_DIG_ANA_RX_DIV_OVRD_OUT	0x11A6	W	0x00000000	Override values for RX control signals going to ANA
LANE1_DIG_ANA_RX_CTL_OVRD_OUT	0x11A7	W	0x00000000	Override values for RX control signals going to ANA
LANE1_DIG_ANA_RX_PWR_OVRD_OUT	0x11A8	W	0x00000000	Override values for RX PWR UP/DN signals going to ANA
LANE1_DIG_ANA_RX_VCO_OVRD_OUT_0	0x11A9	W	0x00000000	Override values for RX VCO signals going to ANA #0
LANE1_DIG_ANA_RX_VCO_OVRD_OUT_1	0x11AA	W	0x00000002	Override values for RX VCO signals going to ANA #1

Name	Offset	Size	Reset Value	Description
LANE1_DIG_ANA_RX_VCO_OVRD_OUT_2	0x11AB	W	0x00000000	Override values for RX VCO signals going to ANA #2
LANE1_DIG_ANA_RX_CAL	0x11AC	W	0x00000000	Sets values for RX CAL signals going to ANA register
LANE1_DIG_ANA_RX_DAC_CTRL	0x11AD	W	0x00000080	Sets values for RX DAC CTRL value going to ANA
LANE1_DIG_ANA_RX_DAC_CTRL_OVRD	0x11AE	W	0x00000000	Overrides RX DAC CTRL bus (en/val/sel) going to ANA
LANE1_DIG_ANA_RX_DAC_CTRL_SEL	0x11AF	W	0x00000000	Sets values for RX DAC CTRL Select signal going to ANA
LANE1_DIG_ANA_RX_AFE_ATT_VGA	0x11B0	W	0x00003000	Value for RX AFE ATT & VGA signals going to ANA
LANE1_DIG_ANA_RX_AFE_CTLE	0x11B1	W	0x00000000	Values for RX AFE CTLE signals going to ANA
LANE1_DIG_ANA_RX_SCOPE	0x11B2	W	0x00000000	Values for RX SCOPE signals going to ANA
LANE1_DIG_ANA_RX_SLICER_CTRL	0x11B3	W	0x00000077	Sets values for RX slicer ctrl signals going to ANA register
LANE1_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST	0x11B4	W	0x00000007	Sets values for RX ANA IQ phase adjust signal going to ANA register
LANE1_DIG_ANA_RX_ANA_IQ_SENSE_EN	0x11B5	W	0x00000000	Sets values for RX ANA IQ SENSE signal
LANE1_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN	0x11B6	W	0x00000000	DAC CTRL enable signal
LANE1_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE	0x11B7	W	0x00000000	Afe update enable signal
LANE1_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK	0x11B8	W	0x00000000	PHASE adjust clock signal
LANE1_DIG_ANA_STATUS_0	0x11B9	W	0x00000000	Lane input status register #0
LANE1_DIG_ANA_STATUS_1	0x11BA	W	0x00000000	Lane input status register #1
LANE1_DIG_ANA_STATUS_LOS	0x11BB	W	0x00000000	LOS status at ana interface
LANE1_DIG_ANA_CREGS_TX_ANA_ATB_REG	0x11C0	W	0x00000000	TX ANA ATB measurement control register
LANE1_DIG_ANA_CREGS_RX_ANA_EQ_CTRL	0x11C4	W	0x00000034	RX ANA EQ control register
LANE1_DIG_ANA_CREGS_RX_ANA_VCO_CTRL	0x11C5	W	0x00000004	RX ANA VCO control register
LANE1_DIG_ANA_CREGS_RX_ANA_VREG_CTRL	0x11C6	W	0x00000001	RX ANA VREG control register
LANE1_DIG_ANA_CREGS_RX_ANA_DISCONNECT	0x11C7	W	0x00000000	RX ANA disconnect control
LANE1_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL	0x11C8	W	0x00000000	RX ANA reserved control register
LANE1_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1	0x11C9	W	0x00000000	RX ANA ATB control register 1
LANE1_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2	0x11CA	W	0x00000000	RX ANA ATB control register 2

Name	Offset	Size	Reset Value	Description
LANE2_DIG_ASIC_LANE_OVRD_IN	0x1200	W	0x00000000	Override values for incoming LANE controls from ASIC
LANE2_DIG_ASIC_RX_ASIC_LOS	0x1201	W	0x00000000	LOS Related signals
LANE2_DIG_ASIC_LOS_OVRD_IN	0x1202	W	0x00000010	Override values for LOS signal at ASIC side
LANE2_DIG_ASIC_LOS_OVRD_IN_1	0x1203	W	0x0000005A	Override values for LOS signal at ASIC side
LANE2_DIG_ASIC_CDR_CONTROL_OVRD_IN	0x1206	W	0x00000000	Override values for incoming CDR settings controls from ASIC
LANE2_DIG_ASIC_RX_OVRD_IN_0	0x1207	W	0x00000000	Override values for incoming RX controls from ASIC, register #0
LANE2_DIG_ASIC_RX_OVRD_IN_1	0x1208	W	0x00000014	Override values for incoming RX controls from ASIC, register #1
LANE2_DIG_ASIC_RX_OVRD_IN_2	0x1209	W	0x000003E8	Override values for incoming RX controls from ASIC, register #2
LANE2_DIG_ASIC_RX_OVRD_IN_3	0x120A	W	0x00000000	Override values for incoming RX controls from ASIC, register #3
LANE2_DIG_ASIC_RX_OVRD_IN_4	0x120B	W	0x00000000	Override values for incoming RX controls from ASIC, register #4
LANE2_DIG_ASIC_RX_OVRD_IN_5	0x120C	W	0x00000000	Override values for incoming RX controls from ASIC, register #5
LANE2_DIG_ASIC_RX_OVRD_EQ_IN_0	0x120D	W	0x00003078	Override values for incoming RX EQ controls from ASIC, register #0
LANE2_DIG_ASIC_RX_OVRD_EQ_IN_1	0x120E	W	0x00004040	Override values for incoming RX EQ controls from ASIC, register #1
LANE2_DIG_ASIC_RX_OVRD_OUT_0	0x120F	W	0x00000000	Override values for outgoing RX controls to ASIC, register #0
LANE2_DIG_ASIC_RX_ASIC_IN_0	0x1215	W	0x00000000	Current values for incoming RX controls from ASIC, register #0
LANE2_DIG_ASIC_RX_ASIC_IN_1	0x1216	W	0x00000000	Current values for incoming RX controls from ASIC, register #1
LANE2_DIG_ASIC_RX_EQ_ASIC_IN_0	0x1217	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #0
LANE2_DIG_ASIC_RX_EQ_ASIC_IN_1	0x1218	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #1
LANE2_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0	0x1219	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #0
LANE2_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1	0x121A	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #1
LANE2_DIG_ASIC_RX_ASIC_OUT_0	0x121B	W	0x00000000	Current values for outgoing RX status controls from PHY, register #0
LANE2_DIG_LBERT_CTL	0x1220	W	0x00000000	Pattern Generator controls
LANE2_DIG_RX_CDR_CDR_CTL_0	0x1224	W	0x0000000F	Control bits for receiver in recovered domain
LANE2_DIG_RX_CDR_CDR_CTL_1	0x1225	W	0x00007039	CDR Control Register #1

Name	Offset	Size	Reset Value	Description
LANE2_DIG_RX_CDR_CDR_CTL_2	0x1226	W	0x00004ABB	CDR Control Register #2
LANE2_DIG_RX_CDR_CDR_CTL_3	0x1227	W	0x0000099B	CDR Control Register #3
LANE2_DIG_RX_CDR_CDR_CTL_4	0x1228	W	0x00000003	CDR Control Register #4
LANE2_DIG_RX_CDR_CDR_CTL_5	0x1229	W	0x00000649	CDR Control Register #5
LANE2_DIG_RX_CDR_CDR_CTL_6	0x122A	W	0x000006DB	CDR Control Register #6
LANE2_DIG_RX_CDR_CDR_CTL_7	0x122B	W	0x00008766	CDR Control Register #7
LANE2_DIG_RX_CDR_CDR_CTL_8	0x122C	W	0x0000ECCA	CDR Control Register #8
LANE2_DIG_RX_CDR_CDR_CTL_9	0x122D	W	0x00006432	CDR Control Register #9
LANE2_DIG_RX_CDR_CDR_CTL_10	0x122E	W	0x0000ECA8	CDR Control Register #10
LANE2_DIG_RX_CDR_STAT	0x122F	W	0x00000000	Current output values to dpll (phug, frug)
LANE2_DIG_RX_PWRCTL_RX_PSTATE_P0	0x1240	W	0x00000CF7	RX Power State Control Register for P0
LANE2_DIG_RX_PWRCTL_RX_PSTATE_P0S	0x1241	W	0x00000407	RX Power State Control Register for P0S
LANE2_DIG_RX_PWRCTL_RX_PSTATE_P1	0x1242	W	0x00000307	RX Power State Control Register for P1
LANE2_DIG_RX_PWRCTL_RX_PSTATE_P2	0x1243	W	0x00000301	RX Power State Control Register for P2
LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_0	0x1244	W	0x000001E6	RX Power UP Time Register #0
LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_1	0x1245	W	0x0000069A	RX Power UP Time Register #1
LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_2	0x1246	W	0x0000001A	RX Power UP Time Register #2
LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_3	0x1247	W	0x00000000	RX Power UP Time Register #3
LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0	0x1248	W	0x00000400	RX VCO calibration controls register #0
LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1	0x1249	W	0x00000100	RX VCO calibration controls register #1
LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2	0x124A	W	0x00002600	RX VCO calibration controls register #2
LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0	0x124B	W	0x00003319	RX Power UP Time Register #0
LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1	0x124C	W	0x00000003	RX Power UP Time Register #1
LANE2_DIG_RX_VCOCAL_RX_VCO_STAT_0	0x124D	W	0x00000000	RX VCO status register #0
LANE2_DIG_RX_VCOCAL_RX_VCO_STAT_1	0x124E	W	0x00000000	RX VCO status register #1
LANE2_DIG_RX_VCOCAL_RX_VCO_STAT_2	0x124F	W	0x00000000	RX VCO status register #2

Name	Offset	Size	Reset Value	Description
LANE2_DIG_RX_RX_ALIGN_XAUI_COMM_MASK	0x1250	W	0x000003FF	XAUI_COMMA mask
LANE2_DIG_RX_LBERT_CTL	0x1251	W	0x00000000	Pattern Matcher controls
LANE2_DIG_RX_LBERT_ERR	0x1252	W	0x00000000	Pattern match error counter
LANE2_DIG_RX_RX_LOS_LOS_0	0x1253	W	0x00000062	LOS Control Register #1
LANE2_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS	0x1255	W	0x00000000	Status of rx_pwrsm_state
LANE2_DIG_RX_DPLL_FREQ	0x125C	W	0x00002000	Current frequency integrator value.
LANE2_DIG_RX_DPLL_FREQ_BOUND_0	0x125D	W	0x000004C8	Frequency Bounds for incoming data stream #0
LANE2_DIG_RX_DPLL_FREQ_BOUND_1	0x125E	W	0x0000019C	Frequency Bounds for incoming data stream #1
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_0	0x1260	W	0x00000C10	Adaptation Configuration Register #0
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_1	0x1261	W	0x00000009	Adaptation Configuration Register #1
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_2	0x1262	W	0x000000C2	Adaptation Configuration Register #2
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_3	0x1263	W	0x00000000	Adaptation Configuration Register #3
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_4	0x1264	W	0x00000000	Adaptation Configuration Register #4
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_5	0x1265	W	0x00000000	Adaptation Configuration Register #5
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_6	0x1266	W	0x0000792B	Adaptation Configuration Register #6
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_7	0x1267	W	0x00004342	Adaptation Configuration Register #7
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_8	0x1268	W	0x00004925	Adaptation Configuration Register #8
LANE2_DIG_RX_ADPTCTL_ADPT_CFG_9	0x1269	W	0x00000000	Adaptation Configuration Register #9
LANE2_DIG_RX_ADPTCTL_RST_ADPT_CFG	0x126A	W	0x0000001F	Reset adaptation Configuration Register
LANE2_DIG_RX_ADPTCTL_ATT_STATUS	0x126B	W	0x00000000	Value of ATT adaptation code
LANE2_DIG_RX_ADPTCTL_VGA_STATUS	0x126C	W	0x00000000	Value of VGA adaptation code
LANE2_DIG_RX_ADPTCTL_CTLE_STATUS	0x126D	W	0x00000000	Value of CTLE adaptation code
LANE2_DIG_RX_ADPTCTL_DFE_TAP1_STATUS	0x126E	W	0x00000000	Value of DFE Tap1 adaptation code
LANE2_DIG_RX_ADPTCTL_DFE_TAP2_STATUS	0x126F	W	0x00000000	Value of DFE Tap2 adaptation code
LANE2_DIG_RX_ADPTCTL_DFE_TAP3_STATUS	0x1270	W	0x00000000	Value of DFE Tap3 adaptation code
LANE2_DIG_RX_ADPTCTL_DFE_TAP4_STATUS	0x1271	W	0x00000000	Value of DFE Tap4 adaptation code

Name	Offset	Size	Reset Value	Description
LANE2_DIG_RX_ADPTCTL_DFE_TAP5_STATUS	0x1272	W	0x00000000	Value of DFE Tap5 adaptation code
LANE2_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST	0x1273	W	0x00000080	Offset values for RX DFE data even vDAC
LANE2_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST	0x1274	W	0x00000080	Offset values for RX DFE data odd vDAC
LANE2_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN	0x1275	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
LANE2_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD	0x1276	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
LANE2_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST	0x1277	W	0x00000080	Offset values for RX DFE error even vDAC
LANE2_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST	0x1278	W	0x00000080	Offset values for RX DFE error odd vDAC
LANE2_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL	0x1279	W	0x00000000	Value of error slicer level
LANE2_DIG_RX_ADPTCTL_ADPT_RESET	0x127A	W	0x00000000	Adaptation reset register
LANE2_DIG_RX_STAT_LD_VAL_1	0x1280	W	0x00000040	Stat load value for the sample counter #1
LANE2_DIG_RX_STAT_DATA_MSK	0x1281	W	0x0000FFFF	Stat data mask bits [15:0]
LANE2_DIG_RX_STAT_MATCH_CTL0	0x1282	W	0x00003C06	Stat match controls register #0
LANE2_DIG_RX_STAT_MATCH_CTL1	0x1283	W	0x00000800	Stat match controls register #1
LANE2_DIG_RX_STAT_STAT_CTL0	0x1284	W	0x00004000	Stat controls register #0
LANE2_DIG_RX_STAT_STAT_CTL1	0x1285	W	0x00000008	Stat controls register #1
LANE2_DIG_RX_STAT_SMPL_CNT1	0x1286	W	0x00000000	Sample counter #1 Status
LANE2_DIG_RX_STAT_STAT_CNT_0	0x1287	W	0x00000000	Stat counter 0 Status
LANE2_DIG_RX_STAT_STAT_CNT_1	0x1288	W	0x00000000	Stat counter 1 Status
LANE2_DIG_RX_STAT_STAT_CNT_2	0x1289	W	0x00000000	Stat counter 2 Status
LANE2_DIG_RX_STAT_STAT_CNT_3	0x128A	W	0x00000000	Stat counter 3 Status
LANE2_DIG_RX_STAT_STAT_CNT_4	0x128B	W	0x00000000	Stat counter 4 Status
LANE2_DIG_RX_STAT_STAT_CNT_5	0x128C	W	0x00000000	Stat counter 5 Status
LANE2_DIG_RX_STAT_STAT_CNT_6	0x128D	W	0x00000000	Stat counter 6 Status
LANE2_DIG_RX_STAT_CAL_COMP_CLK_CTL	0x128E	W	0x00000019	Calibration Comparator Control

Name	Offset	Size	Reset Value	Description
LANE2_DIG_RX_STAT_MATCH_CTL2	0x128F	W	0x00000000	Stat match controls register #2
LANE2_DIG_RX_STAT_MATCH_CTL3	0x1290	W	0x00000000	Stat match controls register #3
LANE2_DIG_RX_STAT_MATCH_CTL4	0x1291	W	0x00000000	Stat match controls register #4
LANE2_DIG_RX_STAT_MATCH_CTL5	0x1292	W	0x00000000	Stat match controls register #5
LANE2_DIG_RX_STAT_STAT_CTL2	0x1293	W	0x00000000	Stat controls register #2
LANE2_DIG_RX_STAT_STAT_STOP	0x1294	W	0x00000000	Stat stop register
LANE2_DIG_ANA_TX_OVRD_OUT	0x12A0	W	0x00000000	Override values for TX signals going to ANA
LANE2_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT	0x12A1	W	0x00000000	Feature enable for tx_ana_lpbk_dfe_mode
LANE2_DIG_ANA_RX_DIV_OVRD_OUT	0x12A6	W	0x00000000	Override values for RX control signals going to ANA
LANE2_DIG_ANA_RX_CTL_OVRD_OUT	0x12A7	W	0x00000000	Override values for RX control signals going to ANA
LANE2_DIG_ANA_RX_PWR_OVRD_OUT	0x12A8	W	0x00000000	Override values for RX PWR UP/DN signals going to ANA
LANE2_DIG_ANA_RX_VCO_OVRD_OUT_0	0x12A9	W	0x00000000	Override values for RX VCO signals going to ANA #0
LANE2_DIG_ANA_RX_VCO_OVRD_OUT_1	0x12AA	W	0x00000002	Override values for RX VCO signals going to ANA #1
LANE2_DIG_ANA_RX_VCO_OVRD_OUT_2	0x12AB	W	0x00000000	Override values for RX VCO signals going to ANA #2
LANE2_DIG_ANA_RX_CAL	0x12AC	W	0x00000000	Sets values for RX CAL signals going to ANA register
LANE2_DIG_ANA_RX_DAC_CTRL	0x12AD	W	0x00000080	Sets values for RX DAC CTRL value going to ANA
LANE2_DIG_ANA_RX_DAC_CTRL_OVRD	0x12AE	W	0x00000000	Overrides RX DAC CTRL bus (en/val/sel) going to ANA
LANE2_DIG_ANA_RX_DAC_CTRL_SEL	0x12AF	W	0x00000000	Sets values for RX DAC CTRL Select signal going to ANA
LANE2_DIG_ANA_RX_AFE_ATT_VGA	0x12B0	W	0x00003000	Value for RX AFE ATT & VGA signals going to ANA
LANE2_DIG_ANA_RX_AFE_CTLE	0x12B1	W	0x00000000	Values for RX AFE CTLE signals going to ANA
LANE2_DIG_ANA_RX_SCOPE	0x12B2	W	0x00000000	Values for RX SCOPE signals going to ANA
LANE2_DIG_ANA_RX_SLICER_CTRL	0x12B3	W	0x00000077	Sets values for RX slicer ctrl signals going to ANA register
LANE2_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST	0x12B4	W	0x00000007	Sets values for RX ANA IQ phase adjust signal going to ANA register
LANE2_DIG_ANA_RX_ANA_IQ_SENSE_EN	0x12B5	W	0x00000000	Sets values for RX ANA IQ SENSE signal
LANE2_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN	0x12B6	W	0x00000000	DAC CTRL enable signal

Name	Offset	Size	Reset Value	Description
LANE2_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE	0x12B7	W	0x00000000	Afe update enable signal
LANE2_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK	0x12B8	W	0x00000000	PHASE adjust clock signal
LANE2_DIG_ANA_STATUS_0	0x12B9	W	0x00000000	Lane input status register #0
LANE2_DIG_ANA_STATUS_1	0x12BA	W	0x00000000	Lane input status register #1
LANE2_DIG_ANA_STATUS_LOS	0x12BB	W	0x00000000	LOS status at ana interface
LANE2_DIG_ANA_CREGS_TX_ANA_ATB_REG	0x12C0	W	0x00000000	TX ANA ATB measurement control register
LANE2_DIG_ANA_CREGS_RX_ANA_EQ_CTRL	0x12C4	W	0x00000034	RX ANA EQ control register
LANE2_DIG_ANA_CREGS_RX_ANA_VCO_CTRL	0x12C5	W	0x00000004	RX ANA VCO control register
LANE2_DIG_ANA_CREGS_RX_ANA_VREG_CTRL	0x12C6	W	0x00000001	RX ANA VREG control register
LANE2_DIG_ANA_CREGS_RX_ANA_DISCONNECT	0x12C7	W	0x00000000	RX ANA disconnect control
LANE2_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL	0x12C8	W	0x00000000	RX ANA reserved control register
LANE2_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1	0x12C9	W	0x00000000	RX ANA ATB control register 1
LANE2_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2	0x12CA	W	0x00000000	RX ANA ATB control register 2
LANE3_DIG_ASIC_LANE_OVRD_IN	0x1300	W	0x00000000	Override values for incoming LANE controls from ASIC
LANE3_DIG_ASIC_RX_ASIC_LOS	0x1301	W	0x00000000	LOS Related signals
LANE3_DIG_ASIC_LOS_OVRD_IN	0x1302	W	0x00000010	Override values for LOS signal at ASIC side
LANE3_DIG_ASIC_LOS_OVRD_IN_1	0x1303	W	0x0000005A	Override values for LOS signal at ASIC side
LANE3_DIG_ASIC_CDR_CONTROL_OVRD_IN	0x1306	W	0x00000000	Override values for incoming CDR settings controls from ASIC
LANE3_DIG_ASIC_RX_OVRD_IN_0	0x1307	W	0x00000000	Override values for incoming RX controls from ASIC, register #0
LANE3_DIG_ASIC_RX_OVRD_IN_1	0x1308	W	0x00000014	Override values for incoming RX controls from ASIC, register #1
LANE3_DIG_ASIC_RX_OVRD_IN_2	0x1309	W	0x000003E8	Override values for incoming RX controls from ASIC, register #2
LANE3_DIG_ASIC_RX_OVRD_IN_3	0x130A	W	0x00000000	Override values for incoming RX controls from ASIC, register #3
LANE3_DIG_ASIC_RX_OVRD_IN_4	0x130B	W	0x00000000	Override values for incoming RX controls from ASIC, register #4
LANE3_DIG_ASIC_RX_OVRD_IN_5	0x130C	W	0x00000000	Override values for incoming RX controls from ASIC, register #5
LANE3_DIG_ASIC_RX_OVRD_EQ_IN_0	0x130D	W	0x00003078	Override values for incoming RX EQ controls from ASIC, register #0

Name	Offset	Size	Reset Value	Description
LANE3_DIG_ASIC_RX_OVRD_EQ_IN_1	0x130E	W	0x00004040	Override values for incoming RX EQ controls from ASIC, register #1
LANE3_DIG_ASIC_RX_OVRD_OUT_0	0x130F	W	0x00000000	Override values for outgoing RX controls to ASIC, register #0
LANE3_DIG_ASIC_RX_ASIC_IN_0	0x1315	W	0x00000000	Current values for incoming RX controls from ASIC, register #0
LANE3_DIG_ASIC_RX_ASIC_IN_1	0x1316	W	0x00000000	Current values for incoming RX controls from ASIC, register #1
LANE3_DIG_ASIC_RX_EQ_ASIC_IN_0	0x1317	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #0
LANE3_DIG_ASIC_RX_EQ_ASIC_IN_1	0x1318	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #1
LANE3_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0	0x1319	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #0
LANE3_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1	0x131A	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #1
LANE3_DIG_ASIC_RX_ASIC_OUT_0	0x131B	W	0x00000000	Current values for outgoing RX status controls from PHY, register #0
LANE3_DIG_LBERT_CTL	0x1320	W	0x00000000	Pattern Generator controls
LANE3_DIG_RX_CDR_CDR_CTL_0	0x1324	W	0x0000000F	Control bits for receiver in recovered domain
LANE3_DIG_RX_CDR_CDR_CTL_1	0x1325	W	0x00007039	CDR Control Register #1
LANE3_DIG_RX_CDR_CDR_CTL_2	0x1326	W	0x00004ABB	CDR Control Register #2
LANE3_DIG_RX_CDR_CDR_CTL_3	0x1327	W	0x0000099B	CDR Control Register #3
LANE3_DIG_RX_CDR_CDR_CTL_4	0x1328	W	0x00000003	CDR Control Register #4
LANE3_DIG_RX_CDR_CDR_CTL_5	0x1329	W	0x00000649	CDR Control Register #5
LANE3_DIG_RX_CDR_CDR_CTL_6	0x132A	W	0x000006DB	CDR Control Register #6
LANE3_DIG_RX_CDR_CDR_CTL_7	0x132B	W	0x00008766	CDR Control Register #7
LANE3_DIG_RX_CDR_CDR_CTL_8	0x132C	W	0x0000ECCA	CDR Control Register #8
LANE3_DIG_RX_CDR_CDR_CTL_9	0x132D	W	0x00006432	CDR Control Register #9
LANE3_DIG_RX_CDR_CDR_CTL_10	0x132E	W	0x0000ECA8	CDR Control Register #10
LANE3_DIG_RX_CDR_STAT	0x132F	W	0x00000000	Current output values to dpll (phug, frug)
LANE3_DIG_RX_PWRCTL_RX_PSTATE_P0	0x1340	W	0x00000CF7	RX Power State Control Register for P0
LANE3_DIG_RX_PWRCTL_RX_PSTATE_P0S	0x1341	W	0x00000407	RX Power State Control Register for P0S

Name	Offset	Size	Reset Value	Description
LANE3_DIG_RX_PWRCTL_RX_PSTATE_P1	0x1342	W	0x00000307	RX Power State Control Register for P1
LANE3_DIG_RX_PWRCTL_RX_PSTATE_P2	0x1343	W	0x00000301	RX Power State Control Register for P2
LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_0	0x1344	W	0x000001E6	RX Power UP Time Register #0
LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_1	0x1345	W	0x0000069A	RX Power UP Time Register #1
LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_2	0x1346	W	0x0000001A	RX Power UP Time Register #2
LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_3	0x1347	W	0x00000000	RX Power UP Time Register #3
LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0	0x1348	W	0x00000400	RX VCO calibration controls register #0
LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1	0x1349	W	0x00000100	RX VCO calibration controls register #1
LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2	0x134A	W	0x00002600	RX VCO calibration controls register #2
LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0	0x134B	W	0x00003319	RX Power UP Time Register #0
LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1	0x134C	W	0x00000003	RX Power UP Time Register #1
LANE3_DIG_RX_VCOCAL_RX_VCO_STAT_0	0x134D	W	0x00000000	RX VCO status register #0
LANE3_DIG_RX_VCOCAL_RX_VCO_STAT_1	0x134E	W	0x00000000	RX VCO status register #1
LANE3_DIG_RX_VCOCAL_RX_VCO_STAT_2	0x134F	W	0x00000000	RX VCO status register #2
LANE3_DIG_RX_RX_ALIGN_XAUI_COMM_MASK	0x1350	W	0x000003FF	XAUI_COMMA mask
LANE3_DIG_RX_LBERT_CTL	0x1351	W	0x00000000	Pattern Matcher controls
LANE3_DIG_RX_LBERT_ERR	0x1352	W	0x00000000	Pattern match error counter
LANE3_DIG_RX_RX_LOS_LOS_0	0x1353	W	0x00000062	LOS Control Register #1
LANE3_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS	0x1355	W	0x00000000	Status of rx_pwrsm_state
LANE3_DIG_RX_DPLL_FREQ	0x135C	W	0x00002000	Current frequency integrator value.
LANE3_DIG_RX_DPLL_FREQ_BOUND_0	0x135D	W	0x000004C8	Frequency Bounds for incoming data stream #0
LANE3_DIG_RX_DPLL_FREQ_BOUND_1	0x135E	W	0x0000019C	Frequency Bounds for incoming data stream #1
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_0	0x1360	W	0x00000C10	Adaptation Configuration Register #0
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_1	0x1361	W	0x00000009	Adaptation Configuration Register #1
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_2	0x1362	W	0x000000C2	Adaptation Configuration Register #2
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_3	0x1363	W	0x00000000	Adaptation Configuration Register #3

Name	Offset	Size	Reset Value	Description
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_4	0x1364	W	0x00000000	Adaptation Configuration Register #4
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_5	0x1365	W	0x00000000	Adaptation Configuration Register #5
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_6	0x1366	W	0x0000792B	Adaptation Configuration Register #6
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_7	0x1367	W	0x00004342	Adaptation Configuration Register #7
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_8	0x1368	W	0x00004925	Adaptation Configuration Register #8
LANE3_DIG_RX_ADPTCTL_ADPT_CFG_9	0x1369	W	0x00000000	Adaptation Configuration Register #9
LANE3_DIG_RX_ADPTCTL_RST_ADPT_CFG	0x136A	W	0x0000001F	Reset adaptation Configuration Register
LANE3_DIG_RX_ADPTCTL_ATT_STATUS	0x136B	W	0x00000000	Value of ATT adaptation code
LANE3_DIG_RX_ADPTCTL_VGA_STATUS	0x136C	W	0x00000000	Value of VGA adaptation code
LANE3_DIG_RX_ADPTCTL_CTLE_STATUS	0x136D	W	0x00000000	Value of CTLE adaptation code
LANE3_DIG_RX_ADPTCTL_DFE_TAP1_STATUS	0x136E	W	0x00000000	Value of DFE Tap1 adaptation code
LANE3_DIG_RX_ADPTCTL_DFE_TAP2_STATUS	0x136F	W	0x00000000	Value of DFE Tap2 adaptation code
LANE3_DIG_RX_ADPTCTL_DFE_TAP3_STATUS	0x1370	W	0x00000000	Value of DFE Tap3 adaptation code
LANE3_DIG_RX_ADPTCTL_DFE_TAP4_STATUS	0x1371	W	0x00000000	Value of DFE Tap4 adaptation code
LANE3_DIG_RX_ADPTCTL_DFE_TAP5_STATUS	0x1372	W	0x00000000	Value of DFE Tap5 adaptation code
LANE3_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST	0x1373	W	0x00000080	Offset values for RX DFE data even vDAC
LANE3_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST	0x1374	W	0x00000080	Offset values for RX DFE data odd vDAC
LANE3_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN	0x1375	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
LANE3_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD	0x1376	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
LANE3_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST	0x1377	W	0x00000080	Offset values for RX DFE error even vDAC
LANE3_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST	0x1378	W	0x00000080	Offset values for RX DFE error odd vDAC
LANE3_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL	0x1379	W	0x00000000	Value of error slicer level
LANE3_DIG_RX_ADPTCTL_ADPT_RESET	0x137A	W	0x00000000	Adaptation reset register
LANE3_DIG_RX_STAT_LD_VAL_1	0x1380	W	0x00000040	Stat load value for the sample counter #1

Name	Offset	Size	Reset Value	Description
LANE3_DIG_RX_STAT_DATA_MSK	0x1381	W	0x0000FFFF	Stat data mask bits [15:0]
LANE3_DIG_RX_STAT_MATCH_CTL0	0x1382	W	0x00003C06	Stat match controls register #0
LANE3_DIG_RX_STAT_MATCH_CTL1	0x1383	W	0x00000800	Stat match controls register #1
LANE3_DIG_RX_STAT_STAT_CTL0	0x1384	W	0x00004000	Stat controls register #0
LANE3_DIG_RX_STAT_STAT_CTL1	0x1385	W	0x00000008	Stat controls register #1
LANE3_DIG_RX_STAT_SMPL_CNT1	0x1386	W	0x00000000	Sample counter #1 Status
LANE3_DIG_RX_STAT_STAT_CNT_0	0x1387	W	0x00000000	Stat counter 0 Status
LANE3_DIG_RX_STAT_STAT_CNT_1	0x1388	W	0x00000000	Stat counter 1 Status
LANE3_DIG_RX_STAT_STAT_CNT_2	0x1389	W	0x00000000	Stat counter 2 Status
LANE3_DIG_RX_STAT_STAT_CNT_3	0x138A	W	0x00000000	Stat counter 3 Status
LANE3_DIG_RX_STAT_STAT_CNT_4	0x138B	W	0x00000000	Stat counter 4 Status
LANE3_DIG_RX_STAT_STAT_CNT_5	0x138C	W	0x00000000	Stat counter 5 Status
LANE3_DIG_RX_STAT_STAT_CNT_6	0x138D	W	0x00000000	Stat counter 6 Status
LANE3_DIG_RX_STAT_CAL_COMP_CLK_CTL	0x138E	W	0x00000019	Calibration Comparator Control
LANE3_DIG_RX_STAT_MATCH_CTL2	0x138F	W	0x00000000	Stat match controls register #2
LANE3_DIG_RX_STAT_MATCH_CTL3	0x1390	W	0x00000000	Stat match controls register #3
LANE3_DIG_RX_STAT_MATCH_CTL4	0x1391	W	0x00000000	Stat match controls register #4
LANE3_DIG_RX_STAT_MATCH_CTL5	0x1392	W	0x00000000	Stat match controls register #5
LANE3_DIG_RX_STAT_STAT_CTL2	0x1393	W	0x00000000	Stat controls register #2
LANE3_DIG_RX_STAT_STAT_STOP	0x1394	W	0x00000000	Stat stop register
LANE3_DIG_ANA_TX_OVRD_OUT	0x13A0	W	0x00000000	Override values for TX signals going to ANA
LANE3_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT	0x13A1	W	0x00000000	Feature enable for tx_ana_lpbk_dfe_mode
LANE3_DIG_ANA_RX_DIV_OVRD_OUT	0x13A6	W	0x00000000	Override values for RX control signals going to ANA
LANE3_DIG_ANA_RX_CTL_OVRD_OUT	0x13A7	W	0x00000000	Override values for RX control signals going to ANA
LANE3_DIG_ANA_RX_PWR_OVRD_OUT	0x13A8	W	0x00000000	Override values for RX PWR UP/DN signals going to ANA
LANE3_DIG_ANA_RX_VCO_OVRD_OUT_0	0x13A9	W	0x00000000	Override values for RX VCO signals going to ANA #0

Name	Offset	Size	Reset Value	Description
LANE3_DIG_ANA_RX_VCO_OVRD_OUT_1	0x13AA	W	0x00000002	Override values for RX VCO signals going to ANA #1
LANE3_DIG_ANA_RX_VCO_OVRD_OUT_2	0x13AB	W	0x00000000	Override values for RX VCO signals going to ANA #2
LANE3_DIG_ANA_RX_CAL	0x13AC	W	0x00000000	Sets values for RX CAL signals going to ANA register
LANE3_DIG_ANA_RX_DAC_CTRL	0x13AD	W	0x00000080	Sets values for RX DAC CTRL value going to ANA
LANE3_DIG_ANA_RX_DAC_CTRL_OVRD	0x13AE	W	0x00000000	Overrides RX DAC CTRL bus (en/val/sel) going to ANA
LANE3_DIG_ANA_RX_DAC_CTRL_SEL	0x13AF	W	0x00000000	Sets values for RX DAC CTRL Select signal going to ANA
LANE3_DIG_ANA_RX_AFE_ATT_VGA	0x13B0	W	0x00003000	Value for RX AFE ATT & VGA signals going to ANA
LANE3_DIG_ANA_RX_AFE_CTLE	0x13B1	W	0x00000000	Values for RX AFE CTLE signals going to ANA
LANE3_DIG_ANA_RX_SCOPE	0x13B2	W	0x00000000	Values for RX SCOPE signals going to ANA
LANE3_DIG_ANA_RX_SLICER_CTRL	0x13B3	W	0x00000077	Sets values for RX slicer ctrl signals going to ANA register
LANE3_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST	0x13B4	W	0x00000007	Sets values for RX ANA IQ phase adjust signal going to ANA register
LANE3_DIG_ANA_RX_ANA_IQ_SENSE_EN	0x13B5	W	0x00000000	Sets values for RX ANA IQ SENSE signal
LANE3_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN	0x13B6	W	0x00000000	DAC CTRL enable signal
LANE3_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE	0x13B7	W	0x00000000	Afe update enable signal
LANE3_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK	0x13B8	W	0x00000000	PHASE adjust clock signal
LANE3_DIG_ANA_STATUS_0	0x13B9	W	0x00000000	Lane input status register #0
LANE3_DIG_ANA_STATUS_1	0x13BA	W	0x00000000	Lane input status register #1
LANE3_DIG_ANA_STATUS_LOS	0x13BB	W	0x00000000	LOS status at ana interface
LANE3_DIG_ANA_CREGS_TX_ANA_ATB_REG	0x13C0	W	0x00000000	TX ANA ATB measurement control register
LANE3_DIG_ANA_CREGS_RX_ANA_EQ_CTRL	0x13C4	W	0x00000034	RX ANA EQ control register
LANE3_DIG_ANA_CREGS_RX_ANA_VCO_CTRL	0x13C5	W	0x00000004	RX ANA VCO control register
LANE3_DIG_ANA_CREGS_RX_ANA_VREG_CTRL	0x13C6	W	0x00000001	RX ANA VREG control register
LANE3_DIG_ANA_CREGS_RX_ANA_DISCONNECT	0x13C7	W	0x00000000	RX ANA disconnect control
LANE3_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL	0x13C8	W	0x00000000	RX ANA reserved control register
LANE3_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1	0x13C9	W	0x00000000	RX ANA ATB control register 1

Name	Offset	Size	Reset Value	Description
LANE3_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2	0x13CA	W	0x00000000	RX ANA ATB control register 2
RAWCMN_DIG_CMN_CTL	0x2000	W	0x00000000	Common control register
RAWCMN_DIG_CR_EXT_REG_OP_XTND	0x2001	W	0x00000000	external interface XTND control register
RAWCMN_DIG_CMN_CTL_1	0x2002	W	0x00000000	Common control register 1
RAWCMN_DIG_AON_CMN_ADAPT_REF_LVL_DAC_CODE	0x2020	W	0x00000044	Override values for incoming SUP signals
RAWCMN_DIG_AON_CMN_RX_RESERVED_REGISTER_0	0x2021	W	0x00000000	Reserved Register 0
RAWCMN_DIG_AON_CMN_RX_RESERVED_REGISTER_1	0x2022	W	0x00000000	Reserved Register 1
RAWCMN_DIG_AON_CMN_SUP_OVRD_IN	0x203B	W	0x00000000	Override values for incoming SUP signals
RAWCMN_DIG_CMNFSM_FSM_FSM_OVRD_CTL	0x2040	W	0x00000000	FSM override control register
RAWCMN_DIG_CMNFSM_FSM_MEM_ADDR_MON	0x2041	W	0x00000000	Memory Address Monitor
RAWCMN_DIG_CMNFSM_FSM_STATUS_MON	0x2042	W	0x00000000	FSM Status Monitor
RAWCMN_DIG_CMNFSM_FSM_CR_REG_OP_XTND_EN	0x2043	W	0x00000000	CR interface timing extension enable
RAWCMN_DIG_CMNFSM_ATB_REQ	0x2044	W	0x00000000	ATB req control register
RAWCMN_DIG_CMNFSM_ATB_RESULT_OUT	0x2045	W	0x00000000	ATB done and result control register
HDMIPCS_DIG_CTRL_XF_HDMI_PWR_CTRL	0x2080	W	0x00000000	Override for HDMI power controls to and from controller
HDMIPCS_DIG_CTRL_XF_REF_FREQ_INFO_OVRD	0x2081	W	0x00000164	ref freq info config and overrides
HDMIPCS_DIG_CTRL_XF_HDMI_CONFIG_OVRD	0x2082	W	0x00000303	Override for HDMI config controls from controller
HDMIPCS_DIG_CTRL_XF_LTP_UPDATE_STATUS_OVRD	0x2083	W	0x00000000	LTP update overrides to and from controller
HDMIPCS_DIG_CTRL_XF_LTP_REQ_OVRD	0x2084	W	0x00000000	Override for LTP req config controls from controller
HDMIPCS_DIG_CTRL_XF_LTP_OVRD_EN	0x2085	W	0x00000000	Override en for LTP req controls to controller
HDMIPCS_DIG_CTRL_XF_LTP_CTRL_OVRD	0x2086	W	0x00000000	LTP controls overrides to and from controller
HDMIPCS_DIG_CTRL_XF_READAPT_EN	0x2087	W	0x00000000	reg for re-adapt request
HDMIPCS_DIG_CTRL_XF_PCS_INTERFACE_SIG_STATUS_1	0x2088	W	0x00000000	read regs for inputs/outputs from/to controller
HDMIPCS_DIG_CTRL_XF_PCS_INTERFACE_SIG_STATUS_2	0x2089	W	0x00000000	read regs for outputs to controller

Name	Offset	Size	Reset Value	Description
HDMIPCS_DIG_CTRL_XF_POWER_SEQ	0x208A	W	0x00000000	read regs for power sequence signals
HDMIPCS_DIG_CTRL_XF_LINK_RETRAIN_REQ_ASIC_OVRD	0x208B	W	0x00000000	Override for link_retrain_req from ASIC
HDMIPCS_DIG_CTRL_XF_LINK_RETRAIN_REQ	0x208C	W	0x00000000	reg for link_retrain request
HDMIPCS_DIG_CTRL_XF_LINK_RETRAIN_REQ_INFO_OVRD	0x208D	W	0x00000000	Override for link_retrain_req_int
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_6G_EQ_SETTINGS	0x2094	W	0x0000A1FF	EQ settings for HDMI2.1 6Gbps in 3/4 lane mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_8G_EQ_SETTINGS	0x2095	W	0x0000A1FF	EQ settings for HDMI2.1 8Gbps in 4 lane mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_10G_EQ_SETTINGS	0x2096	W	0x0000C1FF	EQ settings for HDMI2.1 10Gbps in 4 lane mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_12G_EQ_SETTINGS	0x2097	W	0x0000C1FF	EQ settings for HDMI2.1 12Gbps in 4 lane mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_3G_EQ_SETTINGS_TAP	0x2098	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI2.1 (3Gbps in 3 lane mode)
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_6G_EQ_SETTINGS_TAP	0x2099	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI2.1 (6Gbps in 3/4 lane mode)
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_8G_EQ_SETTINGS_TAP	0x209A	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI2.1 (8Gbps in 4 lane mode)
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_10G_EQ_SETTINGS_TAP	0x209B	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI2.1 (10Gbps in 4 lane mode)
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_12G_EQ_SETTINGS_TAP	0x209C	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI2.1 (12Gbps in 4 lane mode)
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_TMDSCLK_THRESH	0x209D	W	0x0000320F	Low and high thresholds for clock_stable from tmdsclk
HDMIPCS_DIG_DATA_PATH_DATA_PATH_INPUTS	0x20A0	W	0x00000400	Inputs and overrides for data path controls
HDMIPCS_DIG_DATA_PATH_DATA_PATH_INPUT_OVRD	0x20A1	W	0x00000000	overrides for data path inputs

Name	Offset	Size	Reset Value	Description
HDMIPCS_DIG_DATA_PATH_FRL_COMMA_CHAR	0x20A2	W	0x00001011	FRL mode comma character control word
HDMIPCS_DIG_DATA_PATH_FRL_VALID_DATA_TIMEOUT	0x20A3	W	0x00000E2B	FRL mode data absense timeout
HDMIPCS_DIG_DATA_PATH_FRL_DATA_LOCK_DETECT_TIMEOUT	0x20A4	W	0x00005545	FRL mode FLT data timeout
HDMIPCS_DIG_DATA_PATH_DATA_PATH_OUTPUT_OVRD	0x20A5	W	0x00000000	overrides for data path outputs
HDMIPCS_DIG_DATA_PATH_GSKT_STATUS	0x20A6	W	0x00000000	Status of gasket_rd_pos
HDMIPCS_DIG_DATA_PATH_BYTE_ALIGN_STATUS	0x20A7	W	0x00000000	Status of byte_aligned signals
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_RATE_CALC_OVRD	0x20C0	W	0x00000000	overrides for FSM to RATE CALCULATOR
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_PHY_CONTROL	0x20C1	W	0x000000A2	PHY controls and settings
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_PCS_DEBUG	0x20C2	W	0x00000000	PCS Debug related signals
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LTP_PATTERN_REQ	0x20C3	W	0x00005678	LTP_REQ for PATTERNS
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_CONFIG	0x20C4	W	0x000003E5	FSM configurations to modify behavior
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LTP_STATUS_UPDATE	0x20C5	W	0x00000FE0	LTP_REQ for STATUS UPDATE
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_CONTROL	0x20C6	W	0x00000000	FSM controls to force behavior
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_ADAPT_REF_FOM	0x20C7	W	0x00000080	Minimum reference FOM needed for successful LTP
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_HDMI_STATUS	0x20C8	W	0x00000000	main_FSM important status indicators
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FFE_STATUS	0x20C9	W	0x00000000	TxFFE adaptation related important status indicators
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_POWER_STATUS	0x20CA	W	0x00000000	Power Consumption status indicators
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_MISC_STATUS	0x20CB	W	0x00000000	Power Consumption status indicators
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FOM_LANE01	0x20CC	W	0x00000000	BEST FOM achieved in lane 0 and 1

Name	Offset	Size	Reset Value	Description
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FOM_LANE23	0x20CD	W	0x00000000	BEST FOM achieved in lane 2 and 3
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_INPUT_OVRD	0x20CE	W	0x000000F0	overrides for inputs to FSM
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_STATE_STATUS	0x20CF	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_STATE_STATUS
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_1	0x20D0	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_1
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_2	0x20D1	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_2
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_3	0x20D2	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_3
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_4	0x20D3	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_4
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_BYTE_ALIGN_CNT_STATUS	0x20D4	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_BYTE_ALIGN_CNT_STATUS
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LANE_VALID_STATUS	0x20D5	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LANE_VALID_STATUS
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_5	0x20D6	W	0x00000000	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_5
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_STRESS_TARGET_CNT	0x20D7	W	0x000000FF	Stress wait time before BOOTUP
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_STRESS_CNTR_STATUS	0x20D8	W	0x00000000	Stress counter value
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LOS_SETTINGS	0x20D9	W	0x000002D3	Settings for LOS
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LOS_SETTINGS_1	0x20DA	W	0x00000040	Settings for LOS
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FRL_FAST_RELOCK	0x20DB	W	0x00000000	FRL fast relock
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_1	0x20E0	W	0x0000012C	Register to program first rate boundary to calculate rx_rate in TMDS mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_2	0x20E1	W	0x00000258	Register to program second rate boundary to calculate rx_rate in TMDS mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_3	0x20E2	W	0x000004B0	Register to program third rate boundary to calculate rx_rate in TMDS mode

Name	Offset	Size	Reset Value	Description
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_4	0x20E3	W	0x00000960	Register to program forth rate boundary to calculate rx_rate in TMDS mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_TMDS_VCO_REF_CNT_REG	0x20E4	W	0x000008C0	Register to select reference clock and target VCO counts in TMDS mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_FRL_VCO_CNT_REG	0x20E5	W	0x000008C0	Register to select reference clock and target VCO counts in FRL mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_TMDS_TIMEBASE_LOCK_THRES_REG	0x20E6	W	0x00000186	Register to program timebase and lock_thresh in TMDS mode
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_1_REG	0x20E7	W	0x000071E6	First Sector for rx_cdr_setting_sel in HDMI14
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_2_REG	0x20E8	W	0x00006248	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_2_REG
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_3_REG	0x20E9	W	0x000052DA	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_3_REG
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_4_REG	0x20EA	W	0x000043CD	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_4_REG
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_5_REG	0x20EB	W	0x000035B3	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_5_REG
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_ADAPT_EN_BOUNDARY_REG	0x20EC	W	0x00000672	data_rate threshold for afe and dfe en
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_EQ_SETTINGS	0x20ED	W	0x000071EF	EQ settings for HDMI1.4
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_165_EQ_SETTINGS	0x20EE	W	0x000071FF	EQ settings for HDMI1.4 for 1.65gbps data rate and above
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI20_EQ_SETTINGS	0x20EF	W	0x0000A1FF	EQ settings for HDMI2.0
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_CDR_SETTING_SEL	0x20F0	W	0x00000000	settings for rx_cdr_setting_sel in HDMI2.1 for all data rates

Name	Offset	Size	Reset Value	Description
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_EQ_SETTINGS_TAP	0x20F1	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI1.4 for less than 1.65gbps
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI20_CDR_SETTING_SEL	0x20F2	W	0x00000000	settings for rx_cdr_setting_sel in HDMI2.0
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI_DATA_RATE	0x20F3	W	0x00000000	Data Rate calulated by CMU
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_EQ_SETTINGS_MISC_1	0x20F4	W	0x00000124	EQ settings for delta_iq
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_CDR_HIGHFREQ_THRES	0x20F5	W	0x00001388	Threshold for CDR high_freq
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_CDR_LOWFREQ_THRES	0x20F6	W	0x00000DAC	Threshold for CDR low_freq
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_1	0x20F7	W	0x00001010	First two thresholds for ref_range divison
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_3	0x20F8	W	0x00002030	thresholds for ref_range divison
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_5	0x20F9	W	0x00003050	Fifth and sixth thresholds for ref_range divison
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_7	0x20FA	W	0x00000070	seventh thresholds for ref_range divison
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_6_REG	0x20FB	W	0x00002799	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_6_REG
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_7_REG	0x20FC	W	0x00001B65	HDMI20RXPHY_NS_HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_7_REG
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_165_EQ_SETTINGS_TAP	0x20FD	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI1.4 for more than 1.65gbps
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI20_EQ_SETTINGS_TAP	0x20FE	W	0x00000000	EQ settings for dfe_tap1 and dfe_tap2 in HDMI2.0
HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_3G_EQ_SETTINGS	0x20FF	W	0x000071FF	EQ settings for HDMI2.1 3Gbps in 3 lane mode
RAWLANE0_DIG_PCS_XF_RX_OVRD_OUT_2	0x3003	W	0x00000000	Override values for outgoing RX controls to PCS register #2

Name	Offset	Size	Reset Value	Description
RAWLANE0_DIG_PCS_XF_RX_PCS_IN_5	0x3004	W	0x00000000	Current values for incoming RX controls from PCS, register #5
RAWLANE0_DIG_PCS_XF_RX_OVRD_IN	0x3005	W	0x00000200	Override values for incoming RX controls from PCS
RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_1	0x3006	W	0x00000007	Override values for incoming RX controls from PCS, register #1
RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_2	0x3007	W	0x00000000	Override values for incoming RX controls from PCS, register #2
RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_3	0x3008	W	0x00000000	Override values for incoming RX controls from PCS, register #3
RAWLANE0_DIG_PCS_XF_RX_PCS_IN	0x3009	W	0x00000000	Current values for incoming RX controls from PCS
RAWLANE0_DIG_PCS_XF_RX_PCS_IN_1	0x300A	W	0x00000000	Current values for incoming RX controls from PCS, register #1
RAWLANE0_DIG_PCS_XF_RX_PCS_IN_2	0x300B	W	0x00000000	Current values for incoming RX controls from PCS, register #2
RAWLANE0_DIG_PCS_XF_RX_PCS_IN_3	0x300C	W	0x00000000	Current values for incoming RX controls from PCS, register #3
RAWLANE0_DIG_PCS_XF_RX_PCS_IN_4	0x300D	W	0x00000000	Current values for incoming RX controls from PCS, register #4
RAWLANE0_DIG_PCS_XF_RX_OVRD_OUT	0x300E	W	0x00000003	Override values for outgoing RX controls to PCS
RAWLANE0_DIG_PCS_XF_RX_PCS_OUT	0x300F	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE0_DIG_PCS_XF_RX_ADAPT_ACK	0x3010	W	0x00000000	RX adaptation Acknowledge
RAWLANE0_DIG_PCS_XF_RX_ADAPT_FOM	0x3011	W	0x00000000	RX adaptation figure of merit
RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_4	0x3012	W	0x00000000	Override values for incoming RX controls from PCS, register #4
RAWLANE0_DIG_PCS_XF_RX_PCS_OUT_2	0x3013	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE0_DIG_PCS_XF_LANE_NUMBER	0x3015	W	0x00000000	Current lane number
RAWLANE0_DIG_PCS_XF_ATE_OVRD_IN	0x3018	W	0x00000000	ATE override input to control top-level inputs
RAWLANE0_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN	0x3019	W	0x00000000	Override incoming values for rx_eq_delta_iq
RAWLANE0_DIG_PCS_XF_RX_EQ_OVRD_IN_1	0x301D	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #1
RAWLANE0_DIG_PCS_XF_RX_EQ_OVRD_IN_2	0x301E	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #2
RAWLANE0_DIG_FSM_FSM_FSM_OVRD_CTL	0x3020	W	0x00000000	FSM override control register
RAWLANE0_DIG_FSM_FSM_MEM_ADDR_MON	0x3021	W	0x00000000	Memory Address Monitor
RAWLANE0_DIG_FSM_FSM_STATUS_MON	0x3022	W	0x00000000	FSM Status Monitor
RAWLANE0_DIG_FSM_FSM_CR_REG_OP_XTND_EN	0x3023	W	0x00000000	CR interface timing extension enable
RAWLANE0_DIG_FSM_FAST_RX_STARTUP_CAL	0x3024	W	0x00000000	Status of fast RX Start Up Calibration

Name	Offset	Size	Reset Value	Description
RAWLANE0_DIG_FSM_FAST_RX_ADAPT	0x3025	W	0x00000000	Status of fast RX adaptation
RAWLANE0_DIG_FSM_FAST_RX_AFE_CAL	0x3026	W	0x00000000	Status of fast RX AFE Calibration
RAWLANE0_DIG_FSM_FAST_RX_DFE_CAL	0x3027	W	0x00000000	Status of fast RX DFE Calibration
RAWLANE0_DIG_FSM_FAST_RX_BYPASS_CAL	0x3028	W	0x00000000	Status of fast RX bypass Calibration
RAWLANE0_DIG_FSM_FAST_RX_REFLVL_CAL	0x3029	W	0x00000000	Status of fast RX Reference level Calibration
RAWLANE0_DIG_FSM_FAST_RX_IQ_CAL	0x302A	W	0x00000000	Status of fast RX IQ Calibration
RAWLANE0_DIG_FSM_FAST_RX_AFE_ADAPT	0x302B	W	0x00000000	Status of fast RX AFE adaptation
RAWLANE0_DIG_FSM_FAST_RX_DFE_ADAPT	0x302C	W	0x00000000	Status of fast RX DFE adaptation
RAWLANE0_DIG_FSM_FAST_SUP	0x302D	W	0x00000000	Status of fast support block
RAWLANE0_DIG_FSM_FAST_RX_IQ_WALK	0x302E	W	0x00000000	Status of fast RX IQ walk start-up adaptation
RAWLANE0_DIG_FSM_FAST_RX_PWRUP	0x302F	W	0x00000000	Status of fast RX power-up
RAWLANE0_DIG_FSM_FAST_RX_VCO_WAIT	0x3030	W	0x00000000	Status of fast RX VCO Wait Times
RAWLANE0_DIG_FSM_FAST_RX_VCO_CAL	0x3031	W	0x00000000	Status of fast RX VCO calibration
RAWLANE0_DIG_FSM_FAST_RX_CONT_CAL_ADAPT	0x3033	W	0x00000000	Status of fast RX Continuous Calibration/Adaptation
RAWLANE0_DIG_FSM_FAST_RX_CONT_ADAPT	0x3034	W	0x00000000	Status of fast RX Continuous adaptation
RAWLANE0_DIG_FSM_FAST_RX_CONT_DATA_CAL	0x3035	W	0x00000000	Status of fast RX Continuous data Calibration
RAWLANE0_DIG_FSM_FAST_RX_CONT_PHASE_CAL	0x3036	W	0x00000000	Status of fast RX Continuous Phase Calibration
RAWLANE0_DIG_FSM_FAST_RX_CONT_AFE_CAL	0x3037	W	0x00000000	Status of fast RX Continuous AFE Calibration
RAWLANE0_DIG_FSM_FAST_RX_ATT_VGA_ADAPT	0x3038	W	0x00000000	Status of fast RX Flags RSVD 0
RAWLANE0_DIG_FSM_FAST_RX_CTLE_ADAPT	0x3039	W	0x00000000	Status of fast RX Flags RSVD 1
RAWLANE0_DIG_FSM_FAST_RX_VGA_ADAPT	0x303A	W	0x00000000	Status of fast RX Flags RSVD 2
RAWLANE0_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT	0x303B	W	0x00000000	Status of fast RX Flags RSVD 3
RAWLANE0_DIG_FSM_FAST_RX_IQ_ADAPT	0x303C	W	0x00000000	Status of fast RX IQ adapt start-up adaptation
RAWLANE0_DIG_FSM_RX_CTLE_ALGO_EH_SEL	0x303D	W	0x00000000	Status of RX CTLE adapt selected algo
RAWLANE0_DIG_FSM_RX_IQ_PHASE_OFFSET	0x303F	W	0x00000000	Offset value for IQ phase calculation
RAWLANE0_DIG_AON_AFE_ATT_IDAC_OFST	0x3040	W	0x00000080	Offset value for RX AFE ATT iDAC

Name	Offset	Size	Reset Value	Description
RAWLANE0_DIG_AON_AFE_CTLE_IDAC_OFST	0x3041	W	0x00000080	Offset value for RX AFE CTLE iDAC
RAWLANE0_DIG_AON_AFE_VGA1_IDAC_OFST	0x3042	W	0x00000080	Offset values for RX AFE VGA1 iDAC
RAWLANE0_DIG_AON_RX_ADAPT_FOM	0x3043	W	0x00000000	Adaptation figure of merit (FOM)
RAWLANE0_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST	0x3044	W	0x00000080	Offset values for RX DFE summer odd iDAC
RAWLANE0_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST	0x3045	W	0x00000080	Offset values for RX DFE phase even vDAC
RAWLANE0_DIG_AON_DFE_PHASE_ODD_VDAC_OFST	0x3046	W	0x00000080	Offset values for RX DFE phase odd vDAC
RAWLANE0_DIG_AON_DFE_EVEN_REF_LVL	0x3047	W	0x00000000	DFE even reference level
RAWLANE0_DIG_AON_DFE_ODD_REF_LVL	0x3048	W	0x00000000	DFE odd reference level
RAWLANE0_DIG_AON_RX_PHSADJ_LIN	0x3049	W	0x00000007	RX phase adjust Linear Value
RAWLANE0_DIG_AON_RX_PHSADJ_MAP	0x304A	W	0x00000000	RX phase adjust Mapped Value
RAWLANE0_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST	0x304B	W	0x00000080	Offset values for RX DFE data even high vDAC
RAWLANE0_DIG_AON_CDR_UNLOCKED_CNT	0x304C	W	0x00000080	Offset values for RX DFE data even low vDAC
RAWLANE0_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST	0x304D	W	0x00000080	Offset values for RX DFE data odd high vDAC
RAWLANE0_DIG_AON_RX_ADAPT_DONE_NEW	0x304E	W	0x00000080	Offset values for RX DFE data odd low vDAC
RAWLANE0_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST	0x304F	W	0x00000080	Offset values for RX DFE bypass even vDAC
RAWLANE0_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST	0x3050	W	0x00000080	Offset values for RX DFE bypass odd vDAC
RAWLANE0_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST	0x3051	W	0x00000080	Offset values for RX DFE error even vDAC
RAWLANE0_DIG_AON_DFE_ERROR_ODD_VDAC_OFST	0x3052	W	0x00000080	Offset values for RX DFE error odd vDAC
RAWLANE0_DIG_AON_RX_IQ_PHASE_ADJUST	0x3053	W	0x00000007	Value for RX IQ phase adjust
RAWLANE0_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET	0x3054	W	0x00000000	Value for RX IQ phase offset + delta value
RAWLANE0_DIG_AON_RX_FW_REVISION_PMA_LABEL	0x3055	W	0x00000000	Stores PMA label from IPXACT label

Name	Offset	Size	Reset Value	Description
RAWLANE0_DIG_AON_INIT_PWRUP_DONE	0x3056	W	0x00000000	Initial power-up Done Status
RAWLANE0_DIG_AON_RX_ADPT_ATT	0x3057	W	0x00000000	RX Adapted value of ATT
RAWLANE0_DIG_AON_RX_ADPT_VGA	0x3058	W	0x00000000	RX Adapted value of VGA
RAWLANE0_DIG_AON_RX_ADPT_CTLE	0x3059	W	0x00000000	RX Adapted value of CTLE
RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP1	0x305A	W	0x00000000	RX Adapted value of DFE TAP1
RAWLANE0_DIG_AON_RX_ADAPT_DONE	0x305B	W	0x00000000	RX adaptation Done Status
RAWLANE0_DIG_AON_FAST_FLAGS	0x305C	W	0x00000000	Fast flags for simulation only
RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP2	0x305D	W	0x00000800	RX Adapted value of DFE TAP2
RAWLANE0_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT	0x305E	W	0x00000000	boost_val_cost_function_lower_limit
RAWLANE0_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT	0x305F	W	0x00000000	boost_val_cost_function_upper_limit
RAWLANE0_DIG_AON_RX_FW_REVISION_RAW_LABEL	0x3060	W	0x00000000	Stores RAW label from IPXACT label
RAWLANE0_DIG_AON_RX_SLICER_CTRL_EVEN	0x3061	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
RAWLANE0_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE	0x3062	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
RAWLANE0_DIG_AON_RX_FW_REVISION_PCS_LABEL	0x3063	W	0x00000000	Stores PCS label from IPXACT label
RAWLANE0_DIG_AON_ADPT_CTL_0	0x3064	W	0x00000000	Adaptation Control register #0
RAWLANE0_DIG_AON_ADPT_CTL_1	0x3065	W	0x00000000	Adaptation Control register #1
RAWLANE0_DIG_AON_ADPT_CTL_2	0x3066	W	0x00000000	Adaptation Control register #2
RAWLANE0_DIG_AON_ADPT_CTL_3	0x3067	W	0x00000000	Adaptation Control register #3
RAWLANE0_DIG_AON_ADPT_CTL_4	0x3068	W	0x00000000	Adaptation Control register #4
RAWLANE0_DIG_AON_ADPT_CTL_5	0x3069	W	0x00000000	Adaptation Control register #5
RAWLANE0_DIG_AON_ADPT_CTL_6	0x306A	W	0x00000000	Adaptation Control register #6
RAWLANE0_DIG_AON_ADPT_CTL_7	0x306B	W	0x00000000	Adaptation Control register #7
RAWLANE0_DIG_AON_RX_FW_REVISION_FW_LABEL	0x306C	W	0x00000000	Stores FW label from IPXACT label
RAWLANE0_DIG_AON_FAST_FLAGS_2	0x306D	W	0x00000000	Fast flags for simulation only

Name	Offset	Size	Reset Value	Description
RAWLANE0_DIG_AON_RX_RESERVED_REG_0	0x306E	W	0x00000000	Reserved Register 0
RAWLANE0_DIG_AON_TX_RX_OVRD_IN	0x306F	W	0x00000000	Override values for incoming AON TX/RX controls from PCS
RAWLANE0_DIG_AON_RX_PHSADJ_LIN_LEFT	0x3070	W	0x00000000	RX phase adjust Linear Value Left side
RAWLANE0_DIG_AON_RX_PHSADJ_LIN_RIGHT	0x3071	W	0x00000000	RX phase adjust Linear Value Right side
RAWLANE0_DIG_AON_RX_PHSADJ_LIN_ADAPT	0x3072	W	0x00000000	RX phase adjust Linear IQ adapt Value
RAWLANE0_DIG_AON_RX_RESERVED_REG_1	0x3073	W	0x00000000	Reserved Register 1
RAWLANE0_DIG_AON_RX_ADPT_VGA_1	0x3078	W	0x00000000	RX Adapted value of VGA 1st iter
RAWLANE0_DIG_AON_RX_ADPT_CTLE_1	0x3079	W	0x00000000	RX Adapted value of CTLE 1st iter
RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP1_1	0x307A	W	0x00000000	RX Adapted value of DFE TAP1 1st iter
RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP2_1	0x307D	W	0x00000800	RX Adapted value of DFE TAP2 1st iter
RAWLANE0_DIG_IRQ_CTL_RESET_RTN_REQ	0x3080	W	0x00000001	Reset routine request
RAWLANE0_DIG_IRQ_CTL_RX_RESET_IRQ	0x3081	W	0x00000000	Rx reset interrupt
RAWLANE0_DIG_IRQ_CTL_RX_REQ_IRQ	0x3082	W	0x00000000	Rx request interrupt
RAWLANE0_DIG_IRQ_CTL_RX_RATE_IRQ	0x3083	W	0x00000000	Rx rate change interrupt request
RAWLANE0_DIG_IRQ_CTL_RX_PSTATE_IRQ	0x3084	W	0x00000000	Rx pstate change interrupt request
RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ	0x3085	W	0x00000000	Rx adaptation request interrupt
RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ	0x3086	W	0x00000000	Rx adaptation disable interrupt
RAWLANE0_DIG_IRQ_CTL_RX_RESET_IRQ_CLR	0x3087	W	0x00000000	RX reset interrupt clear
RAWLANE0_DIG_IRQ_CTL_RX_REQ_IRQ_CLR	0x3088	W	0x00000000	RX request interrupt clear
RAWLANE0_DIG_IRQ_CTL_RX_RATE_IRQ_CLR	0x3089	W	0x00000000	RX rate change interrupt clear
RAWLANE0_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR	0x308A	W	0x00000000	RX pstate change interrupt clear
RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR	0x308B	W	0x00000000	RX adaptation request interrupt clear
RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR	0x308C	W	0x00000000	RX adaptation disable interrupt clear
RAWLANE0_DIG_IRQ_CTL_IRQ_MASK	0x308D	W	0x00000000	Interrupt Mask
RAWLANE0_DIG_IRQ_CTL_RX_INITIALIZE_IRQ	0x308E	W	0x00000000	Rx initialize change interrupt request

Name	Offset	Size	Reset Value	Description
RAWLANE0_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR	0x308F	W	0x00000000	RX initialize change interrupt clear
RAWLANE0_DIG_PMA_XF_RX_OVRD_OUT	0x30A6	W	0x00000000	Override values for outgoing RX controls to PMA
RAWLANE0_DIG_PMA_XF_RX_PMA_IN	0x30A7	W	0x00000000	Current values for coming RX status controls from PMA
RAWLANE0_DIG_RX_CTL_OFFCAN_CONT_STATUS	0x30E3	W	0x00000000	RX continuous offset cancellation status
RAWLANE0_DIG_RX_CTL_ADAPT_CONT_STATUS	0x30E4	W	0x00000000	RX continuous adaptation status
RAWLANE1_DIG_PCS_XF_RX_OVRD_OUT_2	0x3103	W	0x00000000	Override values for outgoing RX controls to PCS register #2
RAWLANE1_DIG_PCS_XF_RX_PCS_IN_5	0x3104	W	0x00000000	Current values for incoming RX controls from PCS, register #5
RAWLANE1_DIG_PCS_XF_RX_OVRD_IN	0x3105	W	0x00000200	Override values for incoming RX controls from PCS
RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_1	0x3106	W	0x00000007	Override values for incoming RX controls from PCS, register #1
RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_2	0x3107	W	0x00000000	Override values for incoming RX controls from PCS, register #2
RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_3	0x3108	W	0x00000000	Override values for incoming RX controls from PCS, register #3
RAWLANE1_DIG_PCS_XF_RX_PCS_IN	0x3109	W	0x00000000	Current values for incoming RX controls from PCS
RAWLANE1_DIG_PCS_XF_RX_PCS_IN_1	0x310A	W	0x00000000	Current values for incoming RX controls from PCS, register #1
RAWLANE1_DIG_PCS_XF_RX_PCS_IN_2	0x310B	W	0x00000000	Current values for incoming RX controls from PCS, register #2
RAWLANE1_DIG_PCS_XF_RX_PCS_IN_3	0x310C	W	0x00000000	Current values for incoming RX controls from PCS, register #3
RAWLANE1_DIG_PCS_XF_RX_PCS_IN_4	0x310D	W	0x00000000	Current values for incoming RX controls from PCS, register #4
RAWLANE1_DIG_PCS_XF_RX_OVRD_OUT	0x310E	W	0x00000003	Override values for outgoing RX controls to PCS
RAWLANE1_DIG_PCS_XF_RX_PCS_OUT	0x310F	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE1_DIG_PCS_XF_RX_ADAPT_ACK	0x3110	W	0x00000000	RX adaptation Acknowledge
RAWLANE1_DIG_PCS_XF_RX_ADAPT_FOM	0x3111	W	0x00000000	RX adaptation figure of merit
RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_4	0x3112	W	0x00000000	Override values for incoming RX controls from PCS, register #4
RAWLANE1_DIG_PCS_XF_RX_PCS_OUT_2	0x3113	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE1_DIG_PCS_XF_LANE_NUMBER	0x3115	W	0x00000000	Current lane number
RAWLANE1_DIG_PCS_XF_ATE_OVRD_IN	0x3118	W	0x00000000	ATE override input to control top-level inputs
RAWLANE1_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN	0x3119	W	0x00000000	Override incoming values for rx_eq_delta_iq
RAWLANE1_DIG_PCS_XF_RX_EQ_OVRD_IN_1	0x311D	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #1

Name	Offset	Size	Reset Value	Description
RAWLANE1_DIG_PCS_XF_RX_EQ_OVRD_IN_2	0x311E	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #2
RAWLANE1_DIG_FSM_FSM_FSM_OVRD_CTL	0x3120	W	0x00000000	FSM override control register
RAWLANE1_DIG_FSM_FSM_MEM_ADDR_MON	0x3121	W	0x00000000	Memory Address Monitor
RAWLANE1_DIG_FSM_FSM_STATUS_MON	0x3122	W	0x00000000	FSM Status Monitor
RAWLANE1_DIG_FSM_FSM_CR_REG_OP_XTND_EN	0x3123	W	0x00000000	CR interface timing extension enable
RAWLANE1_DIG_FSM_FAST_RX_STARTUP_CAL	0x3124	W	0x00000000	Status of fast RX Start Up Calibration
RAWLANE1_DIG_FSM_FAST_RX_ADAPT	0x3125	W	0x00000000	Status of fast RX adaptation
RAWLANE1_DIG_FSM_FAST_RX_AFE_CAL	0x3126	W	0x00000000	Status of fast RX AFE Calibration
RAWLANE1_DIG_FSM_FAST_RX_DFE_CAL	0x3127	W	0x00000000	Status of fast RX DFE Calibration
RAWLANE1_DIG_FSM_FAST_RX_BYPASS_CAL	0x3128	W	0x00000000	Status of fast RX bypass Calibration
RAWLANE1_DIG_FSM_FAST_RX_REFLVL_CAL	0x3129	W	0x00000000	Status of fast RX Reference level Calibration
RAWLANE1_DIG_FSM_FAST_RX_IQ_CAL	0x312A	W	0x00000000	Status of fast RX IQ Calibration
RAWLANE1_DIG_FSM_FAST_RX_AFE_ADAPT	0x312B	W	0x00000000	Status of fast RX AFE adaptation
RAWLANE1_DIG_FSM_FAST_RX_DFE_ADAPT	0x312C	W	0x00000000	Status of fast RX DFE adaptation
RAWLANE1_DIG_FSM_FAST_SUP	0x312D	W	0x00000000	Status of fast support block
RAWLANE1_DIG_FSM_FAST_RX_IQ_WALK	0x312E	W	0x00000000	Status of fast RX IQ walk start-up adaptation
RAWLANE1_DIG_FSM_FAST_RX_PWRUP	0x312F	W	0x00000000	Status of fast RX power-up
RAWLANE1_DIG_FSM_FAST_RX_VCO_WAIT	0x3130	W	0x00000000	Status of fast RX VCO Wait Times
RAWLANE1_DIG_FSM_FAST_RX_VCO_CAL	0x3131	W	0x00000000	Status of fast RX VCO calibration
RAWLANE1_DIG_FSM_FAST_RX_CONT_CAL_ADAPT	0x3133	W	0x00000000	Status of fast RX Continuous Calibration/Adaptation
RAWLANE1_DIG_FSM_FAST_RX_CONT_ADAPT	0x3134	W	0x00000000	Status of fast RX Continuous adaptation
RAWLANE1_DIG_FSM_FAST_RX_CONT_DATA_CAL	0x3135	W	0x00000000	Status of fast RX Continuous data Calibration
RAWLANE1_DIG_FSM_FAST_RX_CONT_PHASE_CAL	0x3136	W	0x00000000	Status of fast RX Continuous Phase Calibration
RAWLANE1_DIG_FSM_FAST_RX_CONT_AFE_CAL	0x3137	W	0x00000000	Status of fast RX Continuous AFE Calibration
RAWLANE1_DIG_FSM_FAST_RX_ATT_VGA_ADAPT	0x3138	W	0x00000000	Status of fast RX Flags RSVD 0
RAWLANE1_DIG_FSM_FAST_RX_CTLE_ADAPT	0x3139	W	0x00000000	Status of fast RX Flags RSVD 1

Name	Offset	Size	Reset Value	Description
RAWLANE1_DIG_FSM_FAST_RX_VGA_ADAPT	0x313A	W	0x00000000	Status of fast RX Flags RSVD 2
RAWLANE1_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT	0x313B	W	0x00000000	Status of fast RX Flags RSVD 3
RAWLANE1_DIG_FSM_FAST_RX_IQ_ADAPT	0x313C	W	0x00000000	Status of fast RX IQ adapt start-up adaptation
RAWLANE1_DIG_FSM_RX_CTLE_ALGO_EH_SEL	0x313D	W	0x00000000	Status of RX CTLE adapt selected algo
RAWLANE1_DIG_FSM_RX_IQ_PHASE_OFFSET	0x313F	W	0x00000000	Offset value for IQ phase calculation
RAWLANE1_DIG_AON_AFE_ATT_IDAC_OFST	0x3140	W	0x00000080	Offset value for RX AFE ATT iDAC
RAWLANE1_DIG_AON_AFE_CTLE_IDAC_OFST	0x3141	W	0x00000080	Offset value for RX AFE CTLE iDAC
RAWLANE1_DIG_AON_AFE_VGA1_IDAC_OFST	0x3142	W	0x00000080	Offset values for RX AFE VGA1 iDAC
RAWLANE1_DIG_AON_RX_ADAPT_FOM	0x3143	W	0x00000000	Adaptation figure of merit (FOM)
RAWLANE1_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST	0x3144	W	0x00000080	Offset values for RX DFE summer odd iDAC
RAWLANE1_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST	0x3145	W	0x00000080	Offset values for RX DFE phase even vDAC
RAWLANE1_DIG_AON_DFE_PHASE_ODD_VDAC_OFST	0x3146	W	0x00000080	Offset values for RX DFE phase odd vDAC
RAWLANE1_DIG_AON_DFE_EVEN_REF_LVL	0x3147	W	0x00000000	DFE even reference level
RAWLANE1_DIG_AON_DFE_ODD_REF_LVL	0x3148	W	0x00000000	DFE odd reference level
RAWLANE1_DIG_AON_RX_PHSADJ_LIN	0x3149	W	0x00000007	RX phase adjust Linear Value
RAWLANE1_DIG_AON_RX_PHSADJ_MAP	0x314A	W	0x00000000	RX phase adjust Mapped Value
RAWLANE1_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST	0x314B	W	0x00000080	Offset values for RX DFE data even high vDAC
RAWLANE1_DIG_AON_CDR_UNLOCKED_CNT	0x314C	W	0x00000080	Offset values for RX DFE data even low vDAC
RAWLANE1_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST	0x314D	W	0x00000080	Offset values for RX DFE data odd high vDAC
RAWLANE1_DIG_AON_RX_ADAPT_DONE_NEW	0x314E	W	0x00000080	Offset values for RX DFE data odd low vDAC
RAWLANE1_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST	0x314F	W	0x00000080	Offset values for RX DFE bypass even vDAC
RAWLANE1_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST	0x3150	W	0x00000080	Offset values for RX DFE bypass odd vDAC
RAWLANE1_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST	0x3151	W	0x00000080	Offset values for RX DFE error even vDAC

Name	Offset	Size	Reset Value	Description
RAWLANE1_DIG_AON_DFE_ERROR_ODD_VDAC_OFST	0x3152	W	0x00000080	Offset values for RX DFE error odd vDAC
RAWLANE1_DIG_AON_RX_IQ_PHASE_ADJUST	0x3153	W	0x00000007	Value for RX IQ phase adjust
RAWLANE1_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET	0x3154	W	0x00000000	Value for RX IQ phase offset + delta value
RAWLANE1_DIG_AON_RX_FW_REVISION_PMA_LABEL	0x3155	W	0x00000000	Stores PMA label from IPXACT label
RAWLANE1_DIG_AON_INIT_PWRUP_DONE	0x3156	W	0x00000000	Initial power-up Done Status
RAWLANE1_DIG_AON_RX_ADPT_ATT	0x3157	W	0x00000000	RX Adapted value of ATT
RAWLANE1_DIG_AON_RX_ADPT_VGA	0x3158	W	0x00000000	RX Adapted value of VGA
RAWLANE1_DIG_AON_RX_ADPT_CTLE	0x3159	W	0x00000000	RX Adapted value of CTLE
RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP1	0x315A	W	0x00000000	RX Adapted value of DFE TAP1
RAWLANE1_DIG_AON_RX_ADAPT_DONE	0x315B	W	0x00000000	RX adaptation Done Status
RAWLANE1_DIG_AON_FAST_FLAGS	0x315C	W	0x00000000	Fast flags for simulation only
RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP2	0x315D	W	0x00000800	RX Adapted value of DFE TAP2
RAWLANE1_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT	0x315E	W	0x00000000	boost_val_cost_function_lower_limit
RAWLANE1_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT	0x315F	W	0x00000000	boost_val_cost_function_upper_limit
RAWLANE1_DIG_AON_RX_FW_REVISION_RAW_LABEL	0x3160	W	0x00000000	Stores RAW label from IPXACT label
RAWLANE1_DIG_AON_RX_SLICER_CTRL_EVEN	0x3161	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
RAWLANE1_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE	0x3162	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
RAWLANE1_DIG_AON_RX_FW_REVISION_PCS_LABEL	0x3163	W	0x00000000	Stores PCS label from IPXACT label
RAWLANE1_DIG_AON_ADPT_CTL_0	0x3164	W	0x00000000	Adaptation Control register #0
RAWLANE1_DIG_AON_ADPT_CTL_1	0x3165	W	0x00000000	Adaptation Control register #1
RAWLANE1_DIG_AON_ADPT_CTL_2	0x3166	W	0x00000000	Adaptation Control register #2
RAWLANE1_DIG_AON_ADPT_CTL_3	0x3167	W	0x00000000	Adaptation Control register #3
RAWLANE1_DIG_AON_ADPT_CTL_4	0x3168	W	0x00000000	Adaptation Control register #4

Name	Offset	Size	Reset Value	Description
RAWLANE1_DIG_AON_ADPT_CTL_5	0x3169	W	0x00000000	Adaptation Control register #5
RAWLANE1_DIG_AON_ADPT_CTL_6	0x316A	W	0x00000000	Adaptation Control register #6
RAWLANE1_DIG_AON_ADPT_CTL_7	0x316B	W	0x00000000	Adaptation Control register #7
RAWLANE1_DIG_AON_RX_FW_REVISION_FW_LABEL	0x316C	W	0x00000000	Stores FW label from IPXACT label
RAWLANE1_DIG_AON_FAST_FLAGS_2	0x316D	W	0x00000000	Fast flags for simulation only
RAWLANE1_DIG_AON_RX_RESERVED_REG_0	0x316E	W	0x00000000	Reserved Register 0
RAWLANE1_DIG_AON_TXRX_OVRD_IN	0x316F	W	0x00000000	Override values for incoming AON TX/RX controls from PCS
RAWLANE1_DIG_AON_RX_PHSADJ_LIN_LEFT	0x3170	W	0x00000000	RX phase adjust Linear Value Left side
RAWLANE1_DIG_AON_RX_PHSADJ_LIN_RIGHT	0x3171	W	0x00000000	RX phase adjust Linear Value Right side
RAWLANE1_DIG_AON_RX_PHSADJ_LIN_ADAPT	0x3172	W	0x00000000	RX phase adjust Linear IQ adapt Value
RAWLANE1_DIG_AON_RX_RESERVED_REG_1	0x3173	W	0x00000000	Reserved Register 1
RAWLANE1_DIG_AON_RX_ADPT_VGA_1	0x3178	W	0x00000000	RX Adapted value of VGA 1st iter
RAWLANE1_DIG_AON_RX_ADPT_CTLE_1	0x3179	W	0x00000000	RX Adapted value of CTLE 1st iter
RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP1_1	0x317A	W	0x00000000	RX Adapted value of DFE TAP1 1st iter
RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP2_1	0x317D	W	0x00000800	RX Adapted value of DFE TAP2 1st iter
RAWLANE1_DIG_IRQ_CTL_RESET_RTN_REQ	0x3180	W	0x00000001	Reset routine request
RAWLANE1_DIG_IRQ_CTL_RX_RESET_IRQ	0x3181	W	0x00000000	Rx reset interrupt
RAWLANE1_DIG_IRQ_CTL_RX_REQ_IRQ	0x3182	W	0x00000000	Rx request interrupt
RAWLANE1_DIG_IRQ_CTL_RX_RATE_IRQ	0x3183	W	0x00000000	Rx rate change interrupt request
RAWLANE1_DIG_IRQ_CTL_RX_PSTATE_IRQ	0x3184	W	0x00000000	Rx pstate change interrupt request
RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ	0x3185	W	0x00000000	Rx adaptation request interrupt
RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ	0x3186	W	0x00000000	Rx adaptation disable interrupt
RAWLANE1_DIG_IRQ_CTL_RX_RESET_IRQ_CLR	0x3187	W	0x00000000	RX reset interrupt clear
RAWLANE1_DIG_IRQ_CTL_RX_REQ_IRQ_CLR	0x3188	W	0x00000000	RX request interrupt clear
RAWLANE1_DIG_IRQ_CTL_RX_RATE_IRQ_CLR	0x3189	W	0x00000000	RX rate change interrupt clear
RAWLANE1_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR	0x318A	W	0x00000000	RX pstate change interrupt clear

Name	Offset	Size	Reset Value	Description
RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR	0x318B	W	0x00000000	RX adaptation request interrupt clear
RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR	0x318C	W	0x00000000	RX adaptation disable interrupt clear
RAWLANE1_DIG_IRQ_CTL_IRQ_MASK	0x318D	W	0x00000000	Interrupt Mask
RAWLANE1_DIG_IRQ_CTL_RX_INITIALIZE_IRQ	0x318E	W	0x00000000	Rx initialize change interrupt request
RAWLANE1_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR	0x318F	W	0x00000000	RX initialize change interrupt clear
RAWLANE1_DIG_PMA_XF_RX_OVRD_OUT	0x31A6	W	0x00000000	Override values for outgoing RX controls to PMA
RAWLANE1_DIG_PMA_XF_RX_PMA_IN	0x31A7	W	0x00000000	Current values for coming RX status controls from PMA
RAWLANE1_DIG_RX_CTL_OFFCAN_CONT_STATUS	0x31E3	W	0x00000000	RX continuous offset cancellation status
RAWLANE1_DIG_RX_CTL_ADAPT_CONT_STATUS	0x31E4	W	0x00000000	RX continuous adaptation status
RAWLANE2_DIG_PCS_XF_RX_OVRD_OUT_2	0x3203	W	0x00000000	Override values for outgoing RX controls to PCS register #2
RAWLANE2_DIG_PCS_XF_RX_PCS_IN_5	0x3204	W	0x00000000	Current values for incoming RX controls from PCS, register #5
RAWLANE2_DIG_PCS_XF_RX_OVRD_IN	0x3205	W	0x00000200	Override values for incoming RX controls from PCS
RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_1	0x3206	W	0x00000007	Override values for incoming RX controls from PCS, register #1
RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_2	0x3207	W	0x00000000	Override values for incoming RX controls from PCS, register #2
RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_3	0x3208	W	0x00000000	Override values for incoming RX controls from PCS, register #3
RAWLANE2_DIG_PCS_XF_RX_PCS_IN	0x3209	W	0x00000000	Current values for incoming RX controls from PCS
RAWLANE2_DIG_PCS_XF_RX_PCS_IN_1	0x320A	W	0x00000000	Current values for incoming RX controls from PCS, register #1
RAWLANE2_DIG_PCS_XF_RX_PCS_IN_2	0x320B	W	0x00000000	Current values for incoming RX controls from PCS, register #2
RAWLANE2_DIG_PCS_XF_RX_PCS_IN_3	0x320C	W	0x00000000	Current values for incoming RX controls from PCS, register #3
RAWLANE2_DIG_PCS_XF_RX_PCS_IN_4	0x320D	W	0x00000000	Current values for incoming RX controls from PCS, register #4
RAWLANE2_DIG_PCS_XF_RX_OVRD_OUT	0x320E	W	0x00000003	Override values for outgoing RX controls to PCS
RAWLANE2_DIG_PCS_XF_RX_PCS_OUT	0x320F	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE2_DIG_PCS_XF_RX_ADAPT_ACK	0x3210	W	0x00000000	RX adaptation Acknowledge
RAWLANE2_DIG_PCS_XF_RX_ADAPT_FOM	0x3211	W	0x00000000	RX adaptation figure of merit
RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_4	0x3212	W	0x00000000	Override values for incoming RX controls from PCS, register #4

Name	Offset	Size	Reset Value	Description
RAWLANE2_DIG_PCS_XF_RX_PCS_OUT_2	0x3213	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE2_DIG_PCS_XF_LANE_NUMBER	0x3215	W	0x00000000	Current lane number
RAWLANE2_DIG_PCS_XF_ATE_OVRD_IN	0x3218	W	0x00000000	ATE override input to control top-level inputs
RAWLANE2_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN	0x3219	W	0x00000000	Override incoming values for rx_eq_delta_iq
RAWLANE2_DIG_PCS_XF_RX_EQ_OVRD_IN_1	0x321D	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #1
RAWLANE2_DIG_PCS_XF_RX_EQ_OVRD_IN_2	0x321E	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #2
RAWLANE2_DIG_FSM_FSM_FSM_OVRD_CTL	0x3220	W	0x00000000	FSM override control register
RAWLANE2_DIG_FSM_FSM_MEM_ADDR_MON	0x3221	W	0x00000000	Memory Address Monitor
RAWLANE2_DIG_FSM_FSM_STATUS_MON	0x3222	W	0x00000000	FSM Status Monitor
RAWLANE2_DIG_FSM_FSM_CR_REG_OP_XTND_EN	0x3223	W	0x00000000	CR interface timing extension enable
RAWLANE2_DIG_FSM_FAST_RX_STARTUP_CAL	0x3224	W	0x00000000	Status of fast RX Start Up Calibration
RAWLANE2_DIG_FSM_FAST_RX_ADAPT	0x3225	W	0x00000000	Status of fast RX adaptation
RAWLANE2_DIG_FSM_FAST_RX_AFE_CAL	0x3226	W	0x00000000	Status of fast RX AFE Calibration
RAWLANE2_DIG_FSM_FAST_RX_DFE_CAL	0x3227	W	0x00000000	Status of fast RX DFE Calibration
RAWLANE2_DIG_FSM_FAST_RX_BYPASS_CAL	0x3228	W	0x00000000	Status of fast RX bypass Calibration
RAWLANE2_DIG_FSM_FAST_RX_REFLVL_CAL	0x3229	W	0x00000000	Status of fast RX Reference level Calibration
RAWLANE2_DIG_FSM_FAST_RX_IQ_CAL	0x322A	W	0x00000000	Status of fast RX IQ Calibration
RAWLANE2_DIG_FSM_FAST_RX_AFE_ADAPT	0x322B	W	0x00000000	Status of fast RX AFE adaptation
RAWLANE2_DIG_FSM_FAST_RX_DFE_ADAPT	0x322C	W	0x00000000	Status of fast RX DFE adaptation
RAWLANE2_DIG_FSM_FAST_SUP	0x322D	W	0x00000000	Status of fast support block
RAWLANE2_DIG_FSM_FAST_RX_IQ_WALK	0x322E	W	0x00000000	Status of fast RX IQ walk start-up adaptation
RAWLANE2_DIG_FSM_FAST_RX_PWRUP	0x322F	W	0x00000000	Status of fast RX power-up
RAWLANE2_DIG_FSM_FAST_RX_VCO_WAIT	0x3230	W	0x00000000	Status of fast RX VCO Wait Times
RAWLANE2_DIG_FSM_FAST_RX_VCO_CAL	0x3231	W	0x00000000	Status of fast RX VCO calibration
RAWLANE2_DIG_FSM_FAST_RX_CONT_CAL_ADAPT	0x3233	W	0x00000000	Status of fast RX Continuous Calibration/Adaptation
RAWLANE2_DIG_FSM_FAST_RX_CONT_ADAPT	0x3234	W	0x00000000	Status of fast RX Continuous adaptation

Name	Offset	Size	Reset Value	Description
RAWLANE2_DIG_FSM_FAST_RX_CONT_DATA_CAL	0x3235	W	0x00000000	Status of fast RX Continuous data Calibration
RAWLANE2_DIG_FSM_FAST_RX_CONT_PHASE_CAL	0x3236	W	0x00000000	Status of fast RX Continuous Phase Calibration
RAWLANE2_DIG_FSM_FAST_RX_CONT_AFE_CAL	0x3237	W	0x00000000	Status of fast RX Continuous AFE Calibration
RAWLANE2_DIG_FSM_FAST_RX_ATT_VGA_ADAPT	0x3238	W	0x00000000	Status of fast RX Flags RSVD 0
RAWLANE2_DIG_FSM_FAST_RX_CTLE_ADAPT	0x3239	W	0x00000000	Status of fast RX Flags RSVD 1
RAWLANE2_DIG_FSM_FAST_RX_VGA_ADAPT	0x323A	W	0x00000000	Status of fast RX Flags RSVD 2
RAWLANE2_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT	0x323B	W	0x00000000	Status of fast RX Flags RSVD 3
RAWLANE2_DIG_FSM_FAST_RX_IQ_ADAPT	0x323C	W	0x00000000	Status of fast RX IQ adapt start-up adaptation
RAWLANE2_DIG_FSM_RX_CTLE_ALGO_EH_SEL	0x323D	W	0x00000000	Status of RX CTLE adapt selected algo
RAWLANE2_DIG_FSM_RX_IQ_PHASE_OFFSET	0x323F	W	0x00000000	Offset value for IQ phase calculation
RAWLANE2_DIG_AON_AFE_ATT_IDAC_OFST	0x3240	W	0x00000080	Offset value for RX AFE ATT iDAC
RAWLANE2_DIG_AON_AFE_CTLE_IDAC_OFST	0x3241	W	0x00000080	Offset value for RX AFE CTLE iDAC
RAWLANE2_DIG_AON_AFE_VGA1_IDAC_OFST	0x3242	W	0x00000080	Offset values for RX AFE VGA1 iDAC
RAWLANE2_DIG_AON_RX_ADAPT_FOM	0x3243	W	0x00000000	Adaptation figure of merit (FOM)
RAWLANE2_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST	0x3244	W	0x00000080	Offset values for RX DFE summer odd iDAC
RAWLANE2_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST	0x3245	W	0x00000080	Offset values for RX DFE phase even vDAC
RAWLANE2_DIG_AON_DFE_PHASE_ODD_VDAC_OFST	0x3246	W	0x00000080	Offset values for RX DFE phase odd vDAC
RAWLANE2_DIG_AON_DFE_EVEN_REF_LVL	0x3247	W	0x00000000	DFE even reference level
RAWLANE2_DIG_AON_DFE_ODD_REF_LVL	0x3248	W	0x00000000	DFE odd reference level
RAWLANE2_DIG_AON_RX_PHSADJ_LIN	0x3249	W	0x00000007	RX phase adjust Linear Value
RAWLANE2_DIG_AON_RX_PHSADJ_MAP	0x324A	W	0x00000000	RX phase adjust Mapped Value
RAWLANE2_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST	0x324B	W	0x00000080	Offset values for RX DFE data even high vDAC
RAWLANE2_DIG_AON_CDR_UNLOCKED_CNT	0x324C	W	0x00000080	Offset values for RX DFE data even low vDAC
RAWLANE2_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST	0x324D	W	0x00000080	Offset values for RX DFE data odd high vDAC

Name	Offset	Size	Reset Value	Description
RAWLANE2_DIG_AON_RX_ADAPT_DONE_NEW	0x324E	W	0x00000080	Offset values for RX DFE data odd low vDAC
RAWLANE2_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST	0x324F	W	0x00000080	Offset values for RX DFE bypass even vDAC
RAWLANE2_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST	0x3250	W	0x00000080	Offset values for RX DFE bypass odd vDAC
RAWLANE2_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST	0x3251	W	0x00000080	Offset values for RX DFE error even vDAC
RAWLANE2_DIG_AON_DFE_ERROR_ODD_VDAC_OFST	0x3252	W	0x00000080	Offset values for RX DFE error odd vDAC
RAWLANE2_DIG_AON_RX_IQ_PHASE_ADJUST	0x3253	W	0x00000007	Value for RX IQ phase adjust
RAWLANE2_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET	0x3254	W	0x00000000	Value for RX IQ phase offset + delta value
RAWLANE2_DIG_AON_RX_FW_REVISION_PMA_LABEL	0x3255	W	0x00000000	Stores PMA label from IPXACT label
RAWLANE2_DIG_AON_INIT_PWRUP_DONE	0x3256	W	0x00000000	Initial power-up Done Status
RAWLANE2_DIG_AON_RX_ADPT_ATT	0x3257	W	0x00000000	RX Adapted value of ATT
RAWLANE2_DIG_AON_RX_ADPT_VGA	0x3258	W	0x00000000	RX Adapted value of VGA
RAWLANE2_DIG_AON_RX_ADPT_CTLE	0x3259	W	0x00000000	RX Adapted value of CTLE
RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP1	0x325A	W	0x00000000	RX Adapted value of DFE TAP1
RAWLANE2_DIG_AON_RX_ADAPT_DONE	0x325B	W	0x00000000	RX adaptation Done Status
RAWLANE2_DIG_AON_FAST_FLAGS	0x325C	W	0x00000000	Fast flags for simulation only
RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP2	0x325D	W	0x00000800	RX Adapted value of DFE TAP2
RAWLANE2_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT	0x325E	W	0x00000000	boost_val_cost_function_lower_limit
RAWLANE2_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT	0x325F	W	0x00000000	boost_val_cost_function_upper_limit
RAWLANE2_DIG_AON_RX_FW_REVISION_RAW_LABEL	0x3260	W	0x00000000	Stores RAW label from IPXACT label
RAWLANE2_DIG_AON_RX_SLICER_CTRL_EVEN	0x3261	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
RAWLANE2_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE	0x3262	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA

Name	Offset	Size	Reset Value	Description
RAWLANE2_DIG_AON_RX_FW_REVISION_PCS_LABEL	0x3263	W	0x00000000	Stores PCS label from IPXACT label
RAWLANE2_DIG_AON_ADPT_CTL_0	0x3264	W	0x00000000	Adaptation Control register #0
RAWLANE2_DIG_AON_ADPT_CTL_1	0x3265	W	0x00000000	Adaptation Control register #1
RAWLANE2_DIG_AON_ADPT_CTL_2	0x3266	W	0x00000000	Adaptation Control register #2
RAWLANE2_DIG_AON_ADPT_CTL_3	0x3267	W	0x00000000	Adaptation Control register #3
RAWLANE2_DIG_AON_ADPT_CTL_4	0x3268	W	0x00000000	Adaptation Control register #4
RAWLANE2_DIG_AON_ADPT_CTL_5	0x3269	W	0x00000000	Adaptation Control register #5
RAWLANE2_DIG_AON_ADPT_CTL_6	0x326A	W	0x00000000	Adaptation Control register #6
RAWLANE2_DIG_AON_ADPT_CTL_7	0x326B	W	0x00000000	Adaptation Control register #7
RAWLANE2_DIG_AON_RX_FW_REVISION_FW_LABEL	0x326C	W	0x00000000	Stores FW label from IPXACT label
RAWLANE2_DIG_AON_FAST_FLAGS_2	0x326D	W	0x00000000	Fast flags for simulation only
RAWLANE2_DIG_AON_RX_RESERVED_REG_0	0x326E	W	0x00000000	Reserved Register 0
RAWLANE2_DIG_AON_TXRX_OVRD_IN	0x326F	W	0x00000000	Override values for incoming AON TX/RX controls from PCS
RAWLANE2_DIG_AON_RX_PHSADJ_LIN_LEFT	0x3270	W	0x00000000	RX phase adjust Linear Value Left side
RAWLANE2_DIG_AON_RX_PHSADJ_LIN_RIGHT	0x3271	W	0x00000000	RX phase adjust Linear Value Right side
RAWLANE2_DIG_AON_RX_PHSADJ_LIN_ADAPT	0x3272	W	0x00000000	RX phase adjust Linear IQ adapt Value
RAWLANE2_DIG_AON_RX_RESERVED_REG_1	0x3273	W	0x00000000	Reserved Register 1
RAWLANE2_DIG_AON_RX_ADPT_VGA_1	0x3278	W	0x00000000	RX Adapted value of VGA 1st iter
RAWLANE2_DIG_AON_RX_ADPT_CTLE_1	0x3279	W	0x00000000	RX Adapted value of CTLE 1st iter
RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP1_1	0x327A	W	0x00000000	RX Adapted value of DFE TAP1 1st iter
RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP2_1	0x327D	W	0x00000800	RX Adapted value of DFE TAP2 1st iter
RAWLANE2_DIG_IRQ_CTL_RESET_RTN_REQ	0x3280	W	0x00000001	Reset routine request
RAWLANE2_DIG_IRQ_CTL_RX_RESET_IRQ	0x3281	W	0x00000000	Rx reset interrupt
RAWLANE2_DIG_IRQ_CTL_RX_REQ_IRQ	0x3282	W	0x00000000	Rx request interrupt
RAWLANE2_DIG_IRQ_CTL_RX_RATE_IRQ	0x3283	W	0x00000000	Rx rate change interrupt request

Name	Offset	Size	Reset Value	Description
RAWLANE2_DIG_IRQ_CTL_RX_PSTATE_IRQ	0x3284	W	0x00000000	Rx pstate change interrupt request
RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ	0x3285	W	0x00000000	Rx adaptation request interrupt
RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ	0x3286	W	0x00000000	Rx adaptation disable interrupt
RAWLANE2_DIG_IRQ_CTL_RX_RESET_IRQ_CLR	0x3287	W	0x00000000	RX reset interrupt clear
RAWLANE2_DIG_IRQ_CTL_RX_REQ_IRQ_CLR	0x3288	W	0x00000000	RX request interrupt clear
RAWLANE2_DIG_IRQ_CTL_RX_RATE_IRQ_CLR	0x3289	W	0x00000000	RX rate change interrupt clear
RAWLANE2_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR	0x328A	W	0x00000000	RX pstate change interrupt clear
RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR	0x328B	W	0x00000000	RX adaptation request interrupt clear
RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR	0x328C	W	0x00000000	RX adaptation disable interrupt clear
RAWLANE2_DIG_IRQ_CTL_IRQ_MASK	0x328D	W	0x00000000	Interrupt Mask
RAWLANE2_DIG_IRQ_CTL_RX_INITIALIZE_IRQ	0x328E	W	0x00000000	Rx initialize change interrupt request
RAWLANE2_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR	0x328F	W	0x00000000	RX initialize change interrupt clear
RAWLANE2_DIG_PMA_XF_RX_OVRD_OUT	0x32A6	W	0x00000000	Override values for outgoing RX controls to PMA
RAWLANE2_DIG_PMA_XF_RX_PMA_IN	0x32A7	W	0x00000000	Current values for coming RX status controls from PMA
RAWLANE2_DIG_RX_CTL_OFFCAN_CONT_STATUS	0x32E3	W	0x00000000	RX continuous offset cancellation status
RAWLANE2_DIG_RX_CTL_ADAPT_CONT_STATUS	0x32E4	W	0x00000000	RX continuous adaptation status
RAWLANE3_DIG_PCS_XF_RX_OVRD_OUT_2	0x3303	W	0x00000000	Override values for outgoing RX controls to PCS register #2
RAWLANE3_DIG_PCS_XF_RX_PCS_IN_5	0x3304	W	0x00000000	Current values for incoming RX controls from PCS, register #5
RAWLANE3_DIG_PCS_XF_RX_OVRD_IN	0x3305	W	0x00000200	Override values for incoming RX controls from PCS
RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_1	0x3306	W	0x00000007	Override values for incoming RX controls from PCS, register #1
RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_2	0x3307	W	0x00000000	Override values for incoming RX controls from PCS, register #2
RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_3	0x3308	W	0x00000000	Override values for incoming RX controls from PCS, register #3
RAWLANE3_DIG_PCS_XF_RX_PCS_IN	0x3309	W	0x00000000	Current values for incoming RX controls from PCS
RAWLANE3_DIG_PCS_XF_RX_PCS_IN_1	0x330A	W	0x00000000	Current values for incoming RX controls from PCS, register #1
RAWLANE3_DIG_PCS_XF_RX_PCS_IN_2	0x330B	W	0x00000000	Current values for incoming RX controls from PCS, register #2

Name	Offset	Size	Reset Value	Description
RAWLANE3_DIG_PCS_XF_RX_PCS_IN_3	0x330C	W	0x00000000	Current values for incoming RX controls from PCS, register #3
RAWLANE3_DIG_PCS_XF_RX_PCS_IN_4	0x330D	W	0x00000000	Current values for incoming RX controls from PCS, register #4
RAWLANE3_DIG_PCS_XF_RX_OVRD_OUT	0x330E	W	0x00000003	Override values for outgoing RX controls to PCS
RAWLANE3_DIG_PCS_XF_RX_PCS_OUT	0x330F	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE3_DIG_PCS_XF_RX_ADAPT_ACK	0x3310	W	0x00000000	RX adaptation Acknowledge
RAWLANE3_DIG_PCS_XF_RX_ADAPT_FOM	0x3311	W	0x00000000	RX adaptation figure of merit
RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_4	0x3312	W	0x00000000	Override values for incoming RX controls from PCS, register #4
RAWLANE3_DIG_PCS_XF_RX_PCS_OUT_2	0x3313	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANE3_DIG_PCS_XF_LANE_NUMBER	0x3315	W	0x00000000	Current lane number
RAWLANE3_DIG_PCS_XF_ATE_OVRD_IN	0x3318	W	0x00000000	ATE override input to control top-level inputs
RAWLANE3_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN	0x3319	W	0x00000000	Override incoming values for rx_eq_delta_iq
RAWLANE3_DIG_PCS_XF_RX_EQ_OVRD_IN_1	0x331D	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #1
RAWLANE3_DIG_PCS_XF_RX_EQ_OVRD_IN_2	0x331E	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #2
RAWLANE3_DIG_FSM_FSM_FSM_OVRD_CTL	0x3320	W	0x00000000	FSM override control register
RAWLANE3_DIG_FSM_FSM_MEM_ADDR_MON	0x3321	W	0x00000000	Memory Address Monitor
RAWLANE3_DIG_FSM_FSM_STATUS_MON	0x3322	W	0x00000000	FSM Status Monitor
RAWLANE3_DIG_FSM_FSM_CR_REG_OP_XTND_EN	0x3323	W	0x00000000	CR interface timing extension enable
RAWLANE3_DIG_FSM_FAST_RX_STARTUP_CAL	0x3324	W	0x00000000	Status of fast RX Start Up Calibration
RAWLANE3_DIG_FSM_FAST_RX_ADAPT	0x3325	W	0x00000000	Status of fast RX adaptation
RAWLANE3_DIG_FSM_FAST_RX_AFE_CAL	0x3326	W	0x00000000	Status of fast RX AFE Calibration
RAWLANE3_DIG_FSM_FAST_RX_DFE_CAL	0x3327	W	0x00000000	Status of fast RX DFE Calibration
RAWLANE3_DIG_FSM_FAST_RX_BYPASS_CAL	0x3328	W	0x00000000	Status of fast RX bypass Calibration
RAWLANE3_DIG_FSM_FAST_RX_REFLVL_CAL	0x3329	W	0x00000000	Status of fast RX Reference level Calibration
RAWLANE3_DIG_FSM_FAST_RX_IQ_CAL	0x332A	W	0x00000000	Status of fast RX IQ Calibration
RAWLANE3_DIG_FSM_FAST_RX_AFE_ADAPT	0x332B	W	0x00000000	Status of fast RX AFE adaptation
RAWLANE3_DIG_FSM_FAST_RX_DFE_ADAPT	0x332C	W	0x00000000	Status of fast RX DFE adaptation

Name	Offset	Size	Reset Value	Description
RAWLANE3_DIG_FSM_FAST_SUP	0x332D	W	0x00000000	Status of fast support block
RAWLANE3_DIG_FSM_FAST_RX_IQ_WALK	0x332E	W	0x00000000	Status of fast RX IQ walk start-up adaptation
RAWLANE3_DIG_FSM_FAST_RX_PWRUP	0x332F	W	0x00000000	Status of fast RX power-up
RAWLANE3_DIG_FSM_FAST_RX_VCO_WAIT	0x3330	W	0x00000000	Status of fast RX VCO Wait Times
RAWLANE3_DIG_FSM_FAST_RX_VCO_CAL	0x3331	W	0x00000000	Status of fast RX VCO calibration
RAWLANE3_DIG_FSM_FAST_RX_CONT_CAL_ADAPT	0x3333	W	0x00000000	Status of fast RX Continuous Calibration/Adaptation
RAWLANE3_DIG_FSM_FAST_RX_CONT_ADAPT	0x3334	W	0x00000000	Status of fast RX Continuous adaptation
RAWLANE3_DIG_FSM_FAST_RX_CONT_DATA_CAL	0x3335	W	0x00000000	Status of fast RX Continuous data Calibration
RAWLANE3_DIG_FSM_FAST_RX_CONT_PHASE_CAL	0x3336	W	0x00000000	Status of fast RX Continuous Phase Calibration
RAWLANE3_DIG_FSM_FAST_RX_CONT_AFE_CAL	0x3337	W	0x00000000	Status of fast RX Continuous AFE Calibration
RAWLANE3_DIG_FSM_FAST_RX_ATT_VGA_ADAPT	0x3338	W	0x00000000	Status of fast RX Flags RSVD 0
RAWLANE3_DIG_FSM_FAST_RX_CTLE_ADAPT	0x3339	W	0x00000000	Status of fast RX Flags RSVD 1
RAWLANE3_DIG_FSM_FAST_RX_VGA_ADAPT	0x333A	W	0x00000000	Status of fast RX Flags RSVD 2
RAWLANE3_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT	0x333B	W	0x00000000	Status of fast RX Flags RSVD 3
RAWLANE3_DIG_FSM_FAST_RX_IQ_ADAPT	0x333C	W	0x00000000	Status of fast RX IQ adapt start-up adaptation
RAWLANE3_DIG_FSM_RX_CTLE_ALGO_EH_SEL	0x333D	W	0x00000000	Status of RX CTLE adapt selected algo
RAWLANE3_DIG_FSM_RX_IQ_PHASE_OFFSET	0x333F	W	0x00000000	Offset value for IQ phase calculation
RAWLANE3_DIG_AON_AFE_ATT_IDAC_OFST	0x3340	W	0x00000080	Offset value for RX AFE ATT iDAC
RAWLANE3_DIG_AON_AFE_CTLE_IDAC_OFST	0x3341	W	0x00000080	Offset value for RX AFE CTLE iDAC
RAWLANE3_DIG_AON_AFE_VGA1_IDAC_OFST	0x3342	W	0x00000080	Offset values for RX AFE VGA1 iDAC
RAWLANE3_DIG_AON_RX_ADAPT_FOM	0x3343	W	0x00000000	Adaptation figure of merit (FOM)
RAWLANE3_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST	0x3344	W	0x00000080	Offset values for RX DFE summer odd iDAC
RAWLANE3_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST	0x3345	W	0x00000080	Offset values for RX DFE phase even vDAC
RAWLANE3_DIG_AON_DFE_PHASE_ODD_VDAC_OFST	0x3346	W	0x00000080	Offset values for RX DFE phase odd vDAC
RAWLANE3_DIG_AON_DFE_EVEN_REF_LVL	0x3347	W	0x00000000	DFE even reference level

Name	Offset	Size	Reset Value	Description
RAWLANE3_DIG_AON_DFE_ODD_REF_LVL	0x3348	W	0x00000000	DFE odd reference level
RAWLANE3_DIG_AON_RX_PHSADJ_LIN	0x3349	W	0x00000007	RX phase adjust Linear Value
RAWLANE3_DIG_AON_RX_PHSADJ_MAP	0x334A	W	0x00000000	RX phase adjust Mapped Value
RAWLANE3_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST	0x334B	W	0x00000080	Offset values for RX DFE data even high vDAC
RAWLANE3_DIG_AON_CDR_UNLOCKED_CNT	0x334C	W	0x00000080	Offset values for RX DFE data even low vDAC
RAWLANE3_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST	0x334D	W	0x00000080	Offset values for RX DFE data odd high vDAC
RAWLANE3_DIG_AON_RX_ADAPT_DONE_NEW	0x334E	W	0x00000080	Offset values for RX DFE data odd low vDAC
RAWLANE3_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST	0x334F	W	0x00000080	Offset values for RX DFE bypass even vDAC
RAWLANE3_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST	0x3350	W	0x00000080	Offset values for RX DFE bypass odd vDAC
RAWLANE3_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST	0x3351	W	0x00000080	Offset values for RX DFE error even vDAC
RAWLANE3_DIG_AON_DFE_ERROR_ODD_VDAC_OFST	0x3352	W	0x00000080	Offset values for RX DFE error odd vDAC
RAWLANE3_DIG_AON_RX_IQ_PHASE_ADJUST	0x3353	W	0x00000007	Value for RX IQ phase adjust
RAWLANE3_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET	0x3354	W	0x00000000	Value for RX IQ phase offset + delta value
RAWLANE3_DIG_AON_RX_FW_REVISION_PMA_LABEL	0x3355	W	0x00000000	Stores PMA label from IPXACT label
RAWLANE3_DIG_AON_INIT_PWRUP_DONE	0x3356	W	0x00000000	Initial power-up Done Status
RAWLANE3_DIG_AON_RX_ADPT_ATT	0x3357	W	0x00000000	RX Adapted value of ATT
RAWLANE3_DIG_AON_RX_ADPT_VGA	0x3358	W	0x00000000	RX Adapted value of VGA
RAWLANE3_DIG_AON_RX_ADPT_CTLE	0x3359	W	0x00000000	RX Adapted value of CTLE
RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP1	0x335A	W	0x00000000	RX Adapted value of DFE TAP1
RAWLANE3_DIG_AON_RX_ADAPT_DONE	0x335B	W	0x00000000	RX adaptation Done Status
RAWLANE3_DIG_AON_FAST_FLAGS	0x335C	W	0x00000000	Fast flags for simulation only
RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP2	0x335D	W	0x00000800	RX Adapted value of DFE TAP2

Name	Offset	Size	Reset Value	Description
RAWLANE3_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT	0x335E	W	0x00000000	boost_val_cost_function_lower_limit
RAWLANE3_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT	0x335F	W	0x00000000	boost_val_cost_function_upper_limit
RAWLANE3_DIG_AON_RX_FW_REVISION_RAW_LABEL	0x3360	W	0x00000000	Stores RAW label from IPXACT label
RAWLANE3_DIG_AON_RX_SLICER_CTRL_EVEN	0x3361	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
RAWLANE3_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE	0x3362	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
RAWLANE3_DIG_AON_RX_FW_REVISION_PCS_LABEL	0x3363	W	0x00000000	Stores PCS label from IPXACT label
RAWLANE3_DIG_AON_ADPT_CTL_0	0x3364	W	0x00000000	Adaptation Control register #0
RAWLANE3_DIG_AON_ADPT_CTL_1	0x3365	W	0x00000000	Adaptation Control register #1
RAWLANE3_DIG_AON_ADPT_CTL_2	0x3366	W	0x00000000	Adaptation Control register #2
RAWLANE3_DIG_AON_ADPT_CTL_3	0x3367	W	0x00000000	Adaptation Control register #3
RAWLANE3_DIG_AON_ADPT_CTL_4	0x3368	W	0x00000000	Adaptation Control register #4
RAWLANE3_DIG_AON_ADPT_CTL_5	0x3369	W	0x00000000	Adaptation Control register #5
RAWLANE3_DIG_AON_ADPT_CTL_6	0x336A	W	0x00000000	Adaptation Control register #6
RAWLANE3_DIG_AON_ADPT_CTL_7	0x336B	W	0x00000000	Adaptation Control register #7
RAWLANE3_DIG_AON_RX_FW_REVISION_FW_LABEL	0x336C	W	0x00000000	Stores FW label from IPXACT label
RAWLANE3_DIG_AON_FAST_FLAGS_2	0x336D	W	0x00000000	Fast flags for simulation only
RAWLANE3_DIG_AON_RX_RESERVED_REG_0	0x336E	W	0x00000000	Reserved Register 0
RAWLANE3_DIG_AON_TXRX_OVRD_IN	0x336F	W	0x00000000	Override values for incoming AON TX/RX controls from PCS
RAWLANE3_DIG_AON_RX_PHSADJ_LIN_LEFT	0x3370	W	0x00000000	RX phase adjust Linear Value Left side
RAWLANE3_DIG_AON_RX_PHSADJ_LIN_RIGHT	0x3371	W	0x00000000	RX phase adjust Linear Value Right side
RAWLANE3_DIG_AON_RX_PHSADJ_LIN_ADAPT	0x3372	W	0x00000000	RX phase adjust Linear IQ adapt Value
RAWLANE3_DIG_AON_RX_RESERVED_REG_1	0x3373	W	0x00000000	Reserved Register 1
RAWLANE3_DIG_AON_RX_ADPT_VGA_1	0x3378	W	0x00000000	RX Adapted value of VGA 1st iter
RAWLANE3_DIG_AON_RX_ADPT_CTLE_1	0x3379	W	0x00000000	RX Adapted value of CTLE 1st iter

Name	Offset	Size	Reset Value	Description
RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP1_1	0x337A	W	0x00000000	RX Adapted value of DFE TAP1 1st iter
RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP2_1	0x337D	W	0x00000800	RX Adapted value of DFE TAP2 1st iter
RAWLANE3_DIG_IRQ_CTL_RESET_RTN_REQ	0x3380	W	0x00000001	Reset routine request
RAWLANE3_DIG_IRQ_CTL_RX_RESET_IRQ	0x3381	W	0x00000000	Rx reset interrupt
RAWLANE3_DIG_IRQ_CTL_RX_REQ_IRQ	0x3382	W	0x00000000	Rx request interrupt
RAWLANE3_DIG_IRQ_CTL_RX_RATE_IRQ	0x3383	W	0x00000000	Rx rate change interrupt request
RAWLANE3_DIG_IRQ_CTL_RX_PSTATE_IRQ	0x3384	W	0x00000000	Rx pstate change interrupt request
RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ	0x3385	W	0x00000000	Rx adaptation request interrupt
RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ	0x3386	W	0x00000000	Rx adaptation disable interrupt
RAWLANE3_DIG_IRQ_CTL_RX_RESET_IRQ_CLR	0x3387	W	0x00000000	RX reset interrupt clear
RAWLANE3_DIG_IRQ_CTL_RX_REQ_IRQ_CLR	0x3388	W	0x00000000	RX request interrupt clear
RAWLANE3_DIG_IRQ_CTL_RX_RATE_IRQ_CLR	0x3389	W	0x00000000	RX rate change interrupt clear
RAWLANE3_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR	0x338A	W	0x00000000	RX pstate change interrupt clear
RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR	0x338B	W	0x00000000	RX adaptation request interrupt clear
RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR	0x338C	W	0x00000000	RX adaptation disable interrupt clear
RAWLANE3_DIG_IRQ_CTL_IRQ_MASK	0x338D	W	0x00000000	Interrupt Mask
RAWLANE3_DIG_IRQ_CTL_RX_INITIALIZE_IRQ	0x338E	W	0x00000000	Rx initialize change interrupt request
RAWLANE3_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR	0x338F	W	0x00000000	RX initialize change interrupt clear
RAWLANE3_DIG_PMA_XF_RX_OVRD_OUT	0x33A6	W	0x00000000	Override values for outgoing RX controls to PMA
RAWLANE3_DIG_PMA_XF_RX_PMA_IN	0x33A7	W	0x00000000	Current values for coming RX status controls from PMA
RAWLANE3_DIG_RX_CTL_OFFCAN_CONT_STATUS	0x33E3	W	0x00000000	RX continuous offset cancellation status
RAWLANE3_DIG_RX_CTL_ADAPT_CONT_STATUS	0x33E4	W	0x00000000	RX continuous adaptation status
RAWMEM_DIG_ROM_CMN_X_BY_RZ	0x4000~0x4FFF	W	0x00008002	Common mem #X, Bank #Y, Reg #Z (X=0~15, Y=0~7, Z=0~31)
RAWMEM_DIG_RAM_CMN_X_BY_RZ	0x6000~0x6FFF	W	0x00008002	Common mem #X, Bank #Y, Reg #Z (X=0~15, Y=0~7, Z=0~31)
SUPX_DIG_IDCODE_LO	0x8000	W	0x000004CD	Low 16 bits of IDCODE
SUPX_DIG_IDCODE_HI	0x8001	W	0x00003006	High 16 bits of IDCODE

Name	Offset	Size	Reset Value	Description
SUPX_DIG_REFCLK_OVRD_IN	0x8002	W	0x00000700	Override values for incoming REFCLK and RESET controls from ASIC
SUPX_DIG_RX_TERM_ACDC_EN_OVRD_IN	0x8003	W	0x00000000	Override values for incoming RX controls from ASIC
SUPX_DIG_TMDSCLK_CTRL_OVRD_IN	0x8004	W	0x00000004	Override values for incoming TMDSCLK controls from ASIC
SUPX_DIG_SUP_OVRD_IN	0x800D	W	0x00000008	Override values for support block ASIC inputs
SUPX_DIG_SUP_OVRD_OUT	0x800E	W	0x00000010	Override values for support block ASIC outputs
SUPX_DIG_LVL_OVRD_IN	0x800F	W	0x00000010	Override values for level settings
SUPX_DIG_DEBUG	0x8010	W	0x00000000	Debug controls
SUPX_DIG_RX_TERM_EN_ACDC_IN	0x8018	W	0x00000000	Current value for RX_TERM_EN and RX_TERM_ACDC
SUPX_DIG_ASIC_IN	0x8019	W	0x00000000	Current values for incoming SUP control signals from ASIC
SUPX_DIG_LVL_ASIC_IN	0x801A	W	0x00000000	Current values for incoming level controls from ASIC
SUPX_DIG_BANDGAP_ASIC_IN	0x801B	W	0x00000000	Current values for incoming bandgap control from ASIC
SUPX_DIG_CLK_RST_BG_PWRUP_TIME_0	0x8038	W	0x00000082	BG Power UP Time Register #0
SUPX_DIG_CLK_RST_BG_PWRUP_TIME_1	0x8039	W	0x00000208	BG Power UP Time Register #1
SUPX_DIG_ANA_CREGS_ANA_RTUNE_OVRD_IN	0x804A	W	0x00000000	Values for analog rtune block
SUPX_DIG_ANA_CREGS_ANA_ATB_IN	0x804B	W	0x00000000	Values for analog atb switch
SUPX_DIG_ANA_CREGS_ANA_BG_IN	0x804D	W	0x0000050A	Override values for analog bandgap block
SUPX_DIG_ANA_CREGS_TMDS_CLK_SETTING	0x804E	W	0x00000000	settings for TMDS clock reception and sense detection
SUPX_DIG_ANA_CREGS_SUP_ANA_NC	0x804F	W	0x00000000	Reserve values for sup analog block
SUPX_DIG_RTUNE_DEBUG	0x8060	W	0x00000000	Resistor tuning debug controls
SUPX_DIG_RTUNE_CONFIG	0x8061	W	0x00000014	Configure rtune Operation
SUPX_DIG_RTUNE_STAT	0x8062	W	0x00000000	Resistor tuning register status
SUPX_DIG_RTUNE_EARC_SET_VAL	0x8064	W	0x00000000	Set value of EARC Resistor
SUPX_DIG_RTUNE_RX21_SET_VAL	0x8065	W	0x00000000	Set value of RX21 Resistor
SUPX_DIG_RTUNE_EARC_STAT	0x8067	W	0x00000000	EARC Resistor tuning register status
SUPX_DIG_RTUNE_RX21_STAT	0x8068	W	0x00000000	RX21 Resistor tuning register status
SUPX_DIG_ANA_RX_OVERLOAD_PROT_EN_OVRD_OUT	0x8069	W	0x00000000	Override value for rx_ana_det0Vp_en_i and and rx_ana_det0Vn_en_i
SUPX_DIG_ANA_TMDSCLK_EN_OVRD_OUT	0x806A	W	0x00000000	Override value for tmdsclk_an_en signal going to ANA

Name	Offset	Size	Reset Value	Description
SUPX_DIG_ANA_EARC_TERM_CODE_OVRD_OUT	0x806B	W	0x00000000	Override value for EARC term code
SUPX_DIG_ANA_RX_TERM_CODE_OVRD_OUT	0x806C	W	0x00000000	Override value for RX term code
SUPX_DIG_ANA_RTUNE_OVRD_OUT	0x806D	W	0x00000000	Override value for rtune signals going to ANA
SUPX_DIG_ANA_STAT	0x806E	W	0x00000000	SUP input status register for SUP ANA outputs
SUPX_DIG_ANA_ANA_OVRD_OUT	0x806F	W	0x00000000	Override values for ana_async_rst and bandgap signals going to ANA
LANEX_DIG_ASIC_LANE_OVRD_IN	0x9000	W	0x00000000	Override values for incoming LANE controls from ASIC
LANEX_DIG_ASIC_RX_ASIC_LOS	0x9001	W	0x00000000	LOS Related signals
LANEX_DIG_ASIC_LOS_OVRD_IN	0x9002	W	0x00000010	Override values for LOS signal at ASIC side
LANEX_DIG_ASIC_LOS_OVRD_IN_1	0x9003	W	0x0000005A	Override values for LOS signal at ASIC side
LANEX_DIG_ASIC_CDR_CONTROL_OVRD_IN	0x9006	W	0x00000000	Override values for incoming CDR settings controls from ASIC
LANEX_DIG_ASIC_RX_OVRD_IN_0	0x9007	W	0x00000000	Override values for incoming RX controls from ASIC, register #0
LANEX_DIG_ASIC_RX_OVRD_IN_1	0x9008	W	0x00000014	Override values for incoming RX controls from ASIC, register #1
LANEX_DIG_ASIC_RX_OVRD_IN_2	0x9009	W	0x000003E8	Override values for incoming RX controls from ASIC, register #2
LANEX_DIG_ASIC_RX_OVRD_IN_3	0x900A	W	0x00000000	Override values for incoming RX controls from ASIC, register #3
LANEX_DIG_ASIC_RX_OVRD_IN_4	0x900B	W	0x00000000	Override values for incoming RX controls from ASIC, register #4
LANEX_DIG_ASIC_RX_OVRD_IN_5	0x900C	W	0x00000000	Override values for incoming RX controls from ASIC, register #5
LANEX_DIG_ASIC_RX_OVRD_EQ_IN_0	0x900D	W	0x00003078	Override values for incoming RX EQ controls from ASIC, register #0
LANEX_DIG_ASIC_RX_OVRD_EQ_IN_1	0x900E	W	0x00004040	Override values for incoming RX EQ controls from ASIC, register #1
LANEX_DIG_ASIC_RX_OVRD_OUT_0	0x900F	W	0x00000000	Override values for outgoing RX controls to ASIC, register #0
LANEX_DIG_ASIC_RX_ASIC_IN_0	0x9015	W	0x00000000	Current values for incoming RX controls from ASIC, register #0
LANEX_DIG_ASIC_RX_ASIC_IN_1	0x9016	W	0x00000000	Current values for incoming RX controls from ASIC, register #1
LANEX_DIG_ASIC_RX_EQ_ASIC_IN_0	0x9017	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #0
LANEX_DIG_ASIC_RX_EQ_ASIC_IN_1	0x9018	W	0x00000000	Current values for incoming RX EQ controls from ASIC, register #1
LANEX_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0	0x9019	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #0

Name	Offset	Size	Reset Value	Description
LANEX_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1	0x901A	W	0x00000000	Current values for incoming RX CDR VCO controls from ASIC, register #1
LANEX_DIG_ASIC_RX_ASIC_OUT_0	0x901B	W	0x00000000	Current values for outgoing RX status controls from PHY, register #0
LANEX_DIG_LBERT_CTL	0x9020	W	0x00000000	Pattern Generator controls
LANEX_DIG_RX_CDR_CDR_CTL_0	0x9024	W	0x0000000F	Control bits for receiver in recovered domain
LANEX_DIG_RX_CDR_CDR_CTL_1	0x9025	W	0x00007039	CDR Control Register #1
LANEX_DIG_RX_CDR_CDR_CTL_2	0x9026	W	0x00004ABB	CDR Control Register #2
LANEX_DIG_RX_CDR_CDR_CTL_3	0x9027	W	0x0000099B	CDR Control Register #3
LANEX_DIG_RX_CDR_CDR_CTL_4	0x9028	W	0x00000003	CDR Control Register #4
LANEX_DIG_RX_CDR_CDR_CTL_5	0x9029	W	0x00000649	CDR Control Register #5
LANEX_DIG_RX_CDR_CDR_CTL_6	0x902A	W	0x000006DB	CDR Control Register #6
LANEX_DIG_RX_CDR_CDR_CTL_7	0x902B	W	0x00008766	CDR Control Register #7
LANEX_DIG_RX_CDR_CDR_CTL_8	0x902C	W	0x0000ECCA	CDR Control Register #8
LANEX_DIG_RX_CDR_CDR_CTL_9	0x902D	W	0x00006432	CDR Control Register #9
LANEX_DIG_RX_CDR_CDR_CTL_10	0x902E	W	0x0000ECA8	CDR Control Register #10
LANEX_DIG_RX_CDR_STAT	0x902F	W	0x00000000	Current output values to dpll (phug, frug)
LANEX_DIG_RX_PWRCTL_RX_PSTATE_P0	0x9040	W	0x00000CF7	RX Power State Control Register for P0
LANEX_DIG_RX_PWRCTL_RX_PSTATE_P0S	0x9041	W	0x00000407	RX Power State Control Register for P0S
LANEX_DIG_RX_PWRCTL_RX_PSTATE_P1	0x9042	W	0x00000307	RX Power State Control Register for P1
LANEX_DIG_RX_PWRCTL_RX_PSTATE_P2	0x9043	W	0x00000301	RX Power State Control Register for P2
LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_0	0x9044	W	0x000001E6	RX Power UP Time Register #0
LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_1	0x9045	W	0x0000069A	RX Power UP Time Register #1
LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_2	0x9046	W	0x0000001A	RX Power UP Time Register #2
LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_3	0x9047	W	0x00000000	RX Power UP Time Register #3
LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0	0x9048	W	0x00000400	RX VCO calibration controls register #0
LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1	0x9049	W	0x00000100	RX VCO calibration controls register #1
LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2	0x904A	W	0x00002600	RX VCO calibration controls register #2

Name	Offset	Size	Reset Value	Description
LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0	0x904B	W	0x00003319	RX Power UP Time Register #0
LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1	0x904C	W	0x00000003	RX Power UP Time Register #1
LANEX_DIG_RX_VCOCAL_RX_VCO_STAT_0	0x904D	W	0x00000000	RX VCO status register #0
LANEX_DIG_RX_VCOCAL_RX_VCO_STAT_1	0x904E	W	0x00000000	RX VCO status register #1
LANEX_DIG_RX_VCOCAL_RX_VCO_STAT_2	0x904F	W	0x00000000	RX VCO status register #2
LANEX_DIG_RX_RX_ALIGN_XAUI_COMM_MASK	0x9050	W	0x000003FF	XAUI_COMMA mask
LANEX_DIG_RX_LBERT_CTL	0x9051	W	0x00000000	Pattern Matcher controls
LANEX_DIG_RX_LBERT_ERR	0x9052	W	0x00000000	Pattern match error counter
LANEX_DIG_RX_RX_LOS_LOS_0	0x9053	W	0x00000062	LOS Control Register #1
LANEX_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS	0x9055	W	0x00000000	Status of rx_pwrsm_state
LANEX_DIG_RX_DPLL_FREQ	0x905C	W	0x00002000	Current frequency integrator value.
LANEX_DIG_RX_DPLL_FREQ_BOUND_0	0x905D	W	0x000004C8	Frequency Bounds for incoming data stream #0
LANEX_DIG_RX_DPLL_FREQ_BOUND_1	0x905E	W	0x0000019C	Frequency Bounds for incoming data stream #1
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_0	0x9060	W	0x00000C10	Adaptation Configuration Register #0
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_1	0x9061	W	0x00000009	Adaptation Configuration Register #1
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_2	0x9062	W	0x000000C2	Adaptation Configuration Register #2
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_3	0x9063	W	0x00000000	Adaptation Configuration Register #3
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_4	0x9064	W	0x00000000	Adaptation Configuration Register #4
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_5	0x9065	W	0x00000000	Adaptation Configuration Register #5
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_6	0x9066	W	0x0000792B	Adaptation Configuration Register #6
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_7	0x9067	W	0x00004342	Adaptation Configuration Register #7
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_8	0x9068	W	0x00004925	Adaptation Configuration Register #8
LANEX_DIG_RX_ADPTCTL_ADPT_CFG_9	0x9069	W	0x00000000	Adaptation Configuration Register #9
LANEX_DIG_RX_ADPTCTL_RST_ADPT_CFG	0x906A	W	0x0000001F	Reset adaptation Configuration Register
LANEX_DIG_RX_ADPTCTL_ATT_STATUS	0x906B	W	0x00000000	Value of ATT adaptation code
LANEX_DIG_RX_ADPTCTL_VGA_STATUS	0x906C	W	0x00000000	Value of VGA adaptation code

Name	Offset	Size	Reset Value	Description
LANEX_DIG_RX_ADPTCTL_CTLE_STATUS	0x906D	W	0x00000000	Value of CTLE adaptation code
LANEX_DIG_RX_ADPTCTL_DFE_TAP1_STATUS	0x906E	W	0x00000000	Value of DFE Tap1 adaptation code
LANEX_DIG_RX_ADPTCTL_DFE_TAP2_STATUS	0x906F	W	0x00000000	Value of DFE Tap2 adaptation code
LANEX_DIG_RX_ADPTCTL_DFE_TAP3_STATUS	0x9070	W	0x00000000	Value of DFE Tap3 adaptation code
LANEX_DIG_RX_ADPTCTL_DFE_TAP4_STATUS	0x9071	W	0x00000000	Value of DFE Tap4 adaptation code
LANEX_DIG_RX_ADPTCTL_DFE_TAP5_STATUS	0x9072	W	0x00000000	Value of DFE Tap5 adaptation code
LANEX_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST	0x9073	W	0x00000080	Offset values for RX DFE data even vDAC
LANEX_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST	0x9074	W	0x00000080	Offset values for RX DFE data odd vDAC
LANEX_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN	0x9075	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
LANEX_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD	0x9076	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
LANEX_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST	0x9077	W	0x00000080	Offset values for RX DFE error even vDAC
LANEX_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST	0x9078	W	0x00000080	Offset values for RX DFE error odd vDAC
LANEX_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL	0x9079	W	0x00000000	Value of error slicer level
LANEX_DIG_RX_ADPTCTL_ADPT_RESET	0x907A	W	0x00000000	Adaptation reset register
LANEX_DIG_RX_STAT_LD_VAL_1	0x9080	W	0x00000040	Stat load value for the sample counter #1
LANEX_DIG_RX_STAT_DATA_MSK	0x9081	W	0x0000FFFF	Stat data mask bits [15:0]
LANEX_DIG_RX_STAT_MATCH_CTL0	0x9082	W	0x00003C06	Stat match controls register #0
LANEX_DIG_RX_STAT_MATCH_CTL1	0x9083	W	0x00000800	Stat match controls register #1
LANEX_DIG_RX_STAT_STAT_CTL0	0x9084	W	0x00004000	Stat controls register #0
LANEX_DIG_RX_STAT_STAT_CTL1	0x9085	W	0x00000008	Stat controls register #1
LANEX_DIG_RX_STAT_SMPL_CNT1	0x9086	W	0x00000000	Sample counter #1 Status
LANEX_DIG_RX_STAT_STAT_CNT_0	0x9087	W	0x00000000	Stat counter 0 Status
LANEX_DIG_RX_STAT_STAT_CNT_1	0x9088	W	0x00000000	Stat counter 1 Status
LANEX_DIG_RX_STAT_STAT_CNT_2	0x9089	W	0x00000000	Stat counter 2 Status

Name	Offset	Size	Reset Value	Description
LANEX_DIG_RX_STAT_STAT_CNT_3	0x908A	W	0x00000000	Stat counter 3 Status
LANEX_DIG_RX_STAT_STAT_CNT_4	0x908B	W	0x00000000	Stat counter 4 Status
LANEX_DIG_RX_STAT_STAT_CNT_5	0x908C	W	0x00000000	Stat counter 5 Status
LANEX_DIG_RX_STAT_STAT_CNT_6	0x908D	W	0x00000000	Stat counter 6 Status
LANEX_DIG_RX_STAT_CAL_COMP_CLK_CTL	0x908E	W	0x00000019	Calibration Comparator Control
LANEX_DIG_RX_STAT_MATCH_CTL2	0x908F	W	0x00000000	Stat match controls register #2
LANEX_DIG_RX_STAT_MATCH_CTL3	0x9090	W	0x00000000	Stat match controls register #3
LANEX_DIG_RX_STAT_MATCH_CTL4	0x9091	W	0x00000000	Stat match controls register #4
LANEX_DIG_RX_STAT_MATCH_CTL5	0x9092	W	0x00000000	Stat match controls register #5
LANEX_DIG_RX_STAT_STAT_CTL2	0x9093	W	0x00000000	Stat controls register #2
LANEX_DIG_RX_STAT_STAT_STOP	0x9094	W	0x00000000	Stat stop register
LANEX_DIG_ANA_TX_OVRD_OUT	0x90A0	W	0x00000000	Override values for TX signals going to ANA
LANEX_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT	0x90A1	W	0x00000000	Feature enable for tx_ana_lpbk_dfe_mode
LANEX_DIG_ANA_RX_DIV_OVRD_OUT	0x90A6	W	0x00000000	Override values for RX control signals going to ANA
LANEX_DIG_ANA_RX_CTL_OVRD_OUT	0x90A7	W	0x00000000	Override values for RX control signals going to ANA
LANEX_DIG_ANA_RX_PWR_OVRD_OUT	0x90A8	W	0x00000000	Override values for RX PWR UP/DN signals going to ANA
LANEX_DIG_ANA_RX_VCO_OVRD_OUT_0	0x90A9	W	0x00000000	Override values for RX VCO signals going to ANA #0
LANEX_DIG_ANA_RX_VCO_OVRD_OUT_1	0x90AA	W	0x00000002	Override values for RX VCO signals going to ANA #1
LANEX_DIG_ANA_RX_VCO_OVRD_OUT_2	0x90AB	W	0x00000000	Override values for RX VCO signals going to ANA #2
LANEX_DIG_ANA_RX_CAL	0x90AC	W	0x00000000	Sets values for RX CAL signals going to ANA register
LANEX_DIG_ANA_RX_DAC_CTRL	0x90AD	W	0x00000080	Sets values for RX DAC CTRL value going to ANA
LANEX_DIG_ANA_RX_DAC_CTRL_OVRD	0x90AE	W	0x00000000	Overrides RX DAC CTRL bus (en/val/sel) going to ANA
LANEX_DIG_ANA_RX_DAC_CTRL_SEL	0x90AF	W	0x00000000	Sets values for RX DAC CTRL Select signal going to ANA
LANEX_DIG_ANA_RX_AFE_ATT_VGA	0x90B0	W	0x00003000	Value for RX AFE ATT & VGA signals going to ANA
LANEX_DIG_ANA_RX_AFE_CTLE	0x90B1	W	0x00000000	Values for RX AFE CTLE signals going to ANA
LANEX_DIG_ANA_RX_SCOPE	0x90B2	W	0x00000000	Values for RX SCOPE signals going to ANA

Name	Offset	Size	Reset Value	Description
LANEX_DIG_ANA_RX_SLICER_CTRL	0x90B3	W	0x00000077	Sets values for RX slicer ctrl signals going to ANA register
LANEX_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST	0x90B4	W	0x00000007	Sets values for RX ANA IQ phase adjust signal going to ANA register
LANEX_DIG_ANA_RX_ANA_IQ_SENSE_EN	0x90B5	W	0x00000000	Sets values for RX ANA IQ SENSE signal
LANEX_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN	0x90B6	W	0x00000000	DAC CTRL enable signal
LANEX_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE	0x90B7	W	0x00000000	Afe update enable signal
LANEX_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK	0x90B8	W	0x00000000	PHASE adjust clock signal
LANEX_DIG_ANA_STATUS_0	0x90B9	W	0x00000000	Lane input status register #0
LANEX_DIG_ANA_STATUS_1	0x90BA	W	0x00000000	Lane input status register #1
LANEX_DIG_ANA_STATUS_LOS	0x90BB	W	0x00000000	LOS status at ana interface
LANEX_DIG_ANA_CREGS_TX_ANA_ATB_REG	0x90C0	W	0x00000000	TX ANA ATB measurement control register
LANEX_DIG_ANA_CREGS_RX_ANA_EQ_CTRL	0x90C4	W	0x00000034	RX ANA EQ control register
LANEX_DIG_ANA_CREGS_RX_ANA_VCO_CTRL	0x90C5	W	0x00000004	RX ANA VCO control register
LANEX_DIG_ANA_CREGS_RX_ANA_VREG_CTRL	0x90C6	W	0x00000001	RX ANA VREG control register
LANEX_DIG_ANA_CREGS_RX_ANA_DISCONNECT	0x90C7	W	0x00000000	RX ANA disconnect control
LANEX_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL	0x90C8	W	0x00000000	RX ANA reserved control register
LANEX_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1	0x90C9	W	0x00000000	RX ANA ATB control register 1
LANEX_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2	0x90CA	W	0x00000000	RX ANA ATB control register 2
RAWLANEX_DIG_PCS_XF_RX_OVRD_OUT_2	0xA003	W	0x00000000	Override values for outgoing RX controls to PCS register #2
RAWLANEX_DIG_PCS_XF_RX_PCS_IN_5	0xA004	W	0x00000000	Current values for incoming RX controls from PCS, register #5
RAWLANEX_DIG_PCS_XF_RX_OVRD_IN	0xA005	W	0x00000200	Override values for incoming RX controls from PCS
RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_1	0xA006	W	0x00000007	Override values for incoming RX controls from PCS, register #1
RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_2	0xA007	W	0x00000000	Override values for incoming RX controls from PCS, register #2
RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_3	0xA008	W	0x00000000	Override values for incoming RX controls from PCS, register #3
RAWLANEX_DIG_PCS_XF_RX_PCS_IN	0xA009	W	0x00000000	Current values for incoming RX controls from PCS
RAWLANEX_DIG_PCS_XF_RX_PCS_IN_1	0xA00A	W	0x00000000	Current values for incoming RX controls from PCS, register #1

Name	Offset	Size	Reset Value	Description
RAWLANEX_DIG_PCS_XF_RX_PCS_IN_2	0xA00B	W	0x00000000	Current values for incoming RX controls from PCS, register #2
RAWLANEX_DIG_PCS_XF_RX_PCS_IN_3	0xA00C	W	0x00000000	Current values for incoming RX controls from PCS, register #3
RAWLANEX_DIG_PCS_XF_RX_PCS_IN_4	0xA00D	W	0x00000000	Current values for incoming RX controls from PCS, register #4
RAWLANEX_DIG_PCS_XF_RX_OVRD_OUT	0xA00E	W	0x00000003	Override values for outgoing RX controls to PCS
RAWLANEX_DIG_PCS_XF_RX_PCS_OUT	0xA00F	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANEX_DIG_PCS_XF_RX_ADAPT_ACK	0xA010	W	0x00000000	RX adaptation Acknowledge
RAWLANEX_DIG_PCS_XF_RX_ADAPT_FOM	0xA011	W	0x00000000	RX adaptation figure of merit
RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_4	0xA012	W	0x00000000	Override values for incoming RX controls from PCS, register #4
RAWLANEX_DIG_PCS_XF_RX_PCS_OUT_2	0xA013	W	0x00000000	Current values for outgoing RX status controls from raw PCS
RAWLANEX_DIG_PCS_XF_LANE_NUMBER	0xA015	W	0x00000000	Current lane number
RAWLANEX_DIG_PCS_XF_ATE_OVRD_IN	0xA018	W	0x00000000	ATE override input to control top-level inputs
RAWLANEX_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN	0xA019	W	0x00000000	Override incoming values for rx_eq_delta_iq
RAWLANEX_DIG_PCS_XF_RX_EQ_OVRD_IN_1	0xA01D	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #1
RAWLANEX_DIG_PCS_XF_RX_EQ_OVRD_IN_2	0xA01E	W	0x00000000	Override values for incoming RX EQ controls from PCS, register #2
RAWLANEX_DIG_FSM_FSM_FSM_OVRD_CTL	0xA020	W	0x00000000	FSM override control register
RAWLANEX_DIG_FSM_FSM_MEM_ADDR_MON	0xA021	W	0x00000000	Memory Address Monitor
RAWLANEX_DIG_FSM_FSM_STATUS_MON	0xA022	W	0x00000000	FSM Status Monitor
RAWLANEX_DIG_FSM_FSM_CR_REG_OP_XTND_EN	0xA023	W	0x00000000	CR interface timing extension enable
RAWLANEX_DIG_FSM_FAST_RX_STARTUP_CAL	0xA024	W	0x00000000	Status of fast RX Start Up Calibration
RAWLANEX_DIG_FSM_FAST_RX_ADAPT	0xA025	W	0x00000000	Status of fast RX adaptation
RAWLANEX_DIG_FSM_FAST_RX_AFE_CAL	0xA026	W	0x00000000	Status of fast RX AFE Calibration
RAWLANEX_DIG_FSM_FAST_RX_DFE_CAL	0xA027	W	0x00000000	Status of fast RX DFE Calibration
RAWLANEX_DIG_FSM_FAST_RX_BYPASS_CAL	0xA028	W	0x00000000	Status of fast RX bypass Calibration
RAWLANEX_DIG_FSM_FAST_RX_REFLVL_CAL	0xA029	W	0x00000000	Status of fast RX Reference level Calibration
RAWLANEX_DIG_FSM_FAST_RX_IQ_CAL	0xA02A	W	0x00000000	Status of fast RX IQ Calibration
RAWLANEX_DIG_FSM_FAST_RX_AFE_ADAPT	0xA02B	W	0x00000000	Status of fast RX AFE adaptation

Name	Offset	Size	Reset Value	Description
RAWLANEX_DIG_FSM_FAST_RX_DFE_ADAPT	0xA02C	W	0x00000000	Status of fast RX DFE adaptation
RAWLANEX_DIG_FSM_FAST_SUP	0xA02D	W	0x00000000	Status of fast support block
RAWLANEX_DIG_FSM_FAST_RX_IQ_WALK	0xA02E	W	0x00000000	Status of fast RX IQ walk start-up adaptation
RAWLANEX_DIG_FSM_FAST_RX_PWRUP	0xA02F	W	0x00000000	Status of fast RX power-up
RAWLANEX_DIG_FSM_FAST_RX_VCO_WAIT	0xA030	W	0x00000000	Status of fast RX VCO Wait Times
RAWLANEX_DIG_FSM_FAST_RX_VCO_CAL	0xA031	W	0x00000000	Status of fast RX VCO calibration
RAWLANEX_DIG_FSM_FAST_RX_CONT_CAL_ADAPT	0xA033	W	0x00000000	Status of fast RX Continuous Calibration/Adaptation
RAWLANEX_DIG_FSM_FAST_RX_CONT_ADAPT	0xA034	W	0x00000000	Status of fast RX Continuous adaptation
RAWLANEX_DIG_FSM_FAST_RX_CONT_DATA_CAL	0xA035	W	0x00000000	Status of fast RX Continuous data Calibration
RAWLANEX_DIG_FSM_FAST_RX_CONT_PHASE_CAL	0xA036	W	0x00000000	Status of fast RX Continuous Phase Calibration
RAWLANEX_DIG_FSM_FAST_RX_CONT_AFE_CAL	0xA037	W	0x00000000	Status of fast RX Continuous AFE Calibration
RAWLANEX_DIG_FSM_FAST_RX_ATT_VGA_ADAPT	0xA038	W	0x00000000	Status of fast RX Flags RSVD 0
RAWLANEX_DIG_FSM_FAST_RX_CTLE_ADAPT	0xA039	W	0x00000000	Status of fast RX Flags RSVD 1
RAWLANEX_DIG_FSM_FAST_RX_VGA_ADAPT	0xA03A	W	0x00000000	Status of fast RX Flags RSVD 2
RAWLANEX_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT	0xA03B	W	0x00000000	Status of fast RX Flags RSVD 3
RAWLANEX_DIG_FSM_FAST_RX_IQ_ADAPT	0xA03C	W	0x00000000	Status of fast RX IQ adapt start-up adaptation
RAWLANEX_DIG_FSM_RX_CTLE_ALGO_EH_SEL	0xA03D	W	0x00000000	Status of RX CTLE adapt selected algo
RAWLANEX_DIG_FSM_RX_IQ_PHASE_OFFSET	0xA03F	W	0x00000000	Offset value for IQ phase calculation
RAWLANEX_DIG_AON_AFE_ATT_IDAC_OFST	0xA040	W	0x00000080	Offset value for RX AFE ATT iDAC
RAWLANEX_DIG_AON_AFE_CTLE_IDAC_OFST	0xA041	W	0x00000080	Offset value for RX AFE CTLE iDAC
RAWLANEX_DIG_AON_AFE_VGA1_IDAC_OFST	0xA042	W	0x00000080	Offset values for RX AFE VGA1 iDAC
RAWLANEX_DIG_AON_RX_ADAPT_FOM	0xA043	W	0x00000000	Adaptation figure of merit (FOM)
RAWLANEX_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST	0xA044	W	0x00000080	Offset values for RX DFE summer odd iDAC
RAWLANEX_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST	0xA045	W	0x00000080	Offset values for RX DFE phase even vDAC
RAWLANEX_DIG_AON_DFE_PHASE_ODD_VDAC_OFST	0xA046	W	0x00000080	Offset values for RX DFE phase odd vDAC

Name	Offset	Size	Reset Value	Description
RAWLANEX_DIG_AON_DFE_EVEN_REF_LVL	0xA047	W	0x00000000	DFE even reference level
RAWLANEX_DIG_AON_DFE_ODD_REF_LVL	0xA048	W	0x00000000	DFE odd reference level
RAWLANEX_DIG_AON_RX_PHSADJ_LIN	0xA049	W	0x00000007	RX phase adjust Linear Value
RAWLANEX_DIG_AON_RX_PHSADJ_MAP	0xA04A	W	0x00000000	RX phase adjust Mapped Value
RAWLANEX_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST	0xA04B	W	0x00000080	Offset values for RX DFE data even high vDAC
RAWLANEX_DIG_AON_CDR_UNLOCKED_CNT	0xA04C	W	0x00000080	Offset values for RX DFE data even low vDAC
RAWLANEX_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST	0xA04D	W	0x00000080	Offset values for RX DFE data odd high vDAC
RAWLANEX_DIG_AON_RX_ADAPT_DONE_NEW	0xA04E	W	0x00000080	Offset values for RX DFE data odd low vDAC
RAWLANEX_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST	0xA04F	W	0x00000080	Offset values for RX DFE bypass even vDAC
RAWLANEX_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST	0xA050	W	0x00000080	Offset values for RX DFE bypass odd vDAC
RAWLANEX_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST	0xA051	W	0x00000080	Offset values for RX DFE error even vDAC
RAWLANEX_DIG_AON_DFE_ERROR_ODD_VDAC_OFST	0xA052	W	0x00000080	Offset values for RX DFE error odd vDAC
RAWLANEX_DIG_AON_RX_IQ_PHASE_ADJUST	0xA053	W	0x00000007	Value for RX IQ phase adjust
RAWLANEX_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET	0xA054	W	0x00000000	Value for RX IQ phase offset + delta value
RAWLANEX_DIG_AON_RX_FW_REVISION_PMA_LABEL	0xA055	W	0x00000000	Stores PMA label from IPXACT label
RAWLANEX_DIG_AON_INIT_PWRUP_DONE	0xA056	W	0x00000000	Initial power-up Done Status
RAWLANEX_DIG_AON_RX_ADPT_ATT	0xA057	W	0x00000000	RX Adapted value of ATT
RAWLANEX_DIG_AON_RX_ADPT_VGA	0xA058	W	0x00000000	RX Adapted value of VGA
RAWLANEX_DIG_AON_RX_ADPT_CTLE	0xA059	W	0x00000000	RX Adapted value of CTLE
RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP1	0xA05A	W	0x00000000	RX Adapted value of DFE TAP1
RAWLANEX_DIG_AON_RX_ADAPT_DONE	0xA05B	W	0x00000000	RX adaptation Done Status
RAWLANEX_DIG_AON_FAST_FLAGS	0xA05C	W	0x00000000	Fast flags for simulation only
RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP2	0xA05D	W	0x00000800	RX Adapted value of DFE TAP2

Name	Offset	Size	Reset Value	Description
RAWLANEX_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT	0xA05E	W	0x00000000	boost_val_cost_function_lower_limit
RAWLANEX_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT	0xA05F	W	0x00000000	boost_val_cost_function_upper_limit
RAWLANEX_DIG_AON_RX_FW_REVISION_RAW_LABEL	0xA060	W	0x00000000	Stores RAW label from IPXACT label
RAWLANEX_DIG_AON_RX_SLICER_CTRL_EVEN	0xA061	W	0x00000007	Sets values for RX slicer ctrl even signals going to ANA
RAWLANEX_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE	0xA062	W	0x00000007	Sets values for RX slicer ctrl odd signals going to ANA
RAWLANEX_DIG_AON_RX_FW_REVISION_PCS_LABEL	0xA063	W	0x00000000	Stores PCS label from IPXACT label
RAWLANEX_DIG_AON_ADPT_CTL_0	0xA064	W	0x00000000	Adaptation Control register #0
RAWLANEX_DIG_AON_ADPT_CTL_1	0xA065	W	0x00000000	Adaptation Control register #1
RAWLANEX_DIG_AON_ADPT_CTL_2	0xA066	W	0x00000000	Adaptation Control register #2
RAWLANEX_DIG_AON_ADPT_CTL_3	0xA067	W	0x00000000	Adaptation Control register #3
RAWLANEX_DIG_AON_ADPT_CTL_4	0xA068	W	0x00000000	Adaptation Control register #4
RAWLANEX_DIG_AON_ADPT_CTL_5	0xA069	W	0x00000000	Adaptation Control register #5
RAWLANEX_DIG_AON_ADPT_CTL_6	0xA06A	W	0x00000000	Adaptation Control register #6
RAWLANEX_DIG_AON_ADPT_CTL_7	0xA06B	W	0x00000000	Adaptation Control register #7
RAWLANEX_DIG_AON_RX_FW_REVISION_FW_LABEL	0xA06C	W	0x00000000	Stores FW label from IPXACT label
RAWLANEX_DIG_AON_FAST_FLAGS_2	0xA06D	W	0x00000000	Fast flags for simulation only
RAWLANEX_DIG_AON_RX_RESERVED_REG_0	0xA06E	W	0x00000000	Reserved Register 0
RAWLANEX_DIG_AON_TXRX_OVRD_IN	0xA06F	W	0x00000000	Override values for incoming AON TX/RX controls from PCS
RAWLANEX_DIG_AON_RX_PHSADJ_LIN_LEFT	0xA070	W	0x00000000	RX phase adjust Linear Value Left side
RAWLANEX_DIG_AON_RX_PHSADJ_LIN_RIGHT	0xA071	W	0x00000000	RX phase adjust Linear Value Right side
RAWLANEX_DIG_AON_RX_PHSADJ_LIN_ADAPT	0xA072	W	0x00000000	RX phase adjust Linear IQ adapt Value
RAWLANEX_DIG_AON_RX_RESERVED_REG_1	0xA073	W	0x00000000	Reserved Register 1
RAWLANEX_DIG_AON_RX_ADPT_VGA_1	0xA078	W	0x00000000	RX Adapted value of VGA 1st iter
RAWLANEX_DIG_AON_RX_ADPT_CTLE_1	0xA079	W	0x00000000	RX Adapted value of CTLE 1st iter

Name	Offset	Size	Reset Value	Description
RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP1_1	0xA07A	W	0x00000000	RX Adapted value of DFE TAP1 1st iter
RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP2_1	0xA07D	W	0x00000800	RX Adapted value of DFE TAP2 1st iter
RAWLANEX_DIG_IRQ_CTL_RESET_RTN_REQ	0xA080	W	0x00000001	Reset routine request
RAWLANEX_DIG_IRQ_CTL_RX_RESET_IRQ	0xA081	W	0x00000000	Rx reset interrupt
RAWLANEX_DIG_IRQ_CTL_RX_REQ_IRQ	0xA082	W	0x00000000	Rx request interrupt
RAWLANEX_DIG_IRQ_CTL_RX_RATE_IRQ	0xA083	W	0x00000000	Rx rate change interrupt request
RAWLANEX_DIG_IRQ_CTL_RX_PSTATE_IRQ	0xA084	W	0x00000000	Rx pstate change interrupt request
RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ	0xA085	W	0x00000000	Rx adaptation request interrupt
RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ	0xA086	W	0x00000000	Rx adaptation disable interrupt
RAWLANEX_DIG_IRQ_CTL_RX_RESET_IRQ_CLR	0xA087	W	0x00000000	RX reset interrupt clear
RAWLANEX_DIG_IRQ_CTL_RX_REQ_IRQ_CLR	0xA088	W	0x00000000	RX request interrupt clear
RAWLANEX_DIG_IRQ_CTL_RX_RATE_IRQ_CLR	0xA089	W	0x00000000	RX rate change interrupt clear
RAWLANEX_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR	0xA08A	W	0x00000000	RX pstate change interrupt clear
RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR	0xA08B	W	0x00000000	RX adaptation request interrupt clear
RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR	0xA08C	W	0x00000000	RX adaptation disable interrupt clear
RAWLANEX_DIG_IRQ_CTL_IRQ_MASK	0xA08D	W	0x00000000	Interrupt Mask
RAWLANEX_DIG_IRQ_CTL_RX_INITIALIZE_IRQ	0xA08E	W	0x00000000	Rx initialize change interrupt request
RAWLANEX_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR	0xA08F	W	0x00000000	RX initialize change interrupt clear
RAWLANEX_DIG_PMA_XF_RX_OVRD_OUT	0xA0A6	W	0x00000000	Override values for outgoing RX controls to PMA
RAWLANEX_DIG_PMA_XF_RX_PMA_IN	0xA0A7	W	0x00000000	Current values for coming RX status controls from PMA
RAWLANEX_DIG_RX_CTL_OFFCAN_CONT_STATUS	0xA0E3	W	0x00000000	RX continuous offset cancellation status
RAWLANEX_DIG_RX_CTL_ADAPT_CONT_STATUS	0xA0E4	W	0x00000000	RX continuous adaptation status

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

28.4.3 Detail Registers Description

SUP_DIG_IDCODE_LO

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x34cd	data Data

SUP_DIG_IDCODE_HI
Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x3c42	data Data

SUP_DIG_REFCLK_OVRD_IN
Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	bg_en_ovrd_en Enable override for bg_en
12	RW	0x0	bg_en Override value for bg_en
11	RW	0x0	ref_clk_range_ovrd_en Enable override for ref_range
10:8	RW	0x7	ref_clk_range Override value for ref_range
7	RW	0x0	reserved_7 Reserved_7
6	RW	0x0	reserved_6 Reserved_6
5	RW	0x0	reserved_5 Reserved_5
4	RW	0x0	reserved_4 Reserved_4
3	RW	0x0	reserved_3 Reserved_3
2	RW	0x0	reserved_2 Reserved_2
1	RW	0x0	ref_clk_en_ovrd_en Enable override for ref_clk_en
0	RW	0x0	ref_clk_en Override value for ref_clk_en

SUP_DIG_RX_TERM_ACDC_EN_OVRD_IN
Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	term_ovrd_en Enable override for rx_term_acdc and rx_term_en
1	RW	0x0	reserved_1 Reserved_1
0	RW	0x0	term_en Override value for rx_term_en

SUP_DIG_TMDSCLK_CTRL_OVRD_IN
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	tmdsclk_digmux_ovrd_en Override enable for tmdsclk_digmux_en
4	RW	0x0	tmdsclk_digmux_en Override value for tmdsclk_digmux_en
3	RW	0x0	tmdsclk_rst_ovrd_en Override enable for tmdsclk_rst
2	RW	0x1	tmdsclk_rst Override value for tmdsclk_rst
1	RW	0x0	tmdsclk_en_ovrd_en Override enable for tmdsclk_en
0	RW	0x0	tmdsclk_en Override value for tmdsclk_en

SUP_DIG_SUP_OVRD_IN
Address: Operational Base + offset (0x000D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	res_ovrd_en Enable override of res_req_in and res_ack_in
3	RW	0x1	res_ack_in Override value for res_ack_in
2	RW	0x0	res_req_in Override value for res_req_in
1	RW	0x0	rtune_ovrd_en Enable override of rtune_req
0	RW	0x0	rtune_req Override value for rtune_req

SUP_DIG_SUP_OVRD_OUT
Address: Operational Base + offset (0x000E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	bg_lane_state_ovrd_en Enable override for bg_lane_state signal
6	RW	0x0	bg_lane_state Override value for bg_lane_state signal
5	RW	0x0	res_ack_out_ovrd_en Enable override for res_ack_out output
4	RW	0x1	res_ack_out Override value for res_ack_out output
3	RW	0x0	res_req_out_ovrd_en Enable override for res_req_out output
2	RW	0x0	res_req_out Override value for res_req_out output

Bit	Attr	Reset Value	Description
1	RW	0x0	rtune_ack_ovrd_en Enable override for rtune_ack output
0	RW	0x0	rtune_ack Override value for rtune_ack output

SUP_DIG_LVL_OVRD_IN
Address: Operational Base + offset (0x000F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_vref_ctrl_en Enable override value for rx_vref_ctrl
4:0	RW	0x10	rx_vref_ctrl Override value for rx_vref_ctrl

SUP_DIG_DEBUG
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2:0	RW	0x0	dtb_sel The lane DTB's are OR'd together with the support DTB signals selected with the below encodings 3'b000: None 3'b001: None 3'b010: None 3'b011: Rtune DTB output Others: Reserved

SUP_DIG_RX_TERM_EN_ACDC_IN
Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RO	0x0	rereseved_1 Reserved_1
0	RO	0x0	rx_term_en Value from ASIC for rx_term_en

SUP_DIG_ASIC_IN
Address: Operational Base + offset (0x0019)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	rx_dig_det0vn_en Value to ASIC for rx_dig_det0Vn_en
13	RO	0x0	rx_dig_det0vp_en Value to ASIC for rx_dig_det0Vp_en
12	RO	0x0	res_ack_out Value to ASIC for res_ack_out_i

Bit	Attr	Reset Value	Description
11	RO	0x0	res_ack_in Value from ASIC for res_req_in
10	RO	0x0	res_req_out Value to ASIC for res_ack_out_i
9	RO	0x0	res_req_in Value from ASIC for res_req_in
8	RO	0x0	rtune_ack Value to ASIC for rtune_ack_i
7	RO	0x0	rtune_req Value from ASIC for rtune_req
6	RO	0x0	test_powerdown Value from ASIC for test_powerdown
5	RO	0x0	test_burnin Value from ASIC for test_burnin
4	RO	0x0	reserved_4 Reserved_4
3	RO	0x0	reserved_3 Reserved_3
2	RO	0x0	reserved_2 Reserved_2
1	RO	0x0	ref_clk_en Value from ASIC for ref_clk_en
0	RO	0x0	phy_reset Value from ASIC for phy_reset

SUP_DIG_LVL_ASIC_IN
Address: Operational Base + offset (0x001A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_vref_ctrl Value from ASIC for rx_vref_ctrl

SUP_DIG_BANDGAP_ASIC_IN
Address: Operational Base + offset (0x001B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	bg_en Value from ASIC for bg_en

SUP_DIG_CLK_RST_BG_PWRUP_TIME_0
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	fast_bg_wait Enable fast BG times (simulation only)
8:0	RW	0x082	bg_sup_en_time Power up time (in ref_range cycles) for bandgap in SUP (spec >=5us)

SUP_DIG_CLK_RST_BG_PWRUP_TIME_1
Address: Operational Base + offset (0x0039)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x208	bg_lane_en_time Power up time (in ref_range cycles) for bandgap in LANE (spec >= 20us)

SUP_DIG_ANA_CREGS_ANA_RTUNE_OVRD_IN
Address: Operational Base + offset (0x004A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rt_en_frcon Local rtune block enable control, force rtune block on, if asserted
6	RW	0x0	reserved Reserved
5	RW	0x0	rt_dac_mode_1_ RT_DAC_MODE[1]
4	RW	0x0	rt_dac_mode_0_ For 0 NOP, 1 DAC drives atb_s_p or atb_s_m
3	RW	0x0	rt_dac_chop For 0 atb_s_m, for 1 atb_s_p
2	RW	0x0	rt_atb Rtune ATB mode control. Combines with rt_ana_mode[1:0] to perform different functions
1	RW	0x0	rt_sel_atbp Rtune ATB input select: RT_SEL_ATBP function 1'b1: Select atb_s_p 1'b0: Select atb_s_m
0	RW	0x0	rt_sel_atbf Rtune ATB input select: RT_SEL_ATBF function 1'b1: Select gd as input 1'b0: Select atb_s_p/m as input

SUP_DIG_ANA_CREGS_ANA_ATB_IN
Address: Operational Base + offset (0x004B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	sup_ana_ovl_osc_disable4test_int Force the output of protection oscillator
6	RW	0x0	atb_switch_6 Connect atb_s_p to atb_s_m, if asserted
5	RW	0x0	atb_switch_5 Connect atb_s_p to vph, if asserted
4	RW	0x0	atb_switch_4 Connect atb_s_p to gd, if asserted
3	RW	0x0	atb_switch_3 Connect atb_s_p to vp, if asserted

Bit	Attr	Reset Value	Description
2	RW	0x0	atb_switch_2 Connect atb_s_p to vbg_vref, if asserted
1	RW	0x0	atb_switch_1 Connect atb_s_p to vph, if asserted
0	RW	0x0	atb_switch_0 Connect atb_s_p to vbg_bias_vref, if asserted

SUP_DIG_ANA_CREGS_ANA_BG_IN

Address: Operational Base + offset (0x004D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RW	0x1	sel_clk_vref VREG clk reference voltage control.
9:8	RW	0x1	sel_vco_vref VREG VCO reference voltage control.
7:6	RW	0x0	sup_ovl_osc_width_int Pulse width of over-current protection oscillator clk_ovl_osc_width[1:0] 2'b00: Pulse width 64 cycles, and it is 14.08us, pulse period 225.28 us 2'b01: Pulse width 1 cycles, and it is 0.22us, pulse period 225.28 us 2'b10: Pulse width 128 cycles, and it is 28.16us, pulse period 225.28 us 2'b11: Pulse width 32 cycles, and it is 7.04us, pulse period 225.28 us Counter width: 1024. Single clock period: 220ns
5	RW	0x0	temp_meas If asserted, enable temperature measurement. Vbe is sent to atb_s_m, vbg is sent to atb_s_p
4	RW	0x0	por_start_kick_en Enable fast startup using bg kick voltage for POR bandgap outputs
3	RW	0x1	chop_en_int Enable chopper clock for bandgap
2:1	RW	0x1	sel_vbg_vref vbg_vref voltage level select. Default value is 2'b01
0	RW	0x0	bypass_bg Bypass bandgap with VP

SUP_DIG_ANA_CREGS_TMDS_CLK_SETTING

Address: Operational Base + offset (0x004E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:3	RW	0x0	tmdsclk_threshold TMDS clock sense circuit threshold value. Default value is 2'b00
2:1	RW	0x0	tmdsclk_hyst TMDS clock sense circuit hysterisis value. Default value is 2'b00
0	RW	0x0	tmdsclk_sense_en TMDS clock sense enable. Overrides the TMDS clock reception enable.

SUP_DIG_ANA_CREGS_SUP_ANA_NC

Address: Operational Base + offset (0x004F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:3	RW	0x00	reserved_7_3 Reserved bits
2	RW	0x0	clk_sense_mode Clock sense mode programmability 1'b1: Clock sense mode 1'b0: Normal operation
1	RW	0x0	clk_sense_write_en Clock sense programmability enable 1'b1: Programmability enabled 1'b0: Programmability disabled
0	RW	0x0	clk_sense_write_clk Clock input used to latch analog clock sense mode control registers. Falling edge - latching

SUP_DIG_RTUNE_DEBUG

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx21_go Enable RX21 tune to continue in manual tune mode when type is RX21 tune. When in non RX21 manual tune mode, this bit must be 0. When in RX21 manual tune mode and after RX21 manual tune is triggered, if the read only register SUP.RTUNE_STAT.DTB_RTUNE equals to 2'b01, it is required to first release the tune related asynchronous override on analog/digital interface then turn this bit RX21_GO from low to high to continue RX21 manual tune which also indicates that this bit needs to be low when triggering RX21 manual tune.
14:5	RW	0x000	value Value to use when triggering SET_VAL field only the 6 LSB's are used when setting RX cal values
4:3	RW	0x0	type Type of manual tuning or register read/write to execute 2'b00: ADC, or read/write rt_value 2'b01: None 2'b10: EARC tune, or read/write earc_cal_val (10 bits) 2'b11: RX21 tune, or read/write rx21_cal_val (10 bits) or resref detect (no affect when triggering SET_VAL field)
2	RW	0x0	set_val Set value Write to a 1 to manually write the register specified by the TYPE field to the value in the VALUE field
1	RW	0x0	man_tune Write to a 1 to do a manual tuning specified by TYPE field starting a manual tune while a tune is currently running can cause unpredictable results. For use only when you know what the part is doing (w.r.t. resistor tuning)

Bit	Attr	Reset Value	Description
0	RW	0x0	flip_comp Invert analog comparator output

SUP_DIG_RTUNE_CONFIG

Address: Operational Base + offset (0x0061)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RW	0x2	sup_ana_term_ctrl Set the reference resistor in the analog value impedence (Ohms) 3'b000: 54 3'b001: 52 3'b010: 50 (default) 3'b011: 48 3'b100: 46 3'b101: 44 3'b110: 42 3'b111: 40
2	RW	0x1	earc_rx_cal_en Enable calibration of EARC and RX21 resistor
1	RW	0x0	fast_rtune Enable fast resistor tuning (simulation only)
0	RW	0x0	reserved Reserved

SUP_DIG_RTUNE_STAT

Address: Operational Base + offset (0x0062)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RO	0x0	dtb_rtune DTB sampling for rtune
9:0	RO	0x000	stat Current value of the register specified by the DEBUG.TYPE field

SUP_DIG_RTUNE_EARC_SET_VAL

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	earc_set_val Set value of tx-dn resistor. Writing a value to this register will set the tx-dn resistor value.

SUP_DIG_RTUNE_RX21_SET_VAL

Address: Operational Base + offset (0x0065)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use

Bit	Attr	Reset Value	Description
9:0	RW	0x000	rx21_set_val Set value of rx21 resistor. Writing a value to this register will set the tx-up resistor value.

SUP_DIG_RTUNE_EARC_STAT
Address: Operational Base + offset (0x0067)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RO	0x000	earc_stat Current value of the EARC resistor tuning register

SUP_DIG_RTUNE_RX21_STAT
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RO	0x000	rx21_stat Current value of the RX21 resistor tuning register

SUP_DIG_ANA_RX_OVERLOAD_PROT_EN_OVRD_OUT
Address: Operational Base + offset (0x0069)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	ovrd_sel_det0vn Override select bit for rx_ana_det0Vn_en output
2	RW	0x0	rx_ana_det0vn_en_r Overrides for rx_ana_det0Vn_en signal
1	RW	0x0	ovrd_sel_det0vp Override select bit for rx_ana_det0Vp_en output
0	RW	0x0	rx_ana_det0vp_en_r Overrides for rx_ana_det0Vp_en signal

SUP_DIG_ANA_TMDSCLK_EN_OVRD_OUT
Address: Operational Base + offset (0x006A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	ovrd_sel Override bit for tmdsclk_ana_en output
0	RW	0x0	tmdsclk_ana_en_r Overrides the tmdsclk_ana_en_i signal

SUP_DIG_ANA_EARC_TERM_CODE_OVRD_OUT
Address: Operational Base + offset (0x006B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use

Bit	Attr	Reset Value	Description
7	RW	0x0	earc_ovrd_sel Override enable for earc_term_code
6:0	RW	0x00	earc_term_code Overrides the earc_term_code signal

SUP_DIG_ANA_RX_TERM_CODE_OVRD_OUT
Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rx_ovrd_sel Override enable for rx_term_code
6:0	RW	0x00	rx_term_code Overrides the rx_term_code signal

SUP_DIG_ANA_RTUNE_OVRD_OUT
Address: Operational Base + offset (0x006D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RW	0x0	rtune_ovrd_en Override bit for rtune (rt_ana_* and term) outputs
13:4	RW	0x000	rtune_value Overrides the rt_ana_value[9:0] signal
3	RW	0x0	rtune_en Overrides the rt_ana_en signal
2:1	RW	0x0	rtune_mode Overrides the rt_ana_mode[1:0] signal
0	RW	0x0	rtune_comp_rst Overrides the rt_ana_comp_rst signal

SUP_DIG_ANA_STAT
Address: Operational Base + offset (0x006E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rt_ana_comp_result Value from ANA for rt_ana_comp_result

SUP_DIG_ANA_ANA_OVRD_OUT
Address: Operational Base + offset (0x006F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_vreg_fast_start Overrides the signal rx_ana_vreg_fast_start
4	RW	0x0	ana_async_rst_ovrd_en Override enable for ana_async_rst
3	RW	0x0	ana_async_rst Override value for reset register for analog latches

Bit	Attr	Reset Value	Description
2	RW	0x0	bg_ovrd_en Override bit for bandgap outputs
1	RW	0x0	bg_en Overrides the bg_ana_en signal
0	RW	0x0	bg_fast_start Overrides the bg_ana_fast_start signal

LANE0_DIG_ASIC_LANE_OVRD_IN
Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_loopback_clk_en Loopback clock enable. When enabled the VCO clock of current lane is sent to the adjacent lane for TX BIST operation
1	RW	0x0	Reserve_1 Reserve_1
0	RW	0x0	Reserve_0 Reserve_0

LANE0_DIG_ASIC_RX_ASIC_LOS
Address: Operational Base + offset (0x1001)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	los_en Value from asic for rx_los_en
14	RO	0x0	los_clk_en Value from asic for rx_los_clk_en
13:4	RO	0x000	los_timer_thresh Value from asic for rx_los_timer_thresh1
3:1	RO	0x0	los_threshold Value from asic for rx_los_threshold
0	RO	0x0	los Value of rx_los towards asic

LANE0_DIG_ASIC_LOS_OVRD_IN
Address: Operational Base + offset (0x1002)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	rx_los_ovrd Override enable for rx_los
8	RW	0x0	rx_los_r Override value for rx_los
7	RW	0x0	rx_los_threshold_ovrd Override enable for rx_los_threshold
6:4	RW	0x1	rx_los_threshold_r Override value for rx_los_threshold
3	RW	0x0	rx_los_clk_en_ovrd Override enable for rx_los_clk_en
2	RW	0x0	rx_los_clk_en_r Override value for rx_los_clk_en

Bit	Attr	Reset Value	Description
1	RW	0x0	rx_los_en_ovrd Override enable for rx_los_en
0	RW	0x0	rx_los_en_r Override value for rx_los_en

LANE0_DIG_ASIC_LOS_OVRD_IN_1
Address: Operational Base + offset (0x1003)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RW	0x0	rx_los_timer_thresh_ovrd Override enable for rx_los_timer_thresh1
9:0	RW	0x05a	rx_los_timer_thresh_r Override value for rx_los_timer_thresh1

LANE0_DIG_ASIC_CDR_CONTROL_OVRD_IN
Address: Operational Base + offset (0x1006)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:1	RW	0x0	cdr_setting_sel Override values for CDR setting bits which select the CDR gain values
0	RW	0x0	cdr_setting_sel_ovrd_en Override enable for cdr_setting_sel signal

LANE0_DIG_ASIC_RX_OVRD_IN_0
Address: Operational Base + offset (0x1007)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:13	RW	0x0	rate_3_2 Override value for rx_rate[3:2]
12	RW	0x0	width_ovrd_en Enable override for rx_width
11:10	RW	0x0	width Override value for rx_width
9	RW	0x0	rate_ovrd_en Enable override value for rx_rate[1:0]
8:7	RW	0x0	rate_1_0 Override value for rx_rate
6	RW	0x0	pstate_ovrd_en Enable override value for rx_pstate
5:4	RW	0x0	pstate Override value for rx_pstate
3	RW	0x0	data_en_ovrd_en Enable override value for rx_data_en
2	RW	0x0	data_en Override value for rx_data_en
1	RW	0x0	req_ovrd_en Enable override value for rx_req

Bit	Attr	Reset Value	Description
0	RW	0x0	req Override value for rx_req

LANE0_DIG_ASIC_RX_OVRD_IN_1
Address: Operational Base + offset (0x1008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:10	RW	0x0	rx_clk_x2_en Override value for rx_clk_x2_en[2:0]
9	RW	0x0	rx_cdr_vco_highfreq Override value for rx_cdr_vco_highfreq
8	RW	0x0	rx_ref_ld_val_6 Override value for rx_ref_ld_val[6]
7	RW	0x0	en Enable override values for all inputs controlled by this register
6	RW	0x0	rx_cdr_vco_lowfreq Override value for rx_cdr_vco_lowfreq
5:0	RW	0x14	rx_ref_ld_val_5_0 Override value for rx_ref_ld_val[5:0]

LANE0_DIG_ASIC_RX_OVRD_IN_2
Address: Operational Base + offset (0x1009)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	en Enable override values for all inputs controlled by this register
12:0	RW	0x03e8	rx_vco_ld_val Override value for rx_vco_ld_val

LANE0_DIG_ASIC_RX_OVRD_IN_3
Address: Operational Base + offset (0x100A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x00	reserved_14_to_10 Reserved_14_to_10
9	RW	0x0	disable_ovrd_en Enable override for rx_disable
8	RW	0x0	disable Override value for rx_disable
7	RW	0x0	clk_shift_ovrd_en Enable override for rx_clk_shift
6	RW	0x0	clk_shift Override value for rx_clk_shift
5	RW	0x0	align_en_ovrd_en Enable override for rx_align_en
4	RW	0x0	align_en Override value for rx_align_en

Bit	Attr	Reset Value	Description
3	RW	0x0	cdr_ssc_en_ovrd_en Enable override value for rx_cdr_ssc_en
2	RW	0x0	cdr_ssc_en Override value for rx_cdr_ssc_en
1	RW	0x0	cdr_track_en_ovrd_en Enable override value for rx_cdr_track_en
0	RW	0x0	cdr_track_en Override value for rx_cdr_track_en

LANE0_DIG_ASIC_RX_OVRD_IN_4
Address: Operational Base + offset (0x100B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	adpt_ovrd_en Enable override for rx_adpt_dfe_en and rx_adpt_afe_en
5	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
4	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
3	RW	0x0	invert_ovrd_en Enable override for rx_invert
2	RW	0x0	invert Override value for rx_invert
1	RW	0x0	lpd_ovrd_en Enable override for rx_lpd
0	RW	0x0	lpd Override value for rx_lpd

LANE0_DIG_ASIC_RX_OVRD_IN_5
Address: Operational Base + offset (0x100C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	reset_ovrd_en Enable override for rx_reset
0	RW	0x0	reset Override value for rx_reset

LANE0_DIG_ASIC_RX_OVRD_EQ_IN_0
Address: Operational Base + offset (0x100D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x06	eq_ctle_boost Override value for rx_eq_ctle_boost
10:7	RW	0x0	reserved Reserved
6:3	RW	0xf	eq_afe_gain Override value for rx_eq_afe_gain
2:0	RW	0x0	eq_att_lvl Override value for rx_eq_att_lvl

LANE0_DIG_ASIC_RX_OVRD_EQ_IN_1

Address: Operational Base + offset (0x100E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	eq_ovrd_en Enable override value for rx_eq_* inputs
14:7	RW	0x80	eq_dfe_tap1 Override value for rx_eq_dfe_tap1
6:0	RW	0x40	eq_dfe_tap2 Override value for rx_eq_dfe_tap2

LANE0_DIG_ASIC_RX_OVRD_OUT_0

Address: Operational Base + offset (0x100F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	ana_ovl_det_0v_en Enable override for rx_ana_ovl_det_0v_i
7	RW	0x0	ana_ovl_det_0v Override value for rx_ana_ovl_det_0v_i
6	RW	0x0	adapt_sts_ovrd_en Enable override for rx_adapt_sts
5:4	RW	0x0	adapt_sts Override value for rx_adapt_sts
3	RW	0x0	rsv_0 Reserved_0
2	RW	0x0	rsv_1 Reserved_1
1	RW	0x0	ack_ovrd_en Enable override for rx_ack
0	RW	0x0	ack Override value for rx_ack

LANE0_DIG_ASIC_RX_ASIC_IN_0

Address: Operational Base + offset (0x1015)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_track_en Value from ASIC for rx_cdr_track_en
13	RO	0x0	adapt_dfe_en Value from ASIC for rx_adapt_dfe_en
12	RO	0x0	adapt_afe_en Value from ASIC for rx_adapt_afe_en
11	RO	0x0	reserved Reserved
10:9	RO	0x0	width Value from ASIC for rx_width
8:7	RO	0x0	rate_1_0 Value from ASIC for rx_rate[1:0]
6:5	RO	0x0	pstate Value from ASIC for rx_pstate

Bit	Attr	Reset Value	Description
4	RO	0x0	lpd Value from ASIC for rx_lpd
3	RO	0x0	req Value from ASIC for rx_req
2	RO	0x0	data_en Value from ASIC for rx_data_en
1	RO	0x0	invert Value from ASIC for rx_invert
0	RO	0x0	reset Value from ASIC for rx_reset

LANE0_DIG_ASIC_RX_ASIC_IN_1
Address: Operational Base + offset (0x1016)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:8	RO	0x0	rate_3_2 Value from ASIC for rx_rate[3:2]
7	RO	0x0	reserved_7 Reserved_7
6:4	RO	0x0	reserved_6_to_4 Reserved_6_to_4
3	RO	0x0	disable Value from ASIC for rx_disable
2	RO	0x0	clk_shift Value from ASIC for rx_clk_shift
1	RO	0x0	align_en Value from ASIC for rx_align_en
0	RO	0x0	cdr_ssc_en Value from ASIC for rx_cdr_ssc_en

LANE0_DIG_ASIC_RX_EQ_ASIC_IN_0
Address: Operational Base + offset (0x1017)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
10:9	RO	0x0	rx_ana_afe_rate Value from ASIC for rx_ana_afe_rate
8:7	RO	0x0	rx_ana_afe_ctle_pole Value from ASIC for rx_ana_afe_ctle_pole
6:3	RO	0x0	eq_afe_gain Value from ASIC for rx_eq_afe_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

LANE0_DIG_ASIC_RX_EQ_ASIC_IN_1
Address: Operational Base + offset (0x1018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use

Bit	Attr	Reset Value	Description
14:7	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1
6:0	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2

LANE0_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0
Address: Operational Base + offset (0x1019)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RO	0x0	rx_clk_x2_en Value from ASIC for rx_clk_x2_en[2:0]
8	RO	0x0	rx_cdr_vco_highfreq Value from ASIC for rx_cdr_vco_highfreq
7:1	RO	0x00	rx_ref_ld_val Value from ASIC for rx_ref_ld_val
0	RO	0x0	rx_cdr_vco_lowfreq Value from ASIC for rx_cdr_vco_lowfreq

LANE0_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1
Address: Operational Base + offset (0x101A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_vco_ld_val Value from ASIC for rx_vco_ld_val

LANE0_DIG_ASIC_RX_ASIC_OUT_0
Address: Operational Base + offset (0x101B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:3	RO	0x0	adapt_sts Value from PHY for rx_adapt_sts
2	RO	0x0	valid Value from PHY for rx_valid
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	ack Value from PHY for rx_ack

LANE0_DIG_LBERT_CTL
Address: Operational Base + offset (0x1020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:5	RW	0x000	pat0 Pattern for modes 3-5

Bit	Attr	Reset Value	Description
4	RW	0x0	trigger_err Insert a single error into a LSB any write of a 1 to this bit will insert an error
3:0	RW	0x0	mode Pattern to generate when changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: Fixed word (PAT0) 4'b1010: DC balanced word (PAT0, ~PAT0) 4'b1011: Fixed pattern: (000, PAT0, 3ff, ~PAT0) others: Reserved

LANE0_DIG_RX_CDR_CDR_CTL_0

Address: Operational Base + offset (0x1024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:7	RW	0x0	dtb_sel Select to drive various signals onto the dtb 4'b0000: Disabled 4'b0001: Rx_pr_stable, rx_afe_stable from rx_ana_ctl 4'b0010: Com_good, com_bad from rx_align 4'b0011: Shift_in_prog, ana_odd_data from rx_align 4'b0100: 2 MSB's of XAUI align FSM state 4'b0101: 2 LSB's of XAUI align FSM state 4'b0110: Error_high, low from lbert_pm 4'b0111: Ana_los, los_filter from los block 4'b1000: Eios_state[0], eios_det from los block 4'b1001: Cdr_valid, MSB of FSM state from cdr_ctl 4'b1010: 2 LSB's of FSM state from cdr_ctl 4'b1011: Rx_dig_rst, rx_dig_en 4'b1100: Rx_ana_word_clk_i, rx_ana_dword_clk_i 4'b1101: Lbert_pg strobe others: Reserved
6	RW	0x0	always_realign Realign on any misaligned comma
5	RW	0x0	phdet_en_pr_mode Enable partial response phase detector mode
4	RW	0x0	phdet_pol Reverse polarity of phase error

Bit	Attr	Reset Value	Description
3:2	RW	0x3	phdet_edge Edges to use for phase detection. 2'b00: Ignore all edges 2'b01: Use rising edges only 2'b10: Use both edges 2'b11: Use falling edges only
1:0	RW	0x3	phdet_en Enable phase detector. Top bit is odd slicers, bottom is even

LANE0_DIG_RX_CDR_CDR_CTL_1

Address: Operational Base + offset (0x1025)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RW	0x1c	ssc_off_cnt1 When SSC mode is disabled, the 12-bit word count in gain stage 1 is: (SSC_OFF_CNT1 * 4) in 20b mode (SSC_OFF_CNT1 * 5) in 16b mode
9:0	RW	0x039	ssc_off_cnt0 When SSC mode is disabled, the 12-bit word count in gain stage 0 is: (SSC_OFF_CNT0 * 4) in 20b mode (SSC_OFF_CNT0 * 5) in 16b mode

LANE0_DIG_RX_CDR_CDR_CTL_2

Address: Operational Base + offset (0x1026)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x25	ssc_on_cnt1 When SSC mode is enabled, the 12-bit word count in gain stage 1 is: (SSC_ON_CNT1 * 8) in 20b mode (SSC_ON_CNT1 * 10) in 16b mode
8:0	RW	0x0bb	ssc_on_cnt0 When SSC mode is enabled, the 12-bit word count in gain stage 0 is: (SSC_ON_CNT0 * 8) in 20b mode (SSC_ON_CNT0 * 10) in 16b mode

LANE0_DIG_RX_CDR_CDR_CTL_3

Address: Operational Base + offset (0x1027)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:10	RW	0x2	ssc_on_phug1 When SSC mode is enabled, the phug value in gain stage 1 is SSC_ON_PHUG1
9:6	RW	0x6	ssc_on_phug0 When SSC mode is enabled, the phug value in gain stage 0 is SSC_ON_PHUG0
5:3	RW	0x3	ssc_on_frug1 When SSC mode is enabled, the frug value in gain stage 1 is SSC_ON_FRUG1

Bit	Attr	Reset Value	Description
2:0	RW	0x3	ssc_on_frug0 When SSC mode is enabled, the frug value in gain stage 0 is SSC_ON_FRUG0

LANE0_DIG_RX_CDR_CDR_CTL_4

Address: Operational Base + offset (0x1028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:8	RW	0x0	frug_ovrd_value Override value for frug (frequency update gain) 3'b000: 0 3'b001: 1/16 LSB/update 3'b010: 1/8 LSB/update 3'b011: 1/4 LSB/update 3'b100: 1/2 LSB/update 3'b101: 1 LSB/update 3'b110: 2 LSB/update 3'b111: 4 LSB/update
7:4	RW	0x0	phug_ovrd_value Override value for phug (phase update gain) : 4'b0000: 0 4'b0001: 1000 ppm 4'b0010: 2000 ppm 4'b0011: 3000 ppm 4'b0100: 4000 ppm 4'b0101: 5000 ppm 4'b0110: 6000 ppm 4'b0111: 7000 ppm 4'b1000: 8000 ppm 4'b1001: 9000 ppm 4'b1010: 10000 ppm 4'b1011: 11000 ppm 4'b1100: 12000 ppm 4'b1101: 13000 ppm 4'b1110: 14000 ppm 4'b1111: 15000 ppm
3	RW	0x0	ovrd_dpll_gain Override phug and frug values
2:0	RW	0x3	ssc_off_frug0 When SSC mode is disabled, the frug value in gain stage 0 is SSC_OFF_FRUG0

LANE0_DIG_RX_CDR_CDR_CTL_5

Address: Operational Base + offset (0x1029)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs3_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS3_FRUG1

Bit	Attr	Reset Value	Description
8:6	RW	0x1	ssc_off_lbrs2_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS2_FRUG1
5:3	RW	0x1	ssc_off_lbrs1_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS1_FRUG1
2:0	RW	0x1	ssc_off_lbrs0_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS0_FRUG1

LANE0_DIG_RX_CDR_CDR_CTL_6

Address: Operational Base + offset (0x102A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs7_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS7_FRUG1
8:6	RW	0x3	ssc_off_lbrs6_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS6_FRUG1
5:3	RW	0x3	ssc_off_lbrs5_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS5_FRUG1
2:0	RW	0x3	ssc_off_lbrs4_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS4_FRUG1

LANE0_DIG_RX_CDR_CDR_CTL_7

Address: Operational Base + offset (0x102B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x8	ssc_off_lbrs3_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS3_PHUG0
11:8	RW	0x7	ssc_off_lbrs2_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS2_PHUG0
7:4	RW	0x6	ssc_off_lbrs1_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS1_PHUG0
3:0	RW	0x6	ssc_off_lbrs0_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS0_PHUG0

LANE0_DIG_RX_CDR_CDR_CTL_8

Address: Operational Base + offset (0x102C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS7_PHUG0

Bit	Attr	Reset Value	Description
11:8	RW	0xc	ssc_off_lbrs6_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS6_PHUG0
7:4	RW	0xc	ssc_off_lbrs5_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS5_PHUG0
3:0	RW	0xa	ssc_off_lbrs4_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS4_PHUG0

LANE0_DIG_RX_CDR_CDR_CTL_9
Address: Operational Base + offset (0x102D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x6	ssc_off_lbrs3_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS3_PHUG1
11:8	RW	0x4	ssc_off_lbrs2_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS2_PHUG1
7:4	RW	0x3	ssc_off_lbrs1_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS1_PHUG1
3:0	RW	0x2	ssc_off_lbrs0_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS0_PHUG1

LANE0_DIG_RX_CDR_CDR_CTL_10
Address: Operational Base + offset (0x102E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS7_PHUG1
11:8	RW	0xc	ssc_off_lbrs6_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS6_PHUG1
7:4	RW	0xa	ssc_off_lbrs5_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS5_PHUG1
3:0	RW	0x8	ssc_off_lbrs4_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS4_PHUG1

LANE0_DIG_RX_CDR_STAT
Address: Operational Base + offset (0x102F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:4	RO	0x0	frug_value Notes: Current value for dpll_frug[2:0]
3:0	RO	0x0	phug_value Notes: Current value for dpll_phug[3:0]

LANE0_DIG_RX_PWRCTL_RX_PSTATE_P0

Address: Operational Base + offset (0x1040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	rx_p0_dig_clk_en Enable/Disable RX digital clocks in P0
10	RW	0x1	rx_p0_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0, if RX_P0_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0_vco_cal_rst Enable/Disable resetting the RX VCO in P0
8	RW	0x0	rx_p0_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0
7	RW	0x1	rx_p0_ana_cdr_en Value of RX ana cdr_en in P0
6	RW	0x1	rx_p0_ana_deser_en Value of RX ana deserial_en in P0
5	RW	0x1	rx_p0_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0
4	RW	0x1	rx_p0_ana_clk_en Value of RX ana clk_en in P0
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0
1	RW	0x1	rx_p0_ana_afe_en Value of RX ana afe_en in P0
0	RW	0x1	reserved_0 Reserved_0

LANE0_DIG_RX_PWRCTL_RX_PSTATE_P0S

Address: Operational Base + offset (0x1041)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p0s_dig_clk_en Enable/Disable RX digital clocks in P0S
10	RW	0x1	rx_p0s_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0S, if RX_P0S_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0s_vco_cal_rst Enable/Disable resetting the RX VCO in P0S
8	RW	0x0	rx_p0s_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0S
7	RW	0x0	rx_p0s_ana_cdr_en Value of RX ana cdr_en in P0S

Bit	Attr	Reset Value	Description
6	RW	0x0	rx_p0s_ana_deser_en Value of RX ana deserial_en in P0S
5	RW	0x0	rx_p0s_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0S
4	RW	0x0	rx_p0s_ana_clk_en Value of RX ana clk_en in P0S
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0s_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0S
1	RW	0x1	rx_p0s_ana_afe_en Value of RX ana afe_en in P0S
0	RW	0x1	reserved_0 Reserved_0

LANE0_DIG_RX_PWRCTL_RX_PSTATE_P1

Address: Operational Base + offset (0x1042)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p1_dig_clk_en Enable/Disable RX digital clocks in P1
10	RW	0x0	rx_p1_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P1, if RX_P1_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p1_vco_cal_rst Enable/Disable resetting the RX VCO in P1
8	RW	0x1	rx_p1_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P1
7	RW	0x0	rx_p1_ana_cdr_en Value of RX ana cdr_en in P1
6	RW	0x0	rx_p1_ana_deser_en Value of RX ana deserial_en in P1
5	RW	0x0	rx_p1_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P1
4	RW	0x0	rx_p1_ana_clk_en Value of RX ana clk_en in P1
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p1_ana_clk_vreg_en Value of RX ana clk_vreg_en in P1
1	RW	0x1	rx_p1_ana_afe_en Value of RX ana afe_en in P1
0	RW	0x1	reserved_0 Reserved_0

LANE0_DIG_RX_PWRCTL_RX_PSTATE_P2

Address: Operational Base + offset (0x1043)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p2_dig_clk_en Enable/Disable RX digital clocks in P2
10	RW	0x0	rx_p2_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P2, if RX_P2_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p2_vco_cal_rst Enable/Disable resetting the RX VCO in P2
8	RW	0x1	rx_p2_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P2
7	RW	0x0	rx_p2_ana_cdr_en Value of RX ana cdr_en in P2
6	RW	0x0	rx_p2_ana_deser_en Value of RX ana deserial_en in P2
5	RW	0x0	rx_p2_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P2
4	RW	0x0	rx_p2_ana_clk_en Value of RX ana clk_en in P2
3	RW	0x0	reserved
2	RW	0x0	rx_p2_ana_clk_vreg_en Value of RX ana clk_vreg_en in P2
1	RW	0x0	rx_p2_ana_afe_en Value of RX ana afe_en in P2
0	RW	0x1	reserved_0 Reserved_0

LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_0

Address: Operational Base + offset (0x1044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x0f	rx_dpll_clock_switch_time Wait between switching rx_dpll clock from rx_clk to ref_clk or vice-versa
4:0	RW	0x06	rx_state_3a_and_3b_time Wait between Power state 3A and 3B

LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_1

Address: Operational Base + offset (0x1045)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	fast_rx_vreg_en Enable fast RX VREG enable (simulation only)
12:7	RW	0x0d	rx_vreg_en_time Power up time (in ref_range cycles) for RX ana vreg enable (spec 500ns)
6	RW	0x0	fast_rx_afe_en Enable fast RX AFE enable (simulation only)

Bit	Attr	Reset Value	Description
5:0	RW	0x1a	rx_afe_en_time Power up time (in ref_range cycles) for RX ana AFE enable (spec >=1us)

LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_2

Address: Operational Base + offset (0x1046)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	fast_rx_clk_en Enable fast RX clock enable (simulation only)
5:0	RW	0x1a	rx_clk_en_time Power up time (in ref_range cycles) for RX ana clk (or dcc) enable (spec >1us)

LANE0_DIG_RX_PWRCTL_RX_PWRUP_TIME_3

Address: Operational Base + offset (0x1047)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	rx_deser_dis_time Power down time in (ref_range cycles) for RX ana deserializer enable
13:12	RW	0x0	rx_deser_en_time Power up time (in ref_range cycles) for RX ana deserializer enable
11:8	RW	0x0	rx_cdr_en_time Power up time (in ref_range cycles) for RX ana CDR (or dfe/dfe_taps) enable (spec 0ns)
7:2	RW	0x00	rsvd_3_7_2 Reserved
1:0	RW	0x0	rx_rate_time Power up time (in ref_range cycles) for RX ana rate or width change

LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0

Address: Operational Base + offset (0x1048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RW	0x0	vcoclk_correct_update Update the vcoclk_correct
11:9	RW	0x2	int_gain_cal_bounce_cnt Number of bounces (i.e. direction changes) on the int_gain code before indicating that the RX VCO calibration is done
8:6	RW	0x0	int_gain_cal_cnt_shift Number of shifts to apply to ld_cnt inputs when performing int_gain code calibration
5	RW	0x0	int_gain_cal_fixed_cnt_en Enable a fixed count (instead of bounce count) for int_gain code calibration

Bit	Attr	Reset Value	Description
4:0	RW	0x00	int_gain_cal_fixed_cnt Number of steps done during int_gain code calibration when INT_GAIN_CAL_FIXED_CNT_EN is enabled.

LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1

Address: Operational Base + offset (0x1049)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x00	dtb_sel DTB select for RX VCO dtb signals 7'h01: {chkfrq_en, ref_dig_clk} 7'h02: {rx_ana_cdr_vco_en_i, rx_ana_cdr_startup_i} 7'h04: {rx_vco_up, dpll_freq_rst} 7'h08: {rx_vco_contcal_en, rx_vco_cal_rst} 7'h10: {chkfrq_done, vcoclk_too_fast} 7'h20: {cal_dir, rx_vco_cal_done} 7'h40: {curr_state[0], rx_vco_cnt[0]} others: Reserved
8:5	RW	0x8	dpll_cal_ug DPLL calibration update on int_gain code 4'h0: 0 others: (1/16)*2^(DPLL_CAL_UG-1) LSB/update Maximum DPLL_CAL_UG=10, that is 32 LSB/update
4	RW	0x0	disable_int_cal_mode When asserted, then the DPLL frequency register is never modified by the RX VCO calibration FSM (even, if DPLL_CAL_UG is non-zero). In this case, the calibration will always be performed on the VCO freq_tune code. This allows disabling of integral calibration feature, and hence only using freq_tune calibration.
3	RW	0x0	rx_vco_contcal_en Override value for the continuous calibration enable from the RX PWRSM
2	RW	0x0	rx_vco_cal_rst Override value for the calibration reset from the RX PWRSM
1	RW	0x0	rx_vco_freq_rst Override value for the frequency reset from the RX PWRSM
0	RW	0x0	rx_vco_ovrd_sel Override the calibration controls from the RX PWRSM

LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2

Address: Operational Base + offset (0x104A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_rx_vco_cal Skip RX VCO calibration altogether
14	RW	0x0	skip_rx_vco_freq_tune_cal Skip RX VCO coarse calibration
13:10	RW	0x9	freq_tune_cal_steps Number of cal steps of freq tune
9:0	RW	0x200	freq_tune_start_val Starting value of freq tune code

LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0

Address: Operational Base + offset (0x104B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	fast_rx_vco_wait Enable fast RX VCO power up (simulation only)
14:11	RW	0x6	rx_vco_cntr_pwrup_time Power up time (in ref_range cycles) for RX ana VCO cnter (spec >200ns)
10:7	RW	0x6	rx_vco_update_time Settle time (in ref_range cycles) for RX ana VCO update (freq_tune or int_gain) (spec >200ns)
6:0	RW	0x19	rx_vco_startup_time Power up time (in ref_range cycles) for RX ana VCO startup (spec >1us)

LANE0_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1
Address: Operational Base + offset (0x104C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2:0	RW	0x3	rx_vco_cntr_settle_time RX VCO counter value settling time in (ref_dig_clk cycles) (spec: 3 ref_dig_clk cycle)

LANE0_DIG_RX_VCOCAL_RX_VCO_STAT_0
Address: Operational Base + offset (0x104D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	rx_ana_cdr_vco_en Current value of rx_ana_cdr_vco_en_i
12	RO	0x0	rx_ana_cdr_startup Current value of rx_ana_cdr_startup_i
11	RO	0x0	rx_ana_vco_cntr_en Current value of rx_ana_vco_cntr_en_i
10	RO	0x0	rx_ana_vco_cntr_pd Current value of rx_ana_vco_cntr_pd_i
9:0	RO	0x000	rx_ana_cdr_freq_tune Current value of rx_ana_cdr_freq_tune_i

LANE0_DIG_RX_VCOCAL_RX_VCO_STAT_1
Address: Operational Base + offset (0x104E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	dpll_freq_rst Indicates that the RX integral frequency is reset or not
7	RO	0x0	rx_vco_cal_done Indicates that the RX VCO has completed calibration
6	RO	0x0	rx_vco_contcal_en Value of the continuous calibration enable from the RX PWRSM
5	RO	0x0	rx_vco_cal_rst Value of the calibration reset from the RX PWRSM

Bit	Attr	Reset Value	Description
4	RO	0x0	rx_vco_freq_rst Value of the RX VCO frequency reset from the RX PWRSM
3:0	RO	0x0	rx_vco_fsm_state Value of the RX VCO CAL FSM

LANE0_DIG_RX_VCOCAL_RX_VCO_STAT_2
Address: Operational Base + offset (0x104F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	rx_vco_up Indicates that the RX VCO is ready
14	RO	0x0	rx_vco_correct Indicates that the RX VCO clock has the correct frequency
13	RO	0x0	vcoclk_too_fast Indicates that the RX VCO clock frequency is too fast
12:0	RO	0x0000	vco_cntr_final Value of RX VCO counter when refclk counter expired

LANE0_DIG_RX_RX_ALIGN_XAUI_COMM_MASK
Address: Operational Base + offset (0x1050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x3ff	xaui_comm_mask XAUI_COMMA mask. For 10-bit COMMA set the mask to 0x3FF and for 7-bit COMMA set the mask to 0x3F8

LANE0_DIG_RX_LBERT_CTL
Address: Operational Base + offset (0x1051)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	sync Synchronize pattern matcher LFSR with incoming data A write of a one to this bit will reset the error counter and start a synchronization of the PM, there is no need to write this back to zero to run normally.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	mode Pattern to match When changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: D[n] = d[n-10] 4'b1010: D[n] = !d[n-10] 4'b1011: D[n] = !d[n-20] others: Reserved

LANE0_DIG_RX_LBERT_ERR
Address: Operational Base + offset (0x1052)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ov14 If active, multiply count by 128. if OV14=1 and count=2^15-1, signals overflow of counter (2 reads needed to read value)
14:0	RW	0x0000	count A read of this register, or a sync of the PM resets the error count. Current error count, if OV14 field is active, then multiply count by 128 (2 reads needed to read value)

LANE0_DIG_RX_RX_LOS_LOS_0
Address: Operational Base + offset (0x1053)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	rx_los_filt_byp Bypass digital LOS filter
7:3	RW	0x0c	rx_los_t_thresh0_r LOS timer0 threshold to count presence of zeros on rx_los
2:0	RW	0x2	rx_los_wait_r Initial wait time for rx_los after rx_los_en is asserted

LANE0_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS
Address: Operational Base + offset (0x1055)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_pwrsm_state Value for rx_pwrsm_state

LANE0_DIG_RX_DPLL_FREQ
Address: Operational Base + offset (0x105C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:0	RW	0x2000	val Freq is 125*VAL ppm from the reference (2 reads needed to read value)

LANE0_DIG_RX_DPLL_FREQ_BOUND_0
Address: Operational Base + offset (0x105D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:1	RW	0x264	upper_freq_bound Upper frequency bound in terms of LSBs of the integral control code
0	RW	0x0	freq_bound_en Enable the frequency bounds feature

LANE0_DIG_RX_DPLL_FREQ_BOUND_1
Address: Operational Base + offset (0x105E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x19c	lower_freq_bound Lower frequency bound in terms of LSBs of the integral control code

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_0
Address: Operational Base + offset (0x1060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	adpt_clk_div4_en Set the adaptation clock to be divided by 4 (default is div2)
14	RW	0x0	start_asm1 Start adaptation state machine #1 (VGA, CTLE, DFE, EYEH) This register-bit is self-clearing
13:10	RW	0x3	n_tgg_asm1 Number of toggle loop iterations for ASM1
9:0	RW	0x010	n_top_asm1 Number of top level loop iterations for ASM1

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_1
Address: Operational Base + offset (0x1061)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	ctle_pole_ovrd_en Override CTLE pole value (only valid, if adaptation is run)
10:8	RW	0x0	ctle_pole_ovrd_val CTLE pole override value to load at start of adaptation

Bit	Attr	Reset Value	Description
7	RW	0x0	fast_afe_dfe_settle Enable fast AFE and DFE settling time (simulation only)
6:0	RW	0x09	n_wait_asm1 Number of wait cycles for adaptation SM #1

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_2

Address: Operational Base + offset (0x1062)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x06	tgg_pttrn_1 Pattern for the second toggle loop error slicer is moved upward by data tap1, if this pattern is matched
4:0	RW	0x02	tgg_pttrn_0 Pattern for the first toggle loop error slicer is moved downward by data tap1, if this pattern is matched

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_3

Address: Operational Base + offset (0x1063)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	esl_twice_dsl Assert, if error slicer has twice the voltage range as the data slicer (for the same 8 bits).
14	RW	0x0	tgg_en Enable toggling of the error slicer
13	RW	0x0	eyeho_en Enable eye height measurement using odd error slicer
12	RW	0x0	eyehe_en Enable eye height measurement using even error slicer
11:7	RW	0x00	dfe_en Enable DFE adaptation for taps 5-1
6	RW	0x0	att_en Enable ATT adaptation
5	RW	0x0	vga_en Enable VGA adaptation
4:0	RW	0x00	ctle_en Enable CTLE boost adaptation, the five bits determine which correlators are used to adapt the CTLE

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_4

Address: Operational Base + offset (0x1064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	dfe2_th DFE Tap2 correlation decision threshold (2^N-1)
11:8	RW	0x0	dfe1_th DFE Tap1 correlation decision threshold (2^N-1)
7:4	RW	0x0	vga_th VGA correlation decision threshold (2^N-1), During eye height measurement, the VGA_TH is repurposed for error slicer updates.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	ctle_th CTLE correlation decision threshold (2^N-1)

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_5
Address: Operational Base + offset (0x1065)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	th_offset Apply an offset to the decision threshold
11:8	RW	0x0	dfe5_th DFE Tap5 correlation decision threshold (2^N-1)
7:4	RW	0x0	dfe4_th DFE Tap4 correlation decision threshold (2^N-1)
3:0	RW	0x0	dfe3_th DFE Tap3 correlation decision threshold (2^N-1)

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_6
Address: Operational Base + offset (0x1066)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RW	0x3	att_low_th ATT low threshold
12	RW	0x1	vga_sat_cnt_sticky If deasserted, then VGA saturation counts must be consecutive to change ATT
11:9	RW	0x4	vga_sat_cnt VGA saturation count
8:6	RW	0x4	att_mu ATT gain code update gain (2^N)
5:3	RW	0x5	vga_mu VGA gain code update gain (2^N). During eye height measurement, the VGA_MU is repurposed for error slicer updates.
2:0	RW	0x3	ctle_mu CTLE boost code update gain (2^N)

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_7
Address: Operational Base + offset (0x1067)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x10	vga_lev_low VGA level low saturation limit
9:5	RW	0x1a	vga_lev_high VGA level high saturation limit
4:0	RW	0x02	vga_min_sat VGA minimum saturation limit

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_8
Address: Operational Base + offset (0x1068)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x4	dfe5_mu DFE tap5 code update gain (2^N)
11:9	RW	0x4	dfe4_mu DFE tap4 code update gain (2^N)
8:6	RW	0x4	dfe3_mu DFE tap3 code update gain (2^N)
5:3	RW	0x4	dfe2_mu DFE tap2 code update gain (2^N)
2:0	RW	0x5	dfe1_mu DFE tap1 code update gain (2^N)

LANE0_DIG_RX_ADPTCTL_ADPT_CFG_9

Address: Operational Base + offset (0x1069)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	err_slo_adpt_init The error odd slicer is initialized to this value at the start of a new adaptation request.
7:0	RW	0x00	err_sle_adpt_init The error even slicer is initialized to this value at the start of a new adaptation request.

LANE0_DIG_RX_ADPTCTL_RST_ADPT_CFG

Address: Operational Base + offset (0x106A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x1	rst_adpt_tap1 Reset data Tap1 when turning off DFE adaptation (taps 2-5 are always turned off when DFE adaptation is turned off)
3	RW	0x1	rst_adpt_ctle_pole Reset CTLE pole when turning off AFE adaptation
2	RW	0x1	rst_adpt_ctle_boost Reset CTLE boost when turning off AFE adaptation
1	RW	0x1	rst_adpt_vga Reset VGA when turning off AFE adaptation
0	RW	0x1	rst_adpt_att Reset ATT when turning off AFE adaptation

LANE0_DIG_RX_ADPTCTL_ATT_STATUS

Address: Operational Base + offset (0x106B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	asm1_don Asserts when adaptation state machine #1 is done
7:0	RO	0x00	att_adpt_code Value of ATT adaptation code

LANE0_DIG_RX_ADPTCTL_VGA_STATUS

Address: Operational Base + offset (0x106C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
9:0	RO	0x000	vga_adpt_code Value of VGA adaptation code

LANE0_DIG_RX_ADPTCTL_CTLE_STATUS

Address: Operational Base + offset (0x106D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:10	RO	0x0	ctle_pole_adpt_code Value of CTLE pole adaptation code
9:0	RO	0x000	ctle_boost_adpt_code Value of CTLE boost adaptation code

LANE0_DIG_RX_ADPTCTL_DFE_TAP1_STATUS

Address: Operational Base + offset (0x106E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:0	RO	0x0000	dfe_tap1_adpt_code Value of DFE tap1 adaptation code

LANE0_DIG_RX_ADPTCTL_DFE_TAP2_STATUS

Address: Operational Base + offset (0x106F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap2_adpt_code Value of DFE tap2 adaptation code

LANE0_DIG_RX_ADPTCTL_DFE_TAP3_STATUS

Address: Operational Base + offset (0x1070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap3_adpt_code Value of DFE tap3 adaptation code

LANE0_DIG_RX_ADPTCTL_DFE_TAP4_STATUS

Address: Operational Base + offset (0x1071)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap4_adpt_code Value of DFE tap4 adaptation code

LANE0_DIG_RX_ADPTCTL_DFE_TAP5_STATUS

Address: Operational Base + offset (0x1072)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap5_adpt_code Value of DFE tap5 adaptation code

LANE0_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1073)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_vdac_ofst Offset value for DFE data even vDAC

LANE0_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST

Address: Operational Base + offset (0x1074)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_vdac_ofst Offset value for DFE data odd vDAC

LANE0_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN

Address: Operational Base + offset (0x1075)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE0_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD

Address: Operational Base + offset (0x1076)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

LANE0_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1077)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

LANE0_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST

Address: Operational Base + offset (0x1078)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

LANE0_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL

Address: Operational Base + offset (0x1079)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	e_sle_lvl Even error slicer level
7:0	RO	0x00	e_slo_lvl Odd error slicer level

LANE0_DIG_RX_ADPTCTL_ADPT_RESET

Address: Operational Base + offset (0x107A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	reset_asm1 Resets adaptation state machine (ASM1) as well as the stats capture block. This is a self-clearing bit, and requires re-start of ASM1.

LANE0_DIG_RX_STAT_LD_VAL_1

Address: Operational Base + offset (0x1080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sc1_start Start sample counter #1 this is a self-clearing bit
14:0	RW	0x0040	sc1_ld_val Sample counter #1 load value

LANE0_DIG_RX_STAT_DATA_MSK

Address: Operational Base + offset (0x1081)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	data_msk_15_0 Value of data_msk_r[15:0]

LANE0_DIG_RX_STAT_MATCH_CTL0

Address: Operational Base + offset (0x1082)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	scope_dly For clock cycle delays on scope_data_rx_clk, an additional MSB is added in SCOPE_DLY_2
13:10	RW	0xf	data_msk_19_16 Value of data_msk_r[19:16]
9:5	RW	0x00	pttrn_cr1a_4_0 Value of pattern A for 1st correlator (bits 4:0)
4:0	RW	0x06	pttrn_msk_cr1a_4_0 Value of pattern A mask for 1st correlator (bits 4:0)

LANE0_DIG_RX_STAT_MATCH_CTL1

Address: Operational Base + offset (0x1083)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	pttrn_cr1a_adpt_en Enable ORing of adaptation pattern with pattern CR1A
10:6	RW	0x00	pttrn_cr1b_4_0 Value of pattern B for 1st correlator (bits 4:0)
5:1	RW	0x00	pttrn_msk_cr1b_4_0 Value of pattern B mask for 1st correlator (bits 4:0)
0	RW	0x0	pttrn_cr1b_en Enable pattern B matching for 1st correlator

LANE0_DIG_RX_STAT_STAT_CTL0

Address: Operational Base + offset (0x1084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_en Value of skip_en_r
14	RW	0x1	sc_timer_mode Sample counter operation mode 1'b0: Counts number of matched samples 1'b1: Counts clock cycles (i.e. a timer)
13	RW	0x0	stat_rxclk_sel Select stat clock 1'b0: Ref_range_clk 1'b1: Rx_dig_clk (i.e. RX dword clk) Before changing stat_rxclk_sel_r from 1->0, the rx_dig_clk must be active (i.e. enabled)

Bit	Attr	Reset Value	Description
12:10	RW	0x0	stat_src_sel Select stat source input 3'b000: {20{rx_cal_result}} 3'b001: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 3'b010: Rx_phase[39:0] 3'b011: Rx_error[39:0] 3'b100: Rx_data[39:0] 3'b101: Rx_phdir[39:0] 3'b110: 40'hFF_FFFF_FFFF
9:6	RW	0x0	stat_shft_sel Select stat source shift value 4'b0000: Correlate N-1 -> N+3 (use N for offset calibration) 4'b0001: Correlate N+1 -> N+5 (for taps1-5) 4'b0010: Correlate N+6 -> N+10 4'b0011: Correlate N+11 -> N+15 4'b0100: Correlate N+16 -> N+20 4'b0101: Correlate N+21 -> N+25 4'b0110: Correlate N+26 -> N+30 4'b0111: Correlate N+31 -> N+35 4'b1000: Correlate N+36 -> N+39 others: Reserved Setting 0x8 is only used in 20b mode (for checking corr on bits 36-39)
5	RW	0x0	corr_mode_en Enable correlation mode
4:3	RW	0x0	corr_src_sel Select correlation input source 2'b00: Rx_error[39:0] 2'b01: Rx_phase[39:0] 2'b10: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 2'b11: No correlation
2	RW	0x0	corr_shft_sel Select shift for phase. 1'b0: None, 1'b1: >>1
1	RW	0x0	corr_shft_sel_vga Select shift for error going to VGA. 1'b0: None 1'b1: >>1
0	RW	0x0	reserved_0 Reserved bit

LANE0_DIG_RX_STAT_STAT_CTL1

Address: Operational Base + offset (0x1085)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	vld_ctl Gating configuration of stats collection 2'b00: Ignore both cdr_valid and rx_valid 2'b01: Gate stats collection with cdr_valid 2'b10: Gate stats collection with rx_valid 2'b11: Ignore both cdr_valid and rx_valid

Bit	Attr	Reset Value	Description
13	RW	0x0	vld_loss_clr Clearing of stats collection upon loss of valid 1'b0: Hold sample and stat counters 1'b1: Clear sample and stat counters
12:11	RW	0x0	data_dly_sel For clock cycle delays on rx_data[19:0], an additional MSB is added in data_dly_sel_2
10	RW	0x0	stat_clk_en Clock gate enable for stat clock
9	RW	0x0	sc_pause Pause the sample counter and stat counters
8:7	RW	0x0	reserved_8_7 Reserved bits
6	RW	0x0	stat_cnt_6_en Enable for stat counter 6
5	RW	0x0	stat_cnt_5_en Enable for stat counter 5
4	RW	0x0	stat_cnt_4_en Enable for stat counter 4
3	RW	0x1	stat_cnt_3_en Enable for stat counter 3 only counter to be enabled by default, since used for offset calibration
2	RW	0x0	stat_cnt_2_en Enable for stat counter 2
1	RW	0x0	stat_cnt_1_en Enable for stat counter 1
0	RW	0x0	stat_cnt_0_en Enable for stat counter 0

LANE0_DIG_RX_STAT_SMPL_CNT1
Address: Operational Base + offset (0x1086)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter
14:0	RO	0x0000	smpl_cnt1 Current value of sample counter

LANE0_DIG_RX_STAT_STAT_CNT_0
Address: Operational Base + offset (0x1087)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter
14:0	RO	0x0000	stat_cnt_0 Current value of stat counter

LANE0_DIG_RX_STAT_STAT_CNT_1
Address: Operational Base + offset (0x1088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter

Bit	Attr	Reset Value	Description
14:0	RO	0x0000	stat_cnt_1 Current value of stat counter

LANE0_DIG_RX_STAT_STAT_CNT_2
Address: Operational Base + offset (0x1089)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter
14:0	RO	0x0000	stat_cnt_2 Current value of stat counter

LANE0_DIG_RX_STAT_STAT_CNT_3
Address: Operational Base + offset (0x108A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter
14:0	RO	0x0000	stat_cnt_3 Current value of stat counter

LANE0_DIG_RX_STAT_STAT_CNT_4
Address: Operational Base + offset (0x108B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter
14:0	RO	0x0000	stat_cnt_4 Current value of stat counter

LANE0_DIG_RX_STAT_STAT_CNT_5
Address: Operational Base + offset (0x108C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter
14:0	RO	0x0000	stat_cnt_5 Current value of stat counter

LANE0_DIG_RX_STAT_STAT_CNT_6
Address: Operational Base + offset (0x108D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter
14:0	RO	0x0000	stat_cnt_6 Current value of stat counter

LANE0_DIG_RX_STAT_CAL_COMP_CLK_CTL
Address: Operational Base + offset (0x108E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use

Bit	Attr	Reset Value	Description
5:3	RW	0x3	ref_div_cnt Ref range clock count (e.g. 5'd3 = 4 ref_range cycles)
2:0	RW	0x1	prechrge_cnt Precharge count (e.g. 5'd1 = 2 ref_range cycles)

LANE0_DIG_RX_STAT_MATCH_CTL2

Address: Operational Base + offset (0x108F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1a_19_5 Value of pattern A for 1st correlator (bits 19:5)

LANE0_DIG_RX_STAT_MATCH_CTL3

Address: Operational Base + offset (0x1090)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1a_19_5 Value of pattern A mask for 1st correlator (bits 19:5)

LANE0_DIG_RX_STAT_MATCH_CTL4

Address: Operational Base + offset (0x1091)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1b_19_5 Value of pattern B for 1st correlator (bits 19:5)

LANE0_DIG_RX_STAT_MATCH_CTL5

Address: Operational Base + offset (0x1092)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1b_19_5 Value of pattern B mask for 1st correlator (bits 19:5)

LANE0_DIG_RX_STAT_STAT_CTL2

Address: Operational Base + offset (0x1093)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	scope_dly_2 Additional MSB bit for SCOPE_DLY to extend the delay range to 0->7
0	RW	0x0	data_dly_sel_2 Additional MSB bit for data_dly_sel to extend the delay range to 0->7

LANE0_DIG_RX_STAT_STAT_STOP
Address: Operational Base + offset (0x1094)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	sc1_stop Stop sample counters #1 and associated stat counters. This is a self-clearing bit, and requires re-start of sample counter #1.

LANE0_DIG_ANA_TX_OVRD_OUT
Address: Operational Base + offset (0x10A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	tx_ovrd_en Enable override values for all outputs controlled by this register
0	RW	0x0	tx_ana_reset Override value for tx_ana_reset

LANE0_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT
Address: Operational Base + offset (0x10A1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	tx_ana_lpbk_dfe_mode Value for tx_ana_lpbk_dfe_mode

LANE0_DIG_ANA_RX_DIV_OVRD_OUT
Address: Operational Base + offset (0x10A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_ana_div5_en Override value for rx_ana_div5_en
0	RW	0x0	rx_ana_div13p5_en Override value for rx_ana_div13p5_en

LANE0_DIG_ANA_RX_CTL_OVRD_OUT
Address: Operational Base + offset (0x10A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_lbk_clk_en_ovrd Enable override value for rx_ana_loopback_clk_en
14	RW	0x0	rx_ana_adaptation_en_ovrd Enable override value for rx_ana_adaptation_en
13	RW	0x0	rx_ana_dfe_taps_en_ovrd Enable override value for rx_ana_dfe_taps_en
12	RW	0x0	rx_ana_div4_en_ovrd Enable override value for rx_ana_div4_en
11	RW	0x0	rx_ana_word_clk_en_ovrd Enable override value for rx_ana_word_clk_en

Bit	Attr	Reset Value	Description
10	RW	0x0	rx_ana_data_rate_en_ovrd Enable override values for rx_ana_data_rate[3:0]
9	RW	0x0	rx_lbk_clk_en Override value for rx_ana_loopback_clk_en
8	RW	0x0	rx_ana_adaptation_en Override value for rx_ana_adaptation_en
7	RW	0x0	rx_ana_dfe_taps_en Override value for rx_ana_dfe_taps_en
6	RW	0x0	rx_ana_div4_en Override value for rx_ana_div4_en
5	RW	0x0	rx_ana_word_clk_en Override value for rx_ana_word_clk_en
4:1	RW	0x0	rx_ana_data_rate Override value for rx_ana_data_rate
0	RW	0x0	reserved Reserved

LANE0_DIG_ANA_RX_PWR_OVRD_OUT
Address: Operational Base + offset (0x10A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_ana_deserial_en_ovrd Enable override value for rx_ana_deserial_en
12	RW	0x0	rx_ana_cdr_en_ovrd Enable override value for rx_ana_cdr_en
11	RW	0x0	rx_ana_clk_en_ovrd Enable override value for rx_ana_clk_en
10	RW	0x0	rx_ana_clk_dcc_en_ovrd Enable override value for rx_ana_clk_dcc_en
9	RW	0x0	rx_ana_clk_vreg_en_ovrd Enable override value for rx_ana_clk_vreg_en
8	RW	0x0	rx_ana_afe_en_ovrd Enable override value for rx_ana_afe_en
7	RW	0x0	Reserve_0 Reserve_0
6	RW	0x0	rx_ana_deserial_en Override value for rx_ana_deserial_en
5	RW	0x0	rx_ana_cdr_en Override value for rx_ana_cdr_en
4	RW	0x0	rx_ana_clk_en Override value for rx_ana_clk_en
3	RW	0x0	rx_ana_clk_dcc_en Override value for rx_ana_clk_dcc_en
2	RW	0x0	rx_ana_clk_vreg_en Override value for rx_ana_clk_vreg_en
1	RW	0x0	rx_ana_afe_en Override value for rx_ana_afe_en
0	RW	0x0	Reserve_1 Reserve_1

LANE0_DIG_ANA_RX_VCO_OVRD_OUT_0
Address: Operational Base + offset (0x10A9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_cdr_freq_tune_ovrd_en Enable override value for rx_ana_cdr_freq_tune
14	RW	0x0	rx_ana_vco_cntr_clk Override value for rx_ana_vco_cntr_clk
13	RW	0x0	rx_ana_vco_cntr_en Override value for rx_ana_vco_cntr_en
12:3	RW	0x000	rx_ana_cdr_freq_tune Override value for rx_ana_cdr_freq_tune
2	RW	0x0	rx_vco_cdr_ovrd_en Enable override values for cdr_vco_en and cdr_startup
1	RW	0x0	rx_ana_cdr_startup Override value for rx_ana_cdr_startup
0	RW	0x0	rx_ana_cdr_vco_en Override value for rx_ana_cdr_vco_en

LANE0_DIG_ANA_RX_VCO_OVRD_OUT_1
Address: Operational Base + offset (0x10AA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_cdr_vco_highfreq Override value for rx_ana_cdr_vco_highfreq
1	RW	0x1	rx_ana_vco_cntr_pd Override value for rx_ana_vco_cntr_pd
0	RW	0x0	rx_ana_cdr_vco_lowfreq Override value for rx_ana_cdr_vco_lowfreq

LANE0_DIG_ANA_RX_VCO_OVRD_OUT_2
Address: Operational Base + offset (0x10AB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	cdr_freq_tune_clk_self_clear_disable Disable self-clearing for the rx_ana_cdr_freq_tune_clk register
0	RW	0x0	rx_ana_cdr_freq_tune_clk Override value for rx_ana_cdr_freq_tune_clk - self-clearing to generate a pulse 1 cr_clk wide

LANE0_DIG_ANA_RX_CAL
Address: Operational Base + offset (0x10AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_ana_cal_comp_en Value for rx_ana_cal_comp_en

Bit	Attr	Reset Value	Description
14:13	RW	0x0	rx_ana_cal_mode Value for rx_ana_cal_mode[1:0] 2'b00: Dual differential comparison ([vip2 - vim2] greater than [vip1 - vim1]) 2'b01: Differential comparison on input2 (vip2 greater than vim2) 2'b10: Single-ended comparison, negative node to negative node (vim1 greater than vim2) 2'b11: Common mode comparison (vcm2 greater than vcm1)
12	RW	0x0	rx_ana_slicer_cal_en Value for rx_ana_slicer_cal_en
11	RW	0x0	reserved Reserved
10	RW	0x0	rx_ana_cal_lpfbyp_en Value for rx_ana_cal_lpfbyp_en
9:5	RW	0x00	rx_ana_cal_muxb_sel Value for rx_ana_cal_muxb_sel[4:0]
4:0	RW	0x00	rx_ana_cal_muxa_sel Value for rx_ana_cal_muxa_sel[4:0]

LANE0_DIG_ANA_RX_DAC_CTRL
Address: Operational Base + offset (0x10AD)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	rx_ana_cal_dac_ctrl Value for rx_ana_cal_dac_ctrl[7:0]

LANE0_DIG_ANA_RX_DAC_CTRL_OVRD
Address: Operational Base + offset (0x10AE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_cal_dac_ctrl_ovrd Override enable for cal DAC control

LANE0_DIG_ANA_RX_DAC_CTRL_SEL
Address: Operational Base + offset (0x10AF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_ana_cal_dac_ctrl_sel Value for rx_ana_cal_dac_ctrl_sel[4:0]

LANE0_DIG_ANA_RX_AFE_ATT_VGA
Address: Operational Base + offset (0x10B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	rx_ana_afe_rate Value for rx_ana_afe_rate[1:0]
13:12	RW	0x3	rx_ana_afe_ctle_pole Value for rx_ana_afe_ctle_pole[1:0]

Bit	Attr	Reset Value	Description
11	RW	0x0	rx_afe_rate_ovrd_en Override enable for rx_ana_afe_rate
10	RW	0x0	rx_ctle_pole_ovrd_en Override enable for rx_ana_ctle_pole
9	RW	0x0	rx_afe_gain_ovrd_en Override enable for rx_ana_afe_gain
8	RW	0x0	rx_afe_att_lvl_ovrd_en Override enable for rx_ana_afe_att_lvl
7	RW	0x0	rx_afe_update_ovrd_en Override enable for rx_ana_afe_update
6:3	RW	0x0	rx_ana_afe_gain Value for rx_ana_afe_gain[3:0]
2:0	RW	0x0	rx_ana_afe_att_lvl Value for rx_ana_afe_att_lvl[2:0]

LANE0_DIG_ANA_RX_AFE_CTLE

Address: Operational Base + offset (0x10B1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_afe_ctle_boost_ovrd_en Override enable for rx_ana_afe_ctle_boost
4:0	RW	0x00	rx_ana_afe_ctle_boost Value for rx_ana_afe_ctle_boost[4:0]

LANE0_DIG_ANA_RX_SCOPE

Address: Operational Base + offset (0x10B2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_scope_self_clear_disable Disable the self-clearing for rx_ana_scope_ph_clk register
12	RW	0x0	rx_ana_scope_clk_en Enable the scope clocks going to the scope slicer and the lane digital part
11:4	RW	0x00	rx_ana_scope_phase Sets value for rx_ana_scope_phase[7:0]
3	RW	0x0	rx_ana_scope_ph_clk Sets value for rx_ana_scope_ph_clk, this bit is self-clearing (i.e. only asserts for one cr_clk cycle)
2:1	RW	0x0	rx_ana_scope_sel Sets value for rx_ana_scope_sel 2'b00: AFE scope selected 2'b01: DFE even scope selected 2'b10: DFE odd scope selected 2'b11: DFE bypass/AFE buffer scope selected
0	RW	0x0	rx_ana_scope_en Sets value for rx_ana_scope_en

LANE0_DIG_ANA_RX_SLICER_CTRL

Address: Operational Base + offset (0x10B3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	rx_ana_slicer_ctrl_ovrd_en Override enable for RX ANA slicer ctrl
7:4	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE0_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST
Address: Operational Base + offset (0x10B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_ana_iq_phase_adjust Value for rx_ana_iq_phase_adjust[6:0]

LANE0_DIG_ANA_RX_ANA_IQ_SENSE_EN
Address: Operational Base + offset (0x10B5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_ana_iq_sense_en Value for rx_ana_iq_sense_en

LANE0_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN
Address: Operational Base + offset (0x10B6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	dac_ctrl_self_clear_disable Disable self-clearing for the rx_ana_cal_dac_ctrl_en register
0	RW	0x0	rx_ana_cal_dac_ctrl_en Value for rx_ana_cal_dac_ctrl_en, if DAC_CTRL_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE0_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE
Address: Operational Base + offset (0x10B7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	afe_update_self_clear_disable Disable self-clearing for the rx_ana_afe_update_en register
0	RW	0x0	rx_ana_afe_update_en Value for rx_ana_afe_update_en, if AFE_UPDATE_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE0_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK
Address: Operational Base + offset (0x10B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	phase_adjust_self_clear_disable Disable self-clearing for the rx_ana_iq_phase_adjust_clk register
0	RW	0x0	rx_ana_iq_phase_adjust_clk Value for rx_ana_iq_phase_adjust_clk, if PHASE_ADJUST_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE0_DIG_ANA_STATUS_0
Address: Operational Base + offset (0x10B9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RO	0x0	rx_ana_scope_data Value from ANA for rx_ana_scope_data
2	RO	0x0	rx_ana_cal_result Value from ANA for rx_ana_cal_result
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	tx_ana_loopback_en Value of tx_ana_loopback_en

LANE0_DIG_ANA_STATUS_1
Address: Operational Base + offset (0x10BA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_ana_vco_cntr Value from ANA for rx_ana_vco_cntr

LANE0_DIG_ANA_STATUS_LOS
Address: Operational Base + offset (0x10BB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RO	0x0	rx_ana_los_threshold Value to ANA for rx_ana_los_threshold
2	RO	0x0	rx_ana_los_en Value to ANA for rx_ana_los_en
1	RO	0x0	rx_ana_los_clk_en Value to ANA for rx_ana_los_clk_en
0	RO	0x0	rx_ana_los Value from ANA for rx_ana_los

LANE0_DIG_ANA_CREGS_TX_ANA_ATB_REG
Address: Operational Base + offset (0x10C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:3	RW	0x0	tx_ana_nc Reserved bit
2:1	RW	0x0	tx_ana_meas_atb BIST TX ATB measurement control
0	RW	0x0	tx_ana_meas_atb_en BIST TX ATB measurement enable

LANE0_DIG_ANA_CREGS_RX_ANA_EQ_CTRL

Address: Operational Base + offset (0x10C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x1	rx_ana_phdet_odd DFE sample control
4	RW	0x1	rx_ana_phdet_even DFE sample control
3:2	RW	0x1	rx_ana_ctle_offset_cal_enb EQ offset calibration enable
1:0	RW	0x0	rx_ana_afe_bias_mt EQ bias control

LANE0_DIG_ANA_CREGS_RX_ANA_VCO_CTRL

Address: Operational Base + offset (0x10C5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x1	rx_ana_cdr_vco_temp_comp_en VCO temperature compensation enable
1:0	RW	0x0	rx_ana_cdr_vco_startup_code VCO startup code

LANE0_DIG_ANA_CREGS_RX_ANA_VREG_CTRL

Address: Operational Base + offset (0x10C6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_vreg_ovrd_clk_vref VREG clk override reference voltage
4	RW	0x0	rx_ana_vreg_ovrd_vco_vref VREG VCO override reference voltage
3	RW	0x0	rx_ana_vreg_ovrd_vro_vref VREG VRO override reference voltage
2	RW	0x0	rx_ana_vreg_ovrd_cp_vref VREG charge-pump override reference voltage
1:0	RW	0x1	rx_ana_vreg_ring_ctrl VREG ring oscillator control

LANE0_DIG_ANA_CREGS_RX_ANA_DISCONNECT

Address: Operational Base + offset (0x10C7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_dc_path_disconnect TBA
1	RW	0x0	rx_ana_disconnect_m TBA
0	RW	0x0	rx_ana_disconnect_p TBA

LANE0_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL
Address: Operational Base + offset (0x10C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_ana_nc Reserved bits for future use

LANE0_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1
Address: Operational Base + offset (0x10C9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RW	0x0000	rx_meas_atb_14_0 Reserved
0	RW	0x0	rx_meas_atb_en rx_meas_atb_en

LANE0_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2
Address: Operational Base + offset (0x10CA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	rx_meas_atb_29_15 Reserved

LANE1_DIG_ASIC_LANE_OVRD_IN
Address: Operational Base + offset (0x1100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_loopback_clk_en Loopback clock enable. When enabled the VCO clock of current lane is sent to the adjacent lane for TX BIST operation
1	RW	0x0	Reserve_1 Reserve_1
0	RW	0x0	Reserve_0 Reserve_0

LANE1_DIG_ASIC_RX_ASIC_LOS
Address: Operational Base + offset (0x1101)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	los_en Value from asic for rx_los_en
14	RO	0x0	los_clk_en Value from asic for rx_los_clk_en
13:4	RO	0x000	los_timer_thresh Value from asic for rx_los_timer_thresh1
3:1	RO	0x0	los_threshold Value from asic for rx_los_threshold
0	RO	0x0	los Value of rx_los towards asic

LANE1_DIG_ASIC_LOS_OVRD_IN
Address: Operational Base + offset (0x1102)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	rx_los_ovrd Override enable for rx_los
8	RW	0x0	rx_los_r Override value for rx_los
7	RW	0x0	rx_los_threshold_ovrd Override enable for rx_los_threshold
6:4	RW	0x1	rx_los_threshold_r Override value for rx_los_threshold
3	RW	0x0	rx_los_clk_en_ovrd Override enable for rx_los_clk_en
2	RW	0x0	rx_los_clk_en_r Override value for rx_los_clk_en
1	RW	0x0	rx_los_en_ovrd Override enable for rx_los_en
0	RW	0x0	rx_los_en_r Override value for rx_los_en

LANE1_DIG_ASIC_LOS_OVRD_IN_1
Address: Operational Base + offset (0x1103)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RW	0x0	rx_los_timer_thresh_ovrd Override enable for rx_los_timer_thresh1
9:0	RW	0x05a	rx_los_timer_thresh_r Override value for rx_los_timer_thresh1

LANE1_DIG_ASIC_CDR_CONTROL_OVRD_IN
Address: Operational Base + offset (0x1106)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use

Bit	Attr	Reset Value	Description
3:1	RW	0x0	cdr_setting_sel Override values for CDR setting bits which select the CDR gain values
0	RW	0x0	cdr_setting_sel_ovrd_en Override enable for cdr_setting_sel signal

LANE1_DIG_ASIC_RX_OVRD_IN_0

Address: Operational Base + offset (0x1107)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:13	RW	0x0	rate_3_2 Override value for rx_rate[3:2]
12	RW	0x0	width_ovrd_en Enable override for rx_width
11:10	RW	0x0	width Override value for rx_width
9	RW	0x0	rate_ovrd_en Enable override value for rx_rate[1:0]
8:7	RW	0x0	rate_1_0 Override value for rx_rate
6	RW	0x0	pstate_ovrd_en Enable override value for rx_pstate
5:4	RW	0x0	pstate Override value for rx_pstate
3	RW	0x0	data_en_ovrd_en Enable override value for rx_data_en
2	RW	0x0	data_en Override value for rx_data_en
1	RW	0x0	req_ovrd_en Enable override value for rx_req
0	RW	0x0	req Override value for rx_req

LANE1_DIG_ASIC_RX_OVRD_IN_1

Address: Operational Base + offset (0x1108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:10	RW	0x0	rx_clk_x2_en Override value for rx_clk_x2_en[2:0]
9	RW	0x0	rx_cdr_vco_highfreq Override value for rx_cdr_vco_highfreq
8	RW	0x0	rx_ref_ld_val_6 Override value for rx_ref_ld_val[6]
7	RW	0x0	en Enable override values for all inputs controlled by this register
6	RW	0x0	rx_cdr_vco_lowfreq Override value for rx_cdr_vco_lowfreq
5:0	RW	0x14	rx_ref_ld_val_5_0 Override value for rx_ref_ld_val[5:0]

LANE1_DIG_ASIC_RX_OVRD_IN_2

Address: Operational Base + offset (0x1109)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	en Enable override values for all inputs controlled by this register
12:0	RW	0x03e8	rx_vco_ld_val Override value for rx_vco_ld_val

LANE1_DIG_ASIC_RX_OVRD_IN_3

Address: Operational Base + offset (0x110A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x00	reserved_14_to_10 Reserved_14_to_10
9	RW	0x0	disable_ovrd_en Enable override for rx_disable
8	RW	0x0	disable Override value for rx_disable
7	RW	0x0	clk_shift_ovrd_en Enable override for rx_clk_shift
6	RW	0x0	clk_shift Override value for rx_clk_shift
5	RW	0x0	align_en_ovrd_en Enable override for rx_align_en
4	RW	0x0	align_en Override value for rx_align_en
3	RW	0x0	cdr_ssc_en_ovrd_en Enable override value for rx_cdr_ssc_en
2	RW	0x0	cdr_ssc_en Override value for rx_cdr_ssc_en
1	RW	0x0	cdr_track_en_ovrd_en Enable override value for rx_cdr_track_en
0	RW	0x0	cdr_track_en Override value for rx_cdr_track_en

LANE1_DIG_ASIC_RX_OVRD_IN_4

Address: Operational Base + offset (0x110B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	adpt_ovrd_en Enable override for rx_adpt_dfe_en and rx_adpt_afe_en
5	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
4	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
3	RW	0x0	invert_ovrd_en Enable override for rx_invert

Bit	Attr	Reset Value	Description
2	RW	0x0	invert Override value for rx_invert
1	RW	0x0	lpd_ovrd_en Enable override for rx_lpd
0	RW	0x0	lpd Override value for rx_lpd

LANE1_DIG_ASIC_RX_OVRD_IN_5
Address: Operational Base + offset (0x110C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	reset_ovrd_en Enable override for rx_reset
0	RW	0x0	reset Override value for rx_reset

LANE1_DIG_ASIC_RX_OVRD_EQ_IN_0
Address: Operational Base + offset (0x110D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x06	eq_ctle_boost Override value for rx_eq_ctle_boost
10:7	RW	0x0	reserved Reserved
6:3	RW	0xf	eq_afe_gain Override value for rx_eq_afe_gain
2:0	RW	0x0	eq_att_lvl Override value for rx_eq_att_lvl

LANE1_DIG_ASIC_RX_OVRD_EQ_IN_1
Address: Operational Base + offset (0x110E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	eq_ovrd_en Enable override value for rx_eq_* inputs
14:7	RW	0x80	eq_dfe_tap1 Override value for rx_eq_dfe_tap1
6:0	RW	0x40	eq_dfe_tap2 Override value for rx_eq_dfe_tap2

LANE1_DIG_ASIC_RX_OVRD_OUT_0
Address: Operational Base + offset (0x110F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	ana_ovl_det_0v_en Enable override for rx_ana_ovl_det_0v_i
7	RW	0x0	ana_ovl_det_0v Override value for rx_ana_ovl_det_0v_i
6	RW	0x0	adapt_sts_ovrd_en Enable override for rx_adapt_sts

Bit	Attr	Reset Value	Description
5:4	RW	0x0	adapt_sts Override value for rx_adapt_sts
3	RW	0x0	rsv_0 Reserve_0
2	RW	0x0	rsv_1 Reserve_1
1	RW	0x0	ack_ovrd_en Enable override for rx_ack
0	RW	0x0	ack Override value for rx_ack

LANE1_DIG_ASIC_RX_ASIC_IN_0

Address: Operational Base + offset (0x1115)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_track_en Value from ASIC for rx_cdr_track_en
13	RO	0x0	adapt_dfe_en Value from ASIC for rx_adapt_dfe_en
12	RO	0x0	adapt_afe_en Value from ASIC for rx_adapt_afe_en
11	RO	0x0	reserved Reserved
10:9	RO	0x0	width Value from ASIC for rx_width
8:7	RO	0x0	rate_1_0 Value from ASIC for rx_rate[1:0]
6:5	RO	0x0	pstate Value from ASIC for rx_pstate
4	RO	0x0	lpd Value from ASIC for rx_lpd
3	RO	0x0	req Value from ASIC for rx_req
2	RO	0x0	data_en Value from ASIC for rx_data_en
1	RO	0x0	invert Value from ASIC for rx_invert
0	RO	0x0	reset Value from ASIC for rx_reset

LANE1_DIG_ASIC_RX_ASIC_IN_1

Address: Operational Base + offset (0x1116)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:8	RO	0x0	rate_3_2 Value from ASIC for rx_rate[3:2]
7	RO	0x0	reserved_7 Reserved_7
6:4	RO	0x0	reserved_6_to_4 Reserved_6_to_4

Bit	Attr	Reset Value	Description
3	RO	0x0	disable Value from ASIC for rx_disable
2	RO	0x0	clk_shift Value from ASIC for rx_clk_shift
1	RO	0x0	align_en Value from ASIC for rx_align_en
0	RO	0x0	cdr_ssc_en Value from ASIC for rx_cdr_ssc_en

LANE1_DIG_ASIC_RX_EQ_ASIC_IN_0
Address: Operational Base + offset (0x1117)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
10:9	RO	0x0	rx_ana_afe_rate Value from ASIC for rx_ana_afe_rate
8:7	RO	0x0	rx_ana_afe_ctle_pole Value from ASIC for rx_ana_afe_ctle_pole
6:3	RO	0x0	eq_afe_gain Value from ASIC for rx_eq_afe_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

LANE1_DIG_ASIC_RX_EQ_ASIC_IN_1
Address: Operational Base + offset (0x1118)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:7	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1
6:0	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2

LANE1_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0
Address: Operational Base + offset (0x1119)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RO	0x0	rx_clk_x2_en Value from ASIC for rx_clk_x2_en[2:0]
8	RO	0x0	rx_cdr_vco_highfreq Value from ASIC for rx_cdr_vco_highfreq
7:1	RO	0x00	rx_ref_ld_val Value from ASIC for rx_ref_ld_val
0	RO	0x0	rx_cdr_vco_lowfreq Value from ASIC for rx_cdr_vco_lowfreq

LANE1_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1
Address: Operational Base + offset (0x111A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_vco_ld_val Value from ASIC for rx_vco_ld_val

LANE1_DIG_ASIC_RX_ASIC_OUT_0
Address: Operational Base + offset (0x111B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:3	RO	0x0	adapt_sts Value from PHY for rx_adapt_sts
2	RO	0x0	valid Value from PHY for rx_valid
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	ack Value from PHY for rx_ack

LANE1_DIG_LBERT_CTL
Address: Operational Base + offset (0x1120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:5	RW	0x000	pat0 Pattern for modes 3-5
4	RW	0x0	trigger_err Insert a single error into a LSB any write of a 1 to this bit will insert an error
3:0	RW	0x0	mode Pattern to generate when changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: Fixed word (PAT0) 4'b1010: DC balanced word (PAT0, ~PAT0) 4'b1011: Fixed pattern: (000, PAT0, 3ff, ~PAT0) others: Reserved

LANE1_DIG_RX_CDR_CDR_CTL_0
Address: Operational Base + offset (0x1124)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use

Bit	Attr	Reset Value	Description
10:7	RW	0x0	dtb_sel Select to drive various signals onto the dtb 4'b0000: Disabled 4'b0001: Rx_pr_stable, rx_afe_stable from rx_ana_ctl 4'b0010: Com_good, com_bad from rx_align 4'b0011: Shift_in_prog, ana_odd_data from rx_align 4'b0100: 2 MSB's of XAUI align FSM state 4'b0101: 2 LSB's of XAUI align FSM state 4'b0110: Error_high, low from lbert_pm 4'b0111: Ana_los, los_filter from los block 4'b1000: Eios_state[0], eios_det from los block 4'b1001: Cdr_valid, MSB of FSM state from cdr_ctl 4'b1010: 2 LSB's of FSM state from cdr_ctl 4'b1011: Rx_dig_rst, rx_dig_en 4'b1100: Rx_ana_word_clk_i, rx_ana_dword_clk_i 4'b1101: Lbert_pg strobe others: Reserved
6	RW	0x0	always_realign Realign on any misaligned comma
5	RW	0x0	phdet_en_pr_mode Enable partial response phase detector mode
4	RW	0x0	phdet_pol Reverse polarity of phase error
3:2	RW	0x3	phdet_edge Edges to use for phase detection. 2'b00: Ignore all edges 2'b01: Use rising edges only 2'b10: Use both edges 2'b11: Use falling edges only
1:0	RW	0x3	phdet_en Enable phase detector. Top bit is odd slicers, bottom is even

LANE1_DIG_RX_CDR_CDR_CTL_1

Address: Operational Base + offset (0x1125)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RW	0x1c	ssc_off_cnt1 When SSC mode is disabled, the 12-bit word count in gain stage 1 is: (SSC_OFF_CNT1 * 4) in 20b mode (SSC_OFF_CNT1 * 5) in 16b mode
9:0	RW	0x039	ssc_off_cnt0 When SSC mode is disabled, the 12-bit word count in gain stage 0 is: (SSC_OFF_CNT0 * 4) in 20b mode (SSC_OFF_CNT0 * 5) in 16b mode

LANE1_DIG_RX_CDR_CDR_CTL_2

Address: Operational Base + offset (0x1126)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:9	RW	0x25	ssc_on_cnt1 When SSC mode is enabled, the 12-bit word count in gain stage 1 is: (SSC_ON_CNT1 * 8) in 20b mode (SSC_ON_CNT1 * 10) in 16b mode
8:0	RW	0x0bb	ssc_on_cnt0 When SSC mode is enabled, the 12-bit word count in gain stage 0 is: (SSC_ON_CNT0 * 8) in 20b mode (SSC_ON_CNT0 * 10) in 16b mode

LANE1_DIG_RX_CDR_CDR_CTL_3

Address: Operational Base + offset (0x1127)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:10	RW	0x2	ssc_on_phug1 When SSC mode is enabled, the phug value in gain stage 1 is SSC_ON_PHUG1
9:6	RW	0x6	ssc_on_phug0 When SSC mode is enabled, the phug value in gain stage 0 is SSC_ON_PHUG0
5:3	RW	0x3	ssc_on_frug1 When SSC mode is enabled, the frug value in gain stage 1 is SSC_ON_FRUG1
2:0	RW	0x3	ssc_on_frug0 When SSC mode is enabled, the frug value in gain stage 0 is SSC_ON_FRUG0

LANE1_DIG_RX_CDR_CDR_CTL_4

Address: Operational Base + offset (0x1128)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:8	RW	0x0	frug_ovrd_value Override value for frug (frequency update gain) 3'b000: 0 3'b001: 1/16 LSB/update 3'b010: 1/8 LSB/update 3'b011: 1/4 LSB/update 3'b100: 1/2 LSB/update 3'b101: 1 LSB/update 3'b110: 2 LSB/update 3'b111: 4 LSB/update

Bit	Attr	Reset Value	Description
7:4	RW	0x0	phug_ovrd_value Override value for phug (phase update gain) : 16'b0000: 0 16'b0001: 1000 ppm 16'b0010: 2000 ppm 16'b0011: 3000 ppm 16'b0100: 4000 ppm 16'b0101: 5000 ppm 16'b0110: 6000 ppm 16'b0111: 7000 ppm 16'b1000: 8000 ppm 16'b1001: 9000 ppm 16'b1010: 10000 ppm 16'b1011: 11000 ppm 16'b1100: 12000 ppm 16'b1101: 13000 ppm 16'b1110: 14000 ppm 16'b1111: 15000 ppm
3	RW	0x0	ovrd_dpll_gain Override phug and frug values
2:0	RW	0x3	ssc_off_frug0 When SSC mode is disabled, the frug value in gain stage 0 is SSC_OFF_FRUG0

LANE1_DIG_RX_CDR_CDR_CTL_5

Address: Operational Base + offset (0x1129)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs3_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS3_FRUG1
8:6	RW	0x1	ssc_off_lbrs2_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS2_FRUG1
5:3	RW	0x1	ssc_off_lbrs1_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS1_FRUG1
2:0	RW	0x1	ssc_off_lbrs0_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS0_FRUG1

LANE1_DIG_RX_CDR_CDR_CTL_6

Address: Operational Base + offset (0x112A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs7_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS7_FRUG1
8:6	RW	0x3	ssc_off_lbrs6_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS6_FRUG1

Bit	Attr	Reset Value	Description
5:3	RW	0x3	ssc_off_lbrs5_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS5_FRUG1
2:0	RW	0x3	ssc_off_lbrs4_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS4_FRUG1

LANE1_DIG_RX_CDR_CDR_CTL_7

Address: Operational Base + offset (0x112B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x8	ssc_off_lbrs3_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS3_PHUG0
11:8	RW	0x7	ssc_off_lbrs2_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS2_PHUG0
7:4	RW	0x6	ssc_off_lbrs1_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS1_PHUG0
3:0	RW	0x6	ssc_off_lbrs0_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS0_PHUG0

LANE1_DIG_RX_CDR_CDR_CTL_8

Address: Operational Base + offset (0x112C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS7_PHUG0
11:8	RW	0xc	ssc_off_lbrs6_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS6_PHUG0
7:4	RW	0xc	ssc_off_lbrs5_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS5_PHUG0
3:0	RW	0xa	ssc_off_lbrs4_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS4_PHUG0

LANE1_DIG_RX_CDR_CDR_CTL_9

Address: Operational Base + offset (0x112D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x6	ssc_off_lbrs3_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS3_PHUG1
11:8	RW	0x4	ssc_off_lbrs2_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS2_PHUG1
7:4	RW	0x3	ssc_off_lbrs1_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS1_PHUG1

Bit	Attr	Reset Value	Description
3:0	RW	0x2	ssc_off_lbrs0_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS0_PHUG1

LANE1_DIG_RX_CDR_CDR_CTL_10
Address: Operational Base + offset (0x112E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS7_PHUG1
11:8	RW	0xc	ssc_off_lbrs6_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS6_PHUG1
7:4	RW	0xa	ssc_off_lbrs5_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS5_PHUG1
3:0	RW	0x8	ssc_off_lbrs4_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS4_PHUG1

LANE1_DIG_RX_CDR_STAT
Address: Operational Base + offset (0x112F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:4	RO	0x0	frug_value Notes: Current value for dpll_frug[2:0]
3:0	RO	0x0	phug_value Notes: Current value for dpll_phug[3:0]

LANE1_DIG_RX_PWRCTL_RX_PSTATE_P0
Address: Operational Base + offset (0x1140)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	rx_p0_dig_clk_en Enable/Disable RX digital clocks in P0
10	RW	0x1	rx_p0_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0, if RX_P0_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0_vco_cal_rst Enable/Disable resetting the RX VCO in P0
8	RW	0x0	rx_p0_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0
7	RW	0x1	rx_p0_ana_cdr_en Value of RX ana cdr_en in P0
6	RW	0x1	rx_p0_ana_deser_en Value of RX ana deserial_en in P0

Bit	Attr	Reset Value	Description
5	RW	0x1	rx_p0_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0
4	RW	0x1	rx_p0_ana_clk_en Value of RX ana clk_en in P0
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0
1	RW	0x1	rx_p0_ana_afe_en Value of RX ana afe_en in P0
0	RW	0x1	reserved_0 Reserved_0

LANE1_DIG_RX_PWRCTL_RX_PSTATE_P0S

Address: Operational Base + offset (0x1141)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p0s_dig_clk_en Enable/Disable RX digital clocks in P0S
10	RW	0x1	rx_p0s_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0S, if RX_P0S_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0s_vco_cal_rst Enable/Disable resetting the RX VCO in P0S
8	RW	0x0	rx_p0s_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0S
7	RW	0x0	rx_p0s_ana_cdr_en Value of RX ana cdr_en in P0S
6	RW	0x0	rx_p0s_ana_deser_en Value of RX ana deserial_en in P0S
5	RW	0x0	rx_p0s_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0S
4	RW	0x0	rx_p0s_ana_clk_en Value of RX ana clk_en in P0S
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0s_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0S
1	RW	0x1	rx_p0s_ana_afe_en Value of RX ana afe_en in P0S
0	RW	0x1	reserved_0 Reserved_0

LANE1_DIG_RX_PWRCTL_RX_PSTATE_P1

Address: Operational Base + offset (0x1142)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use

Bit	Attr	Reset Value	Description
11	RW	0x0	rx_p1_dig_clk_en Enable/Disable RX digital clocks in P1
10	RW	0x0	rx_p1_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P1, if RX_P1_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p1_vco_cal_rst Enable/Disable resetting the RX VCO in P1
8	RW	0x1	rx_p1_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P1
7	RW	0x0	rx_p1_ana_cdr_en Value of RX ana cdr_en in P1
6	RW	0x0	rx_p1_ana_deser_en Value of RX ana deserial_en in P1
5	RW	0x0	rx_p1_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P1
4	RW	0x0	rx_p1_ana_clk_en Value of RX ana clk_en in P1
3	RW	0x0	reserved
2	RW	0x1	rx_p1_ana_clk_vreg_en Value of RX ana clk_vreg_en in P1
1	RW	0x1	rx_p1_ana_afe_en Value of RX ana afe_en in P1
0	RW	0x1	reserved_0 Reserved_0

LANE1_DIG_RX_PWRCTL_RX_PSTATE_P2

Address: Operational Base + offset (0x1143)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p2_dig_clk_en Enable/Disable RX digital clocks in P2
10	RW	0x0	rx_p2_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P2, if RX_P2_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p2_vco_cal_rst Enable/Disable resetting the RX VCO in P2
8	RW	0x1	rx_p2_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P2
7	RW	0x0	rx_p2_ana_cdr_en Value of RX ana cdr_en in P2
6	RW	0x0	rx_p2_ana_deser_en Value of RX ana deserial_en in P2
5	RW	0x0	rx_p2_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P2
4	RW	0x0	rx_p2_ana_clk_en Value of RX ana clk_en in P2
3	RW	0x0	reserved Reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_p2_ana_clk_vreg_en Value of RX ana clk_vreg_en in P2
1	RW	0x0	rx_p2_ana_afe_en Value of RX ana afe_en in P2
0	RW	0x1	reserved_0 Reserved_0

LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_0

Address: Operational Base + offset (0x1144)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x0f	rx_dpll_clock_switch_time Wait between switching rx_dpll clock from Rx_clk to ref_clk or vice-versa
4:0	RW	0x06	rx_state_3a_and_3b_time Wait between Power state 3A and 3B

LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_1

Address: Operational Base + offset (0x1145)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	fast_rx_vreg_en Enable fast RX VREG enable (simulation only)
12:7	RW	0x0d	rx_vreg_en_time Power up time (in ref_range cycles) for RX ana vreg enable (spec 500ns)
6	RW	0x0	fast_rx_afe_en Enable fast RX AFE enable (simulation only)
5:0	RW	0x1a	rx_afe_en_time Power up time (in ref_range cycles) for RX ana AFE enable (spec >=1us)

LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_2

Address: Operational Base + offset (0x1146)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	fast_rx_clk_en Enable fast RX clock enable (simulation only)
5:0	RW	0x1a	rx_clk_en_time Power up time (in ref_range cycles) for RX ana clk (or dcc) enable (spec >1us)

LANE1_DIG_RX_PWRCTL_RX_PWRUP_TIME_3

Address: Operational Base + offset (0x1147)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	rx_deser_dis_time Power down time in (ref_range cycles) for RX ana deserial enable

Bit	Attr	Reset Value	Description
13:12	RW	0x0	rx_deser_en_time Power up time (in ref_range cycles) for RX ana deserial enable
11:8	RW	0x0	rx_cdr_en_time Power up time (in ref_range cycles) for RX ana CDR (or dfe/dfe_taps) enable (spec 0ns)
7:2	RW	0x00	rsvd_3_7_2 Reserved
1:0	RW	0x0	rx_rate_time Power up time (in ref_range cycles) for RX ana rate or width change

LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0

Address: Operational Base + offset (0x1148)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RW	0x0	vcoclk_correct_update Update the vcoclk_correct
11:9	RW	0x2	int_gain_cal_bounce_cnt Number of bounces (i.e. direction changes) on the int_gain code before indicating that the RX VCO calibration is done
8:6	RW	0x0	int_gain_cal_cnt_shift Number of shifts to apply to ld_cnt inputs when performing int_gain code calibration
5	RW	0x0	int_gain_cal_fixed_cnt_en Enable a fixed count (instead of bounce count) for int_gain code calibration
4:0	RW	0x00	int_gain_cal_fixed_cnt Number of steps done during int_gain code calibration when INT_GAIN_CAL_FIXED_CNT_EN is enabled.

LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1

Address: Operational Base + offset (0x1149)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x00	dtb_sel DTB select for RX VCO dtb signals 7'h01: {chkfrq_en, ref_dig_clk} 7'h02: {rx_ana_cdr_vco_en_i, rx_ana_cdr_startup_i} 7'h04: {rx_vco_up, dpll_freq_rst} 7'h08: {rx_vco_contcal_en, rx_vco_cal_rst} 7'h10: {chkfrq_done, vcoclk_too_fast} 7'h20: {cal_dir, rx_vco_cal_done} 7'h40: {curr_state[0], rx_vco_cnt[0]} others: Reserved
8:5	RW	0x8	dpll_cal_ug DPLL calibration update on int_gain code 3'b000: 0 others: (1/16)*2^(DPLL_CAL_UG-1) LSB/update Maximum DPLL_CAL_UG=10, i.e. 32 LSB/update

Bit	Attr	Reset Value	Description
4	RW	0x0	disable_int_cal_mode When asserted, then the DPLL frequency register is never modified by the RX VCO calibration FSM (even, if DPLL_CAL_UG is non-zero). In this case, the calibration will always be performed on the VCO freq_tune code. This allows disabling of integral calibration feature, and hence only using freq_tune calibration.
3	RW	0x0	rx_vco_contcal_en Override value for the continuous calibration enable from the RX PWRSM
2	RW	0x0	rx_vco_cal_rst Override value for the calibration reset from the RX PWRSM
1	RW	0x0	rx_vco_freq_rst Override value for the frequency reset from the RX PWRSM
0	RW	0x0	rx_vco_ovrd_sel Override the calibration controls from the RX PWRSM

LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2
Address: Operational Base + offset (0x114A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_rx_vco_cal Skip RX VCO calibration altogether
14	RW	0x0	skip_rx_vco_freq_tune_cal Skip RX VCO coarse calibration
13:10	RW	0x9	freq_tune_cal_steps Number of cal steps of freq tune
9:0	RW	0x200	freq_tune_start_val Starting value of freq tune code

LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0
Address: Operational Base + offset (0x114B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	fast_rx_vco_wait Enable fast RX VCO power up (simulation only)
14:11	RW	0x6	rx_vco_cntr_pwrup_time Power up time (in ref_range cycles) for RX ana VCO cnter (spec >200ns)
10:7	RW	0x6	rx_vco_update_time Settle time (in ref_range cycles) for RX ana VCO update (freq_tune or int_gain) (spec >200ns)
6:0	RW	0x19	rx_vco_startup_time Power up time (in ref_range cycles) for RX ana VCO startup (spec >1us)

LANE1_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1
Address: Operational Base + offset (0x114C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use

Bit	Attr	Reset Value	Description
2:0	RW	0x3	rx_vco_cntr_settle_time RX VCO counter value settling time in (ref_dig_clk cycles) (spec: 3 ref_dig_clk cycle)

LANE1_DIG_RX_VCOCAL_RX_VCO_STAT_0

Address: Operational Base + offset (0x114D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	rx_ana_cdr_vco_en Current value of rx_ana_cdr_vco_en_i
12	RO	0x0	rx_ana_cdr_startup Current value of rx_ana_cdr_startup_i
11	RO	0x0	rx_ana_vco_cntr_en Current value of rx_ana_vco_cntr_en_i
10	RO	0x0	rx_ana_vco_cntr_pd Current value of rx_ana_vco_cntr_pd_i
9:0	RO	0x000	rx_ana_cdr_freq_tune Current value of rx_ana_cdr_freq_tune_i

LANE1_DIG_RX_VCOCAL_RX_VCO_STAT_1

Address: Operational Base + offset (0x114E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	dpll_freq_rst Indicates that the RX integral frequency is reset or not
7	RO	0x0	rx_vco_cal_done Indicates that the RX VCO has completed calibration
6	RO	0x0	rx_vco_contcal_en Value of the continuous calibration enable from the RX PWRSM
5	RO	0x0	rx_vco_cal_rst Value of the calibration reset from the RX PWRSM
4	RO	0x0	rx_vco_freq_rst Value of the RX VCO frequency reset from the RX PWRSM
3:0	RO	0x0	rx_vco_fsm_state Value of the RX VCO CAL FSM

LANE1_DIG_RX_VCOCAL_RX_VCO_STAT_2

Address: Operational Base + offset (0x114F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	rx_vco_up Indicates that the RX VCO is ready
14	RO	0x0	rx_vco_correct Indicates that the RX VCO clock has the correct frequency
13	RO	0x0	vcoclk_too_fast Indicates that the RX VCO clock frequency is too fast
12:0	RO	0x0000	vco_cntr_final Value of RX VCO counter when refclk counter expired

LANE1_DIG_RX_RX_ALIGN_XAUI_COMM_MASK

Address: Operational Base + offset (0x1150)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x3ff	xaui_comm_mask XAUI_COMMA mask. For 10-bit COMMA set the mask to 0x3FF and for 7-bit COMMA set the mask to 0x3F8

LANE1_DIG_RX_LBERT_CTL

Address: Operational Base + offset (0x1151)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	sync Synchronize pattern matcher LFSR with incoming data A write of a one to this bit will reset the error counter and start a synchronization of the PM, there is no need to write this back to zero to run normally.
3:0	RW	0x0	mode Pattern to match When changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: D[n] = d[n-10] 4'b1010: D[n] = !d[n-10] 4'b1011: D[n] = !d[n-20] others: Reserved

LANE1_DIG_RX_LBERT_ERR

Address: Operational Base + offset (0x1152)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ov14 If active, multiply count by 128. if OV14=1 and count=2^15-1, signals overflow of counter (2 reads needed to read value)
14:0	RW	0x0000	count A read of this register, or a sync of the PM resets the error count. Current error count, if OV14 field is active, then multiply count by 128 (2 reads needed to read value)

LANE1_DIG_RX_RX_LOS_LOS_0

Address: Operational Base + offset (0x1153)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use

Bit	Attr	Reset Value	Description
8	RW	0x0	rx_los_filt_byp Bypass digital LOS filter
7:3	RW	0x0c	rx_los_t_thresh0_r LOS timer0 threshold to count presence of zeros on rx_los
2:0	RW	0x2	rx_los_wait_r Initial wait time for rx_los after rx_los_en is asserted

LANE1_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS
Address: Operational Base + offset (0x1155)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_pwrsm_state Value for rx_pwrsm_state

LANE1_DIG_RX_DPLL_FREQ
Address: Operational Base + offset (0x115C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:0	RW	0x2000	val Freq is 125*VAL ppm from the reference (2 reads needed to read value)

LANE1_DIG_RX_DPLL_FREQ_BOUND_0
Address: Operational Base + offset (0x115D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:1	RW	0x264	upper_freq_bound Upper frequency bound in terms of LSBs of the integral control code
0	RW	0x0	freq_bound_en Enable the frequency bounds feature

LANE1_DIG_RX_DPLL_FREQ_BOUND_1
Address: Operational Base + offset (0x115E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x19c	lower_freq_bound Lower frequency bound in terms of LSBs of the integral control code

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_0
Address: Operational Base + offset (0x1160)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	adpt_clk_div4_en Set the adaptation clock to be divided by 4 (default is div2)

Bit	Attr	Reset Value	Description
14	RW	0x0	start_asm1 Start adaptation state machine #1 (VGA, CTLE, DFE, EYEH) This register-bit is self-clearing
13:10	RW	0x3	n_tgg_asm1 Number of toggle loop iterations for ASM1
9:0	RW	0x010	n_top_asm1 Number of top level loop iterations for ASM1

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_1
Address: Operational Base + offset (0x1161)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	ctle_pole_ovrd_en Override CTLE pole value (only valid, if adaptation is run)
10:8	RW	0x0	ctle_pole_ovrd_val CTLE pole override value to load at start of adaptation
7	RW	0x0	fast_afe_dfe_settle Enable fast AFE and DFE settling time (simulation only)
6:0	RW	0x09	n_wait_asm1 Number of wait cycles for adaptation SM #1

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_2
Address: Operational Base + offset (0x1162)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x06	tgg_pttrn_1 Pattern for the second toggle loop error slicer is moved upward by data tap1, if this pattern is matched
4:0	RW	0x02	tgg_pttrn_0 Pattern for the first toggle loop error slicer is moved downward by data tap1, if this pattern is matched

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_3
Address: Operational Base + offset (0x1163)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	esl_twice_dsl Assert, if error slicer has twice the voltage range as the data slicer (for the same 8 bits).
14	RW	0x0	tgg_en Enable toggling of the error slicer
13	RW	0x0	eyeho_en Enable eye height measurement using odd error slicer
12	RW	0x0	eyehe_en Enable eye height measurement using even error slicer
11:7	RW	0x00	dfe_en Enable DFE adaptation for taps 5-1
6	RW	0x0	att_en Enable ATT adaptation

Bit	Attr	Reset Value	Description
5	RW	0x0	vga_en Enable VGA adaptation
4:0	RW	0x00	ctle_en Enable CTLE boost adaptation, the five bits determine which correlators are used to adapt the CTLE

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_4
Address: Operational Base + offset (0x1164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	dfe2_th DFE Tap2 correlation decision threshold (2^N-1)
11:8	RW	0x0	dfe1_th DFE Tap1 correlation decision threshold (2^N-1)
7:4	RW	0x0	vga_th VGA correlation decision threshold (2^N-1). During eye height measurement, the VGA_TH is repurposed for error slicer updates.
3:0	RW	0x0	ctle_th CTLE correlation decision threshold (2^N-1)

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_5
Address: Operational Base + offset (0x1165)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	th_offset Apply an offset to the decision threshold
11:8	RW	0x0	dfe5_th DFE Tap5 correlation decision threshold (2^N-1)
7:4	RW	0x0	dfe4_th DFE Tap4 correlation decision threshold (2^N-1)
3:0	RW	0x0	dfe3_th DFE Tap3 correlation decision threshold (2^N-1)

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_6
Address: Operational Base + offset (0x1166)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RW	0x3	att_low_th ATT low threshold
12	RW	0x1	vga_sat_cnt_sticky If deasserted, then VGA saturation counts must be consecutive to change ATT
11:9	RW	0x4	vga_sat_cnt VGA saturation count
8:6	RW	0x4	att_mu ATT gain code update gain (2^N)
5:3	RW	0x5	vga_mu VGA gain code update gain (2^N). During eye height measurement, the VGA_MU is repurposed for error slicer updates.
2:0	RW	0x3	ctle_mu CTLE boost code update gain (2^N)

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_7
Address: Operational Base + offset (0x1167)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x10	vga_lev_low VGA level low saturation limit
9:5	RW	0x1a	vga_lev_high VGA level high saturation limit
4:0	RW	0x02	vga_min_sat VGA minimum saturation limit

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_8
Address: Operational Base + offset (0x1168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x4	dfe5_mu DFE tap5 code update gain (2^N)
11:9	RW	0x4	dfe4_mu DFE tap4 code update gain (2^N)
8:6	RW	0x4	dfe3_mu DFE tap3 code update gain (2^N)
5:3	RW	0x4	dfe2_mu DFE tap2 code update gain (2^N)
2:0	RW	0x5	dfe1_mu DFE tap1 code update gain (2^N)

LANE1_DIG_RX_ADPTCTL_ADPT_CFG_9
Address: Operational Base + offset (0x1169)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	err_slo_adpt_init The error odd slicer is initialized to this value at the start of a new adaptation request.
7:0	RW	0x00	err_sle_adpt_init The error even slicer is initialized to this value at the start of a new adaptation request.

LANE1_DIG_RX_ADPTCTL_RST_ADPT_CFG
Address: Operational Base + offset (0x116A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x1	rst_adpt_tap1 Reset data Tap1 when turning off DFE adaptation (taps 2-5 are always turned off when DFE adaptation is turned off)
3	RW	0x1	rst_adpt_ctle_pole Reset CTLE pole when turning off AFE adaptation
2	RW	0x1	rst_adpt_ctle_boost Reset CTLE boost when turning off AFE adaptation

Bit	Attr	Reset Value	Description
1	RW	0x1	rst_adpt_vga Reset VGA when turning off AFE adaptation
0	RW	0x1	rst_adpt_att Reset ATT when turning off AFE adaptation

LANE1_DIG_RX_ADPTCTL_ATT_STATUS

Address: Operational Base + offset (0x116B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	asm1_don Asserts when adaptation state machine #1 is done
7:0	RO	0x00	att_adpt_code Value of ATT adaptation code

LANE1_DIG_RX_ADPTCTL_VGA_STATUS

Address: Operational Base + offset (0x116C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
9:0	RO	0x000	vga_adpt_code Value of VGA adaptation code

LANE1_DIG_RX_ADPTCTL_CTLE_STATUS

Address: Operational Base + offset (0x116D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:10	RO	0x0	ctle_pole_adpt_code Value of CTLE pole adaptation code
9:0	RO	0x000	ctle_boost_adpt_code Value of CTLE boost adaptation code

LANE1_DIG_RX_ADPTCTL_DFE_TAP1_STATUS

Address: Operational Base + offset (0x116E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:0	RO	0x0000	dfe_tap1_adpt_code Value of DFE tap1 adaptation code

LANE1_DIG_RX_ADPTCTL_DFE_TAP2_STATUS

Address: Operational Base + offset (0x116F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap2_adpt_code Value of DFE tap2 adaptation code

LANE1_DIG_RX_ADPTCTL_DFE_TAP3_STATUS

Address: Operational Base + offset (0x1170)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap3_adpt_code Value of DFE tap3 adaptation code

LANE1_DIG_RX_ADPTCTL_DFE_TAP4_STATUS

Address: Operational Base + offset (0x1171)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap4_adpt_code Value of DFE tap4 adaptation code

LANE1_DIG_RX_ADPTCTL_DFE_TAP5_STATUS

Address: Operational Base + offset (0x1172)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap5_adpt_code Value of DFE tap5 adaptation code

LANE1_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1173)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_vdac_ofst Offset value for DFE data even vDAC

LANE1_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST

Address: Operational Base + offset (0x1174)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_vdac_ofst Offset value for DFE data odd vDAC

LANE1_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN

Address: Operational Base + offset (0x1175)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE1_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD

Address: Operational Base + offset (0x1176)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

LANE1_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1177)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

LANE1_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST

Address: Operational Base + offset (0x1178)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

LANE1_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL

Address: Operational Base + offset (0x1179)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	e_sle_lvl Even error slicer level
7:0	RO	0x00	e_slo_lvl Odd error slicer level

LANE1_DIG_RX_ADPTCTL_ADPT_RESET

Address: Operational Base + offset (0x117A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	reset_asm1 Resets adaptation state machine (ASM1) as well as the stats capture block. This is a self-clearing bit, and requires re-start of ASM1.

LANE1_DIG_RX_STAT_LD_VAL_1

Address: Operational Base + offset (0x1180)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sc1_start Start sample counter #1 this is a self-clearing bit
14:0	RW	0x0040	sc1_ld_val Sample counter #1 load value

LANE1_DIG_RX_STAT_DATA_MSK

Address: Operational Base + offset (0x1181)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	data_msk_15_0 Value of data_msk_r[15:0]

LANE1_DIG_RX_STAT_MATCH_CTL0

Address: Operational Base + offset (0x1182)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	scope_dly For clock cycle delays on scope_data_rx_clk, an additional MSB is added in SCOPE_DLY_2
13:10	RW	0xf	data_msk_19_16 Value of data_msk_r[19:16]
9:5	RW	0x00	pttrn_cr1a_4_0 Value of pattern A for 1st correlator (bits 4:0)
4:0	RW	0x06	pttrn_msk_cr1a_4_0 Value of pattern A mask for 1st correlator (bits 4:0)

LANE1_DIG_RX_STAT_MATCH_CTL1

Address: Operational Base + offset (0x1183)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	pttrn_cr1a_adpt_en Enable ORing of adapation pattern with pattern CR1A
10:6	RW	0x00	pttrn_cr1b_4_0 Value of pattern B for 1st correlator (bits 4:0)
5:1	RW	0x00	pttrn_msk_cr1b_4_0 Value of pattern B mask for 1st correlator (bits 4:0)
0	RW	0x0	pttrn_cr1b_en Enable pattern B matching for 1st correlator

LANE1_DIG_RX_STAT_STAT_CTL0

Address: Operational Base + offset (0x1184)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_en Value of skip_en_r
14	RW	0x1	sc_timer_mode Sample counter operation mode 1'b0: Counts number of matched samples 1'b1: Counts clock cycles (i.e. a timer)
13	RW	0x0	stat_rxclk_sel Select stat clock 1'b0: Ref_range_clk 1'b1: Rx_dig_clk (i.e. RX dword clk) Before changing stat_rxclk_sel_r from 1->0, the rx_dig_clk must be active (i.e. enabled)
12:10	RW	0x0	stat_src_sel Select stat source input 3'b000: {20{rx_cal_result}} 3'b001: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 3'b010: Rx_phase[39:0] 3'b011: Rx_error[39:0] 3'b100: Rx_data[39:0] 3'b101: Rx_phdir[39:0] 3'b110: 40'hFF_FFFF_FFFF others: Reserved
9:6	RW	0x0	stat_shft_sel Select stat source shift value 4'b0000: Correlate N-1 -> N+3 (use N for offset calibration) 4'b0001: Correlate N+1 -> N+5 (for taps1-5) 4'b0010: Correlate N+6 -> N+10 4'b0011: Correlate N+11 -> N+15 4'b0100: Correlate N+16 -> N+20 4'b0101: Correlate N+21 -> N+25 4'b0110: Correlate N+26 -> N+30 4'b0111: Correlate N+31 -> N+35 4'b1000: Correlate N+36 -> N+39 others: Reserved Setting 0x8 is only used in 20b mode (for checking corr on bits 36-39)
5	RW	0x0	corr_mode_en Enable correlation mode
4:3	RW	0x0	corr_src_sel Select correlation input source 2'b00: Rx_error[39:0] 2'b01: Rx_phase[39:0] 2'b10: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 2'b11: No correlation
2	RW	0x0	corr_shft_sel Select shift for phase. 1'b0: None 1'b1: >>1
1	RW	0x0	corr_shft_sel_vga Select shift for error going to VGA. 1'b0: None 1'b1: >>1

Bit	Attr	Reset Value	Description
0	RW	0x0	reserved_0 Reserved bit

LANE1_DIG_RX_STAT_STAT_CTL1

Address: Operational Base + offset (0x1185)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	vld_ctl Gating configuration of stats collection 2'b00: Ignore both cdr_valid and rx_valid 2'b01: Gate stats collection with cdr_valid 2'b10: Gate stats collection with rx_valid 2'b11: Ignore both cdr_valid and rx_valid
13	RW	0x0	vld_loss_clr Clearing of stats collection upon loss of valid 1'b0: Hold sample and stat counters 1'b1: Clear sample and stat counters
12:11	RW	0x0	data_dly_sel For clock cycle delays on rx_data[19:0], an additional MSB is added in data_dly_sel_2
10	RW	0x0	stat_clk_en Clock gate enable for stat clock
9	RW	0x0	sc_pause Pause the sample counter and stat counters
8:7	RW	0x0	reserved_8_7 Reserved bits
6	RW	0x0	stat_cnt_6_en Enable for stat counter 6
5	RW	0x0	stat_cnt_5_en Enable for stat counter 5
4	RW	0x0	stat_cnt_4_en Enable for stat counter 4
3	RW	0x1	stat_cnt_3_en Enable for stat counter 3 only counter to be enabled by default, since used for offset calibration
2	RW	0x0	stat_cnt_2_en Enable for stat counter 2
1	RW	0x0	stat_cnt_1_en Enable for stat counter 1
0	RW	0x0	stat_cnt_0_en Enable for stat counter 0

LANE1_DIG_RX_STAT_SMPL_CNT1

Address: Operational Base + offset (0x1186)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	smpl_cnt1 Current value of sample counter #1

LANE1_DIG_RX_STAT_STAT_CNT_0

Address: Operational Base + offset (0x1187)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_0 Current value of stat counter #0

LANE1_DIG_RX_STAT_STAT_CNT_1

Address: Operational Base + offset (0x1188)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_1 Current value of stat counter #1

LANE1_DIG_RX_STAT_STAT_CNT_2

Address: Operational Base + offset (0x1189)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_2 Current value of stat counter #2

LANE1_DIG_RX_STAT_STAT_CNT_3

Address: Operational Base + offset (0x118A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_3 Current value of stat counter #3

LANE1_DIG_RX_STAT_STAT_CNT_4

Address: Operational Base + offset (0x118B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_4 Current value of stat counter #4

LANE1_DIG_RX_STAT_STAT_CNT_5

Address: Operational Base + offset (0x118C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_5 Current value of stat counter #5

LANE1_DIG_RX_STAT_STAT_CNT_6

Address: Operational Base + offset (0x118D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_6 Current value of stat counter #6

LANE1_DIG_RX_STAT_CAL_COMP_CLK_CTL

Address: Operational Base + offset (0x118E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RW	0x3	ref_div_cnt Ref range clock count (e.g. 5'd3 = 4 ref_range cycles)
2:0	RW	0x1	prechrge_cnt Precharge count (e.g. 5'd1 = 2 ref_range cycles)

LANE1_DIG_RX_STAT_MATCH_CTL2

Address: Operational Base + offset (0x118F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1a_19_5 Value of pattern A for 1st correlator (bits 19:5)

LANE1_DIG_RX_STAT_MATCH_CTL3

Address: Operational Base + offset (0x1190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1a_19_5 Value of pattern A mask for 1st correlator (bits 19:5)

LANE1_DIG_RX_STAT_MATCH_CTL4

Address: Operational Base + offset (0x1191)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1b_19_5 Value of pattern B for 1st correlator (bits 19:5)

LANE1_DIG_RX_STAT_MATCH_CTL5

Address: Operational Base + offset (0x1192)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1b_19_5 Value of pattern B mask for 1st correlator (bits 19:5)

LANE1_DIG_RX_STAT_STAT_CTL2

Address: Operational Base + offset (0x1193)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	scope_dly_2 Additional MSB bit for SCOPE_DLY to extend the delay range to 0->7
0	RW	0x0	data_dly_sel_2 Additional MSB bit for data_dly_sel to extend the delay range to 0->7

LANE1_DIG_RX_STAT_STAT_STOP

Address: Operational Base + offset (0x1194)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	sc1_stop Stop sample counters #1 and associated stat counters. This is a self-clearing bit, and requires re-start of sample counter #1.

LANE1_DIG_ANA_TX_OVRD_OUT

Address: Operational Base + offset (0x11A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	tx_ovrd_en Enable override values for all outputs controlled by this register
0	RW	0x0	tx_ana_reset Override value for tx_ana_reset

LANE1_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT

Address: Operational Base + offset (0x11A1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	tx_ana_lpbk_dfe_mode Value for tx_ana_lpbk_dfe_mode

LANE1_DIG_ANA_RX_DIV_OVRD_OUT

Address: Operational Base + offset (0x11A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_ana_div5_en Override value for rx_ana_div5_en
0	RW	0x0	rx_ana_div13p5_en Override value for rx_ana_div13p5_en

LANE1_DIG_ANA_RX_CTL_OVRD_OUT

Address: Operational Base + offset (0x11A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_lbk_clk_en_ovrd Enable override value for rx_ana_loopback_clk_en
14	RW	0x0	rx_ana_adaptation_en_ovrd Enable override value for rx_ana_adaptation_en
13	RW	0x0	rx_ana_dfe_taps_en_ovrd Enable override value for rx_ana_dfe_taps_en
12	RW	0x0	rx_ana_div4_en_ovrd Enable override value for rx_ana_div4_en
11	RW	0x0	rx_ana_word_clk_en_ovrd Enable override value for rx_ana_word_clk_en
10	RW	0x0	rx_ana_data_rate_en_ovrd Enable override values for rx_ana_data_rate[3:0]
9	RW	0x0	rx_lbk_clk_en Override value for rx_ana_loopback_clk_en
8	RW	0x0	rx_ana_adaptation_en Override value for rx_ana_adaptation_en
7	RW	0x0	rx_ana_dfe_taps_en Override value for rx_ana_dfe_taps_en
6	RW	0x0	rx_ana_div4_en Override value for rx_ana_div4_en
5	RW	0x0	rx_ana_word_clk_en Override value for rx_ana_word_clk_en
4:1	RW	0x0	rx_ana_data_rate Override value for rx_ana_data_rate
0	RW	0x0	reserved Reserved

LANE1_DIG_ANA_RX_PWR_OVRD_OUT

Address: Operational Base + offset (0x11A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_ana_deserial_en_ovrd Enable override value for rx_ana_deserial_en
12	RW	0x0	rx_ana_cdr_en_ovrd Enable override value for rx_ana_cdr_en
11	RW	0x0	rx_ana_clk_en_ovrd Enable override value for rx_ana_clk_en
10	RW	0x0	rx_ana_clk_dcc_en_ovrd Enable override value for rx_ana_clk_dcc_en
9	RW	0x0	rx_ana_clk_vreg_en_ovrd Enable override value for rx_ana_clk_vreg_en
8	RW	0x0	rx_ana_afe_en_ovrd Enable override value for rx_ana_afe_en
7	RW	0x0	Reserve_0 Reserve_0
6	RW	0x0	rx_ana_deserial_en Override value for rx_ana_deserial_en
5	RW	0x0	rx_ana_cdr_en Override value for rx_ana_cdr_en
4	RW	0x0	rx_ana_clk_en Override value for rx_ana_clk_en

Bit	Attr	Reset Value	Description
3	RW	0x0	rx_ana_clk_dcc_en Override value for rx_ana_clk_dcc_en
2	RW	0x0	rx_ana_clk_vreg_en Override value for rx_ana_clk_vreg_en
1	RW	0x0	rx_ana_afe_en Override value for rx_ana_afe_en
0	RW	0x0	Reserve_1 Reserved

LANE1_DIG_ANA_RX_VCO_OVRD_OUT_0

Address: Operational Base + offset (0x11A9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_cdr_freq_tune_ovrd_en Enable override value for rx_ana_cdr_freq_tune
14	RW	0x0	rx_ana_vco_cntr_clk Override value for rx_ana_vco_cntr_clk
13	RW	0x0	rx_ana_vco_cntr_en Override value for rx_ana_vco_cntr_en
12:3	RW	0x000	rx_ana_cdr_freq_tune Override value for rx_ana_cdr_freq_tune
2	RW	0x0	rx_vco_cdr_ovrd_en Enable override values for cdr_vco_en and cdr_startup
1	RW	0x0	rx_ana_cdr_startup Override value for rx_ana_cdr_startup
0	RW	0x0	rx_ana_cdr_vco_en Override value for rx_ana_cdr_vco_en

LANE1_DIG_ANA_RX_VCO_OVRD_OUT_1

Address: Operational Base + offset (0x11AA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_cdr_vco_highfreq Override value for rx_ana_cdr_vco_highfreq
1	RW	0x1	rx_ana_vco_cntr_pd Override value for rx_ana_vco_cntr_pd
0	RW	0x0	rx_ana_cdr_vco_lowfreq Override value for rx_ana_cdr_vco_lowfreq

LANE1_DIG_ANA_RX_VCO_OVRD_OUT_2

Address: Operational Base + offset (0x11AB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	cdr_freq_tune_clk_self_clear_disable Disable self-clearing for the rx_ana_cdr_freq_tune_clk register
0	RW	0x0	rx_ana_cdr_freq_tune_clk Override value for rx_ana_cdr_freq_tune_clk - self-clearing to generate a pulse 1 cr_clk wide

LANE1_DIG_ANA_RX_CAL

Address: Operational Base + offset (0x11AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_ana_cal_comp_en Value for rx_ana_cal_comp_en
14:13	RW	0x0	rx_ana_cal_mode Value for rx_ana_cal_mode[1:0] 2'b00: Dual differential comparison ([vip2 - vim2] greater than [vip1 - vim1]) 2'b01: Differential comparison on input2 (vip2 greater than vim2) 2'b10: Single-ended comparison, negative node to negative node (vim1 greater than vim2) 2'b11: Common mode comparison (vcm2 greater than vcm1)
12	RW	0x0	rx_ana_slicer_cal_en Value for rx_ana_slicer_cal_en
11	RW	0x0	reserved Reserved
10	RW	0x0	rx_ana_cal_lpfbyp_en Value for rx_ana_cal_lpfbyp_en
9:5	RW	0x00	rx_ana_cal_muxb_sel Value for rx_ana_cal_muxb_sel[4:0]
4:0	RW	0x00	rx_ana_cal_muxa_sel Value for rx_ana_cal_muxa_sel[4:0]

LANE1_DIG_ANA_RX_DAC_CTRL

Address: Operational Base + offset (0x11AD)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	rx_ana_cal_dac_ctrl Value for rx_ana_cal_dac_ctrl[7:0]

LANE1_DIG_ANA_RX_DAC_CTRL_OVRD

Address: Operational Base + offset (0x11AE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_cal_dac_ctrl_ovrd Override enable for cal DAC control

LANE1_DIG_ANA_RX_DAC_CTRL_SEL

Address: Operational Base + offset (0x11AF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_ana_cal_dac_ctrl_sel Value for rx_ana_cal_dac_ctrl_sel[4:0]

LANE1_DIG_ANA_RX_AFE_ATT_VGA

Address: Operational Base + offset (0x11B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x0	rx_ana_afe_rate Value for rx_ana_afe_rate[1:0]
13:12	RW	0x3	rx_ana_afe_ctle_pole Value for rx_ana_afe_ctle_pole[1:0]
11	RW	0x0	rx_afe_rate_ovrd_en Override enable for rx_ana_afe_rate
10	RW	0x0	rx_ctle_pole_ovrd_en Override enable for rx_ana_ctle_pole
9	RW	0x0	rx_afe_gain_ovrd_en Override enable for rx_ana_afe_gain
8	RW	0x0	rx_afe_att_lvl_ovrd_en Override enable for rx_ana_afe_att_lvl
7	RW	0x0	rx_afe_update_ovrd_en Override enable for rx_ana_afe_update
6:3	RW	0x0	rx_ana_afe_gain Value for rx_ana_afe_gain[3:0]
2:0	RW	0x0	rx_ana_afe_att_lvl Value for rx_ana_afe_att_lvl[2:0]

LANE1_DIG_ANA_RX_AFE_CTLE

Address: Operational Base + offset (0x11B1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_afe_ctle_boost_ovrd_en Override enable for rx_ana_afe_ctle_boost
4:0	RW	0x00	rx_ana_afe_ctle_boost Value for rx_ana_afe_ctle_boost[4:0]

LANE1_DIG_ANA_RX_SCOPE

Address: Operational Base + offset (0x11B2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_scope_self_clear_disable Disable the self-clearing for rx_ana_scope_ph_clk register
12	RW	0x0	rx_ana_scope_clk_en Enable the scope clocks going to the scope slicer and the lane digital part
11:4	RW	0x00	rx_ana_scope_phase Sets value for rx_ana_scope_phase[7:0]
3	RW	0x0	rx_ana_scope_ph_clk Sets value for rx_ana_scope_ph_clk. This bit is self-clearing (i.e. only asserts for one cr_clk cycle)
2:1	RW	0x0	rx_ana_scope_sel Sets value for rx_ana_scope_sel 2'b00: AFE scope selected 2'b01: DFE even scope selected 2'b10: DFE odd scope selected 2'b11: DFE bypass/AFE buffer scope selected
0	RW	0x0	rx_ana_scope_en Sets value for rx_ana_scope_en

LANE1_DIG_ANA_RX_SLICER_CTRL
Address: Operational Base + offset (0x11B3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	rx_ana_slicer_ctrl_ovrd_en Override enable for RX ANA slicer ctrl
7:4	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE1_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST
Address: Operational Base + offset (0x11B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_ana_iq_phase_adjust Value for rx_ana_iq_phase_adjust[6:0]

LANE1_DIG_ANA_RX_ANA_IQ_SENSE_EN
Address: Operational Base + offset (0x11B5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_ana_iq_sense_en Value for rx_ana_iq_sense_en

LANE1_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN
Address: Operational Base + offset (0x11B6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	dac_ctrl_self_clear_disable Disable self-clearing for the rx_ana_cal_dac_ctrl_en register
0	RW	0x0	rx_ana_cal_dac_ctrl_en Value for rx_ana_cal_dac_ctrl_en. if DAC_CTRL_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE1_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE
Address: Operational Base + offset (0x11B7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	afe_update_self_clear_disable Disable self-clearing for the rx_ana_afe_update_en register

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_ana_afe_update_en Value for rx_ana_afe_update_en. if AFE_UPDATE_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE1_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK
Address: Operational Base + offset (0x11B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	phase_adjust_self_clear_disable Disable self-clearing for the rx_ana_iq_phase_adjust_clk register
0	RW	0x0	rx_ana_iq_phase_adjust_clk Value for rx_ana_iq_phase_adjust_clk. if PHASE_ADJUST_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE1_DIG_ANA_STATUS_0
Address: Operational Base + offset (0x11B9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RO	0x0	rx_ana_scope_data Value from ANA for rx_ana_scope_data
2	RO	0x0	rx_ana_cal_result Value from ANA for rx_ana_cal_result
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	tx_ana_loopback_en Value of tx_ana_loopback_en

LANE1_DIG_ANA_STATUS_1
Address: Operational Base + offset (0x11BA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_ana_vco_cntr Value from ANA for rx_ana_vco_cntr

LANE1_DIG_ANA_STATUS_LOS
Address: Operational Base + offset (0x11BB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RO	0x0	rx_ana_los_threshold Value to ANA for rx_ana_los_threshold
2	RO	0x0	rx_ana_los_en Value to ANA for rx_ana_los_en
1	RO	0x0	rx_ana_los_clk_en Value to ANA for rx_ana_los_clk_en

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_ana_los Value from ANA for rx_ana_los

LANE1_DIG_ANA_CREGS_TX_ANA_ATB_REG

Address: Operational Base + offset (0x11C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:3	RW	0x0	tx_ana_nc Reserved bit
2:1	RW	0x0	tx_ana_meas_atb BIST TX ATB measurement control
0	RW	0x0	tx_ana_meas_atb_en BIST TX ATB measurement enable

LANE1_DIG_ANA_CREGS_RX_ANA_EQ_CTRL

Address: Operational Base + offset (0x11C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x1	rx_ana_phdet_odd DFE sample control
4	RW	0x1	rx_ana_phdet_even DFE sample control
3:2	RW	0x1	rx_ana_ctle_offset_cal_enb EQ offset calibration enable
1:0	RW	0x0	rx_ana_afe_bias_mt EQ bias control

LANE1_DIG_ANA_CREGS_RX_ANA_VCO_CTRL

Address: Operational Base + offset (0x11C5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x1	rx_ana_cdr_vco_temp_comp_en VCO temperature compensation enable
1:0	RW	0x0	rx_ana_cdr_vco_startup_code VCO startup code

LANE1_DIG_ANA_CREGS_RX_ANA_VREG_CTRL

Address: Operational Base + offset (0x11C6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_vreg_ovrd_clk_vref VREG clk override reference voltage
4	RW	0x0	rx_ana_vreg_ovrd_vco_vref VREG VCO override reference voltage
3	RW	0x0	rx_ana_vreg_ovrd_vro_vref VREG VRO override reference voltage

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_ana_vreg_ovrd_cp_vref VREG charge-pump override reference voltage
1:0	RW	0x1	rx_ana_vreg_ring_ctrl VREG ring oscillator control

LANE1_DIG_ANA_CREGS_RX_ANA_DISCONNECT
Address: Operational Base + offset (0x11C7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_dc_path_disconnect TBA
1	RW	0x0	rx_ana_disconnect_m TBA
0	RW	0x0	rx_ana_disconnect_p TBA

LANE1_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL
Address: Operational Base + offset (0x11C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_ana_nc Reserved bits for future use

LANE1_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1
Address: Operational Base + offset (0x11C9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RW	0x0000	rx_meas_atb_14_0 Reserved
0	RW	0x0	rx_meas_atb_en rx_meas_atb_en

LANE1_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2
Address: Operational Base + offset (0x11CA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	rx_meas_atb_29_15 Reserved

LANE2_DIG_ASIC_LANE_OVRD_IN
Address: Operational Base + offset (0x1200)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_loopback_clk_en Loopback clock enable. When enabled the VCO clock of current lane is sent to the adjacent lane for TX BIST operation

Bit	Attr	Reset Value	Description
1	RW	0x0	Reserve_1 Reserve_1
0	RW	0x0	Reserve_0 Reserve_0

LANE2_DIG_ASIC_RX_ASIC_LOS
Address: Operational Base + offset (0x1201)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	los_en Value from asic for rx_los_en
14	RO	0x0	los_clk_en Value from asic for rx_los_clk_en
13:4	RO	0x000	los_timer_thresh Value from asic for rx_los_timer_thresh1
3:1	RO	0x0	los_threshold Value from asic for rx_los_threshold
0	RO	0x0	los Value of rx_los towards asic

LANE2_DIG_ASIC_LOS_OVRD_IN
Address: Operational Base + offset (0x1202)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	rx_los_ovrd Override enable for rx_los
8	RW	0x0	rx_los_r Override value for rx_los
7	RW	0x0	rx_los_threshold_ovrd Override enable for rx_los_threshold
6:4	RW	0x1	rx_los_threshold_r Override value for rx_los_threshold
3	RW	0x0	rx_los_clk_en_ovrd Override enable for rx_los_clk_en
2	RW	0x0	rx_los_clk_en_r Override value for rx_los_clk_en
1	RW	0x0	rx_los_en_ovrd Override enable for rx_los_en
0	RW	0x0	rx_los_en_r Override value for rx_los_en

LANE2_DIG_ASIC_LOS_OVRD_IN_1
Address: Operational Base + offset (0x1203)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RW	0x0	rx_los_timer_thresh_ovrd Override enable for rx_los_timer_thresh1
9:0	RW	0x05a	rx_los_timer_thresh_r Override value for rx_los_timer_thresh1

LANE2_DIG_ASIC_CDR_CONTROL_OVRD_IN
Address: Operational Base + offset (0x1206)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:1	RW	0x0	cdr_setting_sel Override values for CDR setting bits which select the CDR gain values
0	RW	0x0	cdr_setting_sel_ovrd_en Override enable for cdr_setting_sel signal

LANE2_DIG_ASIC_RX_OVRD_IN_0
Address: Operational Base + offset (0x1207)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:13	RW	0x0	rate_3_2 Override value for rx_rate[3:2]
12	RW	0x0	width_ovrd_en Enable override for rx_width
11:10	RW	0x0	width Override value for rx_width
9	RW	0x0	rate_ovrd_en Enable override value for rx_rate[1:0]
8:7	RW	0x0	rate_1_0 Override value for rx_rate
6	RW	0x0	pstate_ovrd_en Enable override value for rx_pstate
5:4	RW	0x0	pstate Override value for rx_pstate
3	RW	0x0	data_en_ovrd_en Enable override value for rx_data_en
2	RW	0x0	data_en Override value for rx_data_en
1	RW	0x0	req_ovrd_en Enable override value for rx_req
0	RW	0x0	req Override value for rx_req

LANE2_DIG_ASIC_RX_OVRD_IN_1
Address: Operational Base + offset (0x1208)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:10	RW	0x0	rx_clk_x2_en Override value for rx_clk_x2_en[2:0]
9	RW	0x0	rx_cdr_vco_highfreq Override value for rx_cdr_vco_highfreq
8	RW	0x0	rx_ref_ld_val_6 Override value for rx_ref_ld_val[6]
7	RW	0x0	en Enable override values for all inputs controlled by this register

Bit	Attr	Reset Value	Description
6	RW	0x0	rx_cdr_vco_lowfreq Override value for rx_cdr_vco_lowfreq
5:0	RW	0x14	rx_ref_ld_val_5_0 Override value for rx_ref_ld_val[5:0]

LANE2_DIG_ASIC_RX_OVRD_IN_2
Address: Operational Base + offset (0x1209)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	en Enable override values for all inputs controlled by this register
12:0	RW	0x03e8	rx_vco_ld_val Override value for rx_vco_ld_val

LANE2_DIG_ASIC_RX_OVRD_IN_3
Address: Operational Base + offset (0x120A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x00	reserved_14_to_10 Reserved_14_to_10
9	RW	0x0	disable_ovrd_en Enable override for rx_disable
8	RW	0x0	disable Override value for rx_disable
7	RW	0x0	clk_shift_ovrd_en Enable override for rx_clk_shift
6	RW	0x0	clk_shift Override value for rx_clk_shift
5	RW	0x0	align_en_ovrd_en Enable override for rx_align_en
4	RW	0x0	align_en Override value for rx_align_en
3	RW	0x0	cdr_ssc_en_ovrd_en Enable override value for rx_cdr_ssc_en
2	RW	0x0	cdr_ssc_en Override value for rx_cdr_ssc_en
1	RW	0x0	cdr_track_en_ovrd_en Enable override value for rx_cdr_track_en
0	RW	0x0	cdr_track_en Override value for rx_cdr_track_en

LANE2_DIG_ASIC_RX_OVRD_IN_4
Address: Operational Base + offset (0x120B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	adpt_ovrd_en Enable override for rx_adpt_dfe_en and rx_adpt_afe_en

Bit	Attr	Reset Value	Description
5	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
4	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
3	RW	0x0	invert_ovrd_en Enable override for rx_invert
2	RW	0x0	invert Override value for rx_invert
1	RW	0x0	lpd_ovrd_en Enable override for rx_lpd
0	RW	0x0	lpd Override value for rx_lpd

LANE2_DIG_ASIC_RX_OVRD_IN_5
Address: Operational Base + offset (0x120C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	reset_ovrd_en Enable override for rx_reset
0	RW	0x0	reset Override value for rx_reset

LANE2_DIG_ASIC_RX_OVRD_EQ_IN_0
Address: Operational Base + offset (0x120D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x06	eq_ctle_boost Override value for rx_eq_ctle_boost
10:7	RW	0x0	reserved Reserved
6:3	RW	0xf	eq_afe_gain Override value for rx_eq_afe_gain
2:0	RW	0x0	eq_att_lvl Override value for rx_eq_att_lvl

LANE2_DIG_ASIC_RX_OVRD_EQ_IN_1
Address: Operational Base + offset (0x120E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	eq_ovrd_en Enable override value for rx_eq_* inputs
14:7	RW	0x80	eq_dfe_tap1 Override value for rx_eq_dfe_tap1
6:0	RW	0x40	eq_dfe_tap2 Override value for rx_eq_dfe_tap2

LANE2_DIG_ASIC_RX_OVRD_OUT_0
Address: Operational Base + offset (0x120F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use

Bit	Attr	Reset Value	Description
8	RW	0x0	ana_ovl_det_0v_en Enable override for rx_ana_ovl_det_0v_i
7	RW	0x0	ana_ovl_det_0v Override value for rx_ana_ovl_det_0v_i
6	RW	0x0	adapt_sts_ovrd_en Enable override for rx_adapt_sts
5:4	RW	0x0	adapt_sts Override value for rx_adapt_sts
3	RW	0x0	rsv_0 Reserve_0
2	RW	0x0	rsv_1 Reserve_1
1	RW	0x0	ack_ovrd_en Enable override for rx_ack
0	RW	0x0	ack Override value for rx_ack

LANE2_DIG_ASIC_RX_ASIC_IN_0
Address: Operational Base + offset (0x1215)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_track_en Value from ASIC for rx_cdr_track_en
13	RO	0x0	adapt_dfe_en Value from ASIC for rx_adapt_dfe_en
12	RO	0x0	adapt_afe_en Value from ASIC for rx_adapt_afe_en
11	RO	0x0	reserved Reserved
10:9	RO	0x0	width Value from ASIC for rx_width
8:7	RO	0x0	rate_1_0 Value from ASIC for rx_rate[1:0]
6:5	RO	0x0	pstate Value from ASIC for rx_pstate
4	RO	0x0	lpd Value from ASIC for rx_lpd
3	RO	0x0	req Value from ASIC for rx_req
2	RO	0x0	data_en Value from ASIC for rx_data_en
1	RO	0x0	invert Value from ASIC for rx_invert
0	RO	0x0	reset Value from ASIC for rx_reset

LANE2_DIG_ASIC_RX_ASIC_IN_1
Address: Operational Base + offset (0x1216)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use

Bit	Attr	Reset Value	Description
9:8	RO	0x0	rate_3_2 Value from ASIC for rx_rate[3:2]
7	RO	0x0	reserved_7 Reserved_7
6:4	RO	0x0	reserved_6_to_4 Reserved_6_to_4
3	RO	0x0	disable Value from ASIC for rx_disable
2	RO	0x0	clk_shift Value from ASIC for rx_clk_shift
1	RO	0x0	align_en Value from ASIC for rx_align_en
0	RO	0x0	cdr_ssc_en Value from ASIC for rx_cdr_ssc_en

LANE2_DIG_ASIC_RX_EQ_ASIC_IN_0
Address: Operational Base + offset (0x1217)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
10:9	RO	0x0	rx_ana_afe_rate Value from ASIC for rx_ana_afe_rate
8:7	RO	0x0	rx_ana_afe_ctle_pole Value from ASIC for rx_ana_afe_ctle_pole
6:3	RO	0x0	eq_afe_gain Value from ASIC for rx_eq_afe_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

LANE2_DIG_ASIC_RX_EQ_ASIC_IN_1
Address: Operational Base + offset (0x1218)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:7	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1
6:0	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2

LANE2_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0
Address: Operational Base + offset (0x1219)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RO	0x0	rx_clk_x2_en Value from ASIC for rx_clk_x2_en[2:0]
8	RO	0x0	rx_cdr_vco_highfreq Value from ASIC for rx_cdr_vco_highfreq
7:1	RO	0x00	rx_ref_ld_val Value from ASIC for rx_ref_ld_val

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_cdr_vco_lowfreq Value from ASIC for rx_cdr_vco_lowfreq

LANE2_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1
Address: Operational Base + offset (0x121A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_vco_ld_val Value from ASIC for rx_vco_ld_val

LANE2_DIG_ASIC_RX_ASIC_OUT_0
Address: Operational Base + offset (0x121B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:3	RO	0x0	adapt_sts Value from PHY for rx_adapt_sts
2	RO	0x0	valid Value from PHY for rx_valid
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	ack Value from PHY for rx_ack

LANE2_DIG_LBERT_CTL
Address: Operational Base + offset (0x1220)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:5	RW	0x000	pat0 Pattern for modes 3-5
4	RW	0x0	trigger_err Insert a single error into a LSB any write of a 1 to this bit will insert an error
3:0	RW	0x0	mode Pattern to generate when changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: Fixed word (PAT0) 4'b1010: DC balanced word (PAT0, ~PAT0) 4'b1011: Fixed pattern: (000, PAT0, 3ff, ~PAT0) others: Reserved

LANE2_DIG_RX_CDR_CDR_CTL_0
Address: Operational Base + offset (0x1224)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:7	RW	0x0	dtb_sel Select to drive various signals onto the dtb 4'b0000: Disabled 4'b0001: Rx_pr_stable, rx_afe_stable from rx_ana_ctl 4'b0010: Com_good, com_bad from rx_align 4'b0011: Shift_in_prog, ana_odd_data from rx_align 4'b0100: 2 MSB's of XAUI align FSM state 4'b0101: 2 LSB's of XAUI align FSM state 4'b0110: Error_high, low from lbert_pm 4'b0111: Ana_los, los_filter from los block 4'b1000: Eios_state[0], eios_det from los block 4'b1001: Cdr_valid, MSB of FSM state from cdr_ctl 4'b1010: 2 LSB's of FSM state from cdr_ctl 4'b1011: Rx_dig_rst, rx_dig_en 4'b1100: Rx_ana_word_clk_i, rx_ana_dword_clk_i 4'b1101: Lbert_pg strobe others: Reserved
6	RW	0x0	always_realign Realign on any misaligned comma
5	RW	0x0	phdet_en_pr_mode Enable partial response phase detector mode
4	RW	0x0	phdet_pol Reverse polarity of phase error
3:2	RW	0x3	phdet_edge Edges to use for phase detection. 2'b00: Ignore all edges 2'b01: Use rising edges only 2'b10: Use both edges 2'b11: Use falling edges only
1:0	RW	0x3	phdet_en Enable phase detector. Top bit is odd slicers, bottom is even

LANE2_DIG_RX_CDR_CDR_CTL_1
Address: Operational Base + offset (0x1225)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RW	0x1c	ssc_off_cnt1 When SSC mode is disabled, the 12-bit word count in gain stage 1 is: (SSC_OFF_CNT1 * 4) in 20b mode (SSC_OFF_CNT1 * 5) in 16b mode
9:0	RW	0x039	ssc_off_cnt0 When SSC mode is disabled, the 12-bit word count in gain stage 0 is: (SSC_OFF_CNT0 * 4) in 20b mode (SSC_OFF_CNT0 * 5) in 16b mode

LANE2_DIG_RX_CDR_CDR_CTL_2
Address: Operational Base + offset (0x1226)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x25	ssc_on_cnt1 When SSC mode is enabled, the 12-bit word count in gain stage 1 is: (SSC_ON_CNT1 * 8) in 20b mode (SSC_ON_CNT1 * 10) in 16b mode
8:0	RW	0x0bb	ssc_on_cnt0 When SSC mode is enabled, the 12-bit word count in gain stage 0 is: (SSC_ON_CNT0 * 8) in 20b mode (SSC_ON_CNT0 * 10) in 16b mode

LANE2_DIG_RX_CDR_CDR_CTL_3
Address: Operational Base + offset (0x1227)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:10	RW	0x2	ssc_on_phug1 When SSC mode is enabled, the phug value in gain stage 1 is SSC_ON_PHUG1
9:6	RW	0x6	ssc_on_phug0 When SSC mode is enabled, the phug value in gain stage 0 is SSC_ON_PHUG0
5:3	RW	0x3	ssc_on_frug1 When SSC mode is enabled, the frug value in gain stage 1 is SSC_ON_FRUG1
2:0	RW	0x3	ssc_on_frug0 When SSC mode is enabled, the frug value in gain stage 0 is SSC_ON_FRUG0

LANE2_DIG_RX_CDR_CDR_CTL_4
Address: Operational Base + offset (0x1228)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:8	RW	0x0	frug_ovrd_value Override value for frug (frequency update gain) 3'b000: 0 3'b001: 1/16 LSB/update 3'b010: 1/8 LSB/update 3'b011: 1/4 LSB/update 3'b100: 1/2 LSB/update 3'b101: 1 LSB/update 3'b110: 2 LSB/update 3'b111: 4 LSB/update

Bit	Attr	Reset Value	Description
7:4	RW	0x0	phug_ovrd_value Override value for phug (phase update gain) : 4'b0000: 0 4'b0001: 1000 ppm 4'b0010: 2000 ppm 4'b0011: 3000 ppm 4'b0100: 4000 ppm 4'b0101: 5000 ppm 4'b0110: 6000 ppm 4'b0111: 7000 ppm 4'b1000: 8000 ppm 4'b1001: 9000 ppm 4'b1010: 10000 ppm 4'b1011: 11000 ppm 4'b1100: 12000 ppm 4'b1101: 13000 ppm 4'b1110: 14000 ppm 4'b1111: 15000 ppm
3	RW	0x0	ovrd_dpll_gain Override phug and frug values
2:0	RW	0x3	ssc_off_frug0 When SSC mode is disabled, the frug value in gain stage 0 is SSC_OFF_FRUG0

LANE2_DIG_RX_CDR_CDR_CTL_5

Address: Operational Base + offset (0x1229)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs3_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS3_FRUG1
8:6	RW	0x1	ssc_off_lbrs2_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS2_FRUG1
5:3	RW	0x1	ssc_off_lbrs1_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS1_FRUG1
2:0	RW	0x1	ssc_off_lbrs0_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS0_FRUG1

LANE2_DIG_RX_CDR_CDR_CTL_6

Address: Operational Base + offset (0x122A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs7_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS7_FRUG1
8:6	RW	0x3	ssc_off_lbrs6_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS6_FRUG1

Bit	Attr	Reset Value	Description
5:3	RW	0x3	ssc_off_lbrs5_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS5_FRUG1
2:0	RW	0x3	ssc_off_lbrs4_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS4_FRUG1

LANE2_DIG_RX_CDR_CDR_CTL_7
Address: Operational Base + offset (0x122B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x8	ssc_off_lbrs3_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS3_PHUG0
11:8	RW	0x7	ssc_off_lbrs2_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS2_PHUG0
7:4	RW	0x6	ssc_off_lbrs1_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS1_PHUG0
3:0	RW	0x6	ssc_off_lbrs0_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS0_PHUG0

LANE2_DIG_RX_CDR_CDR_CTL_8
Address: Operational Base + offset (0x122C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS7_PHUG0
11:8	RW	0xc	ssc_off_lbrs6_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS6_PHUG0
7:4	RW	0xc	ssc_off_lbrs5_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS5_PHUG0
3:0	RW	0xa	ssc_off_lbrs4_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS4_PHUG0

LANE2_DIG_RX_CDR_CDR_CTL_9
Address: Operational Base + offset (0x122D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x6	ssc_off_lbrs3_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS3_PHUG1
11:8	RW	0x4	ssc_off_lbrs2_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS2_PHUG1
7:4	RW	0x3	ssc_off_lbrs1_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS1_PHUG1

Bit	Attr	Reset Value	Description
3:0	RW	0x2	ssc_off_lbrs0_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS0_PHUG1

LANE2_DIG_RX_CDR_CDR_CTL_10

Address: Operational Base + offset (0x122E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS7_PHUG1
11:8	RW	0xc	ssc_off_lbrs6_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS6_PHUG1
7:4	RW	0xa	ssc_off_lbrs5_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS5_PHUG1
3:0	RW	0x8	ssc_off_lbrs4_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS4_PHUG1

LANE2_DIG_RX_CDR_STAT

Address: Operational Base + offset (0x122F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:4	RO	0x0	frug_value Notes: Current value for dpll_frug[2:0]
3:0	RO	0x0	phug_value Notes: Current value for dpll_phug[3:0]

LANE2_DIG_RX_PWRCTL_RX_PSTATE_P0

Address: Operational Base + offset (0x1240)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	rx_p0_dig_clk_en Enable/Disable RX digital clocks in P0
10	RW	0x1	rx_p0_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0, if RX_P0_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0_vco_cal_rst Enable/Disable resetting the RX VCO in P0
8	RW	0x0	rx_p0_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0
7	RW	0x1	rx_p0_ana_cdr_en Value of RX ana cdr_en in P0
6	RW	0x1	rx_p0_ana_deser_en Value of RX ana deserial_en in P0

Bit	Attr	Reset Value	Description
5	RW	0x1	rx_p0_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0
4	RW	0x1	rx_p0_ana_clk_en Value of RX ana clk_en in P0
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0
1	RW	0x1	rx_p0_ana_afe_en Value of RX ana afe_en in P0
0	RW	0x1	reserved_0 Reserved_0

LANE2_DIG_RX_PWRCTL_RX_PSTATE_P0S
Address: Operational Base + offset (0x1241)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p0s_dig_clk_en Enable/Disable RX digital clocks in P0S
10	RW	0x1	rx_p0s_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0S, if RX_P0S_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0s_vco_cal_rst Enable/Disable resetting the RX VCO in P0S
8	RW	0x0	rx_p0s_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0S
7	RW	0x0	rx_p0s_ana_cdr_en Value of RX ana cdr_en in P0S
6	RW	0x0	rx_p0s_ana_deser_en Value of RX ana deserial_en in P0S
5	RW	0x0	rx_p0s_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0S
4	RW	0x0	rx_p0s_ana_clk_en Value of RX ana clk_en in P0S
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0s_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0S
1	RW	0x1	rx_p0s_ana_afe_en Value of RX ana afe_en in P0S
0	RW	0x1	reserved_0 Reserved_0

LANE2_DIG_RX_PWRCTL_RX_PSTATE_P1
Address: Operational Base + offset (0x1242)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use

Bit	Attr	Reset Value	Description
11	RW	0x0	rx_p1_dig_clk_en Enable/Disable RX digital clocks in P1
10	RW	0x0	rx_p1_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P1, if RX_P1_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p1_vco_cal_rst Enable/Disable resetting the RX VCO in P1
8	RW	0x1	rx_p1_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P1
7	RW	0x0	rx_p1_ana_cdr_en Value of RX ana cdr_en in P1
6	RW	0x0	rx_p1_ana_deser_en Value of RX ana deserial_en in P1
5	RW	0x0	rx_p1_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P1
4	RW	0x0	rx_p1_ana_clk_en Value of RX ana clk_en in P1
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p1_ana_clk_vreg_en Value of RX ana clk_vreg_en in P1
1	RW	0x1	rx_p1_ana_afe_en Value of RX ana afe_en in P1
0	RW	0x1	reserved_0 Reserved_0

LANE2_DIG_RX_PWRCTL_RX_PSTATE_P2
Address: Operational Base + offset (0x1243)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p2_dig_clk_en Enable/Disable RX digital clocks in P2
10	RW	0x0	rx_p2_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P2, if RX_P2_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p2_vco_cal_rst Enable/Disable resetting the RX VCO in P2
8	RW	0x1	rx_p2_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P2
7	RW	0x0	rx_p2_ana_cdr_en Value of RX ana cdr_en in P2
6	RW	0x0	rx_p2_ana_deser_en Value of RX ana deserial_en in P2
5	RW	0x0	rx_p2_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P2
4	RW	0x0	rx_p2_ana_clk_en Value of RX ana clk_en in P2
3	RW	0x0	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_p2_ana_clk_vreg_en Value of RX ana clk_vreg_en in P2
1	RW	0x0	rx_p2_ana_afe_en Value of RX ana afe_en in P2
0	RW	0x1	reserved_0 Reserved_0

LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_0

Address: Operational Base + offset (0x1244)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x0f	rx_dpll_clock_switch_time Wait between switching rx_dpll clock from Rx_clk to ref_clk or vice-versa
4:0	RW	0x06	rx_state_3a_and_3b_time Wait between Power state 3A and 3B

LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_1

Address: Operational Base + offset (0x1245)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	fast_rx_vreg_en Enable fast RX VREG enable (simulation only)
12:7	RW	0x0d	rx_vreg_en_time Power up time (in ref_range cycles) for RX ana vreg enable (spec 500ns)
6	RW	0x0	fast_rx_afe_en Enable fast RX AFE enable (simulation only)
5:0	RW	0x1a	rx_afe_en_time Power up time (in ref_range cycles) for RX ana AFE enable (spec >=1us)

LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_2

Address: Operational Base + offset (0x1246)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	fast_rx_clk_en Enable fast RX clock enable (simulation only)
5:0	RW	0x1a	rx_clk_en_time Power up time (in ref_range cycles) for RX ana clk (or dcc) enable (spec >1us)

LANE2_DIG_RX_PWRCTL_RX_PWRUP_TIME_3

Address: Operational Base + offset (0x1247)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	rx_deser_dis_time Power down time in (ref_range cycles) for RX ana deserial enable

Bit	Attr	Reset Value	Description
13:12	RW	0x0	rx_deser_en_time Power up time (in ref_range cycles) for RX ana deserial enable
11:8	RW	0x0	rx_cdr_en_time Power up time (in ref_range cycles) for RX ana CDR (or dfe/dfe_taps) enable (spec 0ns)
7:2	RW	0x00	rsvd_3_7_2 Reserved
1:0	RW	0x0	rx_rate_time Power up time (in ref_range cycles) for RX ana rate or width change

LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0

Address: Operational Base + offset (0x1248)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RW	0x0	vcoclk_correct_update Update the vcoclk_correct
11:9	RW	0x2	int_gain_cal_bounce_cnt Number of bounces (i.e. direction changes) on the int_gain code before indicating that the RX VCO calibration is done
8:6	RW	0x0	int_gain_cal_cnt_shift Number of shifts to apply to ld_cnt inputs when performing int_gain code calibration
5	RW	0x0	int_gain_cal_fixed_cnt_en Enable a fixed count (instead of bounce count) for int_gain code calibration
4:0	RW	0x00	int_gain_cal_fixed_cnt Number of steps done during int_gain code calibration when INT_GAIN_CAL_FIXED_CNT_EN is enabled.

LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1

Address: Operational Base + offset (0x1249)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x00	dtb_sel DTB select for RX VCO dtb signals 7'h01: {chkfrq_en, ref_dig_clk} 7'h02: {rx_ana_cdr_vco_en_i, rx_ana_cdr_startup_i} 7'h04: {rx_vco_up, dpll_freq_rst} 7'h08: {rx_vco_contcal_en, rx_vco_cal_rst} 7'h10: {chkfrq_done, vcoclk_too_fast} 7'h20: {cal_dir, rx_vco_cal_done} 7'h40: {curr_state[0], rx_vco_cnt[0]} others: Reserved
8:5	RW	0x8	dpll_cal_ug DPLL calibration update on int_gain code 3'h0: 0 others: (1/16)*2^(DPLL_CAL_UG-1) LSB/update Maximum DPLL_CAL_UG=10, i.e. 32 LSB/update

Bit	Attr	Reset Value	Description
4	RW	0x0	disable_int_cal_mode When asserted, then the DPLL frequency register is never modified by the RX VCO calibration FSM (even, if DPLL_CAL_UG is non-zero). In this case, the calibration will always be performed on the VCO freq_tune code. This allows disabling of integral calibration feature, and hence only using freq_tune calibration.
3	RW	0x0	rx_vco_contcal_en Override value for the continuous calibration enable from the RX PWRSM
2	RW	0x0	rx_vco_cal_rst Override value for the calibration reset from the RX PWRSM
1	RW	0x0	rx_vco_freq_rst Override value for the frequency reset from the RX PWRSM
0	RW	0x0	rx_vco_ovrd_sel Override the calibration controls from the RX PWRSM

LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2

Address: Operational Base + offset (0x124A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_rx_vco_cal Skip RX VCO calibration altogether
14	RW	0x0	skip_rx_vco_freq_tune_cal Skip RX VCO coarse calibration
13:10	RW	0x9	freq_tune_cal_steps Number of cal steps of freq tune
9:0	RW	0x200	freq_tune_start_val Starting value of freq tune code

LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0

Address: Operational Base + offset (0x124B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	fast_rx_vco_wait Enable fast RX VCO power up (simulation only)
14:11	RW	0x6	rx_vco_cntr_pwrup_time Power up time (in ref_range cycles) for RX ana VCO cnter (spec >200ns)
10:7	RW	0x6	rx_vco_update_time Settle time (in ref_range cycles) for RX ana VCO update (freq_tune or int_gain) (spec >200ns)
6:0	RW	0x19	rx_vco_startup_time Power up time (in ref_range cycles) for RX ana VCO startup (spec >1us)

LANE2_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1

Address: Operational Base + offset (0x124C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use

Bit	Attr	Reset Value	Description
2:0	RW	0x3	rx_vco_cntr_settle_time RX VCO counter value settling time in (ref_dig_clk cycles) (spec: 3 ref_dig_clk cycle)

LANE2_DIG_RX_VCOCAL_RX_VCO_STAT_0

Address: Operational Base + offset (0x124D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	rx_ana_cdr_vco_en Current value of rx_ana_cdr_vco_en_i
12	RO	0x0	rx_ana_cdr_startup Current value of rx_ana_cdr_startup_i
11	RO	0x0	rx_ana_vco_cntr_en Current value of rx_ana_vco_cntr_en_i
10	RO	0x0	rx_ana_vco_cntr_pd Current value of rx_ana_vco_cntr_pd_i
9:0	RO	0x000	rx_ana_cdr_freq_tune Current value of rx_ana_cdr_freq_tune_i

LANE2_DIG_RX_VCOCAL_RX_VCO_STAT_1

Address: Operational Base + offset (0x124E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	dpll_freq_rst Indicates that the RX integral frequency is reset or not
7	RO	0x0	rx_vco_cal_done Indicates that the RX VCO has completed calibration
6	RO	0x0	rx_vco_contcal_en Value of the continuous calibration enable from the RX PWRSM
5	RO	0x0	rx_vco_cal_rst Value of the calibration reset from the RX PWRSM
4	RO	0x0	rx_vco_freq_rst Value of the RX VCO frequency reset from the RX PWRSM
3:0	RO	0x0	rx_vco_fsm_state Value of the RX VCO CAL FSM

LANE2_DIG_RX_VCOCAL_RX_VCO_STAT_2

Address: Operational Base + offset (0x124F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	rx_vco_up Indicates that the RX VCO is ready
14	RO	0x0	rx_vco_correct Indicates that the RX VCO clock has the correct frequency
13	RO	0x0	vcoclk_too_fast Indicates that the RX VCO clock frequency is too fast
12:0	RO	0x0000	vco_cntr_final Value of RX VCO counter when refclk counter expired

LANE2_DIG_RX_RX_ALIGN_XAUI_COMM_MASK

Address: Operational Base + offset (0x1250)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x3ff	xaui_comm_mask XAUI_COMMA mask. For 10-bit COMMA set the mask to 0x3FF and for 7-bit COMMA set the mask to 0x3F8

LANE2_DIG_RX_LBERT_CTL

Address: Operational Base + offset (0x1251)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	sync Synchronize pattern matcher LFSR with incoming data A write of a one to this bit will reset the error counter and start a synchronization of the PM, there is no need to write this back to zero to run normally.
3:0	RW	0x0	mode Pattern to match When changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: D[n] = d[n-10] 4'b1010: D[n] = !d[n-10] 4'b1011: D[n] = !d[n-20] others: Reserved

LANE2_DIG_RX_LBERT_ERR

Address: Operational Base + offset (0x1252)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ov14 If active, multiply count by 128. if OV14=1 and count=2^15-1, signals overflow of counter (2 reads needed to read value)
14:0	RW	0x0000	count A read of this register, or a sync of the PM resets the error count. Current error count, if OV14 field is active, then multiply count by 128 (2 reads needed to read value)

LANE2_DIG_RX_RX_LOS_LOS_0

Address: Operational Base + offset (0x1253)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use

Bit	Attr	Reset Value	Description
8	RW	0x0	rx_los_filt_byp Bypass digital LOS filter
7:3	RW	0x0c	rx_los_t_thresh0_r LOS timer0 threshold to count presence of zeros on rx_los
2:0	RW	0x2	rx_los_wait_r Initial wait time for rx_los after rx_los_en is asserted

LANE2_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS

Address: Operational Base + offset (0x1255)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_pwrsm_state Value for rx_pwrsm_state

LANE2_DIG_RX_DPLL_FREQ

Address: Operational Base + offset (0x125C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:0	RW	0x2000	val Freq is 125*VAL ppm from the reference (2 reads needed to read value)

LANE2_DIG_RX_DPLL_FREQ_BOUND_0

Address: Operational Base + offset (0x125D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:1	RW	0x264	upper_freq_bound Upper frequency bound in terms of LSBs of the integral control code
0	RW	0x0	freq_bound_en Enable the frequency bounds feature

LANE2_DIG_RX_DPLL_FREQ_BOUND_1

Address: Operational Base + offset (0x125E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x19c	lower_freq_bound Lower frequency bound in terms of LSBs of the integral control code

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_0

Address: Operational Base + offset (0x1260)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	adpt_clk_div4_en Set the adaptation clock to be divided by 4 (default is div2)

Bit	Attr	Reset Value	Description
14	RW	0x0	start_asm1 Start adaptation state machine #1 (VGA, CTLE, DFE, EYEH) This register-bit is self-clearing
13:10	RW	0x3	n_tgg_asm1 Number of toggle loop iterations for ASM1
9:0	RW	0x010	n_top_asm1 Number of top level loop iterations for ASM1

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_1

Address: Operational Base + offset (0x1261)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	ctle_pole_ovrd_en Override CTLE pole value (only valid, if adaptation is run)
10:8	RW	0x0	ctle_pole_ovrd_val CTLE pole override value to load at start of adaptation
7	RW	0x0	fast_afe_dfe_settle Enable fast AFE and DFE settling time (simulation only)
6:0	RW	0x09	n_wait_asm1 Number of wait cycles for adaptation SM #1

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_2

Address: Operational Base + offset (0x1262)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x06	tgg_pttrn_1 Pattern for the second toggle loop error slicer is moved upward by data tap1, if this pattern is matched
4:0	RW	0x02	tgg_pttrn_0 Pattern for the first toggle loop error slicer is moved downward by data tap1, if this pattern is matched

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_3

Address: Operational Base + offset (0x1263)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	esl_twice_dsl Assert, if error slicer has twice the voltage range as the data slicer (for the same 8 bits).
14	RW	0x0	tgg_en Enable toggling of the error slicer
13	RW	0x0	eyeho_en Enable eye height measurement using odd error slicer
12	RW	0x0	eyehe_en Enable eye height measurement using even error slicer
11:7	RW	0x00	dfe_en Enable DFE adaptation for taps 5-1
6	RW	0x0	att_en Enable ATT adaptation

Bit	Attr	Reset Value	Description
5	RW	0x0	vga_en Enable VGA adaptation
4:0	RW	0x00	ctle_en Enable CTLE boost adaptation, the five bits determine which correlators are used to adapt the CTLE

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_4
Address: Operational Base + offset (0x1264)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	dfe2_th DFE Tap2 correlation decision threshold (2^N-1)
11:8	RW	0x0	dfe1_th DFE Tap1 correlation decision threshold (2^N-1)
7:4	RW	0x0	vga_th VGA correlation decision threshold (2^N-1), During eye height measurement, the VGA_TH is repurposed for error slicer updates.
3:0	RW	0x0	ctle_th CTLE correlation decision threshold (2^N-1)

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_5
Address: Operational Base + offset (0x1265)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	th_offset Apply an offset to the decision threshold
11:8	RW	0x0	dfe5_th DFE Tap5 correlation decision threshold (2^N-1)
7:4	RW	0x0	dfe4_th DFE Tap4 correlation decision threshold (2^N-1)
3:0	RW	0x0	dfe3_th DFE Tap3 correlation decision threshold (2^N-1)

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_6
Address: Operational Base + offset (0x1266)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RW	0x3	att_low_th ATT low threshold
12	RW	0x1	vga_sat_cnt_sticky If deasserted, then VGA saturation counts must be consecutive to change ATT
11:9	RW	0x4	vga_sat_cnt VGA saturation count
8:6	RW	0x4	att_mu ATT gain code update gain (2^N)
5:3	RW	0x5	vga_mu VGA gain code update gain (2^N). During eye height measurement, the VGA_MU is repurposed for error slicer updates.
2:0	RW	0x3	ctle_mu CTLE boost code update gain (2^N)

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_7
Address: Operational Base + offset (0x1267)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x10	vga_lev_low VGA level low saturation limit
9:5	RW	0x1a	vga_lev_high VGA level high saturation limit
4:0	RW	0x02	vga_min_sat VGA minimum saturation limit

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_8
Address: Operational Base + offset (0x1268)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x4	dfe5_mu DFE tap5 code update gain (2^N)
11:9	RW	0x4	dfe4_mu DFE tap4 code update gain (2^N)
8:6	RW	0x4	dfe3_mu DFE tap3 code update gain (2^N)
5:3	RW	0x4	dfe2_mu DFE tap2 code update gain (2^N)
2:0	RW	0x5	dfe1_mu DFE tap1 code update gain (2^N)

LANE2_DIG_RX_ADPTCTL_ADPT_CFG_9
Address: Operational Base + offset (0x1269)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	err_slo_adpt_init The error odd slicer is initialized to this value at the start of a new adaptation request.
7:0	RW	0x00	err_sle_adpt_init The error even slicer is initialized to this value at the start of a new adaptation request.

LANE2_DIG_RX_ADPTCTL_RST_ADPT_CFG
Address: Operational Base + offset (0x126A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x1	rst_adpt_tap1 Reset data Tap1 when turning off DFE adaptation (taps 2-5 are always turned off when DFE adaptation is turned off)
3	RW	0x1	rst_adpt_ctle_pole Reset CTLE pole when turning off AFE adaptation
2	RW	0x1	rst_adpt_ctle_boost Reset CTLE boost when turning off AFE adaptation

Bit	Attr	Reset Value	Description
1	RW	0x1	rst_adpt_vga Reset VGA when turning off AFE adaptation
0	RW	0x1	rst_adpt_att Reset ATT when turning off AFE adaptation

LANE2_DIG_RX_ADPTCTL_ATT_STATUS
Address: Operational Base + offset (0x126B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	asm1_don Asserts when adaptation state machine #1 is done
7:0	RO	0x00	att_adpt_code Value of ATT adaptation code

LANE2_DIG_RX_ADPTCTL_VGA_STATUS
Address: Operational Base + offset (0x126C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
9:0	RO	0x000	vga_adpt_code Value of VGA adaptation code

LANE2_DIG_RX_ADPTCTL_CTLE_STATUS
Address: Operational Base + offset (0x126D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:10	RO	0x0	ctle_pole_adpt_code Value of CTLE pole adaptation code
9:0	RO	0x000	ctle_boost_adpt_code Value of CTLE boost adaptation code

LANE2_DIG_RX_ADPTCTL_DFE_TAP1_STATUS
Address: Operational Base + offset (0x126E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:0	RO	0x0000	dfe_tap1_adpt_code Value of DFE tap1 adaptation code

LANE2_DIG_RX_ADPTCTL_DFE_TAP2_STATUS
Address: Operational Base + offset (0x126F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap2_adpt_code Value of DFE tap2 adaptation code

LANE2_DIG_RX_ADPTCTL_DFE_TAP3_STATUS

Address: Operational Base + offset (0x1270)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap3_adpt_code Value of DFE tap3 adaptation code

LANE2_DIG_RX_ADPTCTL_DFE_TAP4_STATUS

Address: Operational Base + offset (0x1271)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap4_adpt_code Value of DFE tap4 adaptation code

LANE2_DIG_RX_ADPTCTL_DFE_TAP5_STATUS

Address: Operational Base + offset (0x1272)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap5_adpt_code Value of DFE tap5 adaptation code

LANE2_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1273)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_vdac_ofst Offset value for DFE data even vDAC

LANE2_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST

Address: Operational Base + offset (0x1274)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_vdac_ofst Offset value for DFE data odd vDAC

LANE2_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN

Address: Operational Base + offset (0x1275)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE2_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD

Address: Operational Base + offset (0x1276)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

LANE2_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1277)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

LANE2_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST

Address: Operational Base + offset (0x1278)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

LANE2_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL

Address: Operational Base + offset (0x1279)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	e_sle_lvl Even error slicer level
7:0	RO	0x00	e_slo_lvl Odd error slicer level

LANE2_DIG_RX_ADPTCTL_ADPT_RESET

Address: Operational Base + offset (0x127A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	reset_asm1 Resets adaptation state machine (ASM1) as well as the stats capture block. This is a self-clearing bit, and requires re-start of ASM1.

LANE2_DIG_RX_STAT_LD_VAL_1

Address: Operational Base + offset (0x1280)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sc1_start Start sample counter #1 this is a self-clearing bit
14:0	RW	0x0040	sc1_ld_val Sample counter #1 load value

LANE2_DIG_RX_STAT_DATA_MSK

Address: Operational Base + offset (0x1281)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	data_msk_15_0 Value of data_msk_r[15:0]

LANE2_DIG_RX_STAT_MATCH_CTL0

Address: Operational Base + offset (0x1282)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	scope_dly For clock cycle delays on scope_data_rx_clk, an additional MSB is added in SCOPE_DLY_2
13:10	RW	0xf	data_msk_19_16 Value of data_msk_r[19:16]
9:5	RW	0x00	pttrn_cr1a_4_0 Value of pattern A for 1st correlator (bits 4:0)
4:0	RW	0x06	pttrn_msk_cr1a_4_0 Value of pattern A mask for 1st correlator (bits 4:0)

LANE2_DIG_RX_STAT_MATCH_CTL1

Address: Operational Base + offset (0x1283)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	pttrn_cr1a_adpt_en Enable ORing of adapation pattern with pattern CR1A
10:6	RW	0x00	pttrn_cr1b_4_0 Value of pattern B for 1st correlator (bits 4:0)
5:1	RW	0x00	pttrn_msk_cr1b_4_0 Value of pattern B mask for 1st correlator (bits 4:0)
0	RW	0x0	pttrn_cr1b_en Enable pattern B matching for 1st correlator

LANE2_DIG_RX_STAT_STAT_CTL0

Address: Operational Base + offset (0x1284)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_en Value of skip_en_r
14	RW	0x1	sc_timer_mode Sample counter operation mode 1'b0: Counts number of matched samples 1'b1: Counts clock cycles (i.e. a timer)
13	RW	0x0	stat_rxclk_sel Select stat clock 1'b0: Ref_range_clk 1'b1: Rx_dig_clk (i.e. RX dword clk) Before changing stat_rxclk_sel_r from 1->0, the rx_dig_clk must be active (i.e. enabled)
12:10	RW	0x0	stat_src_sel Select stat source input 3'b000: {20{rx_cal_result}} 3'b001: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 3'b010: Rx_phase[39:0] 3'b011: Rx_error[39:0] 3'b100: Rx_data[39:0] 3'b101: Rx_phdir[39:0] 3'b110: 40'hFF_FFFF_FFFF others: Reserved
9:6	RW	0x0	stat_shft_sel Select stat source shift value 4'b0000: Correlate N-1 -> N+3 (use N for offset calibration) 4'b0001: Correlate N+1 -> N+5 (for taps1-5) 4'b0010: Correlate N+6 -> N+10 4'b0011: Correlate N+11 -> N+15 4'b0100: Correlate N+16 -> N+20 4'b0101: Correlate N+21 -> N+25 4'b0110: Correlate N+26 -> N+30 4'b0111: Correlate N+31 -> N+35 4'b1000: Correlate N+36 -> N+39 others: Reserved Setting 0x8 is only used in 20b mode (for checking corr on bits 36-39)
5	RW	0x0	corr_mode_en Enable correlation mode
4:3	RW	0x0	corr_src_sel Select correlation input source 2'b00: Rx_error[39:0] 2'b01: Rx_phase[39:0] 2'b10: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 2'b11: No correlation
2	RW	0x0	corr_shft_sel Select shift for phase. 1'b0: None 1'b1: >>1
1	RW	0x0	corr_shft_sel_vga Select shift for error going to VGA. 1'b0: None 1'b1: >>1

Bit	Attr	Reset Value	Description
0	RW	0x0	reserved_0 Reserved bit

LANE2_DIG_RX_STAT_STAT_CTL1

Address: Operational Base + offset (0x1285)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	vld_ctl Gating configuration of stats collection 2'b00: Ignore both cdr_valid and rx_valid 2'b01: Gate stats collection with cdr_valid 2'b10: Gate stats collection with rx_valid 2'b11: Ignore both cdr_valid and rx_valid
13	RW	0x0	vld_loss_clr Clearing of stats collection upon loss of valid 1'b0: Hold sample and stat counters 1'b1: Clear sample and stat counters
12:11	RW	0x0	data_dly_sel For clock cycle delays on rx_data[19:0], an additional MSB is added in data_dly_sel_2
10	RW	0x0	stat_clk_en Clock gate enable for stat clock
9	RW	0x0	sc_pause Pause the sample counter and stat counters
8:7	RW	0x0	reserved_8_7 Reserved bits
6	RW	0x0	stat_cnt_6_en Enable for stat counter 6
5	RW	0x0	stat_cnt_5_en Enable for stat counter 5
4	RW	0x0	stat_cnt_4_en Enable for stat counter 4
3	RW	0x1	stat_cnt_3_en Enable for stat counter 3 only counter to be enabled by default, since used for offset calibration
2	RW	0x0	stat_cnt_2_en Enable for stat counter 2
1	RW	0x0	stat_cnt_1_en Enable for stat counter 1
0	RW	0x0	stat_cnt_0_en Enable for stat counter 0

LANE2_DIG_RX_STAT_SMPL_CNT1

Address: Operational Base + offset (0x1286)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	smpl_cnt1 Current value of sample counter #1

LANE2_DIG_RX_STAT_STAT_CNT_0

Address: Operational Base + offset (0x1287)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_0 Current value of stat counter #0

LANE2_DIG_RX_STAT_STAT_CNT_1
Address: Operational Base + offset (0x1288)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_1 Current value of stat counter #1

LANE2_DIG_RX_STAT_STAT_CNT_2
Address: Operational Base + offset (0x1289)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_2 Current value of stat counter #2

LANE2_DIG_RX_STAT_STAT_CNT_3
Address: Operational Base + offset (0x128A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_3 Current value of stat counter #3

LANE2_DIG_RX_STAT_STAT_CNT_4
Address: Operational Base + offset (0x128B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_4 Current value of stat counter #4

LANE2_DIG_RX_STAT_STAT_CNT_5
Address: Operational Base + offset (0x128C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_5 Current value of stat counter #5

LANE2_DIG_RX_STAT_STAT_CNT_6
Address: Operational Base + offset (0x128D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_6 Current value of stat counter #6

LANE2_DIG_RX_STAT_CAL_COMP_CLK_CTL

Address: Operational Base + offset (0x128E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RW	0x3	ref_div_cnt Ref range clock count (e.g. 5'd3 = 4 ref_range cycles)
2:0	RW	0x1	prechrge_cnt Precharge count (e.g. 5'd1 = 2 ref_range cycles)

LANE2_DIG_RX_STAT_MATCH_CTL2

Address: Operational Base + offset (0x128F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1a_19_5 Value of pattern A for 1st correlator (bits 19:5)

LANE2_DIG_RX_STAT_MATCH_CTL3

Address: Operational Base + offset (0x1290)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1a_19_5 Value of pattern A mask for 1st correlator (bits 19:5)

LANE2_DIG_RX_STAT_MATCH_CTL4

Address: Operational Base + offset (0x1291)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1b_19_5 Value of pattern B for 1st correlator (bits 19:5)

LANE2_DIG_RX_STAT_MATCH_CTL5

Address: Operational Base + offset (0x1292)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1b_19_5 Value of pattern B mask for 1st correlator (bits 19:5)

LANE2_DIG_RX_STAT_STAT_CTL2

Address: Operational Base + offset (0x1293)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	scope_dly_2 Additional MSB bit for SCOPE_DLY to extend the delay range to 0->7
0	RW	0x0	data_dly_sel_2 Additional MSB bit for data_dly_sel to extend the delay range to 0->7

LANE2_DIG_RX_STAT_STAT_STOP

Address: Operational Base + offset (0x1294)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	sc1_stop Stop sample counters #1 and associated stat counters. This is a self-clearing bit, and requires re-start of sample counter #1.

LANE2_DIG_ANA_TX_OVRD_OUT

Address: Operational Base + offset (0x12A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	tx_ovrd_en Enable override values for all outputs controlled by this register
0	RW	0x0	tx_ana_reset Override value for tx_ana_reset

LANE2_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT

Address: Operational Base + offset (0x12A1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	tx_ana_lpbk_dfe_mode Value for tx_ana_lpbk_dfe_mode

LANE2_DIG_ANA_RX_DIV_OVRD_OUT

Address: Operational Base + offset (0x12A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_ana_div5_en Override value for rx_ana_div5_en
0	RW	0x0	rx_ana_div13p5_en Override value for rx_ana_div13p5_en

LANE2_DIG_ANA_RX_CTL_OVRD_OUT

Address: Operational Base + offset (0x12A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_lbk_clk_en_ovrd Enable override value for rx_ana_loopback_clk_en
14	RW	0x0	rx_ana_adaptation_en_ovrd Enable override value for rx_ana_adaptation_en
13	RW	0x0	rx_ana_dfe_taps_en_ovrd Enable override value for rx_ana_dfe_taps_en
12	RW	0x0	rx_ana_div4_en_ovrd Enable override value for rx_ana_div4_en
11	RW	0x0	rx_ana_word_clk_en_ovrd Enable override value for rx_ana_word_clk_en
10	RW	0x0	rx_ana_data_rate_en_ovrd Enable override values for rx_ana_data_rate[3:0]
9	RW	0x0	rx_lbk_clk_en Override value for rx_ana_loopback_clk_en
8	RW	0x0	rx_ana_adaptation_en Override value for rx_ana_adaptation_en
7	RW	0x0	rx_ana_dfe_taps_en Override value for rx_ana_dfe_taps_en
6	RW	0x0	rx_ana_div4_en Override value for rx_ana_div4_en
5	RW	0x0	rx_ana_word_clk_en Override value for rx_ana_word_clk_en
4:1	RW	0x0	rx_ana_data_rate Override value for rx_ana_data_rate
0	RW	0x0	reserved

LANE2_DIG_ANA_RX_PWR_OVRD_OUT

Address: Operational Base + offset (0x12A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_ana_deserial_en_ovrd Enable override value for rx_ana_deserial_en
12	RW	0x0	rx_ana_cdr_en_ovrd Enable override value for rx_ana_cdr_en
11	RW	0x0	rx_ana_clk_en_ovrd Enable override value for rx_ana_clk_en
10	RW	0x0	rx_ana_clk_dcc_en_ovrd Enable override value for rx_ana_clk_dcc_en
9	RW	0x0	rx_ana_clk_vreg_en_ovrd Enable override value for rx_ana_clk_vreg_en
8	RW	0x0	rx_ana_afe_en_ovrd Enable override value for rx_ana_afe_en
7	RW	0x0	Reserve_0 Reserve_0
6	RW	0x0	rx_ana_deserial_en Override value for rx_ana_deserial_en
5	RW	0x0	rx_ana_cdr_en Override value for rx_ana_cdr_en
4	RW	0x0	rx_ana_clk_en Override value for rx_ana_clk_en

Bit	Attr	Reset Value	Description
3	RW	0x0	rx_ana_clk_dcc_en Override value for rx_ana_clk_dcc_en
2	RW	0x0	rx_ana_clk_vreg_en Override value for rx_ana_clk_vreg_en
1	RW	0x0	rx_ana_afe_en Override value for rx_ana_afe_en
0	RW	0x0	Reserve_1 Reserve_1

LANE2_DIG_ANA_RX_VCO_OVRD_OUT_0

Address: Operational Base + offset (0x12A9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_cdr_freq_tune_ovrd_en Enable override value for rx_ana_cdr_freq_tune
14	RW	0x0	rx_ana_vco_cntr_clk Override value for rx_ana_vco_cntr_clk
13	RW	0x0	rx_ana_vco_cntr_en Override value for rx_ana_vco_cntr_en
12:3	RW	0x000	rx_ana_cdr_freq_tune Override value for rx_ana_cdr_freq_tune
2	RW	0x0	rx_vco_cdr_ovrd_en Enable override values for cdr_vco_en and cdr_startup
1	RW	0x0	rx_ana_cdr_startup Override value for rx_ana_cdr_startup
0	RW	0x0	rx_ana_cdr_vco_en Override value for rx_ana_cdr_vco_en

LANE2_DIG_ANA_RX_VCO_OVRD_OUT_1

Address: Operational Base + offset (0x12AA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_cdr_vco_highfreq Override value for rx_ana_cdr_vco_highfreq
1	RW	0x1	rx_ana_vco_cntr_pd Override value for rx_ana_vco_cntr_pd
0	RW	0x0	rx_ana_cdr_vco_lowfreq Override value for rx_ana_cdr_vco_lowfreq

LANE2_DIG_ANA_RX_VCO_OVRD_OUT_2

Address: Operational Base + offset (0x12AB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	cdr_freq_tune_clk_self_clear_disable Disable self-clearing for the rx_ana_cdr_freq_tune_clk register
0	RW	0x0	rx_ana_cdr_freq_tune_clk Override value for rx_ana_cdr_freq_tune_clk, self-clearing to generate a pulse 1 cr_clk wide

LANE2_DIG_ANA_RX_CAL

Address: Operational Base + offset (0x12AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_ana_cal_comp_en Value for rx_ana_cal_comp_en
14:13	RW	0x0	rx_ana_cal_mode Value for rx_ana_cal_mode[1:0] 2'b00: Dual differential comparison ([vip2 - vim2] greater than [vip1 - vim1]) 2'b01: Differential comparison on input2 (vip2 greater than vim2) 2'b10: Single-ended comparison, negative node to negative node (vim1 greater than vim2) 2'b11: Common mode comparison (vcm2 greater than vcm1)
12	RW	0x0	rx_ana_slicer_cal_en Value for rx_ana_slicer_cal_en
11	RW	0x0	reserved Reserved
10	RW	0x0	rx_ana_cal_lpfbyp_en Value for rx_ana_cal_lpfbyp_en
9:5	RW	0x00	rx_ana_cal_muxb_sel Value for rx_ana_cal_muxb_sel[4:0]
4:0	RW	0x00	rx_ana_cal_muxa_sel Value for rx_ana_cal_muxa_sel[4:0]

LANE2_DIG_ANA_RX_DAC_CTRL

Address: Operational Base + offset (0x12AD)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	rx_ana_cal_dac_ctrl Value for rx_ana_cal_dac_ctrl[7:0]

LANE2_DIG_ANA_RX_DAC_CTRL_OVRD

Address: Operational Base + offset (0x12AE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_cal_dac_ctrl_ovrd Override enable for cal DAC control

LANE2_DIG_ANA_RX_DAC_CTRL_SEL

Address: Operational Base + offset (0x12AF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_ana_cal_dac_ctrl_sel Value for rx_ana_cal_dac_ctrl_sel[4:0]

LANE2_DIG_ANA_RX_AFE_ATT_VGA

Address: Operational Base + offset (0x12B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x0	rx_ana_afe_rate Value for rx_ana_afe_rate[1:0]
13:12	RW	0x3	rx_ana_afe_ctle_pole Value for rx_ana_afe_ctle_pole[1:0]
11	RW	0x0	rx_afe_rate_ovrd_en Override enable for rx_ana_afe_rate
10	RW	0x0	rx_ctle_pole_ovrd_en Override enable for rx_ana_ctle_pole
9	RW	0x0	rx_afe_gain_ovrd_en Override enable for rx_ana_afe_gain
8	RW	0x0	rx_afe_att_lvl_ovrd_en Override enable for rx_ana_afe_att_lvl
7	RW	0x0	rx_afe_update_ovrd_en Override enable for rx_ana_afe_update
6:3	RW	0x0	rx_ana_afe_gain Value for rx_ana_afe_gain[3:0]
2:0	RW	0x0	rx_ana_afe_att_lvl Value for rx_ana_afe_att_lvl[2:0]

LANE2_DIG_ANA_RX_AFE_CTLE

Address: Operational Base + offset (0x12B1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_afe_ctle_boost_ovrd_en Override enable for rx_ana_afe_ctle_boost
4:0	RW	0x00	rx_ana_afe_ctle_boost Value for rx_ana_afe_ctle_boost[4:0]

LANE2_DIG_ANA_RX_SCOPE

Address: Operational Base + offset (0x12B2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_scope_self_clear_disable Disable the self-clearing for rx_ana_scope_ph_clk register
12	RW	0x0	rx_ana_scope_clk_en Enable the scope clocks going to the scope slicer and the lane digital part
11:4	RW	0x00	rx_ana_scope_phase Sets value for rx_ana_scope_phase[7:0]
3	RW	0x0	rx_ana_scope_ph_clk Sets value for rx_ana_scope_ph_clk. This bit is self-clearing (i.e. only asserts for one cr_clk cycle)
2:1	RW	0x0	rx_ana_scope_sel Sets value for rx_ana_scope_sel 2'b00: AFE scope selected 2'b01: DFE even scope selected 2'b10: DFE odd scope selected 2'b11: DFE bypass/AFE buffer scope selected
0	RW	0x0	rx_ana_scope_en Sets value for rx_ana_scope_en

LANE2_DIG_ANA_RX_SLICER_CTRL
Address: Operational Base + offset (0x12B3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	rx_ana_slicer_ctrl_ovrd_en Override enable for RX ANA slicer ctrl
7:4	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE2_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST
Address: Operational Base + offset (0x12B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_ana_iq_phase_adjust Value for rx_ana_iq_phase_adjust[6:0]

LANE2_DIG_ANA_RX_ANA_IQ_SENSE_EN
Address: Operational Base + offset (0x12B5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_ana_iq_sense_en Value for rx_ana_iq_sense_en

LANE2_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN
Address: Operational Base + offset (0x12B6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	dac_ctrl_self_clear_disable Disable self-clearing for the rx_ana_cal_dac_ctrl_en register
0	RW	0x0	rx_ana_cal_dac_ctrl_en Value for rx_ana_cal_dac_ctrl_en, if DAC_CTRL_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE2_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE
Address: Operational Base + offset (0x12B7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	afe_update_self_clear_disable Disable self-clearing for the rx_ana_afe_update_en register

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_ana_afe_update_en Value for rx_ana_afe_update_en, if AFE_UPDATE_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE2_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK
Address: Operational Base + offset (0x12B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	phase_adjust_self_clear_disable Disable self-clearing for the rx_ana_iq_phase_adjust_clk register
0	RW	0x0	rx_ana_iq_phase_adjust_clk Value for rx_ana_iq_phase_adjust_clk, if PHASE_ADJUST_SELF_CLEAR_DISABLE=0, then this bit is self-clearing(i.e. only asserts for one cr_clk cycle)

LANE2_DIG_ANA_STATUS_0
Address: Operational Base + offset (0x12B9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RO	0x0	rx_ana_scope_data Value from ANA for rx_ana_scope_data
2	RO	0x0	rx_ana_cal_result Value from ANA for rx_ana_cal_result
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	tx_ana_loopback_en Value of tx_ana_loopback_en

LANE2_DIG_ANA_STATUS_1
Address: Operational Base + offset (0x12BA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_ana_vco_cntr Value from ANA for rx_ana_vco_cntr

LANE2_DIG_ANA_STATUS_LOS
Address: Operational Base + offset (0x12BB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RO	0x0	rx_ana_los_threshold Value to ANA for rx_ana_los_threshold
2	RO	0x0	rx_ana_los_en Value to ANA for rx_ana_los_en
1	RO	0x0	rx_ana_los_clk_en Value to ANA for rx_ana_los_clk_en

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_ana_los Value from ANA for rx_ana_los

LANE2_DIG_ANA_CREGS_TX_ANA_ATB_REG

Address: Operational Base + offset (0x12C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:3	RW	0x0	tx_ana_nc Reserved bit
2:1	RW	0x0	tx_ana_meas_atb BIST TX ATB measurement control
0	RW	0x0	tx_ana_meas_atb_en BIST TX ATB measurement enable

LANE2_DIG_ANA_CREGS_RX_ANA_EQ_CTRL

Address: Operational Base + offset (0x12C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x1	rx_ana_phdet_odd DFE sample control
4	RW	0x1	rx_ana_phdet_even DFE sample control
3:2	RW	0x1	rx_ana_ctle_offset_cal_enb EQ offset calibration enable
1:0	RW	0x0	rx_ana_afe_bias_mt EQ bias control

LANE2_DIG_ANA_CREGS_RX_ANA_VCO_CTRL

Address: Operational Base + offset (0x12C5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x1	rx_ana_cdr_vco_temp_comp_en VCO temperature compensation enable
1:0	RW	0x0	rx_ana_cdr_vco_startup_code VCO startup code

LANE2_DIG_ANA_CREGS_RX_ANA_VREG_CTRL

Address: Operational Base + offset (0x12C6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_vreg_ovrd_clk_vref VREG clk override reference voltage
4	RW	0x0	rx_ana_vreg_ovrd_vco_vref VREG VCO override reference voltage
3	RW	0x0	rx_ana_vreg_ovrd_vro_vref VREG VRO override reference voltage

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_ana_vreg_ovrd_cp_vref VREG charge-pump override reference voltage
1:0	RW	0x1	rx_ana_vreg_ring_ctrl VREG ring oscillator control

LANE2_DIG_ANA_CREGS_RX_ANA_DISCONNECT
Address: Operational Base + offset (0x12C7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_dc_path_disconnect TBA
1	RW	0x0	rx_ana_disconnect_m TBA
0	RW	0x0	rx_ana_disconnect_p TBA

LANE2_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL
Address: Operational Base + offset (0x12C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_ana_nc Reserved bits for future use

LANE2_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1
Address: Operational Base + offset (0x12C9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RW	0x0000	rx_meas_atb_14_0 Reserved
0	RW	0x0	rx_meas_atb_en rx_meas_atb_en

LANE2_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2
Address: Operational Base + offset (0x12CA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	rx_meas_atb_29_15 Reserved

LANE3_DIG_ASIC_LANE_OVRD_IN
Address: Operational Base + offset (0x1300)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_loopback_clk_en Loopback clock enable. When enabled the VCO clock of current lane is sent to the adjacent lane for TX BIST operation

Bit	Attr	Reset Value	Description
1	RW	0x0	Reserve_1 Reserve_1
0	RW	0x0	Reserve_0 Reserve_0

LANE3_DIG_ASIC_RX_ASIC_LOS
Address: Operational Base + offset (0x1301)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	los_en Value from asic for rx_los_en
14	RO	0x0	los_clk_en Value from asic for rx_los_clk_en
13:4	RO	0x000	los_timer_thresh Value from asic for rx_los_timer_thresh1
3:1	RO	0x0	los_threshold Value from asic for rx_los_threshold
0	RO	0x0	los Value of rx_los towards asic

LANE3_DIG_ASIC_LOS_OVRD_IN
Address: Operational Base + offset (0x1302)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	rx_los_ovrd Override enable for rx_los
8	RW	0x0	rx_los_r Override value for rx_los
7	RW	0x0	rx_los_threshold_ovrd Override enable for rx_los_threshold
6:4	RW	0x1	rx_los_threshold_r Override value for rx_los_threshold
3	RW	0x0	rx_los_clk_en_ovrd Override enable for rx_los_clk_en
2	RW	0x0	rx_los_clk_en_r Override value for rx_los_clk_en
1	RW	0x0	rx_los_en_ovrd Override enable for rx_los_en
0	RW	0x0	rx_los_en_r Override value for rx_los_en

LANE3_DIG_ASIC_LOS_OVRD_IN_1
Address: Operational Base + offset (0x1303)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RW	0x0	rx_los_timer_thresh_ovrd Override enable for rx_los_timer_thresh1
9:0	RW	0x05a	rx_los_timer_thresh_r Override value for rx_los_timer_thresh1

LANE3_DIG_ASIC_CDR_CONTROL_OVRD_IN
Address: Operational Base + offset (0x1306)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:1	RW	0x0	cdr_setting_sel Override values for CDR setting bits which select the CDR gain values
0	RW	0x0	cdr_setting_sel_ovrd_en Override enable for cdr_setting_sel signal

LANE3_DIG_ASIC_RX_OVRD_IN_0
Address: Operational Base + offset (0x1307)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:13	RW	0x0	rate_3_2 Override value for rx_rate[3:2]
12	RW	0x0	width_ovrd_en Enable override for rx_width
11:10	RW	0x0	width Override value for rx_width
9	RW	0x0	rate_ovrd_en Enable override value for rx_rate[1:0]
8:7	RW	0x0	rate_1_0 Override value for rx_rate
6	RW	0x0	pstate_ovrd_en Enable override value for rx_pstate
5:4	RW	0x0	pstate Override value for rx_pstate
3	RW	0x0	data_en_ovrd_en Enable override value for rx_data_en
2	RW	0x0	data_en Override value for rx_data_en
1	RW	0x0	req_ovrd_en Enable override value for rx_req
0	RW	0x0	req Override value for rx_req

LANE3_DIG_ASIC_RX_OVRD_IN_1
Address: Operational Base + offset (0x1308)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:10	RW	0x0	rx_clk_x2_en Override value for rx_clk_x2_en[2:0]
9	RW	0x0	rx_cdr_vco_highfreq Override value for rx_cdr_vco_highfreq
8	RW	0x0	rx_ref_ld_val_6 Override value for rx_ref_ld_val[6]
7	RW	0x0	en Enable override values for all inputs controlled by this register

Bit	Attr	Reset Value	Description
6	RW	0x0	rx_cdr_vco_lowfreq Override value for rx_cdr_vco_lowfreq
5:0	RW	0x14	rx_ref_ld_val_5_0 Override value for rx_ref_ld_val[5:0]

LANE3_DIG_ASIC_RX_OVRD_IN_2
Address: Operational Base + offset (0x1309)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	en Enable override values for all inputs controlled by this register
12:0	RW	0x03e8	rx_vco_ld_val Override value for rx_vco_ld_val

LANE3_DIG_ASIC_RX_OVRD_IN_3
Address: Operational Base + offset (0x130A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x00	reserved_14_to_10 Reserved_14_to_10
9	RW	0x0	disable_ovrd_en Enable override for rx_disable
8	RW	0x0	disable Override value for rx_disable
7	RW	0x0	clk_shift_ovrd_en Enable override for rx_clk_shift
6	RW	0x0	clk_shift Override value for rx_clk_shift
5	RW	0x0	align_en_ovrd_en Enable override for rx_align_en
4	RW	0x0	align_en Override value for rx_align_en
3	RW	0x0	cdr_ssc_en_ovrd_en Enable override value for rx_cdr_ssc_en
2	RW	0x0	cdr_ssc_en Override value for rx_cdr_ssc_en
1	RW	0x0	cdr_track_en_ovrd_en Enable override value for rx_cdr_track_en
0	RW	0x0	cdr_track_en Override value for rx_cdr_track_en

LANE3_DIG_ASIC_RX_OVRD_IN_4
Address: Operational Base + offset (0x130B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	adpt_ovrd_en Enable override for rx_adpt_dfe_en and rx_adpt_afe_en

Bit	Attr	Reset Value	Description
5	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
4	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
3	RW	0x0	invert_ovrd_en Enable override for rx_invert
2	RW	0x0	invert Override value for rx_invert
1	RW	0x0	lpd_ovrd_en Enable override for rx_lpd
0	RW	0x0	lpd Override value for rx_lpd

LANE3_DIG_ASIC_RX_OVRD_IN_5
Address: Operational Base + offset (0x130C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	reset_ovrd_en Enable override for rx_reset
0	RW	0x0	reset Override value for rx_reset

LANE3_DIG_ASIC_RX_OVRD_EQ_IN_0
Address: Operational Base + offset (0x130D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x06	eq_ctle_boost Override value for rx_eq_ctle_boost
10:7	RW	0x0	reserved Reserved
6:3	RW	0xf	eq_afe_gain Override value for rx_eq_afe_gain
2:0	RW	0x0	eq_att_lvl Override value for rx_eq_att_lvl

LANE3_DIG_ASIC_RX_OVRD_EQ_IN_1
Address: Operational Base + offset (0x130E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	eq_ovrd_en Enable override value for rx_eq_* inputs
14:7	RW	0x80	eq_dfe_tap1 Override value for rx_eq_dfe_tap1
6:0	RW	0x40	eq_dfe_tap2 Override value for rx_eq_dfe_tap2

LANE3_DIG_ASIC_RX_OVRD_OUT_0
Address: Operational Base + offset (0x130F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use

Bit	Attr	Reset Value	Description
8	RW	0x0	ana_ovl_det_0v_en Enable override for rx_ana_ovl_det_0v_i
7	RW	0x0	ana_ovl_det_0v Override value for rx_ana_ovl_det_0v_i
6	RW	0x0	adapt_sts_ovrd_en Enable override for rx_adapt_sts
5:4	RW	0x0	adapt_sts Override value for rx_adapt_sts
3	RW	0x0	rsv_0 Reserve_0
2	RW	0x0	rsv_1 Reserve_1
1	RW	0x0	ack_ovrd_en Enable override for rx_ack
0	RW	0x0	ack Override value for rx_ack

LANE3_DIG_ASIC_RX_ASIC_IN_0

Address: Operational Base + offset (0x1315)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_track_en Value from ASIC for rx_cdr_track_en
13	RO	0x0	adapt_dfe_en Value from ASIC for rx_adapt_dfe_en
12	RO	0x0	adapt_afe_en Value from ASIC for rx_adapt_afe_en
11	RO	0x0	reserved Reserved
10:9	RO	0x0	width Value from ASIC for rx_width
8:7	RO	0x0	rate_1_0 Value from ASIC for rx_rate[1:0]
6:5	RO	0x0	pstate Value from ASIC for rx_pstate
4	RO	0x0	lpd Value from ASIC for rx_lpd
3	RO	0x0	req Value from ASIC for rx_req
2	RO	0x0	data_en Value from ASIC for rx_data_en
1	RO	0x0	invert Value from ASIC for rx_invert
0	RO	0x0	reset Value from ASIC for rx_reset

LANE3_DIG_ASIC_RX_ASIC_IN_1

Address: Operational Base + offset (0x1316)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use

Bit	Attr	Reset Value	Description
9:8	RO	0x0	rate_3_2 Value from ASIC for rx_rate[3:2]
7	RO	0x0	reserved_7 Reserved_7
6:4	RO	0x0	reserved_6_to_4 Reserved_6_to_4
3	RO	0x0	disable Value from ASIC for rx_disable
2	RO	0x0	clk_shift Value from ASIC for rx_clk_shift
1	RO	0x0	align_en Value from ASIC for rx_align_en
0	RO	0x0	cdr_ssc_en Value from ASIC for rx_cdr_ssc_en

LANE3_DIG_ASIC_RX_EQ_ASIC_IN_0
Address: Operational Base + offset (0x1317)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
10:9	RO	0x0	rx_ana_afe_rate Value from ASIC for rx_ana_afe_rate
8:7	RO	0x0	rx_ana_afe_ctle_pole Value from ASIC for rx_ana_afe_ctle_pole
6:3	RO	0x0	eq_afe_gain Value from ASIC for rx_eq_afe_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

LANE3_DIG_ASIC_RX_EQ_ASIC_IN_1
Address: Operational Base + offset (0x1318)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:7	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1
6:0	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2

LANE3_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0
Address: Operational Base + offset (0x1319)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RO	0x0	rx_clk_x2_en Value from ASIC for rx_clk_x2_en[2:0]
8	RO	0x0	rx_cdr_vco_highfreq Value from ASIC for rx_cdr_vco_highfreq
7:1	RO	0x00	rx_ref_ld_val Value from ASIC for rx_ref_ld_val

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_cdr_vco_lowfreq Value from ASIC for rx_cdr_vco_lowfreq

LANE3_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1
Address: Operational Base + offset (0x131A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_vco_ld_val Value from ASIC for rx_vco_ld_val

LANE3_DIG_ASIC_RX_ASIC_OUT_0
Address: Operational Base + offset (0x131B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:3	RO	0x0	adapt_sts Value from PHY for rx_adapt_sts
2	RO	0x0	valid Value from PHY for rx_valid
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	ack Value from PHY for rx_ack

LANE3_DIG_LBERT_CTL
Address: Operational Base + offset (0x1320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:5	RW	0x000	pat0 Pattern for modes 3-5
4	RW	0x0	trigger_err Insert a single error into a LSB any write of a 1 to this bit will insert an error
3:0	RW	0x0	mode Pattern to generate when changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: Fixed word (PAT0) 4'b1010: DC balanced word (PAT0, ~PAT0) 4'b1011: Fixed pattern: (000, PAT0, 3ff, ~PAT0) others: Reserved

LANE3_DIG_RX_CDR_CDR_CTL_0
Address: Operational Base + offset (0x1324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:7	RW	0x0	dtb_sel Select to drive various signals onto the dtb 4'b0000: Disabled 4'b0001: Rx_pr_stable, rx_afe_stable from rx_ana_ctl 4'b0010: Com_good, com_bad from rx_align 4'b0011: Shift_in_prog, ana_odd_data from rx_align 4'b0100: 2 MSB's of XAUI align FSM state 4'b0101: 2 LSB's of XAUI align FSM state 4'b0110: Error_high, low from lbert_pm 4'b0111: Ana_los, los_filter from los block 4'b1000: Eios_state[0], eios_det from los block 4'b1001: Cdr_valid, MSB of FSM state from cdr_ctl 4'b1010: 2 LSB's of FSM state from cdr_ctl 4'b1011: Rx_dig_rst, rx_dig_en 4'b1100: Rx_ana_word_clk_i, rx_ana_dword_clk_i 4'b1101: Lbert_pg strobe others: Reserved
6	RW	0x0	always_realign Realign on any misaligned comma
5	RW	0x0	phdet_en_pr_mode Enable partial response phase detector mode
4	RW	0x0	phdet_pol Reverse polarity of phase error
3:2	RW	0x3	phdet_edge Edges to use for phase detection. 2'b00: Ignore all edges 2'b01: Use rising edges only 2'b10: Use both edges 2'b11: Use falling edges only
1:0	RW	0x3	phdet_en Enable phase detector. Top bit is odd slicers, bottom is even

LANE3_DIG_RX_CDR_CDR_CTL_1
Address: Operational Base + offset (0x1325)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RW	0x1c	ssc_off_cnt1 When SSC mode is disabled, the 12-bit word count in gain stage 1 is: (SSC_OFF_CNT1 * 4) in 20b mode (SSC_OFF_CNT1 * 5) in 16b mode
9:0	RW	0x039	ssc_off_cnt0 When SSC mode is disabled, the 12-bit word count in gain stage 0 is: (SSC_OFF_CNT0 * 4) in 20b mode (SSC_OFF_CNT0 * 5) in 16b mode

LANE3_DIG_RX_CDR_CDR_CTL_2
Address: Operational Base + offset (0x1326)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x25	ssc_on_cnt1 When SSC mode is enabled, the 12-bit word count in gain stage 1 is: (SSC_ON_CNT1 * 8) in 20b mode (SSC_ON_CNT1 * 10) in 16b mode
8:0	RW	0x0bb	ssc_on_cnt0 When SSC mode is enabled, the 12-bit word count in gain stage 0 is: (SSC_ON_CNT0 * 8) in 20b mode (SSC_ON_CNT0 * 10) in 16b mode

LANE3_DIG_RX_CDR_CDR_CTL_3
Address: Operational Base + offset (0x1327)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:10	RW	0x2	ssc_on_phug1 When SSC mode is enabled, the phug value in gain stage 1 is SSC_ON_PHUG1
9:6	RW	0x6	ssc_on_phug0 When SSC mode is enabled, the phug value in gain stage 0 is SSC_ON_PHUG0
5:3	RW	0x3	ssc_on_frug1 When SSC mode is enabled, the frug value in gain stage 1 is SSC_ON_FRUG1
2:0	RW	0x3	ssc_on_frug0 When SSC mode is enabled, the frug value in gain stage 0 is SSC_ON_FRUG0

LANE3_DIG_RX_CDR_CDR_CTL_4
Address: Operational Base + offset (0x1328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:8	RW	0x0	frug_ovrd_value Override value for frug (frequency update gain) 3'b000: 0 3'b001: 1/16 LSB/update 3'b010: 1/8 LSB/update 3'b011: 1/4 LSB/update 3'b100: 1/2 LSB/update 3'b101: 1 LSB/update 3'b110: 2 LSB/update 3'b111: 4 LSB/update

Bit	Attr	Reset Value	Description
7:4	RW	0x0	phug_ovrd_value Override value for phug (phase update gain) : 4'b0000: 0 4'b0001: 1000 ppm 4'b0010: 2000 ppm 4'b0011: 3000 ppm 4'b0100: 4000 ppm 4'b0101: 5000 ppm 4'b0110: 6000 ppm 4'b0111: 7000 ppm 4'b1000: 8000 ppm 4'b1001: 9000 ppm 4'b1010: 10000 ppm 4'b1011: 11000 ppm 4'b1100: 12000 ppm 4'b1101: 13000 ppm 4'b1110: 14000 ppm 4'b1111: 15000 ppm
3	RW	0x0	ovrd_dpll_gain Override phug and frug values
2:0	RW	0x3	ssc_off_frug0 When SSC mode is disabled, the frug value in gain stage 0 is SSC_OFF_FRUG0

LANE3_DIG_RX_CDR_CDR_CTL_5
Address: Operational Base + offset (0x1329)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs3_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS3_FRUG1
8:6	RW	0x1	ssc_off_lbrs2_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS2_FRUG1
5:3	RW	0x1	ssc_off_lbrs1_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS1_FRUG1
2:0	RW	0x1	ssc_off_lbrs0_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS0_FRUG1

LANE3_DIG_RX_CDR_CDR_CTL_6
Address: Operational Base + offset (0x132A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs7_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS7_FRUG1
8:6	RW	0x3	ssc_off_lbrs6_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS6_FRUG1

Bit	Attr	Reset Value	Description
5:3	RW	0x3	ssc_off_lbrs5_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS5_FRUG1
2:0	RW	0x3	ssc_off_lbrs4_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS4_FRUG1

LANE3_DIG_RX_CDR_CDR_CTL_7

Address: Operational Base + offset (0x132B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x8	ssc_off_lbrs3_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS3_PHUG0
11:8	RW	0x7	ssc_off_lbrs2_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS2_PHUG0
7:4	RW	0x6	ssc_off_lbrs1_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS1_PHUG0
3:0	RW	0x6	ssc_off_lbrs0_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS0_PHUG0

LANE3_DIG_RX_CDR_CDR_CTL_8

Address: Operational Base + offset (0x132C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS7_PHUG0
11:8	RW	0xc	ssc_off_lbrs6_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS6_PHUG0
7:4	RW	0xc	ssc_off_lbrs5_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS5_PHUG0
3:0	RW	0xa	ssc_off_lbrs4_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS4_PHUG0

LANE3_DIG_RX_CDR_CDR_CTL_9

Address: Operational Base + offset (0x132D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x6	ssc_off_lbrs3_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS3_PHUG1
11:8	RW	0x4	ssc_off_lbrs2_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS2_PHUG1
7:4	RW	0x3	ssc_off_lbrs1_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS1_PHUG1

Bit	Attr	Reset Value	Description
3:0	RW	0x2	ssc_off_lbrs0_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS0_PHUG1

LANE3_DIG_RX_CDR_CDR_CTL_10

Address: Operational Base + offset (0x132E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS7_PHUG1
11:8	RW	0xc	ssc_off_lbrs6_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS6_PHUG1
7:4	RW	0xa	ssc_off_lbrs5_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS5_PHUG1
3:0	RW	0x8	ssc_off_lbrs4_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS4_PHUG1

LANE3_DIG_RX_CDR_STAT

Address: Operational Base + offset (0x132F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:4	RO	0x0	frug_value Notes: Current value for dpll_frug[2:0]
3:0	RO	0x0	phug_value Notes: Current value for dpll_phug[3:0]

LANE3_DIG_RX_PWRCTL_RX_PSTATE_P0

Address: Operational Base + offset (0x1340)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	rx_p0_dig_clk_en Enable/Disable RX digital clocks in P0
10	RW	0x1	rx_p0_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0, if RX_P0_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0_vco_cal_rst Enable/Disable resetting the RX VCO in P0
8	RW	0x0	rx_p0_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0
7	RW	0x1	rx_p0_ana_cdr_en Value of RX ana cdr_en in P0
6	RW	0x1	rx_p0_ana_deser_en Value of RX ana deserial_en in P0

Bit	Attr	Reset Value	Description
5	RW	0x1	rx_p0_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0
4	RW	0x1	rx_p0_ana_clk_en Value of RX ana clk_en in P0
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0
1	RW	0x1	rx_p0_ana_afe_en Value of RX ana afe_en in P0
0	RW	0x1	reserved_0 Reserved_0

LANE3_DIG_RX_PWRCTL_RX_PSTATE_P0S
Address: Operational Base + offset (0x1341)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p0s_dig_clk_en Enable/Disable RX digital clocks in P0S
10	RW	0x1	rx_p0s_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0S, if RX_P0S_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0s_vco_cal_rst Enable/Disable resetting the RX VCO in P0S
8	RW	0x0	rx_p0s_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0S
7	RW	0x0	rx_p0s_ana_cdr_en Value of RX ana cdr_en in P0S
6	RW	0x0	rx_p0s_ana_deser_en Value of RX ana deserial_en in P0S
5	RW	0x0	rx_p0s_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0S
4	RW	0x0	rx_p0s_ana_clk_en Value of RX ana clk_en in P0S
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0s_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0S
1	RW	0x1	rx_p0s_ana_afe_en Value of RX ana afe_en in P0S
0	RW	0x1	reserved_0 Reserved_0

LANE3_DIG_RX_PWRCTL_RX_PSTATE_P1
Address: Operational Base + offset (0x1342)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use

Bit	Attr	Reset Value	Description
11	RW	0x0	rx_p1_dig_clk_en Enable/Disable RX digital clocks in P1
10	RW	0x0	rx_p1_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P1, if RX_P1_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p1_vco_cal_rst Enable/Disable resetting the RX VCO in P1
8	RW	0x1	rx_p1_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P1
7	RW	0x0	rx_p1_ana_cdr_en Value of RX ana cdr_en in P1
6	RW	0x0	rx_p1_ana_deser_en Value of RX ana deserial_en in P1
5	RW	0x0	rx_p1_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P1
4	RW	0x0	rx_p1_ana_clk_en Value of RX ana clk_en in P1
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p1_ana_clk_vreg_en Value of RX ana clk_vreg_en in P1
1	RW	0x1	rx_p1_ana_afe_en Value of RX ana afe_en in P1
0	RW	0x1	reserved_0 Reserved_0

LANE3_DIG_RX_PWRCTL_RX_PSTATE_P2
Address: Operational Base + offset (0x1343)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p2_dig_clk_en Enable/Disable RX digital clocks in P2
10	RW	0x0	rx_p2_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P2, if RX_P2_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p2_vco_cal_rst Enable/Disable resetting the RX VCO in P2
8	RW	0x1	rx_p2_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P2
7	RW	0x0	rx_p2_ana_cdr_en Value of RX ana cdr_en in P2
6	RW	0x0	rx_p2_ana_deser_en Value of RX ana deserial_en in P2
5	RW	0x0	rx_p2_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P2
4	RW	0x0	rx_p2_ana_clk_en Value of RX ana clk_en in P2

Bit	Attr	Reset Value	Description
3	RW	0x0	reserved Reserved
2	RW	0x0	rx_p2_ana_clk_vreg_en Value of RX ana clk_vreg_en in P2
1	RW	0x0	rx_p2_ana_afe_en Value of RX ana afe_en in P2
0	RW	0x1	reserved_0 Reserved_0

LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_0
Address: Operational Base + offset (0x1344)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x0f	rx_dpll_clock_switch_time Wait between switching rx_dpll clock from Rx_clk to ref_clk or vice-versa
4:0	RW	0x06	rx_state_3a_and_3b_time Wait between Power state 3A and 3B

LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_1
Address: Operational Base + offset (0x1345)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	fast_rx_vreg_en Enable fast RX VREG enable (simulation only)
12:7	RW	0x0d	rx_vreg_en_time Power up time (in ref_range cycles) for RX ana vreg enable (spec 500ns)
6	RW	0x0	fast_rx_afe_en Enable fast RX AFE enable (simulation only)
5:0	RW	0x1a	rx_afe_en_time Power up time (in ref_range cycles) for RX ana AFE enable (spec >=1us)

LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_2
Address: Operational Base + offset (0x1346)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	fast_rx_clk_en Enable fast RX clock enable (simulation only)
5:0	RW	0x1a	rx_clk_en_time Power up time (in ref_range cycles) for RX ana clk (or dcc) enable (spec >1us)

LANE3_DIG_RX_PWRCTL_RX_PWRUP_TIME_3
Address: Operational Base + offset (0x1347)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x0	rx_deser_dis_time Power down time in (ref_range cycles) for RX ana deserial enable
13:12	RW	0x0	rx_deser_en_time Power up time (in ref_range cycles) for RX ana deserial enable
11:8	RW	0x0	rx_cdr_en_time Power up time (in ref_range cycles) for RX ana CDR (or dfe/dfe_taps) enable (spec 0ns)
7:2	RW	0x00	rsvd_3_7_2 Reserved
1:0	RW	0x0	rx_rate_time Power up time (in ref_range cycles) for RX ana rate or width change

LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0
Address: Operational Base + offset (0x1348)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RW	0x0	vcoclk_correct_update Update the vcoclk_correct
11:9	RW	0x2	int_gain_cal_bounce_cnt Number of bounces (i.e. direction changes) on the int_gain code before indicating that the RX VCO calibration is done
8:6	RW	0x0	int_gain_cal_cnt_shift Number of shifts to apply to ld_cnt inputs when performing int_gain code calibration
5	RW	0x0	int_gain_cal_fixed_cnt_en Enable a fixed count (instead of bounce count) for int_gain code calibration
4:0	RW	0x00	int_gain_cal_fixed_cnt Number of steps done during int_gain code calibration when INT_GAIN_CAL_FIXED_CNT_EN is enabled.

LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1
Address: Operational Base + offset (0x1349)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x00	dtb_sel DTB select for RX VCO dtb signals 7'h01: {chkfrq_en, ref_dig_clk} 7'h02: {rx_ana_cdr_vco_en_i, rx_ana_cdr_startup_i} 7'h04: {rx_vco_up, dpll_freq_rst} 7'h08: {rx_vco_contcal_en, rx_vco_cal_rst} 7'h10: {chkfrq_done, vcoclk_too_fast} 7'h20: {cal_dir, rx_vco_cal_done} 7'h40: {curr_state[0], rx_vco_cnt[0]} others: Reserved
8:5	RW	0x8	dpll_cal_ug DPLL calibration update on int_gain code 3'h0: 0 others: (1/16)*2^(DPLL_CAL_UG-1) LSB/update Maximum DPLL_CAL_UG=10, i.e. 32 LSB/update

Bit	Attr	Reset Value	Description
4	RW	0x0	disable_int_cal_mode When asserted, then the DPLL frequency register is never modified by the RX VCO calibration FSM (even, if DPLL_CAL_UG is non-zero). In this case, the calibration will always be performed on the VCO freq_tune code. This allows disabling of integral calibration feature, and hence only using freq_tune calibration.
3	RW	0x0	rx_vco_contcal_en Override value for the continuous calibration enable from the RX PWRSM
2	RW	0x0	rx_vco_cal_rst Override value for the calibration reset from the RX PWRSM
1	RW	0x0	rx_vco_freq_rst Override value for the frequency reset from the RX PWRSM
0	RW	0x0	rx_vco_ovrd_sel Override the calibration controls from the RX PWRSM

LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2
Address: Operational Base + offset (0x134A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_rx_vco_cal Skip RX VCO calibration altogether
14	RW	0x0	skip_rx_vco_freq_tune_cal Skip RX VCO coarse calibration
13:10	RW	0x9	freq_tune_cal_steps Number of cal steps of freq tune
9:0	RW	0x200	freq_tune_start_val Starting value of freq tune code

LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0
Address: Operational Base + offset (0x134B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	fast_rx_vco_wait Enable fast RX VCO power up (simulation only)
14:11	RW	0x6	rx_vco_cntr_pwrup_time Power up time (in ref_range cycles) for RX ana VCO cnter (spec >200ns)
10:7	RW	0x6	rx_vco_update_time Settle time (in ref_range cycles) for RX ana VCO update (freq_tune or int_gain) (spec >200ns)
6:0	RW	0x19	rx_vco_startup_time Power up time (in ref_range cycles) for RX ana VCO startup (spec >1us)

LANE3_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1
Address: Operational Base + offset (0x134C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use

Bit	Attr	Reset Value	Description
2:0	RW	0x3	rx_vco_cntr_settle_time RX VCO counter value settling time in (ref_dig_clk cycles) (spec: 3 ref_dig_clk cycle)

LANE3_DIG_RX_VCOCAL_RX_VCO_STAT_0
Address: Operational Base + offset (0x134D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	rx_ana_cdr_vco_en Current value of rx_ana_cdr_vco_en_i
12	RO	0x0	rx_ana_cdr_startup Current value of rx_ana_cdr_startup_i
11	RO	0x0	rx_ana_vco_cntr_en Current value of rx_ana_vco_cntr_en_i
10	RO	0x0	rx_ana_vco_cntr_pd Current value of rx_ana_vco_cntr_pd_i
9:0	RO	0x000	rx_ana_cdr_freq_tune Current value of rx_ana_cdr_freq_tune_i

LANE3_DIG_RX_VCOCAL_RX_VCO_STAT_1
Address: Operational Base + offset (0x134E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	dpll_freq_rst Indicates that the RX integral frequency is reset or not
7	RO	0x0	rx_vco_cal_done Indicates that the RX VCO has completed calibration
6	RO	0x0	rx_vco_contcal_en Value of the continuous calibration enable from the RX PWRSM
5	RO	0x0	rx_vco_cal_rst Value of the calibration reset from the RX PWRSM
4	RO	0x0	rx_vco_freq_rst Value of the RX VCO frequency reset from the RX PWRSM
3:0	RO	0x0	rx_vco_fsm_state Value of the RX VCO CAL FSM

LANE3_DIG_RX_VCOCAL_RX_VCO_STAT_2
Address: Operational Base + offset (0x134F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	rx_vco_up Indicates that the RX VCO is ready
14	RO	0x0	rx_vco_correct Indicates that the RX VCO clock has the correct frequency
13	RO	0x0	vcoclk_too_fast Indicates that the RX VCO clock frequency is too fast
12:0	RO	0x0000	vco_cntr_final Value of RX VCO counter when refclk counter expired

LANE3_DIG_RX_RX_ALIGN_XAUI_COMM_MASK

Address: Operational Base + offset (0x1350)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x3ff	xaui_comm_mask XAUI_COMMA mask. For 10-bit COMMA set the mask to 0x3FF and for 7-bit COMMA set the mask to 0x3F8

LANE3_DIG_RX_LBERT_CTL

Address: Operational Base + offset (0x1351)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	sync Synchronize pattern matcher LFSR with incoming data A write of a one to this bit will reset the error counter and start a synchronization of the PM, there is no need to write this back to zero to run normally.
3:0	RW	0x0	mode Pattern to match When changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: D[n] = d[n-10] 4'b1010: D[n] = !d[n-10] 4'b1011: D[n] = !d[n-20] others: Reserved

LANE3_DIG_RX_LBERT_ERR

Address: Operational Base + offset (0x1352)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ov14 If active, multiply count by 128. if OV14=1 and count=2^15-1, signals overflow of counter (2 reads needed to read value)
14:0	RW	0x0000	count A read of this register, or a sync of the PM resets the error count. Current error count, if OV14 field is active, then multiply count by 128 (2 reads needed to read value)

LANE3_DIG_RX_RX_LOS_LOS_0

Address: Operational Base + offset (0x1353)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use

Bit	Attr	Reset Value	Description
8	RW	0x0	rx_los_filt_byp Bypass digital LOS filter
7:3	RW	0x0c	rx_los_t_thresh0_r LOS timer0 threshold to count presence of zeros on rx_los
2:0	RW	0x2	rx_los_wait_r Initial wait time for rx_los after rx_los_en is asserted

LANE3_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS
Address: Operational Base + offset (0x1355)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_pwrsm_state Value for rx_pwrsm_state

LANE3_DIG_RX_DPLL_FREQ
Address: Operational Base + offset (0x135C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:0	RW	0x2000	val Freq is 125*VAL ppm from the reference (2 reads needed to read value)

LANE3_DIG_RX_DPLL_FREQ_BOUND_0
Address: Operational Base + offset (0x135D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:1	RW	0x264	upper_freq_bound Upper frequency bound in terms of LSBs of the integral control code
0	RW	0x0	freq_bound_en Enable the frequency bounds feature

LANE3_DIG_RX_DPLL_FREQ_BOUND_1
Address: Operational Base + offset (0x135E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x19c	lower_freq_bound Lower frequency bound in terms of LSBs of the integral control code

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_0
Address: Operational Base + offset (0x1360)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	adpt_clk_div4_en Set the adaptation clock to be divided by 4 (default is div2)

Bit	Attr	Reset Value	Description
14	RW	0x0	start_asm1 Start adaptation state machine #1 (VGA, CTLE, DFE, EYEH) This register-bit is self-clearing
13:10	RW	0x3	n_tgg_asm1 Number of toggle loop iterations for ASM1
9:0	RW	0x010	n_top_asm1 Number of top level loop iterations for ASM1

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_1
Address: Operational Base + offset (0x1361)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	ctle_pole_ovrd_en Override CTLE pole value (only valid, if adaptation is run)
10:8	RW	0x0	ctle_pole_ovrd_val CTLE pole override value to load at start of adaptation
7	RW	0x0	fast_afe_dfe_settle Enable fast AFE and DFE settling time (simulation only)
6:0	RW	0x09	n_wait_asm1 Number of wait cycles for adaptation SM #1

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_2
Address: Operational Base + offset (0x1362)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x06	tgg_pttrn_1 Pattern for the second toggle loop error slicer is moved upward by data tap1, if this pattern is matched
4:0	RW	0x02	tgg_pttrn_0 Pattern for the first toggle loop error slicer is moved downward by data tap1, if this pattern is matched

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_3
Address: Operational Base + offset (0x1363)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	esl_twice_dsl Assert, if error slicer has twice the voltage range as the data slicer (for the same 8 bits).
14	RW	0x0	tgg_en Enable toggling of the error slicer
13	RW	0x0	eyeho_en Enable eye height measurement using odd error slicer
12	RW	0x0	eyehe_en Enable eye height measurement using even error slicer
11:7	RW	0x00	dfe_en Enable DFE adaptation for taps 5-1
6	RW	0x0	att_en Enable ATT adaptation

Bit	Attr	Reset Value	Description
5	RW	0x0	vga_en Enable VGA adaptation
4:0	RW	0x00	ctle_en Enable CTLE boost adaptation, the five bits determine which correlators are used to adapt the CTLE

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_4
Address: Operational Base + offset (0x1364)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	dfe2_th DFE Tap2 correlation decision threshold (2^N-1)
11:8	RW	0x0	dfe1_th DFE Tap1 correlation decision threshold (2^N-1)
7:4	RW	0x0	vga_th VGA correlation decision threshold (2^N-1). During eye height measurement, the VGA_TH is repurposed for error slicer updates.
3:0	RW	0x0	ctle_th CTLE correlation decision threshold (2^N-1)

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_5
Address: Operational Base + offset (0x1365)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	th_offset Apply an offset to the decision threshold
11:8	RW	0x0	dfe5_th DFE Tap5 correlation decision threshold (2^N-1)
7:4	RW	0x0	dfe4_th DFE Tap4 correlation decision threshold (2^N-1)
3:0	RW	0x0	dfe3_th DFE Tap3 correlation decision threshold (2^N-1)

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_6
Address: Operational Base + offset (0x1366)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RW	0x3	att_low_th ATT low threshold
12	RW	0x1	vga_sat_cnt_sticky If deasserted, then VGA saturation counts must be consecutive to change ATT
11:9	RW	0x4	vga_sat_cnt VGA saturation count
8:6	RW	0x4	att_mu ATT gain code update gain (2^N)
5:3	RW	0x5	vga_mu VGA gain code update gain (2^N). During eye height measurement, the VGA_MU is repurposed for error slicer updates.
2:0	RW	0x3	ctle_mu CTLE boost code update gain (2^N)

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_7
Address: Operational Base + offset (0x1367)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x10	vga_lev_low VGA level low saturation limit
9:5	RW	0x1a	vga_lev_high VGA level high saturation limit
4:0	RW	0x02	vga_min_sat VGA minimum saturation limit

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_8
Address: Operational Base + offset (0x1368)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x4	dfe5_mu DFE tap5 code update gain (2^N)
11:9	RW	0x4	dfe4_mu DFE tap4 code update gain (2^N)
8:6	RW	0x4	dfe3_mu DFE tap3 code update gain (2^N)
5:3	RW	0x4	dfe2_mu DFE tap2 code update gain (2^N)
2:0	RW	0x5	dfe1_mu DFE tap1 code update gain (2^N)

LANE3_DIG_RX_ADPTCTL_ADPT_CFG_9
Address: Operational Base + offset (0x1369)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	err_slo_adpt_init The error odd slicer is initialized to this value at the start of a new adaptation request.
7:0	RW	0x00	err_sle_adpt_init The error even slicer is initialized to this value at the start of a new adaptation request.

LANE3_DIG_RX_ADPTCTL_RST_ADPT_CFG
Address: Operational Base + offset (0x136A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x1	rst_adpt_tap1 Reset data Tap1 when turning off DFE adaptation (taps 2-5 are always turned off when DFE adaptation is turned off)
3	RW	0x1	rst_adpt_ctle_pole Reset CTLE pole when turning off AFE adaptation
2	RW	0x1	rst_adpt_ctle_boost Reset CTLE boost when turning off AFE adaptation

Bit	Attr	Reset Value	Description
1	RW	0x1	rst_adpt_vga Reset VGA when turning off AFE adaptation
0	RW	0x1	rst_adpt_att Reset ATT when turning off AFE adaptation

LANE3_DIG_RX_ADPTCTL_ATT_STATUS
Address: Operational Base + offset (0x136B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	asm1_don Asserts when adaptation state machine #1 is done
7:0	RO	0x00	att_adpt_code Value of ATT adaptation code

LANE3_DIG_RX_ADPTCTL_VGA_STATUS
Address: Operational Base + offset (0x136C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
9:0	RO	0x000	vga_adpt_code Value of VGA adaptation code

LANE3_DIG_RX_ADPTCTL_CTLE_STATUS
Address: Operational Base + offset (0x136D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:10	RO	0x0	ctle_pole_adpt_code Value of CTLE pole adaptation code
9:0	RO	0x000	ctle_boost_adpt_code Value of CTLE boost adaptation code

LANE3_DIG_RX_ADPTCTL_DFE_TAP1_STATUS
Address: Operational Base + offset (0x136E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:0	RO	0x0000	dfe_tap1_adpt_code Value of DFE tap1 adaptation code

LANE3_DIG_RX_ADPTCTL_DFE_TAP2_STATUS
Address: Operational Base + offset (0x136F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap2_adpt_code Value of DFE tap2 adaptation code

LANE3_DIG_RX_ADPTCTL_DFE_TAP3_STATUS

Address: Operational Base + offset (0x1370)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap3_adpt_code Value of DFE tap3 adaptation code

LANE3_DIG_RX_ADPTCTL_DFE_TAP4_STATUS

Address: Operational Base + offset (0x1371)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap4_adpt_code Value of DFE tap4 adaptation code

LANE3_DIG_RX_ADPTCTL_DFE_TAP5_STATUS

Address: Operational Base + offset (0x1372)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap5_adpt_code Value of DFE tap5 adaptation code

LANE3_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1373)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_vdac_ofst Offset value for DFE data even vDAC

LANE3_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST

Address: Operational Base + offset (0x1374)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_vdac_ofst Offset value for DFE data odd vDAC

LANE3_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN

Address: Operational Base + offset (0x1375)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE3_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD

Address: Operational Base + offset (0x1376)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

LANE3_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST

Address: Operational Base + offset (0x1377)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

LANE3_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST

Address: Operational Base + offset (0x1378)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

LANE3_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL

Address: Operational Base + offset (0x1379)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	e_sle_lvl Even error slicer level
7:0	RO	0x00	e_slo_lvl Odd error slicer level

LANE3_DIG_RX_ADPTCTL_ADPT_RESET

Address: Operational Base + offset (0x137A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	reset_asm1 Resets adaptation state machine (ASM1) as well as the stats capture block. This is a self-clearing bit, and requires re-start of ASM1.

LANE3_DIG_RX_STAT_LD_VAL_1

Address: Operational Base + offset (0x1380)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sc1_start Start sample counter #1 this is a self-clearing bit
14:0	RW	0x0040	sc1_ld_val Sample counter #1 load value

LANE3_DIG_RX_STAT_DATA_MSK

Address: Operational Base + offset (0x1381)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	data_msk_15_0 Value of data_msk_r[15:0]

LANE3_DIG_RX_STAT_MATCH_CTL0

Address: Operational Base + offset (0x1382)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	scope_dly For clock cycle delays on scope_data_rx_clk, an additional MSB is added in SCOPE_DLY_2
13:10	RW	0xf	data_msk_19_16 Value of data_msk_r[19:16]
9:5	RW	0x00	pttrn_cr1a_4_0 Value of pattern A for 1st correlator (bits 4:0)
4:0	RW	0x06	pttrn_msk_cr1a_4_0 Value of pattern A mask for 1st correlator (bits 4:0)

LANE3_DIG_RX_STAT_MATCH_CTL1

Address: Operational Base + offset (0x1383)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	pttrn_cr1a_adpt_en Enable ORing of adapation pattern with pattern CR1A
10:6	RW	0x00	pttrn_cr1b_4_0 Value of pattern B for 1st correlator (bits 4:0)
5:1	RW	0x00	pttrn_msk_cr1b_4_0 Value of pattern B mask for 1st correlator (bits 4:0)
0	RW	0x0	pttrn_cr1b_en Enable pattern B matching for 1st correlator

LANE3_DIG_RX_STAT_STAT_CTL0

Address: Operational Base + offset (0x1384)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_en Value of skip_en_r
14	RW	0x1	sc_timer_mode Sample counter operation mode 1'b0: Counts number of matched samples 1'b1: Counts clock cycles (i.e. a timer)
13	RW	0x0	stat_rxclk_sel Select stat clock 1'b0: Ref_range_clk 1'b1: Rx_dig_clk (i.e. RX dword clk) Before changing stat_rxclk_sel_r from 1->0, the rx_dig_clk must be active (i.e. enabled)
12:10	RW	0x0	stat_src_sel Select stat source input 3'b000: {20{rx_cal_result}} 3'b001: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 3'b010: Rx_phase[39:0] 3'b011: Rx_error[39:0] 3'b100: Rx_data[39:0] 3'b101: Rx_phdir[39:0] 3'b110: 40'hFF_FFFF_FFFF others: Reserved
9:6	RW	0x0	stat_shft_sel Select stat source shift value 4'b0000: Correlate N-1 -> N+3 (use N for offset calibration) 4'b0001: Correlate N+1 -> N+5 (for taps1-5) 4'b0010: Correlate N+6 -> N+10 4'b0011: Correlate N+11 -> N+15 4'b0100: Correlate N+16 -> N+20 4'b0101: Correlate N+21 -> N+25 4'b0110: Correlate N+26 -> N+30 4'b0111: Correlate N+31 -> N+35 4'b1000: Correlate N+36 -> N+39 others: Reserved Setting 0x8 is only used in 20b mode (for checking corr on bits 36-39)
5	RW	0x0	corr_mode_en Enable correlation mode
4:3	RW	0x0	corr_src_sel Select correlation input source 2'b00: Rx_error[39:0] 2'b01: Rx_phase[39:0] 2'b10: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 2'b11: No correlation
2	RW	0x0	corr_shft_sel Select shift for phase. 1'b0: None 1'b1: >>1
1	RW	0x0	corr_shft_sel_vga Select shift for error going to VGA. 1'b0: None 1'b1: >>1

Bit	Attr	Reset Value	Description
0	RW	0x0	reserved_0 Reserved bit

LANE3_DIG_RX_STAT_STAT_CTL1

Address: Operational Base + offset (0x1385)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	vld_ctl Gating configuration of stats collection 2'b00: Ignore both cdr_valid and rx_valid 2'b01: Gate stats collection with cdr_valid 2'b10: Gate stats collection with rx_valid 2'b11: Ignore both cdr_valid and rx_valid
13	RW	0x0	vld_loss_clr Clearing of stats collection upon loss of valid 1'b0: Hold sample and stat counters 1'b1: Clear sample and stat counters
12:11	RW	0x0	data_dly_sel For clock cycle delays on rx_data[19:0], an additional MSB is added in data_dly_sel_2
10	RW	0x0	stat_clk_en Clock gate enable for stat clock
9	RW	0x0	sc_pause Pause the sample counter and stat counters
8:7	RW	0x0	reserved_8_7 Reserved bits
6	RW	0x0	stat_cnt_6_en Enable for stat counter 6
5	RW	0x0	stat_cnt_5_en Enable for stat counter 5
4	RW	0x0	stat_cnt_4_en Enable for stat counter 4
3	RW	0x1	stat_cnt_3_en Enable for stat counter 3 only counter to be enabled by default, since used for offset calibration
2	RW	0x0	stat_cnt_2_en Enable for stat counter 2
1	RW	0x0	stat_cnt_1_en Enable for stat counter 1
0	RW	0x0	stat_cnt_0_en Enable for stat counter 0

LANE3_DIG_RX_STAT_SMPL_CNT1

Address: Operational Base + offset (0x1386)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	smpl_cnt1 Current value of sample counter #1

LANE3_DIG_RX_STAT_STAT_CNT_0

Address: Operational Base + offset (0x1387)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_0 Current value of stat counter #0

LANE3_DIG_RX_STAT_STAT_CNT_1
Address: Operational Base + offset (0x1388)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_1 Current value of stat counter #1

LANE3_DIG_RX_STAT_STAT_CNT_2
Address: Operational Base + offset (0x1389)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_2 Current value of stat counter #2

LANE3_DIG_RX_STAT_STAT_CNT_3
Address: Operational Base + offset (0x138A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_3 Current value of stat counter #3

LANE3_DIG_RX_STAT_STAT_CNT_4
Address: Operational Base + offset (0x138B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_4 Current value of stat counter #4

LANE3_DIG_RX_STAT_STAT_CNT_5
Address: Operational Base + offset (0x138C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_5 Current value of stat counter #5

LANE3_DIG_RX_STAT_STAT_CNT_6
Address: Operational Base + offset (0x138D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_6 Current value of stat counter #6

LANE3_DIG_RX_STAT_CAL_COMP_CLK_CTL

Address: Operational Base + offset (0x138E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RW	0x3	ref_div_cnt Ref range clock count (e.g. 5'd3 = 4 ref_range cycles)
2:0	RW	0x1	prechrge_cnt Precharge count (e.g. 5'd1 = 2 ref_range cycles)

LANE3_DIG_RX_STAT_MATCH_CTL2

Address: Operational Base + offset (0x138F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1a_19_5 Value of pattern A for 1st correlator (bits 19:5)

LANE3_DIG_RX_STAT_MATCH_CTL3

Address: Operational Base + offset (0x1390)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1a_19_5 Value of pattern A mask for 1st correlator (bits 19:5)

LANE3_DIG_RX_STAT_MATCH_CTL4

Address: Operational Base + offset (0x1391)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1b_19_5 Value of pattern B for 1st correlator (bits 19:5)

LANE3_DIG_RX_STAT_MATCH_CTL5

Address: Operational Base + offset (0x1392)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1b_19_5 Value of pattern B mask for 1st correlator (bits 19:5)

LANE3_DIG_RX_STAT_STAT_CTL2

Address: Operational Base + offset (0x1393)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	scope_dly_2 Additional MSB bit for SCOPE_DLY to extend the delay range to 0->7
0	RW	0x0	data_dly_sel_2 Additional MSB bit for data_dly_sel to extend the delay range to 0->7

LANE3_DIG_RX_STAT_STAT_STOP

Address: Operational Base + offset (0x1394)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	sc1_stop Stop sample counters #1 and associated stat counters. This is a self-clearing bit, and requires re-start of sample counter #1.

LANE3_DIG_ANA_TX_OVRD_OUT

Address: Operational Base + offset (0x13A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	tx_ovrd_en Enable override values for all outputs controlled by this register
0	RW	0x0	tx_ana_reset Override value for tx_ana_reset

LANE3_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT

Address: Operational Base + offset (0x13A1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	tx_ana_lpbk_dfe_mode Value for tx_ana_lpbk_dfe_mode

LANE3_DIG_ANA_RX_DIV_OVRD_OUT

Address: Operational Base + offset (0x13A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_ana_div5_en Override value for rx_ana_div5_en
0	RW	0x0	rx_ana_div13p5_en Override value for rx_ana_div13p5_en

LANE3_DIG_ANA_RX_CTL_OVRD_OUT

Address: Operational Base + offset (0x13A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_lbk_clk_en_ovrd Enable override value for rx_ana_loopback_clk_en
14	RW	0x0	rx_ana_adaptation_en_ovrd Enable override value for rx_ana_adaptation_en
13	RW	0x0	rx_ana_dfe_taps_en_ovrd Enable override value for rx_ana_dfe_taps_en
12	RW	0x0	rx_ana_div4_en_ovrd Enable override value for rx_ana_div4_en
11	RW	0x0	rx_ana_word_clk_en_ovrd Enable override value for rx_ana_word_clk_en
10	RW	0x0	rx_ana_data_rate_en_ovrd Enable override values for rx_ana_data_rate[3:0]
9	RW	0x0	rx_lbk_clk_en Override value for rx_ana_loopback_clk_en
8	RW	0x0	rx_ana_adaptation_en Override value for rx_ana_adaptation_en
7	RW	0x0	rx_ana_dfe_taps_en Override value for rx_ana_dfe_taps_en
6	RW	0x0	rx_ana_div4_en Override value for rx_ana_div4_en
5	RW	0x0	rx_ana_word_clk_en Override value for rx_ana_word_clk_en
4:1	RW	0x0	rx_ana_data_rate Override value for rx_ana_data_rate
0	RW	0x0	reserved Reserved

LANE3_DIG_ANA_RX_PWR_OVRD_OUT
Address: Operational Base + offset (0x13A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_ana_deserial_en_ovrd Enable override value for rx_ana_deserial_en
12	RW	0x0	rx_ana_cdr_en_ovrd Enable override value for rx_ana_cdr_en
11	RW	0x0	rx_ana_clk_en_ovrd Enable override value for rx_ana_clk_en
10	RW	0x0	rx_ana_clk_dcc_en_ovrd Enable override value for rx_ana_clk_dcc_en
9	RW	0x0	rx_ana_clk_vreg_en_ovrd Enable override value for rx_ana_clk_vreg_en
8	RW	0x0	rx_ana_afe_en_ovrd Enable override value for rx_ana_afe_en
7	RW	0x0	Reserve_0 Reserve_0
6	RW	0x0	rx_ana_deserial_en Override value for rx_ana_deserial_en
5	RW	0x0	rx_ana_cdr_en Override value for rx_ana_cdr_en
4	RW	0x0	rx_ana_clk_en Override value for rx_ana_clk_en

Bit	Attr	Reset Value	Description
3	RW	0x0	rx_ana_clk_dcc_en Override value for rx_ana_clk_dcc_en
2	RW	0x0	rx_ana_clk_vreg_en Override value for rx_ana_clk_vreg_en
1	RW	0x0	rx_ana_afe_en Override value for rx_ana_afe_en
0	RW	0x0	Reserve_1 Reserve_1

LANE3_DIG_ANA_RX_VCO_OVRD_OUT_0
Address: Operational Base + offset (0x13A9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_cdr_freq_tune_ovrd_en Enable override value for rx_ana_cdr_freq_tune
14	RW	0x0	rx_ana_vco_cntr_clk Override value for rx_ana_vco_cntr_clk
13	RW	0x0	rx_ana_vco_cntr_en Override value for rx_ana_vco_cntr_en
12:3	RW	0x000	rx_ana_cdr_freq_tune Override value for rx_ana_cdr_freq_tune
2	RW	0x0	rx_vco_cdr_ovrd_en Enable override values for cdr_vco_en and cdr_startup
1	RW	0x0	rx_ana_cdr_startup Override value for rx_ana_cdr_startup
0	RW	0x0	rx_ana_cdr_vco_en Override value for rx_ana_cdr_vco_en

LANE3_DIG_ANA_RX_VCO_OVRD_OUT_1
Address: Operational Base + offset (0x13AA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_cdr_vco_highfreq Override value for rx_ana_cdr_vco_highfreq
1	RW	0x1	rx_ana_vco_cntr_pd Override value for rx_ana_vco_cntr_pd
0	RW	0x0	rx_ana_cdr_vco_lowfreq Override value for rx_ana_cdr_vco_lowfreq

LANE3_DIG_ANA_RX_VCO_OVRD_OUT_2
Address: Operational Base + offset (0x13AB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	cdr_freq_tune_clk_self_clear_disable Disable self-clearing for the rx_ana_cdr_freq_tune_clk register
0	RW	0x0	rx_ana_cdr_freq_tune_clk Override value for rx_ana_cdr_freq_tune_clk - self-clearing to generate a pulse 1 cr_clk wide

LANE3_DIG_ANA_RX_CAL

Address: Operational Base + offset (0x13AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_ana_cal_comp_en Value for rx_ana_cal_comp_en
14:13	RW	0x0	rx_ana_cal_mode Value for rx_ana_cal_mode[1:0] 2'b00: Dual differential comparison ([vip2 - vim2] greater than [vip1 - vim1]) 2'b01: Differential comparison on input2 (vip2 greater than vim2) 2'b10: Single-ended comparison, negative node to negative node (vim1 greater than vim2) 2'b11: Common mode comparison (vcm2 greater than vcm1)
12	RW	0x0	rx_ana_slicer_cal_en Value for rx_ana_slicer_cal_en
11	RW	0x0	reserved Reserved
10	RW	0x0	rx_ana_cal_lpfbyp_en Value for rx_ana_cal_lpfbyp_en
9:5	RW	0x00	rx_ana_cal_muxb_sel Value for rx_ana_cal_muxb_sel[4:0]
4:0	RW	0x00	rx_ana_cal_muxa_sel Value for rx_ana_cal_muxa_sel[4:0]

LANE3_DIG_ANA_RX_DAC_CTRL

Address: Operational Base + offset (0x13AD)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	rx_ana_cal_dac_ctrl Value for rx_ana_cal_dac_ctrl[7:0]

LANE3_DIG_ANA_RX_DAC_CTRL_OVRD

Address: Operational Base + offset (0x13AE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_cal_dac_ctrl_ovrd Override enable for cal DAC control

LANE3_DIG_ANA_RX_DAC_CTRL_SEL

Address: Operational Base + offset (0x13AF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_ana_cal_dac_ctrl_sel Value for rx_ana_cal_dac_ctrl_sel[4:0]

LANE3_DIG_ANA_RX_AFE_ATT_VGA

Address: Operational Base + offset (0x13B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:14	RW	0x0	rx_ana_afe_rate Value for rx_ana_afe_rate[1:0]
13:12	RW	0x3	rx_ana_afe_ctle_pole Value for rx_ana_afe_ctle_pole[1:0]
11	RW	0x0	rx_afe_rate_ovrd_en Override enable for rx_ana_afe_rate
10	RW	0x0	rx_ctle_pole_ovrd_en Override enable for rx_ana_ctle_pole
9	RW	0x0	rx_afe_gain_ovrd_en Override enable for rx_ana_afe_gain
8	RW	0x0	rx_afe_att_lvl_ovrd_en Override enable for rx_ana_afe_att_lvl
7	RW	0x0	rx_afe_update_ovrd_en Override enable for rx_ana_afe_update
6:3	RW	0x0	rx_ana_afe_gain Value for rx_ana_afe_gain[3:0]
2:0	RW	0x0	rx_ana_afe_att_lvl Value for rx_ana_afe_att_lvl[2:0]

LANE3_DIG_ANA_RX_AFE_CTLE

Address: Operational Base + offset (0x13B1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_afe_ctle_boost_ovrd_en Override enable for rx_ana_afe_ctle_boost
4:0	RW	0x00	rx_ana_afe_ctle_boost Value for rx_ana_afe_ctle_boost[4:0]

LANE3_DIG_ANA_RX_SCOPE

Address: Operational Base + offset (0x13B2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_scope_self_clear_disable Disable the self-clearing for rx_ana_scope_ph_clk register
12	RW	0x0	rx_ana_scope_clk_en Enable the scope clocks going to the scope slicer and the lane digital part
11:4	RW	0x00	rx_ana_scope_phase Sets value for rx_ana_scope_phase[7:0]
3	RW	0x0	rx_ana_scope_ph_clk Sets value for rx_ana_scope_ph_clk, this bit is self-clearing (i.e. only asserts for one cr_clk cycle)
2:1	RW	0x0	rx_ana_scope_sel Sets value for rx_ana_scope_sel 2'b00: AFE scope selected 2'b01: DFE even scope selected 2'b10: DFE odd scope selected 2'b11: DFE bypass/AFE buffer scope selected
0	RW	0x0	rx_ana_scope_en Sets value for rx_ana_scope_en

LANE3_DIG_ANA_RX_SLICER_CTRL
Address: Operational Base + offset (0x13B3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	rx_ana_slicer_ctrl_ovrd_en Override enable for RX ANA slicer ctrl
7:4	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANE3_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST
Address: Operational Base + offset (0x13B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_ana_iq_phase_adjust Value for rx_ana_iq_phase_adjust[6:0]

LANE3_DIG_ANA_RX_ANA_IQ_SENSE_EN
Address: Operational Base + offset (0x13B5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_ana_iq_sense_en Value for rx_ana_iq_sense_en

LANE3_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN
Address: Operational Base + offset (0x13B6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	dac_ctrl_self_clear_disable Disable self-clearing for the rx_ana_cal_dac_ctrl_en register
0	RW	0x0	rx_ana_cal_dac_ctrl_en Value for rx_ana_cal_dac_ctrl_en, if DAC_CTRL_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE3_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE
Address: Operational Base + offset (0x13B7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	afe_update_self_clear_disable Disable self-clearing for the rx_ana_afe_update_en register

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_ana_afe_update_en Value for rx_ana_afe_update_en, if AFE_UPDATE_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE3_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK

Address: Operational Base + offset (0x13B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	phase_adjust_self_clear_disable Disable self-clearing for the rx_ana_iq_phase_adjust_clk register
0	RW	0x0	rx_ana_iq_phase_adjust_clk Value for rx_ana_iq_phase_adjust_clk, if PHASE_ADJUST_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANE3_DIG_ANA_STATUS_0

Address: Operational Base + offset (0x13B9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RO	0x0	rx_ana_scope_data Value from ANA for rx_ana_scope_data
2	RO	0x0	rx_ana_cal_result Value from ANA for rx_ana_cal_result
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	tx_ana_loopback_en Value of tx_ana_loopback_en

LANE3_DIG_ANA_STATUS_1

Address: Operational Base + offset (0x13BA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_ana_vco_cntr Value from ANA for rx_ana_vco_cntr

LANE3_DIG_ANA_STATUS_LOS

Address: Operational Base + offset (0x13BB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RO	0x0	rx_ana_los_threshold Value to ANA for rx_ana_los_threshold
2	RO	0x0	rx_ana_los_en Value to ANA for rx_ana_los_en
1	RO	0x0	rx_ana_los_clk_en Value to ANA for rx_ana_los_clk_en

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_ana_los Value from ANA for rx_ana_los

LANE3_DIG_ANA_CREGS_TX_ANA_ATB_REG
Address: Operational Base + offset (0x13C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:3	RW	0x0	tx_ana_nc Reserved bit
2:1	RW	0x0	tx_ana_meas_atb BIST TX ATB measurement control
0	RW	0x0	tx_ana_meas_atb_en BIST TX ATB measurement enable

LANE3_DIG_ANA_CREGS_RX_ANA_EQ_CTRL
Address: Operational Base + offset (0x13C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x1	rx_ana_phdet_odd DFE sample control
4	RW	0x1	rx_ana_phdet_even DFE sample control
3:2	RW	0x1	rx_ana_ctle_offset_cal_enb EQ offset calibration enable
1:0	RW	0x0	rx_ana_afe_bias_mt EQ bias control

LANE3_DIG_ANA_CREGS_RX_ANA_VCO_CTRL
Address: Operational Base + offset (0x13C5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x1	rx_ana_cdr_vco_temp_comp_en VCO temperature compensation enable
1:0	RW	0x0	rx_ana_cdr_vco_startup_code VCO startup code

LANE3_DIG_ANA_CREGS_RX_ANA_VREG_CTRL
Address: Operational Base + offset (0x13C6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_vreg_ovrd_clk_vref VREG clk override reference voltage
4	RW	0x0	rx_ana_vreg_ovrd_vco_vref VREG VCO override reference voltage
3	RW	0x0	rx_ana_vreg_ovrd_vro_vref VREG VRO override reference voltage

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_ana_vreg_ovrd_cp_vref VREG charge-pump override reference voltage
1:0	RW	0x1	rx_ana_vreg_ring_ctrl VREG ring oscillator control

LANE3_DIG_ANA_CREGS_RX_ANA_DISCONNECT
Address: Operational Base + offset (0x13C7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_dc_path_disconnect TBA
1	RW	0x0	rx_ana_disconnect_m TBA
0	RW	0x0	rx_ana_disconnect_p TBA

LANE3_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL
Address: Operational Base + offset (0x13C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_ana_nc Reserved bits for future use

LANE3_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1
Address: Operational Base + offset (0x13C9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RW	0x0000	rx_meas_atb_14_0 Reserved
0	RW	0x0	rx_meas_atb_en Reserved

LANE3_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2
Address: Operational Base + offset (0x13CA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	rx_meas_atb_29_15 Reserved

RAWCMN_DIG_CMN_CTL
Address: Operational Base + offset (0x2000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RW	0x0	phy_func_rst Resets the PHY except registers in the Raw PCS common and always-on registers. Useful for resetting the PHY after reloading the Memory and without resetting the memory.

RAWCMN_DIG_CR_EXT_REG_OP_XTND
Address: Operational Base + offset (0x2001)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2:1	RW	0x0	sram_rd_access_delay Configurable access delay for reading through SRAM. 2'b00: 2 cycles 2'b01: 3 cycles 2'b10: 4 cycles 2'b11: 5 cycles
0	RW	0x0	data Required to prevent timing violations while accessing through external interface.

RAWCMN_DIG_CMN_CTL_1
Address: Operational Base + offset (0x2002)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rtune_req_ovrd_en Override enable for rtune_req
0	RW	0x0	rtune_req_ovrd_val Override value for rtune_req

RAWCMN_DIG_AON_CMN_ADAPT_REF_LVL_DAC_CODE
Address: Operational Base + offset (0x2020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x44	adapt_ref_lvl_dac_code Adaptation ref level target dac code for 150mv

RAWCMN_DIG_AON_CMN_RX_RESERVED_REGISTER_0
Address: Operational Base + offset (0x2021)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rsrvd_0 Reserved fields

RAWCMN_DIG_AON_CMN_RX_RESERVED_REGISTER_1
Address: Operational Base + offset (0x2022)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	rsrvd_0 Reserved fields

RAWCMN_DIG_AON_CMN_SUP_OVRD_IN

Address: Operational Base + offset (0x203B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	ref_clk_en_ovrd_en Override enable for ref_clk_en
0	RW	0x0	ref_clk_en_ovrd_val Override value for ref_clk_en

RAWCMN_DIG_CMNFSM_FSM_FSM_OVRD_CTL

Address: Operational Base + offset (0x2040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RW	0x0	fsm_ovrd_en Enable overriding the FSM execution of commands must be asserted to use FSM_CMD_START and FSM_JMP_EN features
13	RW	0x0	fsm_cmd_start Start executing the new command this is a self-clearing bit
12	RW	0x0	fsm_jmp_en Force the FSM to jump to FSM_JMP_ADDR in the program memory is applied when FSM_CMD_START is pulsed.
11:0	RW	0x000	fsm_jmp_addr The jump address used when FSM_JUMP_EN=1, the address is encoded as follows: [11:8] mem_lane, [7:5] bank, [4:0] register

RAWCMN_DIG_CMNFSM_FSM_MEM_ADDR_MON

Address: Operational Base + offset (0x2041)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	mem_addr Current value of memory address used in lane FSM

RAWCMN_DIG_CMNFSM_FSM_STATUS_MON

Address: Operational Base + offset (0x2042)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	rdmsk_disabled Check, if read mask is currently disabled (i.e. mask is all ones)
9	RO	0x0	wrmsk_disabled Check, if write mask is currently disabled (i.e. mask is all ones)
8	RO	0x0	wait_cnt_eq0 Check, if wait counter currently equals zero
7	RO	0x0	alu_res_eq0 Check, if ALU result register currently equals zero

Bit	Attr	Reset Value	Description
6	RO	0x0	alu_ovflw Current value of ALU overflow bit
5	RO	0x0	cmd_rdy New command is ready for execution (applicable when FSM_OVRD_EN=1)
4:0	RO	0x00	state Current state of lane FSM

RAWCMN_DIG_CMNFSM_FSM_CR_REG_OP_XTND_EN

Address: Operational Base + offset (0x2043)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	cr_reg_op_xtnd_en CR interface timing extension enable 1'b0: No timing extension 1'b1: Timing extension

RAWCMN_DIG_CMNFSM_ATB_REQ

Address: Operational Base + offset (0x2044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	atb_request Used to enable ATB state machine in FW

RAWCMN_DIG_CMNFSM_ATB_RESULT_OUT

Address: Operational Base + offset (0x2045)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RW	0x0	atb_done Used to check, if ATB request has been serviced
9:0	RW	0x000	rt_ana_val Contains the final value after ATB req till the new req is asserted (10 bit)

HDMIPCS_DIG_CTRL_XF_HDMI_PWR_CTRL

Address: Operational Base + offset (0x2080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	pddq_ovrd_en Override enable for PDDQ
6	RW	0x0	pddq_ovrd_val Override value for PDDQ
5	RW	0x0	hdmi_disable_ovrd_en Override enable for HDMI_DISABLE
4	RW	0x0	hdmi_disable_ovrd_val Override value for HDMI_DISABLE

Bit	Attr	Reset Value	Description
3	RW	0x0	pddq_ack_ovrd_en Override enable for PDDQ_ACK
2	RW	0x0	pddq_ack_ovrd_val Override value for PDDQ_ACK
1	RW	0x0	hdmi_disable_ack_ovrd_en Override enable for HDMI_DISABLE_ACK
0	RW	0x0	hdmi_disable_ack_ovrd_val Override value for HDMI_DISABLE_ACK

HDMIPCS_DIG_CTRL_XF_REF_FREQ_INFO_OVRD
Address: Operational Base + offset (0x2081)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	reffreq_sel_ovrd_en Override enable for reffreq_sel
10:8	RW	0x1	reffreq_sel_ovrd_val Override value for reffreq_sel
7	RW	0x0	ref_freq_ovrd_en Override enable for ref freq setting
6:0	RW	0x64	ref_freq_ovrd_val Override value for ref freq in MHz

HDMIPCS_DIG_CTRL_XF_HDMI_CONFIG_OVRD
Address: Operational Base + offset (0x2082)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rxdata_width_ovrd_en Override enable for RXDATA_WIDTH
14	RW	0x0	rxdata_width_ovrd_val Override value for RXDATA_WIDTH
13	RW	0x0	tmds_clock_ratio_ovrd_en Override enable for TMDS_CLOCK_RATIO
12	RW	0x0	tmds_clock_ratio_ovrd_val Override value for TMDS_CLOCK_RATIO
11	RW	0x0	frl_rate_ovrd_en Override enable for FRL_RATE
10:7	RW	0x6	frl_rate_ovrd_val Override value for FRL_RATE
6	RW	0x0	phy_mode_ovrd_en Override enable for PHY_MODE
5	RW	0x0	phy_mode_ovrd_val Override value for PHY_MODE
4	RW	0x0	frl_lane_num_ovrd_en Override enable for FRL_LANE_NUM
3	RW	0x0	frl_lane_num_ovrd_val Override value for FRL_LANE_NUM
2	RW	0x0	frl_bit_rate_ovrd_en Override enable for FRL_BIT_RATE
1:0	RW	0x3	frl_bit_rate_ovrd_val Override value for FRL_BIT_RATE

HDMIPCS_DIG_CTRL_XF_LTP_UPDATE_STATUS_OVRD

Address: Operational Base + offset (0x2083)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	flt_update_status_ovrd_en Override enable for FLT_UPDATE_STATUS
0	RW	0x0	flt_update_status_ovrd_val Override value for FLT_UPDATE_STATUS

HDMIPCS_DIG_CTRL_XF_LTP_REQ_OVRD

Address: Operational Base + offset (0x2084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	ln0_ltp_req_ovrd_val Override value for LTP_REQ of lane 0
11:8	RW	0x0	ln1_ltp_req_ovrd_val Override value for LTP_REQ of lane 1
7:4	RW	0x0	ln2_ltp_req_ovrd_val Override value for LTP_REQ of lane 2
3:0	RW	0x0	ln3_ltp_req_ovrd_val Override value for LTP_REQ of lane 3

HDMIPCS_DIG_CTRL_XF_LTP_OVRD_EN

Address: Operational Base + offset (0x2085)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	ln0_ltp_req_ovrd_en Override enable for LTP_REQ of lane 0
2	RW	0x0	ln1_ltp_req_ovrd_en Override enable for LTP_REQ of lane 1
1	RW	0x0	ln2_ltp_req_ovrd_en Override enable for LTP_REQ of lane 2
0	RW	0x0	ln3_ltp_req_ovrd_en Override enable for LTP_REQ of lane 3

HDMIPCS_DIG_CTRL_XF_LTP_CTRL_OVRD

Address: Operational Base + offset (0x2086)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RW	0x0	ffe_levels_ovrd_en Override enable for FFE_LEVELS
9:6	RW	0x0	ffe_levels_ovrd_val Override value for FFE_LEVELS
5	RW	0x0	flt_ready_ovrd_en Override enable for FLT_READY
4	RW	0x0	flt_ready_ovrd_val Override value for FLT_READY
3	RW	0x0	flt_update_ovrd_en Override enable for FLT_UPDATE

Bit	Attr	Reset Value	Description
2	RW	0x0	flt_update_ovrd_val Override value for FLT_UPDATE
1	RW	0x0	rxdata_valid_ovrd_en Override enable for RXDATA_VALID
0	RW	0x0	rxdata_valid_ovrd_val Override value for RXDATA_VALID

HDMIPCS_DIG_CTRL_XF_READAPT_EN

Address: Operational Base + offset (0x2087)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	readapt_self_clear_disable Disable self-clearing for the readapt_en_r register
0	RW	0x0	readapt_en_r Readapt request from creg

HDMIPCS_DIG_CTRL_XF_PCS_INTERFACE_SIG_STATUS_1

Address: Operational Base + offset (0x2088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	rxdata_valid Value to ASIC for rxdata_valid
14	RO	0x0	flt_update Value to ASIC for flt_update
13:11	RO	0x0	reffreq_sel Value from ASIC for reffreq_sel
10	RO	0x0	rxdata_width Value from ASIC for rxdata_width
9	RO	0x0	tmds_clock_ratio Value from ASIC for tmds_clock_ratio
8:5	RO	0x0	frl_rate Value from ASIC for frl_rate
4:1	RO	0x0	ffe_levels Value from ASIC for ffe_levels
0	RO	0x0	flt_update_status Value from ASIC for flt_update_status

HDMIPCS_DIG_CTRL_XF_PCS_INTERFACE_SIG_STATUS_2

Address: Operational Base + offset (0x2089)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	ln3_ltp_req Value to ASIC for ln3_ltp_req
11:8	RO	0x0	ln2_ltp_req Value to ASIC for ln2_ltp_req
7:4	RO	0x0	ln1_ltp_req Value to ASIC for ln1_ltp_req
3:0	RO	0x0	ln0_ltp_req Value to ASIC for ln0_ltp_req

HDMIPCS_DIG_CTRL_XF_POWER_SEQ

Address: Operational Base + offset (0x208A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RO	0x0	pddq Value from ASIC for pddq
2	RO	0x0	pddq_ack_i Value to ASIC for pddq_ack
1	RO	0x0	hdmi_disable Value from ASIC for hdmi_disable
0	RO	0x0	hdmi_disable_ack_i Value to ASIC for hdmi_disable_ack

HDMIPCS_DIG_CTRL_XF_LINK_RETRAIN_REQ_ASIC_OVRD

Address: Operational Base + offset (0x208B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	link_retrain_req_asic_ovrd_en Override enable for link_retrain_req_int
0	RW	0x0	link_retrain_req_asic_ovrd_val Override value for link_retrain_req_int

HDMIPCS_DIG_CTRL_XF_LINK_RETRAIN_REQ

Address: Operational Base + offset (0x208C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	link_retrain_self_clear_disable Disable self-clearing for the link_retrain_req_r register
0	RW	0x0	link_retrain_req_r link retrain request from creg

HDMIPCS_DIG_CTRL_XF_LINK_RETRAIN_REQ_INFO_OVRD

Address: Operational Base + offset (0x208D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	link_retrain_req_ovrd_en Override enable for link_retrain_req_int
0	RW	0x0	link_retrain_req_ovrd_val Override value for link_retrain_req_int

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_6G_EQ_SETTINGS

Address: Operational Base + offset (0x2094)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x2	hdmi21_6g_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI2.1 for 6Gbps in 3/4 lane mode
13:12	RW	0x2	hdmi21_6g_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI2.1 for 6Gbps in 3/4 lane mode

Bit	Attr	Reset Value	Description
11:9	RW	0x0	hdmi21_6g_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI2.1 for 6Gbps in 3/4 lane mode
8:4	RW	0x1f	hdmi21_6g_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI2.1 for 6Gbps in 3/4 lane mode
3:0	RW	0xf	hdmi21_6g_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI2.1 for 6Gbps in 3/4 lane mode

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_8G_EQ_SETTINGS
Address: Operational Base + offset (0x2095)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x2	hdmi21_8g_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI2.1 for 8Gbps in 4 lane mode
13:12	RW	0x2	hdmi21_8g_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI2.1 for 8Gbps in 4 lane mode
11:9	RW	0x0	hdmi21_8g_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI2.1 for 8Gbps in 4 lane mode
8:4	RW	0x1f	hdmi21_8g_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI2.1 for 8Gbps in 4 lane mode
3:0	RW	0xf	hdmi21_8g_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI2.1 for 8Gbps in 4 lane mode

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_10G_EQ_SETTINGS
Address: Operational Base + offset (0x2096)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x3	hdmi21_10g_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI2.1 for 10Gbps in 4 lane mode
13:12	RW	0x0	hdmi21_10g_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI2.1 for 10Gbps in 4 lane mode
11:9	RW	0x0	hdmi21_10g_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI2.1 for 10Gbps in 4 lane mode
8:4	RW	0x1f	hdmi21_10g_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI2.1 for 10Gbps in 4 lane mode
3:0	RW	0xf	hdmi21_10g_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI2.1 for 10Gbps in 4 lane mode

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_12G_EQ_SETTINGS
Address: Operational Base + offset (0x2097)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x3	hdmi21_12g_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI2.1 for 12Gbps in 4 lane mode
13:12	RW	0x0	hdmi21_12g_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI2.1 for 12Gbps in 4 lane mode
11:9	RW	0x0	hdmi21_12g_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI2.1 for 12Gbps in 4 lane mode
8:4	RW	0x1f	hdmi21_12g_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI2.1 for 12Gbps in 4 lane mode
3:0	RW	0xf	hdmi21_12g_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI2.1 for 12Gbps in 4 lane mode

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_3G_EQ_SETTINGS_TAP

Address: Operational Base + offset (0x2098)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi21_3g_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap1 in HDMI2.1 (3Gbps in 3 lane mode)
7:0	RW	0x00	hdmi21_3g_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI2.1 (3Gbps in 3 lane mode)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_6G_EQ_SETTINGS_TAP

Address: Operational Base + offset (0x2099)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi21_6g_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap1 in HDMI2.1 (6Gbps in 3/4 lane mode)
7:0	RW	0x00	hdmi21_6g_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI2.1 (6Gbps in 3/4 lane mode)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_8G_EQ_SETTINGS_TAP

Address: Operational Base + offset (0x209A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi21_8g_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap1 in HDMI2.1 (8Gbps in 4 lane mode)
7:0	RW	0x00	hdmi21_8g_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI2.1 (8Gbps in 4 lane mode)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_10G_EQ_SETTINGS_TAP

Address: Operational Base + offset (0x209B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi21_10g_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap1 in HDMI2.1 (10Gbps in 4 lane mode)
7:0	RW	0x00	hdmi21_10g_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI2.1 (10Gbps in 4 lane mode)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_12G_EQ_SETTINGS_TAP

Address: Operational Base + offset (0x209C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi21_12g_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap1 in HDMI2.1 (12Gbps in 4 lane mode)
7:0	RW	0x00	hdmi21_12g_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI2.1 (12Gbps in 4 lane mode)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_TMDSCLK_THRESH

Address: Operational Base + offset (0x209D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use

Bit	Attr	Reset Value	Description
14	RW	0x0	tmdsclk_thresh_byp Bypass tmdsclk thesh check for clock_stable
13:5	RW	0x190	tmdsclk_high_thresh Thresh above which clock_stable remains low
4:0	RW	0x0f	tmdsclk_low_thresh Thresh below which clock_stable remains low

HDMIPCS_DIG_DATA_PATH_DATA_PATH_INPUTS
Address: Operational Base + offset (0x20A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	dat_seq_swap reverses the data chronology on the parallel data
10:8	RW	0x4	frl_rxclkx2_en FRL mode clkx2 en 3'b100: Div13.5, 3'b010: Div20, 3'b001: Div10, 3'b000: No rxclkx2 others: Reserved
7:5	RW	0x0	tmds_rxclkx2_en TMDS mode clkx2 en 3'b100: Div13.5, 3'b010: Div20, 3'b001: Div10, 3'b000: No rxclkx2 others: Reserved
4:3	RW	0x0	lane_clk_sel Common clock select for clock aligner FIFO
2	RW	0x0	aligner_bypass Value for ALIGNER_BYPASS
1	RW	0x0	gasket_rd_pos_ovrd_en Override enable for GASKET_RD_POS
0	RW	0x0	gasket_rd_pos_ovrd_val Override value for GASKET_RD_POS

HDMIPCS_DIG_DATA_PATH_DATA_PATH_INPUT_OVRD
Address: Operational Base + offset (0x20A1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	fifo_en_ovrd_en Override enable for FIFO_EN
6	RW	0x0	fifo_en_ovrd_val Override value for FIFO_EN
5	RW	0x0	flt_long_timeout_ovrd_en Override enable for FLT_LONG_TIMEOUT_EN
4	RW	0x0	flt_long_timeout_ovrd_val Override value for FLT_LONG_TIMEOUT_EN
3	RW	0x0	rx_clk_div_en_ovrd_en Override enable for RX_CLK_DIV_EN

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_clk_div_en_ovrd_val Override value for RX_CLK_DIV_EN
1	RW	0x0	rx_reset_ovrd_en Override enable for RX_RESET
0	RW	0x0	rx_reset_ovrd_val Override value for RX_RESET

HDMIPCS_DIG_DATA_PATH_FRL_COMMA_CHAR

Address: Operational Base + offset (0x20A2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	frl_strict_byte_align 1-Byte will misalign, if comma character change its position even once. 0-byte will remain align for one change of position of comma character
12:0	RW	0x1011	frl_comma FRL mode comma character control word maximum 13 bits allowed of position [16:4] from 18 bits

HDMIPCS_DIG_DATA_PATH_FRL_VALID_DATA_TIMEOUT

Address: Operational Base + offset (0x20A3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RW	0x0715	valid_timeout_count FRL mode data word count for absence of data detection after valid about 3 SB in 3 lane mode
0	RW	0x1	valid_timeout_enable FRL mode enable data word count for absence of data detection after valid

HDMIPCS_DIG_DATA_PATH_FRL_DATA_LOCK_DETECT_TIMEOUT

Address: Operational Base + offset (0x20A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RW	0x2aa2	lock_detect_timeout_count FRL mode data word count for absence of SR/SSB detection after CDR lock and adaptation
0	RW	0x1	lock_detect_timeout_enable FRL mode enable data word count for absence of SR/SSB detection after CDR lock and adaptation

HDMIPCS_DIG_DATA_PATH_DATA_PATH_OUTPUT_OVRD

Address: Operational Base + offset (0x20A5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx0_byte_aligned_ovrd_en Override enable for RX0_BYTE_ALIGNED
14	RW	0x0	rx0_byte_aligned_ovrd_val Override value for RX0_BYTE_ALIGNED
13	RW	0x0	rx1_byte_aligned_ovrd_en Override enable for RX1_BYTE_ALIGNED

Bit	Attr	Reset Value	Description
12	RW	0x0	rx1_byte_aligned_ovrd_val Override value for RX1_BYTE_ALIGNED
11	RW	0x0	rx2_byte_aligned_ovrd_en Override enable for RX2_BYTE_ALIGNED
10	RW	0x0	rx2_byte_aligned_ovrd_val Override value for RX2_BYTE_ALIGNED
9	RW	0x0	rx3_byte_aligned_ovrd_en Override enable for RX3_BYTE_ALIGNED
8	RW	0x0	rx3_byte_aligned_ovrd_val Override value for RX3_BYTE_ALIGNED
7	RW	0x0	ln0_timed_out_ovrd_en Override enable for LN0_TIMED_OUT
6	RW	0x0	ln0_timed_out_ovrd_val Override value for LN0_TIMED_OUT
5	RW	0x0	ln1_timed_out_ovrd_en Override enable for LN1_TIMED_OUT
4	RW	0x0	ln1_timed_out_ovrd_val Override value for LN1_TIMED_OUT
3	RW	0x0	ln2_timed_out_ovrd_en Override enable for LN2_TIMED_OUT
2	RW	0x0	ln2_timed_out_ovrd_val Override value for LN2_TIMED_OUT
1	RW	0x0	ln3_timed_out_ovrd_en Override enable for LN3_TIMED_OUT
0	RW	0x0	ln3_timed_out_ovrd_val Override value for LN3_TIMED_OUT

HDMIPCS_DIG_DATA_PATH_GSKT_STATUS

Address: Operational Base + offset (0x20A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	gasket_rd_pos Indicates FRL word formation

HDMIPCS_DIG_DATA_PATH_BYTE_ALIGN_STATUS

Address: Operational Base + offset (0x20A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RO	0x0	rx_alignment_done Indicates value of rx_alignment_done
3	RO	0x0	rx0_byte_aligned_i Indicates value of rx3_byte_aligned
2	RO	0x0	rx1_byte_aligned_i Indicates value of rx2_byte_aligned
1	RO	0x0	rx2_byte_aligned_i Indicates value of rx1_byte_aligned
0	RO	0x0	rx3_byte_aligned_i Indicates value of rx0_byte_aligned

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_RATE_CALC_OVRD

Address: Operational Base + offset (0x20C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	ref_range_calc_done_ovrd_en Override enable for REF_RANGE_CALC_DONE
10	RW	0x0	ref_range_calc_done_ovrd_val Override value for REF_RANGE_CALC_DONE
9	RW	0x0	ld_calc_done_ovrd_en Override enable for LD_CALC_DONE
8	RW	0x0	ld_calc_done_ovrd_val Override value for LD_CALC_DONE
7	RW	0x0	cmu_en_ovrd_en Override enable for CMU_EN
6	RW	0x0	cmu_en_ovrd_val Override value for CMU_EN
5	RW	0x0	ref_range_calc_en_ovrd_en Override enable for REF_RANGE_CALC_EN
4	RW	0x0	ref_range_calc_en_ovrd_val Override value for REF_RANGE_CALC_EN
3	RW	0x0	clock_stable_ovrd_en Override enable for CLOCK_STABLE
2	RW	0x0	clock_stable_ovrd_val Override value for CLOCK_STABLE
1	RW	0x0	ld_calc_en_ovrd_en Override enable for LD_CALC_EN
0	RW	0x0	ld_calc_en_ovrd_val Override value for LD_CALC_EN

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_PHY_CONTROL

Address: Operational Base + offset (0x20C1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	rx_adapt_cont If mission mode adaptation should be enabled
8	RW	0x0	rx_offcan_cont If mission mode calibration should be enabled
7:6	RW	0x2	hdmi_pwrdn_state HDMI power down state
5:1	RW	0x11	rx_vref_ctrl Bandgap reference voltage select. Nominal value decimal 17.
0	RW	0x0	rx_cdr_ssc_en CDR ssc enable control

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_PCS_DEBUG

Address: Operational Base + offset (0x20C2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use

Bit	Attr	Reset Value	Description
4:0	RW	0x00	dtb_sel Select to drive various signals onto the dtb 5'b00000: Disabled 5'b00001: PCS main_state 5'b00010: 0, ln3_timeout, ln2_timeout, ln1_timeout, ln0_timeout 5'b00011: Ln1_ffe_levels_used[2:0], ln0_ffe_levels_used[1:0] 5'b00100: Ln3_ffe_levels_used[2:0], ln2_ffe_levels_used[1:0] 5'b00101: Rx_alignment_done, rx3_byte_aligned, rx2_byte_aligned, rx1_byte_aligned, rx0_byte_aligned 5'b00110: Fom_not_good, program_ln3_to_best_ffe, program_ln2_to_best_ffe, program_ln1_to_best_ffe, program_ln0_to_best_ffe 5'b00111: Tmdsclk,rx3_dig_ovl_det_0V, rx2_dig_ovl_det_0V, rx1_dig_ovl_det_0V, rx0_dig_ovl_det_0V 5'b01000: Clock_stable, main_state[3:0] 5'b01001: Flt_bypass, main_state[3:0] 5'b01010: Clock_stable, lane_needs_pwrdn, ext_config_change, data_valid_int_d, rx_clk_div_disabled_i 5'b01011: 2'b0, rxclk_out_en, rx_cdr_vco_highfreq, rx_cdr_vco_lowfreq 5'b01100: 0, rx0_valid, rx1_valid, rx2_valid, rx3_valid 5'b01101: 0, rx_rate others: Reserved

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LTP_PATTERN_REQ

Address: Operational Base + offset (0x20C3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x5	ltp_pattern_5 LTP pattern 5
11:8	RW	0x6	ltp_pattern_6 LTP pattern 6
7:4	RW	0x7	ltp_pattern_7 LTP pattern 7
3:0	RW	0x8	ltp_pattern_8 LTP pattern 8

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_CONFIG

Address: Operational Base + offset (0x20C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	fpga_pma_pwrup Skip pma CDR handover and adaptation
10	RW	0x0	frl_lane_num_bootup Frl_lane_num at bootup
9	RW	0x1	rxdata_width_bootup Rxdata_width at bootup
8	RW	0x1	phy_mode_bootup Phy_mode at bootup
7:6	RW	0x3	frl_bit_rate_bootup Frl_bit_rate at bootup
5	RW	0x1	tmds_clock_ratio_bootup Tmds_clock_ratio at bootup

Bit	Attr	Reset Value	Description
4	RW	0x0	flt_bypass Bypass FRL link training when asserted
3	RW	0x0	skip_rertune Do rtune only first time after pddq removal
2	RW	0x1	supportsffe If '0' ffe_levels not checked and new ffe setting request is never made
1	RW	0x0	dont_stop_ref_clk Ref_clk is stoppped to save power by default
0	RW	0x1	redo_rtune Do rtune everytime pddq'd

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LTP_STATUS_UPDATE

Address: Operational Base + offset (0x20C5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:8	RW	0xf	change_frl_rate LTP request to suggest FLT has failed for this FRL_RATE and rate should be updated
7:4	RW	0xe	ffe_req_update LTP request to suggest TxFFE update is needed
3:0	RW	0x0	flt_successful LTP request to suggest FLT is successful

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_CONTROL

Address: Operational Base + offset (0x20C6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:1	RW	0x00	force_state State to enter when force_state_change is 1
0	RW	0x0	force_state_change Enable force FSM to change state

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_ADAPT_REF_FOM

Address: Operational Base + offset (0x20C7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	adapt_ref_fom Minimum reference FOM needed for successful LTP (reset value to be updated in pcs_raw_macros)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_HDMI_STATUS

Address: Operational Base + offset (0x20C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	byte_misalign_in_fsmdone Indicates value of byte_misalign_in_fsmdone

Bit	Attr	Reset Value	Description
14	RO	0x0	frl_fast_relock Indicates value of frl_fast_relock
13	RO	0x0	power_seq_complete Indicates value of power_seq_complete
12	RO	0x0	readapt_en_cur Indicates currently active readapt_en
11	RO	0x0	phy_mode_cur Indicates currently active PHY mode
10	RO	0x0	frl_lane_num_cur Indicates currently active FRL lane mode (3/4)
9:8	RO	0x0	frl_bit_rate_cur Indicates currently active FRL bit ratee
7	RO	0x0	tmds_clock_ratio_cur Indicates currently active TMDS mode status
6	RO	0x0	rxdata_width_cur Indicates currently active rxdata width configuration
5	RO	0x0	stress_int Indicates overload detection in one of the lanes
4	RO	0x0	lane_needs_pwrdn Indicates change in pddq or hdmi_disable or source has indicated rate change
3	RO	0x0	ext_config_change Indicates either frl_rate has changed or tmds_clock_ratio or rxdata_width
2	RO	0x0	hdmi_config_change Indicates either external configuration has changed or clock_stable has changed
1	RO	0x0	cdr_is_locked Indicates successful valid from all active lanes after complete powerup
0	RO	0x0	data_valid_int Internal rxdata_valid indicates successful byte alignment and skew alignment

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FFE_STATUS
Address: Operational Base + offset (0x20C9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:13	RO	0x0	ln3_best_ffe_setting Indicates target ffe setting for lane 3, if try_all_ffe is '0'
12:11	RO	0x0	ln2_best_ffe_setting Indicates target ffe setting for lane 2, if try_all_ffe is '0'
10:9	RO	0x0	ln1_best_ffe_setting Indicates target ffe setting for lane 1, if try_all_ffe is '0'
8:7	RO	0x0	ln0_best_ffe_setting Indicates target ffe setting for lane 0, if try_all_ffe is '0'
6	RO	0x0	program_ln3_to_best_ffe Indicates FSM has tried all the ffe settings and is programming lane 3 TX to the best ffe configuration
5	RO	0x0	program_ln2_to_best_ffe Indicates FSM has tried all the ffe settings and is programming lane 2 TX to the best ffe configuration

Bit	Attr	Reset Value	Description
4	RO	0x0	program_ln1_to_best_ffe Indicates FSM has tried all the ffe settings and is programming lane 1 TX to the best ffe configuration
3	RO	0x0	program_ln0_to_best_ffe Indicates FSM has tried all the ffe settings and is programming lane 0 TX to the best ffe configuration
2	RO	0x0	try_all_ffe Indicates that main_FSM is just checking the fom and lock status for all available ffe settings
1:0	RO	0x0	ffe_levels_tried Number of ffe levels which are tried during first run

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_POWER_STATUS

Address: Operational Base + offset (0x20CA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	fifo_en If asserted indicates FSM has enabled PCS data path
13	RO	0x0	rx3_adapt_req If asserted indicates FSM has requested adaptation for lane 3
12	RO	0x0	rx2_adapt_req If asserted indicates FSM has requested adaptation for lane 2
11	RO	0x0	rx1_adapt_req If asserted indicates FSM has requested adaptation for lane 1
10	RO	0x0	rx0_adapt_req If asserted indicates FSM has requested adaptation for lane 0
9:8	RO	0x0	rx3_pstate If '00' indicates FSM has requested lane 3 to full power up
7:6	RO	0x0	rx0_pstate If '00' indicates FSM has requested lane 0/1/2 to full power up
5	RO	0x0	cmu_en If asserted indicates TMDS receiver is enabled and clock measurement unit is active
4	RO	0x0	ref_clk_en If asserted indicates ref_clk and cr clk is enabled
3	RO	0x0	hdmi_disable_cur If asserted indicates HDMI is still disabled and only bg is running
2	RO	0x0	bg_done If asserted indicates bandgap is stable and enabled
1	RO	0x0	bg_en If asserted indicates bandgap is requested to be enabled
0	RO	0x0	pddq_cur If asserted indicates HDMI is in lowest power state with everything disabled

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_MISC_STATUS

Address: Operational Base + offset (0x20CB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ln3_timed_out If high, no comma on lane3 detected for long time

Bit	Attr	Reset Value	Description
14	RO	0x0	ln2_timed_out If high, no comma on lane2 detected for long time
13	RO	0x0	ln1_timed_out If high, no comma on lane1 detected for long time
12	RO	0x0	ln0_timed_out If high, no comma on lane0 detected for long time
11	RO	0x0	flt_ongoing_cur If de-asserted, FSM completed link training
10	RO	0x0	vco_refclk_select_i If '0' indicates TMDS clock is used as reference clock for VCO calibration
9	RO	0x0	rx_term_en If asserted indicates termination of all lanes in enabled
8	RO	0x0	flt_ongoing If asserted indicates FSM is performing FRL link training
7	RO	0x0	clock_stable If asserted indicates tmdsclk receiver is receiving stable clock
6	RO	0x0	tmdsclk_rst If deasserted indicates glcm between ref_clk and tmdsclk is released for switchover as tmdsclk is stable
5	RO	0x0	tmdsclk_digmux_en If asserted indicates TMDS clock is used as reference clock for VCO calibration and is enabled
4	RO	0x0	tmdsclk_en If asserted indicates TMDS clock receiver is enabled
3	RO	0x0	ld_calc_done If asserted indicates settings are available for requested data rate
2	RO	0x0	ld_calc_en If asserted indicates FSM has concluded the data rate and settings are requested
1	RO	0x0	ref_range_calc_done If asserted indicates ref_range value for requested reffreq is available
0	RO	0x0	ref_range_calc_en If asserted indicates reffreq info is stable and ref_range value is requested

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FOM_LANE01
Address: Operational Base + offset (0x20CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	ln0_adapt_fom Reflects the best FOM achieved so far for lane 0
7:0	RO	0x00	ln1_adapt_fom Reflects the best FOM achieved so far for lane 1

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FOM_LANE23
Address: Operational Base + offset (0x20CD)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	ln2_adapt_fom Reflects the best FOM achieved so far for lane 2
7:0	RO	0x00	ln3_adapt_fom Reflects the best FOM achieved so far for lane 3

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_INPUT_OVRD
Address: Operational Base + offset (0x20CE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8:4	RW	0x0f	clken_target_cnt Extra time enable for running RX CLOCKS from FSM_DONE to HPDN in FRL mode
3	RW	0x0	rx_alignment_done_ovrd_en Override enable for RX_ALIGNMENT_DONE
2	RW	0x0	rx_alignment_done_ovrd_val Override value for RX_ALIGNMENT_DONE
1	RW	0x0	rx_clk_div_disabled_ovrd_en Override enable for RX_CLK_DIV_DISABLED
0	RW	0x0	rx_clk_div_disabled_ovrd_val Override value for RX_CLK_DIV_DISABLED

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_STATE_STATUS
Address: Operational Base + offset (0x20CF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:8	RO	0x00	next_state FSM next_state status
7:5	RO	0x0	reserved Added to make readability better for next_state and main_state
4:0	RO	0x00	main_state FSM current state

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_1
Address: Operational Base + offset (0x20D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	rx_cdr_vco_highfreq Status of RX_CDR_VCO_HIGHFREQ
14	RO	0x0	rx_cdr_vco_lowfreq Status of RX_CDR_VCO_LOWFREQ
13:11	RO	0x0	rx_cdr_setting_sel Status of RX_CDR_SETTING_SEL
10:3	RO	0x00	rx_eq_dfe_tap1 Status of RX_EQ_DFE_TAP1
2:0	RO	0x0	rx_eq_att_lvl Status of RX_EQ_ATT_LVL

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_2
Address: Operational Base + offset (0x20D1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	rx_adapt_afe_en Status of RX_ADAPT_AFE_EN

Bit	Attr	Reset Value	Description
13	RO	0x0	rx_adapt_dfe_en Status of RX_ADAPT_DFE_EN
12:0	RO	0x0000	rx_vco_ld_val Status of RX_VCO_LD_VAL

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_3
Address: Operational Base + offset (0x20D2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:11	RO	0x0	rx_eq_afe_gain Status of RX_EQ_AFE_GAIN
10:7	RO	0x0	rx_rate Status of RX_RATE
6:0	RO	0x00	rx_ref_ld_val Status of RX_REF_LD_VAL

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_4
Address: Operational Base + offset (0x20D3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	ref_range Status of REF_RANGE
12:9	RO	0x0	rx_eq_delta_iq Status of RX_EQ_DELTA_IQ
8:7	RO	0x0	rx_eq_ctle_pole Status of RX_EQ_CTLE_POLE
6:2	RO	0x00	rx_eq_ctle_boost Status of RX_EQ_CTLE_BOOST
1:0	RO	0x0	rx_eq_afe_rate Status of RX_EQ_AFE_RATE

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_BYTE_ALIGN_CNT_STATUS
Address: Operational Base + offset (0x20D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	rx0_byte_negedge_counter Count of rx0_byte_aligned_sync
11:8	RO	0x0	rx1_byte_negedge_counter Count of rx1_byte_aligned_sync
7:4	RO	0x0	rx2_byte_negedge_counter Count of rx2_byte_aligned_sync
3:0	RO	0x0	rx3_byte_negedge_counter Count of rx3_byte_aligned_sync

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LANE_VALID_STATUS
Address: Operational Base + offset (0x20D5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RO	0x0	rx0_valid Status of rx0_valid from PMA

Bit	Attr	Reset Value	Description
2	RO	0x0	rx1_valid Status of rx1_valid from PMA
1	RO	0x0	rx2_valid Status of rx2_valid from PMA
0	RO	0x0	rx3_valid Status of rx3_valid from PMA

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CAL_STATUS_5

Address: Operational Base + offset (0x20D6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RO	0x00	rx_eq_dfe_tap2 Status of RX_EQ_DFE_TAP2

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FSM_STRESS_TARGET_CNT

Address: Operational Base + offset (0x20D7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x0ff	stress_target_cnt Stress wait time before BOOTUP

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_STRESS_CNTR_STATUS

Address: Operational Base + offset (0x20D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RO	0x000	stress_cntr Value of stress counter

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LOS_SETTINGS

Address: Operational Base + offset (0x20D9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:3	RW	0x05a	rx_los_timer_thresh1_r Threshold timer to check validity of rx_los signal
2:0	RW	0x3	rx_los_threshold Threshold levels for LOS block

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_LOS_SETTINGS_1

Address: Operational Base + offset (0x20DA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use

Bit	Attr	Reset Value	Description
9:8	RW	0x0	data_to_no_data_sel In FLT bypass, selection to choose exit from data to no data state 2'b00: Only TIMEOUT 2'b01: Only LOS 2'b10: LOS or TIMEOUT 2'b11: LOS and TIMEOUT
7:2	RW	0x10	los_en_wait_cnt Wait count after rx_los_clk_en is high
1	RW	0x0	los_bypass Bypass LOS detection
0	RW	0x0	frl_act_det_sel Select activity detection based on all lanes or one lane. 1'b0: Based on any lane 1'b1: Based on all lanes

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_FRL_FAST_RELOCK

Address: Operational Base + offset (0x20DB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	frl_fast_relock_self_clear_disable Disable self-clearing for frl_fast_relock
0	RW	0x0	frl_fast_relock Fast relock in FRL modes when PHY is in HDMI_PWRDN

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_1

Address: Operational Base + offset (0x20E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:0	RW	0x12c	rate_hdmi14_boundary_1_val HDMI Rate boundary for div_ratio 32. Defined for 8us.

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_2

Address: Operational Base + offset (0x20E1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:0	RW	0x258	rate_hdmi14_boundary_2_val HDMI Rate boundary for div_ratio 16. Defined for 8us.

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_3

Address: Operational Base + offset (0x20E2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:0	RW	0x4b0	rate_hdmi14_boundary_3_val HDMI Rate boundary for div_ratio 8. Defined for 8us.

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_RATE_BOUNDARY_4

Address: Operational Base + offset (0x20E3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x960	rate_hdmi14_boundary_4_val HDMI Rate boundary for div_ratio 4. Defined for 8us.

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_TMDS_VCO_REF_CNT_REG

Address: Operational Base + offset (0x20E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RW	0x0	vco_refclk_select Select reference clock for VCO in TMDS mode. 1'b0: Tmdsclk used as ref 1'b1: Ref_clk used as ref
11:0	RW	0x8c0	tmds_target_vco_cnt Targeted VCO counts in TMDS mode. Max allowed count is 3000.

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_FRL_VCO_CNT_REG

Address: Operational Base + offset (0x20E5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x8c0	frl_target_vco_cnt Targeted VCO counts in FRL mode. Max allowed count is 3000.

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_TMDS_TIMEBASE_LOCK_THRES_REG

Address: Operational Base + offset (0x20E6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	tmds_timebase_mult Choose the timebase window. 2'b00: 8us 2'b01: 16us 2'b10: 32us 2'b11: 64us
13:7	RW	0x03	stbl_thres Threshold window to check TMDS clock is stable or not.
6:0	RW	0x06	lock_thres Threshold window beyond which TMDS clock is considered unstable (after clock stable)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_1_REG

Address: Operational Base + offset (0x20E7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use

Bit	Attr	Reset Value	Description
14:12	RW	0x7	hdmi14_val_cdr_setting_bnd_1 Value of rx_cdr_setting_sel, if hdmi_data_rate_for_cdr is less than cdr_setting_boundary_1
11:0	RW	0x1e6	cdr_setting_boundary_1 Threshold for cdr_setting_sel

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_2_REG

Address: Operational Base + offset (0x20E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x6	hdmi14_val_cdr_setting_bnd_2 Value of rx_cdr_setting_sel, if hdmi_data_rate_for_cdr is less than cdr_setting_boundary_2
11:0	RW	0x248	cdr_setting_boundary_2 Threshold for cdr_setting_sel

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_3_REG

Address: Operational Base + offset (0x20E9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x5	hdmi14_val_cdr_setting_bnd_3 Value of rx_cdr_setting_sel, if hdmi_data_rate_for_cdr is less than cdr_setting_boundary_3
11:0	RW	0x2da	cdr_setting_boundary_3 Threshold for cdr_setting_sel

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_4_REG

Address: Operational Base + offset (0x20EA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x4	hdmi14_val_cdr_setting_bnd_4 Value of rx_cdr_setting_sel, if hdmi_data_rate_for_cdr is less than cdr_setting_boundary_4
11:0	RW	0x3cd	cdr_setting_boundary_4 Threshold for cdr_setting_sel

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_5_REG

Address: Operational Base + offset (0x20EB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use

Bit	Attr	Reset Value	Description
14:12	RW	0x3	hdmi14_val_cdr_setting_bnd_5 Value of rx_cdr_setting_sel, if hdmi_data_rate_for_cdr is less than cdr_setting_boundary_5
11:0	RW	0x5b3	cdr_setting_boundary_5 Threshold for cdr_setting_sel

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_ADAPT_EN_BOUNDARY_REG
Address: Operational Base + offset (0x20EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	hdmi14_165_afe_en Specifiies afe_en below adapt_en_boundary
12	RW	0x0	hdmi14_165_dfe_en Specifiies dfe_en below adapt_en_boundary
11:0	RW	0x672	adapt_en_boundary Specifies below this data rate, afe and dfe not needed

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_EQ_SETTINGS
Address: Operational Base + offset (0x20ED)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x1	hdmi14_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI1.4
13:12	RW	0x3	hdmi14_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI1.4
11:9	RW	0x0	hdmi14_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI1.4
8:4	RW	0x1e	hdmi14_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI1.4
3:0	RW	0xf	hdmi14_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI1.4

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_165_EQ_SETTINGS
Address: Operational Base + offset (0x20EE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x1	hdmi14_165_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI1.4 for 1.65gbps data rate and above
13:12	RW	0x3	hdmi14_165_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI1.4 for 1.65gbps data rate and above
11:9	RW	0x0	hdmi14_165_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI1.4 for 1.65gbps data rate and above
8:4	RW	0x1f	hdmi14_165_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI1.4 for 1.65gbps data rate and above
3:0	RW	0xf	hdmi14_165_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI1.4 for 1.65gbps data rate and above

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI20_EQ_SETTINGS
Address: Operational Base + offset (0x20EF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x2	hdmi20_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI2.0
13:12	RW	0x2	hdmi20_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI2.0
11:9	RW	0x0	hdmi20_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI2.0
8:4	RW	0x1f	hdmi20_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI2.0
3:0	RW	0xf	hdmi20_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI2.0

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_CDR_SETTING_SEL
Address: Operational Base + offset (0x20F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x0	hdmi21_12g_val_cdr_setting_sel Value of rx_cdr_setting_sel in HDMI2.1 (12Gbps in 4 lane mode)
11:9	RW	0x0	hdmi21_10g_val_cdr_setting_sel Value of rx_cdr_setting_sel in HDMI2.1 (10Gbps in 4 lane mode)
8:6	RW	0x0	hdmi21_8g_val_cdr_setting_sel Value of rx_cdr_setting_sel in HDMI2.1 (8Gbps in 4 lane mode)
5:3	RW	0x0	hdmi21_6g_val_cdr_setting_sel Value of rx_cdr_setting_sel in HDMI2.1 (6Gbps in 3/4 lane mode)
2:0	RW	0x0	hdmi21_3g_val_cdr_setting_sel Value of rx_cdr_setting_sel in HDMI2.1 (3Gbps in 3 lane mode)

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_EQ_SETTINGS_TAP
Address: Operational Base + offset (0x20F1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi14_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap1 in HDMI1.4 for less than 1.65gbps
7:0	RW	0x00	hdmi14_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI1.4 for less than 1.65gbps

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI20_CDR_SETTING_SEL
Address: Operational Base + offset (0x20F2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2:0	RW	0x0	hdmi20_val_cdr_setting_sel Value of rx_cdr_setting_sel in HDMI2.0

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI_DATA_RATE
Address: Operational Base + offset (0x20F3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:0	RO	0x0000	hdmi_data_rate Indicates hdmi_data_rate in mbps

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_EQ_SETTINGS_MISC_1
Address: Operational Base + offset (0x20F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	rx_eq_delta_iq_val_1 Value of rx_eq_delta_iq for first boundary
11:8	RW	0x1	rx_eq_delta_iq_val_2 Value of rx_eq_delta_iq for second boundary
7:4	RW	0x2	rx_eq_delta_iq_val_3 Value of rx_eq_delta_iq for third boundary
3:0	RW	0x4	rx_eq_delta_iq_val_4 Value of rx_eq_delta_iq for fourth boundary

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_CDR_HIGHFREQ_THRES
Address: Operational Base + offset (0x20F5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x1388	rx_cdr_vco_highfreq_thres Threshold for rx_cdr_vco_highfreq

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_CDR_LOWFREQ_THRES
Address: Operational Base + offset (0x20F6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0dac	rx_cdr_vco_lowfreq_thres Threshold for rx_cdr_vco_lowfreq

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_1
Address: Operational Base + offset (0x20F7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:7	RW	0x20	ref_range_div_thres_2 Threshold for second ref_range divider
6:0	RW	0x10	ref_range_div_thres_1 Threshold for first ref_range divider

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_3
Address: Operational Base + offset (0x20F8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use

Bit	Attr	Reset Value	Description
13:7	RW	0x40	ref_range_div_thres_4 Threshold for Fourth ref_range divider
6:0	RW	0x30	ref_range_div_thres_3 Threshold for Third ref_range divider

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_5
Address: Operational Base + offset (0x20F9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:7	RW	0x60	ref_range_div_thres_6 Threshold for sixth ref_range divider
6:0	RW	0x50	ref_range_div_thres_5 Threshold for Fifth ref_range divider

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_REF_RANGE_DIV_7
Address: Operational Base + offset (0x20FA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x70	ref_range_div_thres_7 Threshold for seventh ref_range divider

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_6_REG
Address: Operational Base + offset (0x20FB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x2	hdmi14_val_cdr_setting_bnd_6 Value of rx_cdr_setting_sel, if hdmi_data_rate_for_cdr is less than cdr_setting_boundary_6
11:0	RW	0x799	cdr_setting_boundary_6 Threshold for cdr_setting_sel

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_CDR_SETTING_7_REG
Address: Operational Base + offset (0x20FC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x1	hdmi14_val_cdr_setting_bnd_7 Value of rx_cdr_setting_sel, if hdmi_data_rate_for_cdr is less than cdr_setting_boundary_7
11:0	RW	0xb65	cdr_setting_boundary_7 Threshold for cdr_setting_sel

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI14_165_EQ_SETTINGS_TAP
Address: Operational Base + offset (0x20FD)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi14_165_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap1 in HDMI1.4 for more than 1.65gbps
7:0	RW	0x00	hdmi14_165_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI1.4 for more than 1.65gbps

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI20_EQ_SETTINGS_TAP
Address: Operational Base + offset (0x20FE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hdmi20_val_rx_eq_dfe_tap1 Value of rx_eq_dfe_tap0 in HDMI2.0
7:0	RW	0x00	hdmi20_val_rx_eq_dfe_tap2 Value of rx_eq_dfe_tap2 in HDMI2.0

HDMIPCS_DIG_CTRL_PATH_MAIN_FSM_RATE_CALC_HDMI21_3G_EQ_SETTINGS
Address: Operational Base + offset (0x20FF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x1	hdmi21_3g_val_rx_eq_ctle_pole Value of rx_eq_ctle_pole in HDMI2.1 for 3Gbps in 3 lane mode
13:12	RW	0x3	hdmi21_3g_val_rx_eq_afe_rate Value of rx_eq_afe_rate in HDMI2.1 for 3Gbps in 3 lane mode
11:9	RW	0x0	hdmi21_3g_val_rx_eq_att_lvl Value of rx_eq_att_lvl in HDMI2.1 for 3Gbps in 3 lane mode
8:4	RW	0x1f	hdmi21_3g_val_rx_eq_ctle_boost Value of rx_eq_ctle_boost in HDMI2.1 for 3Gbps in 3 lane mode
3:0	RW	0xf	hdmi21_3g_val_rx_eq_afe_gain Value of rx_eq_afe_gain in HDMI2.1 for 3Gbps in 3 lane mode

RAWLANE0_DIG_PCS_XF_RX_OVRD_OUT_2
Address: Operational Base + offset (0x3003)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_valid_ovrd_en Enable override for rx_valid
0	RW	0x0	rx_valid Override value for rx_valid

RAWLANE0_DIG_PCS_XF_RX_PCS_IN_5
Address: Operational Base + offset (0x3004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_valid Value from PCS for rx_valid_i

RAWLANE0_DIG_PCS_XF_RX_OVRD_IN
Address: Operational Base + offset (0x3005)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
10	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
9	RW	0x1	ovrd_en Enable override values for all fields in this register
8	RW	0x0	lpd Override value for rx_lpd
7:6	RW	0x0	pstate Override value for rx_pstate
5:4	RW	0x0	reserved Reserved
3:0	RW	0x0	rate Override value for rx_rate

RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_1
Address: Operational Base + offset (0x3006)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	req_ovrd_en Override enable for rx_req
2	RW	0x1	req_ovrd_val Override value for rx_req
1	RW	0x1	reset_ovrd_en Override enable for rx_reset
0	RW	0x1	reset_ovrd_val Override value for rx_reset

RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_2
Address: Operational Base + offset (0x3007)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	vco_val_ovrd_en Enable override for VCO controls
14	RW	0x0	vco_highfreq_val_ovrd Override value for rx_cdr_vco_highfreq
13	RW	0x0	vco_lowfreq_val_ovrd Override value for rx_cdr_vco_lowfreq
12:0	RW	0x0000	vco_ld_val_ovrd Override value for rx_vco_ld_val

RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_3
Address: Operational Base + offset (0x3008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	cont_ovrd_en Enable override values for rx_adapt_cont and rx_offcan_cont

Bit	Attr	Reset Value	Description
3	RW	0x0	offcan_cont Override value for rx_offcan_cont
2	RW	0x0	adapt_cont Override value for rx_adapt_cont
1	RW	0x0	adapt_req_ovrd_en Enable override values for rx_adapt_req
0	RW	0x0	adapt_req Override value for rx_adapt_req

RAWLANE0_DIG_PCS_XF_RX_PCS_IN
Address: Operational Base + offset (0x3009)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reset Value from PCS for rx_reset
14	RO	0x0	offcan_cont Value from PCS for rx_offcan_cont
13	RO	0x0	adapt_cont Value from PCS for rx_adapt_cont
12	RO	0x0	adapt_req Value from PCS for rx_adapt_req
11	RO	0x0	adapt_dfe_en Value from PCS for rx_adapt_dfe_en
10	RO	0x0	adapt_afe_en Value from PCS for rx_adapt_afe_en
9	RO	0x0	lpd Value from PCS for rx_lpd
8:7	RO	0x0	pstate Value from PCS for rx_pstate
6:5	RO	0x0	reserved_r_1 Reserved
4:1	RO	0x0	rate Value from PCS for rx_rate
0	RO	0x0	req Value from PCS for rx_req

RAWLANE0_DIG_PCS_XF_RX_PCS_IN_1
Address: Operational Base + offset (0x300A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RO	0x00	ref_ld_val Value from PCS for rx_ref_ld_val

RAWLANE0_DIG_PCS_XF_RX_PCS_IN_2
Address: Operational Base + offset (0x300B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_vco_highfreq Value from PCS for rx_cdr_vco_highfreq

Bit	Attr	Reset Value	Description
13	RO	0x0	cdr_vco_lowfreq Value from PCS for rx_cdr_vco_lowfreq
12:0	RO	0x0000	vco_ld_val Value from PCS for rx_vco_ld_val

RAWLANE0_DIG_PCS_XF_RX_PCS_IN_3
Address: Operational Base + offset (0x300C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	eq_afe_rate Value from ASIC for rx_eq_afe_rate
13:12	RO	0x0	eq_ctle_pole Value from ASIC for rx_eq_ctle_pole
11:7	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
6:3	RO	0x0	eq_vga1_gain Value from ASIC for rx_eq_vga1_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

RAWLANE0_DIG_PCS_XF_RX_PCS_IN_4
Address: Operational Base + offset (0x300D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2
7:0	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1

RAWLANE0_DIG_PCS_XF_RX_OVRD_OUT
Address: Operational Base + offset (0x300E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x1	en_ctl Enable override values for all control outputs of this register
0	RW	0x1	ack Override value for rx_ack

RAWLANE0_DIG_PCS_XF_RX_PCS_OUT
Address: Operational Base + offset (0x300F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE0_DIG_PCS_XF_RX_ADAPT_ACK
Address: Operational Base + offset (0x3010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RW	0x0	rx_eq_afe_rate_ovrd_val Override val for rx_eq_afe_rate[1:0]
9:8	RW	0x0	rx_eq_ctle_pole_ovrd_val Override val for rx_eq_ctle_pole[1:0]
7	RW	0x0	rx_eq_att_ovrd_en Individual override enable for ATT
6	RW	0x0	rx_eq_vga1_gain_ovrd_en Individual override enable for gain
5	RW	0x0	rx_eq_ctle_boost_ovrd_en Individual override enable for boost
4	RW	0x0	rx_eq_ctle_pole_ovrd_en Individual override enable for pole
3	RW	0x0	rx_eq_afe_rate_ovrd_en Individual override enable for rate
2	RW	0x0	rx_eq_dfe_t1_ovrd_en Individual override enable for TAP1
1	RW	0x0	rx_eq_dfe_t2_ovrd_en Individual override enable for TAP2
0	RW	0x0	rx_adapt_ack RX adaptation acknowledge

RAWLANE0_DIG_PCS_XF_RX_ADAPT_FOM

Address: Operational Base + offset (0x3011)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom RX adaptation figure of merit

RAWLANE0_DIG_PCS_XF_RX_OVRD_IN_4

Address: Operational Base + offset (0x3012)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	ref_ld_val_ovrd_en Enable override for rx_ref_ld_val
6:0	RW	0x00	ref_ld_val_ovrd Override value for rx_ref_ld_val

RAWLANE0_DIG_PCS_XF_RX_PCS_OUT_2

Address: Operational Base + offset (0x3013)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE0_DIG_PCS_XF_LANE_NUMBER

Address: Operational Base + offset (0x3015)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	lane_number Current lane number

RAWLANE0_DIG_PCS_XF_ATE_OVRD_IN

Address: Operational Base + offset (0x3018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rx_adapt_dfe_en_ovrd_en Enable override value for rx_adapt_dfe_en input
6	RW	0x0	rx_adapt_dfe_en_ovrd_val Override value for rx_adapt_dfe_en input
5	RW	0x0	rx_adapt_afe_en_ovrd_en Enable override value for rx_adapt_afe_en input
4	RW	0x0	rx_adapt_afe_en_ovrd_val Override value for rx_adapt_afe_en input
3	RW	0x0	rx_req_ate_ovrd_en Enable override value for rx_req input
2	RW	0x0	rx_req_ate_ovrd_val Override value for top-level rx_req input
1	RW	0x0	rx_reset_ate_ovrd_en Enable override value for rx_reset input
0	RW	0x0	rx_reset_ate_ovrd_val Override value for top-level rx_reset input

RAWLANE0_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN

Address: Operational Base + offset (0x3019)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	rx_eq_delta_iq_ovrd_en Enable override value for rx_eq_delta_iq
3:0	RW	0x0	rx_eq_delta_iq_ovrd_val Override value for rx_eq_delta_iq

RAWLANE0_DIG_PCS_XF_RX_EQ_OVRD_IN_1

Address: Operational Base + offset (0x301D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:8	RW	0x00	rx_eq_ctle_boost_ovrd_val Override value for rx_eq_ctle_boost[4:0]
7	RW	0x0	rx_eq_ovrd_en Enable override values for all RX EQ settings
6:4	RW	0x0	rx_eq_att_lvl_ovrd_val Override value for rx_eq_att_lvl[2:0]
3:0	RW	0x0	rx_eq_afe_gain_ovrd_val Override value for rx_eq_afe_gain[3:0]

RAWLANE0_DIG_PCS_XF_RX_EQ_OVRD_IN_2
Address: Operational Base + offset (0x301E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	rx_eq_dfe_tap2_ovrd_val Override value for rx_eq_dfe_tap2[7:0]
7:0	RW	0x00	rx_eq_dfe_tap1_ovrd_val Override value for rx_eq_dfe_tap1[7:0]

RAWLANE0_DIG_FSM_FSM_FSM_OVRD_CTL
Address: Operational Base + offset (0x3020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RW	0x0	fsm_ovrd_en Enable overriding the FSM execution of commands must be asserted to use FSM_CMD_START and FSM_JMP_EN features
13	RW	0x0	fsm_cmd_start Start executing the new command this is a self-clearing bit
12	RW	0x0	fsm_jmp_en Force the FSM to jump to FSM_JMP_ADDR in the program memory is applied when FSM_CMD_START is pulsed.
11:0	RW	0x000	fsm_jmp_addr The jump address used when FSM_JUMP_EN=1, the address is encoded as follows: [11:8] mem_lane, [7:5] bank, [4:0] register

RAWLANE0_DIG_FSM_FSM_MEM_ADDR_MON
Address: Operational Base + offset (0x3021)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	mem_addr Current value of memory address used in lane FSM

RAWLANE0_DIG_FSM_FSM_STATUS_MON
Address: Operational Base + offset (0x3022)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	rdmsk_disabled Check, if read mask is currently disabled (i.e. mask is all ones)
9	RO	0x0	wrmsk_disabled Check, if write mask is currently disabled (i.e. mask is all ones)
8	RO	0x0	wait_cnt_eq0 Check, if wait counter currently equals zero
7	RO	0x0	alu_res_eq0 Check, if ALU result register currently equals zero
6	RO	0x0	alu_ovflw Current value of ALU overflow bit
5	RO	0x0	cmd_rdy New command is ready for execution (applicable when FSM_OVRD_EN=1)

Bit	Attr	Reset Value	Description
4:0	RO	0x00	state Current state of lane FSM

RAWLANE0_DIG_FSM_FSM_CR_REG_OP_XTND_EN
Address: Operational Base + offset (0x3023)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	cr_reg_op_xtnd_en CR interface timing extension enable 1'b0: No timing extension 1'b1: Timing extension

RAWLANE0_DIG_FSM_FAST_RX_STARTUP_CAL
Address: Operational Base + offset (0x3024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_startup_cal Status of fast RX start-up calibration

RAWLANE0_DIG_FSM_FAST_RX_ADAPT
Address: Operational Base + offset (0x3025)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_adapt Status of fast RX adaptation

RAWLANE0_DIG_FSM_FAST_RX_AFE_CAL
Address: Operational Base + offset (0x3026)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_cal Status of fast RX AFE DAC start-up calibration

RAWLANE0_DIG_FSM_FAST_RX_DFE_CAL
Address: Operational Base + offset (0x3027)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_cal Status of fast RX DFE slicer start-up calibration

RAWLANE0_DIG_FSM_FAST_RX_BYPASS_CAL
Address: Operational Base + offset (0x3028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_bypass_cal Status of fast RX bypass slicer start-up calibration

RAWLANE0_DIG_FSM_FAST_RX_REFLVL_CAL

Address: Operational Base + offset (0x3029)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_reflvl_cal Status of fast RX reference level (100mv, 125mv, 150mv) start-up calibration

RAWLANE0_DIG_FSM_FAST_RX_IQ_CAL

Address: Operational Base + offset (0x302A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_cal Status of fast RX IQ start-up calibration

RAWLANE0_DIG_FSM_FAST_RX_AFE_ADAPT

Address: Operational Base + offset (0x302B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_adapt Status of fast RX AFE DAC start-up adaptation

RAWLANE0_DIG_FSM_FAST_RX_DFE_ADAPT

Address: Operational Base + offset (0x302C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_adapt Status of fast RX DFE DAC start-up adaptation

RAWLANE0_DIG_FSM_FAST_SUP

Address: Operational Base + offset (0x302D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_sup Status of fast support block (Rtune)

RAWLANE0_DIG_FSM_FAST_RX_IQ_WALK

Address: Operational Base + offset (0x302E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_walk Status of fast RX IQ walk start-up adaptation

RAWLANE0_DIG_FSM_FAST_RX_PWRUP
Address: Operational Base + offset (0x302F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_pwrup Status of fast RX power-up (LOS, VREG/AFE and DCC)

RAWLANE0_DIG_FSM_FAST_RX_VCO_WAIT
Address: Operational Base + offset (0x3030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_wait Status of fast RX VCO wait times

RAWLANE0_DIG_FSM_FAST_RX_VCO_CAL
Address: Operational Base + offset (0x3031)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_cal Status of fast RX VCO calibration

RAWLANE0_DIG_FSM_FAST_RX_CONT_CAL_ADAPT
Address: Operational Base + offset (0x3033)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_cal_adapt Status of fast RX continuous calibration/adaptation

RAWLANE0_DIG_FSM_FAST_RX_CONT_ADAPT
Address: Operational Base + offset (0x3034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_adapt Status of fast RX continuous adaptation

RAWLANE0_DIG_FSM_FAST_RX_CONT_DATA_CAL
Address: Operational Base + offset (0x3035)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_data_cal Status of fast RX continuous data calibration

RAWLANE0_DIG_FSM_FAST_RX_CONT_PHASE_CAL
Address: Operational Base + offset (0x3036)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_phase_cal Status of fast RX continuous phase calibration

RAWLANE0_DIG_FSM_FAST_RX_CONT_AFE_CAL
Address: Operational Base + offset (0x3037)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_afe_cal Status of fast RX continuous AFE calibration

RAWLANE0_DIG_FSM_FAST_RX_ATT_VGA_ADAPT
Address: Operational Base + offset (0x3038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_0 Reserved

RAWLANE0_DIG_FSM_FAST_RX_CTLE_ADAPT
Address: Operational Base + offset (0x3039)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_1 Reserved

RAWLANE0_DIG_FSM_FAST_RX_VGA_ADAPT
Address: Operational Base + offset (0x303A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_2 Reserved

RAWLANE0_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT
Address: Operational Base + offset (0x303B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_3 Reserved

RAWLANE0_DIG_FSM_FAST_RX_IQ_ADAPT
Address: Operational Base + offset (0x303C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_adapt Status of fast RX IQ adapt start-up adaptation

RAWLANE0_DIG_FSM_RX_CTLE_ALGO_EH_SEL
Address: Operational Base + offset (0x303D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_ctle_algo_eh_sel Status of RX CTLE adapt selected algo

RAWLANE0_DIG_FSM_RX_IQ_PHASE_OFFSET
Address: Operational Base + offset (0x303F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	rx_iq_phase_offset Offset value for IQ phase calculation

RAWLANE0_DIG_AON_AFE_ATT_IDAC_OFST
Address: Operational Base + offset (0x3040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_att_idac_ofst Offset value for AFE ATT iDAC

RAWLANE0_DIG_AON_AFE_CTLE_IDAC_OFST
Address: Operational Base + offset (0x3041)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_ctle_idac_ofst Offset value for AFE CTLE iDAC

RAWLANE0_DIG_AON_AFE_VGA1_IDAC_OFST
Address: Operational Base + offset (0x3042)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_vga1_idac_ofst Offset value for AFE VGA1 iDAC

RAWLANE0_DIG_AON_RX_ADAPT_FOM
Address: Operational Base + offset (0x3043)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom Adaptation figure of merit (FOM)

RAWLANE0_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST
Address: Operational Base + offset (0x3044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_summer_odd_idac_ofst Offset value for DFE summer odd iDAC

RAWLANE0_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST
Address: Operational Base + offset (0x3045)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_even_vdac_ofst Offset value for DFE phase even vDAC

RAWLANE0_DIG_AON_DFE_PHASE_ODD_VDAC_OFST
Address: Operational Base + offset (0x3046)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_odd_vdac_ofst Offset value for DFE phase odd vDAC

RAWLANE0_DIG_AON_DFE_EVEN_REF_LVL
Address: Operational Base + offset (0x3047)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_even_ref_lvl DFE even reference level

RAWLANE0_DIG_AON_DFE_ODD_REF_LVL
Address: Operational Base + offset (0x3048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_odd_ref_lvl DFE odd reference level

RAWLANE0_DIG_AON_RX_PHSADJ_LIN
Address: Operational Base + offset (0x3049)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x07	rx_phsadj_lin Linear value for RX phase adjust

RAWLANE0_DIG_AON_RX_PHSADJ_MAP
Address: Operational Base + offset (0x304A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_phsadj_map Mapped value for RX phase adjust

RAWLANE0_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST
Address: Operational Base + offset (0x304B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_high_vdac_ofst Offset value for DFE data even high vDAC

RAWLANE0_DIG_AON_CDR_UNLOCKED_CNT
Address: Operational Base + offset (0x304C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_low_vdac_ofst Offset value for DFE data even low vDAC

RAWLANE0_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST
Address: Operational Base + offset (0x304D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_high_vdac_ofst Offset value for DFE data odd high vDAC

RAWLANE0_DIG_AON_RX_ADAPT_DONE_NEW
Address: Operational Base + offset (0x304E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_low_vdac_ofst Offset value for DFE data odd low vDAC

RAWLANE0_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST
Address: Operational Base + offset (0x304F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_even_vdac_ofst Offset value for DFE bypass even vDAC

RAWLANE0_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST
Address: Operational Base + offset (0x3050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_odd_vdac_ofst Offset value for DFE bypass odd vDAC

RAWLANE0_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST
Address: Operational Base + offset (0x3051)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

RAWLANE0_DIG_AON_DFE_ERROR_ODD_VDAC_OFST
Address: Operational Base + offset (0x3052)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

RAWLANE0_DIG_AON_RX_IQ_PHASE_ADJUST
Address: Operational Base + offset (0x3053)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_iq_phase_adjust Value for RX IQ phase adjust

RAWLANE0_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET
Address: Operational Base + offset (0x3054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_iq_phase_delta_offset Value for RX IQ phase offset + delta value

RAWLANE0_DIG_AON_RX_FW_REVISION_PMA_LABEL
Address: Operational Base + offset (0x3055)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pma_label PMA label

RAWLANE0_DIG_AON_INIT_PWRUP_DONE
Address: Operational Base + offset (0x3056)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	init_pwrup_done Indicates whether initial power-up has completed or not.

RAWLANE0_DIG_AON_RX_ADPT_ATT
Address: Operational Base + offset (0x3057)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	att_adpt_val Stored RX adapted ATT value

RAWLANE0_DIG_AON_RX_ADPT_VGA
Address: Operational Base + offset (0x3058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value

RAWLANE0_DIG_AON_RX_ADPT_CTLE
Address: Operational Base + offset (0x3059)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value

RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP1
Address: Operational Base + offset (0x305A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value

RAWLANE0_DIG_AON_RX_ADAPT_DONE
Address: Operational Base + offset (0x305B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_done Indicates whether RX adaptation has completed or not.

RAWLANE0_DIG_AON_FAST_FLAGS
Address: Operational Base + offset (0x305C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ctle_algo_eh_sel Decides between 1'b1 - "EYE_HEIGHT" or 1'b0 - "MIN_BOT_TOB" algorithms
14	RW	0x0	fast_rx_iq_adapt Enable fast RX IQ adapt
13	RW	0x0	fast_rx_iq_walk Enable fast RX IQ walk
12	RW	0x0	fast_rx_vco_cal Enable fast RX VCO calibration
11	RW	0x0	fast_rx_vco_wait Enable fast RX VCO wait times
10	RW	0x0	fast_rx_pwrup Enable fast RX power-up (LOS, VREG/AFE and DCC)
9	RW	0x0	fast_sup Enable fast support block (rtune)
8	RW	0x0	fast_rx_dfe_adapt Enables fast RX DFE DAC start-up adaptation
7	RW	0x0	fast_rx_afe_adapt Enables fast RX AFE DAC start-up adaptation
6	RW	0x0	fast_rx_iq_cal Enables fast RX IQ start-up calibration
5	RW	0x0	fast_rx_reflvl_cal Enables fast RX reference level (100mv, 125mv, 150mv) start-up calibration
4	RW	0x0	fast_rx_bypass_cal Enables fast RX bypass slicer start-up calibration
3	RW	0x0	fast_rx_dfe_cal Enables fast RX DFE slicer start-up calibration
2	RW	0x0	fast_rx_afe_cal Enables fast RX AFE DAC start-up calibration
1	RW	0x0	fast_rx_adapt Enables fast RX adaptation
0	RW	0x0	fast_rx_startup_cal Enables fast RX start-up calibration

RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP2
Address: Operational Base + offset (0x305D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value

RAWLANE0_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT
Address: Operational Base + offset (0x305E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_lower_limit Stored boost val cost func lower limit

RAWLANE0_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT
Address: Operational Base + offset (0x305F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_upper_limit Stored boost val cost func upper limit

RAWLANE0_DIG_AON_RX_FW_REVISION_RAW_LABEL
Address: Operational Base + offset (0x3060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	raw_label RAW label

RAWLANE0_DIG_AON_RX_SLICER_CTRL_EVEN
Address: Operational Base + offset (0x3061)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

RAWLANE0_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE
Address: Operational Base + offset (0x3062)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

RAWLANE0_DIG_AON_RX_FW_REVISION_PCS_LABEL

Address: Operational Base + offset (0x3063)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pcs_label PCS label

RAWLANE0_DIG_AON_ADPT_CTL_0

Address: Operational Base + offset (0x3064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_ADPT_CTL_1

Address: Operational Base + offset (0x3065)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_ADPT_CTL_2

Address: Operational Base + offset (0x3066)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_ADPT_CTL_3

Address: Operational Base + offset (0x3067)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_ADPT_CTL_4

Address: Operational Base + offset (0x3068)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_ADPT_CTL_5

Address: Operational Base + offset (0x3069)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_ADPT_CTL_6

Address: Operational Base + offset (0x306A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_ADPT_CTL_7
Address: Operational Base + offset (0x306B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE0_DIG_AON_RX_FW_REVISION_FW_LABEL
Address: Operational Base + offset (0x306C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	fw_label FW label

RAWLANE0_DIG_AON_FAST_FLAGS_2
Address: Operational Base + offset (0x306D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11	RW	0x0	ctle_adapt_sts CTLE adaptation status flag
10	RW	0x0	fast_frl_adpt_byp_aft_ltp Enable fast FRL bypass after link training
9	RW	0x0	skip_ctle_bin_srch_abrt Skip CTLE binary search abort
8	RW	0x0	ctle_algo_two_pt_exit CTLE algo two point exit
7	RW	0x0	fast_rx_vga_adapt Enables fast RX VGA adaptation
6	RW	0x0	fast_rx_ctle_adapt Enables fast RX CTLE adaptation
5	RW	0x0	fast_rx_att_vga_adapt Enables fast RX ATT_VGA adaptation
4	RW	0x0	fast_rx_cont_afe_cal Enables fast RX continuous AFE calibration
3	RW	0x0	fast_rx_cont_phase_cal Enables fast RX continuous phase calibration
2	RW	0x0	fast_rx_cont_data_cal Enables fast RX continuous data calibration
1	RW	0x0	fast_rx_cont_adapt Enables fast RX continuous adaptation
0	RW	0x0	fast_rx_cont_cal_adapt Enables fast RX continuous calibration/adaptation

RAWLANE0_DIG_AON_RX_RESERVED_REG_0
Address: Operational Base + offset (0x306E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	reserved_0 Reserved fields

RAWLANE0_DIG_AON_TXRX_OVRD_IN
Address: Operational Base + offset (0x306F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_disable_ovrd_en Override enable for rx_disable
0	RW	0x0	rx_disable_ovrd_val Override value for rx_disable

RAWLANE0_DIG_AON_RX_PHSADJ_LIN_LEFT
Address: Operational Base + offset (0x3070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_left Linear value for RX phase adjust on left

RAWLANE0_DIG_AON_RX_PHSADJ_LIN_RIGHT
Address: Operational Base + offset (0x3071)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_right Linear value for RX phase adjust on right

RAWLANE0_DIG_AON_RX_PHSADJ_LIN_ADAPT
Address: Operational Base + offset (0x3072)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_adapt Linear value for RX phase adjust IQ adapt value

RAWLANE0_DIG_AON_RX_RESERVED_REG_1
Address: Operational Base + offset (0x3073)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_1 Reserved fields

RAWLANE0_DIG_AON_RX_ADPT_VGA_1
Address: Operational Base + offset (0x3078)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use

Bit	Attr	Reset Value	Description
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value 1st iter

RAWLANE0_DIG_AON_RX_ADPT_CTLE_1
Address: Operational Base + offset (0x3079)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value 1st iter

RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP1_1
Address: Operational Base + offset (0x307A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value 1st iter

RAWLANE0_DIG_AON_RX_ADPT_DFE_TAP2_1
Address: Operational Base + offset (0x307D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value 1st iter

RAWLANE0_DIG_IRQ_CTL_RESET_RTN_REQ
Address: Operational Base + offset (0x3080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x1	reset_rtn_req Reset routine request

RAWLANE0_DIG_IRQ_CTL_RX_RESET_IRQ
Address: Operational Base + offset (0x3081)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_reset Rx reset interrupt

RAWLANE0_DIG_IRQ_CTL_RX_REQ_IRQ
Address: Operational Base + offset (0x3082)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_req Rx request interrupt

RAWLANE0_DIG_IRQ_CTL_RX_RATE_IRQ
Address: Operational Base + offset (0x3083)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_rate_irq Rx rate change interrupt request

RAWLANE0_DIG_IRQ_CTL_RX_PSTATE_IRQ
Address: Operational Base + offset (0x3084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_pstate_irq Rx pstate change interrupt request

RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ
Address: Operational Base + offset (0x3085)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_req_irq Rx adaptation request interrupt

RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ
Address: Operational Base + offset (0x3086)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_dis_irq Rx adaptation disable interrupt

RAWLANE0_DIG_IRQ_CTL_RX_RESET_IRQ_CLR
Address: Operational Base + offset (0x3087)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_reset_irq_clr RX reset interrupt clear (self-clearing)

RAWLANE0_DIG_IRQ_CTL_RX_REQ_IRQ_CLR
Address: Operational Base + offset (0x3088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_req_irq_clr RX request interrupt clear (self-clearing)

RAWLANE0_DIG_IRQ_CTL_RX_RATE_IRQ_CLR
Address: Operational Base + offset (0x3089)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_rate_irq_clr RX rate change interrupt clear (self-clearing)

RAWLANE0_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR
Address: Operational Base + offset (0x308A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_pstate_irq_clr RX pstate change interrupt clear (self-clearing)

RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR
Address: Operational Base + offset (0x308B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_req_irq_clr RX adaptation request interrupt clear (self-clearing)

RAWLANE0_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR
Address: Operational Base + offset (0x308C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_dis_irq_clr RX adaptation disable interrupt clear (self-clearing)

RAWLANE0_DIG_IRQ_CTL_IRQ_MASK
Address: Operational Base + offset (0x308D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	rx_initialize_irq_msk Mask for RX initialize interrupt (0 = cannot interrupt)
5	RW	0x0	rx_reset_irq_msk Mask for RX reset interrupt (0 = cannot interrupt)
4	RW	0x0	rx_adapt_dis_irq_msk Mask for RX adaptation disable interrupt (0 = cannot interrupt)
3	RW	0x0	rx_adapt_req_irq_msk Mask for RX adaptation request interrupt (0 = cannot interrupt)

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_pstate_irq_msk Mask for RX pstate change interrupt (0 = cannot interrupt)
1	RW	0x0	rx_rate_irq_msk Mask for RX rate change interrupt (0 = cannot interrupt)
0	RW	0x0	rx_req_irq_msk Mask for RX request interrupt (0 = cannot interrupt)

RAWLANE0_DIG_IRQ_CTL_RX_INITIALIZE_IRQ
Address: Operational Base + offset (0x308E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_initialize_irq Rx initialize interrupt request

RAWLANE0_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR
Address: Operational Base + offset (0x308F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_initialize_irq_clr RX initialize interrupt clear (self-clearing)

RAWLANE0_DIG_PMA_XF_RX_OVRD_OUT
Address: Operational Base + offset (0x30A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	rx_reset_ovrd_en Override enable for rx_reset
2	RW	0x0	rx_reset_ovrd_val Override value for rx_reset
1	RW	0x0	rx_req_ovrd_en Override enable for rx_req
0	RW	0x0	rx_req_ovrd_val Override value for rx_req

RAWLANE0_DIG_PMA_XF_RX_PMA_IN
Address: Operational Base + offset (0x30A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from PMA for rx_ack

RAWLANE0_DIG_RX_CTL_OFFCAN_CONT_STATUS
Address: Operational Base + offset (0x30E3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous offset cancellation

RAWLANE0_DIG_RX_CTL_ADAPT_CONT_STATUS

Address: Operational Base + offset (0x30E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous adaptation

RAWLANE1_DIG_PCS_XF_RX_OVRD_OUT_2

Address: Operational Base + offset (0x3103)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_valid_ovrd_en Enable override for rx_valid
0	RW	0x0	rx_valid Override value for rx_valid

RAWLANE1_DIG_PCS_XF_RX_PCS_IN_5

Address: Operational Base + offset (0x3104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_valid Value from PCS for rx_valid_i

RAWLANE1_DIG_PCS_XF_RX_OVRD_IN

Address: Operational Base + offset (0x3105)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
10	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
9	RW	0x1	ovrd_en Enable override values for all fields in this register
8	RW	0x0	lpd Override value for rx_lpd
7:6	RW	0x0	pstate Override value for rx_pstate
5:4	RW	0x0	reserved Reserved
3:0	RW	0x0	rate Override value for rx_rate

RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_1
Address: Operational Base + offset (0x3106)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	req_ovrd_en Override enable for rx_req
2	RW	0x1	req_ovrd_val Override value for rx_req
1	RW	0x1	reset_ovrd_en Override enable for rx_reset
0	RW	0x1	reset_ovrd_val Override value for rx_reset

RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_2
Address: Operational Base + offset (0x3107)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	vco_val_ovrd_en Enable override for VCO controls
14	RW	0x0	vco_highfreq_val_ovrd Override value for rx_cdr_vco_highfreq
13	RW	0x0	vco_lowfreq_val_ovrd Override value for rx_cdr_vco_lowfreq
12:0	RW	0x0000	vco_ld_val_ovrd Override value for rx_vco_ld_val

RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_3
Address: Operational Base + offset (0x3108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	cont_ovrd_en Enable override values for rx_adapt_cont and rx_offcan_cont
3	RW	0x0	offcan_cont Override value for rx_offcan_cont
2	RW	0x0	adapt_cont Override value for rx_adapt_cont
1	RW	0x0	adapt_req_ovrd_en Enable override values for rx_adapt_req
0	RW	0x0	adapt_req Override value for rx_adapt_req

RAWLANE1_DIG_PCS_XF_RX_PCS_IN
Address: Operational Base + offset (0x3109)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reset Value from PCS for rx_reset
14	RO	0x0	offcan_cont Value from PCS for rx_offcan_cont

Bit	Attr	Reset Value	Description
13	RO	0x0	adapt_cont Value from PCS for rx_adapt_cont
12	RO	0x0	adapt_req Value from PCS for rx_adapt_req
11	RO	0x0	adapt_dfe_en Value from PCS for rx_adapt_dfe_en
10	RO	0x0	adapt_afe_en Value from PCS for rx_adapt_afe_en
9	RO	0x0	lpd Value from PCS for rx_lpd
8:7	RO	0x0	pstate Value from PCS for rx_pstate
6:5	RO	0x0	reserved_r_1 Reserved
4:1	RO	0x0	rate Value from PCS for rx_rate
0	RO	0x0	req Value from PCS for rx_req

RAWLANE1_DIG_PCS_XF_RX_PCS_IN_1
Address: Operational Base + offset (0x310A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RO	0x00	ref_ld_val Value from PCS for rx_ref_ld_val

RAWLANE1_DIG_PCS_XF_RX_PCS_IN_2
Address: Operational Base + offset (0x310B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_vco_highfreq Value from PCS for rx_cdr_vco_highfreq
13	RO	0x0	cdr_vco_lowfreq Value from PCS for rx_cdr_vco_lowfreq
12:0	RO	0x0000	vco_ld_val Value from PCS for rx_vco_ld_val

RAWLANE1_DIG_PCS_XF_RX_PCS_IN_3
Address: Operational Base + offset (0x310C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	eq_afe_rate Value from ASIC for rx_eq_afe_rate
13:12	RO	0x0	eq_ctle_pole Value from ASIC for rx_eq_ctle_pole
11:7	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
6:3	RO	0x0	eq_vga1_gain Value from ASIC for rx_eq_vga1_gain

Bit	Attr	Reset Value	Description
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

RAWLANE1_DIG_PCS_XF_RX_PCS_IN_4
Address: Operational Base + offset (0x310D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2
7:0	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1

RAWLANE1_DIG_PCS_XF_RX_OVRD_OUT
Address: Operational Base + offset (0x310E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x1	en_ctl Enable override values for all control outputs of this register
0	RW	0x1	ack Override value for rx_ack

RAWLANE1_DIG_PCS_XF_RX_PCS_OUT
Address: Operational Base + offset (0x310F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE1_DIG_PCS_XF_RX_ADAPT_ACK
Address: Operational Base + offset (0x3110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RW	0x0	rx_eq_afe_rate_ovrd_val Override val for rx_eq_afe_rate[1:0]
9:8	RW	0x0	rx_eq_ctle_pole_ovrd_val Override val for rx_eq_ctle_pole[1:0]
7	RW	0x0	rx_eq_att_ovrd_en Individual override enable for ATT
6	RW	0x0	rx_eq_vga1_gain_ovrd_en Individual override enable for gain
5	RW	0x0	rx_eq_ctle_boost_ovrd_en Individual override enable for boost
4	RW	0x0	rx_eq_ctle_pole_ovrd_en Individual override enable for pole
3	RW	0x0	rx_eq_afe_rate_ovrd_en Individual override enable for rate
2	RW	0x0	rx_eq_dfe_t1_ovrd_en Individual override enable for TAP1

Bit	Attr	Reset Value	Description
1	RW	0x0	rx_eq_dfe_t2_ovrd_en Individual override enable for TAP2
0	RW	0x0	rx_adapt_ack RX adaptation acknowledge

RAWLANE1_DIG_PCS_XF_RX_ADAPT_FOM
Address: Operational Base + offset (0x3111)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom RX adaptation figure of merit

RAWLANE1_DIG_PCS_XF_RX_OVRD_IN_4
Address: Operational Base + offset (0x3112)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	ref_ld_val_ovrd_en Enable override for rx_ref_ld_val
6:0	RW	0x00	ref_ld_val_ovrd Override value for rx_ref_ld_val

RAWLANE1_DIG_PCS_XF_RX_PCS_OUT_2
Address: Operational Base + offset (0x3113)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE1_DIG_PCS_XF_LANE_NUMBER
Address: Operational Base + offset (0x3115)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	lane_number Current lane number

RAWLANE1_DIG_PCS_XF_ATE_OVRD_IN
Address: Operational Base + offset (0x3118)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rx_adapt_dfe_en_ovrd_en Enable override value for rx_adapt_dfe_en input
6	RW	0x0	rx_adapt_dfe_en_ovrd_val Override value for rx_adapt_dfe_en input

Bit	Attr	Reset Value	Description
5	RW	0x0	rx_adapt_afe_en_ovrd_en Enable override value for rx_adapt_afe_en input
4	RW	0x0	rx_adapt_afe_en_ovrd_val Override value for rx_adapt_afe_en input
3	RW	0x0	rx_req_ate_ovrd_en Enable override value for rx_req input
2	RW	0x0	rx_req_ate_ovrd_val Override value for top-level rx_req input
1	RW	0x0	rx_reset_ate_ovrd_en Enable override value for rx_reset input
0	RW	0x0	rx_reset_ate_ovrd_val Override value for top-level rx_reset input

RAWLANE1_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN
Address: Operational Base + offset (0x3119)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	rx_eq_delta_iq_ovrd_en Enable override value for rx_eq_delta_iq
3:0	RW	0x0	rx_eq_delta_iq_ovrd_val Override value for rx_eq_delta_iq

RAWLANE1_DIG_PCS_XF_RX_EQ_OVRD_IN_1
Address: Operational Base + offset (0x311D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:8	RW	0x00	rx_eq_ctle_boost_ovrd_val Override value for rx_eq_ctle_boost[4:0]
7	RW	0x0	rx_eq_ovrd_en Enable override values for all RX EQ settings
6:4	RW	0x0	rx_eq_att_lvl_ovrd_val Override value for rx_eq_att_lvl[2:0]
3:0	RW	0x0	rx_eq_afe_gain_ovrd_val Override value for rx_eq_afe_gain[3:0]

RAWLANE1_DIG_PCS_XF_RX_EQ_OVRD_IN_2
Address: Operational Base + offset (0x311E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	rx_eq_dfe_tap2_ovrd_val Override value for rx_eq_dfe_tap2[7:0]
7:0	RW	0x00	rx_eq_dfe_tap1_ovrd_val Override value for rx_eq_dfe_tap1[7:0]

RAWLANE1_DIG_FSM_FSM_FSM_OVRD_CTL
Address: Operational Base + offset (0x3120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use

Bit	Attr	Reset Value	Description
14	RW	0x0	fsm_ovrd_en Enable overriding the FSM execution of commands must be asserted to use FSM_CMD_START and FSM_JMP_EN features
13	RW	0x0	fsm_cmd_start Start executing the new command this is a self-clearing bit
12	RW	0x0	fsm_jmp_en Force the FSM to jump to FSM_JMP_ADDR in the program memory is applied when FSM_CMD_START is pulsed.
11:0	RW	0x000	fsm_jmp_addr The jump address used when FSM_JUMP_EN=1, the address is encoded as follows: [11:8] mem_lane, [7:5] bank, [4:0] register

RAWLANE1_DIG_FSM_FSM_MEM_ADDR_MON

Address: Operational Base + offset (0x3121)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	mem_addr Current value of memory address used in lane FSM

RAWLANE1_DIG_FSM_FSM_STATUS_MON

Address: Operational Base + offset (0x3122)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	rdmsk_disabled Check, if read mask is currently disabled (i.e. mask is all ones)
9	RO	0x0	wrmsk_disabled Check, if write mask is currently disabled (i.e. mask is all ones)
8	RO	0x0	wait_cnt_eq0 Check, if wait counter currently equals zero
7	RO	0x0	alu_res_eq0 Check, if ALU result register currently equals zero
6	RO	0x0	alu_ovflw Current value of ALU overflow bit
5	RO	0x0	cmd_rdy New command is ready for execution (applicable when FSM_OVRD_EN=1)
4:0	RO	0x00	state Current state of lane FSM

RAWLANE1_DIG_FSM_FSM_CR_REG_OP_XTND_EN

Address: Operational Base + offset (0x3123)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	cr_reg_op_xtnd_en CR interface timing extension enable 1'b0: No timing extension 1'b1: Timing extension

RAWLANE1_DIG_FSM_FAST_RX_STARTUP_CAL

Address: Operational Base + offset (0x3124)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_startup_cal Status of fast RX start-up calibration

RAWLANE1_DIG_FSM_FAST_RX_ADAPT
Address: Operational Base + offset (0x3125)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_adapt Status of fast RX adaptation

RAWLANE1_DIG_FSM_FAST_RX_AFE_CAL
Address: Operational Base + offset (0x3126)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_cal Status of fast RX AFE DAC start-up calibration

RAWLANE1_DIG_FSM_FAST_RX_DFE_CAL
Address: Operational Base + offset (0x3127)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_cal Status of fast RX DFE slicer start-up calibration

RAWLANE1_DIG_FSM_FAST_RX_BYPASS_CAL
Address: Operational Base + offset (0x3128)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_bypass_cal Status of fast RX bypass slicer start-up calibration

RAWLANE1_DIG_FSM_FAST_RX_REFLVL_CAL
Address: Operational Base + offset (0x3129)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_reflvl_cal Status of fast RX reference level (100mv, 125mv, 150mv) start-up calibration

RAWLANE1_DIG_FSM_FAST_RX_IQ_CAL
Address: Operational Base + offset (0x312A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_cal Status of fast RX IQ start-up calibration

RAWLANE1_DIG_FSM_FAST_RX_AFE_ADAPT
Address: Operational Base + offset (0x312B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_adapt Status of fast RX AFE DAC start-up adaptation

RAWLANE1_DIG_FSM_FAST_RX_DFE_ADAPT
Address: Operational Base + offset (0x312C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_adapt Status of fast RX DFE DAC start-up adaptation

RAWLANE1_DIG_FSM_FAST_SUP
Address: Operational Base + offset (0x312D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_sup Status of fast support block (Rtune)

RAWLANE1_DIG_FSM_FAST_RX_IQ_WALK
Address: Operational Base + offset (0x312E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_walk Status of fast RX IQ walk start-up adaptation

RAWLANE1_DIG_FSM_FAST_RX_PWRUP
Address: Operational Base + offset (0x312F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_pwrup Status of fast RX power-up (LOS, VREG/AFE and DCC)

RAWLANE1_DIG_FSM_FAST_RX_VCO_WAIT
Address: Operational Base + offset (0x3130)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_wait Status of fast RX VCO wait times

RAWLANE1_DIG_FSM_FAST_RX_VCO_CAL

Address: Operational Base + offset (0x3131)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_cal Status of fast RX VCO calibration

RAWLANE1_DIG_FSM_FAST_RX_CONT_CAL_ADAPT

Address: Operational Base + offset (0x3133)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_cal_adapt Status of fast RX continuous calibration/adaptation

RAWLANE1_DIG_FSM_FAST_RX_CONT_ADAPT

Address: Operational Base + offset (0x3134)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_adapt Status of fast RX continuous adaptation

RAWLANE1_DIG_FSM_FAST_RX_CONT_DATA_CAL

Address: Operational Base + offset (0x3135)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_data_cal Status of fast RX continuous data calibration

RAWLANE1_DIG_FSM_FAST_RX_CONT_PHASE_CAL

Address: Operational Base + offset (0x3136)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_phase_cal Status of fast RX continuous phase calibration

RAWLANE1_DIG_FSM_FAST_RX_CONT_AFE_CAL

Address: Operational Base + offset (0x3137)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_afe_cal Status of fast RX continuous AFE calibration

RAWLANE1_DIG_FSM_FAST_RX_ATT_VGA_ADAPT

Address: Operational Base + offset (0x3138)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_0 Reserved

RAWLANE1_DIG_FSM_FAST_RX_CTLE_ADAPT

Address: Operational Base + offset (0x3139)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_1 Reserved

RAWLANE1_DIG_FSM_FAST_RX_VGA_ADAPT

Address: Operational Base + offset (0x313A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_2 Reserved

RAWLANE1_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT

Address: Operational Base + offset (0x313B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_3 Reserved

RAWLANE1_DIG_FSM_FAST_RX_IQ_ADAPT

Address: Operational Base + offset (0x313C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_adapt Status of fast RX IQ adapt start-up adaptation

RAWLANE1_DIG_FSM_RX_CTLE_ALGO_EH_SEL

Address: Operational Base + offset (0x313D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_ctle_algo_eh_sel Status of RX CTLE adapt selected algo

RAWLANE1_DIG_FSM_RX_IQ_PHASE_OFFSET
Address: Operational Base + offset (0x313F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	rx_iq_phase_offset Offset value for IQ phase calculation

RAWLANE1_DIG_AON_AFE_ATT_IDAC_OFST
Address: Operational Base + offset (0x3140)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_att_idac_ofst Offset value for AFE ATT iDAC

RAWLANE1_DIG_AON_AFE_CTLE_IDAC_OFST
Address: Operational Base + offset (0x3141)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_ctle_idac_ofst Offset value for AFE CTLE iDAC

RAWLANE1_DIG_AON_AFE_VGA1_IDAC_OFST
Address: Operational Base + offset (0x3142)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_vga1_idac_ofst Offset value for AFE VGA1 iDAC

RAWLANE1_DIG_AON_RX_ADAPT_FOM
Address: Operational Base + offset (0x3143)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom Adaptation figure of merit (FOM)

RAWLANE1_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST
Address: Operational Base + offset (0x3144)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_summer_odd_idac_ofst Offset value for DFE summer odd iDAC

RAWLANE1_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST

Address: Operational Base + offset (0x3145)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_even_vdac_ofst Offset value for DFE phase even vDAC

RAWLANE1_DIG_AON_DFE_PHASE_ODD_VDAC_OFST

Address: Operational Base + offset (0x3146)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_odd_vdac_ofst Offset value for DFE phase odd vDAC

RAWLANE1_DIG_AON_DFE_EVEN_REF_LVL

Address: Operational Base + offset (0x3147)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_even_ref_lvl DFE even reference level

RAWLANE1_DIG_AON_DFE_ODD_REF_LVL

Address: Operational Base + offset (0x3148)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_odd_ref_lvl DFE odd reference level

RAWLANE1_DIG_AON_RX_PHSADJ_LIN

Address: Operational Base + offset (0x3149)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x07	rx_phsadj_lin Linear value for RX phase adjust

RAWLANE1_DIG_AON_RX_PHSADJ_MAP

Address: Operational Base + offset (0x314A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_phsadj_map Mapped value for RX phase adjust

RAWLANE1_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST
Address: Operational Base + offset (0x314B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_high_vdac_ofst Offset value for DFE data even high vDAC

RAWLANE1_DIG_AON_CDR_UNLOCKED_CNT
Address: Operational Base + offset (0x314C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_low_vdac_ofst Offset value for DFE data even low vDAC

RAWLANE1_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST
Address: Operational Base + offset (0x314D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_high_vdac_ofst Offset value for DFE data odd high vDAC

RAWLANE1_DIG_AON_RX_ADAPT_DONE_NEW
Address: Operational Base + offset (0x314E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_low_vdac_ofst Offset value for DFE data odd low vDAC

RAWLANE1_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST
Address: Operational Base + offset (0x314F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_even_vdac_ofst Offset value for DFE bypass even vDAC

RAWLANE1_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST
Address: Operational Base + offset (0x3150)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_odd_vdac_ofst Offset value for DFE bypass odd vDAC

RAWLANE1_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST

Address: Operational Base + offset (0x3151)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

RAWLANE1_DIG_AON_DFE_ERROR_ODD_VDAC_OFST

Address: Operational Base + offset (0x3152)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

RAWLANE1_DIG_AON_RX_IQ_PHASE_ADJUST

Address: Operational Base + offset (0x3153)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_iq_phase_adjust Value for RX IQ phase adjust

RAWLANE1_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET

Address: Operational Base + offset (0x3154)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_iq_phase_delta_offset Value for RX IQ phase offset + delta value

RAWLANE1_DIG_AON_RX_FW_REVISION_PMA_LABEL

Address: Operational Base + offset (0x3155)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pma_label PMA label

RAWLANE1_DIG_AON_INIT_PWRUP_DONE

Address: Operational Base + offset (0x3156)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	init_pwrup_done Indicates whether initial power-up has completed or not.

RAWLANE1_DIG_AON_RX_ADPT_ATT
Address: Operational Base + offset (0x3157)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	att_adpt_val Stored RX adapted ATT value

RAWLANE1_DIG_AON_RX_ADPT_VGA
Address: Operational Base + offset (0x3158)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value

RAWLANE1_DIG_AON_RX_ADPT_CTLE
Address: Operational Base + offset (0x3159)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value

RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP1
Address: Operational Base + offset (0x315A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value

RAWLANE1_DIG_AON_RX_ADAPT_DONE
Address: Operational Base + offset (0x315B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_done Indicates whether RX adaptation has completed or not.

RAWLANE1_DIG_AON_FAST_FLAGS
Address: Operational Base + offset (0x315C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ctle_algo_eh_sel Decides between 1'b1 - "EYE_HEIGHT" or 1'b0 - "MIN_BOT_TOB" algorithms
14	RW	0x0	fast_rx_iq_adapt Enable fast RX IQ adapt
13	RW	0x0	fast_rx_iq_walk Enable fast RX IQ walk
12	RW	0x0	fast_rx_vco_cal Enable fast RX VCO calibration
11	RW	0x0	fast_rx_vco_wait Enable fast RX VCO wait times
10	RW	0x0	fast_rx_pwrup Enable fast RX power-up (LOS, VREG/AFE and DCC)
9	RW	0x0	fast_sup Enable fast support block (rtune)
8	RW	0x0	fast_rx_dfe_adapt Enables fast RX DFE DAC start-up adaptation
7	RW	0x0	fast_rx_afe_adapt Enables fast RX AFE DAC start-up adaptation
6	RW	0x0	fast_rx_iq_cal Enables fast RX IQ start-up calibration
5	RW	0x0	fast_rx_reflvl_cal Enables fast RX reference level (100mv, 125mv, 150mv) start-up calibration
4	RW	0x0	fast_rx_bypass_cal Enables fast RX bypass slicer start-up calibration
3	RW	0x0	fast_rx_dfe_cal Enables fast RX DFE slicer start-up calibration
2	RW	0x0	fast_rx_afe_cal Enables fast RX AFE DAC start-up calibration
1	RW	0x0	fast_rx_adapt Enables fast RX adaptation
0	RW	0x0	fast_rx_startup_cal Enables fast RX start-up calibration

RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP2
Address: Operational Base + offset (0x315D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value

RAWLANE1_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT
Address: Operational Base + offset (0x315E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_lower_limit Stored boost val cost func lower limit

RAWLANE1_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT
Address: Operational Base + offset (0x315F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_upper_limit Stored boost val cost func upper limit

RAWLANE1_DIG_AON_RX_FW_REVISION_RAW_LABEL
Address: Operational Base + offset (0x3160)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	raw_label RAW label

RAWLANE1_DIG_AON_RX_SLICER_CTRL_EVEN
Address: Operational Base + offset (0x3161)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

RAWLANE1_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE
Address: Operational Base + offset (0x3162)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

RAWLANE1_DIG_AON_RX_FW_REVISION_PCS_LABEL
Address: Operational Base + offset (0x3163)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pcs_label PCS label

RAWLANE1_DIG_AON_ADPT_CTL_0
Address: Operational Base + offset (0x3164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_ADPT_CTL_1
Address: Operational Base + offset (0x3165)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_ADPT_CTL_2
Address: Operational Base + offset (0x3166)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_ADPT_CTL_3
Address: Operational Base + offset (0x3167)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_ADPT_CTL_4
Address: Operational Base + offset (0x3168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_ADPT_CTL_5
Address: Operational Base + offset (0x3169)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_ADPT_CTL_6
Address: Operational Base + offset (0x316A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_ADPT_CTL_7
Address: Operational Base + offset (0x316B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE1_DIG_AON_RX_FW_REVISION_FW_LABEL
Address: Operational Base + offset (0x316C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	fw_label FW label

RAWLANE1_DIG_AON_FAST_FLAGS_2

Address: Operational Base + offset (0x316D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11	RW	0x0	ctle_adapt_sts CTLE adaptation status flag
10	RW	0x0	fast_frl_adpt_byp_aft_ltp Enable fast FRL bypass after link training
9	RW	0x0	skip_ctle_bin_srch_abrt Skip CTLE binary search abort
8	RW	0x0	ctle_algo_two_pt_exit CTLE algo two point exit
7	RW	0x0	fast_rx_vga_adapt Enables fast RX VGA adaptation
6	RW	0x0	fast_rx_ctle_adapt Enables fast RX CTLE adaptation
5	RW	0x0	fast_rx_att_vga_adapt Enables fast RX ATT_VGA adaptation
4	RW	0x0	fast_rx_cont_afe_cal Enables fast RX continuous AFE calibration
3	RW	0x0	fast_rx_cont_phase_cal Enables fast RX continuous phase calibration
2	RW	0x0	fast_rx_cont_data_cal Enables fast RX continuous data calibration
1	RW	0x0	fast_rx_cont_adapt Enables fast RX continuous adaptation
0	RW	0x0	fast_rx_cont_cal_adapt Enables fast RX continuous calibration/adaptation

RAWLANE1_DIG_AON_RX_RESERVED_REG_0

Address: Operational Base + offset (0x316E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_0 Reserved fields

RAWLANE1_DIG_AON_TXRX_OVRD_IN

Address: Operational Base + offset (0x316F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_disable_ovrd_en Override enable for rx_disable
0	RW	0x0	rx_disable_ovrd_val Override value for rx_disable

RAWLANE1_DIG_AON_RX_PHSADJ_LIN_LEFT

Address: Operational Base + offset (0x3170)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_left Linear value for RX phase adjust on left

RAWLANE1_DIG_AON_RX_PHSADJ_LIN_RIGHT
Address: Operational Base + offset (0x3171)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_right Linear value for RX phase adjust on right

RAWLANE1_DIG_AON_RX_PHSADJ_LIN_ADAPT
Address: Operational Base + offset (0x3172)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_adapt Linear value for RX phase adjust IQ adapt value

RAWLANE1_DIG_AON_RX_RESERVED_REG_1
Address: Operational Base + offset (0x3173)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_1 Reserved fields

RAWLANE1_DIG_AON_RX_ADPT_VGA_1
Address: Operational Base + offset (0x3178)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value 1st iter

RAWLANE1_DIG_AON_RX_ADPT_CTLE_1
Address: Operational Base + offset (0x3179)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value 1st iter

RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP1_1
Address: Operational Base + offset (0x317A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value 1st iter

RAWLANE1_DIG_AON_RX_ADPT_DFE_TAP2_1
Address: Operational Base + offset (0x317D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value 1st iter

RAWLANE1_DIG_IRQ_CTL_RESET_RTN_REQ
Address: Operational Base + offset (0x3180)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x1	reset_rtn_req Reset routine request

RAWLANE1_DIG_IRQ_CTL_RX_RESET_IRQ
Address: Operational Base + offset (0x3181)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_reset Rx reset interrupt

RAWLANE1_DIG_IRQ_CTL_RX_REQ_IRQ
Address: Operational Base + offset (0x3182)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_req Rx request interrupt

RAWLANE1_DIG_IRQ_CTL_RX_RATE_IRQ
Address: Operational Base + offset (0x3183)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_rate_irq Rx rate change interrupt request

RAWLANE1_DIG_IRQ_CTL_RX_PSTATE_IRQ
Address: Operational Base + offset (0x3184)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_pstate_irq Rx pstate change interrupt request

RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ
Address: Operational Base + offset (0x3185)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_req_irq Rx adaptation request interrupt

RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ
Address: Operational Base + offset (0x3186)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_dis_irq Rx adaptation disable interrupt

RAWLANE1_DIG_IRQ_CTL_RX_RESET_IRQ_CLR
Address: Operational Base + offset (0x3187)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_reset_irq_clr RX reset interrupt clear (self-clearing)

RAWLANE1_DIG_IRQ_CTL_RX_REQ_IRQ_CLR
Address: Operational Base + offset (0x3188)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_req_irq_clr RX request interrupt clear (self-clearing)

RAWLANE1_DIG_IRQ_CTL_RX_RATE_IRQ_CLR
Address: Operational Base + offset (0x3189)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_rate_irq_clr RX rate change interrupt clear (self-clearing)

RAWLANE1_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR
Address: Operational Base + offset (0x318A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_pstate_irq_clr RX pstate change interrupt clear (self-clearing)

RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR
Address: Operational Base + offset (0x318B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_req_irq_clr RX adaptation request interrupt clear (self-clearing)

RAWLANE1_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR
Address: Operational Base + offset (0x318C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_dis_irq_clr RX adaptation disable interrupt clear (self-clearing)

RAWLANE1_DIG_IRQ_CTL_IRQ_MASK
Address: Operational Base + offset (0x318D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	rx_initialize_irq_msk Mask for RX initialize interrupt (0 = cannot interrupt)
5	RW	0x0	rx_reset_irq_msk Mask for RX reset interrupt (0 = cannot interrupt)
4	RW	0x0	rx_adapt_dis_irq_msk Mask for RX adaptation disable interrupt (0 = cannot interrupt)
3	RW	0x0	rx_adapt_req_irq_msk Mask for RX adaptation request interrupt (0 = cannot interrupt)
2	RW	0x0	rx_pstate_irq_msk Mask for RX pstate change interrupt (0 = cannot interrupt)
1	RW	0x0	rx_rate_irq_msk Mask for RX rate change interrupt (0 = cannot interrupt)
0	RW	0x0	rx_req_irq_msk Mask for RX request interrupt (0 = cannot interrupt)

RAWLANE1_DIG_IRQ_CTL_RX_INITIALIZE_IRQ
Address: Operational Base + offset (0x318E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_initialize_irq Rx initialize interrupt request

RAWLANE1_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR
Address: Operational Base + offset (0x318F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_initialize_irq_clr RX initialize interrupt clear (self-clearing)

RAWLANE1_DIG_PMA_XF_RX_OVRD_OUT
Address: Operational Base + offset (0x31A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	rx_reset_ovrd_en Override enable for rx_reset
2	RW	0x0	rx_reset_ovrd_val Override value for rx_reset
1	RW	0x0	rx_req_ovrd_en Override enable for rx_req
0	RW	0x0	rx_req_ovrd_val Override value for rx_req

RAWLANE1_DIG_PMA_XF_RX_PMA_IN
Address: Operational Base + offset (0x31A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from PMA for rx_ack

RAWLANE1_DIG_RX_CTL_OFFCAN_CONT_STATUS
Address: Operational Base + offset (0x31E3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous offset cancellation

RAWLANE1_DIG_RX_CTL_ADAPT_CONT_STATUS
Address: Operational Base + offset (0x31E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous adaptation

RAWLANE2_DIG_PCS_XF_RX_OVRD_OUT_2
Address: Operational Base + offset (0x3203)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use

Bit	Attr	Reset Value	Description
1	RW	0x0	rx_valid_ovrd_en Enable override for rx_valid
0	RW	0x0	rx_valid Override value for rx_valid

RAWLANE2_DIG_PCS_XF_RX_PCS_IN_5

Address: Operational Base + offset (0x3204)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_valid Value from PCS for rx_valid_i

RAWLANE2_DIG_PCS_XF_RX_OVRD_IN

Address: Operational Base + offset (0x3205)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
10	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
9	RW	0x1	ovrd_en Enable override values for all fields in this register
8	RW	0x0	lpd Override value for rx_lpd
7:6	RW	0x0	pstate Override value for rx_pstate
5:4	RW	0x0	reserved Reserved
3:0	RW	0x0	rate Override value for rx_rate

RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_1

Address: Operational Base + offset (0x3206)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	req_ovrd_en Override enable for rx_req
2	RW	0x1	req_ovrd_val Override value for rx_req
1	RW	0x1	reset_ovrd_en Override enable for rx_reset
0	RW	0x1	reset_ovrd_val Override value for rx_reset

RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_2

Address: Operational Base + offset (0x3207)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	vco_val_ovrd_en Enable override for VCO controls
14	RW	0x0	vco_highfreq_val_ovrd Override value for rx_cdr_vco_highfreq
13	RW	0x0	vco_lowfreq_val_ovrd Override value for rx_cdr_vco_lowfreq
12:0	RW	0x0000	vco_ld_val_ovrd Override value for rx_vco_ld_val

RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_3
Address: Operational Base + offset (0x3208)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	cont_ovrd_en Enable override values for rx_adapt_cont and rx_offcan_cont
3	RW	0x0	offcan_cont Override value for rx_offcan_cont
2	RW	0x0	adapt_cont Override value for rx_adapt_cont
1	RW	0x0	adapt_req_ovrd_en Enable override values for rx_adapt_req
0	RW	0x0	adapt_req Override value for rx_adapt_req

RAWLANE2_DIG_PCS_XF_RX_PCS_IN
Address: Operational Base + offset (0x3209)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reset Value from PCS for rx_reset
14	RO	0x0	offcan_cont Value from PCS for rx_offcan_cont
13	RO	0x0	adapt_cont Value from PCS for rx_adapt_cont
12	RO	0x0	adapt_req Value from PCS for rx_adapt_req
11	RO	0x0	adapt_dfe_en Value from PCS for rx_adapt_dfe_en
10	RO	0x0	adapt_afe_en Value from PCS for rx_adapt_afe_en
9	RO	0x0	lpd Value from PCS for rx_lpd
8:7	RO	0x0	pstate Value from PCS for rx_pstate
6:5	RO	0x0	reserved_r_1 Reserved
4:1	RO	0x0	rate Value from PCS for rx_rate
0	RO	0x0	req Value from PCS for rx_req

RAWLANE2_DIG_PCS_XF_RX_PCS_IN_1

Address: Operational Base + offset (0x320A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RO	0x00	ref_ld_val Value from PCS for rx_ref_ld_val

RAWLANE2_DIG_PCS_XF_RX_PCS_IN_2

Address: Operational Base + offset (0x320B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_vco_highfreq Value from PCS for rx_cdr_vco_highfreq
13	RO	0x0	cdr_vco_lowfreq Value from PCS for rx_cdr_vco_lowfreq
12:0	RO	0x0000	vco_ld_val Value from PCS for rx_vco_ld_val

RAWLANE2_DIG_PCS_XF_RX_PCS_IN_3

Address: Operational Base + offset (0x320C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	eq_afe_rate Value from ASIC for rx_eq_afe_rate
13:12	RO	0x0	eq_ctle_pole Value from ASIC for rx_eq_ctle_pole
11:7	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
6:3	RO	0x0	eq_vga1_gain Value from ASIC for rx_eq_vga1_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

RAWLANE2_DIG_PCS_XF_RX_PCS_IN_4

Address: Operational Base + offset (0x320D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2
7:0	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1

RAWLANE2_DIG_PCS_XF_RX_OVRD_OUT

Address: Operational Base + offset (0x320E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x1	en_ctl Enable override values for all control outputs of this register
0	RW	0x1	ack Override value for rx_ack

RAWLANE2_DIG_PCS_XF_RX_PCS_OUT
Address: Operational Base + offset (0x320F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE2_DIG_PCS_XF_RX_ADAPT_ACK
Address: Operational Base + offset (0x3210)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RW	0x0	rx_eq_afe_rate_ovrd_val Override val for rx_eq_afe_rate[1:0]
9:8	RW	0x0	rx_eq_ctle_pole_ovrd_val Override val for rx_eq_ctle_pole[1:0]
7	RW	0x0	rx_eq_att_ovrd_en Individual override enable for ATT
6	RW	0x0	rx_eq_vga1_gain_ovrd_en Individual override enable for gain
5	RW	0x0	rx_eq_ctle_boost_ovrd_en Individual override enable for boost
4	RW	0x0	rx_eq_ctle_pole_ovrd_en Individual override enable for pole
3	RW	0x0	rx_eq_afe_rate_ovrd_en Individual override enable for rate
2	RW	0x0	rx_eq_dfe_t1_ovrd_en Individual override enable for TAP1
1	RW	0x0	rx_eq_dfe_t2_ovrd_en Individual override enable for TAP2
0	RW	0x0	rx_adapt_ack RX adaptation Acknowledge

RAWLANE2_DIG_PCS_XF_RX_ADAPT_FOM
Address: Operational Base + offset (0x3211)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom RX adaptation figure of merit

RAWLANE2_DIG_PCS_XF_RX_OVRD_IN_4
Address: Operational Base + offset (0x3212)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	ref_ld_val_ovrd_en Enable override for rx_ref_ld_val

Bit	Attr	Reset Value	Description
6:0	RW	0x00	ref_ld_val_ovrd Override value for rx_ref_ld_val

RAWLANE2_DIG_PCS_XF_RX_PCS_OUT_2
Address: Operational Base + offset (0x3213)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE2_DIG_PCS_XF_LANE_NUMBER
Address: Operational Base + offset (0x3215)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	lane_number Current lane number

RAWLANE2_DIG_PCS_XF_ATE_OVRD_IN
Address: Operational Base + offset (0x3218)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rx_adapt_dfe_en_ovrd_en Enable override value for rx_adapt_dfe_en input
6	RW	0x0	rx_adapt_dfe_en_ovrd_val Override value for rx_adapt_dfe_en input
5	RW	0x0	rx_adapt_afe_en_ovrd_en Enable override value for rx_adapt_afe_en input
4	RW	0x0	rx_adapt_afe_en_ovrd_val Override value for rx_adapt_afe_en input
3	RW	0x0	rx_req_ate_ovrd_en Enable override value for rx_req input
2	RW	0x0	rx_req_ate_ovrd_val Override value for top-level rx_req input
1	RW	0x0	rx_reset_ate_ovrd_en Enable override value for rx_reset input
0	RW	0x0	rx_reset_ate_ovrd_val Override value for top-level rx_reset input

RAWLANE2_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN
Address: Operational Base + offset (0x3219)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	rx_eq_delta_iq_ovrd_en Enable override value for rx_eq_delta_iq
3:0	RW	0x0	rx_eq_delta_iq_ovrd_val Override value for rx_eq_delta_iq

RAWLANE2_DIG_PCS_XF_RX_EQ_OVRD_IN_1
Address: Operational Base + offset (0x321D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:8	RW	0x00	rx_eq_ctle_boost_ovrd_val Override value for rx_eq_ctle_boost[4:0]
7	RW	0x0	rx_eq_ovrd_en Enable override values for all RX EQ settings
6:4	RW	0x0	rx_eq_att_lvl_ovrd_val Override value for rx_eq_att_lvl[2:0]
3:0	RW	0x0	rx_eq_afe_gain_ovrd_val Override value for rx_eq_afe_gain[3:0]

RAWLANE2_DIG_PCS_XF_RX_EQ_OVRD_IN_2
Address: Operational Base + offset (0x321E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	rx_eq_dfe_tap2_ovrd_val Override value for rx_eq_dfe_tap2[7:0]
7:0	RW	0x00	rx_eq_dfe_tap1_ovrd_val Override value for rx_eq_dfe_tap1[7:0]

RAWLANE2_DIG_FSM_FSM_FSM_OVRD_CTL
Address: Operational Base + offset (0x3220)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RW	0x0	fsm_ovrd_en Enable overriding the FSM execution of commands must be asserted to use FSM_CMD_START and FSM_JMP_EN features
13	RW	0x0	fsm_cmd_start Start executing the new command, this is a self-clearing bit
12	RW	0x0	fsm_jmp_en Force the FSM to jump to FSM_JMP_ADDR in the program memory is applied when FSM_CMD_START is pulsed.
11:0	RW	0x000	fsm_jmp_addr The jump address used when FSM_JUMP_EN=1, the address is encoded as follows: [11:8] mem_lane, [7:5] bank, [4:0] register

RAWLANE2_DIG_FSM_FSM_MEM_ADDR_MON
Address: Operational Base + offset (0x3221)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	mem_addr Current value of memory address used in lane FSM

RAWLANE2_DIG_FSM_FSM_STATUS_MON
Address: Operational Base + offset (0x3222)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	rdmsk_disabled Check, if read mask is currently disabled (i.e. mask is all ones)
9	RO	0x0	wrmsk_disabled Check, if write mask is currently disabled (i.e. mask is all ones)
8	RO	0x0	wait_cnt_eq0 Check, if wait counter currently equals zero
7	RO	0x0	alu_res_eq0 Check, if ALU result register currently equals zero
6	RO	0x0	alu_ovflw Current value of ALU overflow bit
5	RO	0x0	cmd_rdy New command is ready for execution (applicable when FSM_OVRD_EN=1)
4:0	RO	0x00	state Current state of lane FSM

RAWLANE2_DIG_FSM_FSM_CR_REG_OP_XTND_EN

Address: Operational Base + offset (0x3223)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	cr_reg_op_xtnd_en CR interface timing extension enable 1'b0: No timing extension 1'b1: Timing extension

RAWLANE2_DIG_FSM_FAST_RX_STARTUP_CAL

Address: Operational Base + offset (0x3224)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_startup_cal Status of fast RX start-up calibration

RAWLANE2_DIG_FSM_FAST_RX_ADAPT

Address: Operational Base + offset (0x3225)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_adapt Status of fast RX adaptation

RAWLANE2_DIG_FSM_FAST_RX_AFE_CAL

Address: Operational Base + offset (0x3226)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RO	0x0	fast_rx_afe_cal Status of fast RX AFE DAC start-up calibration

RAWLANE2_DIG_FSM_FAST_RX_DFE_CAL

Address: Operational Base + offset (0x3227)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_cal Status of fast RX DFE slicer start-up calibration

RAWLANE2_DIG_FSM_FAST_RX_BYPASS_CAL

Address: Operational Base + offset (0x3228)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_bypass_cal Status of fast RX bypass slicer start-up calibration

RAWLANE2_DIG_FSM_FAST_RX_REFLVL_CAL

Address: Operational Base + offset (0x3229)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_reflvl_cal Status of fast RX reference level (100mv, 125mv, 150mv) start-up calibration

RAWLANE2_DIG_FSM_FAST_RX_IQ_CAL

Address: Operational Base + offset (0x322A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_cal Status of fast RX IQ start-up calibration

RAWLANE2_DIG_FSM_FAST_RX_AFE_ADAPT

Address: Operational Base + offset (0x322B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_adapt Status of fast RX AFE DAC start-up adaptation

RAWLANE2_DIG_FSM_FAST_RX_DFE_ADAPT

Address: Operational Base + offset (0x322C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_adapt Status of fast RX DFE DAC start-up adaptation

RAWLANE2_DIG_FSM_FAST_SUP

Address: Operational Base + offset (0x322D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_sup Status of fast support block (Rtune)

RAWLANE2_DIG_FSM_FAST_RX_IQ_WALK

Address: Operational Base + offset (0x322E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_walk Status of fast RX IQ walk start-up adaptation

RAWLANE2_DIG_FSM_FAST_RX_PWRUP

Address: Operational Base + offset (0x322F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_pwrup Status of fast RX power-up (LOS, VREG/AFE and DCC)

RAWLANE2_DIG_FSM_FAST_RX_VCO_WAIT

Address: Operational Base + offset (0x3230)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_wait Status of fast RX VCO wait times

RAWLANE2_DIG_FSM_FAST_RX_VCO_CAL

Address: Operational Base + offset (0x3231)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_cal Status of fast RX VCO calibration

RAWLANE2_DIG_FSM_FAST_RX_CONT_CAL_ADAPT

Address: Operational Base + offset (0x3233)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_cal_adapt Status of fast RX continuous calibration/adaptation

RAWLANE2_DIG_FSM_FAST_RX_CONT_ADAPT
Address: Operational Base + offset (0x3234)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_adapt Status of fast RX continuous adaptation

RAWLANE2_DIG_FSM_FAST_RX_CONT_DATA_CAL
Address: Operational Base + offset (0x3235)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_data_cal Status of fast RX continuous data calibration

RAWLANE2_DIG_FSM_FAST_RX_CONT_PHASE_CAL
Address: Operational Base + offset (0x3236)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_phase_cal Status of fast RX continuous phase calibration

RAWLANE2_DIG_FSM_FAST_RX_CONT_AFE_CAL
Address: Operational Base + offset (0x3237)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_afe_cal Status of fast RX continuous AFE calibration

RAWLANE2_DIG_FSM_FAST_RX_ATT_VGA_ADAPT
Address: Operational Base + offset (0x3238)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_0 Reserved

RAWLANE2_DIG_FSM_FAST_RX_CTLE_ADAPT
Address: Operational Base + offset (0x3239)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_1 Reserved

RAWLANE2_DIG_FSM_FAST_RX_VGA_ADAPT
Address: Operational Base + offset (0x323A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_2 Reserved

RAWLANE2_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT
Address: Operational Base + offset (0x323B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_3 Reserved

RAWLANE2_DIG_FSM_FAST_RX_IQ_ADAPT
Address: Operational Base + offset (0x323C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_adapt Status of fast RX IQ adapt start-up adaptation

RAWLANE2_DIG_FSM_RX_CTLE_ALGO_EH_SEL
Address: Operational Base + offset (0x323D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_ctle_algo_eh_sel Status of RX CTLE adapt selected algo

RAWLANE2_DIG_FSM_RX_IQ_PHASE_OFFSET
Address: Operational Base + offset (0x323F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	rx_iq_phase_offset Offset value for IQ phase calculation

RAWLANE2_DIG_AON_AFE_ATT_IDAC_OFST
Address: Operational Base + offset (0x3240)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_att_idac_ofst Offset value for AFE ATT iDAC

RAWLANE2_DIG_AON_AFE_CTLE_IDAC_OFST

Address: Operational Base + offset (0x3241)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_ctle_idac_ofst Offset value for AFE CTLE iDAC

RAWLANE2_DIG_AON_AFE_VGA1_IDAC_OFST

Address: Operational Base + offset (0x3242)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_vga1_idac_ofst Offset value for AFE VGA1 iDAC

RAWLANE2_DIG_AON_RX_ADAPT_FOM

Address: Operational Base + offset (0x3243)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom Adaptation figure of merit (FOM)

RAWLANE2_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST

Address: Operational Base + offset (0x3244)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_summer_odd_idac_ofst Offset value for DFE summer odd iDAC

RAWLANE2_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST

Address: Operational Base + offset (0x3245)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_even_vdac_ofst Offset value for DFE phase even vDAC

RAWLANE2_DIG_AON_DFE_PHASE_ODD_VDAC_OFST

Address: Operational Base + offset (0x3246)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_odd_vdac_ofst Offset value for DFE phase odd vDAC

RAWLANE2_DIG_AON_DFE_EVEN_REF_LVL
Address: Operational Base + offset (0x3247)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_even_ref_lvl DFE even reference level

RAWLANE2_DIG_AON_DFE_ODD_REF_LVL
Address: Operational Base + offset (0x3248)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_odd_ref_lvl DFE odd reference level

RAWLANE2_DIG_AON_RX_PHSADJ_LIN
Address: Operational Base + offset (0x3249)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x07	rx_phsadj_lin Linear value for RX phase adjust

RAWLANE2_DIG_AON_RX_PHSADJ_MAP
Address: Operational Base + offset (0x324A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_phsadj_map Mapped value for RX phase adjust

RAWLANE2_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST
Address: Operational Base + offset (0x324B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_high_vdac_ofst Offset value for DFE data even high vDAC

RAWLANE2_DIG_AON_CDR_UNLOCKED_CNT
Address: Operational Base + offset (0x324C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_low_vdac_ofst Offset value for DFE data even low vDAC

RAWLANE2_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST
Address: Operational Base + offset (0x324D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_high_vdac_ofst Offset value for DFE data odd high vDAC

RAWLANE2_DIG_AON_RX_ADAPT_DONE_NEW
Address: Operational Base + offset (0x324E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_low_vdac_ofst Offset value for DFE data odd low vDAC

RAWLANE2_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST
Address: Operational Base + offset (0x324F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_even_vdac_ofst Offset value for DFE bypass even vDAC

RAWLANE2_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST
Address: Operational Base + offset (0x3250)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_odd_vdac_ofst Offset value for DFE bypass odd vDAC

RAWLANE2_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST
Address: Operational Base + offset (0x3251)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

RAWLANE2_DIG_AON_DFE_ERROR_ODD_VDAC_OFST
Address: Operational Base + offset (0x3252)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

RAWLANE2_DIG_AON_RX_IQ_PHASE_ADJUST

Address: Operational Base + offset (0x3253)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_iq_phase_adjust Value for RX IQ phase adjust

RAWLANE2_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET

Address: Operational Base + offset (0x3254)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_iq_phase_delta_offset Value for RX IQ phase offset + delta value

RAWLANE2_DIG_AON_RX_FW_REVISION_PMA_LABEL

Address: Operational Base + offset (0x3255)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pma_label PMA label

RAWLANE2_DIG_AON_INIT_PWRUP_DONE

Address: Operational Base + offset (0x3256)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	init_pwrup_done Indicates whether initial power-up has completed or not.

RAWLANE2_DIG_AON_RX_ADPT_ATT

Address: Operational Base + offset (0x3257)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	att_adpt_val Stored RX adapted ATT value

RAWLANE2_DIG_AON_RX_ADPT_VGA

Address: Operational Base + offset (0x3258)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value

RAWLANE2_DIG_AON_RX_ADPT_CTLE

Address: Operational Base + offset (0x3259)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value

RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP1

Address: Operational Base + offset (0x325A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value

RAWLANE2_DIG_AON_RX_ADAPT_DONE

Address: Operational Base + offset (0x325B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_done Indicates whether RX adaptation has completed or not.

RAWLANE2_DIG_AON_FAST_FLAGS

Address: Operational Base + offset (0x325C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ctle_algo_eh_sel Decides between 1'b1 - "EYE_HEIGHT" or 1'b0 - "MIN_BOT_TOB" algorithms
14	RW	0x0	fast_rx_iq_adapt Enable fast RX IQ adapt
13	RW	0x0	fast_rx_iq_walk Enable fast RX IQ walk
12	RW	0x0	fast_rx_vco_cal Enable fast RX VCO calibration
11	RW	0x0	fast_rx_vco_wait Enable fast RX VCO wait times
10	RW	0x0	fast_rx_pwrup Enable fast RX power-up (LOS, VREG/AFE and DCC)
9	RW	0x0	fast_sup Enable fast support block (rtune)
8	RW	0x0	fast_rx_dfe_adapt Enables fast RX DFE DAC start-up adaptation

Bit	Attr	Reset Value	Description
7	RW	0x0	fast_rx_afe_adapt Enables fast RX AFE DAC start-up adaptation
6	RW	0x0	fast_rx_iq_cal Enables fast RX IQ start-up calibration
5	RW	0x0	fast_rx_reflvl_cal Enables fast RX reference level (100mv, 125mv, 150mv) start-up calibration
4	RW	0x0	fast_rx_bypass_cal Enables fast RX bypass slicer start-up calibration
3	RW	0x0	fast_rx_dfe_cal Enables fast RX DFE slicer start-up calibration
2	RW	0x0	fast_rx_afe_cal Enables fast RX AFE DAC start-up calibration
1	RW	0x0	fast_rx_adapt Enables fast RX adaptation
0	RW	0x0	fast_rx_startup_cal Enables fast RX start-up calibration

RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP2
Address: Operational Base + offset (0x325D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value

RAWLANE2_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT
Address: Operational Base + offset (0x325E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_lower_limit Stored boost val cost func lower limit

RAWLANE2_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT
Address: Operational Base + offset (0x325F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_upper_limit Stored boost val cost func upper limit

RAWLANE2_DIG_AON_RX_FW_REVISION_RAW_LABEL
Address: Operational Base + offset (0x3260)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	raw_label RAW label

RAWLANE2_DIG_AON_RX_SLICER_CTRL_EVEN
Address: Operational Base + offset (0x3261)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

RAWLANE2_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE
Address: Operational Base + offset (0x3262)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

RAWLANE2_DIG_AON_RX_FW_REVISION_PCS_LABEL
Address: Operational Base + offset (0x3263)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pcs_label PCS label

RAWLANE2_DIG_AON_ADPT_CTL_0
Address: Operational Base + offset (0x3264)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_ADPT_CTL_1
Address: Operational Base + offset (0x3265)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_ADPT_CTL_2
Address: Operational Base + offset (0x3266)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_ADPT_CTL_3
Address: Operational Base + offset (0x3267)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_ADPT_CTL_4
Address: Operational Base + offset (0x3268)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_ADPT_CTL_5
Address: Operational Base + offset (0x3269)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_ADPT_CTL_6
Address: Operational Base + offset (0x326A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_ADPT_CTL_7
Address: Operational Base + offset (0x326B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE2_DIG_AON_RX_FW_REVISION_FW_LABEL
Address: Operational Base + offset (0x326C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	fw_label FW label

RAWLANE2_DIG_AON_FAST_FLAGS_2
Address: Operational Base + offset (0x326D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11	RW	0x0	ctle_adapt_sts CTLE adaptation status flag
10	RW	0x0	fast_frl_adpt_byp_aft_ltp Enable fast FRL bypass after link training
9	RW	0x0	skip_ctle_bin_srch_abrt Skip CTLE binary search abort
8	RW	0x0	ctle_algo_two_pt_exit CTLE algo two point exit
7	RW	0x0	fast_rx_vga_adapt Enables fast RX VGA adaptation
6	RW	0x0	fast_rx_ctle_adapt Enables fast RX CTLE adaptation

Bit	Attr	Reset Value	Description
5	RW	0x0	fast_rx_att_vga_adapt Enables fast RX ATT_VGA adaptation
4	RW	0x0	fast_rx_cont_afe_cal Enables fast RX continuous AFE calibration
3	RW	0x0	fast_rx_cont_phase_cal Enables fast RX continuous phase calibration
2	RW	0x0	fast_rx_cont_data_cal Enables fast RX continuous data calibration
1	RW	0x0	fast_rx_cont_adapt Enables fast RX continuous adaptation
0	RW	0x0	fast_rx_cont_cal_adapt Enables fast RX continuous calibration/adaptation

RAWLANE2_DIG_AON_RX_RESERVED_REG_0
Address: Operational Base + offset (0x326E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_0 Reserved fields

RAWLANE2_DIG_AON_TXRX_OVRD_IN
Address: Operational Base + offset (0x326F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_disable_ovrd_en Override enable for rx_disable
0	RW	0x0	rx_disable_ovrd_val Override value for rx_disable

RAWLANE2_DIG_AON_RX_PHSADJ_LIN_LEFT
Address: Operational Base + offset (0x3270)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_left Linear value for RX phase adjust on left

RAWLANE2_DIG_AON_RX_PHSADJ_LIN_RIGHT
Address: Operational Base + offset (0x3271)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_right Linear value for RX phase adjust on right

RAWLANE2_DIG_AON_RX_PHSADJ_LIN_ADAPT
Address: Operational Base + offset (0x3272)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_adapt Linear value for RX phase adjust IQ adapt value

RAWLANE2_DIG_AON_RX_RESERVED_REG_1
Address: Operational Base + offset (0x3273)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_1 Reserved fields

RAWLANE2_DIG_AON_RX_ADPT_VGA_1
Address: Operational Base + offset (0x3278)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value 1st iter

RAWLANE2_DIG_AON_RX_ADPT_CTLE_1
Address: Operational Base + offset (0x3279)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value 1st iter

RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP1_1
Address: Operational Base + offset (0x327A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value 1st iter

RAWLANE2_DIG_AON_RX_ADPT_DFE_TAP2_1
Address: Operational Base + offset (0x327D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value 1st iter

RAWLANE2_DIG_IRQ_CTL_RESET_RTN_REQ
Address: Operational Base + offset (0x3280)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RW	0x1	reset_rtn_req Reset routine request

RAWLANE2_DIG_IRQ_CTL_RX_RESET_IRQ
Address: Operational Base + offset (0x3281)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_reset Rx reset interrupt

RAWLANE2_DIG_IRQ_CTL_RX_REQ_IRQ
Address: Operational Base + offset (0x3282)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_req Rx request interrupt

RAWLANE2_DIG_IRQ_CTL_RX_RATE_IRQ
Address: Operational Base + offset (0x3283)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_rate_irq Rx rate change interrupt request

RAWLANE2_DIG_IRQ_CTL_RX_PSTATE_IRQ
Address: Operational Base + offset (0x3284)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_pstate_irq Rx pstate change interrupt request

RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ
Address: Operational Base + offset (0x3285)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_req_irq Rx adaptation request interrupt

RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ
Address: Operational Base + offset (0x3286)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_adapt_dis_irq Rx adaptation disable interrupt

RAWLANE2_DIG_IRQ_CTL_RX_RESET_IRQ_CLR
Address: Operational Base + offset (0x3287)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_reset_irq_clr RX reset interrupt clear (self-clearing)

RAWLANE2_DIG_IRQ_CTL_RX_REQ_IRQ_CLR
Address: Operational Base + offset (0x3288)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_req_irq_clr RX request interrupt clear (self-clearing)

RAWLANE2_DIG_IRQ_CTL_RX_RATE_IRQ_CLR
Address: Operational Base + offset (0x3289)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_rate_irq_clr RX rate change interrupt clear (self-clearing)

RAWLANE2_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR
Address: Operational Base + offset (0x328A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_pstate_irq_clr RX pstate change interrupt clear (self-clearing)

RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR
Address: Operational Base + offset (0x328B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_req_irq_clr RX adaptation request interrupt clear (self-clearing)

RAWLANE2_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR
Address: Operational Base + offset (0x328C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_adapt_dis_irq_clr RX adaptation disable interrupt clear (self-clearing)

RAWLANE2_DIG_IRQ_CTL_IRQ_MASK
Address: Operational Base + offset (0x328D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	rx_initialize_irq_msk Mask for RX initialize interrupt (0 = cannot interrupt)
5	RW	0x0	rx_reset_irq_msk Mask for RX reset interrupt (0 = cannot interrupt)
4	RW	0x0	rx_adapt_dis_irq_msk Mask for RX adaptation disable interrupt (0 = cannot interrupt)
3	RW	0x0	rx_adapt_req_irq_msk Mask for RX adaptation request interrupt (0 = cannot interrupt)
2	RW	0x0	rx_pstate_irq_msk Mask for RX pstate change interrupt (0 = cannot interrupt)
1	RW	0x0	rx_rate_irq_msk Mask for RX rate change interrupt (0 = cannot interrupt)
0	RW	0x0	rx_req_irq_msk Mask for RX request interrupt (0 = cannot interrupt)

RAWLANE2_DIG_IRQ_CTL_RX_INITIALIZE_IRQ
Address: Operational Base + offset (0x328E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_initialize_irq Rx initialize interrupt request

RAWLANE2_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR
Address: Operational Base + offset (0x328F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_initialize_irq_clr RX initialize interrupt clear (self-clearing)

RAWLANE2_DIG_PMA_XF_RX_OVRD_OUT
Address: Operational Base + offset (0x32A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	rx_reset_ovrd_en Override enable for rx_reset
2	RW	0x0	rx_reset_ovrd_val Override value for rx_reset
1	RW	0x0	rx_req_ovrd_en Override enable for rx_req

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_req_ovrd_val Override value for rx_req

RAWLANE2_DIG_PMA_XF_RX_PMA_IN
Address: Operational Base + offset (0x32A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from PMA for rx_ack

RAWLANE2_DIG_RX_CTL_OFFCAN_CONT_STATUS
Address: Operational Base + offset (0x32E3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous offset cancellation

RAWLANE2_DIG_RX_CTL_ADAPT_CONT_STATUS
Address: Operational Base + offset (0x32E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous adaptation

RAWLANE3_DIG_PCS_XF_RX_OVRD_OUT_2
Address: Operational Base + offset (0x3303)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_valid_ovrd_en Enable override for rx_valid
0	RW	0x0	rx_valid Override value for rx_valid

RAWLANE3_DIG_PCS_XF_RX_PCS_IN_5
Address: Operational Base + offset (0x3304)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_valid Value from PCS for rx_valid_i

RAWLANE3_DIG_PCS_XF_RX_OVRD_IN
Address: Operational Base + offset (0x3305)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
10	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
9	RW	0x1	ovrd_en Enable override values for all fields in this register
8	RW	0x0	lpd Override value for rx_lpd
7:6	RW	0x0	pstate Override value for rx_pstate
5:4	RW	0x0	reserved Reserved
3:0	RW	0x0	rate Override value for rx_rate

RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_1
Address: Operational Base + offset (0x3306)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	req_ovrd_en Override enable for rx_req
2	RW	0x1	req_ovrd_val Override value for rx_req
1	RW	0x1	reset_ovrd_en Override enable for rx_reset
0	RW	0x1	reset_ovrd_val Override value for rx_reset

RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_2
Address: Operational Base + offset (0x3307)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	vco_val_ovrd_en Enable override for VCO controls
14	RW	0x0	vco_highfreq_val_ovrd Override value for rx_cdr_vco_highfreq
13	RW	0x0	vco_lowfreq_val_ovrd Override value for rx_cdr_vco_lowfreq
12:0	RW	0x0000	vco_ld_val_ovrd Override value for rx_vco_ld_val

RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_3
Address: Operational Base + offset (0x3308)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	cont_ovrd_en Enable override values for rx_adapt_cont and rx_offcan_cont

Bit	Attr	Reset Value	Description
3	RW	0x0	offcan_cont Override value for rx_offcan_cont
2	RW	0x0	adapt_cont Override value for rx_adapt_cont
1	RW	0x0	adapt_req_ovrd_en Enable override values for rx_adapt_req
0	RW	0x0	adapt_req Override value for rx_adapt_req

RAWLANE3_DIG_PCS_XF_RX_PCS_IN
Address: Operational Base + offset (0x3309)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reset Value from PCS for rx_reset
14	RO	0x0	offcan_cont Value from PCS for rx_offcan_cont
13	RO	0x0	adapt_cont Value from PCS for rx_adapt_cont
12	RO	0x0	adapt_req Value from PCS for rx_adapt_req
11	RO	0x0	adapt_dfe_en Value from PCS for rx_adapt_dfe_en
10	RO	0x0	adapt_afe_en Value from PCS for rx_adapt_afe_en
9	RO	0x0	lpd Value from PCS for rx_lpd
8:7	RO	0x0	pstate Value from PCS for rx_pstate
6:5	RO	0x0	reserved_r_1 Reserved
4:1	RO	0x0	rate Value from PCS for rx_rate
0	RO	0x0	req Value from PCS for rx_req

RAWLANE3_DIG_PCS_XF_RX_PCS_IN_1
Address: Operational Base + offset (0x330A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RO	0x00	ref_ld_val Value from PCS for rx_ref_ld_val

RAWLANE3_DIG_PCS_XF_RX_PCS_IN_2
Address: Operational Base + offset (0x330B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_vco_highfreq Value from PCS for rx_cdr_vco_highfreq

Bit	Attr	Reset Value	Description
13	RO	0x0	cdr_vco_lowfreq Value from PCS for rx_cdr_vco_lowfreq
12:0	RO	0x0000	vco_ld_val Value from PCS for rx_vco_ld_val

RAWLANE3_DIG_PCS_XF_RX_PCS_IN_3
Address: Operational Base + offset (0x330C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	eq_afe_rate Value from ASIC for rx_eq_afe_rate
13:12	RO	0x0	eq_ctle_pole Value from ASIC for rx_eq_ctle_pole
11:7	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
6:3	RO	0x0	eq_vga1_gain Value from ASIC for rx_eq_vga1_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

RAWLANE3_DIG_PCS_XF_RX_PCS_IN_4
Address: Operational Base + offset (0x330D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2
7:0	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1

RAWLANE3_DIG_PCS_XF_RX_OVRD_OUT
Address: Operational Base + offset (0x330E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x1	en_ctl Enable override values for all control outputs of this register
0	RW	0x1	ack Override value for rx_ack

RAWLANE3_DIG_PCS_XF_RX_PCS_OUT
Address: Operational Base + offset (0x330F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE3_DIG_PCS_XF_RX_ADAPT_ACK
Address: Operational Base + offset (0x3310)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RW	0x0	rx_eq_afe_rate_ovrd_val Override val for rx_eq_afe_rate[1:0]
9:8	RW	0x0	rx_eq_ctle_pole_ovrd_val Override val for rx_eq_ctle_pole[1:0]
7	RW	0x0	rx_eq_att_ovrd_en Individual override enable for ATT
6	RW	0x0	rx_eq_vga1_gain_ovrd_en Individual override enable for gain
5	RW	0x0	rx_eq_ctle_boost_ovrd_en Individual override enable for boost
4	RW	0x0	rx_eq_ctle_pole_ovrd_en Individual override enable for pole
3	RW	0x0	rx_eq_afe_rate_ovrd_en Individual override enable for rate
2	RW	0x0	rx_eq_dfe_t1_ovrd_en Individual override enable for TAP1
1	RW	0x0	rx_eq_dfe_t2_ovrd_en Individual override enable for TAP2
0	RW	0x0	rx_adapt_ack RX adaptation Acknowledge

RAWLANE3_DIG_PCS_XF_RX_ADAPT_FOM
Address: Operational Base + offset (0x3311)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom RX adaptation figure of merit

RAWLANE3_DIG_PCS_XF_RX_OVRD_IN_4
Address: Operational Base + offset (0x3312)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	ref_ld_val_ovrd_en Enable override for rx_ref_ld_val
6:0	RW	0x00	ref_ld_val_ovrd Override value for rx_ref_ld_val

RAWLANE3_DIG_PCS_XF_RX_PCS_OUT_2
Address: Operational Base + offset (0x3313)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANE3_DIG_PCS_XF_LANE_NUMBER
Address: Operational Base + offset (0x3315)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	lane_number Current lane number

RAWLANE3_DIG_PCS_XF_ATE_OVRD_IN

Address: Operational Base + offset (0x3318)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rx_adapt_dfe_en_ovrd_en Enable override value for rx_adapt_dfe_en input
6	RW	0x0	rx_adapt_dfe_en_ovrd_val Override value for rx_adapt_dfe_en input
5	RW	0x0	rx_adapt_afe_en_ovrd_en Enable override value for rx_adapt_afe_en input
4	RW	0x0	rx_adapt_afe_en_ovrd_val Override value for rx_adapt_afe_en input
3	RW	0x0	rx_req_ate_ovrd_en Enable override value for rx_req input
2	RW	0x0	rx_req_ate_ovrd_val Override value for top-level rx_req input
1	RW	0x0	rx_reset_ate_ovrd_en Enable override value for rx_reset input
0	RW	0x0	rx_reset_ate_ovrd_val Override value for top-level rx_reset input

RAWLANE3_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN

Address: Operational Base + offset (0x3319)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	rx_eq_delta_iq_ovrd_en Enable override value for rx_eq_delta_iq
3:0	RW	0x0	rx_eq_delta_iq_ovrd_val Override value for rx_eq_delta_iq

RAWLANE3_DIG_PCS_XF_RX_EQ_OVRD_IN_1

Address: Operational Base + offset (0x331D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:8	RW	0x00	rx_eq_ctle_boost_ovrd_val Override value for rx_eq_ctle_boost[4:0]
7	RW	0x0	rx_eq_ovrd_en Enable override values for all RX EQ settings
6:4	RW	0x0	rx_eq_att_lvl_ovrd_val Override value for rx_eq_att_lvl[2:0]
3:0	RW	0x0	rx_eq_afe_gain_ovrd_val Override value for rx_eq_afe_gain[3:0]

RAWLANE3_DIG_PCS_XF_RX_EQ_OVRD_IN_2
Address: Operational Base + offset (0x331E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	rx_eq_dfe_tap2_ovrd_val Override value for rx_eq_dfe_tap2[7:0]
7:0	RW	0x00	rx_eq_dfe_tap1_ovrd_val Override value for rx_eq_dfe_tap1[7:0]

RAWLANE3_DIG_FSM_FSM_FSM_OVRD_CTL
Address: Operational Base + offset (0x3320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RW	0x0	fsm_ovrd_en Enable overriding the FSM execution of commands must be asserted to use FSM_CMD_START and FSM_JMP_EN features
13	RW	0x0	fsm_cmd_start Start executing the new command, this is a self-clearing bit
12	RW	0x0	fsm_jmp_en Force the FSM to jump to FSM_JMP_ADDR in the program memory is applied when FSM_CMD_START is pulsed.
11:0	RW	0x000	fsm_jmp_addr The jump address used when FSM_JUMP_EN=1, the address is encoded as follows: [11:8] mem_lane, [7:5] bank, [4:0] register

RAWLANE3_DIG_FSM_FSM_MEM_ADDR_MON
Address: Operational Base + offset (0x3321)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	mem_addr Current value of memory address used in lane FSM

RAWLANE3_DIG_FSM_FSM_STATUS_MON
Address: Operational Base + offset (0x3322)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	rdmsk_disabled Check, if read mask is currently disabled (i.e. mask is all ones)
9	RO	0x0	wrmsk_disabled Check, if write mask is currently disabled (i.e. mask is all ones)
8	RO	0x0	wait_cnt_eq0 Check, if wait counter currently equals zero
7	RO	0x0	alu_res_eq0 Check, if ALU result register currently equals zero
6	RO	0x0	alu_ovflw Current value of ALU overflow bit
5	RO	0x0	cmd_rdy New command is ready for execution (applicable when FSM_OVRD_EN=1)

Bit	Attr	Reset Value	Description
4:0	RO	0x00	state Current state of lane FSM

RAWLANE3_DIG_FSM_FSM_CR_REG_OP_XTND_EN
Address: Operational Base + offset (0x3323)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	cr_reg_op_xtnd_en CR interface timing extension enable 1'b0: No timing extension 1'b1: Timing extension

RAWLANE3_DIG_FSM_FAST_RX_STARTUP_CAL
Address: Operational Base + offset (0x3324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_startup_cal Status of fast RX start-up calibration

RAWLANE3_DIG_FSM_FAST_RX_ADAPT
Address: Operational Base + offset (0x3325)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_adapt Status of fast RX adaptation

RAWLANE3_DIG_FSM_FAST_RX_AFE_CAL
Address: Operational Base + offset (0x3326)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_cal Status of fast RX AFE DAC start-up calibration

RAWLANE3_DIG_FSM_FAST_RX_DFE_CAL
Address: Operational Base + offset (0x3327)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_cal Status of fast RX DFE slicer start-up calibration

RAWLANE3_DIG_FSM_FAST_RX_BYPASS_CAL
Address: Operational Base + offset (0x3328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_bypass_cal Status of fast RX bypass slicer start-up calibration

RAWLANE3_DIG_FSM_FAST_RX_REFLVL_CAL
Address: Operational Base + offset (0x3329)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_reflvl_cal Status of fast RX reference level (100mv, 125mv, 150mv) start-up calibration

RAWLANE3_DIG_FSM_FAST_RX_IQ_CAL
Address: Operational Base + offset (0x332A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_cal Status of fast RX IQ start-up calibration

RAWLANE3_DIG_FSM_FAST_RX_AFE_ADAPT
Address: Operational Base + offset (0x332B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_adapt Status of fast RX AFE DAC start-up adaptation

RAWLANE3_DIG_FSM_FAST_RX_DFE_ADAPT
Address: Operational Base + offset (0x332C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_adapt Status of fast RX DFE DAC start-up adaptation

RAWLANE3_DIG_FSM_FAST_SUP
Address: Operational Base + offset (0x332D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_sup Status of fast support block (Rtune)

RAWLANE3_DIG_FSM_FAST_RX_IQ_WALK
Address: Operational Base + offset (0x332E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_walk Status of fast RX IQ walk start-up adaptation

RAWLANE3_DIG_FSM_FAST_RX_PWRUP
Address: Operational Base + offset (0x332F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_pwrup Status of fast RX power-up (LOS, VREG/AFE and DCC)

RAWLANE3_DIG_FSM_FAST_RX_VCO_WAIT
Address: Operational Base + offset (0x3330)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_wait Status of fast RX VCO wait times

RAWLANE3_DIG_FSM_FAST_RX_VCO_CAL
Address: Operational Base + offset (0x3331)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_cal Status of fast RX VCO calibration

RAWLANE3_DIG_FSM_FAST_RX_CONT_CAL_ADAPT
Address: Operational Base + offset (0x3333)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_cal_adapt Status of fast RX continuous calibration/adaptation

RAWLANE3_DIG_FSM_FAST_RX_CONT_ADAPT
Address: Operational Base + offset (0x3334)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_adapt Status of fast RX continuous adaptation

RAWLANE3_DIG_FSM_FAST_RX_CONT_DATA_CAL
Address: Operational Base + offset (0x3335)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_data_cal Status of fast RX continuous data calibration

RAWLANE3_DIG_FSM_FAST_RX_CONT_PHASE_CAL
Address: Operational Base + offset (0x3336)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_phase_cal Status of fast RX continuous phase calibration

RAWLANE3_DIG_FSM_FAST_RX_CONT_AFE_CAL
Address: Operational Base + offset (0x3337)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_afe_cal Status of fast RX continuous AFE calibration

RAWLANE3_DIG_FSM_FAST_RX_ATT_VGA_ADAPT
Address: Operational Base + offset (0x3338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_0 Reserved

RAWLANE3_DIG_FSM_FAST_RX_CTLE_ADAPT
Address: Operational Base + offset (0x3339)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_1 Reserved

RAWLANE3_DIG_FSM_FAST_RX_VGA_ADAPT
Address: Operational Base + offset (0x333A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_2 Reserved

RAWLANE3_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT
Address: Operational Base + offset (0x333B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_3 Reserved

RAWLANE3_DIG_FSM_FAST_RX_IQ_ADAPT
Address: Operational Base + offset (0x333C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_adapt Status of fast RX IQ adapt start-up adaptation

RAWLANE3_DIG_FSM_RX_CTLE_ALGO_EH_SEL
Address: Operational Base + offset (0x333D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_ctle_algo_eh_sel Status of RX CTLE adapt selected algo

RAWLANE3_DIG_FSM_RX_IQ_PHASE_OFFSET
Address: Operational Base + offset (0x333F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	rx_iq_phase_offset Offset value for IQ phase calculation

RAWLANE3_DIG_AON_AFE_ATT_IDAC_OFST
Address: Operational Base + offset (0x3340)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_att_idac_ofst Offset value for AFE ATT iDAC

RAWLANE3_DIG_AON_AFE_CTLE_IDAC_OFST
Address: Operational Base + offset (0x3341)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_ctle_idac_ofst Offset value for AFE CTLE iDAC

RAWLANE3_DIG_AON_AFE_VGA1_IDAC_OFST
Address: Operational Base + offset (0x3342)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_vga1_idac_ofst Offset value for AFE VGA1 iDAC

RAWLANE3_DIG_AON_RX_ADAPT_FOM
Address: Operational Base + offset (0x3343)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom Adaptation figure of merit (FOM)

RAWLANE3_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST
Address: Operational Base + offset (0x3344)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_summer_odd_idac_ofst Offset value for DFE summer odd iDAC

RAWLANE3_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST
Address: Operational Base + offset (0x3345)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_even_vdac_ofst Offset value for DFE phase even vDAC

RAWLANE3_DIG_AON_DFE_PHASE_ODD_VDAC_OFST
Address: Operational Base + offset (0x3346)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_odd_vdac_ofst Offset value for DFE phase odd vDAC

RAWLANE3_DIG_AON_DFE_EVEN_REF_LVL
Address: Operational Base + offset (0x3347)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_even_ref_lvl DFE even reference level

RAWLANE3_DIG_AON_DFE_ODD_REF_LVL
Address: Operational Base + offset (0x3348)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_odd_ref_lvl DFE odd reference level

RAWLANE3_DIG_AON_RX_PHSADJ_LIN
Address: Operational Base + offset (0x3349)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x07	rx_phsadj_lin Linear value for RX phase adjust

RAWLANE3_DIG_AON_RX_PHSADJ_MAP
Address: Operational Base + offset (0x334A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_phsadj_map Mapped value for RX phase adjust

RAWLANE3_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST
Address: Operational Base + offset (0x334B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_high_vdac_ofst Offset value for DFE data even high vDAC

RAWLANE3_DIG_AON_CDR_UNLOCKED_CNT
Address: Operational Base + offset (0x334C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_low_vdac_ofst Offset value for DFE data even low vDAC

RAWLANE3_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST
Address: Operational Base + offset (0x334D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_high_vdac_ofst Offset value for DFE data odd high vDAC

RAWLANE3_DIG_AON_RX_ADAPT_DONE_NEW
Address: Operational Base + offset (0x334E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_low_vdac_ofst Offset value for DFE data odd low vDAC

RAWLANE3_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST
Address: Operational Base + offset (0x334F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_even_vdac_ofst Offset value for DFE bypass even vDAC

RAWLANE3_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST
Address: Operational Base + offset (0x3350)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_odd_vdac_ofst Offset value for DFE bypass odd vDAC

RAWLANE3_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST
Address: Operational Base + offset (0x3351)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

RAWLANE3_DIG_AON_DFE_ERROR_ODD_VDAC_OFST
Address: Operational Base + offset (0x3352)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

RAWLANE3_DIG_AON_RX_IQ_PHASE_ADJUST
Address: Operational Base + offset (0x3353)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_iq_phase_adjust Value for RX IQ phase adjust

RAWLANE3_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET
Address: Operational Base + offset (0x3354)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_iq_phase_delta_offset Value for RX IQ phase offset + delta value

RAWLANE3_DIG_AON_RX_FW_REVISION_PMA_LABEL
Address: Operational Base + offset (0x3355)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pma_label PMA label

RAWLANE3_DIG_AON_INIT_PWRUP_DONE
Address: Operational Base + offset (0x3356)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	init_pwrup_done Indicates whether initial power-up has completed or not.

RAWLANE3_DIG_AON_RX_ADPT_ATT
Address: Operational Base + offset (0x3357)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	att_adpt_val Stored RX adapted ATT value

RAWLANE3_DIG_AON_RX_ADPT_VGA
Address: Operational Base + offset (0x3358)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value

RAWLANE3_DIG_AON_RX_ADPT_CTLE
Address: Operational Base + offset (0x3359)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value

RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP1
Address: Operational Base + offset (0x335A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value

RAWLANE3_DIG_AON_RX_ADAPT_DONE

Address: Operational Base + offset (0x335B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_done Indicates whether RX adaptation has completed or not.

RAWLANE3_DIG_AON_FAST_FLAGS

Address: Operational Base + offset (0x335C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ctle_algo_eh_sel Decides between 1'b1 - "EYE_HEIGHT" or 1'b0 - "MIN_BOT_TOB" algorithms
14	RW	0x0	fast_rx_iq_adapt Enable fast RX IQ adapt
13	RW	0x0	fast_rx_iq_walk Enable fast RX IQ walk
12	RW	0x0	fast_rx_vco_cal Enable fast RX VCO calibration
11	RW	0x0	fast_rx_vco_wait Enable fast RX VCO wait times
10	RW	0x0	fast_rx_pwrup Enable fast RX power-up (LOS, VREG/AFE and DCC)
9	RW	0x0	fast_sup Enable fast support block (rtune)
8	RW	0x0	fast_rx_dfe_adapt Enables fast RX DFE DAC start-up adaptation
7	RW	0x0	fast_rx_afe_adapt Enables fast RX AFE DAC start-up adaptation
6	RW	0x0	fast_rx_iq_cal Enables fast RX IQ start-up calibration
5	RW	0x0	fast_rx_reflvl_cal Enables fast RX reference level (100mv, 125mv, 150mv) start-up calibration
4	RW	0x0	fast_rx_bypass_cal Enables fast RX bypass slicer start-up calibration
3	RW	0x0	fast_rx_dfe_cal Enables fast RX DFE slicer start-up calibration
2	RW	0x0	fast_rx_afe_cal Enables fast RX AFE DAC start-up calibration
1	RW	0x0	fast_rx_adapt Enables fast RX adaptation
0	RW	0x0	fast_rx_startup_cal Enables fast RX start-up calibration

RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP2
Address: Operational Base + offset (0x335D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value

RAWLANE3_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT
Address: Operational Base + offset (0x335E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_lower_limit Stored boost val cost func lower limit

RAWLANE3_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT
Address: Operational Base + offset (0x335F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_upper_limit Stored boost val cost func upper limit

RAWLANE3_DIG_AON_RX_FW_REVISION_RAW_LABEL
Address: Operational Base + offset (0x3360)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	raw_label RAW label

RAWLANE3_DIG_AON_RX_SLICER_CTRL_EVEN
Address: Operational Base + offset (0x3361)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

RAWLANE3_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE
Address: Operational Base + offset (0x3362)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

RAWLANE3_DIG_AON_RX_FW_REVISION_PCS_LABEL

Address: Operational Base + offset (0x3363)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pcs_label PCS label

RAWLANE3_DIG_AON_ADPT_CTL_0

Address: Operational Base + offset (0x3364)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_ADPT_CTL_1

Address: Operational Base + offset (0x3365)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_ADPT_CTL_2

Address: Operational Base + offset (0x3366)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_ADPT_CTL_3

Address: Operational Base + offset (0x3367)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_ADPT_CTL_4

Address: Operational Base + offset (0x3368)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_ADPT_CTL_5

Address: Operational Base + offset (0x3369)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_ADPT_CTL_6

Address: Operational Base + offset (0x336A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_ADPT_CTL_7
Address: Operational Base + offset (0x336B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANE3_DIG_AON_RX_FW_REVISION_FW_LABEL
Address: Operational Base + offset (0x336C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	fw_label FW label

RAWLANE3_DIG_AON_FAST_FLAGS_2
Address: Operational Base + offset (0x336D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11	RW	0x0	ctle_adapt_sts CTLE adaptation status flag
10	RW	0x0	fast_frl_adpt_byp_aft_ltp Enable fast FRL bypass after link training
9	RW	0x0	skip_ctle_bin_srch_abrt Skip CTLE binary search abort
8	RW	0x0	ctle_algo_two_pt_exit CTLE algo two point exit
7	RW	0x0	fast_rx_vga_adapt Enables fast RX VGA adaptation
6	RW	0x0	fast_rx_ctle_adapt Enables fast RX CTLE adaptation
5	RW	0x0	fast_rx_att_vga_adapt Enables fast RX ATT_VGA adaptation
4	RW	0x0	fast_rx_cont_afe_cal Enables fast RX continuous AFE calibration
3	RW	0x0	fast_rx_cont_phase_cal Enables fast RX continuous phase calibration
2	RW	0x0	fast_rx_cont_data_cal Enables fast RX continuous data calibration
1	RW	0x0	fast_rx_cont_adapt Enables fast RX continuous adaptation
0	RW	0x0	fast_rx_cont_cal_adapt Enables fast RX continuous calibration/adaptation

RAWLANE3_DIG_AON_RX_RESERVED_REG_0
Address: Operational Base + offset (0x336E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	reserved_0 Reserved fields

RAWLANE3_DIG_AON_TXRX_OVRD_IN
Address: Operational Base + offset (0x336F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_disable_ovrd_en Override enable for rx_disable
0	RW	0x0	rx_disable_ovrd_val Override value for rx_disable

RAWLANE3_DIG_AON_RX_PHSADJ_LIN_LEFT
Address: Operational Base + offset (0x3370)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_left Linear value for RX phase adjust on left

RAWLANE3_DIG_AON_RX_PHSADJ_LIN_RIGHT
Address: Operational Base + offset (0x3371)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_right Linear value for RX phase adjust on right

RAWLANE3_DIG_AON_RX_PHSADJ_LIN_ADAPT
Address: Operational Base + offset (0x3372)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_adapt Linear value for RX phase adjust IQ adapt value

RAWLANE3_DIG_AON_RX_RESERVED_REG_1
Address: Operational Base + offset (0x3373)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_1 Reserved fields

RAWLANE3_DIG_AON_RX_ADPT_VGA_1
Address: Operational Base + offset (0x3378)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use

Bit	Attr	Reset Value	Description
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value 1st iter

RAWLANE3_DIG_AON_RX_ADPT_CTLE_1
Address: Operational Base + offset (0x3379)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value 1st iter

RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP1_1
Address: Operational Base + offset (0x337A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value 1st iter

RAWLANE3_DIG_AON_RX_ADPT_DFE_TAP2_1
Address: Operational Base + offset (0x337D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value 1st iter

RAWLANE3_DIG_IRQ_CTL_RESET_RTN_REQ
Address: Operational Base + offset (0x3380)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x1	reset_rtn_req Reset routine request

RAWLANE3_DIG_IRQ_CTL_RX_RESET_IRQ
Address: Operational Base + offset (0x3381)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_reset Rx reset interrupt

RAWLANE3_DIG_IRQ_CTL_RX_REQ_IRQ
Address: Operational Base + offset (0x3382)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_req Rx request interrupt

RAWLANE3_DIG_IRQ_CTL_RX_RATE_IRQ
Address: Operational Base + offset (0x3383)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_rate_irq Rx rate change interrupt request

RAWLANE3_DIG_IRQ_CTL_RX_PSTATE_IRQ
Address: Operational Base + offset (0x3384)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_pstate_irq Rx pstate change interrupt request

RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ
Address: Operational Base + offset (0x3385)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_req_irq Rx adaptation request interrupt

RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ
Address: Operational Base + offset (0x3386)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_dis_irq Rx adaptation disable interrupt

RAWLANE3_DIG_IRQ_CTL_RX_RESET_IRQ_CLR
Address: Operational Base + offset (0x3387)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_reset_irq_clr RX reset interrupt clear (self-clearing)

RAWLANE3_DIG_IRQ_CTL_RX_REQ_IRQ_CLR
Address: Operational Base + offset (0x3388)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RW	0x0	rx_req_irq_clr RX request interrupt clear (self-clearing)

RAWLANE3_DIG_IRQ_CTL_RX_RATE_IRQ_CLR
Address: Operational Base + offset (0x3389)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_rate_irq_clr RX rate change interrupt clear (self-clearing)

RAWLANE3_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR
Address: Operational Base + offset (0x338A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_pstate_irq_clr RX pstate change interrupt clear (self-clearing)

RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR
Address: Operational Base + offset (0x338B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_req_irq_clr RX adaptation request interrupt clear (self-clearing)

RAWLANE3_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR
Address: Operational Base + offset (0x338C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_dis_irq_clr RX adaptation disable interrupt clear (self-clearing)

RAWLANE3_DIG_IRQ_CTL_IRQ_MASK
Address: Operational Base + offset (0x338D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	rx_initialize_irq_msk Mask for RX initialize interrupt (0 = cannot interrupt)
5	RW	0x0	rx_reset_irq_msk Mask for RX reset interrupt (0 = cannot interrupt)
4	RW	0x0	rx_adapt_dis_irq_msk Mask for RX adaptation disable interrupt (0 = cannot interrupt)
3	RW	0x0	rx_adapt_req_irq_msk Mask for RX adaptation request interrupt (0 = cannot interrupt)

Bit	Attr	Reset Value	Description
2	RW	0x0	rx_pstate_irq_msk Mask for RX pstate change interrupt (0 = cannot interrupt)
1	RW	0x0	rx_rate_irq_msk Mask for RX rate change interrupt (0 = cannot interrupt)
0	RW	0x0	rx_req_irq_msk Mask for RX request interrupt (0 = cannot interrupt)

RAWLANE3_DIG_IRQ_CTL_RX_INITIALIZE_IRQ
Address: Operational Base + offset (0x338E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_initialize_irq Rx initialize interrupt request

RAWLANE3_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR
Address: Operational Base + offset (0x338F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_initialize_irq_clr RX initialize interrupt clear (self-clearing)

RAWLANE3_DIG_PMA_XF_RX_OVRD_OUT
Address: Operational Base + offset (0x33A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	rx_reset_ovrd_en Override enable for rx_reset
2	RW	0x0	rx_reset_ovrd_val Override value for rx_reset
1	RW	0x0	rx_req_ovrd_en Override enable for rx_req
0	RW	0x0	rx_req_ovrd_val Override value for rx_req

RAWLANE3_DIG_PMA_XF_RX_PMA_IN
Address: Operational Base + offset (0x33A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from PMA for rx_ack

RAWLANE3_DIG_RX_CTL_OFFCAN_CONT_STATUS
Address: Operational Base + offset (0x33E3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous offset cancellation

RAWLANE3_DIG_RX_CTL_ADAPT_CONT_STATUS

Address: Operational Base + offset (0x33E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous adaptation

RAWMEM_DIG_ROM_CMNX_BY_RZ

Address: Operational Base + offset (0x4000~0x4FFF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x8002	data Memory data

RAWMEM_DIG_RAM_CMNX_BY_RZ

Address: Operational Base + offset (0x6000~0x6FFF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x8002	data Memory data

SUPX_DIG_IDCODE_LO

Address: Operational Base + offset (0x8000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x04cd	data Data

SUPX_DIG_IDCODE_HI

Address: Operational Base + offset (0x8001)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x3006	data Data

SUPX_DIG_REFCLK_OVRD_IN

Address: Operational Base + offset (0x8002)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	bg_en_ovrd_en Enable override for bg_en
12	RW	0x0	bg_en Override value for bg_en
11	RW	0x0	ref_clk_range_ovrd_en Enable override for ref_range

Bit	Attr	Reset Value	Description
10:8	RW	0x7	ref_clk_range Override value for ref_range
7	RW	0x0	reserved_7 Reserved_7
6	RW	0x0	reserved_6 Reserved_6
5	RW	0x0	reserved_5 Reserved_5
4	RW	0x0	reserved_4 Reserved_4
3	RW	0x0	reserved_3 Reserved_3
2	RW	0x0	reserved_2 Reserved_2
1	RW	0x0	ref_clk_en_ovrd_en Enable override for ref_clk_en
0	RW	0x0	ref_clk_en Override value for ref_clk_en

SUPX_DIG_RX_TERM_ACDC_EN_OVRD_IN
Address: Operational Base + offset (0x8003)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	term_ovrd_en Enable override for rx_term_acdc and rx_term_en
1	RW	0x0	reserved_1 Reserved_1
0	RW	0x0	term_en Override value for rx_term_en

SUPX_DIG_TMDSCLK_CTRL_OVRD_IN
Address: Operational Base + offset (0x8004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	tmdsclk_digmux_ovrd_en Override enable for tmdsclk_digmux_en
4	RW	0x0	tmdsclk_digmux_en Override value for tmdsclk_digmux_en
3	RW	0x0	tmdsclk_rst_ovrd_en Override enable for tmdsclk_rst
2	RW	0x1	tmdsclk_rst Override value for tmdsclk_rst
1	RW	0x0	tmdsclk_en_ovrd_en Override enable for tmdsclk_en
0	RW	0x0	tmdsclk_en Override value for tmdsclk_en

SUPX_DIG_SUP_OVRD_IN
Address: Operational Base + offset (0x800D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	res_ovrd_en Enable override of res_req_in and res_ack_in
3	RW	0x1	res_ack_in Override value for res_ack_in
2	RW	0x0	res_req_in Override value for res_req_in
1	RW	0x0	rtune_ovrd_en Enable override of rtune_req
0	RW	0x0	rtune_req Override value for rtune_req

SUPX_DIG_SUP_OVRD_OUT

Address: Operational Base + offset (0x800E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	bg_lane_state_ovrd_en Enable override for bg_lane_state signal
6	RW	0x0	bg_lane_state Override value for bg_lane_state signal
5	RW	0x0	res_ack_out_ovrd_en Enable override for res_ack_out output
4	RW	0x1	res_ack_out Override value for res_ack_out output
3	RW	0x0	res_req_out_ovrd_en Enable override for res_req_out output
2	RW	0x0	res_req_out Override value for res_req_out output
1	RW	0x0	rtune_ack_ovrd_en Enable override for rtune_ack output
0	RW	0x0	rtune_ack Override value for rtune_ack output

SUPX_DIG_LVL_OVRD_IN

Address: Operational Base + offset (0x800F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_vref_ctrl_en Enable override value for rx_vref_ctrl
4:0	RW	0x10	rx_vref_ctrl Override value for rx_vref_ctrl

SUPX_DIG_DEBUG

Address: Operational Base + offset (0x8010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use

Bit	Attr	Reset Value	Description
2:0	RW	0x0	dtb_sel The lane DTB's are OR'd together with the support DTB signals selected with the below encodings 3'b000: None 3'b001: None 3'b010: None 3'b011: Rtune DTB output

SUPX_DIG_RX_TERM_EN_ACDC_IN
Address: Operational Base + offset (0x8018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RO	0x0	rereseved_1 Reserved_1
0	RO	0x0	rx_term_en Value from ASIC for rx_term_en

SUPX_DIG_ASIC_IN
Address: Operational Base + offset (0x8019)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	rx_dig_det0vn_en Value to ASIC for rx_dig_det0Vn_en
13	RO	0x0	rx_dig_det0vp_en Value to ASIC for rx_dig_det0Vp_en
12	RO	0x0	res_ack_out Value to ASIC for res_ack_out_i
11	RO	0x0	res_ack_in Value from ASIC for res_req_in
10	RO	0x0	res_req_out Value to ASIC for res_ack_out_i
9	RO	0x0	res_req_in Value from ASIC for res_req_in
8	RO	0x0	rtune_ack Value to ASIC for rtune_ack_i
7	RO	0x0	rtune_req Value from ASIC for rtune_req
6	RO	0x0	test_powerdown Value from ASIC for test_powerdown
5	RO	0x0	test_burnin Value from ASIC for test_burnin
4	RO	0x0	reserved_4 Reserved_4
3	RO	0x0	reserved_3 Reserved_3
2	RO	0x0	reserved_2 Reserved_2
1	RO	0x0	ref_clk_en Value from ASIC for ref_clk_en

Bit	Attr	Reset Value	Description
0	RO	0x0	phy_reset Value from ASIC for phy_reset

SUPX_DIG_LVL_ASIC_IN

Address: Operational Base + offset (0x801A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_vref_ctrl Value from ASIC for rx_vref_ctrl

SUPX_DIG_BANDGAP_ASIC_IN

Address: Operational Base + offset (0x801B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	bg_en Value from ASIC for bg_en

SUPX_DIG_CLK_RST_BG_PWRUP_TIME_0

Address: Operational Base + offset (0x8038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	fast_bg_wait Enable fast BG times (simulation only)
8:0	RW	0x082	bg_sup_en_time Power up time (in ref_range cycles) for bandgap in SUP (spec >=5us)

SUPX_DIG_CLK_RST_BG_PWRUP_TIME_1

Address: Operational Base + offset (0x8039)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x208	bg_lane_en_time Power up time (in ref_range cycles) for bandgap in LANE (spec >= 20us)

SUPX_DIG_ANA_CREGS_ANA_RTUNE_OVRD_IN

Address: Operational Base + offset (0x804A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rt_en_frcon Local rtune block enable control, force rtune block on, if asserted
6	RW	0x0	reserved Reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	rt_dac_mode_1_ RT_DAC_MODE[1]
4	RW	0x0	rt_dac_mode_0_ For 0 NOP, 1 DAC drives atb_s_p or atb_s_m
3	RW	0x0	rt_dac_chop For 0 atb_s_m, for 1 atb_s_p
2	RW	0x0	rt_atb Rtune ATB mode control. Combines with rt_ana_mode[1:0] to perform different functions
1	RW	0x0	rt_sel_atbp Rtune ATB input select: RT_SEL_ATBP function 1'b1: Select atb_s_p 1'b0: Select atb_s_m
0	RW	0x0	rt_sel_atbf Rtune ATB input select: RT_SEL_ATBF function 1'b1: Select gd as input 1'b0: Select atb_s_p/m as input

SUPX_DIG_ANA_CREGS_ANA_ATB_IN
Address: Operational Base + offset (0x804B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	sup_ana_ovl_osc_disable4test_int Force the output of protection oscillator
6	RW	0x0	atb_switch_6 Connect atb_s_p to atb_s_m, if asserted
5	RW	0x0	atb_switch_5 Connect atb_s_p to vph, if asserted
4	RW	0x0	atb_switch_4 Connect atb_s_p to gd, if asserted
3	RW	0x0	atb_switch_3 Connect atb_s_p to vp, if asserted
2	RW	0x0	atb_switch_2 Connect atb_s_p to vbg_vref, if asserted
1	RW	0x0	atb_switch_1 Connect atb_s_p to vph, if asserted
0	RW	0x0	atb_switch_0 Connect atb_s_p to vbg_bias_vref, if asserted

SUPX_DIG_ANA_CREGS_ANA_BG_IN
Address: Operational Base + offset (0x804D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RW	0x1	sel_clk_vref VREG clk reference voltage control.
9:8	RW	0x1	sel_vco_vref VREG VCO reference voltage control.

Bit	Attr	Reset Value	Description
7:6	RW	0x0	sup_ovl_osc_width_int Pulse width of over-current protection oscillator clk_ovl_osc_width[1:0] 2'b00: Pulse width is 64, that is 14.08us, and pulse period is 225.28us 2'b01: Pulse width is 1, that is 0.22us, and pulse period is 225.28us 2'b10: Pulse width is 128, that is 28.16us, and pulse period is 225.28us 2'b11: Pulse width is 32, that is 7.04us, and pulse period is 225.28us Counter width: 1024. Single clock period: 220ns
5	RW	0x0	temp_meas If asserted, enable temperature measurement. Vbe is sent to atb_s_m, vbg is sent to atb_s_p
4	RW	0x0	por_start_kick_en Enable fast startup using bg kick voltage for POR bandgap outputs
3	RW	0x1	chop_en_int Enable chopper clock for bandgap
2:1	RW	0x1	sel_vbg_vref vbg_vref voltage level select. Default value is 2'b01
0	RW	0x0	bypass_bg Bypass bandgap with VP

SUPX_DIG_ANA_CREGS_TMDS_CLK_SETTING

Address: Operational Base + offset (0x804E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:3	RW	0x0	tmdsclk_threshold TMDS clock sense circuit threshold value. Default value is 2'b00
2:1	RW	0x0	tmdsclk_hyst TMDS clock sense circuit hysterisis value. Default value is 2'b00
0	RW	0x0	tmdsclk_sense_en TMDS clock sense enable. Overrides the TMDS clock reception enable.

SUPX_DIG_ANA_CREGS_SUP_ANA_NC

Address: Operational Base + offset (0x804F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:3	RW	0x00	reserved_7_3 Reseved bits
2	RW	0x0	clk_sense_mode Clock sense mode programmability 1'b0: Normal operation 1'b1: Clock sense mode
1	RW	0x0	clk_sense_write_en Clock sense programmability enable 1'b0: Programmability disabled 1'b1: Programmability enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	clk_sense_write_clk Clock input used to latch analog clock sense mode control registers. Falling edge - latching

SUPX_DIG_RTUNE_DEBUG

Address: Operational Base + offset (0x8060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx21_go Enable RX21 tune to continue in manual tune mode when TYPE is RX21 tune. When in non RX21 manual tune mode, this bit must be 0. When in RX21 manual tune mode and after RX21 manual tune is triggered, if the read only register SUP.RTUNE_STAT.DTB_RTUNE equals to 2'b01, it is required to first release the rtune related asynchronous override on analog/digital interface then turn this bit RX21_GO from low to high to continue RX21 manual tune which also indicates that this bit needs to be low when triggering RX21 manual tune.
14:5	RW	0x000	value Value to use when triggering SET_VAL field only the 6 LSB's are used when setting RX cal values
4:3	RW	0x0	type Type of manual tuning or register read/write to execute 2'b00: ADC, or read/write rt_value 2'b01: None 2'b10: EARC tune, or read/write earc_cal_val (10 bits) 2'b11: RX21 tune, or read/write rx21_cal_val (10 bits) or resref detect (no affect when triggering SET_VAL field)
2	RW	0x0	set_val Set value Write to a 1 to manually write the register specified by the TYPE field to the value in the VALUE field
1	RW	0x0	man_tune Write to a 1 to do a manual tuning specified by TYPE field starting a manual tune while a tune is currently running can cause unpredictable results. For use only when you know what the part is doing (w.r.t. resistor tuning)
0	RW	0x0	flip_comp Invert analog comparator output

SUPX_DIG_RTUNE_CONFIG

Address: Operational Base + offset (0x8061)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use

Bit	Attr	Reset Value	Description
5:3	RW	0x2	sup_ana_term_ctrl Set the reference resistor in the analog Value Impedence (Ohms) 3'b000: 54 3'b001: 52 3'b010: 50 (default) 3'b011: 48 3'b100: 46 3'b101: 44 3'b110: 42 3'b111: 40
2	RW	0x1	earc_rx_cal_en Enable calibration of EARC and RX21 resistor
1	RW	0x0	fast_rtune Enable fast resistor tuning (simulation only)
0	RW	0x0	reserved Reserved

SUPX_DIG_RTUNE_STAT

Address: Operational Base + offset (0x8062)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RO	0x0	dtb_rtune DTB sampling for rtune
9:0	RO	0x000	stat Current value of the register specified by the DEBUG.TYPE field

SUPX_DIG_RTUNE_EARC_SET_VAL

Address: Operational Base + offset (0x8064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	earc_set_val Set value of tx-dn resistor. Writing a value to this register will set the tx-dn resistor value.

SUPX_DIG_RTUNE_RX21_SET_VAL

Address: Operational Base + offset (0x8065)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	rx21_set_val Set value of rx21 resistor. Writing a value to this register will set the tx-up resistor value.

SUPX_DIG_RTUNE_EARC_STAT

Address: Operational Base + offset (0x8067)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use

Bit	Attr	Reset Value	Description
9:0	RO	0x000	earc_stat Current value of the EARC resistor tuning register

SUPX_DIG_RTUNE_RX21_STAT
Address: Operational Base + offset (0x8068)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RO	0x000	rx21_stat Current value of the RX21 resistor tuning register

SUPX_DIG_ANA_RX_OVERLOAD_PROT_EN_OVRD_OUT
Address: Operational Base + offset (0x8069)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	ovrd_sel_det0vn Override select bit for rx_ana_det0Vn_en output
2	RW	0x0	rx_ana_det0vn_en_r Overrides for rx_ana_det0Vn_en signal
1	RW	0x0	ovrd_sel_det0vp Override select bit for rx_ana_det0Vp_en output
0	RW	0x0	rx_ana_det0vp_en_r Overrides for rx_ana_det0Vp_en signal

SUPX_DIG_ANA_TMDSCLK_EN_OVRD_OUT
Address: Operational Base + offset (0x806A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	ovrd_sel Override bit for tmdsclk_ana_en output
0	RW	0x0	tmdsclk_ana_en_r Overrides the tmdsclk_ana_en_i signal

SUPX_DIG_ANA_EARC_TERM_CODE_OVRD_OUT
Address: Operational Base + offset (0x806B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	earc_ovrd_sel Override enable for earc_term_code
6:0	RW	0x00	earc_term_code Overrides the earc_term_code signal

SUPX_DIG_ANA_RX_TERM_CODE_OVRD_OUT
Address: Operational Base + offset (0x806C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rx_ovrd_sel Override enable for rx_term_code
6:0	RW	0x00	rx_term_code Overrides the rx_term_code signal

SUPX_DIG_ANA_RTUNE_OVRD_OUT

Address: Operational Base + offset (0x806D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RW	0x0	rtune_ovrd_en Override bit for rtune (rt_ana_* and term) outputs
13:4	RW	0x000	rtune_value Overrides the rt_ana_value[9:0] signal
3	RW	0x0	rtune_en Overrides the rt_ana_en signal
2:1	RW	0x0	rtune_mode Overrides the rt_ana_mode[1:0] signal
0	RW	0x0	rtune_comp_rst Overrides the rt_ana_comp_rst signal

SUPX_DIG_ANA_STAT

Address: Operational Base + offset (0x806E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rt_ana_comp_result Value from ANA for rt_ana_comp_result

SUPX_DIG_ANA_ANA_OVRD_OUT

Address: Operational Base + offset (0x806F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_vreg_fast_start Overrides the signal rx_ana_vreg_fast_start
4	RW	0x0	ana_async_rst_ovrd_en Override enable for ana_async_rst
3	RW	0x0	ana_async_rst Override value for reset register for analog latches
2	RW	0x0	bg_ovrd_en Override bit for bandgap outputs
1	RW	0x0	bg_en Overrides the bg_ana_en signal
0	RW	0x0	bg_fast_start Overrides the bg_ana_fast_start signal

LANEX_DIG_ASIC_LANE_OVRD_IN

Address: Operational Base + offset (0x9000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_loopback_clk_en Loopback clock enable. When enabled the VCO clock of current lane is sent to the adjacent lane for TX BIST operation
1	RW	0x0	Reserve_1 Reserve_1
0	RW	0x0	Reserve_0 Reserve_0

LANEX_DIG_ASIC_RX_ASIC_LOS

Address: Operational Base + offset (0x9001)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	los_en Value from asic for rx_los_en
14	RO	0x0	los_clk_en Value from asic for rx_los_clk_en
13:4	RO	0x000	los_timer_thresh Value from asic for rx_los_timer_thresh1
3:1	RO	0x0	los_threshold Value from asic for rx_los_threshold
0	RO	0x0	los Value of rx_los towards asic

LANEX_DIG_ASIC_LOS_OVRD_IN

Address: Operational Base + offset (0x9002)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9	RW	0x0	rx_los_ovrd Override enable for rx_los
8	RW	0x0	rx_los_r Override value for rx_los
7	RW	0x0	rx_los_threshold_ovrd Override enable for rx_los_threshold
6:4	RW	0x1	rx_los_threshold_r Override value for rx_los_threshold
3	RW	0x0	rx_los_clk_en_ovrd Override enable for rx_los_clk_en
2	RW	0x0	rx_los_clk_en_r Override value for rx_los_clk_en
1	RW	0x0	rx_los_en_ovrd Override enable for rx_los_en
0	RW	0x0	rx_los_en_r Override value for rx_los_en

LANEX_DIG_ASIC_LOS_OVRD_IN_1

Address: Operational Base + offset (0x9003)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RW	0x0	rx_los_timer_thresh_ovrd Override enable for rx_los_timer_thresh1
9:0	RW	0x05a	rx_los_timer_thresh_r Override value for rx_los_timer_thresh1

LANEX_DIG_ASIC_CDR_CONTROL_OVRD_IN
Address: Operational Base + offset (0x9006)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:1	RW	0x0	cdr_setting_sel Qverride values for CDR setting bits which select the CDR gain values
0	RW	0x0	cdr_setting_sel_ovrd_en Qverride enable for cdr_setting_sel signal

LANEX_DIG_ASIC_RX_OVRD_IN_0
Address: Operational Base + offset (0x9007)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:13	RW	0x0	rate_3_2 Override value for rx_rate[3:2]
12	RW	0x0	width_ovrd_en Enable override for rx_width
11:10	RW	0x0	width Override value for rx_width
9	RW	0x0	rate_ovrd_en Enable override value for rx_rate[1:0]
8:7	RW	0x0	rate_1_0 Override value for rx_rate
6	RW	0x0	pstate_ovrd_en Enable override value for rx_pstate
5:4	RW	0x0	pstate Override value for rx_pstate
3	RW	0x0	data_en_ovrd_en Enable override value for rx_data_en
2	RW	0x0	data_en Override value for rx_data_en
1	RW	0x0	req_ovrd_en Enable override value for rx_req
0	RW	0x0	req Override value for rx_req

LANEX_DIG_ASIC_RX_OVRD_IN_1
Address: Operational Base + offset (0x9008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use

Bit	Attr	Reset Value	Description
12:10	RW	0x0	rx_clk_x2_en Override value for rx_clk_x2_en[2:0]
9	RW	0x0	rx_cdr_vco_highfreq Override value for rx_cdr_vco_highfreq
8	RW	0x0	rx_ref_ld_val_6 Override value for rx_ref_ld_val[6]
7	RW	0x0	en Enable override values for all inputs controlled by this register
6	RW	0x0	rx_cdr_vco_lowfreq Override value for rx_cdr_vco_lowfreq
5:0	RW	0x14	rx_ref_ld_val_5_0 Override value for rx_ref_ld_val[5:0]

LANEX_DIG_ASIC_RX_OVRD_IN_2
Address: Operational Base + offset (0x9009)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	en Enable override values for all inputs controlled by this register
12:0	RW	0x03e8	rx_vco_ld_val Override value for rx_vco_ld_val

LANEX_DIG_ASIC_RX_OVRD_IN_3
Address: Operational Base + offset (0x900A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x00	reserved_14_to_10 Reserved_14_to_10
9	RW	0x0	disable_ovrd_en Enable override for rx_disable
8	RW	0x0	disable Override value for rx_disable
7	RW	0x0	clk_shift_ovrd_en Enable override for rx_clk_shift
6	RW	0x0	clk_shift Override value for rx_clk_shift
5	RW	0x0	align_en_ovrd_en Enable override for rx_align_en
4	RW	0x0	align_en Override value for rx_align_en
3	RW	0x0	cdr_ssc_en_ovrd_en Enable override value for rx_cdr_ssc_en
2	RW	0x0	cdr_ssc_en Override value for rx_cdr_ssc_en
1	RW	0x0	cdr_track_en_ovrd_en Enable override value for rx_cdr_track_en
0	RW	0x0	cdr_track_en Override value for rx_cdr_track_en

LANEX_DIG_ASIC_RX_OVRD_IN_4

Address: Operational Base + offset (0x900B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	adpt_ovrd_en Enable override for rx_adpt_dfe_en and rx_adpt_afe_en
5	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
4	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
3	RW	0x0	invert_ovrd_en Enable override for rx_invert
2	RW	0x0	invert Override value for rx_invert
1	RW	0x0	lpd_ovrd_en Enable override for rx_lpd
0	RW	0x0	lpd Override value for rx_lpd

LANEX_DIG_ASIC_RX_OVRD_IN_5
Address: Operational Base + offset (0x900C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	reset_ovrd_en Enable override for rx_reset
0	RW	0x0	reset Override value for rx_reset

LANEX_DIG_ASIC_RX_OVRD_EQ_IN_0
Address: Operational Base + offset (0x900D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RW	0x06	eq_ctle_boost Override value for rx_eq_ctle_boost
10:7	RW	0x0	reserved
6:3	RW	0xf	eq_afe_gain Override value for rx_eq_afe_gain
2:0	RW	0x0	eq_att_lvl Override value for rx_eq_att_lvl

LANEX_DIG_ASIC_RX_OVRD_EQ_IN_1
Address: Operational Base + offset (0x900E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	eq_ovrd_en Enable override value for rx_eq_* inputs
14:7	RW	0x80	eq_dfe_tap1 Override value for rx_eq_dfe_tap1
6:0	RW	0x40	eq_dfe_tap2 Override value for rx_eq_dfe_tap2

LANEX_DIG_ASIC_RX_OVRD_OUT_0

Address: Operational Base + offset (0x900F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	ana_ovl_det_0v_en Enable override for rx_ana_ovl_det_0v_i
7	RW	0x0	ana_ovl_det_0v Override value for rx_ana_ovl_det_0v_i
6	RW	0x0	adapt_sts_ovrd_en Enable override for rx_adapt_sts
5:4	RW	0x0	adapt_sts Override value for rx_adapt_sts
3	RW	0x0	rsv_0 Reserve_0
2	RW	0x0	rsv_1 Reserve_1
1	RW	0x0	ack_ovrd_en Enable override for rx_ack
0	RW	0x0	ack Override value for rx_ack

LANEX_DIG_ASIC_RX_ASIC_IN_0

Address: Operational Base + offset (0x9015)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_track_en Value from ASIC for rx_cdr_track_en
13	RO	0x0	adapt_dfe_en Value from ASIC for rx_adapt_dfe_en
12	RO	0x0	adapt_afe_en Value from ASIC for rx_adapt_afe_en
11	RO	0x0	reserved
10:9	RO	0x0	width Value from ASIC for rx_width
8:7	RO	0x0	rate_1_0 Value from ASIC for rx_rate[1:0]
6:5	RO	0x0	pstate Value from ASIC for rx_pstate
4	RO	0x0	lpd Value from ASIC for rx_lpd
3	RO	0x0	req Value from ASIC for rx_req
2	RO	0x0	data_en Value from ASIC for rx_data_en
1	RO	0x0	invert Value from ASIC for rx_invert
0	RO	0x0	reset Value from ASIC for rx_reset

LANEX_DIG_ASIC_RX_ASIC_IN_1

Address: Operational Base + offset (0x9016)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:8	RO	0x0	rate_3_2 Value from ASIC for rx_rate[3:2]
7	RO	0x0	reserved_7 Reserved_7
6:4	RO	0x0	reserved_6_to_4 Reserved_6_to_4
3	RO	0x0	disable Value from ASIC for rx_disable
2	RO	0x0	clk_shift Value from ASIC for rx_clk_shift
1	RO	0x0	align_en Value from ASIC for rx_align_en
0	RO	0x0	cdr_ssc_en Value from ASIC for rx_cdr_ssc_en

LANEX_DIG_ASIC_RX_EQ_ASIC_IN_0
Address: Operational Base + offset (0x9017)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
10:9	RO	0x0	rx_ana_afe_rate Value from ASIC for rx_ana_afe_rate
8:7	RO	0x0	rx_ana_afe_ctle_pole Value from ASIC for rx_ana_afe_ctle_pole
6:3	RO	0x0	eq_afe_gain Value from ASIC for rx_eq_afe_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

LANEX_DIG_ASIC_RX_EQ_ASIC_IN_1
Address: Operational Base + offset (0x9018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:7	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1
6:0	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2

LANEX_DIG_ASIC_RX_CDR_VCO_ASIC_IN_0
Address: Operational Base + offset (0x9019)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RO	0x0	rx_clk_x2_en Value from ASIC for rx_clk_x2_en[2:0]
8	RO	0x0	rx_cdr_vco_highfreq Value from ASIC for rx_cdr_vco_highfreq

Bit	Attr	Reset Value	Description
7:1	RO	0x00	rx_ref_ld_val Value from ASIC for rx_ref_ld_val
0	RO	0x0	rx_cdr_vco_lowfreq Value from ASIC for rx_cdr_vco_lowfreq

LANEX_DIG_ASIC_RX_CDR_VCO_ASIC_IN_1

Address: Operational Base + offset (0x901A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_vco_ld_val Value from ASIC for rx_vco_ld_val

LANEX_DIG_ASIC_RX_ASIC_OUT_0

Address: Operational Base + offset (0x901B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:3	RO	0x0	adapt_sts Value from PHY for rx_adapt_sts
2	RO	0x0	valid Value from PHY for rx_valid
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	ack Value from PHY for rx_ack

LANEX_DIG_LBERT_CTL

Address: Operational Base + offset (0x9020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:5	RW	0x000	pat0 Pattern for modes 3-5
4	RW	0x0	trigger_err Insert a single error into a LSB any write of a 1 to this bit will insert an error

Bit	Attr	Reset Value	Description
3:0	RW	0x0	mode Pattern to generate when changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: Fixed word (PAT0) 4'b1010: DC balanced word (PAT0, ~PAT0) 4'b1011: Fixed pattern: (000, PAT0, 3ff, ~PAT0) others: Reserved

LANEX_DIG_RX_CDR_CDR_CTL_0
Address: Operational Base + offset (0x9024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:7	RW	0x0	dtb_sel Select to drive various signals onto the dtb 4'b0000: Disabled 4'b0001: Rx_pr_stable, rx_afe_stable from rx_ana_ctl 4'b0010: Com_good, com_bad from rx_align 4'b0011: Shift_in_prog, ana_odd_data from rx_align 4'b0100: 2 MSB's of XAUI align FSM state 4'b0101: 2 LSB's of XAUI align FSM state 4'b0110: Error_high, low from lbert_pm 4'b0111: Ana_los, los_filter from los block 4'b1000: Eios_state[0], eios_det from los block 4'b1001: Cdr_valid, MSB of FSM state from cdr_ctl 4'b1010: 2 LSB's of FSM state from cdr_ctl 4'b1011: Rx_dig_rst, rx_dig_en 4'b1100: Rx_ana_word_clk_i, rx_ana_dword_clk_i 4'b1101: Lbert_pg strobe others: Reserved
6	RW	0x0	always_realign Realign on any misaligned comma
5	RW	0x0	phdet_en_pr_mode Enable partial response phase detector mode
4	RW	0x0	phdet_pol Reverse polarity of phase error
3:2	RW	0x3	phdet_edge Edges to use for phase detection. 2'b00: Ignore all edges 2'b01: Use rising edges only 2'b10: Use both edges 2'b11: Use falling edges only
1:0	RW	0x3	phdet_en Enable phase detector. Top bit is odd slicers, bottom is even

LANEX_DIG_RX_CDR_CDR_CTL_1
Address: Operational Base + offset (0x9025)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RW	0x1c	ssc_off_cnt1 When SSC mode is disabled, the 12-bit word count in gain stage 1 is: (SSC_OFF_CNT1 * 4) in 20b mode (SSC_OFF_CNT1 * 5) in 16b mode
9:0	RW	0x039	ssc_off_cnt0 When SSC mode is disabled, the 12-bit word count in gain stage 0 is: (SSC_OFF_CNT0 * 4) in 20b mode (SSC_OFF_CNT0 * 5) in 16b mode

LANEX_DIG_RX_CDR_CDR_CTL_2
Address: Operational Base + offset (0x9026)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RW	0x25	ssc_on_cnt1 When SSC mode is enabled, the 12-bit word count in gain stage 1 is: (SSC_ON_CNT1 * 8) in 20b mode (SSC_ON_CNT1 * 10) in 16b mode
8:0	RW	0x0bb	ssc_on_cnt0 When SSC mode is enabled, the 12-bit word count in gain stage 0 is: (SSC_ON_CNT0 * 8) in 20b mode (SSC_ON_CNT0 * 10) in 16b mode

LANEX_DIG_RX_CDR_CDR_CTL_3
Address: Operational Base + offset (0x9027)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:10	RW	0x2	ssc_on_phug1 When SSC mode is enabled, the phug value in gain stage 1 is SSC_ON_PHUG1
9:6	RW	0x6	ssc_on_phug0 When SSC mode is enabled, the phug value in gain stage 0 is SSC_ON_PHUG0
5:3	RW	0x3	ssc_on_frug1 When SSC mode is enabled, the frug value in gain stage 1 is SSC_ON_FRUG1
2:0	RW	0x3	ssc_on_frug0 When SSC mode is enabled, the frug value in gain stage 0 is SSC_ON_FRUG0

LANEX_DIG_RX_CDR_CDR_CTL_4
Address: Operational Base + offset (0x9028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use

Bit	Attr	Reset Value	Description
10:8	RW	0x0	frug_ovrd_value Override value for frug (frequency update gain) 8'b000: 0 8'b001: 1/16 LSB/update 8'b010: 1/8 LSB/update 8'b011: 1/4 LSB/update 8'b100: 1/2 LSB/update 8'b101: 1 LSB/update 8'b110: 2 LSB/update 8'b111: 4 LSB/update
7:4	RW	0x0	phug_ovrd_value Override value for phug (phase update gain) : 4'b0000: 0 4'b0001: 1000 ppm 4'b0010: 2000 ppm 4'b0011: 3000 ppm 4'b0100: 4000 ppm 4'b0101: 5000 ppm 4'b0110: 6000 ppm 4'b0111: 7000 ppm 4'b1000: 8000 ppm 4'b1001: 9000 ppm 4'b1010: 10000 ppm 4'b1011: 11000 ppm 4'b1100: 12000 ppm 4'b1101: 13000 ppm 4'b1110: 14000 ppm 4'b1111: 15000 ppm
3	RW	0x0	ovrd_dpll_gain Override phug and frug values
2:0	RW	0x3	ssc_off_frug0 When SSC mode is disabled, the frug value in gain stage 0 is SSC_OFF_FRUG0

LANEX_DIG_RX_CDR_CDR_CTL_5

Address: Operational Base + offset (0x9029)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs3_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS3_FRUG1
8:6	RW	0x1	ssc_off_lbrs2_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS2_FRUG1
5:3	RW	0x1	ssc_off_lbrs1_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS1_FRUG1
2:0	RW	0x1	ssc_off_lbrs0_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS0_FRUG1

LANEX_DIG_RX_CDR_CDR_CTL_6

Address: Operational Base + offset (0x902A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:9	RW	0x3	ssc_off_lbrs7_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS7_FRUG1
8:6	RW	0x3	ssc_off_lbrs6_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS6_FRUG1
5:3	RW	0x3	ssc_off_lbrs5_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS5_FRUG1
2:0	RW	0x3	ssc_off_lbrs4_frug1 When SSC mode is disabled, the frug value in gain stage 1 is SSC_OFF_LBRS4_FRUG1

LANEX_DIG_RX_CDR_CDR_CTL_7

Address: Operational Base + offset (0x902B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x8	ssc_off_lbrs3_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS3_PHUG0
11:8	RW	0x7	ssc_off_lbrs2_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS2_PHUG0
7:4	RW	0x6	ssc_off_lbrs1_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS1_PHUG0
3:0	RW	0x6	ssc_off_lbrs0_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS0_PHUG0

LANEX_DIG_RX_CDR_CDR_CTL_8

Address: Operational Base + offset (0x902C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS7_PHUG0
11:8	RW	0xc	ssc_off_lbrs6_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS6_PHUG0
7:4	RW	0xc	ssc_off_lbrs5_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS5_PHUG0
3:0	RW	0xa	ssc_off_lbrs4_phug0 When SSC mode is disabled, the phug value in gain stage 0 is SSC_OFF_LBRS4_PHUG0

LANEX_DIG_RX_CDR_CDR_CTL_9

Address: Operational Base + offset (0x902D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RW	0x6	ssc_off_lbrs3_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS3_PHUG1
11:8	RW	0x4	ssc_off_lbrs2_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS2_PHUG1
7:4	RW	0x3	ssc_off_lbrs1_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS1_PHUG1
3:0	RW	0x2	ssc_off_lbrs0_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS0_PHUG1

LANEX_DIG_RX_CDR_CDR_CTL_10
Address: Operational Base + offset (0x902E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0xe	ssc_off_lbrs7_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS7_PHUG1
11:8	RW	0xc	ssc_off_lbrs6_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS6_PHUG1
7:4	RW	0xa	ssc_off_lbrs5_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS5_PHUG1
3:0	RW	0x8	ssc_off_lbrs4_phug1 When SSC mode is disabled, the phug value in gain stage 1 is SSC_OFF_LBRS4_PHUG1

LANEX_DIG_RX_CDR_STAT
Address: Operational Base + offset (0x902F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:4	RO	0x0	frug_value Notes: Current value for dpll_frug[2:0]
3:0	RO	0x0	phug_value Notes: Current value for dpll_phug[3:0]

LANEX_DIG_RX_PWRCTL_RX_PSTATE_P0
Address: Operational Base + offset (0x9040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x1	rx_p0_dig_clk_en Enable/Disable RX digital clocks in P0
10	RW	0x1	rx_p0_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0, if RX_P0_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored

Bit	Attr	Reset Value	Description
9	RW	0x0	rx_p0_vco_cal_rst Enable/Disable resetting the RX VCO in P0
8	RW	0x0	rx_p0_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0
7	RW	0x1	rx_p0_ana_cdr_en Value of RX ana cdr_en in P0
6	RW	0x1	rx_p0_ana_deser_en Value of RX ana deserial_en in P0
5	RW	0x1	rx_p0_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0
4	RW	0x1	rx_p0_ana_clk_en Value of RX ana clk_en in P0
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0
1	RW	0x1	rx_p0_ana_afe_en Value of RX ana afe_en in P0
0	RW	0x1	reserved_0 Reserved_0

LANEX_DIG_RX_PWRCTL_RX_PSTATE_P0S

Address: Operational Base + offset (0x9041)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p0s_dig_clk_en Enable/Disable RX digital clocks in P0S
10	RW	0x1	rx_p0s_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P0S, if RX_P0S_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x0	rx_p0s_vco_cal_rst Enable/Disable resetting the RX VCO in P0S
8	RW	0x0	rx_p0s_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P0S
7	RW	0x0	rx_p0s_ana_cdr_en Value of RX ana cdr_en in P0S
6	RW	0x0	rx_p0s_ana_deser_en Value of RX ana deserial_en in P0S
5	RW	0x0	rx_p0s_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P0S
4	RW	0x0	rx_p0s_ana_clk_en Value of RX ana clk_en in P0S
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p0s_ana_clk_vreg_en Value of RX ana clk_vreg_en in P0S
1	RW	0x1	rx_p0s_ana_afe_en Value of RX ana afe_en in P0S
0	RW	0x1	reserved_0 Reserved_0

LANEX_DIG_RX_PWRCTL_RX_PSTATE_P1

Address: Operational Base + offset (0x9042)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p1_dig_clk_en Enable/Disable RX digital clocks in P1
10	RW	0x0	rx_p1_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P1, if RX_P1_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p1_vco_cal_rst Enable/Disable resetting the RX VCO in P1
8	RW	0x1	rx_p1_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P1
7	RW	0x0	rx_p1_ana_cdr_en Value of RX ana cdr_en in P1
6	RW	0x0	rx_p1_ana_deser_en Value of RX ana deserial_en in P1
5	RW	0x0	rx_p1_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P1
4	RW	0x0	rx_p1_ana_clk_en Value of RX ana clk_en in P1
3	RW	0x0	reserved Reserved
2	RW	0x1	rx_p1_ana_clk_vreg_en Value of RX ana clk_vreg_en in P1
1	RW	0x1	rx_p1_ana_afe_en Value of RX ana afe_en in P1
0	RW	0x1	reserved_0 Reserved_0

LANEX_DIG_RX_PWRCTL_RX_PSTATE_P2

Address: Operational Base + offset (0x9043)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	rx_p2_dig_clk_en Enable/Disable RX digital clocks in P2
10	RW	0x0	rx_p2_vco_contcal_en Enable/Disable continuous calibration of the RX VCO in P2, if RX_P2_DIG_CLK_EN and the top-level rx_data_en are both asserted, then continuous calibration is turned off and this value is ignored
9	RW	0x1	rx_p2_vco_cal_rst Enable/Disable resetting the RX VCO in P2
8	RW	0x1	rx_p2_vco_freq_rst Enable/Disable resetting the RX VCO frequency in P2
7	RW	0x0	rx_p2_ana_cdr_en Value of RX ana cdr_en in P2

Bit	Attr	Reset Value	Description
6	RW	0x0	rx_p2_ana_deser_en Value of RX ana deserial_en in P2
5	RW	0x0	rx_p2_ana_clk_dcc_en Value of RX ana CLK_DCC_EN in P2
4	RW	0x0	rx_p2_ana_clk_en Value of RX ana clk_en in P2
3	RW	0x0	reserved Reserved
2	RW	0x0	rx_p2_ana_clk_vreg_en Value of RX ana clk_vreg_en in P2
1	RW	0x0	rx_p2_ana_afe_en Value of RX ana afe_en in P2
0	RW	0x1	reserved_0 Reserved_0

LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_0
Address: Operational Base + offset (0x9044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x0f	rx_dpll_clock_switch_time Wait between switching rx_dpll clock from Rx_clk to ref_clk or vice-versa
4:0	RW	0x06	rx_state_3a_and_3b_time Wait between Power state 3A and 3B

LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_1
Address: Operational Base + offset (0x9045)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	fast_rx_vreg_en Enable fast RX VREG enable (simulation only)
12:7	RW	0x0d	rx_vreg_en_time Power up time (in ref_range cycles) for RX ana vreg enable (spec 500ns)
6	RW	0x0	fast_rx_afe_en Enable fast RX AFE enable (simulation only)
5:0	RW	0x1a	rx_afe_en_time Power up time (in ref_range cycles) for RX ana AFE enable (spec >=1us)

LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_2
Address: Operational Base + offset (0x9046)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	fast_rx_clk_en Enable fast RX clock enable (simulation only)

Bit	Attr	Reset Value	Description
5:0	RW	0x1a	rx_clk_en_time Power up time (in ref_range cycles) for RX ana clk (or dcc) enable (spec >1us)

LANEX_DIG_RX_PWRCTL_RX_PWRUP_TIME_3

Address: Operational Base + offset (0x9047)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	rx_deser_dis_time Power down time in (ref_range cycles) for RX ana deserial enable
13:12	RW	0x0	rx_deser_en_time Power up time (in ref_range cycles) for RX ana deserial enable
11:8	RW	0x0	rx_cdr_en_time Power up time (in ref_range cycles) for RX ana CDR (or dfe/dfe_taps) enable (spec 0ns)
7:2	RW	0x00	rsvd_3_7_2 Reserved
1:0	RW	0x0	rx_rate_time Power up time (in ref_range cycles) for RX ana rate or width change

LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_0

Address: Operational Base + offset (0x9048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RW	0x0	vcoclk_correct_update Update the vcoclk_correct
11:9	RW	0x2	int_gain_cal_bounce_cnt Number of bounces (i.e. direction changes) on the int_gain code before indicating that the RX VCO calibration is done
8:6	RW	0x0	int_gain_cal_cnt_shift Number of shifts to apply to ld_cnt inputs when performing int_gain code calibration
5	RW	0x0	int_gain_cal_fixed_cnt_en Enable a fixed count (instead of bounce count) for int_gain code calibration
4:0	RW	0x00	int_gain_cal_fixed_cnt Number of steps done during int_gain code calibration when INT_GAIN_CAL_FIXED_CNT_EN is enabled.

LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_1

Address: Operational Base + offset (0x9049)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:9	RW	0x00	dtb_sel DTB select for RX VCO dtb signals 7'h01: {chkfrq_en, ref_dig_clk} 7'h02: {rx_ana_cdr_vco_en_i, rx_ana_cdr_startup_i} 7'h04: {rx_vco_up, dpll_freq_rst} 7'h08: {rx_vco_contcal_en, rx_vco_cal_rst} 7'h10: {chkfrq_done, vcoclk_too_fast} 7'h20: {cal_dir, rx_vco_cal_done} 7'h40: {curr_state[0], rx_vco_cnt[0]} others: Reserved
8:5	RW	0x8	dpll_cal_ug DPLL calibration update on int_gain code 3'b000: 0 others: (1/16)*2^(DPLL_CAL_UG-1) LSB/update Maximum DPLL_CAL_UG=10, i.e. 32 LSB/update
4	RW	0x0	disable_int_cal_mode When asserted, then the DPLL frequency register is never modified by the RX VCO calibration FSM (even, if DPLL_CAL_UG is non-zero). In this case, the calibration will always be performed on the VCO freq_tune code. This allows disabling of integral calibration feature, and hence only using freq_tune calibration.
3	RW	0x0	rx_vco_contcal_en Override value for the continuous calibration enable from the RX PWRSM
2	RW	0x0	rx_vco_cal_rst Override value for the calibration reset from the RX PWRSM
1	RW	0x0	rx_vco_freq_rst Override value for the frequency reset from the RX PWRSM
0	RW	0x0	rx_vco_ovrd_sel Override the calibration controls from the RX PWRSM

LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_CTRL_2
Address: Operational Base + offset (0x904A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_rx_vco_cal Skip RX VCO calibration altogether
14	RW	0x0	skip_rx_vco_freq_tune_cal Skip RX VCO coarse calibration
13:10	RW	0x9	freq_tune_cal_steps Number of cal steps of freq tune
9:0	RW	0x200	freq_tune_start_val Starting value of freq tune code

LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_0
Address: Operational Base + offset (0x904B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	fast_rx_vco_wait Enable fast RX VCO power up (simulation only)
14:11	RW	0x6	rx_vco_cntr_pwrup_time Power up time (in ref_range cycles) for RX ana VCO cnter (spec >200ns)

Bit	Attr	Reset Value	Description
10:7	RW	0x6	rx_vco_update_time Settle time (in ref_range cycles) for RX ana VCO update (freq_tune or int_gain) (spec >200ns)
6:0	RW	0x19	rx_vco_startup_time Power up time (in ref_range cycles) for RX ana VCO startup (spec >1us)

LANEX_DIG_RX_VCOCAL_RX_VCO_CAL_TIME_1
Address: Operational Base + offset (0x904C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2:0	RW	0x3	rx_vco_cntr_settle_time RX VCO counter value settling time in (ref_dig_clk cycles) (spec: 3 ref_dig_clk cycle)

LANEX_DIG_RX_VCOCAL_RX_VCO_STAT_0
Address: Operational Base + offset (0x904D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	rx_ana_cdr_vco_en Current value of rx_ana_cdr_vco_en_i
12	RO	0x0	rx_ana_cdr_startup Current value of rx_ana_cdr_startup_i
11	RO	0x0	rx_ana_vco_cntr_en Current value of rx_ana_vco_cntr_en_i
10	RO	0x0	rx_ana_vco_cntr_pd Current value of rx_ana_vco_cntr_pd_i
9:0	RO	0x000	rx_ana_cdr_freq_tune Current value of rx_ana_cdr_freq_tune_i

LANEX_DIG_RX_VCOCAL_RX_VCO_STAT_1
Address: Operational Base + offset (0x904E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	dpll_freq_rst Indicates that the RX integral frequency is reset or not
7	RO	0x0	rx_vco_cal_done Indicates that the RX VCO has completed calibration
6	RO	0x0	rx_vco_contcal_en Value of the continuous calibration enable from the RX PWRSM
5	RO	0x0	rx_vco_cal_rst Value of the calibration reset from the RX PWRSM
4	RO	0x0	rx_vco_freq_rst Value of the RX VCO frequency reset from the RX PWRSM
3:0	RO	0x0	rx_vco_fsm_state Value of the RX VCO CAL FSM

LANEX_DIG_RX_VCOCAL_RX_VCO_STAT_2

Address: Operational Base + offset (0x904F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	rx_vco_up Indicates that the RX VCO is ready
14	RO	0x0	rx_vco_correct Indicates that the RX VCO clock has the correct frequency
13	RO	0x0	vcoclk_too_fast Indicates that the RX VCO clock frequency is too fast
12:0	RO	0x0000	vco_cntr_final Value of RX VCO counter when refclk counter expired

LANEX_DIG_RX_RX_ALIGN_XAUI_COMM_MASK

Address: Operational Base + offset (0x9050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x3ff	xaui_comm_mask XAUI_COMMA mask. For 10-bit COMMA set the mask to 0x3FF and for 7-bit COMMA set the mask to 0x3F8

LANEX_DIG_RX_LBERT_CTL

Address: Operational Base + offset (0x9051)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	sync Synchronize pattern matcher LFSR with incoming data A write of a one to this bit will reset the error counter and start a synchronization of the PM, there is no need to write this back to zero to run normally.
3:0	RW	0x0	mode Pattern to match When changing modes, you must change to disabled first 4'b0000: Disabled 4'b0001: LFSR31: X^31 + X^28 + 1 4'b0010: LFSR23: X^23 + X^18 + 1 4'b0011: LFSR23: X^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1 4'b0100: LFSR16: X^16 + x^5 + x^4 + x^3 + 1 4'b0101: LFSR15: X^15 + X^14 + 1 4'b0110: LFSR11: X^11 + X^9 + 1 4'b0111: LFSR9: X^9 + X^5 + 1 4'b1000: LFSR7: X^7 + X^6 + 1 4'b1001: D[n] = d[n-10] 4'b1010: D[n] = !d[n-10] 4'b1011: D[n] = !d[n-20] others: Reserved

LANEX_DIG_RX_LBERT_ERR

Address: Operational Base + offset (0x9052)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	ov14 If active, multiply count by 128. if OV14=1 and count=2^15-1, signals overflow of counter (2 reads needed to read value)
14:0	RW	0x0000	count A read of this register, or a sync of the PM resets the error count. Current error count, if OV14 field is active, then multiply count by 128 (2 reads needed to read value)

LANEX_DIG_RX_RX_LOS_LOS_0

Address: Operational Base + offset (0x9053)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	rx_los_filt_byp Bypass digital LOS filter
7:3	RW	0x0c	rx_los_t_thresh0_r LOS timer0 threshold to count presence of zeros on rx_los
2:0	RW	0x2	rx_los_wait_r Initial wait time for rx_los after rx_los_en is asserted

LANEX_DIG_RX_PWRCTL_PWR_CTRL_STATE_STATUS

Address: Operational Base + offset (0x9055)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_pwrsm_state Value for rx_pwrsm_state

LANEX_DIG_RX_DPLL_FREQ

Address: Operational Base + offset (0x905C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13:0	RW	0x2000	val Freq is 125*VAL ppm from the reference (2 reads needed to read value)

LANEX_DIG_RX_DPLL_FREQ_BOUND_0

Address: Operational Base + offset (0x905D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10:1	RW	0x264	upper_freq_bound Upper frequency bound in terms of LSBs of the integral control code
0	RW	0x0	freq_bound_en Enable the frequency bounds feature

LANEX_DIG_RX_DPLL_FREQ_BOUND_1

Address: Operational Base + offset (0x905E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x19c	lower_freq_bound Lower frequency bound in terms of LSBs of the integral control code

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_0

Address: Operational Base + offset (0x9060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	adpt_clk_div4_en Set the adaptation clock to be divided by 4 (default is div2)
14	RW	0x0	start_asm1 Start adaptation state machine #1 (VGA, CTLE, DFE, EYEH) This register-bit is self-clearing
13:10	RW	0x3	n_tgg_asm1 Number of toggle loop iterations for ASM1
9:0	RW	0x010	n_top_asm1 Number of top level loop iterations for ASM1

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_1

Address: Operational Base + offset (0x9061)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	ctle_pole_ovrd_en Override CTLE pole value (only valid, if adaptation is run)
10:8	RW	0x0	ctle_pole_ovrd_val CTLE pole override value to load at start of adaptation
7	RW	0x0	fast_afe_dfe_settle Enable fast AFE and DFE settling time (simulation only)
6:0	RW	0x09	n_wait_asm1 Number of wait cycles for adaptation SM #1

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_2

Address: Operational Base + offset (0x9062)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:5	RW	0x06	tgg_pttrn_1 Pattern for the second toggle loop error slicer is moved upward by data tap1, if this pattern is matched
4:0	RW	0x02	tgg_pttrn_0 Pattern for the first toggle loop error slicer is moved downward by data tap1, if this pattern is matched

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_3

Address: Operational Base + offset (0x9063)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	esl_twice_dsl Assert, if error slicer has twice the voltage range as the data slicer (for the same 8 bits).
14	RW	0x0	tgg_en Enable toggling of the error slicer
13	RW	0x0	eyeho_en Enable eye height measurement using odd error slicer
12	RW	0x0	eyehe_en Enable eye height measurement using even error slicer
11:7	RW	0x00	dfe_en Enable DFE adaptation for taps 5-1
6	RW	0x0	att_en Enable ATT adaptation
5	RW	0x0	vga_en Enable VGA adaptation
4:0	RW	0x00	ctle_en Enable CTLE boost adaptation, the five bits determine which correlators are used to adapt the CTLE

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_4

Address: Operational Base + offset (0x9064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	dfe2_th DFE Tap2 correlation decision threshold (2^N-1)
11:8	RW	0x0	dfe1_th DFE Tap1 correlation decision threshold (2^N-1)
7:4	RW	0x0	vga_th VGA correlation decision threshold (2^N-1). During eye height measurement, the VGA_TH is repurposed for error slicer updates.
3:0	RW	0x0	ctle_th CTLE correlation decision threshold (2^N-1)

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_5

Address: Operational Base + offset (0x9065)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	th_offset Apply an offset to the decision threshold
11:8	RW	0x0	dfe5_th DFE Tap5 correlation decision threshold (2^N-1)
7:4	RW	0x0	dfe4_th DFE Tap4 correlation decision threshold (2^N-1)
3:0	RW	0x0	dfe3_th DFE Tap3 correlation decision threshold (2^N-1)

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_6

Address: Operational Base + offset (0x9066)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RW	0x3	att_low_th ATT low threshold

Bit	Attr	Reset Value	Description
12	RW	0x1	vga_sat_cnt_sticky If deasserted, then VGA saturation counts must be consecutive to change ATT
11:9	RW	0x4	vga_sat_cnt VGA saturation count
8:6	RW	0x4	att_mu ATT gain code update gain (2^N)
5:3	RW	0x5	vga_mu VGA gain code update gain (2^N). During eye height measurement, the VGA_MU is repurposed for error slicer updates.
2:0	RW	0x3	ctle_mu CTLE boost code update gain (2^N)

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_7
Address: Operational Base + offset (0x9067)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:10	RW	0x10	vga_lev_low VGA level low saturation limit
9:5	RW	0x1a	vga_lev_high VGA level high saturation limit
4:0	RW	0x02	vga_min_sat VGA minimum saturation limit

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_8
Address: Operational Base + offset (0x9068)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:12	RW	0x4	dfe5_mu DFE tap5 code update gain (2^N)
11:9	RW	0x4	dfe4_mu DFE tap4 code update gain (2^N)
8:6	RW	0x4	dfe3_mu DFE tap3 code update gain (2^N)
5:3	RW	0x4	dfe2_mu DFE tap2 code update gain (2^N)
2:0	RW	0x5	dfe1_mu DFE tap1 code update gain (2^N)

LANEX_DIG_RX_ADPTCTL_ADPT_CFG_9
Address: Operational Base + offset (0x9069)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	err_slo_adpt_init The error odd slicer is initialized to this value at the start of a new adaptation request.
7:0	RW	0x00	err_sle_adpt_init The error even slicer is initialized to this value at the start of a new adaptation request.

LANEX_DIG_RX_ADPTCTL_RST_ADPT_CFG
Address: Operational Base + offset (0x906A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x1	rst_adpt_tap1 Reset data Tap1 when turning off DFE adaptation (taps 2-5 are always turned off when DFE adaptation is turned off)
3	RW	0x1	rst_adpt_ctle_pole Reset CTLE pole when turning off AFE adaptation
2	RW	0x1	rst_adpt_ctle_boost Reset CTLE boost when turning off AFE adaptation
1	RW	0x1	rst_adpt_vga Reset VGA when turning off AFE adaptation
0	RW	0x1	rst_adpt_att Reset ATT when turning off AFE adaptation

LANEX_DIG_RX_ADPTCTL_ATT_STATUS
Address: Operational Base + offset (0x906B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RO	0x0	asm1_don Asserts when adaptation state machine #1 is done
7:0	RO	0x00	att_adpt_code Value of ATT adaptation code

LANEX_DIG_RX_ADPTCTL_VGA_STATUS
Address: Operational Base + offset (0x906C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
9:0	RO	0x000	vga_adpt_code Value of VGA adaptation code

LANEX_DIG_RX_ADPTCTL_CTLE_STATUS
Address: Operational Base + offset (0x906D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:10	RO	0x0	ctle_pole_adpt_code Value of CTLE pole adaptation code
9:0	RO	0x000	ctle_boost_adpt_code Value of CTLE boost adaptation code

LANEX_DIG_RX_ADPTCTL_DFE_TAP1_STATUS

Address: Operational Base + offset (0x906E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
12:0	RO	0x0000	dfe_tap1_adpt_code Value of DFE tap1 adaptation code

LANEX_DIG_RX_ADPTCTL_DFE_TAP2_STATUS

Address: Operational Base + offset (0x906F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap2_adpt_code Value of DFE tap2 adaptation code

LANEX_DIG_RX_ADPTCTL_DFE_TAP3_STATUS

Address: Operational Base + offset (0x9070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap3_adpt_code Value of DFE tap3 adaptation code

LANEX_DIG_RX_ADPTCTL_DFE_TAP4_STATUS

Address: Operational Base + offset (0x9071)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap4_adpt_code Value of DFE tap4 adaptation code

LANEX_DIG_RX_ADPTCTL_DFE_TAP5_STATUS

Address: Operational Base + offset (0x9072)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12	RO	0x0	asm1_done Asserts when adaptation state machine #1 is done
11:0	RO	0x000	dfe_tap5_adpt_code Value of DFE tap5 adaptation code

LANEX_DIG_RX_ADPTCTL_DFE_DATA_EVEN_VDAC_OFST

Address: Operational Base + offset (0x9073)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_vdac_ofst Offset value for DFE data even vDAC

LANEX_DIG_RX_ADPTCTL_DFE_DATA_ODD_VDAC_OFST
Address: Operational Base + offset (0x9074)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_vdac_ofst Offset value for DFE data odd vDAC

LANEX_DIG_RX_ADPTCTL_RX_SLICER_CTRL_EVEN
Address: Operational Base + offset (0x9075)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANEX_DIG_RX_ADPTCTL_RX_SLICER_CTRL_ODD
Address: Operational Base + offset (0x9076)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

LANEX_DIG_RX_ADPTCTL_DFE_ERROR_EVEN_VDAC_OFST
Address: Operational Base + offset (0x9077)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

LANEX_DIG_RX_ADPTCTL_DFE_ERROR_ODD_VDAC_OFST
Address: Operational Base + offset (0x9078)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

LANEX_DIG_RX_ADPTCTL_ERROR_SLICER_LEVEL
Address: Operational Base + offset (0x9079)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	e_sle_lvl Even error slicer level
7:0	RO	0x00	e_slo_lvl Odd error slicer level

LANEX_DIG_RX_ADPTCTL_ADPT_RESET

Address: Operational Base + offset (0x907A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	reset_asm1 Resets adaptation state machine (ASM1) as well as the stats capture block. This is a self-clearing bit, and requires re-start of ASM1.

LANEX_DIG_RX_STAT_LD_VAL_1

Address: Operational Base + offset (0x9080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sc1_start Start sample counter #1 this is a self-clearing bit
14:0	RW	0x0040	sc1_ld_val Sample counter #1 load value

LANEX_DIG_RX_STAT_DATA_MSK

Address: Operational Base + offset (0x9081)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	data_msk_15_0 Value of data_msk_r[15:0]

LANEX_DIG_RX_STAT_MATCH_CTL0

Address: Operational Base + offset (0x9082)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	scope_dly For clock cycle delays on scope_data_rx_clk, an additional MSB is added in SCOPE_DLY_2
13:10	RW	0xf	data_msk_19_16 Value of data_msk_r[19:16]
9:5	RW	0x00	pttrn_cr1a_4_0 Value of pattern A for 1st correlator (bits 4:0)
4:0	RW	0x06	pttrn_msk_cr1a_4_0 Value of pattern A mask for 1st correlator (bits 4:0)

LANEX_DIG_RX_STAT_MATCH_CTL1

Address: Operational Base + offset (0x9083)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use

Bit	Attr	Reset Value	Description
11	RW	0x1	pttrn_cr1a_adpt_en Enable ORing of adapation pattern with pattern CR1A
10:6	RW	0x00	pttrn_cr1b_4_0 Value of pattern B for 1st correlator (bits 4:0)
5:1	RW	0x00	pttrn_msk_cr1b_4_0 Value of pattern B mask for 1st correlator (bits 4:0)
0	RW	0x0	pttrn_cr1b_en Enable pattern B matching for 1st correlator

LANEX_DIG_RX_STAT_STAT_CTL0
Address: Operational Base + offset (0x9084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	skip_en Value of skip_en_r
14	RW	0x1	sc_timer_mode Sample counter operation mode 1'b0: Counts number of matched samples 1'b1: Counts clock cycles (i.e. a timer)
13	RW	0x0	stat_rxclk_sel Select stat clock 1'b0: Ref_range_clk 1'b1: Rx_dig_clk (i.e. RX dword clk) Before changing stat_rxclk_sel_r from 1->0, the rx_dig_clk must be active (i.e. enabled)
12:10	RW	0x0	stat_src_sel Select stat source input 3'b000: {20{rx_cal_result}} 3'b001: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 3'b010: Rx_phase[39:0] 3'b011: Rx_error[39:0] 3'b100: Rx_data[39:0] 3'b101: Rx_phdir[39:0] 3'b110: 40'hFF_FFFF_FFFF others: Reserved
9:6	RW	0x0	stat_shft_sel Select stat source shift value 4'b0000: Correlate N-1 -> N+3 (use N for offset calibration) 4'b0001: Correlate N+1 -> N+5 (for taps1-5) 4'b0010: Correlate N+6 -> N+10 4'b0011: Correlate N+11 -> N+15 4'b0100: Correlate N+16 -> N+20 4'b0101: Correlate N+21 -> N+25 4'b0110: Correlate N+26 -> N+30 4'b0111: Correlate N+31 -> N+35 4'b1000: Correlate N+36 -> N+39 others: Reserved Setting 0x8 is only used in 20b mode (for checking corr on bits 36-39)
5	RW	0x0	corr_mode_en Enable correlation mode

Bit	Attr	Reset Value	Description
4:3	RW	0x0	corr_src_sel Select correlation input source 2'b00: Rx_error[39:0] 2'b01: Rx_phase[39:0] 2'b10: {{20{scope_data_rxclk_dly_s01}}, {20{scope_data_rxclk_dly}}} 2'b11: No correlation
2	RW	0x0	corr_shft_sel Select shift for phase. 1'b0: None 1'b1: >>1
1	RW	0x0	corr_shft_sel_vga Select shift for error going to VGA. 1'b0: None 1'b1: >>1
0	RW	0x0	reserved_0 Reserved bit

LANEX_DIG_RX_STAT_STAT_CTL1

Address: Operational Base + offset (0x9085)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	vld_ctl Gating configuration of stats collection 2'b00: Ignore both cdr_valid and rx_valid 2'b01: Gate stats collection with cdr_valid 2'b10: Gate stats collection with rx_valid 2'b11: Ignore both cdr_valid and rx_valid
13	RW	0x0	vld_loss_clr Clearing of stats collection upon loss of valid 1'b0: Hold sample and stat counters 1'b1: Clear sample and stat counters
12:11	RW	0x0	data_dly_sel For clock cycle delays on rx_data[19:0], an additional MSB is added in data_dly_sel_2
10	RW	0x0	stat_clk_en Clock gate enable for stat clock
9	RW	0x0	sc_pause Pause the sample counter and stat counters
8:7	RW	0x0	reserved_8_7 Reserved bits
6	RW	0x0	stat_cnt_6_en Enable for stat counter 6
5	RW	0x0	stat_cnt_5_en Enable for stat counter 5
4	RW	0x0	stat_cnt_4_en Enable for stat counter 4
3	RW	0x1	stat_cnt_3_en Enable for stat counter 3 only counter to be enabled by default, since used for offset calibration
2	RW	0x0	stat_cnt_2_en Enable for stat counter 2
1	RW	0x0	stat_cnt_1_en Enable for stat counter 1

Bit	Attr	Reset Value	Description
0	RW	0x0	stat_cnt_0_en Enable for stat counter 0

LANEX_DIG_RX_STAT_SMPL_CNT1
Address: Operational Base + offset (0x9086)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	smpl_cnt1 Current value of sample counter #1

LANEX_DIG_RX_STAT_STAT_CNT_0
Address: Operational Base + offset (0x9087)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_0 Current value of stat counter #0

LANEX_DIG_RX_STAT_STAT_CNT_1
Address: Operational Base + offset (0x9088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_1 Current value of stat counter #1

LANEX_DIG_RX_STAT_STAT_CNT_2
Address: Operational Base + offset (0x9089)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_2 Current value of stat counter #2

LANEX_DIG_RX_STAT_STAT_CNT_3
Address: Operational Base + offset (0x908A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_3 Current value of stat counter #3

LANEX_DIG_RX_STAT_STAT_CNT_4
Address: Operational Base + offset (0x908B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1

Bit	Attr	Reset Value	Description
14:0	RO	0x0000	stat_cnt_4 Current value of stat counter #4

LANEX_DIG_RX_STAT_STAT_CNT_5
Address: Operational Base + offset (0x908C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_5 Current value of stat counter #5

LANEX_DIG_RX_STAT_STAT_CNT_6
Address: Operational Base + offset (0x908D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	smpl_cnt1_done Status of sample counter #1
14:0	RO	0x0000	stat_cnt_6 Current value of stat counter #6

LANEX_DIG_RX_STAT_CAL_COMP_CLK_CTL
Address: Operational Base + offset (0x908E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RW	0x3	ref_div_cnt Ref range clock count (e.g. 5'd3 = 4 ref_range cycles)
2:0	RW	0x1	prechrge_cnt Precharge count (e.g. 5'd1 = 2 ref_range cycles)

LANEX_DIG_RX_STAT_MATCH_CTL2
Address: Operational Base + offset (0x908F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1a_19_5 Value of pattern A for 1st correlator (bits 19:5)

LANEX_DIG_RX_STAT_MATCH_CTL3
Address: Operational Base + offset (0x9090)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1a_19_5 Value of pattern A mask for 1st correlator (bits 19:5)

LANEX_DIG_RX_STAT_MATCH_CTL4
Address: Operational Base + offset (0x9091)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_cr1b_19_5 Value of pattern B for 1st correlator (bits 19:5)

LANEX_DIG_RX_STAT_MATCH_CTL5

Address: Operational Base + offset (0x9092)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	pttrn_msk_cr1b_19_5 Value of pattern B mask for 1st correlator (bits 19:5)

LANEX_DIG_RX_STAT_STAT_CTL2

Address: Operational Base + offset (0x9093)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	scope_dly_2 Additional MSB bit for SCOPE_DLY to extend the delay range to 0->7
0	RW	0x0	data_dly_sel_2 Additional MSB bit for data_dly_sel to extend the delay range to 0->7

LANEX_DIG_RX_STAT_STAT_STOP

Address: Operational Base + offset (0x9094)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	sc1_stop Stop sample counters #1 and associated stat counters. This is a self-clearing bit, and requires re-start of sample counter #1.

LANEX_DIG_ANA_TX_OVRD_OUT

Address: Operational Base + offset (0x90A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	tx_ovrd_en Enable override values for all outputs controlled by this register
0	RW	0x0	tx_ana_reset Override value for tx_ana_reset

LANEX_DIG_ANA_TX_ANA_LPBK_DFE_MODE_OUT

Address: Operational Base + offset (0x90A1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use

Bit	Attr	Reset Value	Description
0	RW	0x0	tx_ana_lpbk_dfe_mode Value for tx_ana_lpbk_dfe_mode

LANEX_DIG_ANA_RX_DIV_OVRD_OUT

Address: Operational Base + offset (0x90A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_ana_div5_en Override value for rx_ana_div5_en
0	RW	0x0	rx_ana_div13p5_en Override value for rx_ana_div13p5_en

LANEX_DIG_ANA_RX_CTL_OVRD_OUT

Address: Operational Base + offset (0x90A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_lbk_clk_en_ovrd Enable override value for rx_ana_loopback_clk_en
14	RW	0x0	rx_ana_adaptation_en_ovrd Enable override value for rx_ana_adaptation_en
13	RW	0x0	rx_ana_dfe_taps_en_ovrd Enable override value for rx_ana_dfe_taps_en
12	RW	0x0	rx_ana_div4_en_ovrd Enable override value for rx_ana_div4_en
11	RW	0x0	rx_ana_word_clk_en_ovrd Enable override value for rx_ana_word_clk_en
10	RW	0x0	rx_ana_data_rate_en_ovrd Enable override values for rx_ana_data_rate[3:0]
9	RW	0x0	rx_lbk_clk_en Override value for rx_ana_loopback_clk_en
8	RW	0x0	rx_ana_adaptation_en Override value for rx_ana_adaptation_en
7	RW	0x0	rx_ana_dfe_taps_en Override value for rx_ana_dfe_taps_en
6	RW	0x0	rx_ana_div4_en Override value for rx_ana_div4_en
5	RW	0x0	rx_ana_word_clk_en Override value for rx_ana_word_clk_en
4:1	RW	0x0	rx_ana_data_rate Override value for rx_ana_data_rate
0	RW	0x0	reserved Reserved

LANEX_DIG_ANA_RX_PWR_OVRD_OUT

Address: Operational Base + offset (0x90A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_ana_deserial_en_ovrd Enable override value for rx_ana_deserial_en

Bit	Attr	Reset Value	Description
12	RW	0x0	rx_ana_cdr_en_ovrd Enable override value for rx_ana_cdr_en
11	RW	0x0	rx_ana_clk_en_ovrd Enable override value for rx_ana_clk_en
10	RW	0x0	rx_ana_clk_dcc_en_ovrd Enable override value for rx_ana_clk_dcc_en
9	RW	0x0	rx_ana_clk_vreg_en_ovrd Enable override value for rx_ana_clk_vreg_en
8	RW	0x0	rx_ana_afe_en_ovrd Enable override value for rx_ana_afe_en
7	RW	0x0	Reserve_0 Reserve_0
6	RW	0x0	rx_ana_deserial_en Override value for rx_ana_deserial_en
5	RW	0x0	rx_ana_cdr_en Override value for rx_ana_cdr_en
4	RW	0x0	rx_ana_clk_en Override value for rx_ana_clk_en
3	RW	0x0	rx_ana_clk_dcc_en Override value for rx_ana_clk_dcc_en
2	RW	0x0	rx_ana_clk_vreg_en Override value for rx_ana_clk_vreg_en
1	RW	0x0	rx_ana_afe_en Override value for rx_ana_afe_en
0	RW	0x0	Reserve_1 Reserve_1

LANEX_DIG_ANA_RX_VCO_OVRD_OUT_0
Address: Operational Base + offset (0x90A9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_cdr_freq_tune_ovrd_en Enable override value for rx_ana_cdr_freq_tune
14	RW	0x0	rx_ana_vco_cntr_clk Override value for rx_ana_vco_cntr_clk
13	RW	0x0	rx_ana_vco_cntr_en Override value for rx_ana_vco_cntr_en
12:3	RW	0x000	rx_ana_cdr_freq_tune Override value for rx_ana_cdr_freq_tune
2	RW	0x0	rx_vco_cdr_ovrd_en Enable override values for cdr_vco_en and cdr_startup
1	RW	0x0	rx_ana_cdr_startup Override value for rx_ana_cdr_startup
0	RW	0x0	rx_ana_cdr_vco_en Override value for rx_ana_cdr_vco_en

LANEX_DIG_ANA_RX_VCO_OVRD_OUT_1
Address: Operational Base + offset (0x90AA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_cdr_vco_highfreq Override value for rx_ana_cdr_vco_highfreq

Bit	Attr	Reset Value	Description
1	RW	0x1	rx_ana_vco_cntr_pd Override value for rx_ana_vco_cntr_pd
0	RW	0x0	rx_ana_cdr_vco_lowfreq Override value for rx_ana_cdr_vco_lowfreq

LANEX_DIG_ANA_RX_VCO_OVRD_OUT_2
Address: Operational Base + offset (0x90AB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	cdr_freq_tune_clk_self_clear_disable Disable self-clearing for the rx_ana_cdr_freq_tune_clk register
0	RW	0x0	rx_ana_cdr_freq_tune_clk Override value for rx_ana_cdr_freq_tune_clk - self-clearing to generate a pulse 1 cr_clk wide

LANEX_DIG_ANA_RX_CAL
Address: Operational Base + offset (0x90AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	rx_ana_cal_comp_en Value for rx_ana_cal_comp_en
14:13	RW	0x0	rx_ana_cal_mode Value for rx_ana_cal_mode[1:0] 2'b00: Dual differential comparison ([vip2 - vim2] greater than [vip1 - vim1]) 2'b01: Differential comparison on input2 (vip2 greater than vim2) 2'b10: Single-ended comparison, negative node to negative node (vim1 greater than vim2) 2'b11: Common mode comparison (vcm2 greater than vcm1)
12	RW	0x0	rx_ana_slicer_cal_en Value for rx_ana_slicer_cal_en
11	RW	0x0	reserved Reserved
10	RW	0x0	rx_ana_cal_lpfbyp_en Value for rx_ana_cal_lpfbyp_en
9:5	RW	0x00	rx_ana_cal_muxb_sel Value for rx_ana_cal_muxb_sel[4:0]
4:0	RW	0x00	rx_ana_cal_muxa_sel Value for rx_ana_cal_muxa_sel[4:0]

LANEX_DIG_ANA_RX_DAC_CTRL
Address: Operational Base + offset (0x90AD)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	rx_ana_cal_dac_ctrl Value for rx_ana_cal_dac_ctrl[7:0]

LANEX_DIG_ANA_RX_DAC_CTRL_OVRD
Address: Operational Base + offset (0x90AE)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_cal_dac_ctrl_ovrd Override enable for cal DAC control

LANEX_DIG_ANA_RX_DAC_CTRL_SEL
Address: Operational Base + offset (0x90AF)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_ana_cal_dac_ctrl_sel Value for rx_ana_cal_dac_ctrl_sel[4:0]

LANEX_DIG_ANA_RX_AFE_ATT_VGA
Address: Operational Base + offset (0x90B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	rx_ana_afe_rate Value for rx_ana_afe_rate[1:0]
13:12	RW	0x3	rx_ana_afe_ctle_pole Value for rx_ana_afe_ctle_pole[1:0]
11	RW	0x0	rx_afe_rate_ovrd_en Override enable for rx_ana_afe_rate
10	RW	0x0	rx_ctle_pole_ovrd_en Override enable for rx_ana_ctle_pole
9	RW	0x0	rx_afe_gain_ovrd_en Override enable for rx_ana_afe_gain
8	RW	0x0	rx_afe_att_lvl_ovrd_en Override enable for rx_ana_afe_att_lvl
7	RW	0x0	rx_afe_update_ovrd_en Override enable for rx_ana_afe_update
6:3	RW	0x0	rx_ana_afe_gain Value for rx_ana_afe_gain[3:0]
2:0	RW	0x0	rx_ana_afe_att_lvl Value for rx_ana_afe_att_lvl[2:0]

LANEX_DIG_ANA_RX_AFE_CTLE
Address: Operational Base + offset (0x90B1)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_afe_ctle_boost_ovrd_en Override enable for rx_ana_afe_ctle_boost
4:0	RW	0x00	rx_ana_afe_ctle_boost Value for rx_ana_afe_ctle_boost[4:0]

LANEX_DIG_ANA_RX_SCOPE
Address: Operational Base + offset (0x90B2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved_15_14 Reserved for future use
13	RW	0x0	rx_scope_self_clear_disable Disable the self-clearing for rx_ana_scope_ph_clk register
12	RW	0x0	rx_ana_scope_clk_en Enable the scope clocks going to the scope slicer and the lane digital part
11:4	RW	0x00	rx_ana_scope_phase Sets value for rx_ana_scope_phase[7:0]
3	RW	0x0	rx_ana_scope_ph_clk Sets value for rx_ana_scope_ph_clk, This bit is self-clearing (i.e. only asserts for one cr_clk cycle)
2:1	RW	0x0	rx_ana_scope_sel Sets value for rx_ana_scope_sel 2'b00: AFE scope selected 2'b01: DFE even scope selected 2'b10: DFE odd scope selected 2'b11: DFE bypass/AFE buffer scope selected
0	RW	0x0	rx_ana_scope_en Sets value for rx_ana_scope_en

LANEX_DIG_ANA_RX_SLICER_CTRL
Address: Operational Base + offset (0x90B3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:9	RO	0x00	reserved_15_9 Reserved for future use
8	RW	0x0	rx_ana_slicer_ctrl_ovrd_en Override enable for RX ANA slicer ctrl
7:4	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

LANEX_DIG_ANA_RX_ANA_IQ_PHASE_ADJUST
Address: Operational Base + offset (0x90B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_ana_iq_phase_adjust Value for rx_ana_iq_phase_adjust[6:0]

LANEX_DIG_ANA_RX_ANA_IQ_SENSE_EN
Address: Operational Base + offset (0x90B5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_ana_iq_sense_en Value for rx_ana_iq_sense_en

LANEX_DIG_ANA_RX_ANA_CAL_DAC_CTRL_EN
Address: Operational Base + offset (0x90B6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	dac_ctrl_self_clear_disable Disable self-clearing for the rx_ana_cal_dac_ctrl_en register
0	RW	0x0	rx_ana_cal_dac_ctrl_en Value for rx_ana_cal_dac_ctrl_en, if DAC_CTRL_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANEX_DIG_ANA_RX_ANA_SIGNALS_CHANGES_ENABLE
Address: Operational Base + offset (0x90B7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	afe_update_self_clear_disable Disable self-clearing for the rx_ana_afe_update_en register
0	RW	0x0	rx_ana_afe_update_en Value for rx_ana_afe_update_en, if AFE_UPDATE_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANEX_DIG_ANA_RX_ANA_PHASE_ADJUST_CLK
Address: Operational Base + offset (0x90B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	phase_adjust_self_clear_disable Disable self-clearing for the rx_ana_iq_phase_adjust_clk register
0	RW	0x0	rx_ana_iq_phase_adjust_clk Value for rx_ana_iq_phase_adjust_clk, if PHASE_ADJUST_SELF_CLEAR_DISABLE=0, then this bit is self-clearing (i.e. only asserts for one cr_clk cycle)

LANEX_DIG_ANA_STATUS_0
Address: Operational Base + offset (0x90B9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RO	0x0	rx_ana_scope_data Value from ANA for rx_ana_scope_data
2	RO	0x0	rx_ana_cal_result Value from ANA for rx_ana_cal_result
1	RO	0x0	rsv_0 Reserve_0
0	RO	0x0	tx_ana_loopback_en Value of tx_ana_loopback_en

LANEX_DIG_ANA_STATUS_1
Address: Operational Base + offset (0x90BA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RO	0x0000	rx_ana_vco_cntr Value from ANA for rx_ana_vco_cntr

LANEX_DIG_ANA_STATUS_LOS
Address: Operational Base + offset (0x90BB)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5:3	RO	0x0	rx_ana_los_threshold Value to ANA for rx_ana_los_threshold
2	RO	0x0	rx_ana_los_en Value to ANA for rx_ana_los_en
1	RO	0x0	rx_ana_los_clk_en Value to ANA for rx_ana_los_clk_en
0	RO	0x0	rx_ana_los Value from ANA for rx_ana_los

LANEX_DIG_ANA_CREGS_TX_ANA_ATB_REG
Address: Operational Base + offset (0x90C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:3	RW	0x0	tx_ana_nc Reserved bit
2:1	RW	0x0	tx_ana_meas_atb BIST TX ATB measurement control
0	RW	0x0	tx_ana_meas_atb_en BIST TX ATB measurement enable

LANEX_DIG_ANA_CREGS_RX_ANA_EQ_CTRL
Address: Operational Base + offset (0x90C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x1	rx_ana_phdet_odd DFE sample control
4	RW	0x1	rx_ana_phdet_even DFE sample control
3:2	RW	0x1	rx_ana_ctle_offset_cal_enb EQ offset calibration enable
1:0	RW	0x0	rx_ana_afe_bias_mt EQ bias control

LANEX_DIG_ANA_CREGS_RX_ANA_VCO_CTRL
Address: Operational Base + offset (0x90C5)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x1	rx_ana_cdr_vco_temp_comp_en VCO temperature compensation enable
1:0	RW	0x0	rx_ana_cdr_vco_startup_code VCO startup code

LANEX_DIG_ANA_CREGS_RX_ANA_VREG_CTRL
Address: Operational Base + offset (0x90C6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:6	RO	0x000	reserved_15_6 Reserved for future use
5	RW	0x0	rx_ana_vreg_ovrd_clk_vref VREG clk override reference voltage
4	RW	0x0	rx_ana_vreg_ovrd_vco_vref VREG VCO override reference voltage
3	RW	0x0	rx_ana_vreg_ovrd_vro_vref VREG VRO override reference voltage
2	RW	0x0	rx_ana_vreg_ovrd_cp_vref VREG charge-pump override reference voltage
1:0	RW	0x1	rx_ana_vreg_ring_ctrl VREG ring oscillator control

LANEX_DIG_ANA_CREGS_RX_ANA_DISCONNECT
Address: Operational Base + offset (0x90C7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:3	RO	0x0000	reserved_15_3 Reserved for future use
2	RW	0x0	rx_ana_dc_path_disconnect TBA
1	RW	0x0	rx_ana_disconnect_m TBA
0	RW	0x0	rx_ana_disconnect_p TBA

LANEX_DIG_ANA_CREGS_RX_ANA_RSRVD_CTRL
Address: Operational Base + offset (0x90C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_ana_nc Reserved bits for future use

LANEX_DIG_ANA_CREGS_RX_ANA_ATB_CTRL1
Address: Operational Base + offset (0x90C9)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RW	0x0000	rx_meas_atb_14_0 Reserved
0	RW	0x0	rx_meas_atb_en Reserved

LANEX_DIG_ANA_CREGS_RX_ANA_ATB_CTRL2
Address: Operational Base + offset (0x90CA)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14:0	RW	0x0000	rx_meas_atb_29_15 Reserved

RAWLANEX_DIG_PCS_XF_RX_OVRD_OUT_2
Address: Operational Base + offset (0xA003)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_valid_ovrd_en Enable override for rx_valid
0	RW	0x0	rx_valid Override value for rx_valid

RAWLANEX_DIG_PCS_XF_RX_PCS_IN_5
Address: Operational Base + offset (0xA004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_valid Value from PCS for rx_valid_i

RAWLANEX_DIG_PCS_XF_RX_OVRD_IN
Address: Operational Base + offset (0xA005)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11	RW	0x0	adapt_dfe_en Override value for rx_adapt_dfe_en
10	RW	0x0	adapt_afe_en Override value for rx_adapt_afe_en
9	RW	0x1	ovrd_en Enable override values for all fields in this register
8	RW	0x0	lpd Override value for rx_lpd
7:6	RW	0x0	pstate Override value for rx_pstate
5:4	RW	0x0	reserved Reserved
3:0	RW	0x0	rate Override value for rx_rate

RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_1
Address: Operational Base + offset (0xA006)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	req_ovrd_en Override enable for rx_req
2	RW	0x1	req_ovrd_val Override value for rx_req
1	RW	0x1	reset_ovrd_en Override enable for rx_reset
0	RW	0x1	reset_ovrd_val Override value for rx_reset

RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_2
Address: Operational Base + offset (0xA007)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	vco_val_ovrd_en Enable override for VCO controls
14	RW	0x0	vco_highfreq_val_ovrd Override value for rx_cdr_vco_highfreq
13	RW	0x0	vco_lowfreq_val_ovrd Override value for rx_cdr_vco_lowfreq
12:0	RW	0x0000	vco_ld_val_ovrd Override value for rx_vco_ld_val

RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_3
Address: Operational Base + offset (0xA008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	cont_ovrd_en Enable override values for rx_adapt_cont and rx_offcan_cont
3	RW	0x0	offcan_cont Override value for rx_offcan_cont
2	RW	0x0	adapt_cont Override value for rx_adapt_cont
1	RW	0x0	adapt_req_ovrd_en Enable override values for rx_adapt_req
0	RW	0x0	adapt_req Override value for rx_adapt_req

RAWLANEX_DIG_PCS_XF_RX_PCS_IN
Address: Operational Base + offset (0xA009)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reset Value from PCS for rx_reset
14	RO	0x0	offcan_cont Value from PCS for rx_offcan_cont
13	RO	0x0	adapt_cont Value from PCS for rx_adapt_cont
12	RO	0x0	adapt_req Value from PCS for rx_adapt_req

Bit	Attr	Reset Value	Description
11	RO	0x0	adapt_dfe_en Value from PCS for rx_adapt_dfe_en
10	RO	0x0	adapt_afe_en Value from PCS for rx_adapt_afe_en
9	RO	0x0	lpd Value from PCS for rx_lpd
8:7	RO	0x0	pstate Value from PCS for rx_pstate
6:5	RO	0x0	reserved_r_1 Reserved
4:1	RO	0x0	rate Value from PCS for rx_rate
0	RO	0x0	req Value from PCS for rx_req

RAWLANEX_DIG_PCS_XF_RX_PCS_IN_1
Address: Operational Base + offset (0xA00A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RO	0x00	ref_ld_val Value from PCS for rx_ref_ld_val

RAWLANEX_DIG_PCS_XF_RX_PCS_IN_2
Address: Operational Base + offset (0xA00B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RO	0x0	cdr_vco_highfreq Value from PCS for rx_cdr_vco_highfreq
13	RO	0x0	cdr_vco_lowfreq Value from PCS for rx_cdr_vco_lowfreq
12:0	RO	0x0000	vco_ld_val Value from PCS for rx_vco_ld_val

RAWLANEX_DIG_PCS_XF_RX_PCS_IN_3
Address: Operational Base + offset (0xA00C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	eq_afe_rate Value from ASIC for rx_eq_afe_rate
13:12	RO	0x0	eq_ctle_pole Value from ASIC for rx_eq_ctle_pole
11:7	RO	0x00	eq_ctle_boost Value from ASIC for rx_eq_ctle_boost
6:3	RO	0x0	eq_vga1_gain Value from ASIC for rx_eq_vga1_gain
2:0	RO	0x0	eq_att_lvl Value from ASIC for rx_eq_att_lvl

RAWLANEX_DIG_PCS_XF_RX_PCS_IN_4
Address: Operational Base + offset (0xA00D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	eq_dfe_tap2 Value from ASIC for rx_eq_dfe_tap2
7:0	RO	0x00	eq_dfe_tap1 Value from ASIC for rx_eq_dfe_tap1

RAWLANEX_DIG_PCS_XF_RX_OVRD_OUT
Address: Operational Base + offset (0xA00E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x1	en_ctl Enable override values for all control outputs of this register
0	RW	0x1	ack Override value for rx_ack

RAWLANEX_DIG_PCS_XF_RX_PCS_OUT
Address: Operational Base + offset (0xA00F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANEX_DIG_PCS_XF_RX_ADAPT_ACK
Address: Operational Base + offset (0xA010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:10	RW	0x0	rx_eq_afe_rate_ovrd_val Override val for rx_eq_afe_rate[1:0]
9:8	RW	0x0	rx_eq_ctle_pole_ovrd_val Override val for rx_eq_ctle_pole[1:0]
7	RW	0x0	rx_eq_att_ovrd_en Individual override enable for ATT
6	RW	0x0	rx_eq_vga1_gain_ovrd_en Individual override enable for gain
5	RW	0x0	rx_eq_ctle_boost_ovrd_en Individual override enable for boost
4	RW	0x0	rx_eq_ctle_pole_ovrd_en Individual override enable for pole
3	RW	0x0	rx_eq_afe_rate_ovrd_en Individual override enable for rate
2	RW	0x0	rx_eq_dfe_t1_ovrd_en Individual override enable for TAP1
1	RW	0x0	rx_eq_dfe_t2_ovrd_en Individual override enable for TAP2
0	RW	0x0	rx_adapt_ack RX adaptation Acknowledge

RAWLANEX_DIG_PCS_XF_RX_ADAPT_FOM

Address: Operational Base + offset (0xA011)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom RX adaptation figure of merit

RAWLANEX_DIG_PCS_XF_RX_OVRD_IN_4

Address: Operational Base + offset (0xA012)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	ref_ld_val_ovrd_en Enable override for rx_ref_ld_val
6:0	RW	0x00	ref_ld_val_ovrd Override value for rx_ref_ld_val

RAWLANEX_DIG_PCS_XF_RX_PCS_OUT_2

Address: Operational Base + offset (0xA013)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from raw PCS for rx_ack

RAWLANEX_DIG_PCS_XF_LANE_NUMBER

Address: Operational Base + offset (0xA015)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	lane_number Current lane number

RAWLANEX_DIG_PCS_XF_ATE_OVRD_IN

Address: Operational Base + offset (0xA018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7	RW	0x0	rx_adapt_dfe_en_ovrd_en Enable override value for rx_adapt_dfe_en input
6	RW	0x0	rx_adapt_dfe_en_ovrd_val Override value for rx_adapt_dfe_en input
5	RW	0x0	rx_adapt_afe_en_ovrd_en Enable override value for rx_adapt_afe_en input
4	RW	0x0	rx_adapt_afe_en_ovrd_val Override value for rx_adapt_afe_en input
3	RW	0x0	rx_req_ate_ovrd_en Enable override value for rx_req input
2	RW	0x0	rx_req_ate_ovrd_val Override value for top-level rx_req input

Bit	Attr	Reset Value	Description
1	RW	0x0	rx_reset_ate_ovrd_en Enable override value for rx_reset input
0	RW	0x0	rx_reset_ate_ovrd_val Override value for top-level rx_reset input

RAWLANEX_DIG_PCS_XF_RX_EQ_DELTA_IQ_OVRD_IN

Address: Operational Base + offset (0xA019)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4	RW	0x0	rx_eq_delta_iq_ovrd_en Enable override value for rx_eq_delta_iq
3:0	RW	0x0	rx_eq_delta_iq_ovrd_val Override value for rx_eq_delta_iq

RAWLANEX_DIG_PCS_XF_RX_EQ_OVRD_IN_1

Address: Operational Base + offset (0xA01D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:8	RW	0x00	rx_eq_ctle_boost_ovrd_val Override value for rx_eq_ctle_boost[4:0]
7	RW	0x0	rx_eq_ovrd_en Enable override values for all RX EQ settings
6:4	RW	0x0	rx_eq_att_lvl_ovrd_val Override value for rx_eq_att_lvl[2:0]
3:0	RW	0x0	rx_eq_afe_gain_ovrd_val Override value for rx_eq_afe_gain[3:0]

RAWLANEX_DIG_PCS_XF_RX_EQ_OVRD_IN_2

Address: Operational Base + offset (0xA01E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	rx_eq_dfe_tap2_ovrd_val Override value for rx_eq_dfe_tap2[7:0]
7:0	RW	0x00	rx_eq_dfe_tap1_ovrd_val Override value for rx_eq_dfe_tap1[7:0]

RAWLANEX_DIG_FSM_FSM_FSM_OVRD_CTL

Address: Operational Base + offset (0xA020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	reserved_15_15 Reserved for future use
14	RW	0x0	fsm_ovrd_en Enable overriding the FSM execution of commands must be asserted to use FSM_CMD_START and FSM_JMP_EN features
13	RW	0x0	fsm_cmd_start Start executing the new command, this is a self-clearing bit
12	RW	0x0	fsm_jmp_en Force the FSM to jump to FSM_JMP_ADDR in the program memory is applied when FSM_CMD_START is pulsed.

Bit	Attr	Reset Value	Description
11:0	RW	0x000	fsm_jmp_addr The jump address used when FSM_JUMP_EN=1, the address is encoded as follows: [11:8] mem_lane, [7:5] bank, [4:0] register

RAWLANEX_DIG_FSM_FSM_MEM_ADDR_MON

Address: Operational Base + offset (0xA021)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	mem_addr Current value of memory address used in lane FSM

RAWLANEX_DIG_FSM_FSM_STATUS_MON

Address: Operational Base + offset (0xA022)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:11	RO	0x00	reserved_15_11 Reserved for future use
10	RO	0x0	rdmsk_disabled Check, if read mask is currently disabled (i.e. mask is all ones)
9	RO	0x0	wrmsk_disabled Check, if write mask is currently disabled (i.e. mask is all ones)
8	RO	0x0	wait_cnt_eq0 Check, if wait counter currently equals zero
7	RO	0x0	alu_res_eq0 Check, if ALU result register currently equals zero
6	RO	0x0	alu_ovflw Current value of ALU overflow bit
5	RO	0x0	cmd_rdy New command is ready for execution (applicable when FSM_OVRD_EN=1)
4:0	RO	0x00	state Current state of lane FSM

RAWLANEX_DIG_FSM_FSM_CR_REG_OP_XTND_EN

Address: Operational Base + offset (0xA023)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	cr_reg_op_xtnd_en CR interface timing extension enable 1'b0: No timing extension 1'b1: Timing extension

RAWLANEX_DIG_FSM_FAST_RX_STARTUP_CAL

Address: Operational Base + offset (0xA024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_startup_cal Status of fast RX start-up calibration

RAWLANEX_DIG_FSM_FAST_RX_ADAPT

Address: Operational Base + offset (0xA025)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_adapt Status of fast RX adaptation

RAWLANEX_DIG_FSM_FAST_RX_AFE_CAL
Address: Operational Base + offset (0xA026)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_cal Status of fast RX AFE DAC start-up calibration

RAWLANEX_DIG_FSM_FAST_RX_DFE_CAL
Address: Operational Base + offset (0xA027)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_cal Status of fast RX DFE slicer start-up calibration

RAWLANEX_DIG_FSM_FAST_RX_BYPASS_CAL
Address: Operational Base + offset (0xA028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_bypass_cal Status of fast RX bypass slicer start-up calibration

RAWLANEX_DIG_FSM_FAST_RX_REFLVL_CAL
Address: Operational Base + offset (0xA029)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_reflvl_cal Status of fast RX reference level (100mv, 125mv, 150mv) start-up calibration

RAWLANEX_DIG_FSM_FAST_RX_IQ_CAL
Address: Operational Base + offset (0xA02A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_cal Status of fast RX IQ start-up calibration

RAWLANEX_DIG_FSM_FAST_RX_AFE_ADAPT

Address: Operational Base + offset (0xA02B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_afe_adapt Status of fast RX AFE DAC start-up adaptation

RAWLANEX_DIG_FSM_FAST_RX_DFE_ADAPT

Address: Operational Base + offset (0xA02C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_dfe_adapt Status of fast RX DFE DAC start-up adaptation

RAWLANEX_DIG_FSM_FAST_SUP

Address: Operational Base + offset (0xA02D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_sup Status of fast support block (Rtune)

RAWLANEX_DIG_FSM_FAST_RX_IQ_WALK

Address: Operational Base + offset (0xA02E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_walk Status of fast RX IQ walk start-up adaptation

RAWLANEX_DIG_FSM_FAST_RX_PWRUP

Address: Operational Base + offset (0xA02F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_pwrup Status of fast RX power-up (LOS, VREG/AFE and DCC)

RAWLANEX_DIG_FSM_FAST_RX_VCO_WAIT

Address: Operational Base + offset (0xA030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_wait Status of fast RX VCO wait times

RAWLANEX_DIG_FSM_FAST_RX_VCO_CAL

Address: Operational Base + offset (0xA031)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_vco_cal Status of fast RX VCO calibration

RAWLANEX_DIG_FSM_FAST_RX_CONT_CAL_ADAPT
Address: Operational Base + offset (0xA033)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_cal_adapt Status of fast RX continuous calibration/adaptation

RAWLANEX_DIG_FSM_FAST_RX_CONT_ADAPT
Address: Operational Base + offset (0xA034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_adapt Status of fast RX continuous adaptation

RAWLANEX_DIG_FSM_FAST_RX_CONT_DATA_CAL
Address: Operational Base + offset (0xA035)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_data_cal Status of fast RX continuous data calibration

RAWLANEX_DIG_FSM_FAST_RX_CONT_PHASE_CAL
Address: Operational Base + offset (0xA036)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_phase_cal Status of fast RX continuous phase calibration

RAWLANEX_DIG_FSM_FAST_RX_CONT_AFE_CAL
Address: Operational Base + offset (0xA037)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_cont_afe_cal Status of fast RX continuous AFE calibration

RAWLANEX_DIG_FSM_FAST_RX_ATT_VGA_ADAPT
Address: Operational Base + offset (0xA038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_0 Reserved

RAWLANEX_DIG_FSM_FAST_RX_CTLE_ADAPT
Address: Operational Base + offset (0xA039)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_1 Reserved

RAWLANEX_DIG_FSM_FAST_RX_VGA_ADAPT
Address: Operational Base + offset (0xA03A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_2 Reserved

RAWLANEX_DIG_FSM_CTLE_ALGO_TWO_PT_EXIT
Address: Operational Base + offset (0xA03B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_flags_rsvd_3 Reserved

RAWLANEX_DIG_FSM_FAST_RX_IQ_ADAPT
Address: Operational Base + offset (0xA03C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	fast_rx_iq_adapt Status of fast RX IQ adapt start-up adaptation

RAWLANEX_DIG_FSM_RX_CTLE_ALGO_EH_SEL
Address: Operational Base + offset (0xA03D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_ctle_algo_eh_sel Status of RX CTLE adapt selected algo

RAWLANEX_DIG_FSM_RX_IQ_PHASE_OFFSET
Address: Operational Base + offset (0xA03F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RO	0x0	rx_iq_phase_offset Offset value for IQ phase calculation

RAWLANEX_DIG_AON_AFE_ATT_IDAC_OFST
Address: Operational Base + offset (0xA040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_att_idac_ofst Offset value for AFE ATT iDAC

RAWLANEX_DIG_AON_AFE_CTLE_IDAC_OFST
Address: Operational Base + offset (0xA041)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_ctle_idac_ofst Offset value for AFE CTLE iDAC

RAWLANEX_DIG_AON_AFE_VGA1_IDAC_OFST
Address: Operational Base + offset (0xA042)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	afe_vga1_idac_ofst Offset value for AFE VGA1 iDAC

RAWLANEX_DIG_AON_RX_ADAPT_FOM
Address: Operational Base + offset (0xA043)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	rx_adapt_fom Adaptation figure of merit (FOM)

RAWLANEX_DIG_AON_DFE_SUMMER_ODD_IDAC_OFST
Address: Operational Base + offset (0xA044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_summer_odd_idac_ofst Offset value for DFE summer odd iDAC

RAWLANEX_DIG_AON_DFE_PHASE_EVEN_VDAC_OFST
Address: Operational Base + offset (0xA045)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_even_vdac_ofst Offset value for DFE phase even vDAC

RAWLANEX_DIG_AON_DFE_PHASE_ODD_VDAC_OFST
Address: Operational Base + offset (0xA046)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_phase_odd_vdac_ofst Offset value for DFE phase odd vDAC

RAWLANEX_DIG_AON_DFE_EVEN_REF_LVL
Address: Operational Base + offset (0xA047)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_even_ref_lvl DFE even reference level

RAWLANEX_DIG_AON_DFE_ODD_REF_LVL
Address: Operational Base + offset (0xA048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	dfe_odd_ref_lvl DFE odd reference level

RAWLANEX_DIG_AON_RX_PHSADJ_LIN
Address: Operational Base + offset (0xA049)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x07	rx_phsadj_lin Linear value for RX phase adjust

RAWLANEX_DIG_AON_RX_PHSADJ_MAP
Address: Operational Base + offset (0xA04A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RO	0x00	rx_phsadj_map Mapped value for RX phase adjust

RAWLANEX_DIG_AON_DFE_DATA_EVEN_HIGH_VDAC_OFST
Address: Operational Base + offset (0xA04B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_high_vdac_ofst Offset value for DFE data even high vDAC

RAWLANEX_DIG_AON_CDR_UNLOCKED_CNT
Address: Operational Base + offset (0xA04C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_even_low_vdac_ofst Offset value for DFE data even low vDAC

RAWLANEX_DIG_AON_DFE_DATA_ODD_HIGH_VDAC_OFST
Address: Operational Base + offset (0xA04D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_high_vdac_ofst Offset value for DFE data odd high vDAC

RAWLANEX_DIG_AON_RX_ADAPT_DONE_NEW
Address: Operational Base + offset (0xA04E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_data_odd_low_vdac_ofst Offset value for DFE data odd low vDAC

RAWLANEX_DIG_AON_DFE_BYPASS_EVEN_VDAC_OFST
Address: Operational Base + offset (0xA04F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_even_vdac_ofst Offset value for DFE bypass even vDAC

RAWLANEX_DIG_AON_DFE_BYPASS_ODD_VDAC_OFST
Address: Operational Base + offset (0xA050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_bypass_odd_vdac_ofst Offset value for DFE bypass odd vDAC

RAWLANEX_DIG_AON_DFE_ERROR_EVEN_VDAC_OFST
Address: Operational Base + offset (0xA051)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_even_vdac_ofst Offset value for DFE error even vDAC

RAWLANEX_DIG_AON_DFE_ERROR_ODD_VDAC_OFST
Address: Operational Base + offset (0xA052)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x80	dfe_error_odd_vdac_ofst Offset value for DFE error odd vDAC

RAWLANEX_DIG_AON_RX_IQ_PHASE_ADJUST
Address: Operational Base + offset (0xA053)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6:0	RW	0x07	rx_iq_phase_adjust Value for RX IQ phase adjust

RAWLANEX_DIG_AON_RX_IQ_PHASE_DELTA_OFFSET
Address: Operational Base + offset (0xA054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_iq_phase_delta_offset Value for RX IQ phase offset + delta value

RAWLANEX_DIG_AON_RX_FW_REVISION_PMA_LABEL
Address: Operational Base + offset (0xA055)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pma_label PMA label

RAWLANEX_DIG_AON_INIT_PWRUP_DONE
Address: Operational Base + offset (0xA056)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	init_pwrup_done Indicates whether initial power-up has completed or not.

RAWLANEX_DIG_AON_RX_ADPT_ATT
Address: Operational Base + offset (0xA057)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	att_adpt_val Stored RX adapted ATT value

RAWLANEX_DIG_AON_RX_ADPT_VGA
Address: Operational Base + offset (0xA058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value

RAWLANEX_DIG_AON_RX_ADPT_CTLE
Address: Operational Base + offset (0xA059)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value

RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP1
Address: Operational Base + offset (0xA05A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value

RAWLANEX_DIG_AON_RX_ADAPT_DONE
Address: Operational Base + offset (0xA05B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_done Indicates whether RX adaptation has completed or not.

RAWLANEX_DIG_AON_FAST_FLAGS
Address: Operational Base + offset (0xA05C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ctle_algo_eh_sel Decides between 1'b1 - "EYE_HEIGHT" or 1'b0 - "MIN_BOT_TOB" algorithms
14	RW	0x0	fast_rx_iq_adapt Enable fast RX IQ adapt
13	RW	0x0	fast_rx_iq_walk Enable fast RX IQ walk

Bit	Attr	Reset Value	Description
12	RW	0x0	fast_rx_vco_cal Enable fast RX VCO calibration
11	RW	0x0	fast_rx_vco_wait Enable fast RX VCO wait times
10	RW	0x0	fast_rx_pwrup Enable fast RX power-up (LOS, VREG/AFE and DCC)
9	RW	0x0	fast_sup Enable fast support block (rtune)
8	RW	0x0	fast_rx_dfe_adapt Enables fast RX DFE DAC start-up adaptation
7	RW	0x0	fast_rx_afe_adapt Enables fast RX AFE DAC start-up adaptation
6	RW	0x0	fast_rx_iq_cal Enables fast RX IQ start-up calibration
5	RW	0x0	fast_rx_reflvl_cal Enables fast RX reference level (100mv, 125mv, 150mv) start-up calibration
4	RW	0x0	fast_rx_bypass_cal Enables fast RX bypass slicer start-up calibration
3	RW	0x0	fast_rx_dfe_cal Enables fast RX DFE slicer start-up calibration
2	RW	0x0	fast_rx_afe_cal Enables fast RX AFE DAC start-up calibration
1	RW	0x0	fast_rx_adapt Enables fast RX adaptation
0	RW	0x0	fast_rx_startup_cal Enables fast RX start-up calibration

RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP2
Address: Operational Base + offset (0xA05D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value

RAWLANEX_DIG_AON_RX_ADPT_BOOST_FUNC_LOWER_LIMIT
Address: Operational Base + offset (0xA05E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_lower_limit Stored boost val cost func lower limit

RAWLANEX_DIG_AON_RX_ADPT_BOOST_FUNC_UPPER_LIMIT
Address: Operational Base + offset (0xA05F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reserved_15_8 Reserved for future use
7:0	RW	0x00	boost_func_upper_limit Stored boost val cost func upper limit

RAWLANEX_DIG_AON_RX_FW_REVISION_RAW_LABEL
Address: Operational Base + offset (0xA060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	raw_label RAW label

RAWLANEX_DIG_AON_RX_SLICER_CTRL_EVEN
Address: Operational Base + offset (0xA061)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_e Value for rx_ana_slicer_ctrl_e[3:0]

RAWLANEX_DIG_AON_FRL_MODE_INIT_ADAPT_SET_DONE
Address: Operational Base + offset (0xA062)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3:0	RW	0x7	rx_ana_slicer_ctrl_o Value for rx_ana_slicer_ctrl_o[3:0]

RAWLANEX_DIG_AON_RX_FW_REVISION_PCS_LABEL
Address: Operational Base + offset (0xA063)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	pcs_label PCS label

RAWLANEX_DIG_AON_ADPT_CTL_0
Address: Operational Base + offset (0xA064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_ADPT_CTL_1
Address: Operational Base + offset (0xA065)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_ADPT_CTL_2
Address: Operational Base + offset (0xA066)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_ADPT_CTL_3
Address: Operational Base + offset (0xA067)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_ADPT_CTL_4
Address: Operational Base + offset (0xA068)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_ADPT_CTL_5
Address: Operational Base + offset (0xA069)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_ADPT_CTL_6
Address: Operational Base + offset (0xA06A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_ADPT_CTL_7
Address: Operational Base + offset (0xA06B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	val Value of adaptation control

RAWLANEX_DIG_AON_RX_FW_REVISION_FW_LABEL
Address: Operational Base + offset (0xA06C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved
11:0	RW	0x000	fw_label FW label

RAWLANEX_DIG_AON_FAST_FLAGS_2
Address: Operational Base + offset (0xA06D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x0	reserved Reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	ctle_adapt_sts CTLE adaptation status flag
10	RW	0x0	fast_frl_adpt_byp_aft_ltp Enable fast FRL bypass after link training
9	RW	0x0	skip_ctle_bin_srch_abrt Skip CTLE binary search abort
8	RW	0x0	ctle_algo_two_pt_exit CTLE algo two point exit
7	RW	0x0	fast_rx_vga_adapt Enables fast RX VGA adaptation
6	RW	0x0	fast_rx_ctle_adapt Enables fast RX CTLE adaptation
5	RW	0x0	fast_rx_att_vga_adapt Enables fast RX ATT_VGA adaptation
4	RW	0x0	fast_rx_cont_afe_cal Enables fast RX continuous AFE calibration
3	RW	0x0	fast_rx_cont_phase_cal Enables fast RX continuous phase calibration
2	RW	0x0	fast_rx_cont_data_cal Enables fast RX continuous data calibration
1	RW	0x0	fast_rx_cont_adapt Enables fast RX continuous adaptation
0	RW	0x0	fast_rx_cont_cal_adapt Enables fast RX continuous calibration/adaptation

RAWLANEX_DIG_AON_RX_RESERVED_REG_0
Address: Operational Base + offset (0xA06E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_0 Reserved fields

RAWLANEX_DIG_AON_TXRX_OVRD_IN
Address: Operational Base + offset (0xA06F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:2	RO	0x0000	reserved_15_2 Reserved for future use
1	RW	0x0	rx_disable_ovrd_en Override enable for rx_disable
0	RW	0x0	rx_disable_ovrd_val Override value for rx_disable

RAWLANEX_DIG_AON_RX_PHSADJ_LIN_LEFT
Address: Operational Base + offset (0xA070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_left Linear value for RX phase adjust on left

RAWLANEX_DIG_AON_RX_PHSADJ_LIN_RIGHT
Address: Operational Base + offset (0xA071)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_right Linear value for RX phase adjust on right

RAWLANEX_DIG_AON_RX_PHSADJ_LIN_ADAPT

Address: Operational Base + offset (0xA072)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:5	RO	0x000	reserved_15_5 Reserved for future use
4:0	RW	0x00	rx_phsadj_lin_adapt Linear value for RX phase adjust IQ adapt value

RAWLANEX_DIG_AON_RX_RESERVED_REG_1

Address: Operational Base + offset (0xA073)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	reserved_1 Reserved fields

RAWLANEX_DIG_AON_RX_ADPT_VGA_1

Address: Operational Base + offset (0xA078)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	vga_adpt_val Stored RX adapted VGA value 1st iter

RAWLANEX_DIG_AON_RX_ADPT_CTLE_1

Address: Operational Base + offset (0xA079)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	reserved_15_10 Reserved for future use
9:0	RW	0x000	ctle_boost_adpt_val Stored RX adapted CTLE boost value 1st iter

RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP1_1

Address: Operational Base + offset (0xA07A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	reserved_15_13 Reserved for future use
12:0	RW	0x0000	dfe_tap1_adpt_val Stored RX adapted DFE TAP1 value 1st iter

RAWLANEX_DIG_AON_RX_ADPT_DFE_TAP2_1

Address: Operational Base + offset (0xA07D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved_15_12 Reserved for future use
11:0	RW	0x800	dfe_tap2_adpt_val Stored RX adapted DFE TAP2 value 1st iter

RAWLANEX_DIG_IRQ_CTL_RESET_RTN_REQ
Address: Operational Base + offset (0xA080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x1	reset_rtn_req Reset routine request

RAWLANEX_DIG_IRQ_CTL_RX_RESET_IRQ
Address: Operational Base + offset (0xA081)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_reset Rx reset interrupt

RAWLANEX_DIG_IRQ_CTL_RX_REQ_IRQ
Address: Operational Base + offset (0xA082)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_req Rx request interrupt

RAWLANEX_DIG_IRQ_CTL_RX_RATE_IRQ
Address: Operational Base + offset (0xA083)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_rate_irq Rx rate change interrupt request

RAWLANEX_DIG_IRQ_CTL_RX_PSTATE_IRQ
Address: Operational Base + offset (0xA084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_pstate_irq Rx pstate change interrupt request

RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ
Address: Operational Base + offset (0xA085)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_req_irq Rx adaptation request interrupt

RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ
Address: Operational Base + offset (0xA086)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_adapt_dis_irq Rx adaptation disable interrupt

RAWLANEX_DIG_IRQ_CTL_RX_RESET_IRQ_CLR
Address: Operational Base + offset (0xA087)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_reset_irq_clr RX reset interrupt clear (self-clearing)

RAWLANEX_DIG_IRQ_CTL_RX_REQ_IRQ_CLR
Address: Operational Base + offset (0xA088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_req_irq_clr RX request interrupt clear (self-clearing)

RAWLANEX_DIG_IRQ_CTL_RX_RATE_IRQ_CLR
Address: Operational Base + offset (0xA089)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_rate_irq_clr RX rate change interrupt clear (self-clearing)

RAWLANEX_DIG_IRQ_CTL_RX_PSTATE_IRQ_CLR
Address: Operational Base + offset (0xA08A)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_pstate_irq_clr RX pstate change interrupt clear (self-clearing)

RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_REQ_IRQ_CLR
Address: Operational Base + offset (0xA08B)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_req_irq_clr RX adaptation request interrupt clear (self-clearing)

RAWLANEX_DIG_IRQ_CTL_RX_ADAPT_DIS_IRQ_CLR
Address: Operational Base + offset (0xA08C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_adapt_dis_irq_clr RX adaptation disable interrupt clear (self-clearing)

RAWLANEX_DIG_IRQ_CTL_IRQ_MASK
Address: Operational Base + offset (0xA08D)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:7	RO	0x000	reserved_15_7 Reserved for future use
6	RW	0x0	rx_initialize_irq_msk Mask for RX initialize interrupt (0 = cannot interrupt)
5	RW	0x0	rx_reset_irq_msk Mask for RX reset interrupt (0 = cannot interrupt)
4	RW	0x0	rx_adapt_dis_irq_msk Mask for RX adaptation disable interrupt (0 = cannot interrupt)
3	RW	0x0	rx_adapt_req_irq_msk Mask for RX adaptation request interrupt (0 = cannot interrupt)
2	RW	0x0	rx_pstate_irq_msk Mask for RX pstate change interrupt (0 = cannot interrupt)
1	RW	0x0	rx_rate_irq_msk Mask for RX rate change interrupt (0 = cannot interrupt)
0	RW	0x0	rx_req_irq_msk Mask for RX request interrupt (0 = cannot interrupt)

RAWLANEX_DIG_IRQ_CTL_RX_INITIALIZE_IRQ
Address: Operational Base + offset (0xA08E)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	rx_initialize_irq Rx initialize interrupt request

RAWLANEX_DIG_IRQ_CTL_RX_INITIALIZE_IRQ_CLR
Address: Operational Base + offset (0xA08F)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RW	0x0	rx_initialize_irq_clr RX initialize interrupt clear (self-clearing)

RAWLANEX_DIG_PMA_XF_RX_OVRD_OUT

Address: Operational Base + offset (0xA0A6)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RO	0x000	reserved_15_4 Reserved for future use
3	RW	0x0	rx_reset_ovrd_en Override enable for rx_reset
2	RW	0x0	rx_reset_ovrd_val Override value for rx_reset
1	RW	0x0	rx_req_ovrd_en Override enable for rx_req
0	RW	0x0	rx_req_ovrd_val Override value for rx_req

RAWLANEX_DIG_PMA_XF_RX_PMA_IN
Address: Operational Base + offset (0xA0A7)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	ack Value from PMA for rx_ack

RAWLANEX_DIG_RX_CTL_OFFCAN_CONT_STATUS
Address: Operational Base + offset (0xA0E3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous offset cancellation

RAWLANEX_DIG_RX_CTL_ADAPT_CONT_STATUS
Address: Operational Base + offset (0xA0E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:1	RO	0x0000	reserved_15_1 Reserved for future use
0	RO	0x0	enable Enable status for RX continuous adaptation

28.5 Interface Description

Table 28-1 HDMIRX PHY interface description

Module Pin	Direction	Pad Name	IOMUX Setting
IO_HDMIRXPHY_RX0_M	I/O	HDMI_RX_D0N	NS
IO_HDMIRXPHY_RX0_P	I/O	HDMI_RX_D0P	NS
IO_HDMIRXPHY_RX1_M	I/O	HDMI_RX_D1N	NS
IO_HDMIRXPHY_RX1_P	I/O	HDMI_RX_D1P	NS
IO_HDMIRXPHY_RX2_M	I/O	HDMI_RX_D2N	NS
IO_HDMIRXPHY_RX2_P	I/O	HDMI_RX_D2P	NS
IO_HDMIRXPHY_RX3_M	I/O	HDMI_RX_CLKN	NS
IO_HDMIRXPHY_RX3_P	I/O	HDMI_RX_CLKP	NS
IO_HDMIRXPHY_RESREF	I/O	HDMI_RX_REXT	NS

Notes: I=input, O=output, I/O=input/output, bidirectional

28.6 Application Notes

28.6.1 HDMIRX PHY Application

28.6.1.1 HDMIRX PHY Power Up sequence

The figure below shows the HDMIRX PHY power up reset sequence along with the power supply ramp-up.

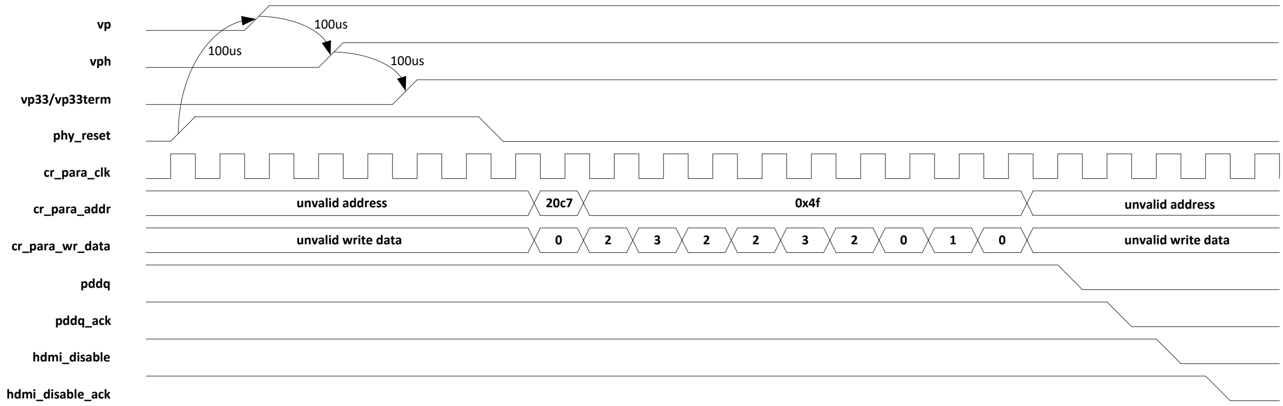

Fig. 28-5 HDMIRX PHY power up sequence

The cr_para_wr_data in 0x4f address has specific indication.

Table 28-2 HDMIRX PHY power up CMD sequence map

0X4F value	clk_sense_mode	clk_sense_write_en	clk_sense_write_clk	Description
0x2	0	1	0	set write enable
0x3	0	1	1	
0x2	0	1	0	
0x2	0	1	0	reset clock sense
0x3	0	1	1	
0x2	0	1	0	
0x0	0	0	0	reset write enable
0x1	0	0	1	
0x0	0	0	0	
0x0	0	0	0	default state

HDMIRX controller has one cr_para interface to configure HDMIRX PHY, and driver can configure the HDMIRX controller register to configure HDMIRX PHY.

Table 28-3 HDMIRX PHY power up configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0xc0[0]	phy_reset	0x1	0x1	Reset HDMIRX PHY
Wait for 100us				
0xc0[0]	phy_reset	0x1	0x0	Release HDMIRX PHY reset
0xe0[1:0]	phycreg_cr_para_selection_mode	0x0	0x3	This signal control the selection between the PHY JTAG and cr_para interface. The driver select the cr_para interface here.
Read the [10]bit of SYS_GRF_SOC_STATUS1(0x384, The GRF base address is 0XFD58C000), until this bit is 1'b1. This signal sram_init_done indicates the HDMIRX PHY SRAM initial done.				
Write the [1]bit of SYS_GRF_SOC_CON1(0x304), configure 1'b1. This signal is HDMIRX PHY sram_ext_ld_done signal, it is the handshake signal with sram_init_done signal				

SFR Address	SFR Name	Default Value	Setting Value	Description
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x20c7	Configure the first write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x0	Configure the first write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the first wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the second write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the second write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the second wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the third write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x3	Configure the third write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the third wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 4th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the 4th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				

SFR Address	SFR Name	Default Value	Setting Value	Description
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 4th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 5th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the 5th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 5th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 6th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x3	Configure the 6th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 6th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 7th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the 7th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 7th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 8th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x0	Configure the 8th write data

SFR Address	SFR Name	Default Value	Setting Value	Description
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 8th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 9th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x1	Configure the 9th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 9th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 10th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x0	Configure the 10th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 10th wdata finish
0xc0[1]	phy_pddq	0x1	0x0	Configure PHY pddq 1’b0, and HDMIRX PHY begins to enable its reference voltage generator and performs termination calibration.
Read 0xc8[0] bit, it is pddq_ack, read this register bit, wait and until it is 1’b0. It indicates pddq finish.				
0xc0[8]	phy_hdmi_disable	0x1	0x0	Configure PHY hdmi_disable 1’b0, and HDMIRX PHY begins to enter initialization sequence, and PHY begins to power up circuit calibrations.

SFR Address	SFR Name	Default Value	Setting Value	Description
Read 0xc8[1] bit, it is hdmi_disable_ack, read this register bit, wait and until it is 1’b0. It indicates power up finish.				
0xc0[11:9]	reffreq_sel	0x0	0x0	Select HDMIRX PHY cr_para_clk frequency. Default value is 24M. 3’b000: 24M 3’b001: 25M 3’b010: 27M 3’b011: 48M 3’b100: 50M 3’b101: 54M 3’b110: 100M
0xc0[15]	rxdata_width	0x0	0x1	Configure the rxdata width. 1’b0 is 20 bit valid, 1’b1 is 40 bit valid. And this version is quad pixel, so it is 40 bit valid.
Read 0x58c[1] bit, it is scdc_tmdsbitclkratio, before the HDMITX sends >= 3.4Gbps channel video, and it will be configured 1’b1 by the DDC bus.				
0xc0[16]	tmds_clk_ratio	0x0	0x0	If the HDMIRX PHY channel bit rate is >= 3.4Gbps, for example 4k resolution, tmds_clk_ration must be configured 1’b1.

28.6.1.2 HDMIRX PHY Power down sequence

The figure below is HDMIRX PHY power down timing diagram.

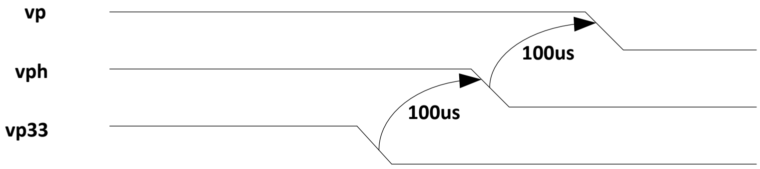

Fig. 28-6 HDMIRX PHY power down sequence

VPH, VP, VPDIG, and VP33TERM are power supply inputs of the PMA Hard Macro in the PHY. Vpdig is the core supply for the Soft IP part.

28.6.1.3 HDMIRX PHY Clock Sense mode

Analog Front End of HDMI RX PHY supports clock sense mode feature which allows to reduce power consumption of the PHY in suspend mode and monitor TMDS clock lines for any activity to wake up the system. In clock sense mode only reduced number of analog blocks is enabled – LDO, clock_sense block, termination and input protection.

In order to minimize current consumption even more vp/vpdig (core supply) can be powered down. To enable such option all AFE blocks used in close sense mode are supplied from 3.3V/1.8V domain. Output of the clock sense block is connected to dedicated clock_sense bump/pin and its level should be monitored by customer power management unit to wake up HDMIRX PHY subsystem once TMDS clock lane activity is detected. Since there might be no vp/vp_dig (core supply) available in clock sense mode it is necessary to store configuration of blocks used during clock sense mode in analog registers supplied from 1.8V/3.3V domain. The figure below shows the clock sense mode diagram.

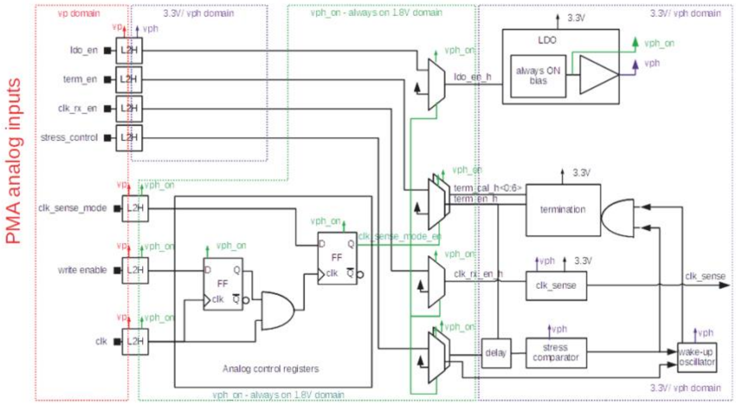

Fig. 28-7 HDMIRX PHY clock sense mode diagram

The figure below shows the HDMIRX PHY clock sense mode configuration sequence.

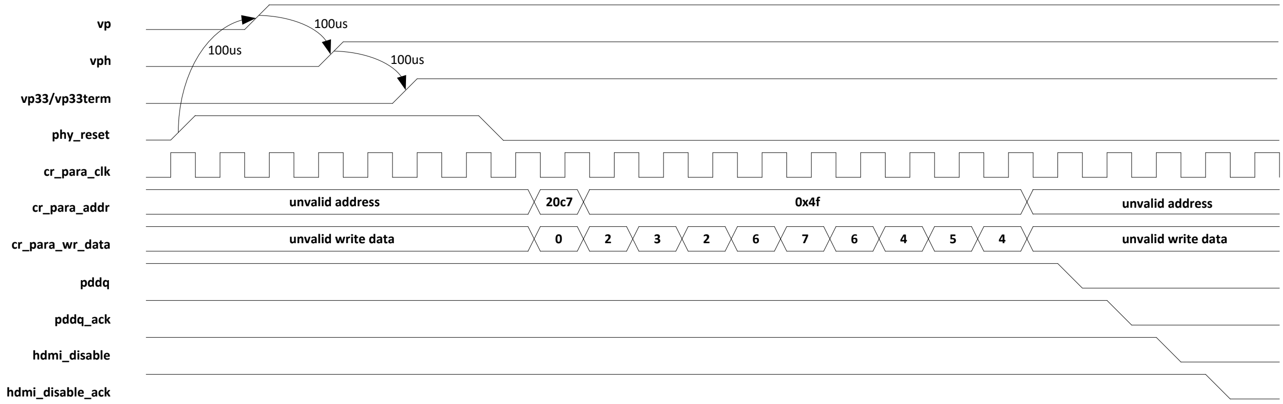

Fig. 28-8 HDMIRX PHY clock sense mode configuration sequence

The table below is the HDMIRX PHY clock sense mode configuration sequence map.

Table 28-4 HDMIRX PHY clock sense mode configuration sequence map

0X4F value	clk_sense_mode	clk_sense_write_en	clk_sense_write_clk	Description
0x2	0	1	0	set write enable
0x3	0	1	1	
0x2	0	1	0	
0x6	1	1	0	set clock sense
0x7	1	1	1	
0x6	1	1	0	
0x4	1	0	0	reset write enable
0x5	1	0	1	
0x4	1	0	0	
0x0	0	0	0	default state

Driver can configure the HDMIRX controller register to configure HDMIRX PHY, which in clock sense mode.

Table 28-5 HDMIRX PHY clk sense mode power up configuration operation

SFR Address	SFR Name	Default Value	Setting Value	Description
0xc0[0]	phy_reset	0x1	0x1	Reset HDMIRX PHY
Wait for 100us				
0xc0[0]	phy_reset	0x1	0x0	Release HDMIRX PHY reset

SFR Address	SFR Name	Default Value	Setting Value	Description
0xe0[1:0]	phycreg_cr_para_selection_mode	0x0	0x3	This signal control the selection between the PHY JTAG and cr_para interface. The driver select the cr_para interface here.
Read the [10]bit of SYS_GRF_SOC_STATUS1(0x384, The GRF base address is 0XFD58C000), until this bit is 1’b1. This signal sram_init_done indicates the HDMIRX PHY SRAM initial done.				
Write the [1]bit of SYS_GRF_SOC_CON1(0x304), configure 1’b1. This signal is HDMIRX PHY sram_ext_ld_done signal, it is the handshake signal with sram_init_done signal				
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x20c7	Configure the first write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x0	Configure the first write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the first wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the second write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the second write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the second wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the third write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x3	Configure the third write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				

SFR Address	SFR Name	Default Value	Setting Value	Description
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the third wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 4th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x2	Configure the 4th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 4th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 5th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x6	Configure the 5th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 5th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 6th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x7	Configure the 6th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1'b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 6th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 7th write address

SFR Address	SFR Name	Default Value	Setting Value	Description
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x6	Configure the 7th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 7th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 8th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x4	Configure the 8th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 8th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 9th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x5	Configure the 9th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 9th wdata finish
0xe4[15:0]	phycreg_cr_para_addr	0x0	0x4f	Configure the 10th write address
0xe8[15:0]	phycreg_cr_para_wdata	0x0	0x4	Configure the 10th write data
0xf0[1]	phycreg_cr_para_write_p	0x0	0x1	Configure the write enable(it is just one cycle pulse)
Read the 0x5030[10] bit, it is phycreg_cr_write_done_irq status, read this register and wait this signal until it is 1’b1.				

SFR Address	SFR Name	Default Value	Setting Value	Description
0x5038[10]	phycreg_cr_write_done_clear	0x0	0x1	Clear the phycreg_cr_write_done_irq status, and the 10th wdata finish
0xc0[1]	phy_pddq	0x1	0x0	Configure PHY pddq 1'b0, and HDMIRX PHY begins to enable its reference voltage generator and performs termination calibration.
Read 0xc8[0] bit, it is pddq_ack, read this register bit, wait and until it is 1'b0. It indicates pddq finish.				
0xc0[8]	phy_hdmi_disable	0x1	0x0	Configure PHY hdmi_disable 1'b0, and HDMIRX PHY begins to enter initialization sequence, and PHY begins to power up circuit calibrations.
Read 0xc8[1] bit, it is hdmi_disable_ack, read this register bit, wait and until it is 1'b0. It indicates power up finish.				
0xc0[11:9]	reffreq_sel	0x0	0x0	Select HDMIRX PHY cr_para_clk frequency. Default value is 24M. 3'b000: 24M 3'b001: 25M 3'b010: 27M 3'b011: 48M 3'b100: 50M 3'b101: 54M 3'b110: 100M
0xc0[15]	rxdata_width	0x0	0x1	Configure the rxdata width. 1'b0 is 20 bit valid, 1'b1 is 40 bit valid. And this version is quad pixel, so it is 40 bit valid.
Read 0x58c[1] bit, it is scdc_tmdsbitclkratio, before the HDMITX sends >= 3.4Gbps channel video, and it will be configured 1'b1 by the DDC bus.				
0xc0[16]	tmds_clk_ratio	0x0	0x0	If the HDMIRX PHY channel bit rate is >= 3.4Gbps, for example 4k resolution, tmds_clk_ration must be configured 1'b1.

28.6.1.4 RX Data Path

The RX data-path is active when the main FSM either observes a stable clock on the TMDSCLK in HDMI1.4/20 modes. When data-path is enabled, Hard macro block asserts rxX_valid (per lane, X=0, 1, 2) when a predetermined bit-locking timer expires. Thereafter, the data on all the active lanes (lane0, lane1, lane2) is aligned on a single clock, symbol

alignment is performed, inter-lane skew is corrected and valid data is provided at the rxX_data[39:0](X=0, 1, 2) ports. The validity of the data is indicated by asserting rxdata_valid port.
The 40 bit valid data is shown in diagram below.

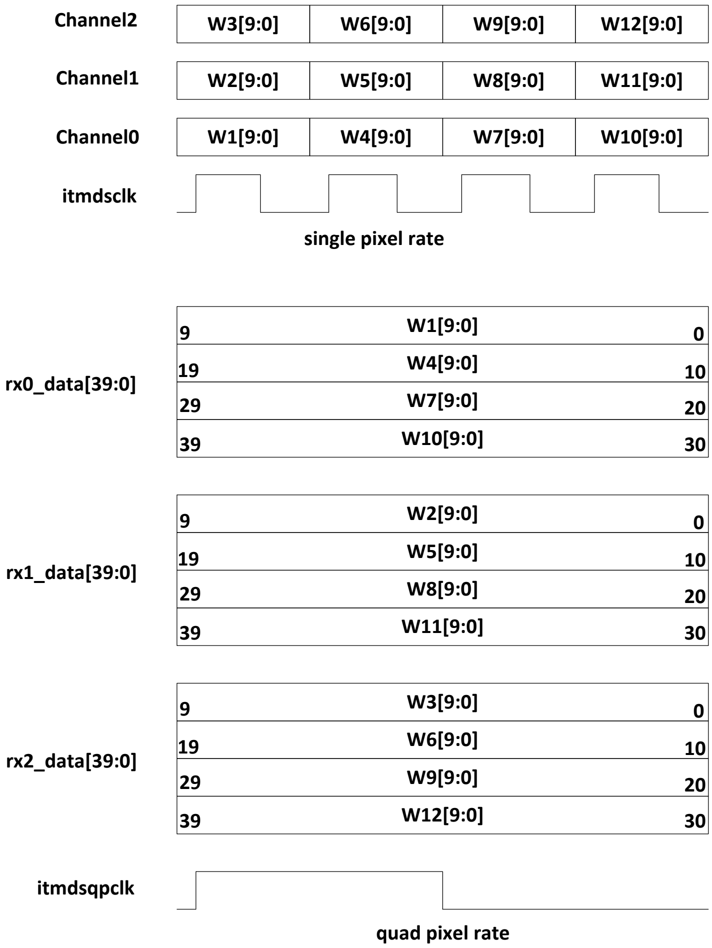

Fig. 28-9 HDMIRX PHY output quad pixel rate diagram

28.6.1.5 External SRAM

The raw PCS stores the instruction code to execute the calibration and adaptation algorithms. In order to minimize the area of the raw PCS, this pre-optimized and pre-validated code is stored in the form of hard-coded look up table. An external SRAM must be included for the purpose of updating the IP firmware. This provides flexibility for future and post-silicon product enhancements.
After de-assertion of phy_reset, the boot loader in the raw PCS loads the code from the internal look up table to the external SRAM and asserts output signal: sram_init_done(SYS_GRF_SOC_STATUS1[27], 0x384). After initialization of SRAM, user can change the SRAM contents (or access any PHY register) using either the JTAG or the CR Parallel Interface by addressing the SRAM address space in the register map. After external access to the SRAM (or any other PHY register) is complete, input sram_ext_ld_done (SYS_GRF_SOC_CON1[1], 0x304) should be set high, allowing the FSM in the raw PCS to start executing the code from SRAM.
Figure below shows the timing diagram of SRAM initialization and loading.

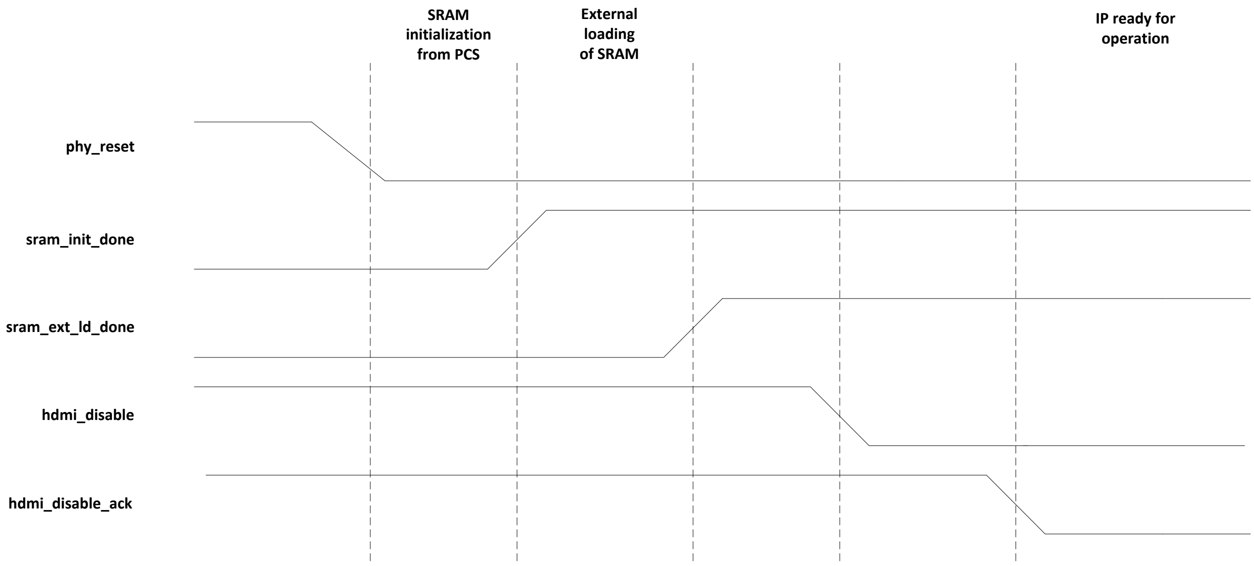

Fig. 28-10 HDMIRX PHY SRAM initialization and loading sequence

Before assertion of sram_init_done, the boot loader controls the SRAM interface. The firmware program is read from the ROM and written to SRAM.
When the boot loader is complete(sram_init_done is asserted), The cr_para interface can be used to access all register/ROM/SRAM in the HDMIRX PHY before firmware starts executing instructions. This access is controlled by internal memory arbiter.
Wait for at least 1 cr_para clock after the final external SRAM access before asserting sram_ext_ld_done signal. This is to ensure the final external SRAM access has been completed.