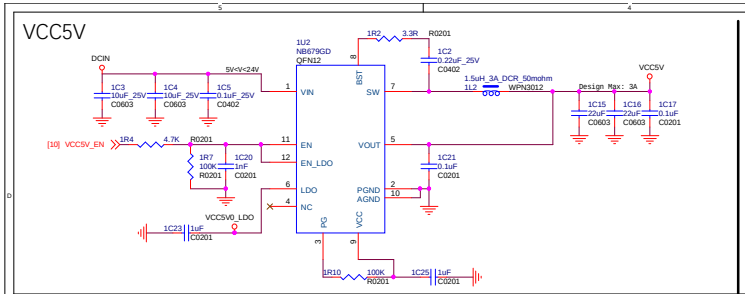
KHADAS

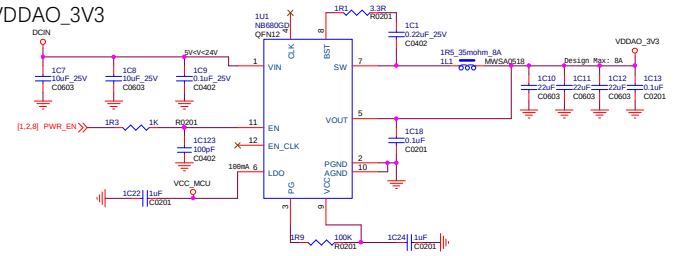
Something a little different.

Shenzhen Wesion Technology Co., Ltd.			
Project:	**VIM4**		
File:	Khadas		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	0

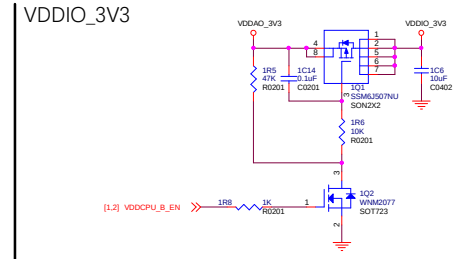
VCC5V



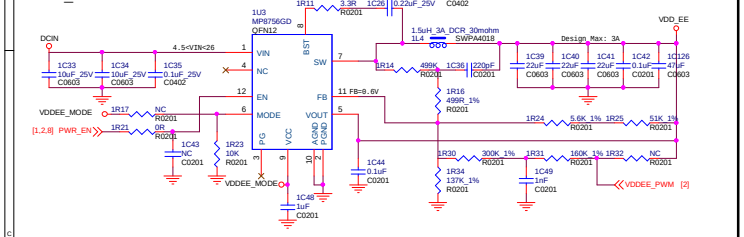
VDDAO_3V3



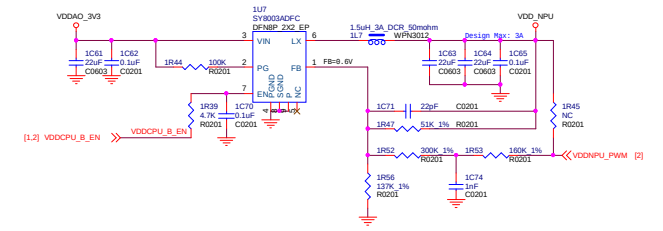
VDDIO_3V3



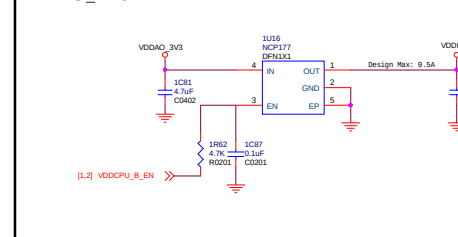
VDD_EE



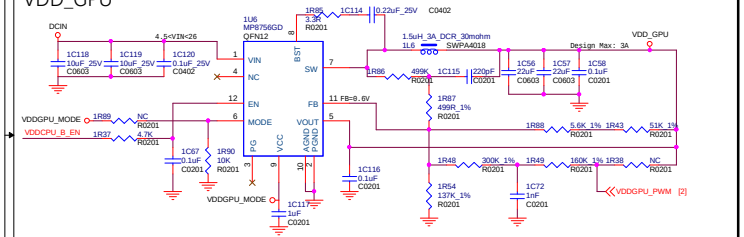
VDD_NPU



VDDIO_1V8



VDD_GPU



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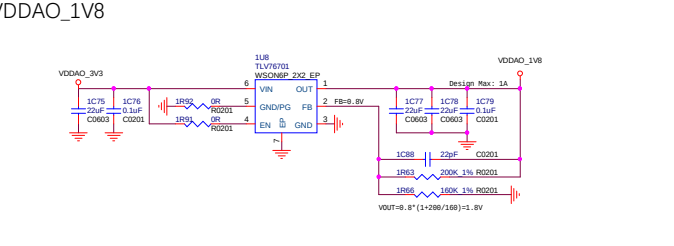
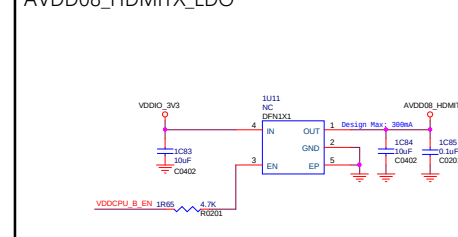
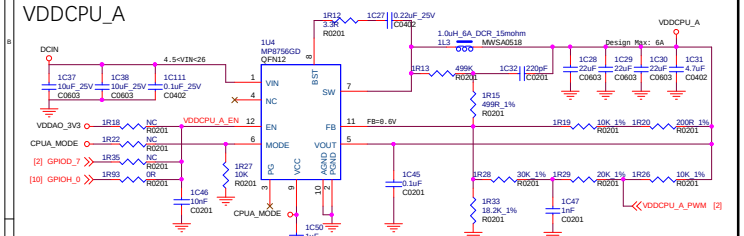


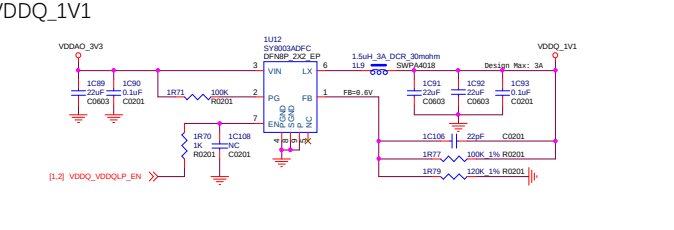
AVDD08_HDMITX_LDO



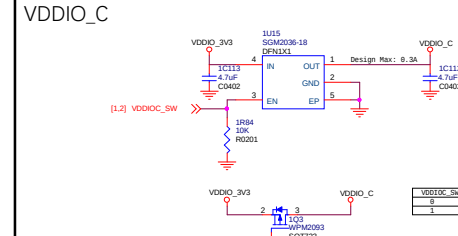
VDDCPU_A



VDDQ_1V1

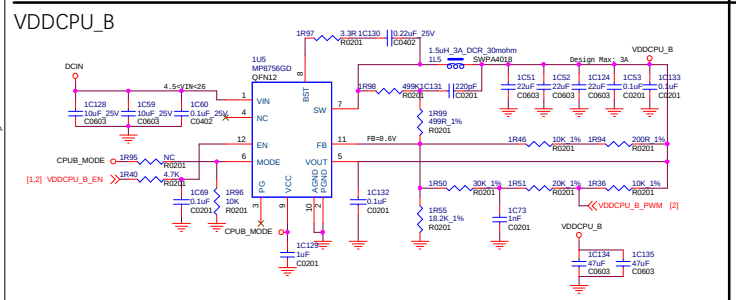


VDDIO_C

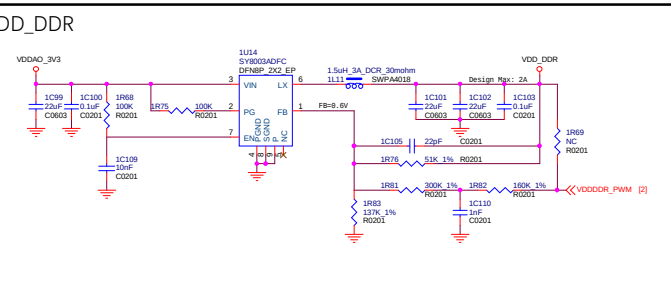


VDDIOC_SW	VDDIO_C
0	3.3V
1	1.8V

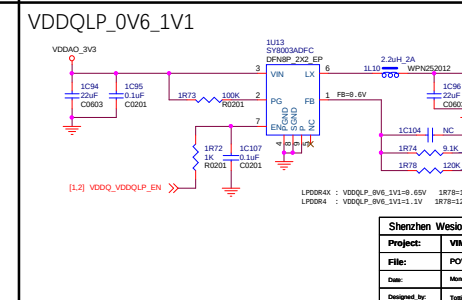
VDDCPU_B



VDD_DDR

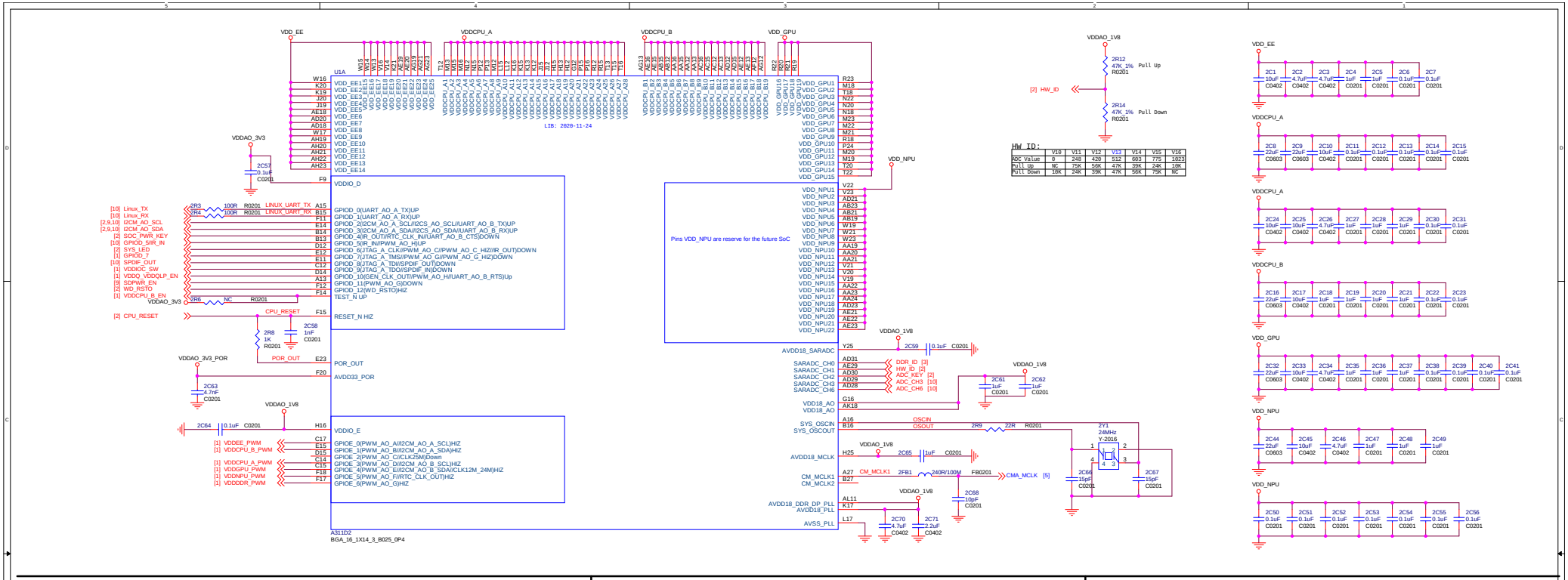


VDDQLP_0V6_1V1

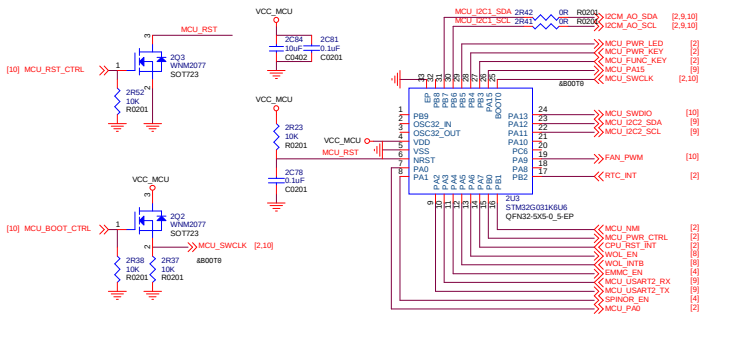


LPDDR4X : VDDQLP_0V6_1V1=0.65V 1R78=120K_1% 1R74=9.1K_1%(default)
LPDDR4 : VDDQLP_0V6_1V1=1.1V 1R78=120K_1% 1R74=100K_1%

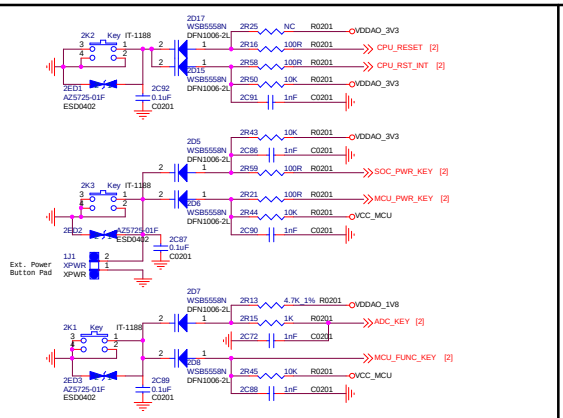
Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	POWER		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	1



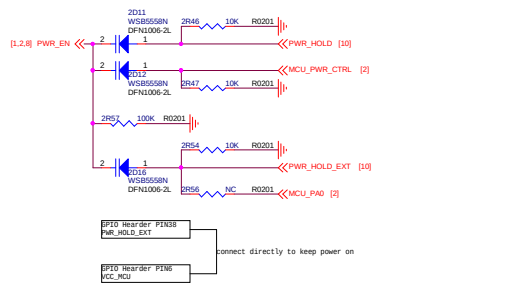
MCU



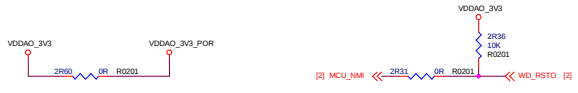
Buttons



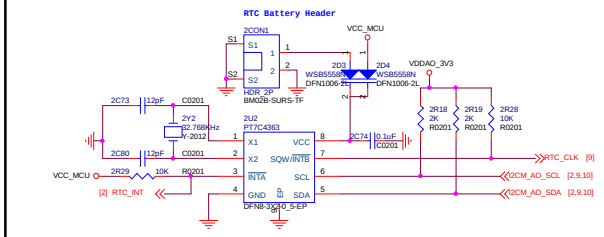
PWR_EN



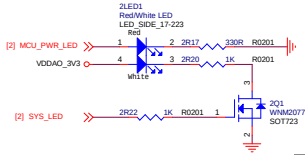
RESET & Watchdog



RTC

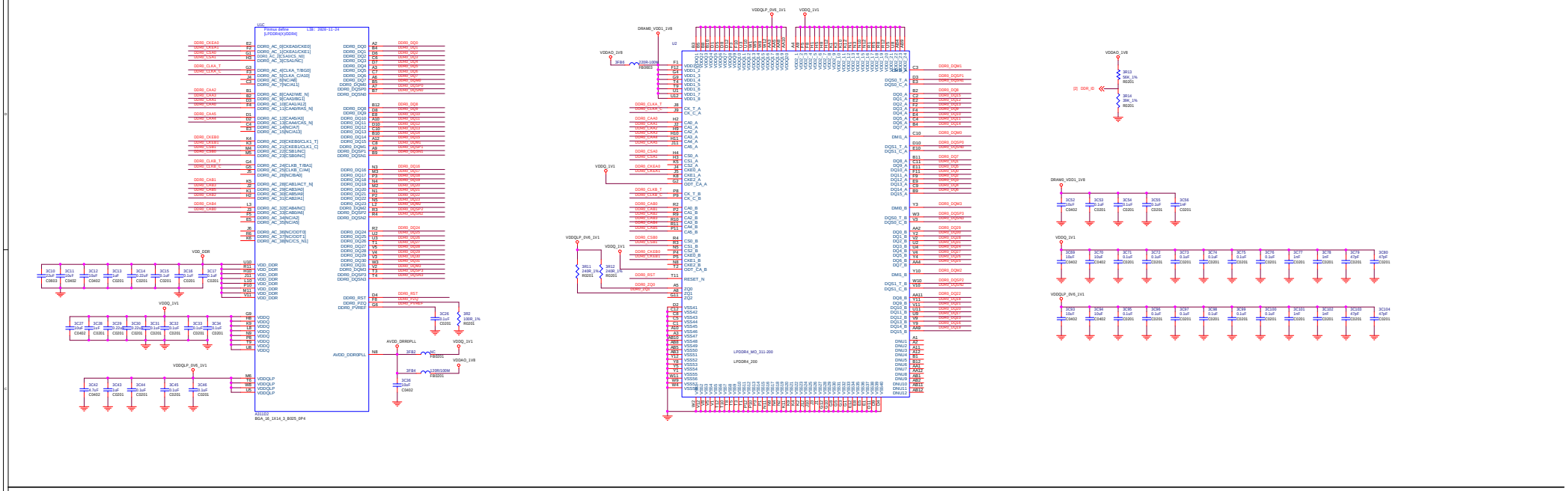


LED

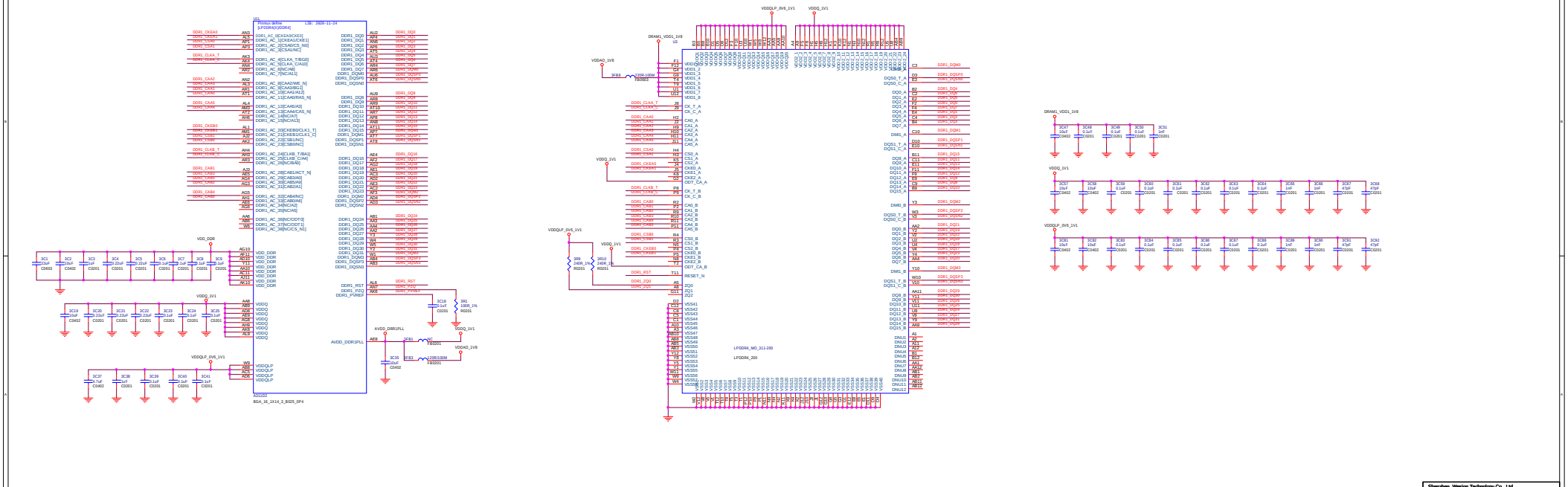


Shenzhen Wesion Technology Co., Ltd.	
Project:	VIM4
File:	CPU/MCU/RTC
Date:	Monday, November 21, 2022
Rev:	V13
Designed_by:	Totti
Sheet:	2

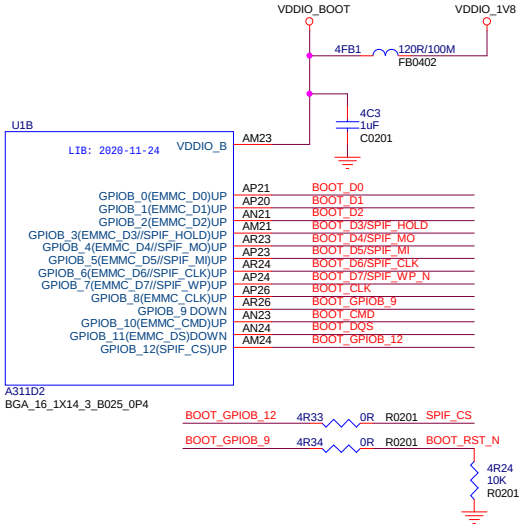
DDR Channel 0



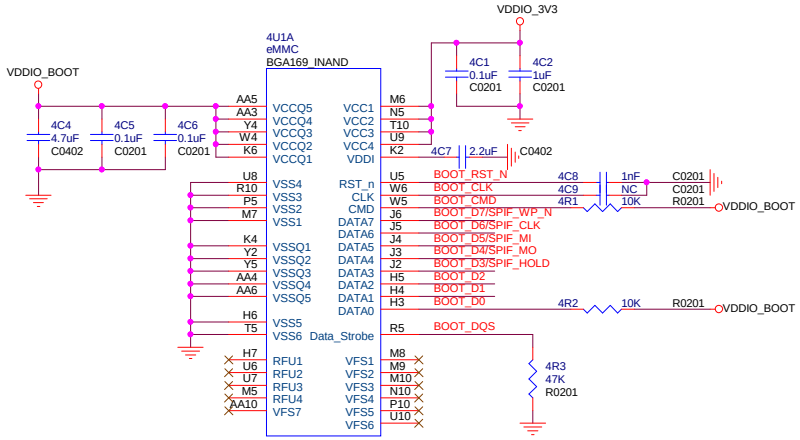
DDR Channel 1

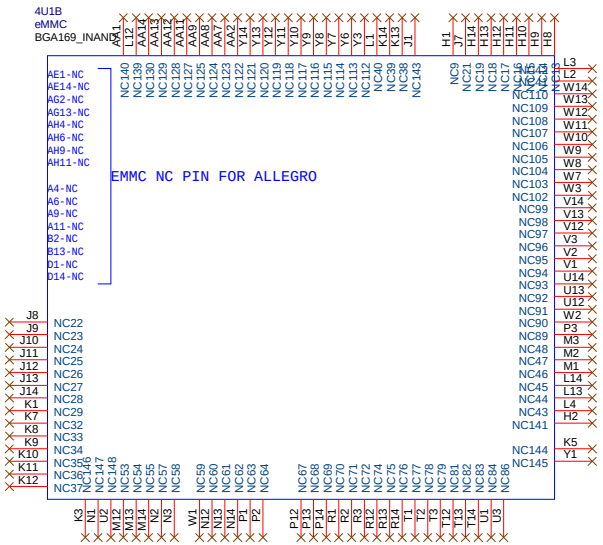


Shenzhen Wesion Technology Co., Ltd	
Project:	VIM4
File:	DDR
Date:	Monday, November 21, 2022
Rev:	V13
Designed_by:	Yuli
Sheet:	3



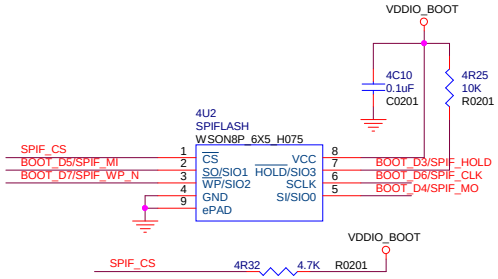
EMMC



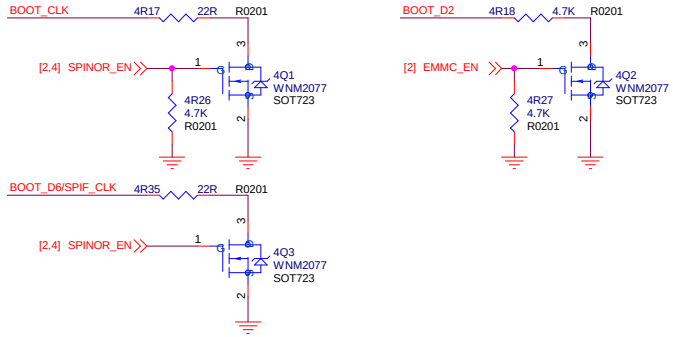


Power ON Config

SPI Flash



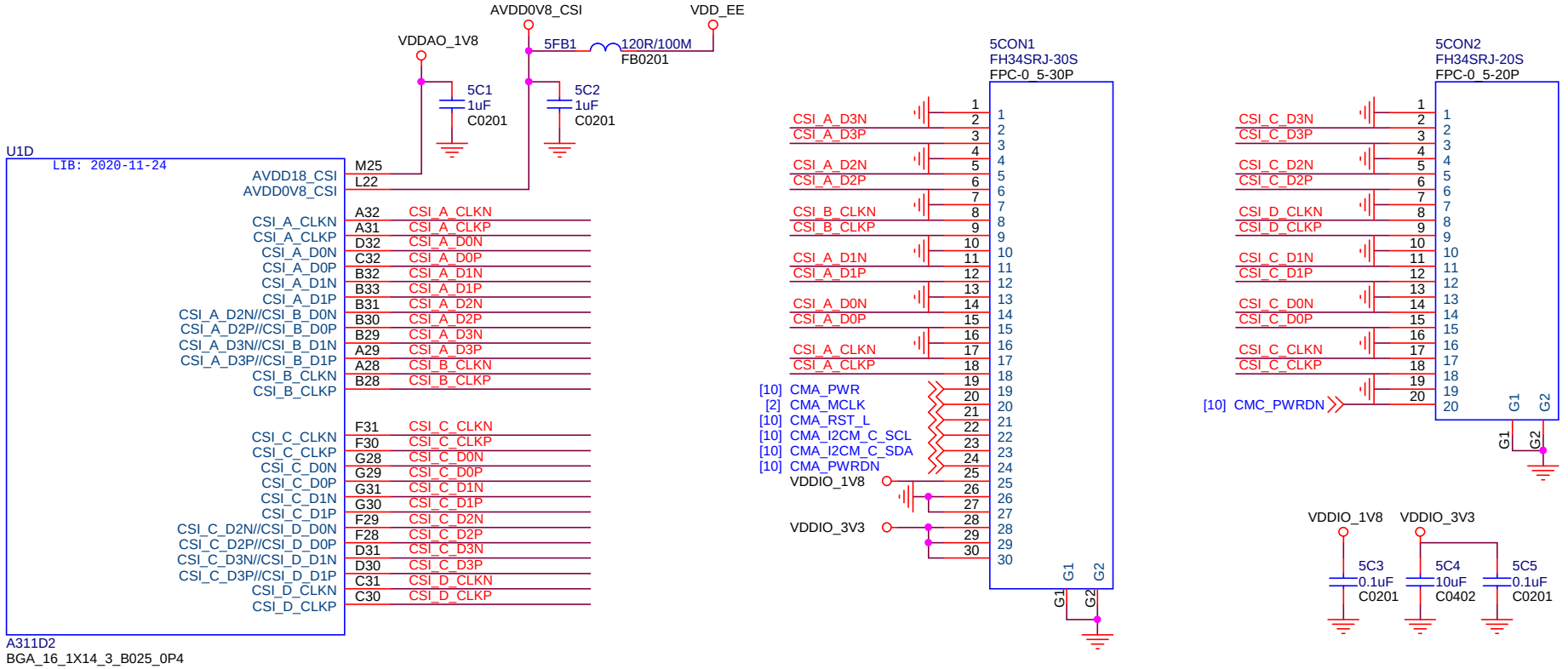
TST



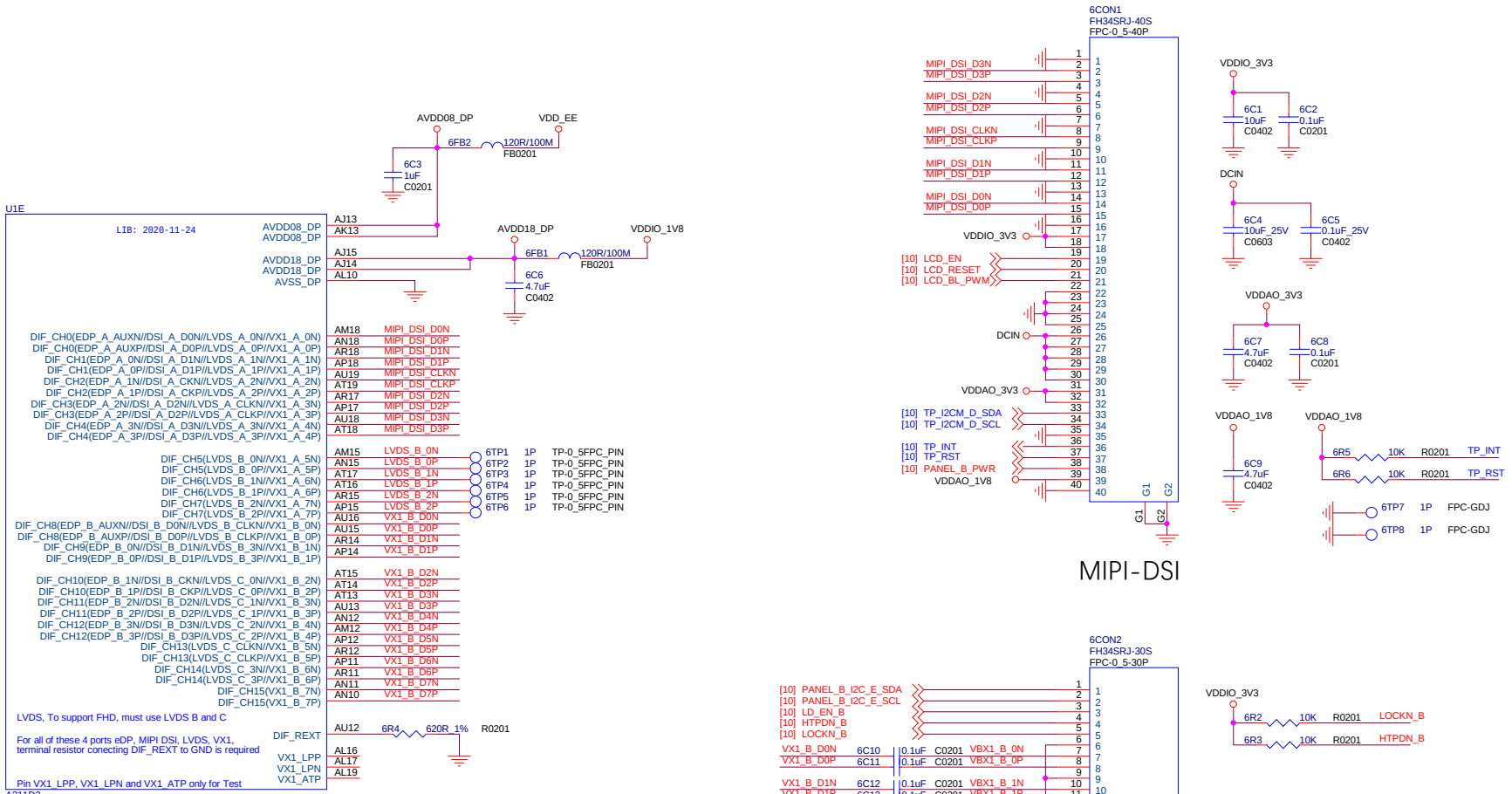
Booting Sequence Diagram

EMMC_EN	SPINOR_EN	1st Boot	2nd Boot	3rd Boot	4th Boot
0	0	SD Card	eMMC	SPI Flash	USB
1	0	SD Card	SPI Flash	eMMC	USB
x	1	USB			

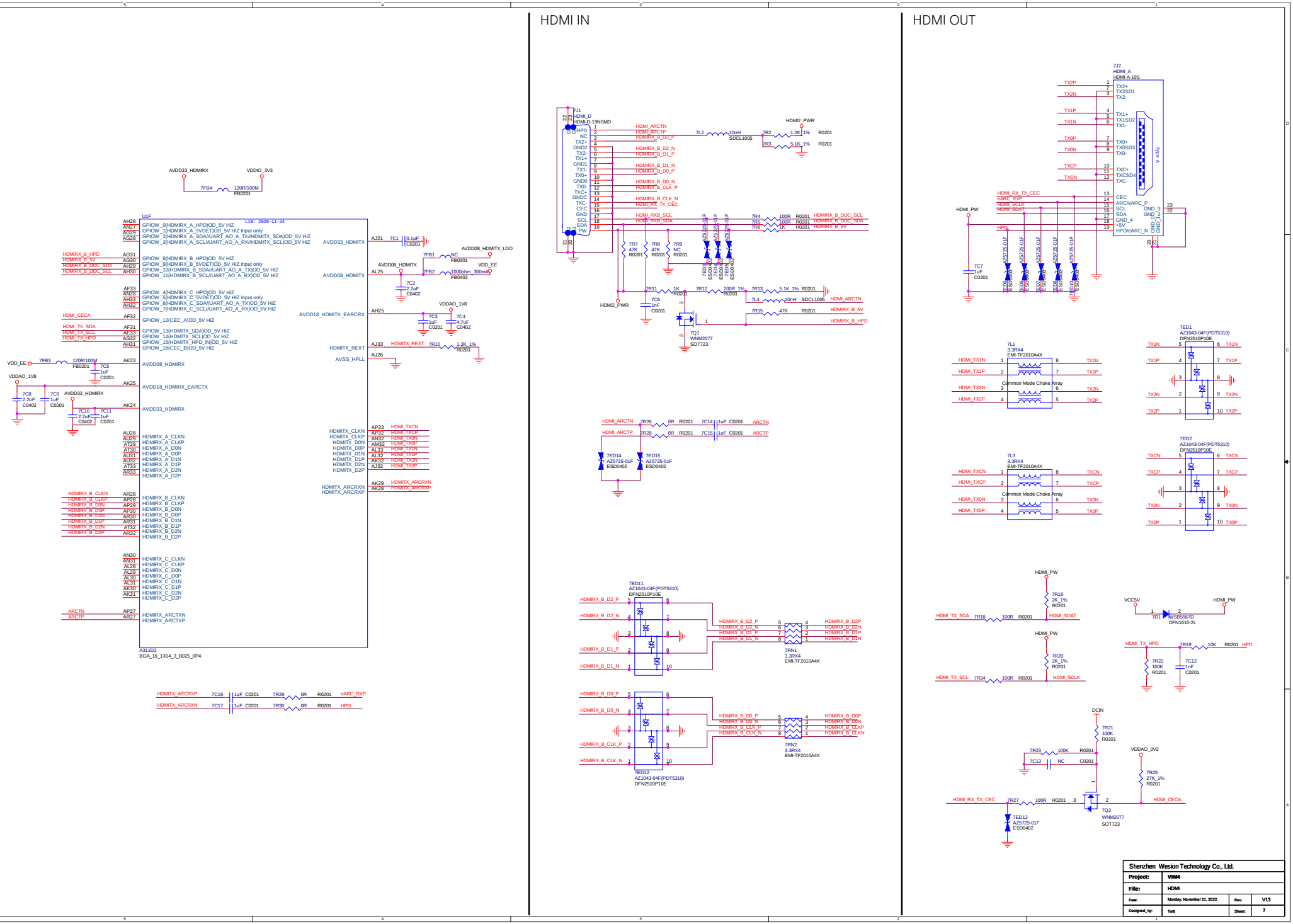
Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	eMMC		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	4



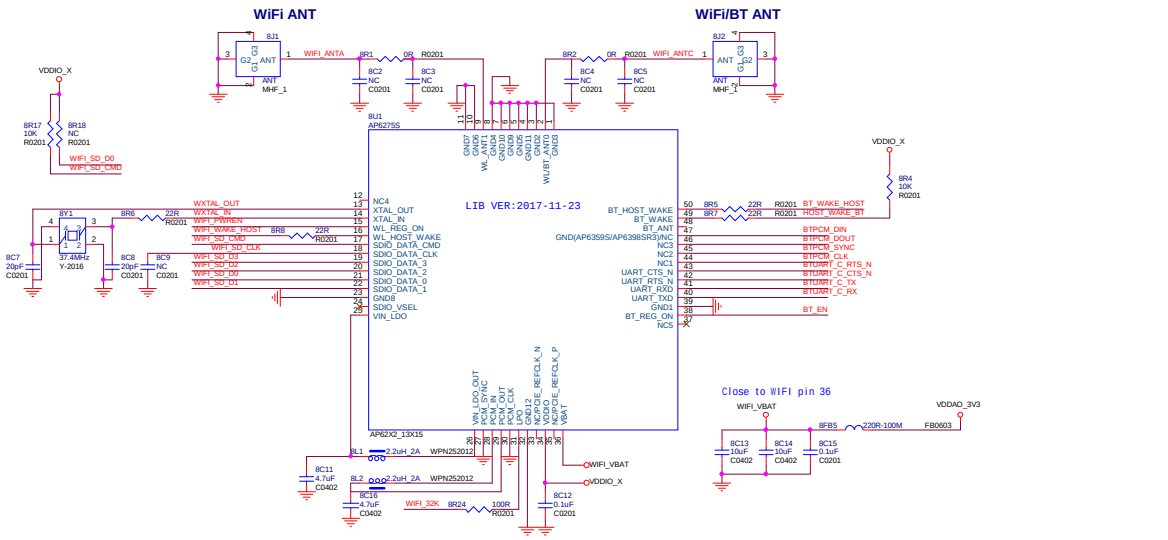
Shenzhen Wesion Technology Co., Ltd.			
Project:	**VIM4**		
File:	CSI_CAMERA		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	5



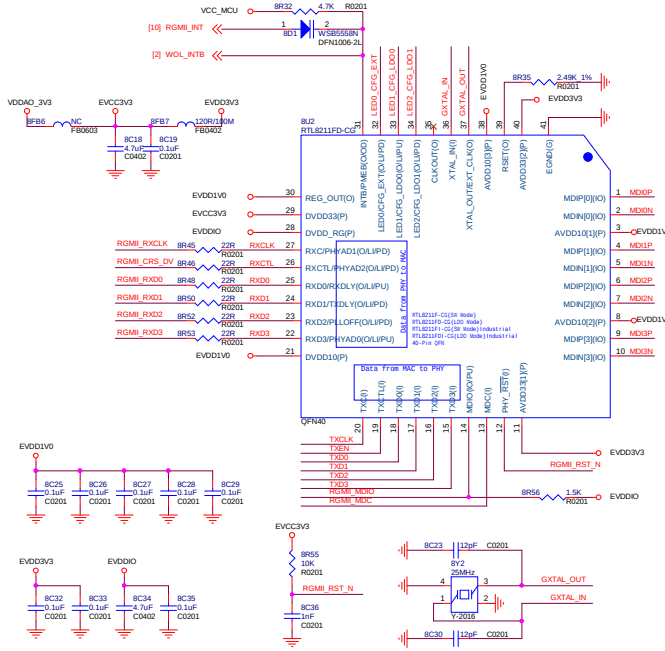
Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	DSI/eDP/LVDS/VX1		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	6


HDMI IN
HDMI OUT
U1F
LIB: 2020-11-24
A311D2
BGA_16_1X14_3_B025_0P4
J1
HDMI_D
HDMI-D-19WSMD
7J2
HDMI_A
HDMI-A-19S
Type A
7ED1
AZ1043-04F(PDT5310)
DFN2510P10E
7ED2
AZ1043-04F(PDT5310)
DFN2510P10E
7ED11
AZ1043-04F(PDT5310)
DFN2510P10E
7ED12
AZ1043-04F(PDT5310)
DFN2510P10E
7RN1
3.3RX4
EMI-TF2010A4X
7RN2
3.3RX4
EMI-TF2010A4X
7L1
3.3RX4
EMI-TF2010A4X
7L3
3.3RX4
EMI-TF2010A4X
Common Mode Choke Array
7Q1
WNM2077
SOT723
7Q2
WNM2077
SOT723
7D1
MSB5567D
DFN1610-2L
HDMI_PW
HDMI2_PWR
VDDAO_1V8
VDD_EE
AVDD33_HDMIRX
VDDIO_3V3
AVDD08_HDMITX_LDO
AVDD08_HDMITX
AVDD18_HDMITX_EARCRX
HDMITX_REXT
AVSS_HPLL
AVDD08_HDMIRX
AVDD18_HDMIRX_EARCTX
AVDD33_HDMIRX
HDMI_ARCTN
HDMI_ARCTP
HDMI_RX_TX_CEC
HDMI_SCLK
HDMI_SDAT
HDMI_RX5P
HDMI_TX_SDA
HDMI_TX_SCL
HDMI_TX_HPD
HDMI_CECA
HPD
DCIN
VCC5V
VDDAO_3V3
HDMIRX_B_HPD
HDMIRX_B_5V
HDMIRX_B_DDC_SCL
HDMIRX_B_DDC_SDA
HDMIRX_B_CLKN
HDMIRX_B_CLKP
HDMIRX_B_D0N
HDMIRX_B_D0P
HDMIRX_B_D1N
HDMIRX_B_D1P
HDMIRX_B_D2N
HDMIRX_B_D2P
HDMITX_CLKN
HDMITX_CLKP
HDMITX_D0N
HDMITX_D0P
HDMITX_D1N
HDMITX_D1P
HDMITX_D2N
HDMITX_D2P
HDMITX_ARCRXN
HDMITX_ARCRXP
eARC_RXP
HPD
Shenzhen Wesion Technology Co., Ltd.
Project: VIM4
File: HDMI
Date: Monday, November 21, 2022
Rev: V13
Designed_by: Totti
Sheet: 7

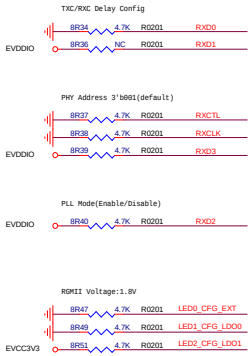
Wi-Fi & BT



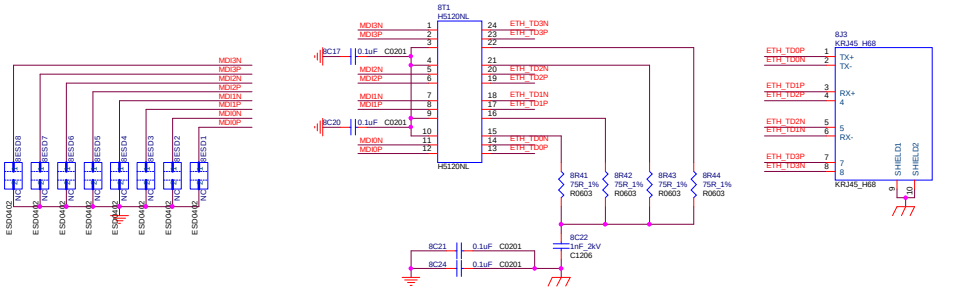
Ethernet



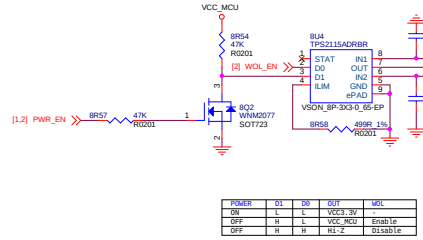
Configuration



RJ45

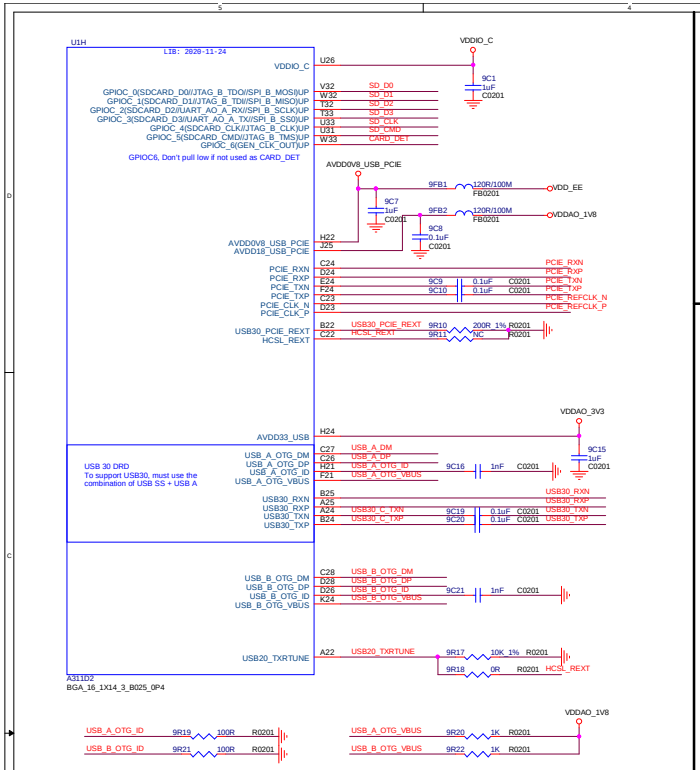


WOL

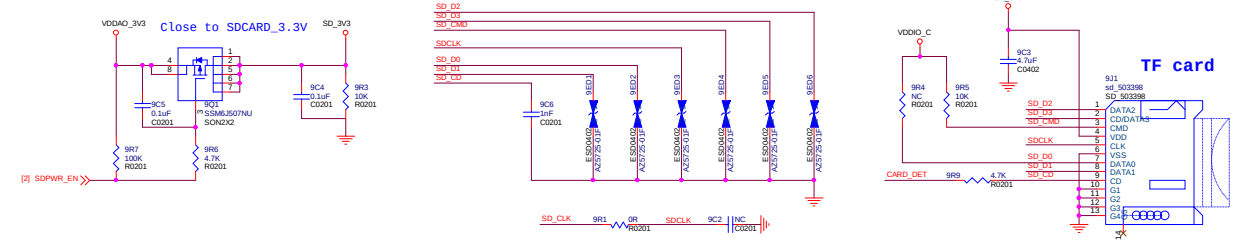


POWER	D1	D0	OUT	WOL
ON	L	L	VCC3.3V	-
OFF	H	L	VCC_MCU	Enable
OFF	H	H	Hi-Z	Disable

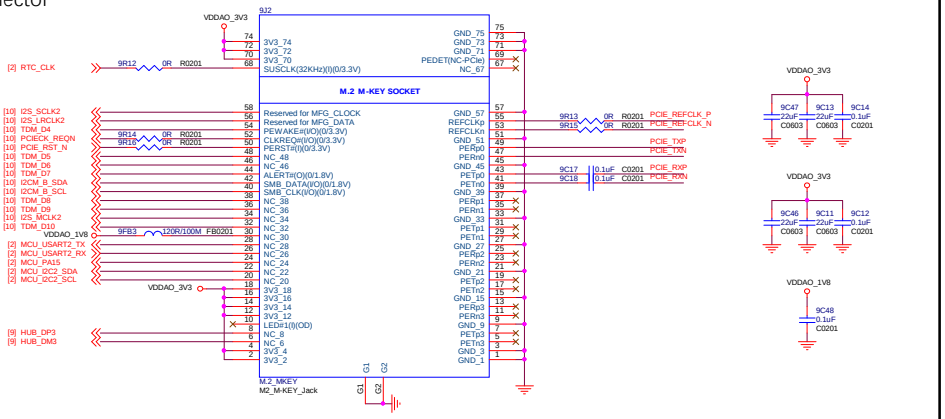
Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	ETH_RGMII/WIFI		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	8



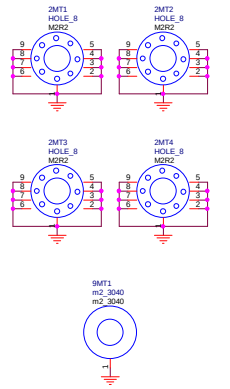
SD Card



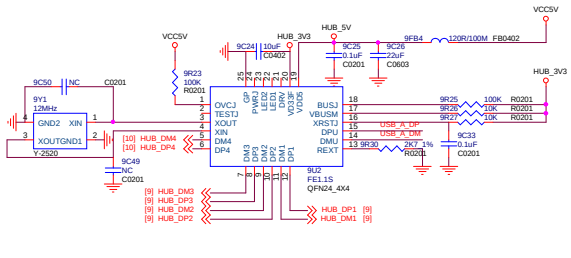
M.2 Connector



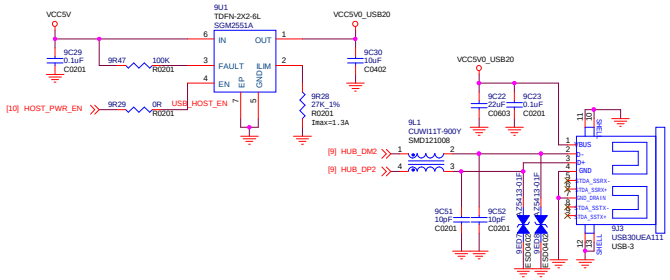
Mouting Holes



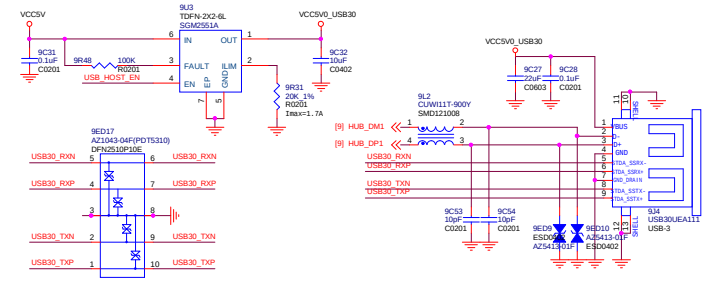
USB HUB



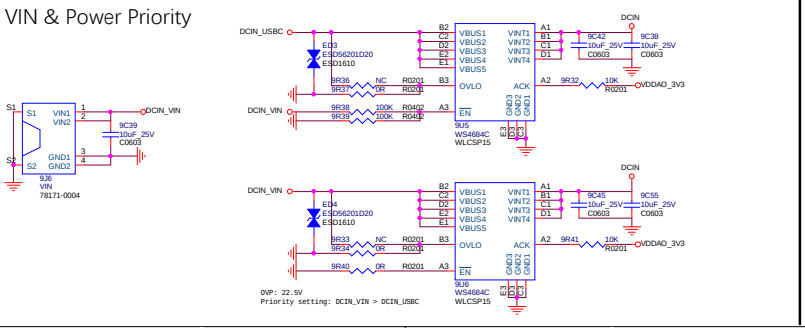
USB 2.0



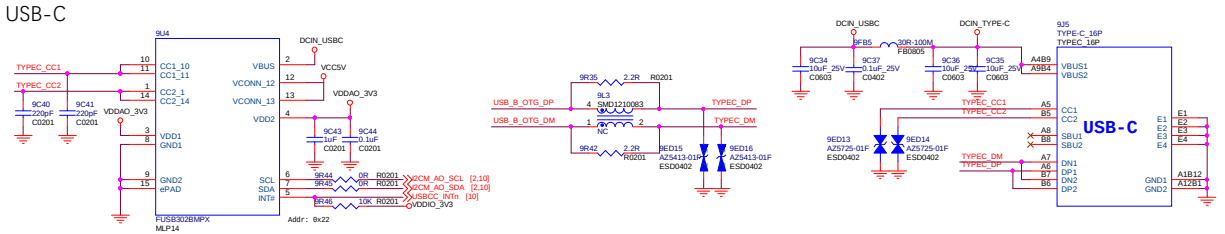
USB 3.0



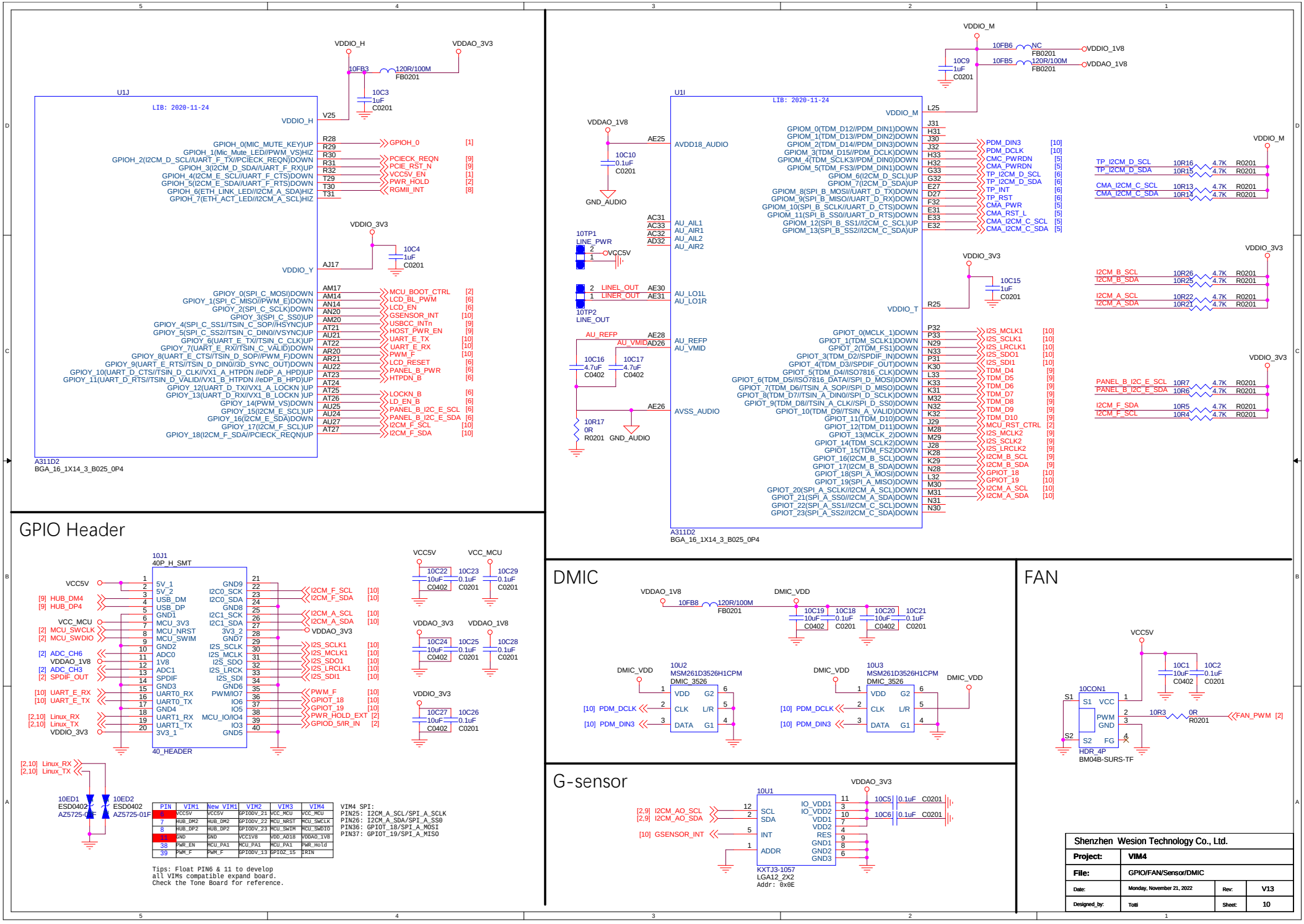
VIN & Power Priority



USB-C



Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	USB/PCIE/SDIO		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	9


U1J
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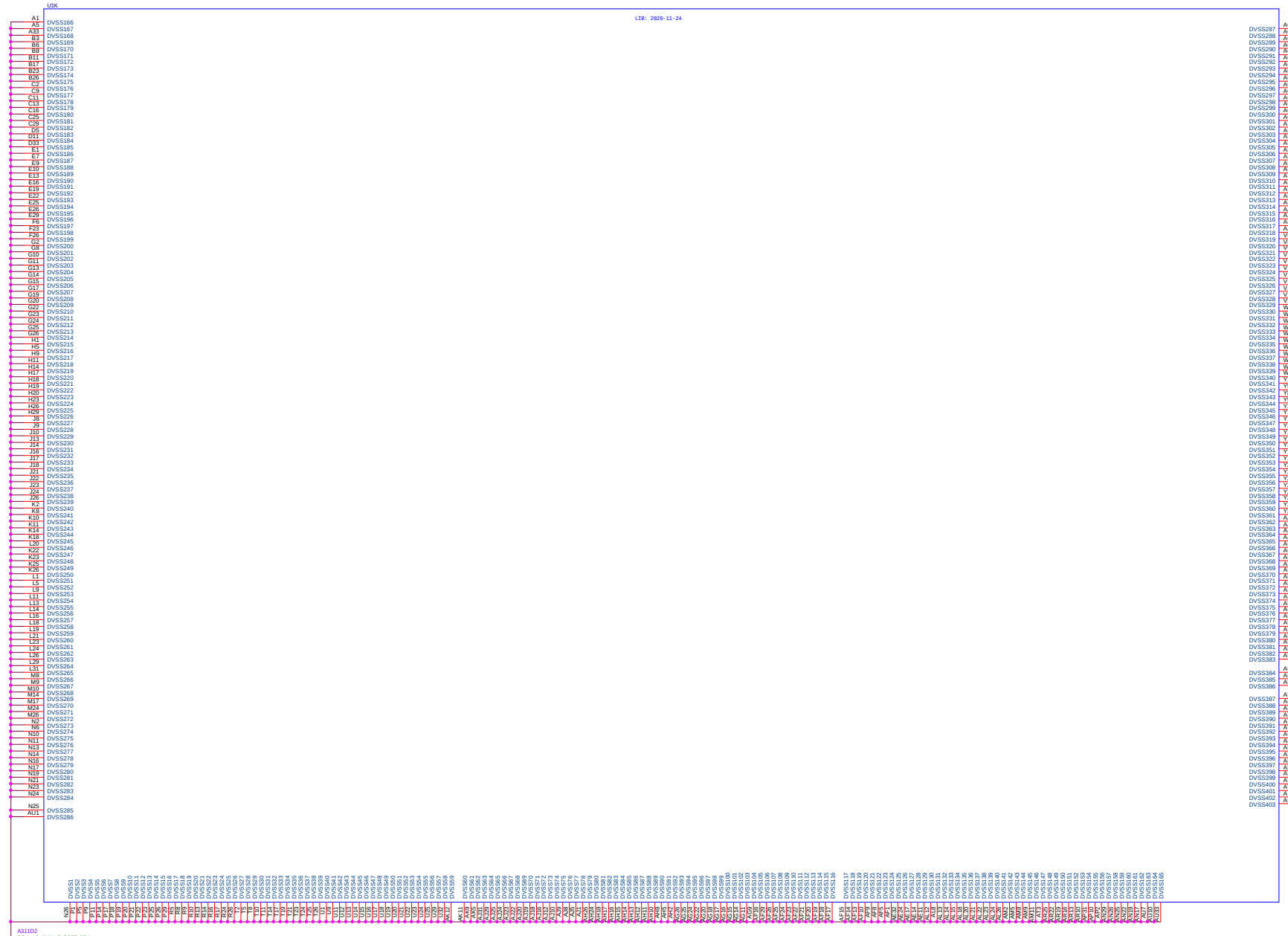
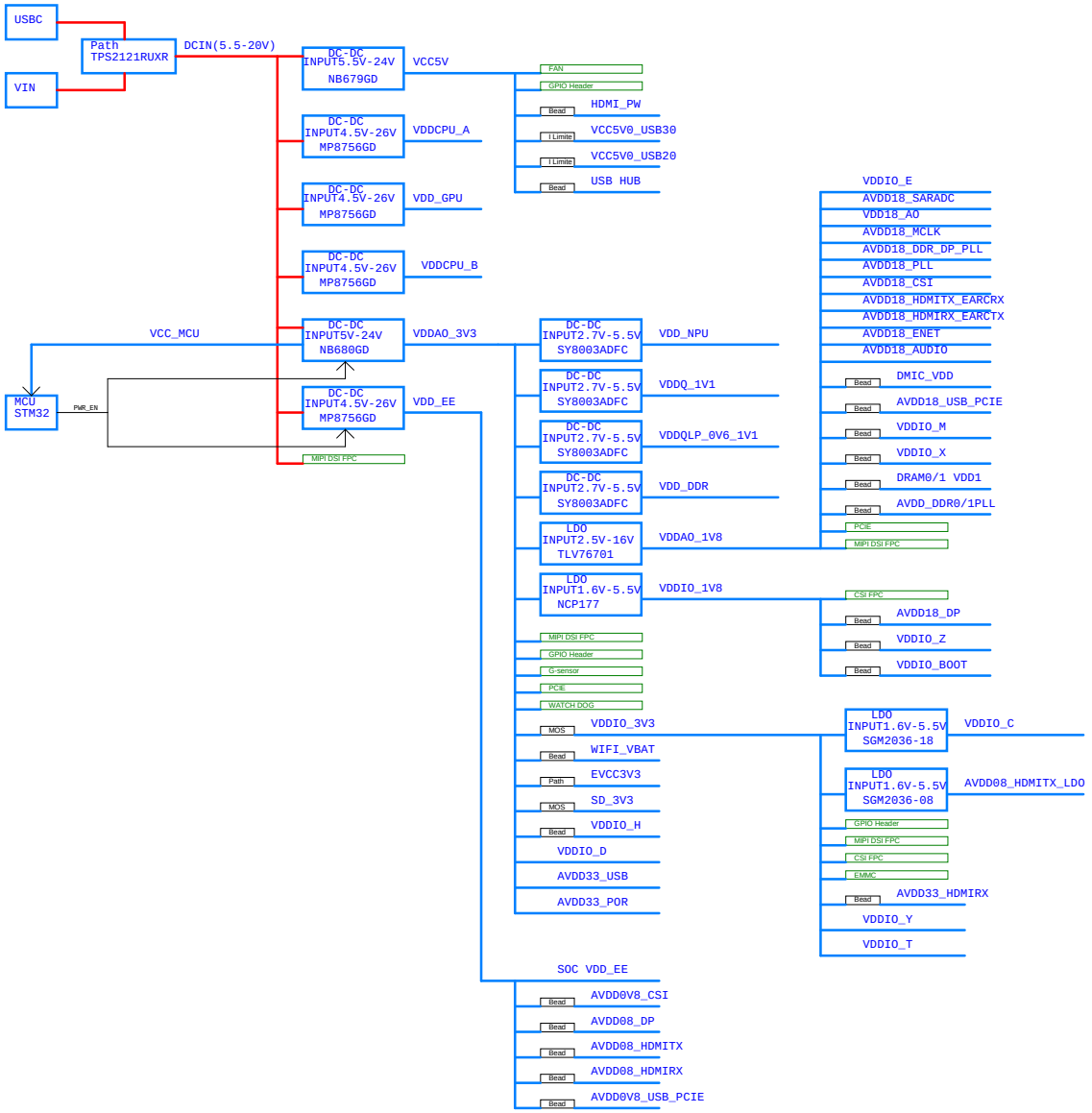
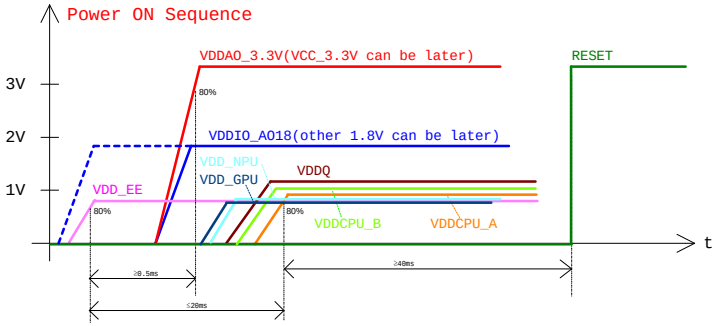
VDDIO_H
VDDAO_3V3
10FB3
120R/100M
FB0201
10C3
1uF
C0201
V25
R28 GPIOH_0 [1]
R29
R30
R31 PCIECK_REQN [9]
R32 PCIE_RST_N [9]
T29 VCC5V_EN [1]
T30 PWR_HOLD [2]
T31 RGMII_INT [8]
GPIOH_0(MIC_MUTE_KEY)UP
GPIOH_1(Mic_Mute_LED//PWM_VS)HIZ
GPIOH_2(I2CM_D_SCL//UART_F_TX//PCIECK_REQN)DOWN
GPIOH_3(I2CM_D_SDA//UART_F_RX)UP
GPIOH_4(I2CM_E_SCL//UART_F_CTS)DOWN
GPIOH_5(I2CM_E_SDA//UART_F_RTS)DOWN
GPIOH_6(ETH_LINK_LED//I2CM_A_SDA)HIZ
GPIOH_7(ETH_ACT_LED//I2CM_A_SCL)HIZ
VDDIO_3V3
10C4
1uF
C0201
VDDIO_Y
AJ17
AM17 MCU_BOOT_CTRL [2]
AM14 LCD_BL_PWM [6]
AN14 LCD_EN [6]
AN20 GSENSOR_INT [10]
AM20 USBCC_INTn [9]
AT21 HOST_PWR_EN [9]
AU21 UART_E_TX [10]
AT22 UART_E_RX [10]
AR20 PWM_F [10]
AR21 LCD_RESET [6]
AU22 PANEL_B_PWR [6]
AT23 HTPDN_B [6]
AT24
AT25 LOCKN_B [6]
AT26 LD_EN_B [6]
AU25 PANEL_B_I2C_E_SCL [6]
AU24 PANEL_B_I2C_E_SDA [6]
AU27 I2CM_F_SCL [10]
AT27 I2CM_F_SDA [10]
GPIOY_0(SPI_C_MOSI)DOWN
GPIOY_1(SPI_C_MISO//PWM_E)DOWN
GPIOY_2(SPI_C_SCLK)DOWN
GPIOY_3(SPI_C_SS0)UP
GPIOY_4(SPI_C_SS1//TSIN_C_SOP//HSYNC)UP
GPIOY_5(SPI_C_SS2//TSIN_C_DIN0//VSYNC)UP
GPIOY_6(UART_E_TX//TSIN_C_CLK)UP
GPIOY_7(UART_E_RX//TSIN_C_VALID)DOWN
GPIOY_8(UART_E_CTS//TSIN_D_SOP//PWM_F)DOWN
GPIOY_9(UART_E_RTS//TSIN_D_DIN0//3D_SYNC_OUT)DOWN
GPIOY_10(UART_D_CTS//TSIN_D_CLK//VX1_A_HTPDN //eDP_A_HPD)UP
GPIOY_11(UART_D_RTS//TSIN_D_VALID//VX1_B_HTPDN //eDP_B_HPD)UP
GPIOY_12(UART_D_TX//VX1_A_LOCKN)UP
GPIOY_13(UART_D_RX//VX1_B_LOCKN)UP
GPIOY_14(PWM_VS)DOWN
GPIOY_15(I2CM_E_SCL)UP
GPIOY_16(I2CM_E_SDA)DOWN
GPIOY_17(I2CM_F_SCL)UP
GPIOY_18(I2CM_F_SDA//PCIECK_REQN)UP
A311D2
BGA_16_1X14_3_B025_0P4
U1I
LIB: 2020-11-24
VDDIO_M
10C9
1uF
C0201
10FB6 NC FB0201 VDDIO_1V8
10FB5 120R/100M FB0201 VDDAO_1V8
L25
VDDAO_1V8
AE25 AVDD18_AUDIO
10C10
0.1uF
C0201
GND_AUDIO
AC31 AU_AIL1
AC33 AU_AIR1
AC32 AU_AIL2
AD32 AU_AIR2
10TP1
LINE_PWR
VCC5V
2 LINEL_OUT AE30 AU_LO1L
1 LINER_OUT AE31 AU_LO1R
10TP2
LINE_OUT
AU_REFP AE28 AU_REFP
AU_VMID AD26 AU_VMID
10C16
4.7uF
C0402
10C17
4.7uF
C0402
AE26 AVSS_AUDIO
10R17
0R
R0201
GND_AUDIO
J31 GPIOM_0(TDM_D12//PDM_DIN1)DOWN
H31 GPIOM_1(TDM_D13//PDM_DIN2)DOWN
J30 GPIOM_2(TDM_D14//PDM_DIN3)DOWN
J32 GPIOM_3(TDM_D15//PDM_DCLK)DOWN
H33 GPIOM_4(TDM_SCLK3//PDM_DIN0)DOWN
H32 GPIOM_5(TDM_FS3//PDM_DIN1)DOWN
G33 GPIOM_6(I2CM_D_SCL)UP
G32 GPIOM_7(I2CM_D_SDA)UP
E27 GPIOM_8(SPI_B_MOSI//UART_D_TX)DOWN
D27 GPIOM_9(SPI_B_MISO//UART_D_RX)DOWN
F32 GPIOM_10(SPI_B_SCLK//UART_D_CTS)DOWN
E31 GPIOM_11(SPI_B_SS0//UART_D_RTS)DOWN
E33 GPIOM_12(SPI_B_SS1//I2CM_C_SCL)UP
E32 GPIOM_13(SPI_B_SS2//I2CM_C_SDA)UP
PDM_DIN3 [10]
PDM_DCLK [10]
CMC_PWRDN [5]
CMA_PWRDN [5]
TP_I2CM_D_SCL [6]
TP_I2CM_D_SDA [6]
TP_INT [6]
TP_RST [6]
CMA_PWR [5]
CMA_RST_L [5]
CMA_I2CM_C_SCL [5]
CMA_I2CM_C_SDA [5]
VDDIO_M
TP_I2CM_D_SCL 10R16 4.7K R0201
TP_I2CM_D_SDA 10R15 4.7K R0201
CMA_I2CM_C_SCL 10R13 4.7K R0201
CMA_I2CM_C_SDA 10R14 4.7K R0201
VDDIO_3V3
10C15
1uF
C0201
VDDIO_T
R25
P32 GPIOT_0(MCLK_1)DOWN
P33 GPIOT_1(TDM_SCLK1)DOWN
N29 GPIOT_2(TDM_FS1)DOWN
N33 GPIOT_3(TDM_D2//SPDIF_IN)DOWN
P31 GPIOT_4(TDM_D3//SPDIF_OUT)DOWN
K30 GPIOT_5(TDM_D4//ISO7816_CLK)DOWN
L33 GPIOT_6(TDM_D5//ISO7816_DATA//SPI_D_MOSI)DOWN
K33 GPIOT_7(TDM_D6//TSIN_A_SOP//SPI_D_MISO)DOWN
K31 GPIOT_8(TDM_D7//TSIN_A_DIN0//SPI_D_SCLK)DOWN
M32 GPIOT_9(TDM_D8//TSIN_A_CLK//SPI_D_SS0)DOWN
N32 GPIOT_10(TDM_D9//TSIN_A_VALID)DOWN
K32 GPIOT_11(TDM_D10)DOWN
J29 GPIOT_12(TDM_D11)DOWN
M28 GPIOT_13(MCLK_2)DOWN
M29 GPIOT_14(TDM_SCLK2)DOWN
J28 GPIOT_15(TDM_FS2)DOWN
K28 GPIOT_16(I2CM_B_SCL)DOWN
K29 GPIOT_17(I2CM_B_SDA)DOWN
N28 GPIOT_18(SPI_A_MOSI)DOWN
L32 GPIOT_19(SPI_A_MISO)DOWN
M30 GPIOT_20(SPI_A_SCLK//I2CM_A_SCL)DOWN
M31 GPIOT_21(SPI_A_SS0//I2CM_A_SDA)DOWN
N31 GPIOT_22(SPI_A_SS1//I2CM_C_SCL)DOWN
N30 GPIOT_23(SPI_A_SS2//I2CM_C_SDA)DOWN
I2S_MCLK1 [10]
I2S_SCLK1 [10]
I2S_LRCLK1 [10]
I2S_SDO1 [10]
I2S_SDI1 [10]
TDM_D4 [9]
TDM_D5 [9]
TDM_D6 [9]
TDM_D7 [9]
TDM_D8 [9]
TDM_D9 [9]
TDM_D10 [9]
MCU_RST_CTRL [2]
I2S_MCLK2 [9]
I2S_SCLK2 [9]
I2S_LRCLK2 [9]
I2CM_B_SCL [9]
I2CM_B_SDA [9]
GPIOT_18 [10]
GPIOT_19 [10]
I2CM_A_SCL [10]
I2CM_A_SDA [10]
VDDIO_3V3
I2CM_B_SCL 10R26 4.7K R0201
I2CM_B_SDA 10R25 4.7K R0201
I2CM_A_SCL 10R22 4.7K R0201
I2CM_A_SDA 10R21 4.7K R0201
VDDIO_3V3
PANEL_B_I2C_E_SCL 10R7 4.7K R0201
PANEL_B_I2C_E_SDA 10R6 4.7K R0201
I2CM_F_SDA 10R5 4.7K R0201
I2CM_F_SCL 10R4 4.7K R0201
A311D2
BGA_16_1X14_3_B025_0P4
GPIO Header
10J1
40P_H_SMT
VCC5V
[9] HUB_DM4
[9] HUB_DP4
VCC_MCU
[2] MCU_SWCLK
[2] MCU_SWDIO
[2] ADC_CH6
VDDAO_1V8
[2] ADC_CH3
[2] SPDIF_OUT
[10] UART_E_RX
[10] UART_E_TX
[2,10] Linux_RX
[2,10] Linux_TX
VDDIO_3V3
5V_1
5V_2
USB_DM
USB_DP
GND1
MCU_3V3
MCU_NRST
MCU_SWIM
GND2
ADC0
1V8
ADC1
SPDIF
GND3
UART0_RX
UART0_TX
GND4
UART1_RX
UART1_TX
3V3_1
GND9
I2C0_SCK
I2C0_SDA
GND8
I2C1_SCK
I2C1_SDA
3V3_2
GND7
I2S_SCLK
I2S_MCLK
I2S_SDO
I2S_LRCK
I2S_SDI
GND6
PWM/IO7
IO6
IO5
MCU_IO/IO4
IO3
GND5
I2CM_F_SCL [10]
I2CM_F_SDA [10]
I2CM_A_SCL [10]
I2CM_A_SDA [10]
VDDAO_3V3
I2S_SCLK1 [10]
I2S_MCLK1 [10]
I2S_SDO1 [10]
I2S_LRCLK1 [10]
I2S_SDI1 [10]
PWM_F [10]
GPIOT_18 [10]
GPIOT_19 [10]
PWR_HOLD_EXT [2]
GPIOD_5/IR_IN [2]
40_HEADER
VCC5V
VCC_MCU
10C22 10uF C0402
10C23 0.1uF C0201
10C29 0.1uF C0201
VDDAO_3V3
VDDAO_1V8
10C24 10uF C0402
10C25 0.1uF C0201
10C28 0.1uF C0201
VDDIO_3V3
10C27 10uF C0402
10C26 0.1uF C0201
[2,10] Linux_RX
[2,10] Linux_TX
10ED1 ESD0402 AZ5725-01F
10ED2 ESD0402 AZ5725-01F
PIN | VIM1 | New VIM1 | VIM2 | VIM3 | VIM4
6 | VCC5V | VCC5V | GPIO0V_21 | VCC_MCU | VCC_MCU
7 | HUB_DM2 | HUB_DM2 | GPIO0V_22 | MCU_NRST | MCU_SWCLK
8 | HUB_DP2 | HUB_DP2 | GPIO0V_23 | MCU_SWIM | MCU_SWDIO
11 | GND | GND | VCC1V8 | VDD_AO18 | VDDAO_1V8
38 | PWR_EN | MCU_PA1 | MCU_PA1 | MCU_PA1 | PWR_Hold
39 | PWM_F | PWM_F | GPIO0V_13 | GPIOZ_15 | IRIN
VIM4 SPI:
PIN25: I2CM_A_SCL/SPI_A_SCLK
PIN26: I2CM_A_SDA/SPI_A_SS0
PIN36: GPIOT_18/SPI_A_MOSI
PIN37: GPIOT_19/SPI_A_MISO
Tips: Float PIN6 & 11 to develop
all VIMs compatible expand board.
Check the Tone Board for reference.
DMIC
VDDAO_1V8
10FB8 120R/100M FB0201
DMIC_VDD
10C19 10uF C0402
10C18 0.1uF C0201
10C20 10uF C0402
10C21 0.1uF C0201
10U2
MSM261D3526H1CPM
DMIC_3526
DMIC_VDD
[10] PDM_DCLK
[10] PDM_DIN3
VDD
CLK
DATA
G2
L/R
G1
10U3
MSM261D3526H1CPM
DMIC_3526
DMIC_VDD
[10] PDM_DCLK
[10] PDM_DIN3
G-sensor
[2,9] I2CM_AO_SCL
[2,9] I2CM_AO_SDA
[10] GSENSOR_INT
SCL
SDA
INT
ADDR
10U1
VDDAO_3V3
IO_VDD1
IO_VDD2
VDD1
VDD2
RES
GND1
GND2
GND3
10C5 0.1uF C0201
10C6 0.1uF C0201
KXTJ3-1057
LGA12_2X2
Addr: 0x0E
FAN
VCC5V
10C1 10uF C0402
10C2 0.1uF C0201
10CON1
S1
S2
VCC
PWM
GND
FG
10R3 0R R0201
FAN_PWM [2]
HDR_4P
BM04B-SURS-TF
Shenzhen Wesion Technology Co., Ltd.
Project: VIM4
File: GPIO/FAN/Sensor/DMIC
Date: Monday, November 21, 2022
Rev: V13
Designed_by: Totti
Sheet: 10



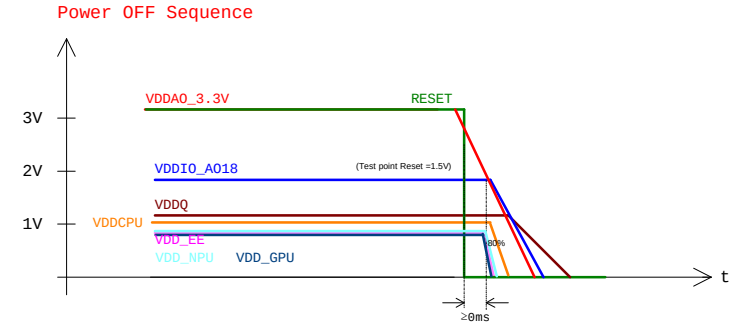
Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	DVSS		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	11

Power Tree:



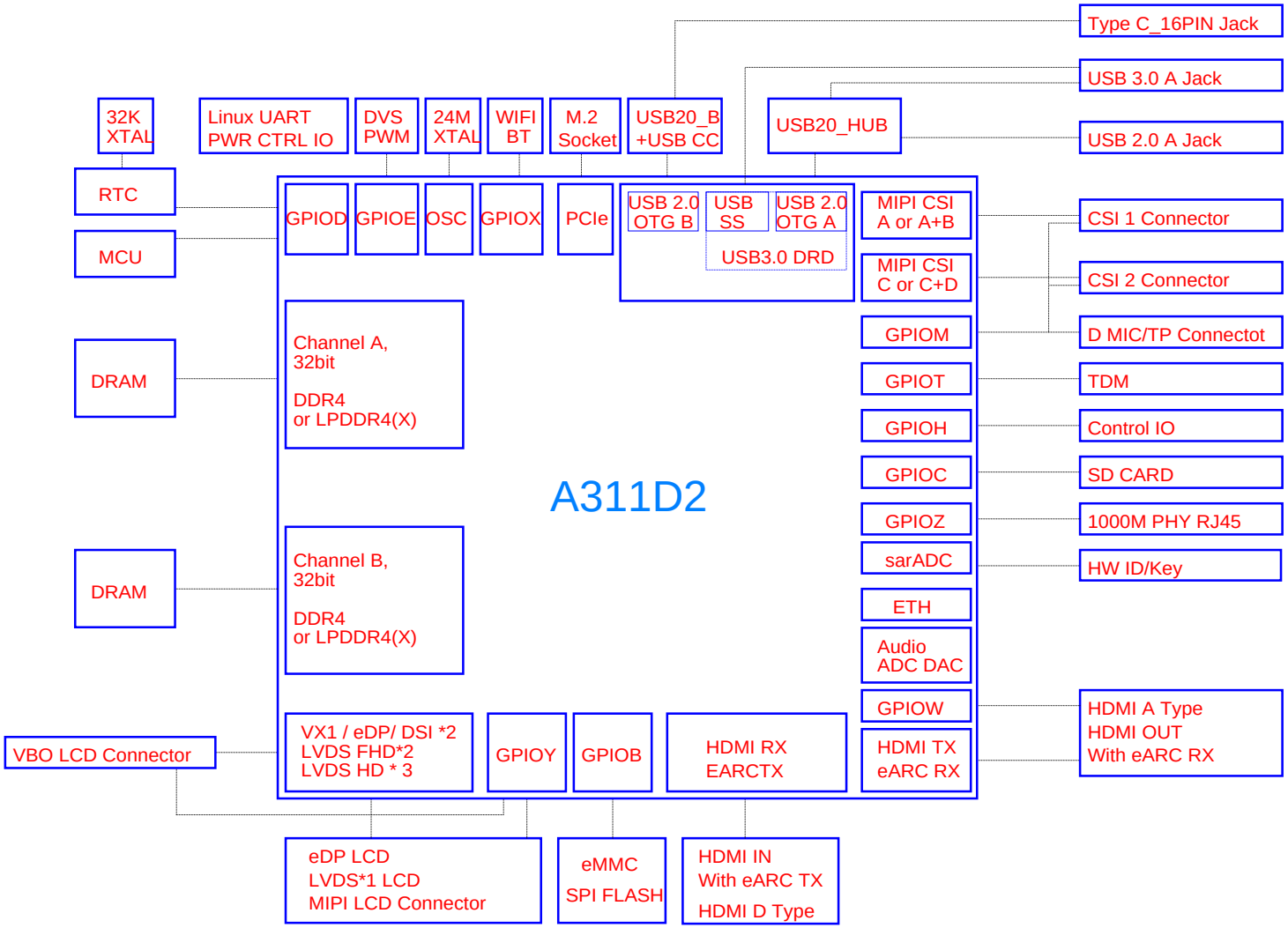


1) All test values refer to 80% of typical power voltage.
2) VDDAO_3.3V & VCC3.3V should ramp up > 0.5ms later than VDD_EE.
3) All power sources should get stable within 20ms (except VDDQ,VDD_QLP).
4) No sequence requirement between VDD18_AO and VDD_EE.
No sequence requirement between VDDCPU_A & VDDCPU_B & VDD_NPU & VDD_GPU & VDDQ
& VDD_QLP & VDD_DDR and other power source.
5) VDDIO_AO18 should ramps up earlier or at the same time with VDDAO_3.3V & VCC3.3V,
VDDAO_3.3V & VCC3.3V should never be 2.5V higher than VDD18_AO.
6) RESET_n should keep low for at least 40ms after power up (except VDDQ,VDD_QLP).



A reset IC should monitor VDDIO3.3V, output lower (lower than 1.5V) before other power rails turning off.
There is no power off sequence requirement between other power rails.

Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	POWER TREE		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Totti	Sheet:	12



Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	BLOCK		
Date:	Monday, November 21, 2022	Rev:	V13
Designed_by:	Tobi	Sheet:	13