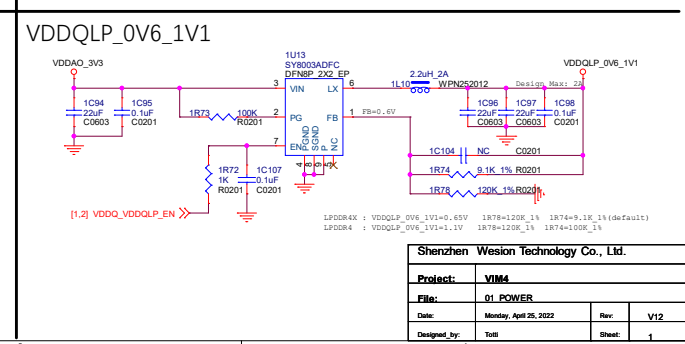
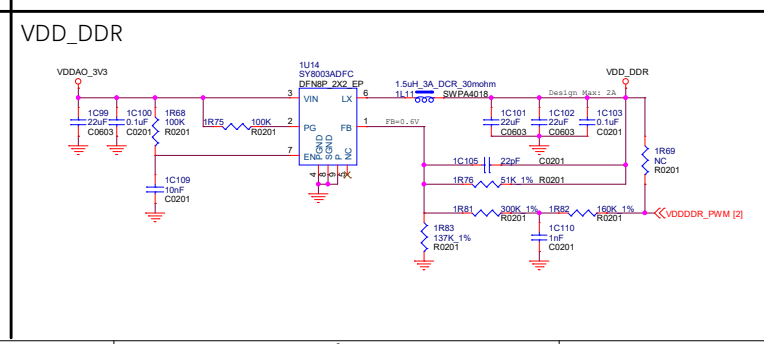
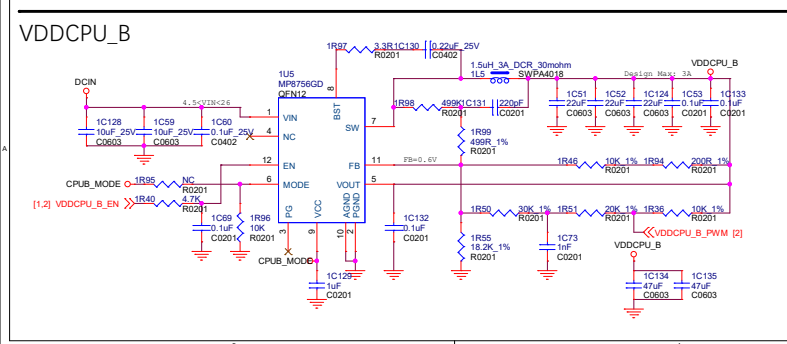
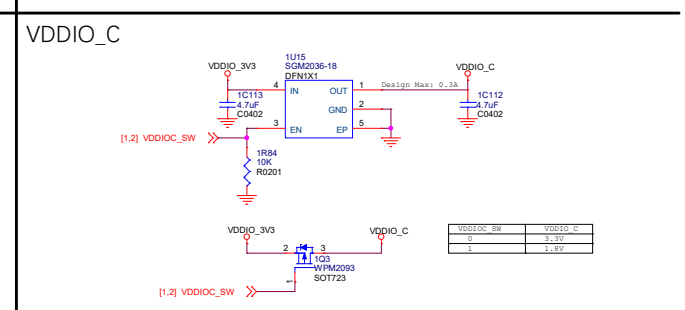
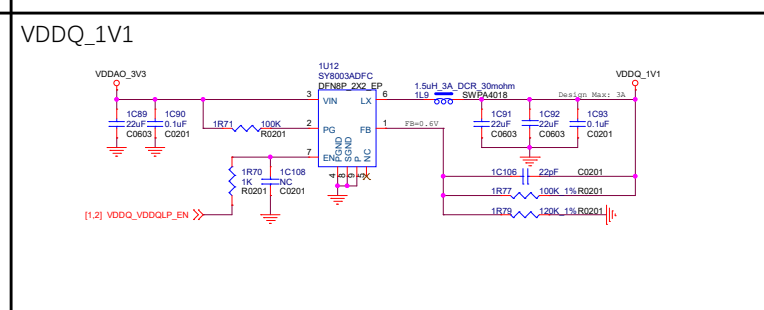
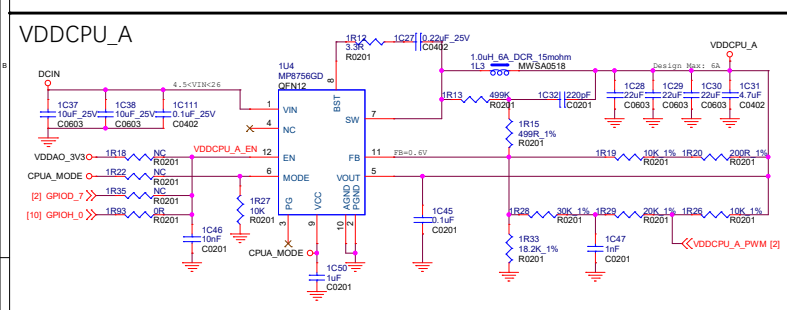
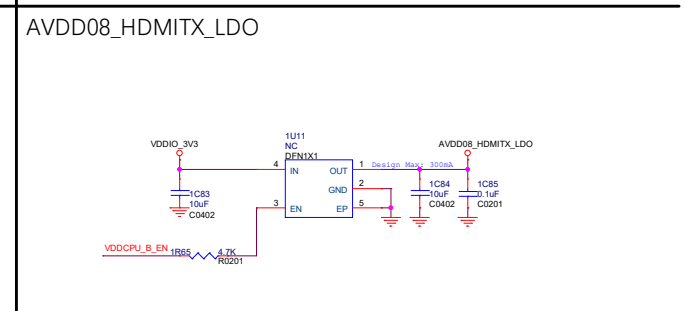
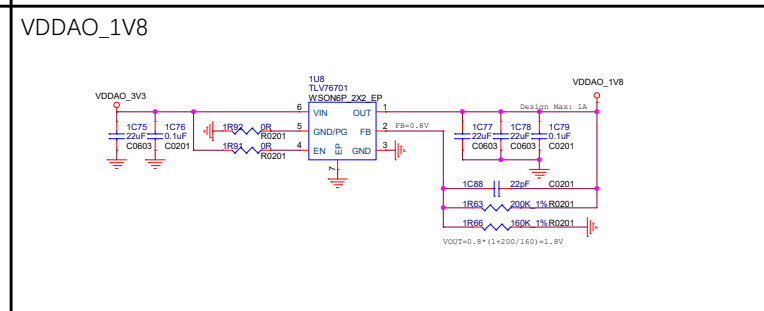
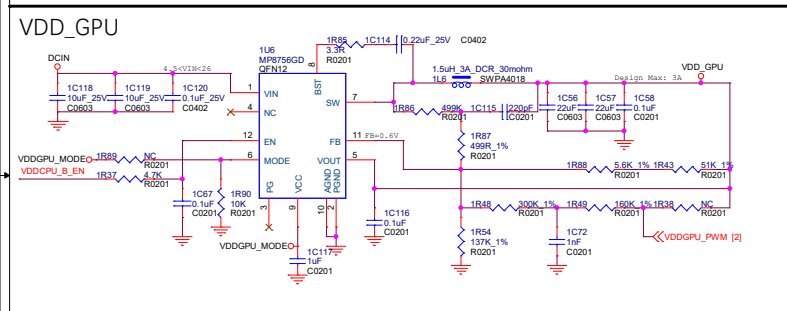
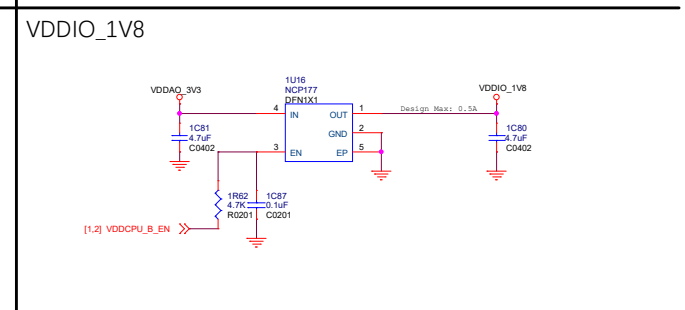
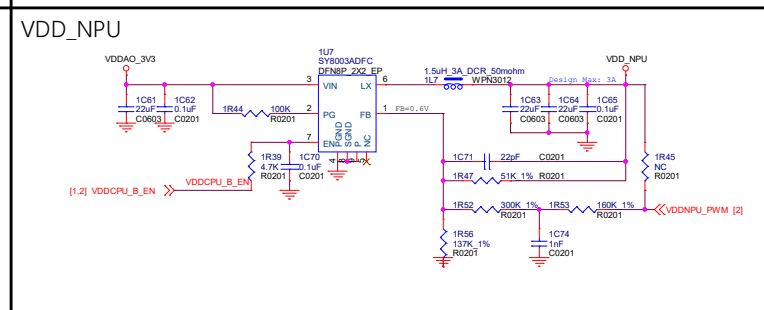
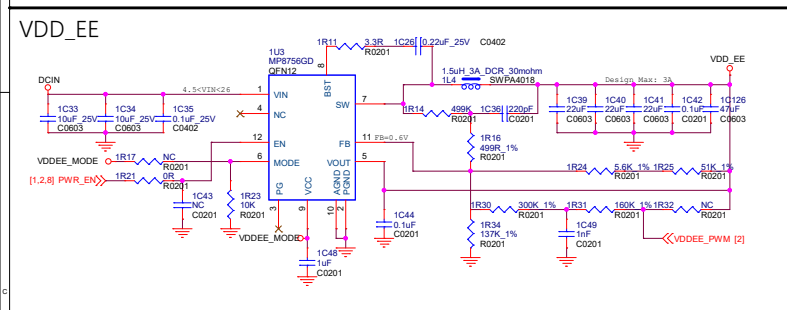
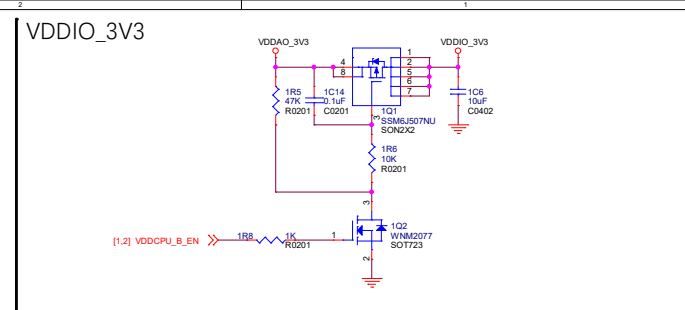
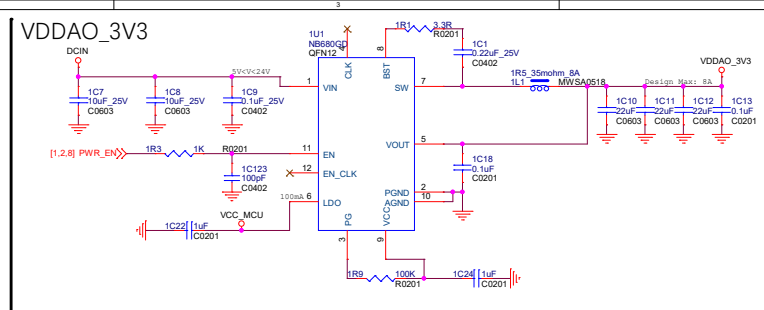
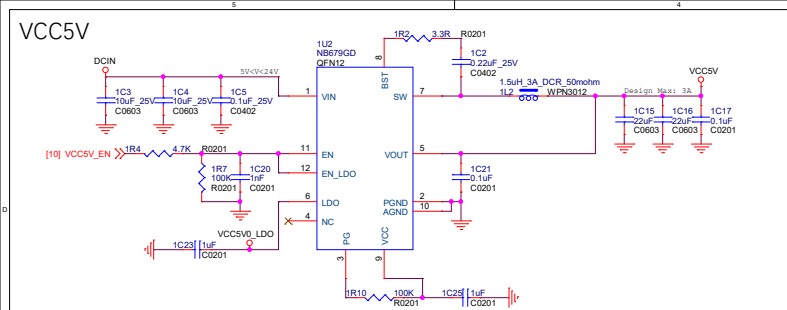
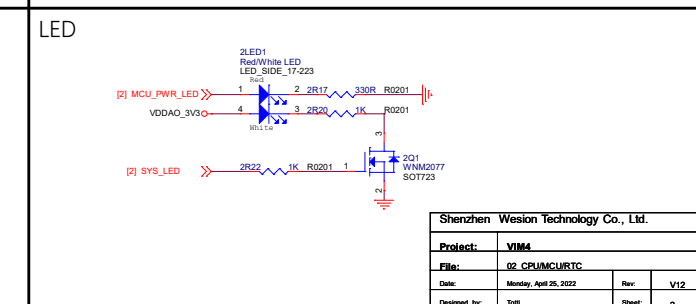
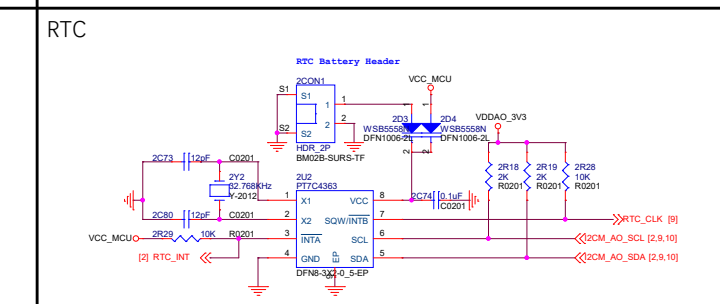
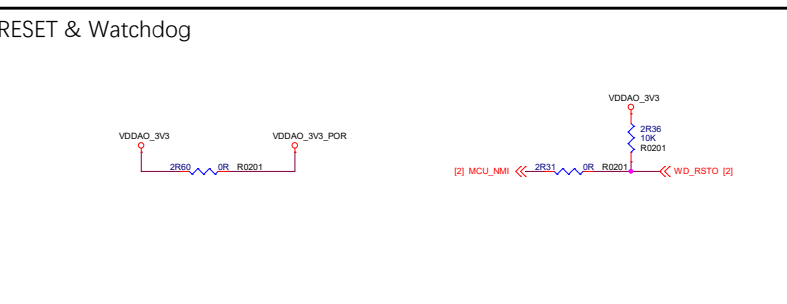
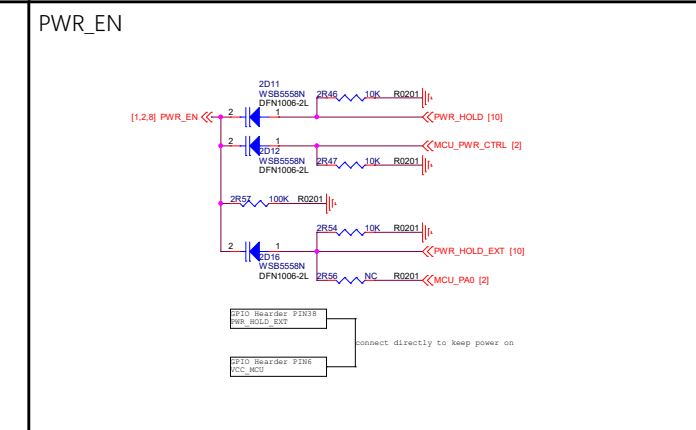
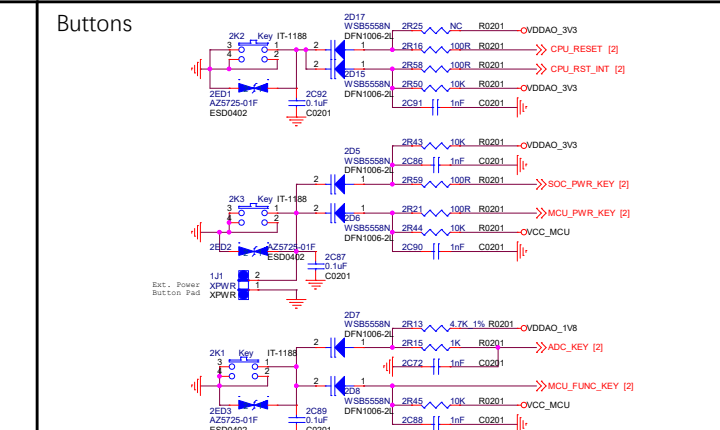
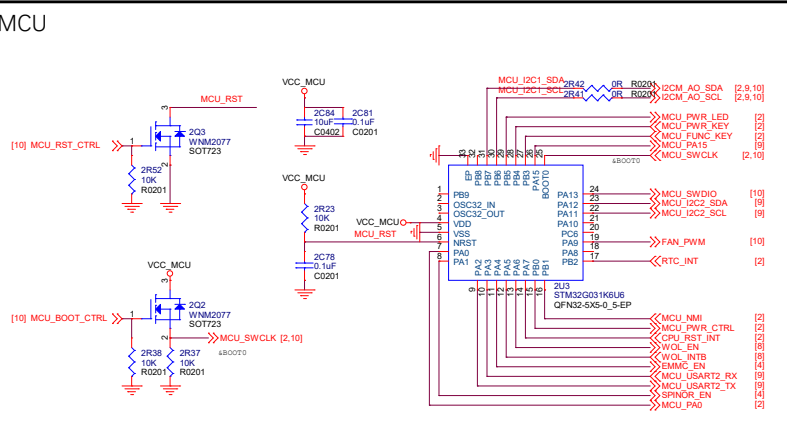
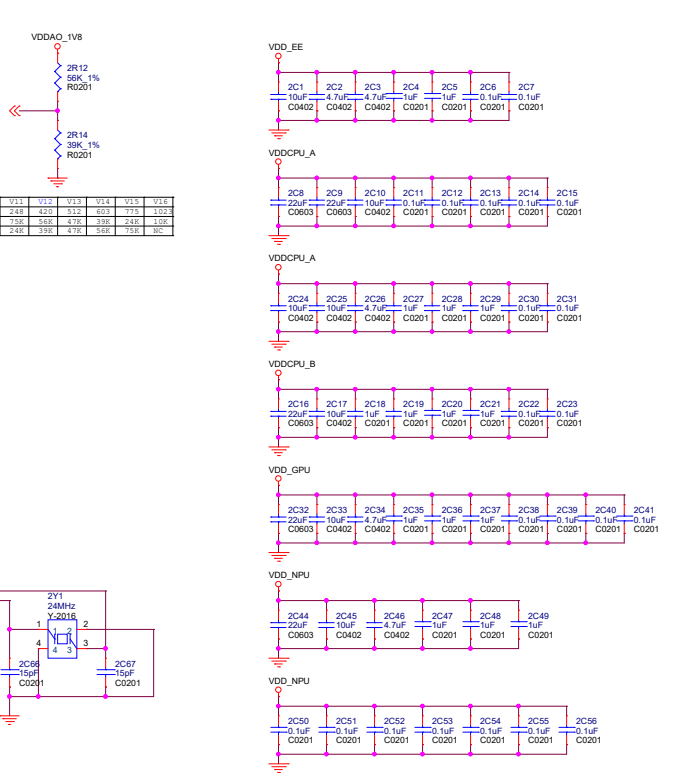
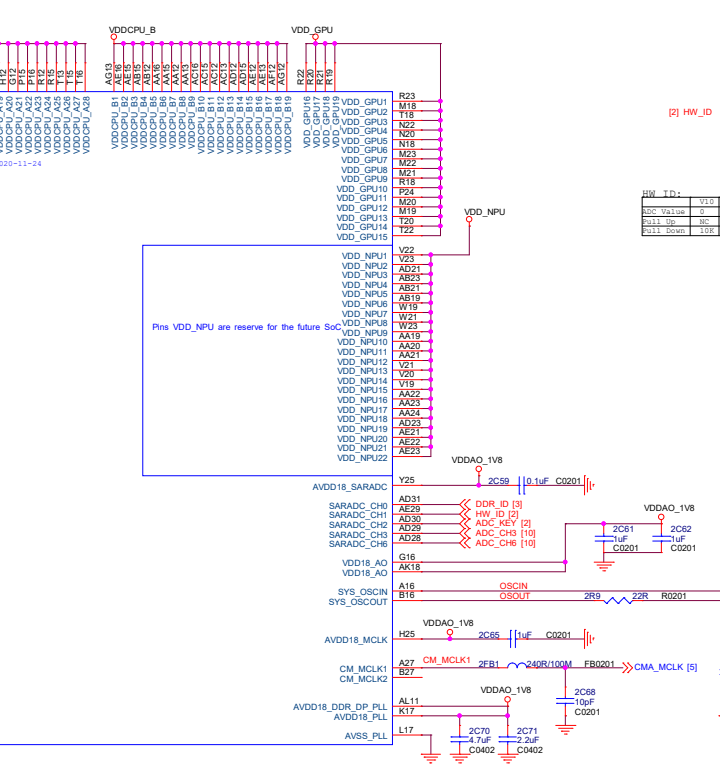
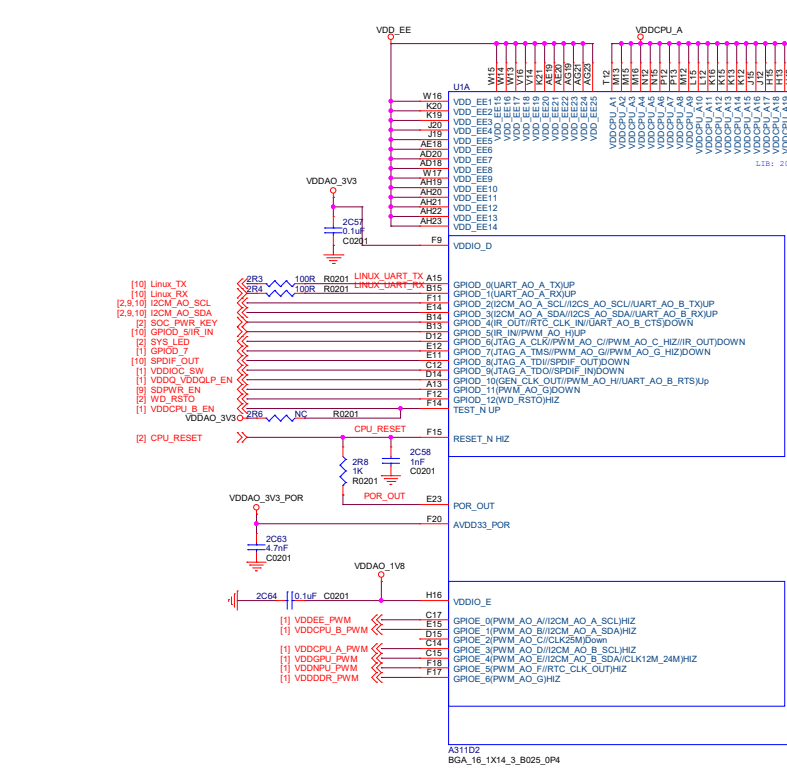


KHADASS

Something a little different.

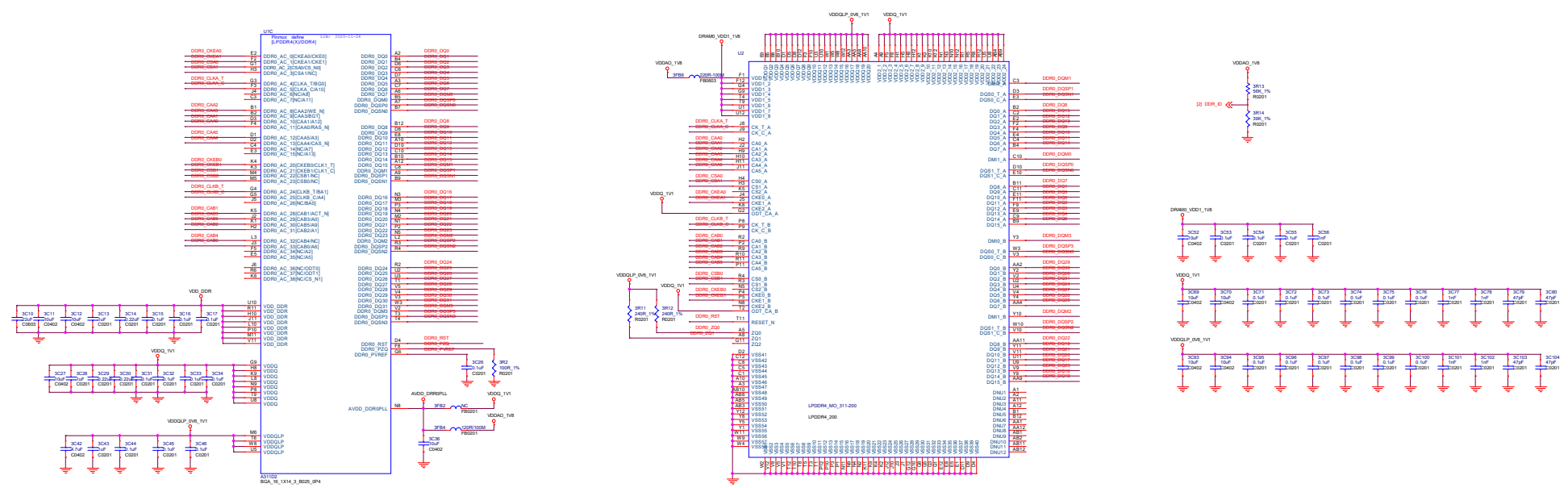
Shenzhen Wesion Technology Co., Ltd.			
<b>Project:</b>	VIM4		
<b>File:</b>	14 Khadas		
<b>Date:</b>	Thursday, April 07, 2022	<b>Rev:</b>	V12
<b>Designed_by:</b>	Totti	<b>Sheet:</b>	0



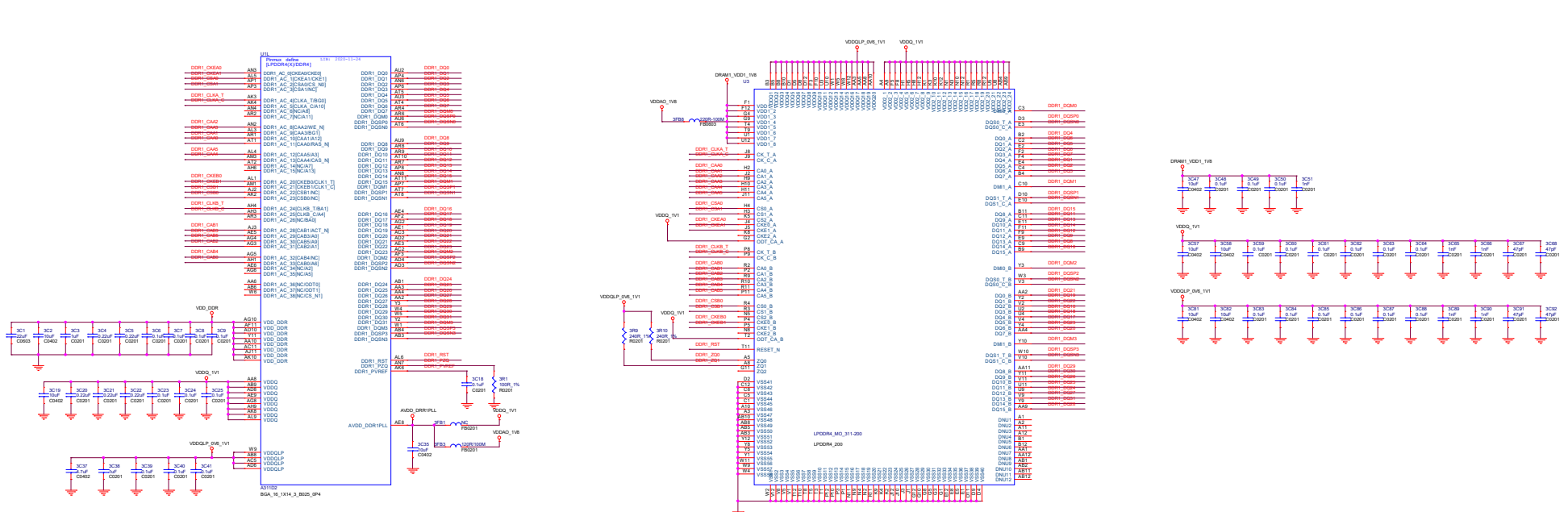


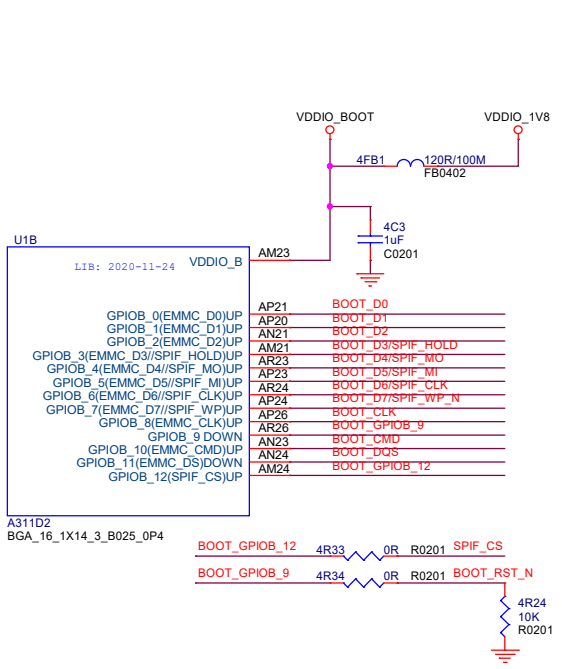
Shenzhen Weson Technology Co., Ltd.			
Project:	VIMS4	Rev:	V12
File:	02_CPU/MCUTCRC	Date:	Monday, April 25, 2022
Designed_by:	TSL	Checked:	2

DDR Channel 0

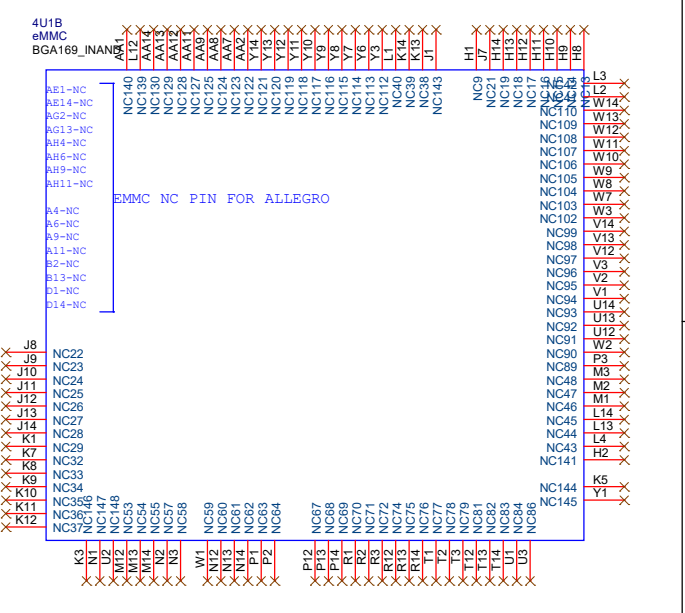
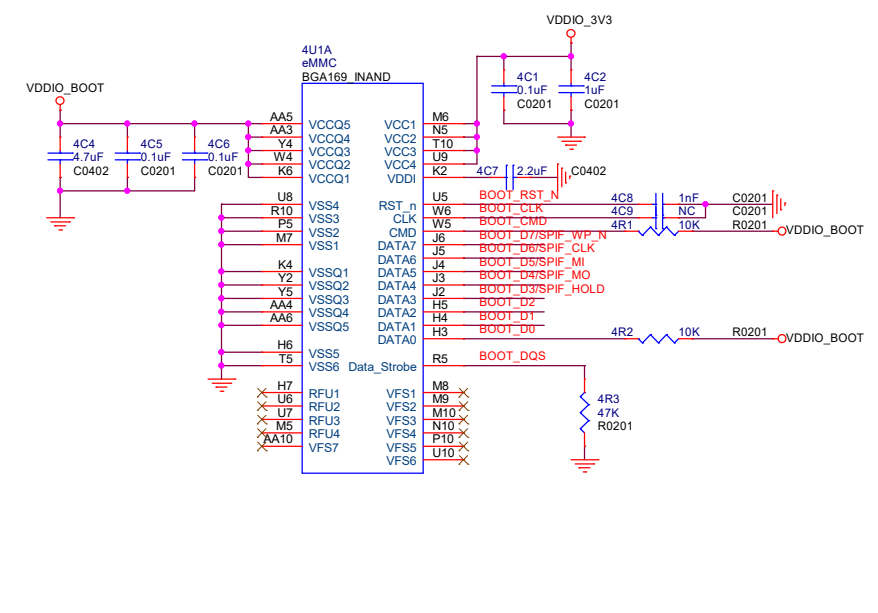


DDR Channel 1

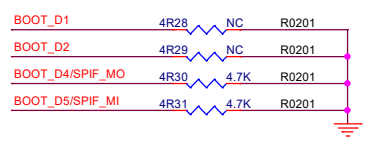




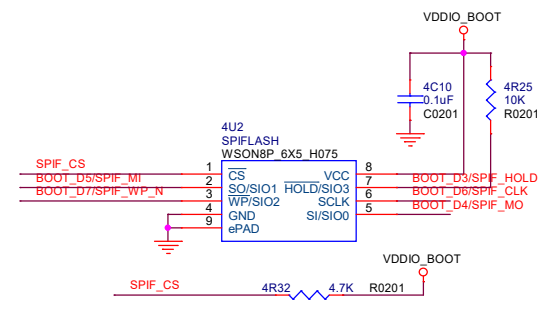
### EMMC



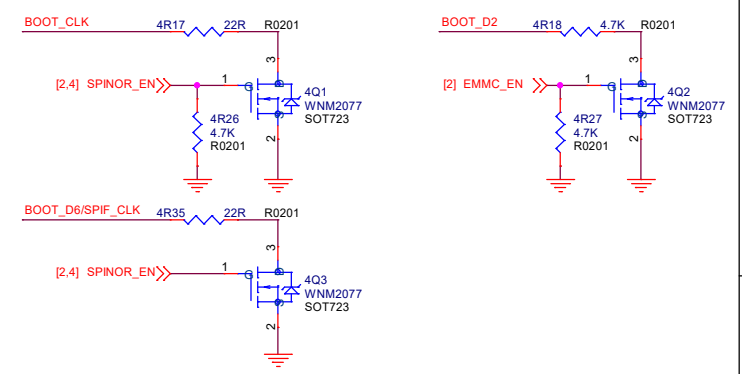
### Power ON Config



### SPI Flash

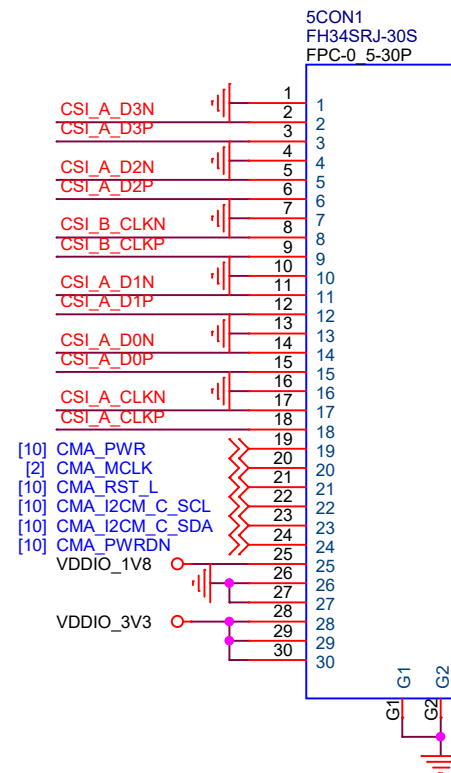
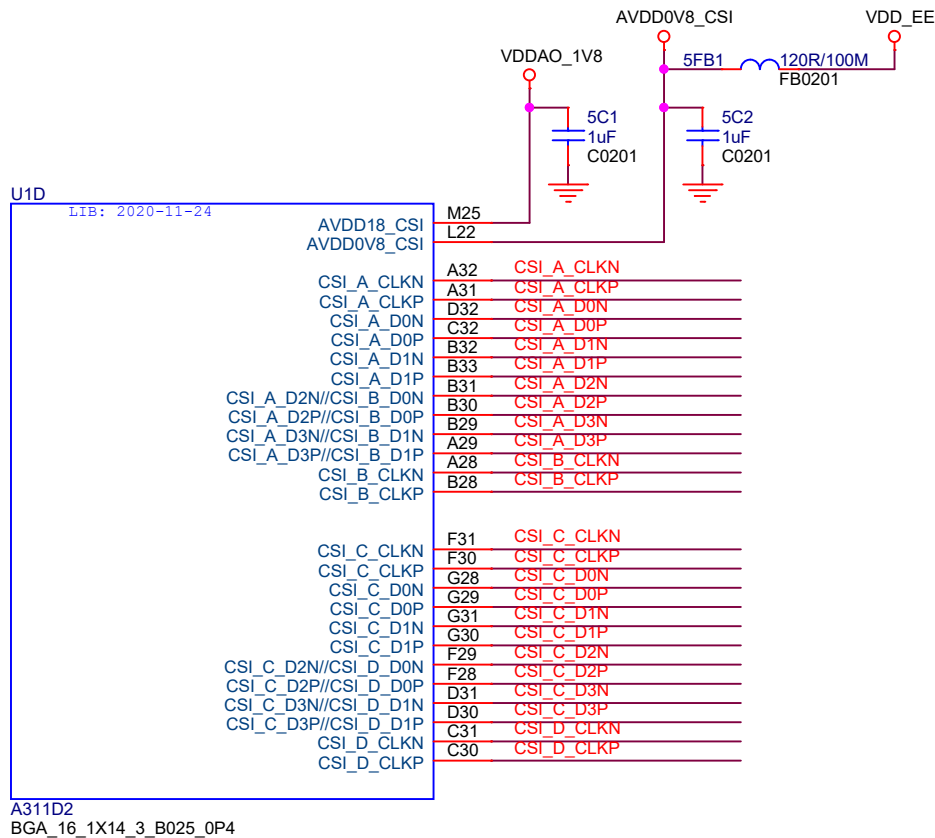


### TST

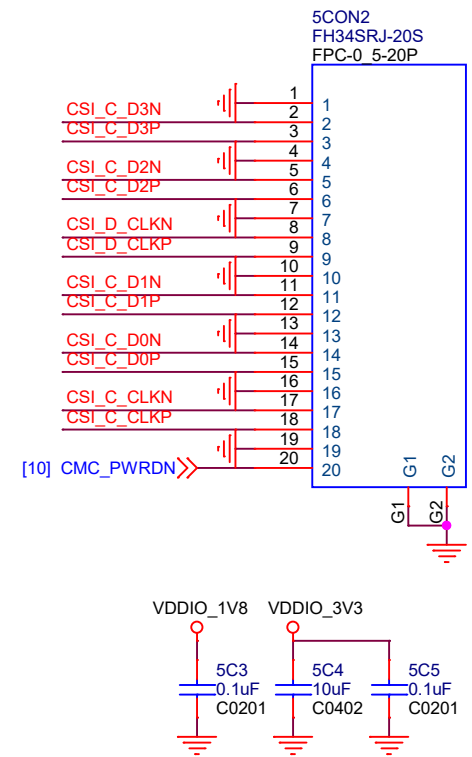


Booting Sequence Diagram

EMMC EN	SPINOR EN	1st Boot	2nd Boot	3rd Boot	4th Boot
0	0	SD Card	eMMC	SPI Flash	USB
1	0	SD Card	SPI Flash	eMMC	USB
x	1	USB	SPI Flash	eMMC	USB

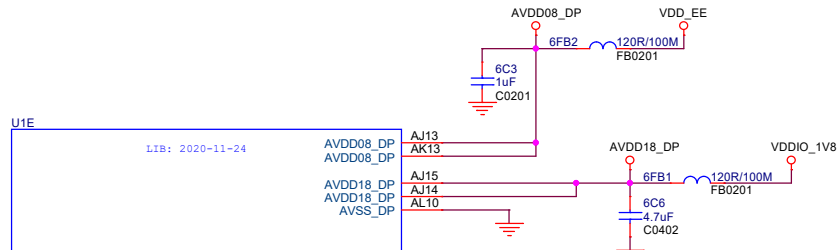


MIPI-CSI1



MIPI-CSI2

Shenzhen Wesion Technology Co., Ltd.			
<b>Project:</b>	VIM4		
<b>File:</b>	05 CSI CAMERA		
<b>Date:</b>	Monday, April 25, 2022	<b>Rev:</b>	V12
<b>Designed_by:</b>	Totti	<b>Sheet:</b>	5



LIB: 2020-11-24

DIF_CH0(EDP_A_AUXN/DSI_A_D0N/LVDS_A_0N/IX1_A_0N)	AM18	MIPI_DSI_D0N	6TP1	1P	TP-0_5FPC_PIN
DIF_CH0(EDP_A_AUXP/DSI_A_D0P/LVDS_A_0P/IX1_A_0P)	AN18	MIPI_DSI_D0P	6TP2	1P	TP-0_5FPC_PIN
DIF_CH1(EDP_A_0N/DSI_A_D1N/LVDS_A_1N/IX1_A_1N)	AP18	MIPI_DSI_D1P	6TP3	1P	TP-0_5FPC_PIN
DIF_CH1(EDP_A_0P/DSI_A_D1P/LVDS_A_1P/IX1_A_1P)	AU19	MIPI_DSI_CLKN	6TP4	1P	TP-0_5FPC_PIN
DIF_CH2(EDP_A_1N/DSI_A_CKN/LVDS_A_2N/IX1_A_2N)	AT19	MIPI_DSI_CLKP	6TP5	1P	TP-0_5FPC_PIN
DIF_CH2(EDP_A_1P/DSI_A_CKP/LVDS_A_2P/IX1_A_2P)	AR17	MIPI_DSI_D2P	6TP6	1P	TP-0_5FPC_PIN
DIF_CH3(EDP_A_2N/DSI_A_D2N/LVDS_A_3N/IX1_A_3N)	AP17	MIPI_DSI_D2N			
DIF_CH3(EDP_A_2P/DSI_A_D2P/LVDS_A_3P/IX1_A_3P)	AU18	MIPI_DSI_D3N			
DIF_CH4(EDP_A_3N/DSI_A_D3N/LVDS_A_3N/IX1_A_4N)	AT18	MIPI_DSI_D3P			
DIF_CH4(EDP_A_3P/DSI_A_D3P/LVDS_A_3P/IX1_A_4P)					
DIF_CH5(LVDS_B_0N/IX1_A_5N)	AM15	LVDS_B_0N	6TP1	1P	TP-0_5FPC_PIN
DIF_CH5(LVDS_B_0P/IX1_A_5P)	AN15	LVDS_B_0P	6TP2	1P	TP-0_5FPC_PIN
DIF_CH6(LVDS_B_1N/IX1_A_6N)	AT17	LVDS_B_1N	6TP3	1P	TP-0_5FPC_PIN
DIF_CH6(LVDS_B_1P/IX1_A_6P)	AP16	LVDS_B_2N	6TP4	1P	TP-0_5FPC_PIN
DIF_CH7(LVDS_B_2N/IX1_A_7N)	AP15	LVDS_B_2P	6TP5	1P	TP-0_5FPC_PIN
DIF_CH7(LVDS_B_2P/IX1_A_7P)	AU16	VX1_B_D0N	6TP6	1P	TP-0_5FPC_PIN
DIF_CH8(EDP_B_AUXN/DSI_B_D0N/LVDS_B_CLKN/IX1_B_0N)	AU15	VX1_B_D0P			
DIF_CH8(EDP_B_AUXP/DSI_B_D0P/LVDS_B_CLKP/IX1_B_0P)	AR14	VX1_B_D1N			
DIF_CH9(EDP_B_0N/DSI_B_D1N/LVDS_B_3N/IX1_B_1N)	AP14	VX1_B_D1P			
DIF_CH9(EDP_B_0P/DSI_B_D1P/LVDS_B_3P/IX1_B_1P)					
DIF_CH10(EDP_B_1N/DSI_B_CKN/LVDS_C_0N/IX1_B_2N)	AT15	VX1_B_D2N			
DIF_CH10(EDP_B_1P/DSI_B_CKP/LVDS_C_0P/IX1_B_2P)	AT14	VX1_B_D2P			
DIF_CH11(EDP_B_2N/DSI_B_D2N/LVDS_C_1N/IX1_B_3N)	AT13	VX1_B_D3N			
DIF_CH11(EDP_B_2P/DSI_B_D2P/LVDS_C_1P/IX1_B_3P)	AU13	VX1_B_D3P			
DIF_CH12(EDP_B_3N/DSI_B_D3N/LVDS_C_2N/IX1_B_4N)	AN12	VX1_B_D4N			
DIF_CH12(EDP_B_3P/DSI_B_D3P/LVDS_C_2P/IX1_B_4P)	AM12	VX1_B_D4P			
DIF_CH13(LVDS_C_CLKN/IX1_B_5N)	AP12	VX1_B_D5N			
DIF_CH13(LVDS_C_CLKP/IX1_B_5P)	AR12	VX1_B_D5P			
DIF_CH14(LVDS_C_3N/IX1_B_6N)	AP11	VX1_B_D6N			
DIF_CH14(LVDS_C_3P/IX1_B_6P)	AR11	VX1_B_D6P			
DIF_CH15(VX1_B_7N)	AN11	VX1_B_D7N			
DIF_CH15(VX1_B_7P)	AN10	VX1_B_D7P			

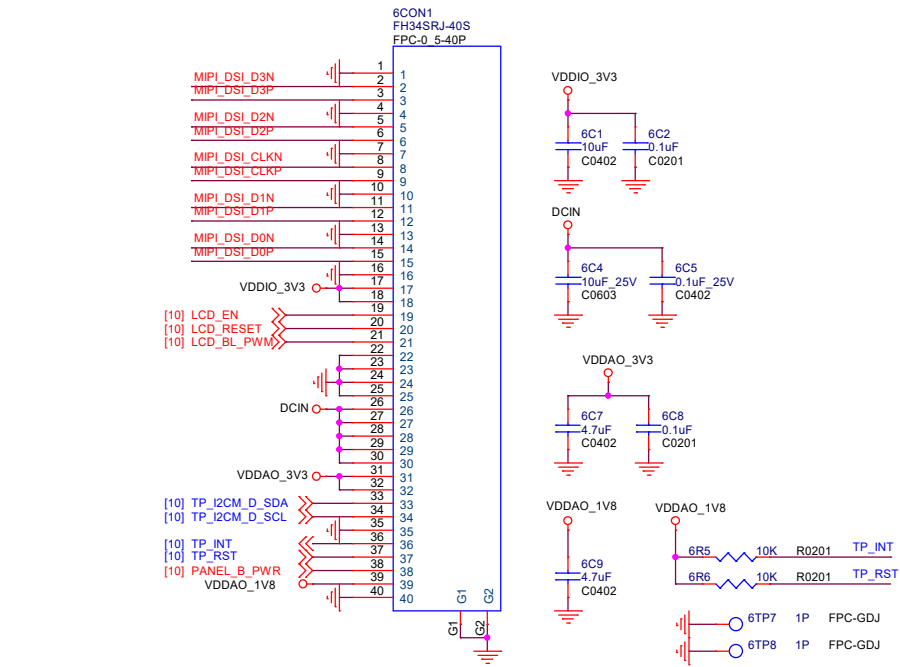
LVDS. To support FHD, must use LVDS B and C

For all of these 4 ports eDP, MIPI DSI, LVDS, VX1, DIF\_REXT terminal resistor connecting DIF\_REXT to GND is required

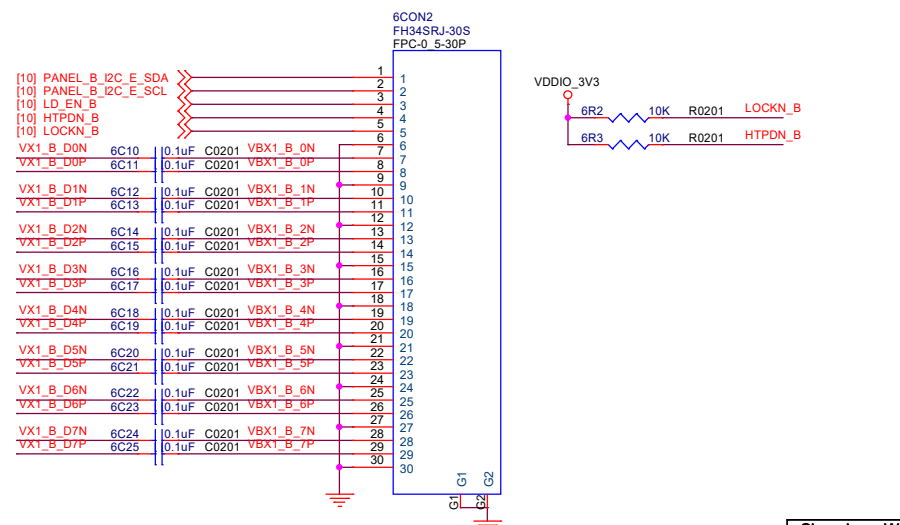
VX1\_LPP VX1\_LPN VX1\_ATP

Pin VX1\_LPP, VX1\_LPN and VX1\_ATP only for Test

A311D2  
BGA\_16\_1X14\_3\_B025\_0P4

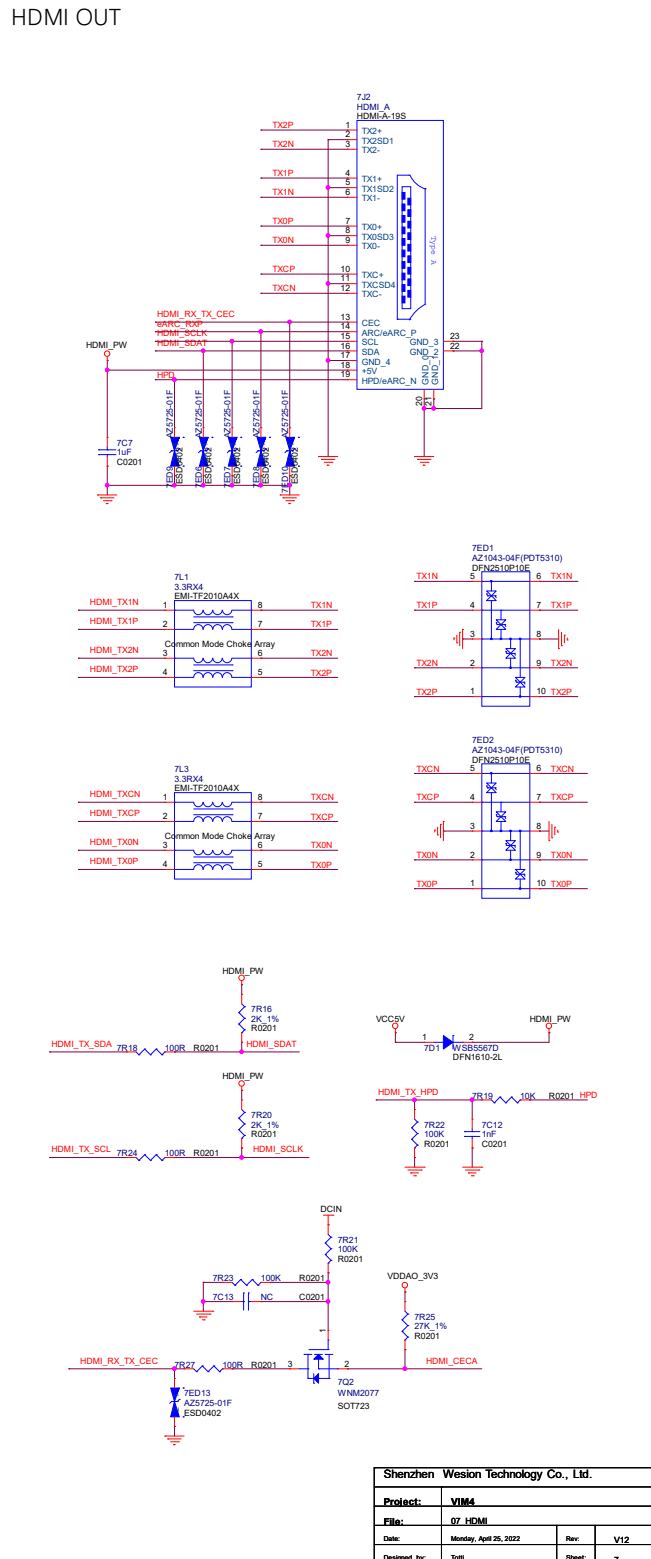
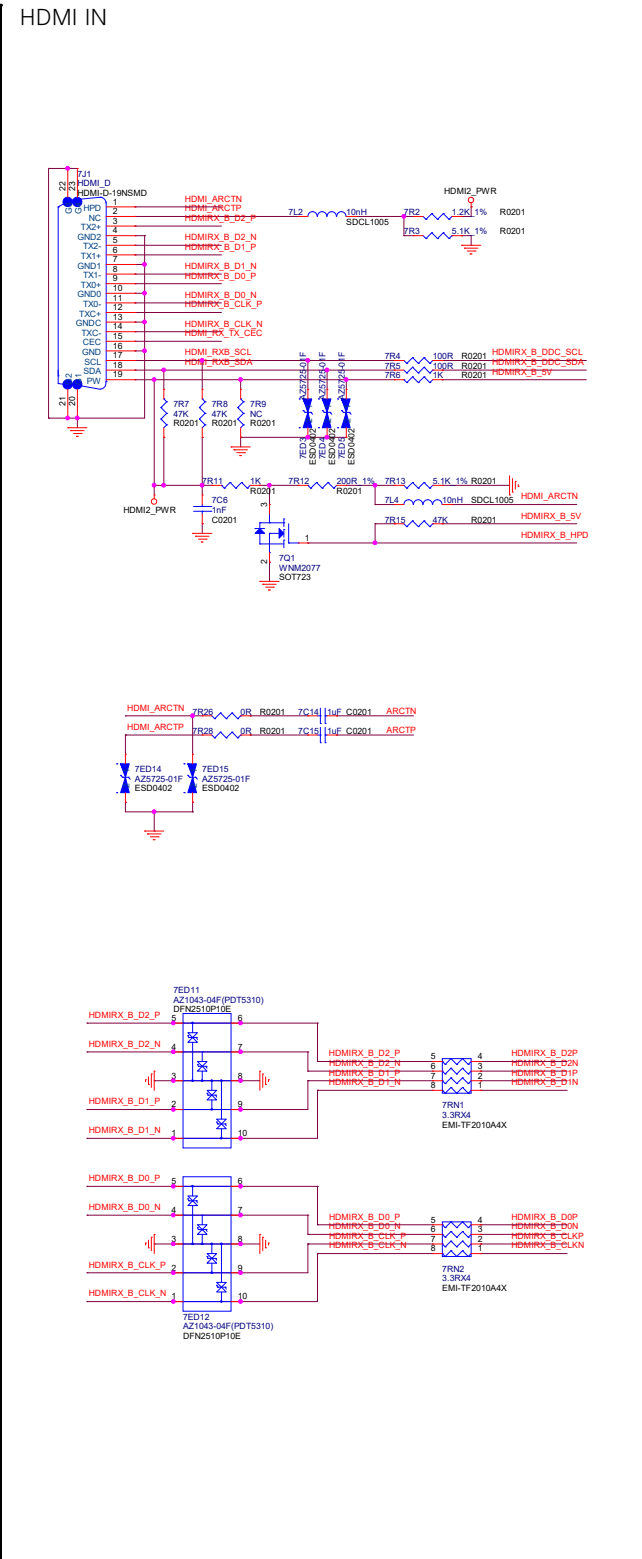
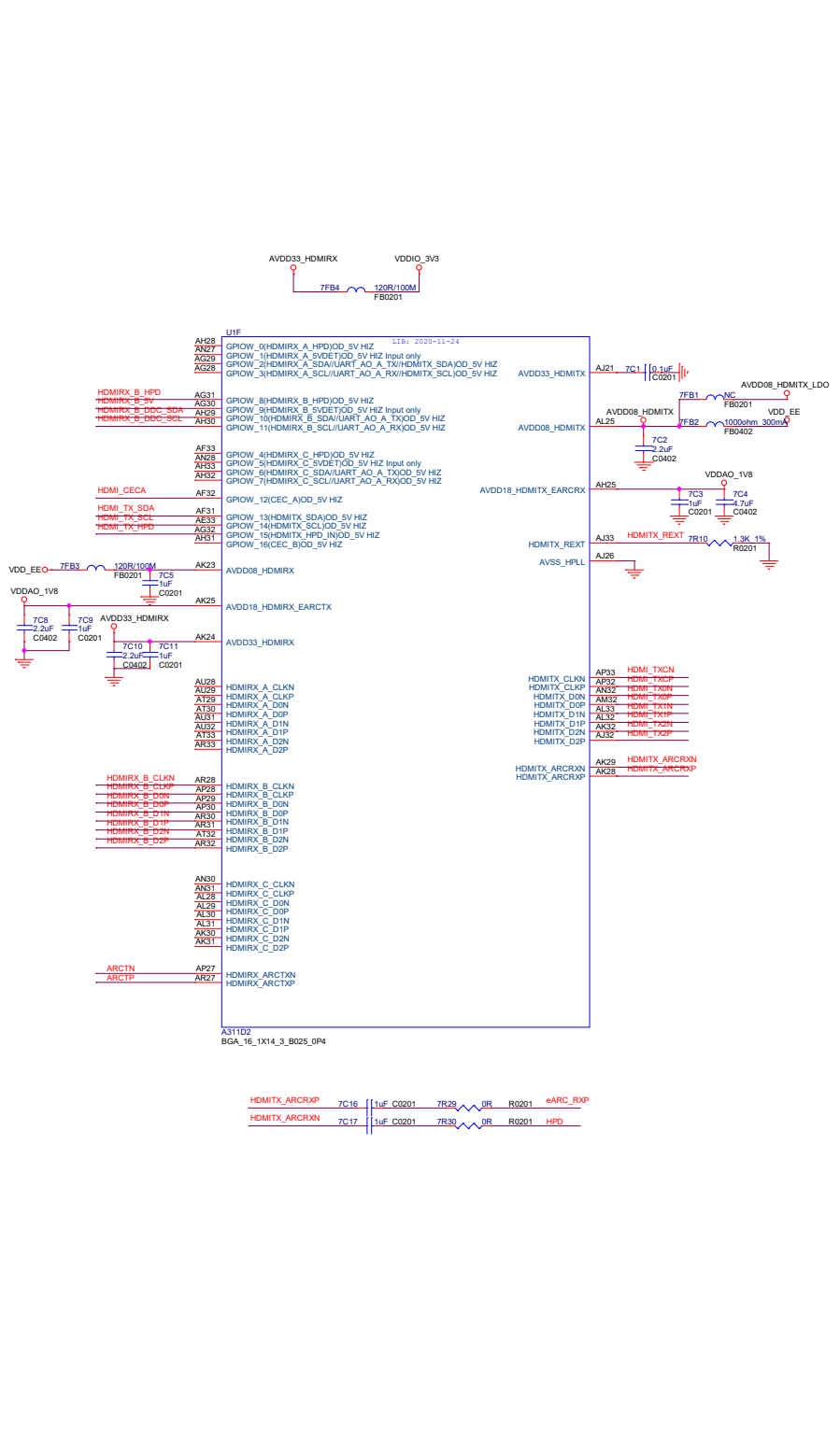


### MIPI-DSI



### VBO / DSI

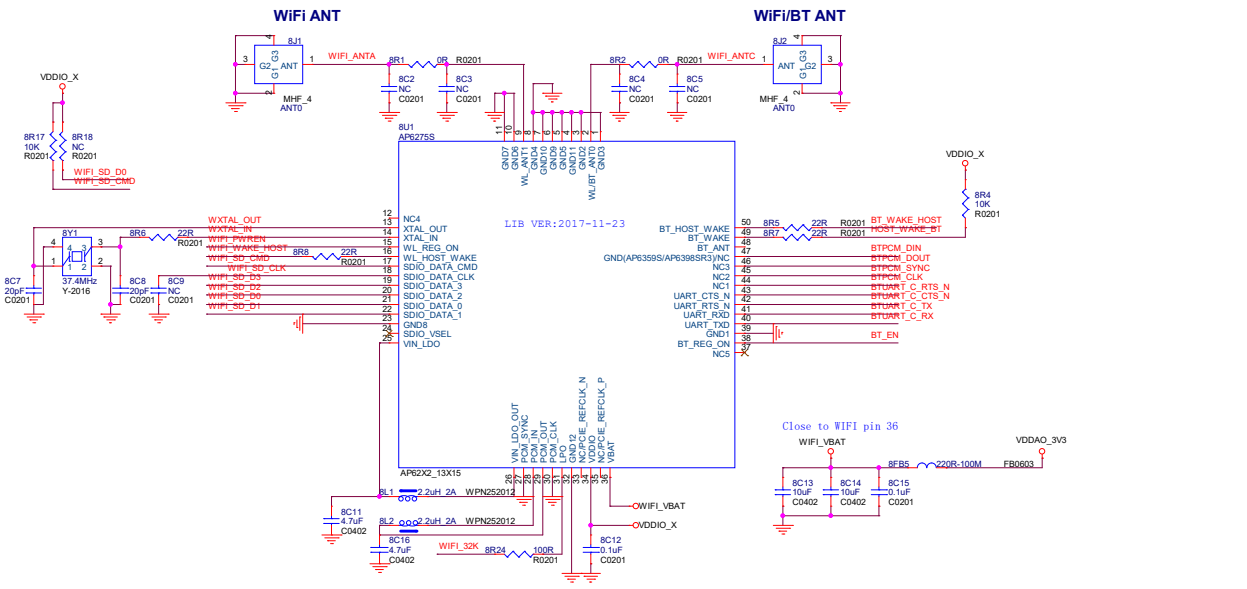
Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	06_DSI/eDPI/LVDS/VX1		
Date:	Monday, April 25, 2022	Rev:	V12
Designed_by:	Totti	Sheet:	6



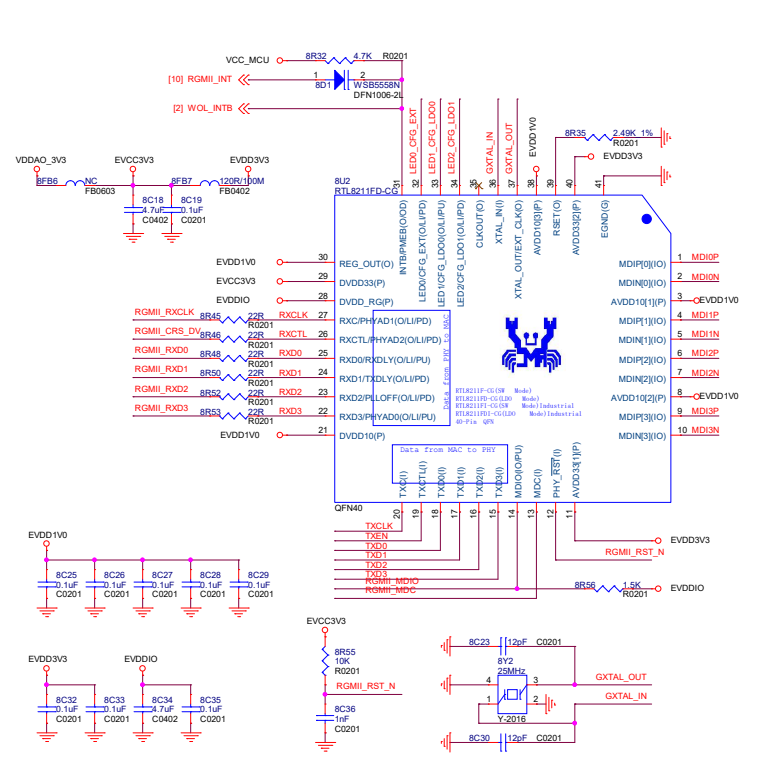




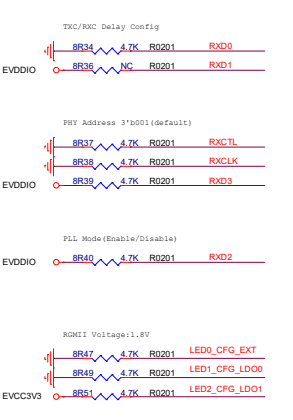
### Wi-Fi & BT



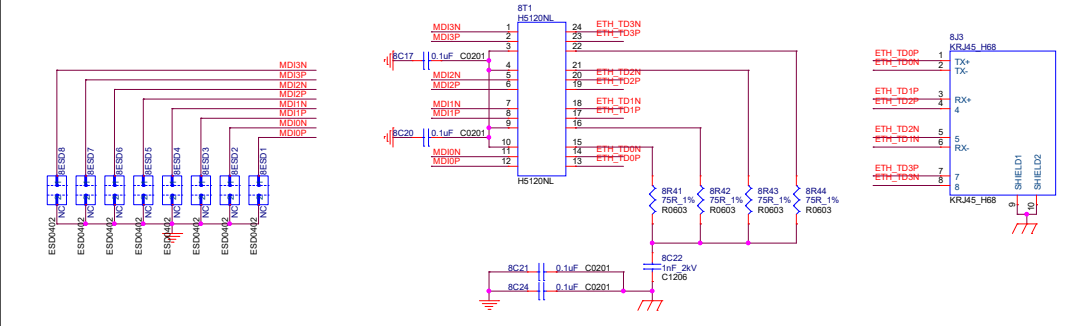
### Ethernet



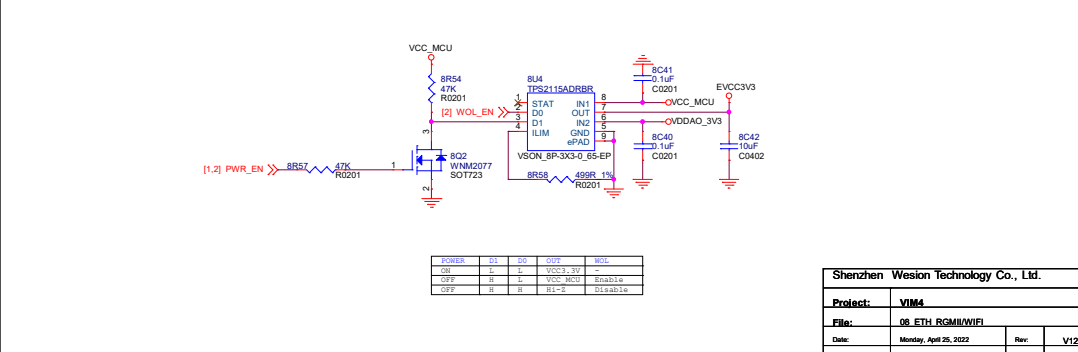
### Configuration

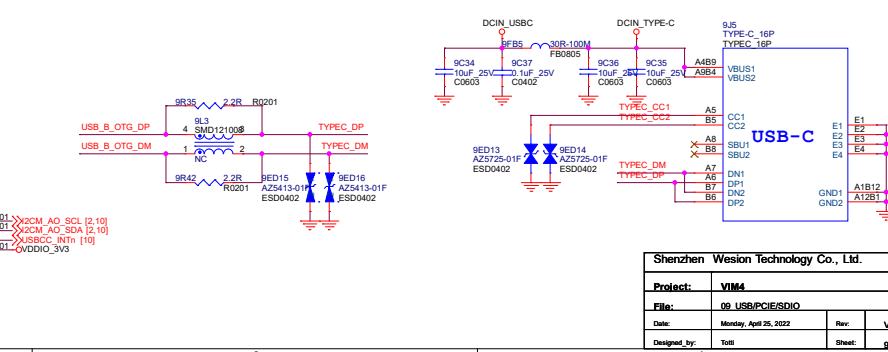
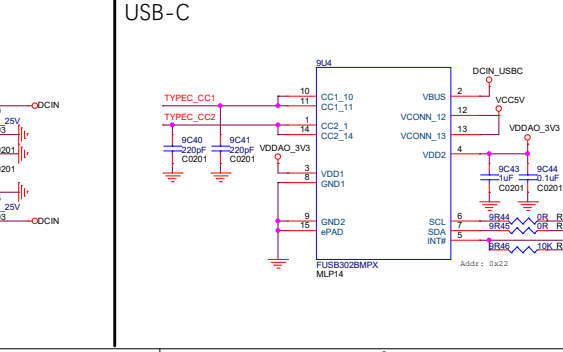
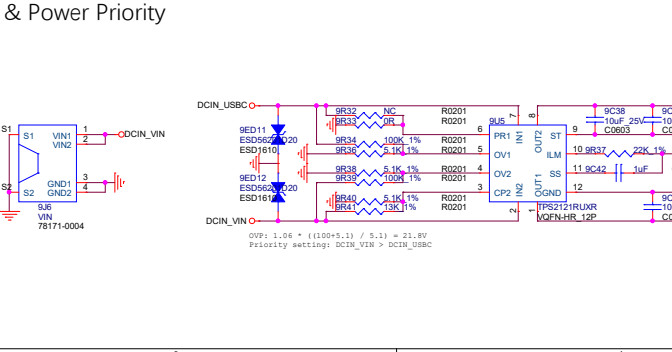
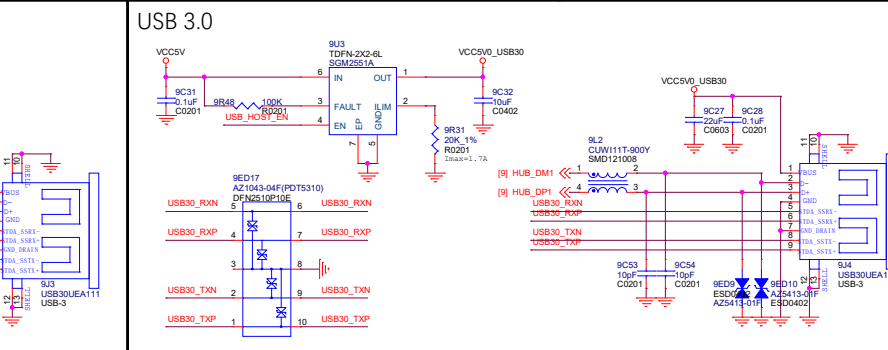
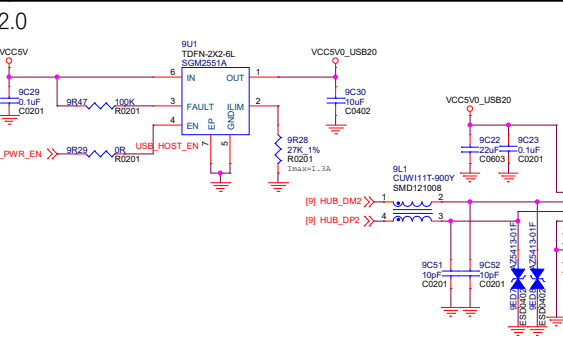
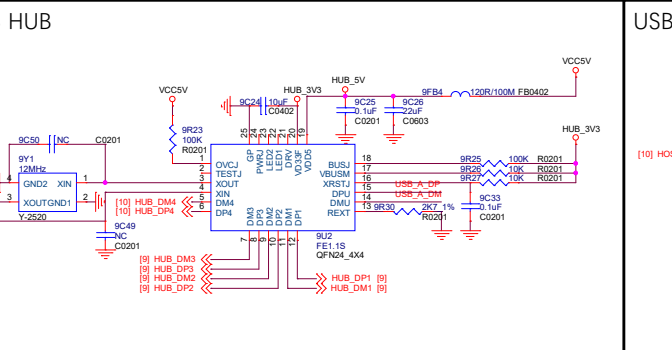
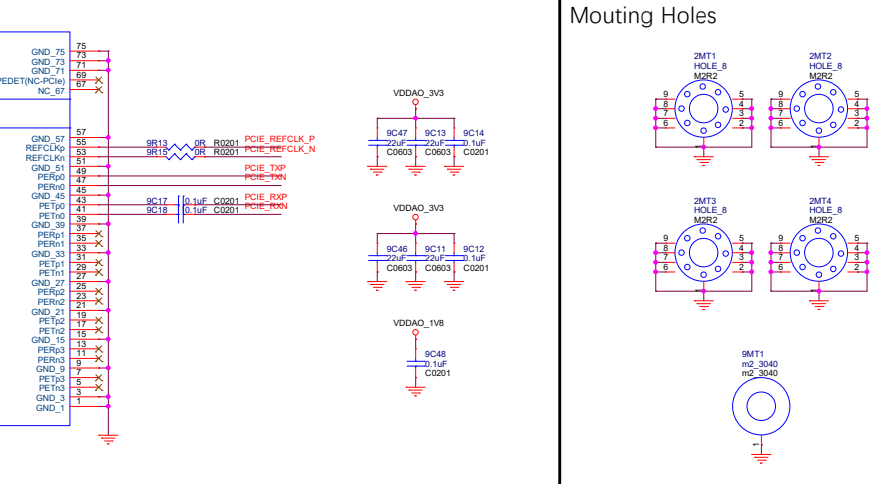
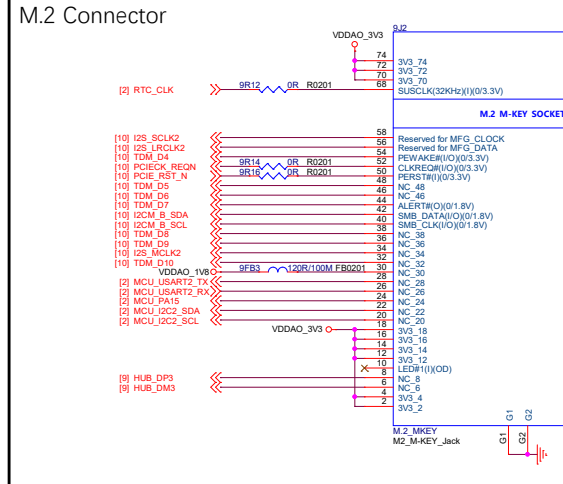
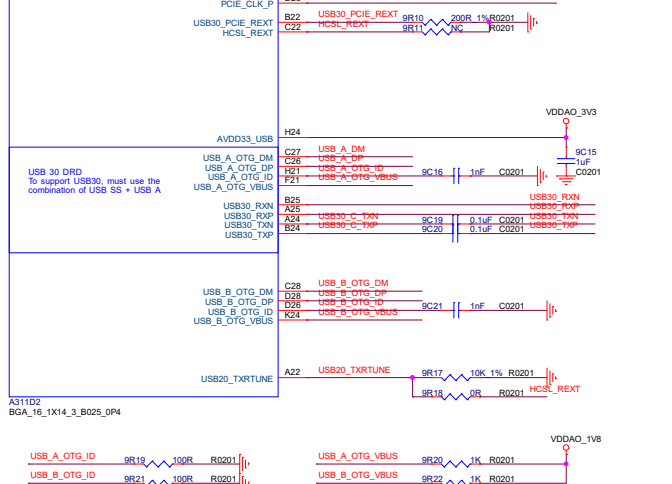
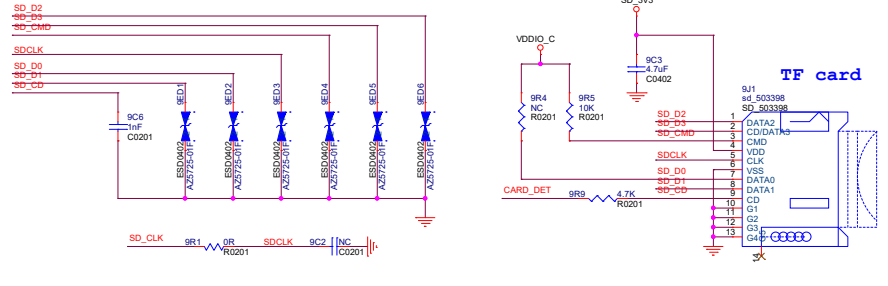
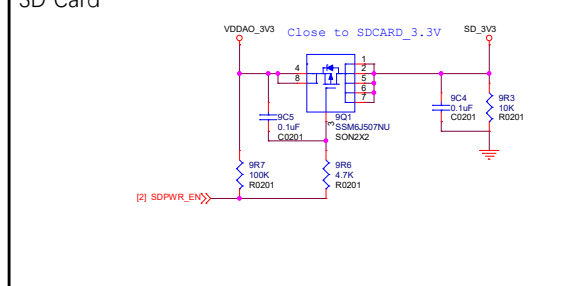
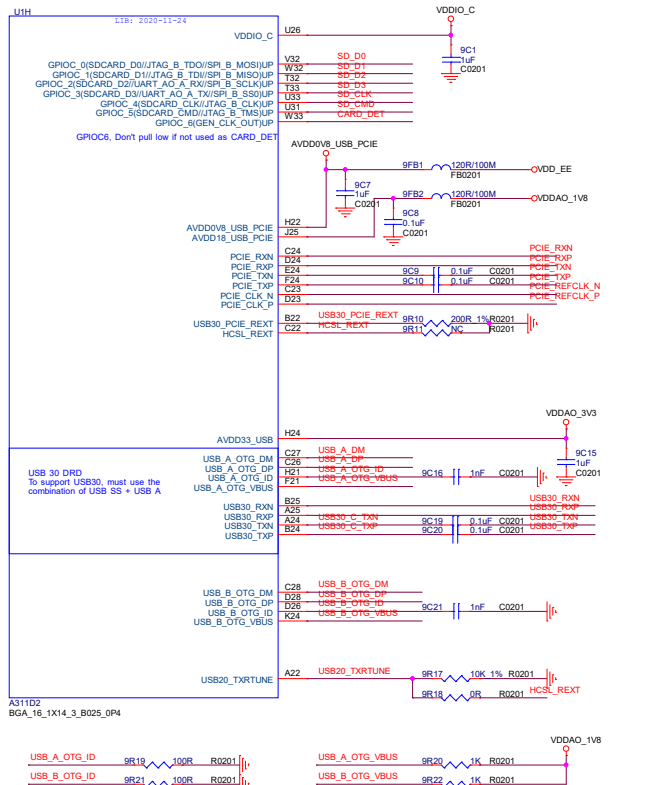


### RJ45



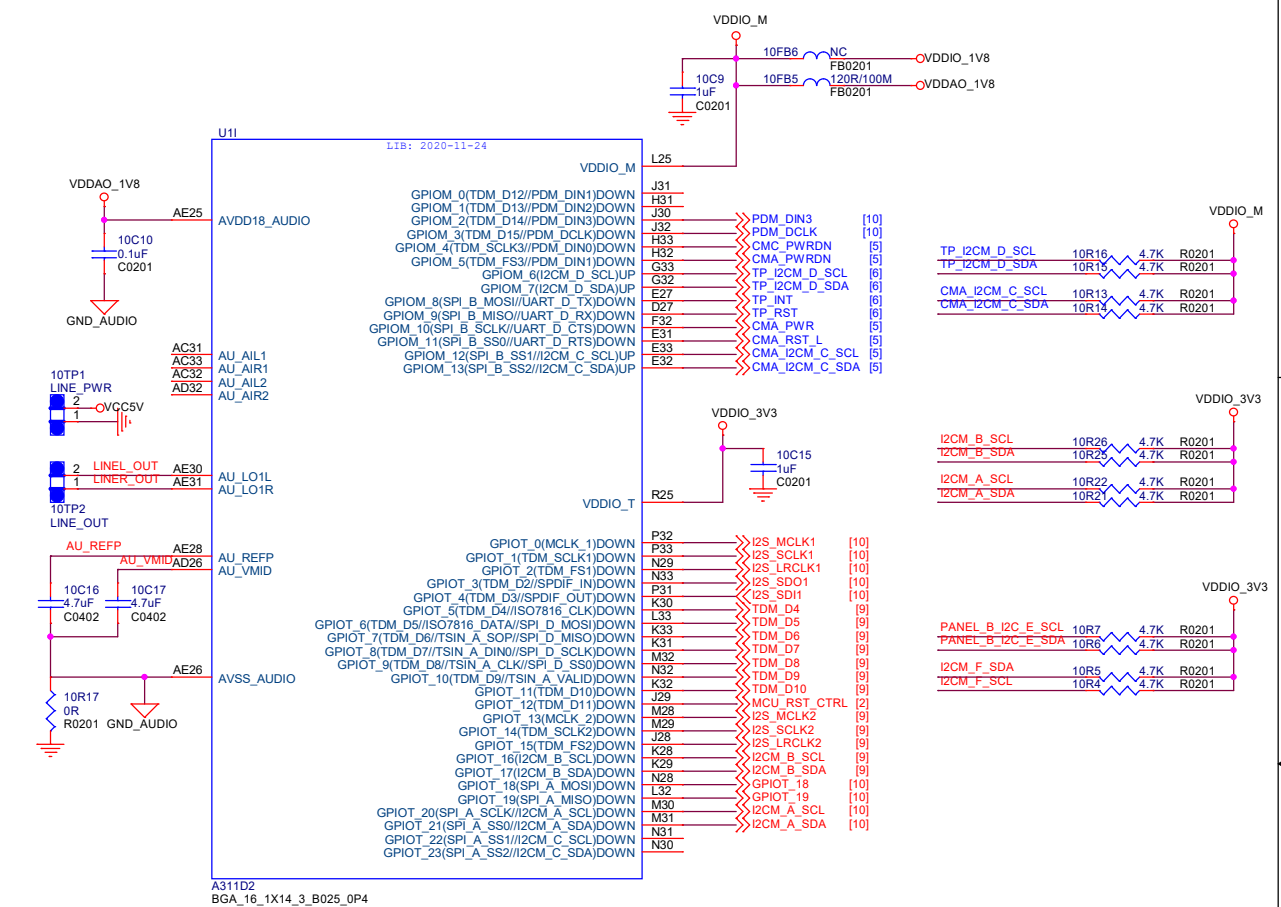
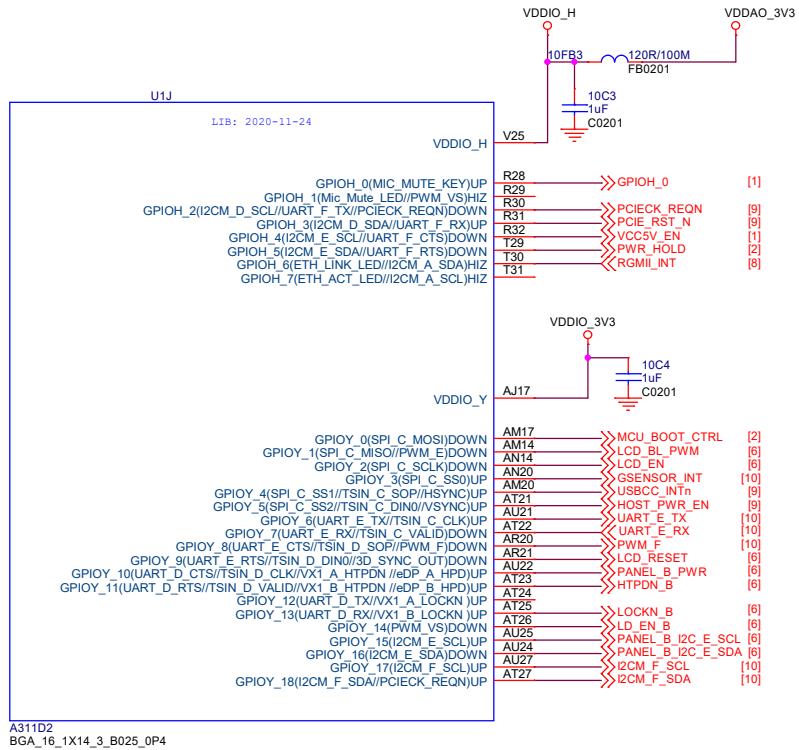
### WOL



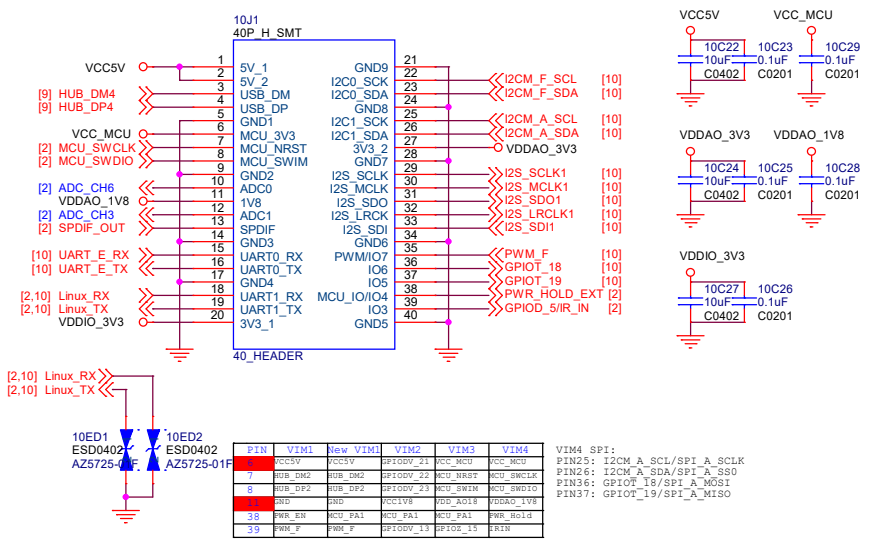


Shenzhen Weson Technology Co., Ltd.

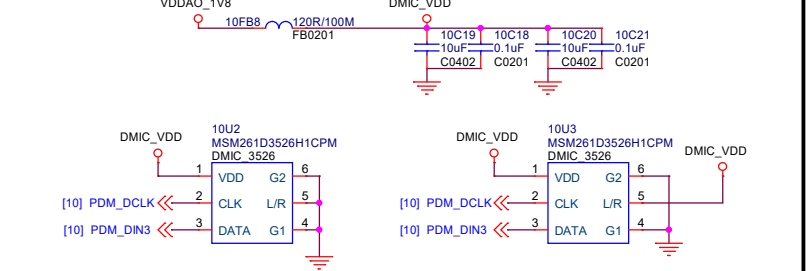
Project:	VIM4
File:	09_USB/PCIE/SIO
Date:	Monday, April 25, 2022
Rev:	V12
Designed by:	TSS
Drawn:	g



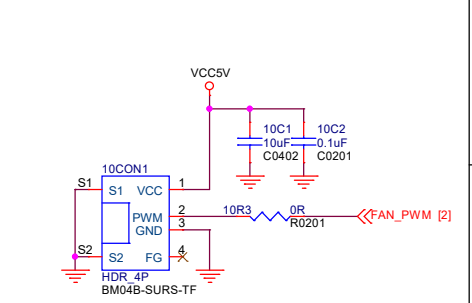
### GPIO Header



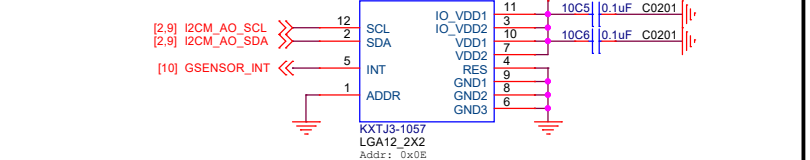
### DMIC



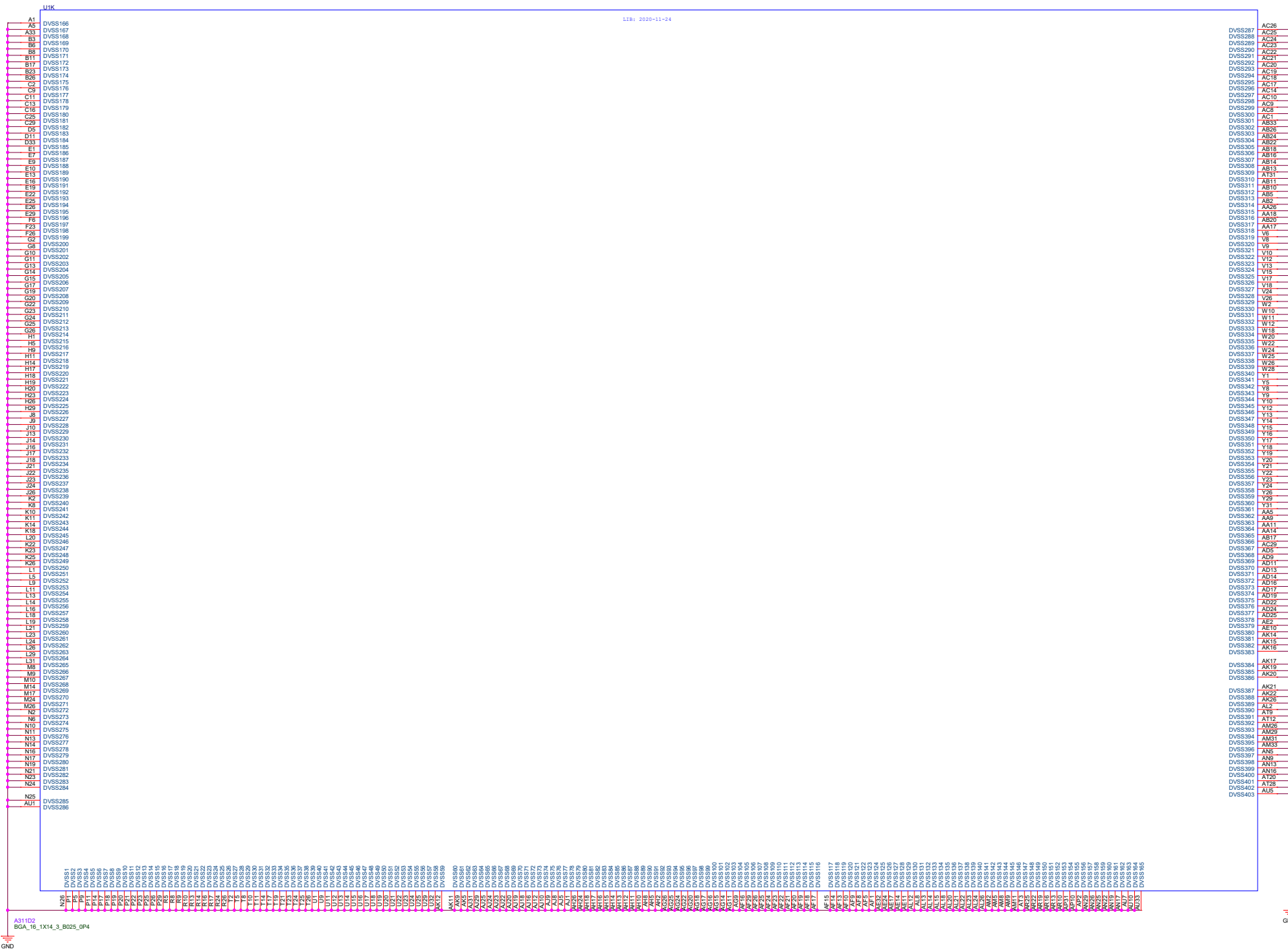
### FAN



### G-sensor



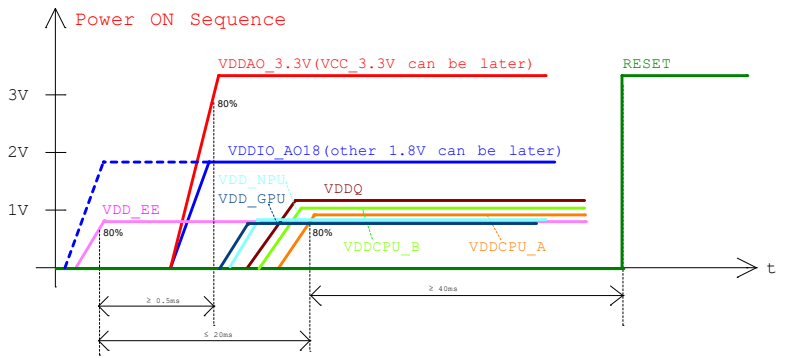
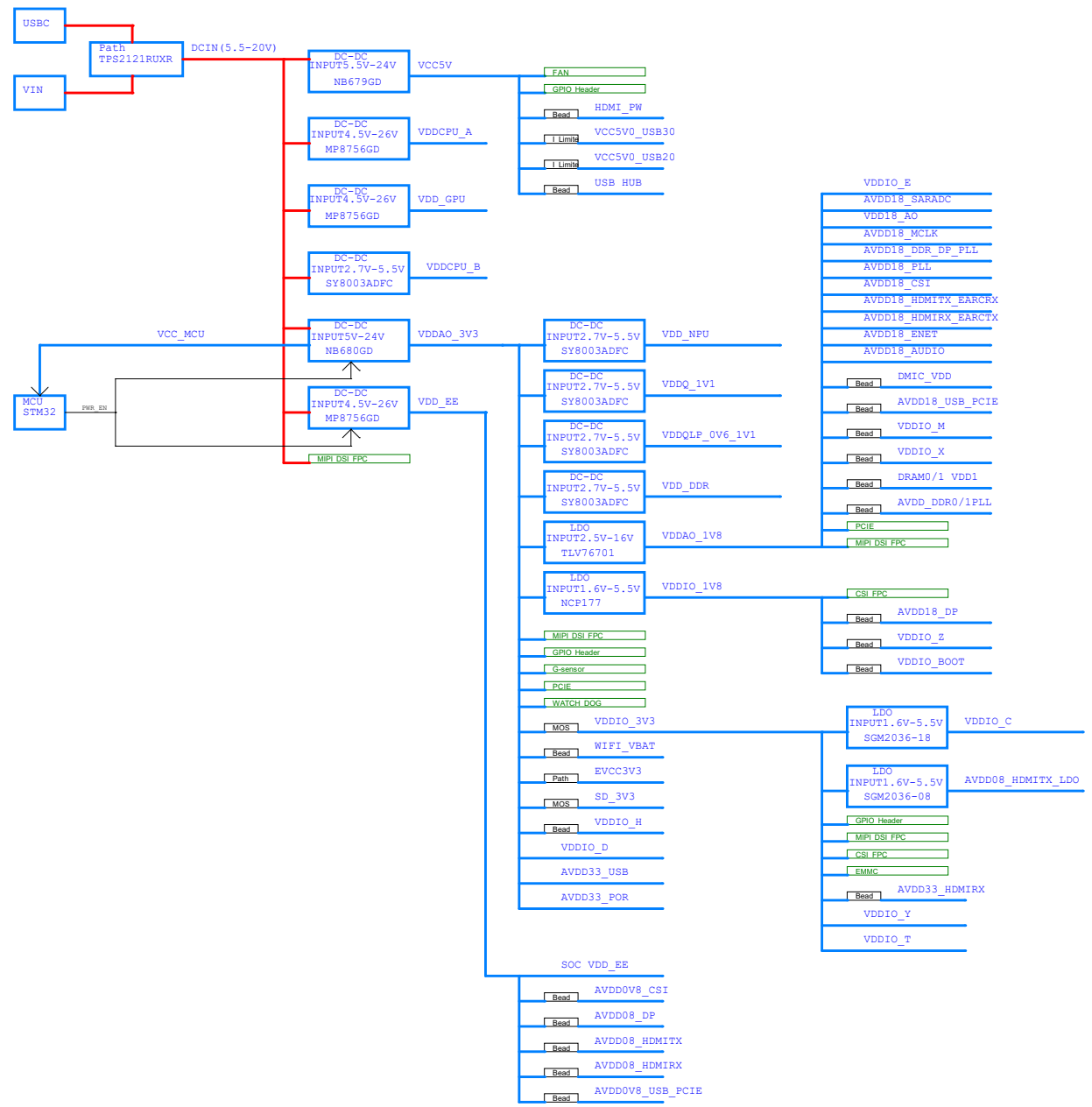
Shenzhen Wesion Technology Co., Ltd.			
Project:	VIM4		
File:	10_GPIO/FAN/Sensor/DMIC		
Date:	Monday, April 25, 2022	Rev:	V12
Designed by:	Totti	Sheet:	10



A31102  
BGA\_16\_1X14\_3\_B025\_0P4

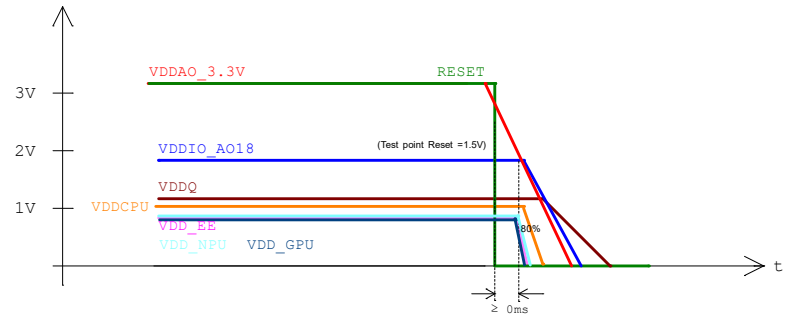
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Power Tree:



- 1) All test values refer to 80% of typical power voltage.
- 2) VDDAO\_3.3V & VCC3.3V should ramp up > 0.5ms later than VDD\_EE.
- 3) All power sources should get stable within 20ms (except VDDQ,VDD\_QLP ).
- 4) No sequence requirement between VDD18\_AO and VDD\_EE.  
No sequence requirement between VDDCPU\_A & VDDCPU\_B & VDD\_NPU & VDD\_GPU & VDDQ & VDD\_QLP & VDD\_DDR and other power source.
- 5) VDDIO\_AO18 should ramps up earlier or at the same time with VDDAO\_3.3V & VCC3.3V.
- 6) RESET\_n should keep low for at least 40ms after power up (except VDDQ,VDD\_QLP).

Power OFF Sequence



A reset IC should monitor VDDIO3.3V, output lower (lower than 1.5V) before other power rails turning off.  
There is no power off sequence requirement between other power rails.

