A311D2

Quick Reference Manual (Rev.C)

Revision: 0.2

Release Date: 2022-10-13

Trademarks

Amlogic, and other Amlogic icons are trademarks of Amlogic companies. All other trademarks and registered trademarks are property of their respective holders.

Disclaimer

Amlogic may make improvements and/or changes in this document or in the product described in this document at any time.

This product is not intended for use in medical, life saving, or life sustaining applications.

Circuit diagrams and other information relating to products of Amlogic are included as a means of illustrating typical applications. Consequently, complete information sufficient for production design is not necessarily given. Amlogic makes no representations or warranties with respect to the accuracy or completeness of the contents presented in this document.

Contact Information

- Website: www.amlogic.com
- Pre-sales consultation: contact@amlogic.com
- Technical support: support@amlogic.com

Revision History

Issue 0.2 (2022-10-13)

This is the 0.2 release.

Compared to last version, the following contents are changed.

Section	Change Description
4.5 and 5.2	Added a note about IO interface.

Issue 0.1 (2022-05-15)

This is the preliminary 0.1 release.

Contents

1 About This Document

This document is applicable for A311D2 series SoCs, please contact your Amlogic sales representative for details.

2 General Description

A311D2 is an advanced application processor designed for smart display. It integrates a powerful CPU/GPU subsystem, a powerful NPU (Neural network Processing Unit), a secured 8K video CODEC engine with all major peripherals to form the ultimate high-performance smart display chip.

The main system CPU is based on Big.LITTLE architecture which integrates a quad-core ARM Cortex-A73 CPU cluster and a quad-core Cortex-A53 cluster with unified L2 cache for each cluster to improve system performance. In addition, the CPU includes the NEON SIMD co-processor to improve software media processing capability.

The graphic subsystem consists of two graphic engines and a flexible video/graphic output pipeline. The ARM Mali-G52 MC4 (2EE) GPU handles all OpenGL ES 3.2, Vulkan 1.1 and OpenCL 2.0 graphic programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. Together, the CPU and GPU handle all operating system, network, user-interface and game related tasks.

Amlogic Video Engine (AVE-10) is a subsystem which uses dedicated hardware video decoders and encoders to offloads the CPUs from all video CODEC processing. AVE-10 is capable of decoding 8K4K resolution video within Trusted Video Path (TVP) for secured DRM applications. It supports all major video formats including MPEG-1/2/4, VC-1/WMV, AVS+, AVS2, MJPEG, H.264, H265-10, VP9-10, AV1 and also JPEG. The independent encoder can concurrently encode in JPEG up to 1080P at 60fps and H.265/H.264 up to 4K at 50fps.

The video/graphics output pipeline includes Dolby Vision Optional, HDR10+, HDR10, HLG and Technicolor Prime HDR processing, BT.2020/ BT.2100 processing, motion compensated and motion adaptive de-interlacer, flexible programmable super scalar, local dimming and many picture enhancement filters before passing the enhanced image to the video output ports. It supports 3 separate display controllers that can be flexibly configured to the V-by-One, LVDS, eDP, MIPI-DSI and HDMI output.

3 HDMI 2.1 receiver ports are available. The HDMI ports can receive up to 4K2K HDR video and support dynamic HDR, ALLM, QFT, QMS, VRR and HDCP 1.4/2.3.

The built-in three demux can process the video streams from the serial transport stream input interface, which can connect to external tuner/demodulator. DVB Common Descrambler 1.0 is supported in addition to DES, Triple DES (TDES/3DES) and AES streaming crypto formats. An integrated ISO7816 controller is included for interfacing to external smart card.

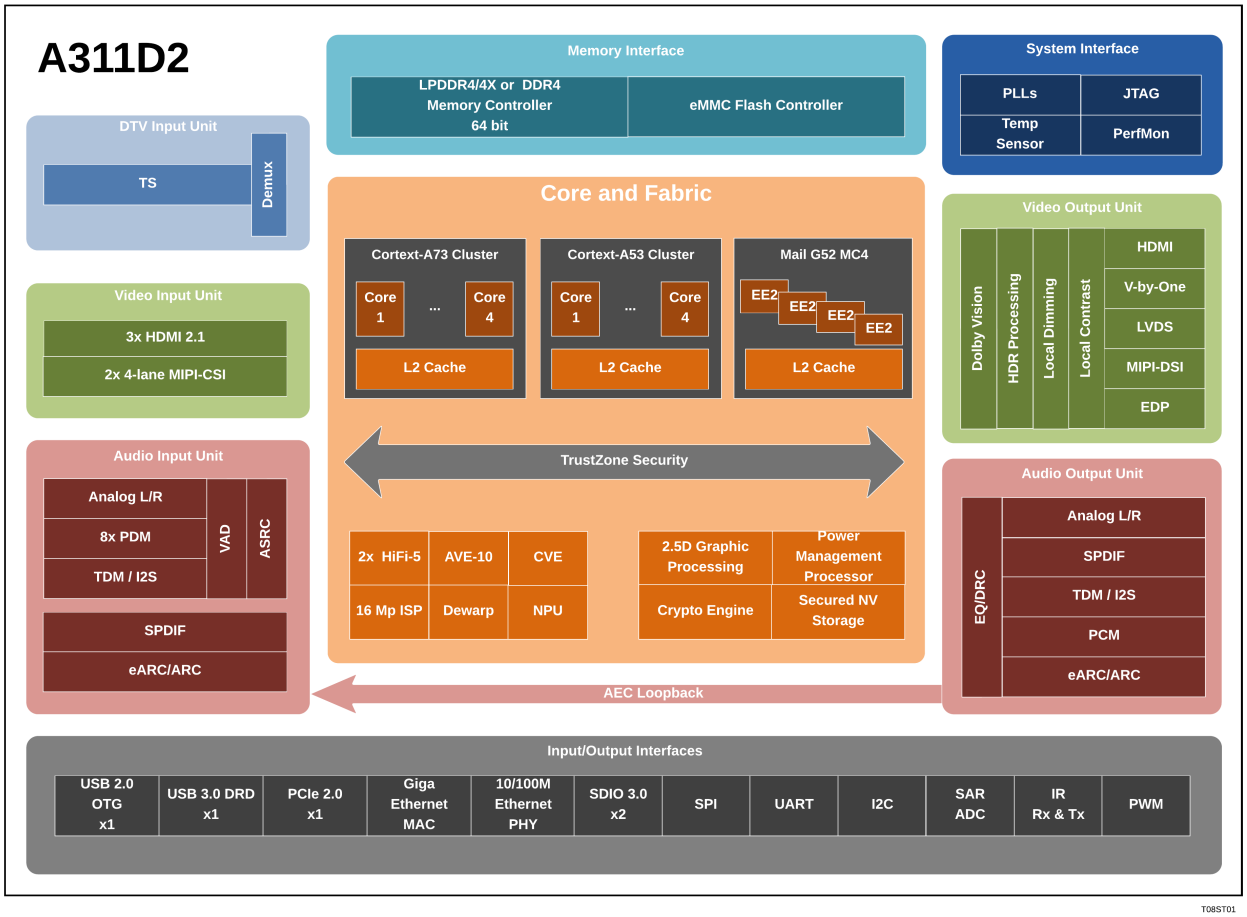
It is optimized for low power far-field voice application. Two dedicated HiFi 5 DSPs offload the main CPU for the top of the line audio front end and wake-word algorithms. It also has built-in Voice Activity Detection (VAD) module for ultra-low power operations during system standby and full digital MIC interface including PDM, TDM and I2S up to 8 channels are available.

The SoC integrates rich advanced network and peripheral interfaces, including a 10/100/1000M Ethernet MAC with RGMII, 10/100M Ethernet PHY, USB3.0 DRD, PCIe 2.0 and USB 2.0 high-speed port, SDIO 3.0 controller, eMMC 5.1 controller and multiple SDIO/SD card controllers, UART, I2C, high-speed SPI PWMs and a built-in IR blaster. The flexible and programmable QoS-based switch fabric and memory controller tie all the processing cores and peripherals together and connects to the DRAM memory bus.

Standard development environment utilizing SecureOS, Linux and GNU/GCC Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

3 Features Summary

Figure 3-1 Features Summary



CPU Sub-system

- Quad core ARM Cortex-A73 + Quad core Cortex-A53 CPU
- ARMv8.0 architecture with Neon extensions and cryptography extension
- Unified system L2 cache for each cluster
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics
- CoreSight debugger support

NPU

- 3.2 Tops
- 512KB Internal RAM and SMMU address re-mapper
- Supports all major deep learning frameworks including Tensorflow, Tensorflow Lite, ONNX, Pytorch, Darknet, MxNet and Caffe

CVE

- Supports a variety of intelligent analysis applications

3D Graphics Processing Unit

- ARM Mali-G52 MC4 (2EE) GPU
- 8-wide warps, 2x dual texture pipe, 8x 8-wide execution engines (EE)
- Concurrent multi-core processing
- OpenGL ES 3.2, Vulkan 1.1 and OpenCL 2.0 support

2.5D Graphics Processor

- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter
- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Fast color space conversion
- Advanced anti-flickering filter

Crypto Engine

- AES block cipher with 128/256 bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- DES/3DES block cipher with ECB and CBC modes supporting 64 bits key for DES and 192 bits key for 3DES
- Hardware key-ladder operation and DVB-CSA for transport stream encryption
- Built-in hardware True Random Number Generator (TRNG) and SHA-1/SHA-2 engine

Video/Picture CODEC

- Amlogic Video Engine (AVE-10) with dedicated hardware decoders up to 8Kx4K@24fps and encoders up to 4Kx2K@50fps
- Supports multi-video decoder up to 4Kx2K@60fps + 1x1080P@60fps
- Supports multiple “secured” video decoding sessions and simultaneous decoding and encoding
- Video/Picture Decoding
  - AV1 MP-10@5.1 up to 8Kx4K@24fps or 4Kx2K@60fps
  - H.265 HEVC MP-10@L5.1 up to 8Kx4K@24fps or 4Kx2K@60fps
  - VP9 Profile 2-10 up to 8Kx4K@24fps or 4Kx2K@60fps
  - AVS2 MP up to 4Kx2K@60fps
  - H.264 AVC HP@L5.1 up to 4Kx2K@30fps
  - MPEG-4 ASP@L5 up to 1080P@60fps (ISO-14496)
  - WMV/VC-1 SP/MP/AP up to 1080P@60fps
  - AVS-P16(AVS+) /AVS-P2 JiZhun Profile up to 1080P@60fps
  - MPEG-2 MP/HL up to 1080P@60fps (ISO-13818)
  - MPEG-1 MP/HL up to 1080P@60fps (ISO-11172)
  - Multiple language and multiple format sub-title video support
  - MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
  - Supports JPEG thumbnail, scaling, rotation and transition effects
- Video/Picture Encoding
  - H.265 main-profile and H.264 high-profile video encoder up to 4K@50fps with low latency
  - Independent JPEG and H.264 encoder with configurable performance/bit-rate

- JPEG image encoding up to 1080P at 60fps

11th Generation Advanced Amlogic TruLife Image Engine

- Supports Dolby Vision Optional, HDR10/10+, HLG, HLG, Prime HDR
- Full 12-bit internal data processing
- Motion compensated noise reduction and 3D digital noise reduction for random noise up to 4K resolution
- Block noise, mosquito noise, spatial noise and temporal noise reduction
- Motion compensated and motion adaptive de-interlacer
- Edge interpolation with low angle protection and processing
- 3:2/2:2 pulldown and Video on Film (VOF) detection and processing
- Smart sharpness with SuperScaler technology including de-ring, LTI, CTI, de-jaggy, peaking. Reproduce more high-frequency details while protecting flesh tones flexibly.
- Dynamic non-Linear contrast for detail enhancement
- 3D LUTs with 17x17x17 nodes, provide 4913 different control points, which is competent for matching calibrated displays to a target color space
- High precision HSL color space based color management with low saturation protection, independent luma/hue/saturation adjustment to achieve blue/green extension, fresh tone correction, and wider gamut for video
- Video mixer: 4x1080p60 or 1x4Kp60 + 1x1080p60 graphic plane and 3x4Kp60 video plane
- Independent HDR re-mapping of video and graphic layer
- Local dimming control for high nits backlights

Video Input/output Interface

- 3x HDMI 2.1 receiver and 1x HDMI 2.1 transmitter ports with EMP, ALLM, QFT, QMS, VRR, eARC, HDCP 1.4 /2.3, and up to 4Kx2K@60 max resolution
- 2x 8-lane V-by-One output with 1, 2, 4 regions supported, up to 4Kx2K 60Hz resolution
- LVDS output supporting up to 3x 1280x720 or 1x 1280x720 + 1x 1920x1080 resolution
- 2x 4-lane MIPI-DSI interface with panel calibration, resolution up to 2x 1920x1200 for each port
- 2x 4-lane eDP supporting panel up to 2560x1600 resolution
- Three independent Gamma table for LCD panel tuning
- Dithering logic for mapping to different LCD panel color depth

Camera Interface

- MIPI-CSI camera interface with 2x4 lanes
- Supports RAW, YUV or RGB camera input formats

ISP

- 16 Mp ISP with the resolution up to 4608x3456
- HDR sensor de-companding/ Dynamic Defect Pixel Correction/ Green channel equalization/ EW image flip
- 3A (AE/AWB/AF)
- Spatial/ Temporal/ Color Noise reduction
- Static White balance
- Lens shading correction
- Demosaic
- Chromatic aberration/ purple Fringing correction

- linear matrix color correction
- Gamma correction

Dewarp Unit

- Supports single frame off line processing up to 4608x3456 video source
- Supports YUV semi-planer 420 format for both input and output
- Supports gray scale image processing
- Supports 360/ 180/ normal fish eye correction modes

Audio Processing and Input/Output

- HiFi 5 audio DSP Optional for highly optimized audio/voice processing
  - 64 KB Instruction Cache and 96 KB Data Cache
  - 32 MPU entries
  - MUL32, MUL16 and DIV32
  - HiFi 5 Single Precision Vector FP
  - HiFi 5 Half Precision Vector FP
  - HiFi 5 Neural Network Extension
- Supports MP3, AAC, WMA, RM, FLAC, Ogg, Dolby Audio Optional, DTS Optional and programmable with 7.1/5.1 down-mixing
- Low-power VAD and internal AEC loopback path
- 3 built-in TDM/I2S ports with TDM/PCM mode up to 192kHz x 32bits x 8ch or 48kHz x 32bits x 32ch and I2S mode up to 192kHz x 32bits x 8ch
- Digital microphone PDM voice input with programmable CIC, LPF and HPF, supports up to 8 DMICs
- 1 L/R analog input channel and 1 L/R output channel
- Supports concurrent dual audio stereo channel output with combination of I2S+PCM
- Supports Audio EQ/DRC for audio speaker
- Supports dynamic EQ adjustment

DTV Broadcasting Interface

- 3x Transport stream (TS) input interface with built-in demux processor for connecting to external digital TV tuner/demodulator
- Built-in PWM, I2C and SPI interfaces to control tuner and demodulator
- Integrated ISO 7816 smart card controller

Memory and Storage Interface

- 64-bit DRAM memory interface with dual ranks, max 16GB total logic address space and max 8GB total DDR capacity physical address
- Compatible with JEDEC standard DDR4-3200 /LPDDR4/LPDDR4X-4266 SDRAM
- 4-bit SD card and 4-bit SDIO interface support up to SDR104/HS200 mode
- 8-bit eMMC memory interface support up to HS400 mode
- Built-in 8k bits OTP memory for secured key storage

Network Interface

- IEEE 802.3 10/100/1000M Ethernet MAC with RGMII interface
- 10/100M Ethernet PHY interface
- WiFi/IEEE802.11 supporting via PCIe, USB or SDIO

- Bluetooth supporting via USB or UART
- Network interface optimized for mixed WIFI and BT traffic

Integrated I/O Controllers and Interfaces

- One USB 2.0 high-speed USB I/O which supports USB OTG
- One USB 3.0 DRD port up to 5Gbps
- One PCIe 2.0 (Root Complex) port
- Multiple UARTs, I2Cs and PWMs
- SPI interface
- Programmable remote control input circuitry and IR-blaster output
- Built-in 10bit SAR ADC with 5 channels
- General Purpose IOs with built-in pull up and pull down

System, Peripherals and Misc. Interfaces

- Integrated general purpose timers, counters, DMA controllers
- 24 MHz crystal input
- Embedded debug interface using ICE/JTAG

Power Management

- Multiple internal power domains controlled by software
- Multiple sleep modes for CPU, system, DRAM, etc.
- Multiple internal PLLs to adjust the operating frequencies
- Multi-voltage I/O design for 1.8V and 3.3V

Security

- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, encrypted hardware self-setup OTP, encrypted DRAM with memory integrity checker, hardware key ladder and internal control buses and storage
- Separated secure/non-secure Entropy true RNG and video watermarking
- Pre-region/ID memory security control and electric fence
- Hardware based Trusted Video Path (TVP), and secured contents (needs SecureOS software)
- Secured IO and secured clock

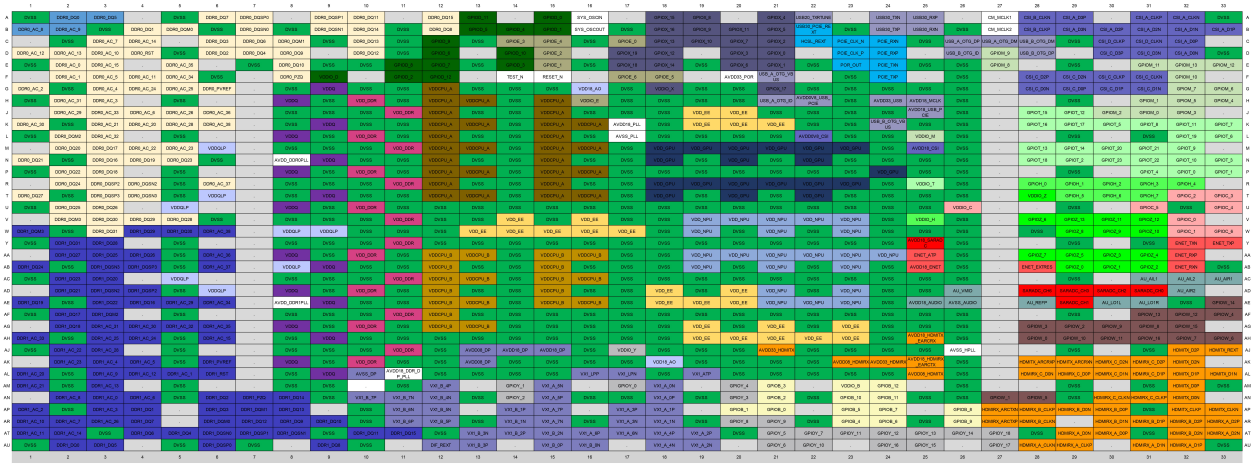
Package

- FCBGA, 14.3 mm x 16.1 mm, 0.4 ball pitch, RoHS compliant

4 Pinout Specification

4.1 Pinout Diagram

Figure 4-1 Pinout Diagram (top view)



4.2 Pin Order

BALL #	NET NAME
A1	DVSS
A2	DDR0_DQ0
A3	DDR0_DQ5
A5	DVSS
A6	DDR0_DQ7
A7	DDR0_DQSP0
A9	DDR0_DQSP1
A10	DDR0_DQ11
A12	DDR0_DQ15
A13	GPIOD_11
A15	GPIOD_0
A16	SYS_OSCIN
A18	GPIOX_15
A19	GPIOX_8
A21	GPIOX_4
A22	USB20_TXRTUNE
A24	USB30_TXN
A25	USB30_RXP
A27	CM_MCLK1

BALL #	NET NAME
A28	CSI_B_CLKN
A29	CSI_A_D3P
A31	CSI_A_CLKP
A32	CSI_A_CLKN
A33	DVSS
B1	DDR0_AC_8
B2	DDR0_AC_9
B3	DVSS
B4	DDR0_DQ1
B5	DDR0_DQM0
B6	DVSS
B7	DDR0_DQSN0
B8	DVSS
B9	DDR0_DQSN1
B10	DDR0_DQ14
B11	DVSS
B12	DDR0_DQ8
B13	GPIOD_5
B14	GPIOD_4

BALL #	NET NAME
B15	GPIOD_1
B16	SYS_OSCOUT
B17	DVSS
B18	GPIOX_16
B19	GPIOX_9
B20	GPIOX_11
B21	GPIOX_5
B22	USB30_PCIE_REXT
B23	DVSS
B24	USB30_TXP
B25	USB30_RXN
B26	DVSS
B27	CM_MCLK2
B28	CSI_B_CLKP
B29	CSI_A_D3N
B30	CSI_A_D2P
B31	CSI_A_D2N
B32	CSI_A_D1N
B33	CSI_A_D1P

BALL #	NET NAME
C2	DVSS
C3	DDR0_AC_7
C4	DDR0_AC_14
C6	DDR0_DQ3
C7	DDR0_DQ6
C8	DDR0_DQM1
C9	DVSS
C10	DDR0_DQ13
C11	DVSS
C12	GPIOD_9
C13	DVSS
C14	GPIOE_3
C15	GPIOE_4
C16	DVSS
C17	GPIOE_0
C18	GPIOX_13
C19	GPIOX_10
C20	GPIOX_7
C21	GPIOX_2
C22	HCSL_REXT
C23	PCIE_CLK_N
C24	PCIE_RXN
C25	DVSS
C26	USB_A_OTG_DP
C27	USB_A_OTG_DM
C28	USB_B_OTG_DM
C29	DVSS
C30	CSI_D_CLKP
C31	CSI_D_CLKN
C32	CSI_A_D0P
D1	DDR0_AC_12
D2	DDR0_AC_13
D3	DDR0_AC_10
D4	DDR0_RST
D5	DVSS
D6	DDR0_DQ2

BALL #	NET NAME
D7	DDR0_DQ4
D8	DDR0_DQ9
D10	DDR0_DQ12
D11	DVSS
D12	GPIOD_6
D14	GPIOD_10
D15	GPIOE_2
D17	GPIOX_19
D18	GPIOX_12
D20	GPIOX_3
D21	GPIOX_0
D23	PCIE_CLK_P
D24	PCIE_RXP
D26	USB_B_OTG_ID
D27	GPIOM_9
D28	USB_B_OTG_DP
D30	CSI_C_D3P
D31	CSI_C_D3N
D32	CSI_A_D0N
D33	DVSS
E1	DVSS
E2	DDR0_AC_0
E3	DDR0_AC_15
E5	DDR0_AC_35
E7	DVSS
E8	DDR0_DQ10
E9	DVSS
E10	DVSS
E11	GPIOD_8
E12	GPIOD_7
E13	DVSS
E14	GPIOD_3
E15	GPIOE_1
E16	DVSS
E17	GPIOX_18
E18	GPIOX_14

BALL #	NET NAME
E19	DVSS
E20	GPIOX_6
E21	GPIOX_1
E22	DVSS
E23	POR_OUT
E24	PCIE_TXN
E25	DVSS
E26	DVSS
E27	GPIOM_8
E29	DVSS
E31	GPIOM_11
E32	GPIOM_13
E33	GPIOM_12
F2	DDR0_AC_1
F3	DDR0_AC_5
F4	DDR0_AC_11
F5	DDR0_AC_34
F6	DVSS
F8	DDR0_PZQ
F9	VDDIO_D
F11	GPIOD_2
F12	GPIOD_12
F14	TEST_N
F15	RESET_N
F17	GPIOE_6
F18	GPIOE_5
F20	AVDD33_POR
F21	USB_A_OTG_VBUS
F23	DVSS
F24	PCIE_TXP
F26	DVSS
F28	CSI_C_D2P
F29	CSI_C_D2N
F30	CSI_C_CLKP
F31	CSI_C_CLKN
F32	GPIOM_10

BALL #	NET NAME
G1	DDR0_AC_2
G2	DVSS
G3	DDR0_AC_4
G4	DDR0_AC_24
G5	DDR0_AC_25
G6	DDR0_PVREF
G8	DVSS
G9	VDDQ
G10	DVSS
G11	DVSS
G12	VDDCPU_A
G13	DVSS
G14	DVSS
G15	DVSS
G16	VDD18_AO
G17	DVSS
G18	VDDIO_X
G19	DVSS
G20	DVSS
G21	GPIOX_17
G22	DVSS
G23	DVSS
G24	DVSS
G25	DVSS
G26	DVSS
G28	CSI_C_D0N
G29	CSI_C_D0P
G30	CSI_C_D1P
G31	CSI_C_D1N
G32	GPIOM_7
G33	GPIOM_6
H1	DVSS
H2	DDR0_AC_31
H3	DDR0_AC_3
H5	DVSS
H8	VDDQ
H9	DVSS

BALL #	NET NAME
H10	VDD_DDR
H11	DVSS
H12	VDDCPU_A
H13	VDDCPU_A
H14	DVSS
H15	VDDCPU_A
H16	VDDIO_E
H17	DVSS
H18	DVSS
H19	DVSS
H20	DVSS
H21	USB_A_OTG_ID
H22	AVDD0V8_USB_PCIE
H23	DVSS
H24	AVDD33_USB
H25	AVDD18_MCLK
H26	DVSS
H29	DVSS
H31	GPIOM_1
H32	GPIOM_5
H33	GPIOM_4
J2	DDR0_AC_29
J3	DDR0_AC_33
J4	DDR0_AC_6
J5	DDR0_AC_26
J6	DDR0_AC_36
J8	DVSS
J9	DVSS
J10	DVSS
J11	VDD_DDR
J12	VDDCPU_A
J13	DVSS
J14	DVSS
J15	VDDCPU_A
J16	DVSS
J17	DVSS
J18	DVSS

BALL #	NET NAME
J19	VDD_EE
J20	VDD_EE
J21	DVSS
J22	DVSS
J23	DVSS
J24	DVSS
J25	AVDD18_USB_PCIE
J26	DVSS
J28	GPIOT_15
J29	GPIOT_12
J30	GPIOM_2
J31	GPIOM_0
J32	GPIOM_3
K1	DDR0_AC_30
K2	DVSS
K3	DDR0_AC_21
K4	DDR0_AC_20
K5	DDR0_AC_28
K6	DDR0_AC_38
K8	DVSS
K9	VDDQ
K10	DVSS
K11	DVSS
K12	VDDCPU_A
K13	VDDCPU_A
K14	DVSS
K15	VDDCPU_A
K16	VDDCPU_A
K17	AVDD18_PLL
K18	DVSS
K19	VDD_EE
K20	VDD_EE
K21	VDD_EE
K22	DVSS
K23	DVSS
K24	USB_B_OTG_VBUS
K25	DVSS

BALL #	NET NAME
K26	DVSS
K28	GPIOT_16
K29	GPIOT_17
K30	GPIOT_5
K31	GPIOT_8
K32	GPIOT_11
K33	GPIOT_7
L1	DVSS
L2	DDR0_DQM2
L3	DDR0_AC_32
L5	DVSS
L8	VDDQ
L9	DVSS
L10	VDD_DDR
L11	DVSS
L12	VDDCPU_A
L13	DVSS
L14	DVSS
L15	VDDCPU_A
L16	DVSS
L17	AVSS_PLL
L18	DVSS
L19	DVSS
L20	DVSS
L21	DVSS
L22	AVDD0V8_CSI
L23	DVSS
L24	DVSS
L25	VDDIO_M
L26	DVSS
L29	DVSS
L31	DVSS
L32	GPIOT_19
L33	GPIOT_6
M2	DDR0_DQ20
M3	DDR0_DQ17
M4	DDR0_AC_22

BALL #	NET NAME
M5	DDR0_AC_23
M6	VDDQLP
M8	DVSS
M9	DVSS
M10	DVSS
M11	VDD_DDR
M12	VDDCPU_A
M13	VDDCPU_A
M14	DVSS
M15	VDDCPU_A
M16	VDDCPU_A
M17	DVSS
M18	VDD_GPU
M19	VDD_GPU
M20	VDD_GPU
M21	VDD_GPU
M22	VDD_GPU
M23	VDD_GPU
M24	DVSS
M25	AVDD18_CSI
M26	DVSS
M28	GPIOT_13
M29	GPIOT_14
M30	GPIOT_20
M31	GPIOT_21
M32	GPIOT_9
N1	DDR0_DQ21
N2	DVSS
N3	DDR0_DQ16
N4	DDR0_DQ19
N5	DDR0_DQ23
N6	DVSS
N8	AVDD_DDR0PLL
N9	VDDQ
N10	DVSS
N11	DVSS

BALL #	NET NAME
N12	VDDCPU_A
N13	DVSS
N14	DVSS
N15	VDDCPU_A
N16	DVSS
N17	DVSS
N18	VDD_GPU
N19	DVSS
N20	VDD_GPU
N21	DVSS
N22	VDD_GPU
N23	DVSS
N24	DVSS
N25	DVSS
N26	DVSS
N28	GPIOT_18
N29	GPIOT_2
N30	GPIOT_23
N31	GPIOT_22
N32	GPIOT_10
N33	GPIOT_3
P1	DVSS
P2	DDR0_DQ22
P3	DDR0_DQ18
P5	DVSS
P8	VDDQ
P9	DVSS
P10	VDD_DDR
P11	DVSS
P12	VDDCPU_A
P13	VDDCPU_A
P14	DVSS
P15	VDDCPU_A
P16	VDDCPU_A
P17	DVSS
P18	DVSS
P19	DVSS

BALL #	NET NAME
P20	DVSS
P21	DVSS
P22	DVSS
P23	DVSS
P24	VDD_GPU
P25	DVSS
P26	DVSS
P29	DVSS
P31	GPIOT_4
P32	GPIOT_0
P33	GPIOT_1
R2	DDR0_DQ24
R3	DDR0_DQSP2
R4	DDR0_DQSN2
R5	DVSS
R6	DDR0_AC_37
R8	DVSS
R9	DVSS
R10	DVSS
R11	VDD_DDR
R12	VDDCPU_A
R13	DVSS
R14	DVSS
R15	VDDCPU_A
R16	DVSS
R17	DVSS
R18	VDD_GPU
R19	VDD_GPU
R20	VDD_GPU
R21	VDD_GPU
R22	VDD_GPU
R23	VDD_GPU
R24	DVSS
R25	VDDIO_T
R26	DVSS
R28	GPIOH_0
R29	GPIOH_1

BALL #	NET NAME
R30	GPIOH_2
R31	GPIOH_3
R32	GPIOH_4
T1	DDR0_DQ27
T2	DVSS
T3	DDR0_DQSP3
T4	DDR0_DQSN3
T5	DVSS
T6	VDDQLP
T8	DVSS
T9	VDDQ
T10	DVSS
T11	DVSS
T12	VDDCPU_A
T13	VDDCPU_A
T14	DVSS
T15	VDDCPU_A
T16	VDDCPU_A
T17	DVSS
T18	VDD_GPU
T19	DVSS
T20	VDD_GPU
T21	DVSS
T22	VDD_GPU
T23	DVSS
T24	DVSS
T25	DVSS
T26	DVSS
T28	VDDIO_Z
T29	GPIOH_5
T30	GPIOH_6
T31	GPIOH_7
T32	GPIOC_2
T33	GPIOC_3
U1	DVSS
U2	DDR0_DQ25
U3	DDR0_DQ26

BALL #	NET NAME
U5	VDDQLP
U8	VDDQ
U9	DVSS
U10	VDD_DDR
U11	DVSS
U12	DVSS
U13	DVSS
U14	DVSS
U15	DVSS
U16	DVSS
U17	DVSS
U18	DVSS
U19	DVSS
U20	DVSS
U21	DVSS
U22	DVSS
U23	DVSS
U24	DVSS
U25	DVSS
U26	VDDIO_C
U29	DVSS
U31	GPIOC_5
U32	DVSS
U33	GPIOC_4
V2	DDR0_DQM3
V3	DDR0_DQ30
V4	DDR0_DQ29
V5	DDR0_DQ28
V6	DVSS
V8	DVSS
V9	DVSS
V10	DVSS
V11	VDD_DDR
V12	DVSS
V13	DVSS
V14	VDD_EE
V15	DVSS
V16	VDD_EE

BALL #	NET NAME
V17	DVSS
V18	DVSS
V19	VDD_NPU
V20	VDD_NPU
V21	VDD_NPU
V22	VDD_NPU
V23	VDD_NPU
V24	DVSS
V25	VDDIO_H
V26	DVSS
V28	GPIOZ_6
V29	GPIOZ_13
V30	GPIOZ_11
V31	GPIOZ_12
V32	GPIOC_0
W1	DDR1_DQM3
W2	DVSS
W3	DDR0_DQ31
W4	DDR1_DQ29
W5	DDR1_DQ30
W6	DDR1_AC_38
W8	VDDQLP
W9	VDDQLP
W10	DVSS
W11	DVSS
W12	DVSS
W13	VDD_EE
W14	VDD_EE
W15	VDD_EE
W16	VDD_EE
W17	VDD_EE
W18	DVSS
W19	VDD_NPU
W20	DVSS
W21	VDD_NPU
W22	DVSS

BALL #	NET NAME
W23	VDD_NPU
W24	DVSS
W25	DVSS
W26	DVSS
W28	DVSS
W29	GPIOZ_8
W30	GPIOZ_9
W31	GPIOZ_10
W32	GPIOC_1
W33	GPIOC_6
Y1	DVSS
Y2	DDR1_DQ31
Y3	DDR1_DQ28
Y5	DVSS
Y8	DVSS
Y9	DVSS
Y10	DVSS
Y11	VDD_DDR
Y12	DVSS
Y13	DVSS
Y14	DVSS
Y15	DVSS
Y16	DVSS
Y17	DVSS
Y18	DVSS
Y19	DVSS
Y20	DVSS
Y21	DVSS
Y22	DVSS
Y23	DVSS
Y24	DVSS
Y25	AVDD18_SARADC
Y26	DVSS
Y29	DVSS
Y31	DVSS
Y32	ENET_TXN
Y33	ENET_TXP

BALL #	NET NAME
AA2	DDR1_DQ27
AA3	DDR1_DQ25
AA4	DDR1_DQ26
AA5	DVSS
AA6	DDR1_AC_36
AA8	VDDQ
AA9	DVSS
AA10	VDD_DDR
AA11	DVSS
AA12	VDDCPU_B
AA13	VDDCPU_B
AA14	DVSS
AA15	VDDCPU_B
AA16	VDDCPU_B
AA17	DVSS
AA18	DVSS
AA19	VDD_NPU
AA20	VDD_NPU
AA21	VDD_NPU
AA22	VDD_NPU
AA23	VDD_NPU
AA24	VDD_NPU
AA25	ENET_ATP
AA26	DVSS
AA28	GPIOZ_7
AA29	GPIOZ_5
AA30	GPIOZ_3
AA31	GPIOZ_4
AA32	ENET_RXP
AB1	DDR1_DQ24
AB2	DVSS
AB3	DDR1_DQSN3
AB4	DDR1_DQSP3
AB5	DVSS
AB6	DDR1_AC_37
AB8	VDDQLP

BALL #	NET NAME
AB9	VDDQ
AB10	DVSS
AB11	DVSS
AB12	VDDCPU_B
AB13	DVSS
AB14	DVSS
AB15	VDDCPU_B
AB16	DVSS
AB17	DVSS
AB18	DVSS
AB19	VDD_NPU
AB20	DVSS
AB21	VDD_NPU
AB22	DVSS
AB23	VDD_NPU
AB24	DVSS
AB25	AVDD18_ENET
AB26	DVSS
AB28	ENET_EXTRES
AB29	GPIOZ_0
AB30	GPIOZ_1
AB31	GPIOZ_2
AB32	ENET_RXN
AB33	DVSS
AC1	DVSS
AC2	DDR1_DQ23
AC3	DDR1_DQ20
AC5	VDDQLP
AC8	DVSS
AC9	DVSS
AC10	DVSS
AC11	VDD_DDR
AC12	VDDCPU_B
AC13	VDDCPU_B
AC14	DVSS
AC15	VDDCPU_B
AC16	VDDCPU_B

BALL #	NET NAME
AC17	DVSS
AC18	DVSS
AC19	DVSS
AC20	DVSS
AC21	DVSS
AC22	DVSS
AC23	DVSS
AC24	DVSS
AC25	DVSS
AC26	DVSS
AC29	DVSS
AC31	AU_AIL1
AC32	AU_AIL2
AC33	AU_AIR1
AD2	DDR1_DQ21
AD3	DDR1_DQSN2
AD4	DDR1_DQSP2
AD5	DVSS
AD6	VDDQLP
AD8	VDDQ
AD9	DVSS
AD10	VDD_DDR
AD11	DVSS
AD12	VDDCPU_B
AD13	DVSS
AD14	DVSS
AD15	VDDCPU_B
AD16	DVSS
AD17	DVSS
AD18	VDD_EE
AD19	DVSS
AD20	VDD_EE
AD21	VDD_NPU
AD22	DVSS
AD23	VDD_NPU
AD24	DVSS
AD25	DVSS

BALL #	NET NAME
AD26	AU_VMID
AD28	SARADC_CH6
AD29	SARADC_CH3
AD30	SARADC_CH2
AD31	SARADC_CH0
AD32	AU_AIR2
AE1	DDR1_DQ19
AE2	DVSS
AE3	DDR1_DQ22
AE4	DDR1_DQ16
AE5	DDR1_AC_29
AE6	DDR1_AC_34
AE8	AVDD_DDR1PLL
AE9	VDDQ
AE10	DVSS
AE11	DVSS
AE12	VDDCPU_B
AE13	VDDCPU_B
AE14	DVSS
AE15	VDDCPU_B
AE16	VDDCPU_B
AE17	DVSS
AE18	VDD_EE
AE19	VDD_EE
AE20	VDD_EE
AE21	VDD_NPU
AE22	VDD_NPU
AE23	VDD_NPU
AE24	DVSS
AE25	AVDD18_AUDIO
AE26	AVSS_AUDIO
AE28	AU_REFP
AE29	SARADC_CH1
AE30	AU_LO1L
AE31	AU_LO1R
AE32	DVSS

BALL #	NET NAME
AE33	GPIOW_14
AF1	DVSS
AF2	DDR1_DQ17
AF3	DDR1_DQM2
AF5	DVSS
AF8	DVSS
AF9	DVSS
AF10	DVSS
AF11	VDD_DDR
AF12	VDDCPU_B
AF13	DVSS
AF14	DVSS
AF15	DVSS
AF16	DVSS
AF17	DVSS
AF18	DVSS
AF19	DVSS
AF20	DVSS
AF21	DVSS
AF22	DVSS
AF23	DVSS
AF24	DVSS
AF25	DVSS
AF26	DVSS
AF29	DVSS
AF31	GPIOW_13
AF32	GPIOW_12
AF33	GPIOW_4
AG2	DDR1_DQ18
AG3	DDR1_AC_31
AG4	DDR1_AC_30
AG5	DDR1_AC_32
AG6	DDR1_AC_35
AG8	VDDQ
AG9	DVSS
AG10	VDD_DDR
AG11	DVSS

BALL #	NET NAME
AG12	VDDCPU_B
AG13	VDDCPU_B
AG14	DVSS
AG15	DVSS
AG16	DVSS
AG17	DVSS
AG18	DVSS
AG19	VDD_EE
AG20	DVSS
AG21	VDD_EE
AG22	DVSS
AG23	VDD_EE
AG24	DVSS
AG25	DVSS
AG26	DVSS
AG28	GPIOW_3
AG29	GPIOW_2
AG30	GPIOW_9
AG31	GPIOW_8
AG32	GPIOW_15
AH1	DDR1_AC_33
AH2	DVSS
AH3	DDR1_AC_25
AH4	DDR1_AC_24
AH5	DVSS
AH6	DDR1_AC_15
AH8	DVSS
AH9	VDDQ
AH10	DVSS
AH11	DVSS
AH12	DVSS
AH13	DVSS
AH14	DVSS
AH15	DVSS
AH16	DVSS
AH17	DVSS
AH18	DVSS

BALL #	NET NAME
AH19	VDD_EE
AH20	VDD_EE
AH21	VDD_EE
AH22	VDD_EE
AH23	VDD_EE
AH24	DVSS
AH25	AVDD18_HDMITX_ EARCRX
AH26	DVSS
AH28	GPIOW_0
AH29	GPIOW_10
AH30	GPIOW_11
AH31	GPIOW_16
AH32	GPIOW_7
AH33	GPIOW_6
AJ1	DVSS
AJ2	DDR1_AC_22
AJ3	DDR1_AC_28
AJ5	DVSS
AJ8	DVSS
AJ9	DVSS
AJ10	DVSS
AJ11	VDD_DDR
AJ12	DVSS
AJ13	AVDD08_DP
AJ14	AVDD18_DP
AJ15	AVDD18_DP
AJ16	DVSS
AJ17	VDDIO_Y
AJ18	DVSS
AJ19	DVSS
AJ20	DVSS
AJ21	AVDD33_HDMITX
AJ22	DVSS
AJ23	DVSS
AJ24	DVSS
AJ25	DVSS

BALL #	NET NAME
AJ26	AVSS_HPLL
AJ29	DVSS
AJ31	DVSS
AJ32	HDMITX_D2P
AJ33	HDMITX_REXT
AK2	DDR1_AC_23
AK3	DDR1_AC_4
AK4	DDR1_AC_5
AK5	DVSS
AK6	DDR1_PVREF
AK8	VDDQ
AK9	DVSS
AK10	VDD_DDR
AK11	DVSS
AK12	DVSS
AK13	AVDD08_DP
AK14	DVSS
AK15	DVSS
AK16	DVSS
AK17	DVSS
AK18	VDD18_AO
AK19	DVSS
AK20	DVSS
AK21	DVSS
AK22	DVSS
AK23	AVDD08_HDMIRX
AK24	AVDD33_HDMIRX
AK25	AVDD18_HDMIRX_ EARCTX
AK26	DVSS
AK28	HDMITX_ARCRXP
AK29	HDMITX_ARCRXN
AK30	HDMIRX_C_D2N
AK31	HDMIRX_C_D2P
AK32	HDMITX_D2N
AL1	DDR1_AC_20
AL2	DVSS

BALL #	NET NAME
AL3	DDR1_AC_9
AL4	DDR1_AC_12
AL5	DDR1_AC_1
AL6	DDR1_RST
AL8	DVSS
AL9	VDDQ
AL10	AVSS_DP
AL11	AVDD18_DDR_DP_PLL
AL12	DVSS
AL13	DVSS
AL14	DVSS
AL15	DVSS
AL16	VX1_LPP
AL17	VX1_LPN
AL18	DVSS
AL19	VX1_ATP
AL20	DVSS
AL21	DVSS
AL22	DVSS
AL23	DVSS
AL24	DVSS
AL25	AVDD08_HDMITX
AL26	DVSS
AL28	HDMIRX_C_D0N
AL29	HDMIRX_C_D0P
AL30	HDMIRX_C_D1N
AL31	HDMIRX_C_D1P
AL32	HDMITX_D1P
AL33	HDMITX_D1N
AM1	DDR1_AC_21
AM2	DVSS
AM3	DDR1_AC_13
AM5	DVSS
AM8	DVSS
AM9	DVSS
AM11	DVSS
AM12	VX1_B_4P

BALL #	NET NAME
AM14	GPIOY_1
AM15	VX1_A_5N
AM17	GPIOY_0
AM18	VX1_A_0N
AM20	GPIOY_4
AM21	GPIOB_3
AM23	VDDIO_B
AM24	GPIOB_12
AM26	DVSS
AM29	DVSS
AM31	DVSS
AM32	HDMITX_D0P
AM33	DVSS
AN2	DDR1_AC_8
AN3	DDR1_AC_0
AN4	DDR1_AC_6
AN5	DVSS
AN6	DDR1_DQ2
AN7	DDR1_PZQ
AN8	DDR1_DQ14
AN9	DVSS
AN10	VX1_B_7P
AN11	VX1_B_7N
AN12	VX1_B_4N
AN13	DVSS
AN14	GPIOY_2
AN15	VX1_A_5P
AN16	DVSS
AN17	DVSS
AN18	VX1_A_0P
AN19	DVSS
AN20	GPIOY_3
AN21	GPIOB_2
AN22	DVSS
AN23	GPIOB_10
AN24	GPIOB_11

BALL #	NET NAME
AN25	DVSS
AN26	DVSS
AN27	GPIOW_1
AN28	GPIOW_5
AN29	DVSS
AN30	HDMIRX_C_CLKN
AN31	HDMIRX_C_CLKP
AN32	HDMITX_D0N
AP1	DDR1_AC_2
AP2	DVSS
AP3	DDR1_AC_3
AP4	DDR1_DQ1
AP6	DDR1_DQ3
AP7	DDR1_DQM1
AP8	DDR1_DQ13
AP10	DVSS
AP11	VX1_B_6N
AP12	VX1_B_5N
AP14	VX1_B_1P
AP15	VX1_A_7P
AP17	VX1_A_3P
AP18	VX1_A_1P
AP20	GPIOB_1
AP21	GPIOB_0
AP23	GPIOB_5
AP24	GPIOB_7
AP26	GPIOB_8
AP27	HDMIRX_ARCTXN
AP28	HDMIRX_B_CLKP
AP29	HDMIRX_B_D0N
AP30	HDMIRX_B_D0P
AP31	DVSS
AP32	HDMITX_CLKP
AP33	HDMITX_CLKN
AR1	DDR1_AC_10
AR2	DDR1_AC_7

BALL #	NET NAME
AR3	DDR1_AC_26
AR4	DDR1_DQ7
AR6	DDR1_DQM0
AR7	DDR1_DQ12
AR8	DDR1_DQ9
AR9	DDR1_DQ10
AR10	DVSS
AR11	VX1_B_6P
AR12	VX1_B_5P
AR13	DVSS
AR14	VX1_B_1N
AR15	VX1_A_7N
AR16	DVSS
AR17	VX1_A_3N
AR18	VX1_A_1N
AR19	DVSS
AR20	GPIOY_8
AR21	GPIOY_9
AR22	DVSS
AR23	GPIOB_4
AR24	GPIOB_6
AR25	DVSS
AR26	GPIOB_9
AR27	HDMIRX_ARCTXP
AR28	HDMIRX_B_CLKN
AR30	HDMIRX_B_D1N
AR31	HDMIRX_B_D1P
AR32	HDMIRX_B_D2P
AR33	HDMIRX_A_D2P
AT1	DDR1_AC_11
AT2	DDR1_AC_14
AT3	DVSS
AT4	DDR1_DQ6
AT5	DDR1_DQ4
AT6	DDR1_DQSN0
AT7	DDR1_DQSP1

BALL #	NET NAME
AT8	DDR1_DQSN1
AT9	DVSS
AT10	DDR1_DQ11
AT11	DDR1_DQ15
AT12	DVSS
AT13	VX1_B_3N
AT14	VX1_B_2P
AT15	VX1_B_2N
AT16	VX1_A_6P
AT17	VX1_A_6N
AT18	VX1_A_4P
AT19	VX1_A_2P
AT20	DVSS
AT21	GPIOY_5
AT22	GPIOY_7
AT23	GPIOY_11
AT24	GPIOY_12
AT25	GPIOY_13
AT26	GPIOY_14
AT27	GPIOY_18
AT28	DVSS
AT29	HDMIRX_A_D0N
AT30	HDMIRX_A_D0P
AT31	DVSS
AT32	HDMIRX_B_D2N
AT33	HDMIRX_A_D2N
AU1	DVSS
AU2	DDR1_DQ0
AU3	DDR1_DQ5
AU5	DVSS
AU6	DDR1_DQSP0
AU7	DVSS
AU9	DDR1_DQ8
AU10	DVSS
AU12	DIF_REXT
AU13	VX1_B_3P

BALL #	NET NAME
AU15	VX1_B_0P
AU16	VX1_B_0N
AU18	VX1_A_4N
AU19	VX1_A_2N
AU21	GPIOY_6
AU22	GPIOY_10

BALL #	NET NAME
AU24	GPIOY_16
AU25	GPIOY_15
AU27	GPIOY_17
AU28	HDMIRX_A_CLKN
AU29	HDMIRX_A_CLKP
AU31	HDMIRX_A_D1N

BALL #	NET NAME
AU32	HDMIRX_A_D1P
AU33	DVSS

4.3 Pin Description

The pin assignments are described in the following table.

Table 4-1 Pin Assignments

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
Audio					
AU_AIL1	AI	-	Audio line in, left channel of port 1	AVDD18_ AUDIO	NC
AU_AIL2	AI	-	Audio line in, left channel of port 2	AVDD18_ AUDIO	NC
AU_AIR1	AI	-	Audio line in, right channel of port 1	AVDD18_ AUDIO	NC
AU_AIR2	AI	-	Audio line in, right channel of port 2	AVDD18_ AUDIO	NC
AU_LO1L	AO	-	Audio line out, left channel of port 1	AVDD18_ AUDIO	NC
AU_LO1R	AO	-	Audio line out, right channel of port 1	AVDD18_ AUDIO	NC
AU_REFP	A	-	Audio ADC/DAC positive reference voltage	AVDD18_ AUDIO	NC
AU_VMID	A	-	MID voltage of audio ADC/DAC	AVDD18_ AUDIO	NC
AVSS_ AUDIO	AP	-	Analog ground for Audio ADC/DAC	-	To VSS
AVDD18_ AUDIO	AP	-	Analog 1.8V for Audio Audio ADC/DAC	-	To 1.8V
MIPI CSI					
CSI_A_ CLKN	AI	-	MIPI CSI CLK negative input for channel A	AVDD18_ CSI	NC
CSI_A_ CLKP	AI	-	MIPI CSI CLK positive input for channel A	AVDD18_ CSI	NC
CSI_A_D0N	AIO	-	MIPI CSI channel A data 0 negative input	AVDD18_ CSI	NC
CSI_A_D0P	AIO	-	MIPI CSI channel A data 0 positive input	AVDD18_ CSI	NC
CSI_A_D1N	AIO	-	MIPI CSI channel A data 1 negative input	AVDD18_ CSI	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
CSI_A_D1P	AIO	-	MIPI CSI channel A data 1 positive input	AVDD18_ CSI	NC
CSI_A_D2N	AIO	-	MIPI CSI channel A data 2 or channel B data0 negative input	AVDD18_ CSI	NC
CSI_A_D2P	AIO	-	MIPI CSI channel A data 2 or channel B data0 positive input	AVDD18_ CSI	NC
CSI_A_D3N	AIO	-	MIPI CSI channel A data 3 or channel B data1 negative input	AVDD18_ CSI	NC
CSI_A_D3P	AIO	-	MIPI CSI channel A data 3 or channel B data1 positive input	AVDD18_ CSI	NC
CSI_B_ CLKN	AI	-	MIPI CSI CLK negative input for channel B	AVDD18_ CSI	NC
CSI_B_ CLKP	AI	-	MIPI CSI CLK positive input for channel B	AVDD18_ CSI	NC
CSI_C_ CLKN	AI	-	MIPI CSI CLK negative input for channel C	AVDD18_ CSI	NC
CSI_C_ CLKP	AI	-	MIPI CSI CLK positive input for channel C	AVDD18_ CSI	NC
CSI_C_D0N	AIO	-	MIPI CSI channel C data 0 negative input	AVDD18_ CSI	NC
CSI_C_D0P	AIO	-	MIPI CSI channel C data 0 positive input	AVDD18_ CSI	NC
CSI_C_D1N	AIO	-	MIPI CSI channel C data 1 negative input	AVDD18_ CSI	NC
CSI_C_D1P	AIO	-	MIPI CSI channel C data 1 positive input	AVDD18_ CSI	NC
CSI_C_D2N	AIO	-	MIPI CSI channel C data 2 or channel D data0 negative input	AVDD18_ CSI	NC
CSI_C_D2P	AIO	-	MIPI CSI channel C data 2 or channel D data0 positive input	AVDD18_ CSI	NC
CSI_C_D3N	AIO	-	MIPI CSI channel C data 3 or channel D data1 negative input	AVDD18_ CSI	NC
CSI_C_D3P	AIO	-	MIPI CSI channel C data 3 or channel D data1 positive input	AVDD18_ CSI	NC
CSI_D_ CLKN	AI	-	MIPI CSI CLK negative input for channel D	AVDD18_ CSI	NC
CSI_D_ CLKP	AI	-	MIPI CSI CLK positive input for channel D	AVDD18_ CSI	NC
AVDD0V8_ CSI	AP	-	Analog Power supply 0.8V for MIPI CSI	-	To 0.8V
AVDD18_ CSI	AP	-	Analog 1.8V power supply for MIPI CSI	-	To 1.8V
DDR0					
DDR0_AC_ 0	DO	-	DDR PHY0 address/command/control signal bit 0	VDDQ	NC
DDR0_AC_ 1	DO	-	DDR PHY0 address/command/control signal bit 1	VDDQ	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
DDR0_AC_2	DO	-	DDR PHY0 address/command/control signal bit 2	VDDQ	NC
DDR0_AC_3	DO	-	DDR PHY0 address/command/control signal bit 3	VDDQ	NC
DDR0_AC_4	DO	-	DDR PHY0 address/command/control signal bit 4	VDDQ	NC
DDR0_AC_5	DO	-	DDR PHY0 address/command/control signal bit 5	VDDQ	NC
DDR0_AC_6	DO	-	DDR PHY0 address/command/control signal bit 6	VDDQ	NC
DDR0_AC_7	DO	-	DDR PHY0 address/command/control signal bit 7	VDDQ	NC
DDR0_AC_8	DO	-	DDR PHY0 address/command/control signal bit 8	VDDQ	NC
DDR0_AC_9	DO	-	DDR PHY0 address/command/control signal bit 9	VDDQ	NC
DDR0_AC_10	DO	-	DDR PHY0 address/command/control signal bit 10	VDDQ	NC
DDR0_AC_11	DO	-	DDR PHY0 address/command/control signal bit 11	VDDQ	NC
DDR0_AC_12	DO	-	DDR PHY0 address/command/control signal bit 12	VDDQ	NC
DDR0_AC_13	DO	-	DDR PHY0 address/command/control signal bit 13	VDDQ	NC
DDR0_AC_14	DO	-	DDR PHY0 address/command/control signal bit 14	VDDQ	NC
DDR0_AC_15	DO	-	DDR PHY0 address/command/control signal bit 15	VDDQ	NC
DDR0_AC_20	DO	-	DDR PHY0 address/command/control signal bit 20	VDDQ	NC
DDR0_AC_21	DO	-	DDR PHY0 address/command/control signal bit 21	VDDQ	NC
DDR0_AC_22	DO	-	DDR PHY0 address/command/control signal bit 22	VDDQ	NC
DDR0_AC_23	DO	-	DDR PHY0 address/command/control signal bit 23	VDDQ	NC
DDR0_AC_24	DO	-	DDR PHY0 address/command/control signal bit 24	VDDQ	NC
DDR0_AC_25	DO	-	DDR PHY0 address/command/control signal bit 25	VDDQ	NC
DDR0_AC_26	DO	-	DDR PHY0 address/command/control signal bit 26	VDDQ	NC
DDR0_AC_28	DO	-	DDR PHY0 address/command/control signal bit 28	VDDQ	NC
DDR0_AC_29	DO	-	DDR PHY0 address/command/control signal bit 29	VDDQ	NC
DDR0_AC_30	DO	-	DDR PHY0 address/command/control signal bit 30	VDDQ	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
DDR0_AC_31	DO	-	DDR PHY0 address/command/control signal bit 31	VDDQ	NC
DDR0_AC_32	DO	-	DDR PHY0 address/command/control signal bit 32	VDDQ	NC
DDR0_AC_33	DO	-	DDR PHY0 address/command/control signal bit 33	VDDQ	NC
DDR0_AC_34	DO	-	DDR PHY0 address/command/control signal bit 34	VDDQ	NC
DDR0_AC_35	DO	-	DDR PHY0 address/command/control signal bit 35	VDDQ	NC
DDR0_AC_36	DO	-	DDR PHY0 address/command/control signal bit 36	VDDQ	NC
DDR0_AC_37	DO	-	DDR PHY0 address/command/control signal bit 37	VDDQ	NC
DDR0_AC_38	DO	-	DDR PHY0 address/command/control signal bit 38	VDDQ	NC
DDR0_DQ0	DIO	-	DRAM0 data bus bit 0	VDDQ	To DRAM0
DDR0_DQ1	DIO	-	DRAM0 data bus bit 1	VDDQ	To DRAM0
DDR0_DQ2	DIO	-	DRAM0 data bus bit 2	VDDQ	To DRAM0
DDR0_DQ3	DIO	-	DRAM0 data bus bit 3	VDDQ	To DRAM0
DDR0_DQ4	DIO	-	DRAM0 data bus bit 4	VDDQ	To DRAM0
DDR0_DQ5	DIO	-	DRAM0 data bus bit 5	VDDQ	To DRAM0
DDR0_DQ6	DIO	-	DRAM0 data bus bit 6	VDDQ	To DRAM0
DDR0_DQ7	DIO	-	DRAM0 data bus bit 7	VDDQ	To DRAM0
DDR0_DQ8	DIO	-	DRAM0 data bus bit 8	VDDQ	To DRAM0
DDR0_DQ9	DIO	-	DRAM0 data bus bit 9	VDDQ	To DRAM0
DDR0_DQ10	DIO	-	DRAM0 data bus bit 10	VDDQ	To DRAM0
DDR0_DQ11	DIO	-	DRAM0 data bus bit 11	VDDQ	To DRAM0
DDR0_DQ12	DIO	-	DRAM0 data bus bit 12	VDDQ	To DRAM0
DDR0_DQ13	DIO	-	DRAM0 data bus bit 13	VDDQ	To DRAM0
DDR0_DQ14	DIO	-	DRAM0 data bus bit 14	VDDQ	To DRAM0
DDR0_DQ15	DIO	-	DRAM0 data bus bit 15	VDDQ	To DRAM0

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
DDR0_DQ16	DIO	-	DRAM0 data bus bit 16	VDDQ	NC
DDR0_DQ17	DIO	-	DRAM0 data bus bit 17	VDDQ	NC
DDR0_DQ18	DIO	-	DRAM0 data bus bit 18	VDDQ	NC
DDR0_DQ19	DIO	-	DRAM0 data bus bit 19	VDDQ	NC
DDR0_DQ20	DIO	-	DRAM0 data bus bit 20	VDDQ	NC
DDR0_DQ21	DIO	-	DRAM0 data bus bit 21	VDDQ	NC
DDR0_DQ22	DIO	-	DRAM0 data bus bit 22	VDDQ	NC
DDR0_DQ23	DIO	-	DRAM0 data bus bit 23	VDDQ	NC
DDR0_DQ24	DIO	-	DRAM0 data bus bit 24	VDDQ	NC
DDR0_DQ25	DIO	-	DRAM0 data bus bit 25	VDDQ	NC
DDR0_DQ26	DIO	-	DRAM0 data bus bit 26	VDDQ	NC
DDR0_DQ27	DIO	-	DRAM0 data bus bit 27	VDDQ	NC
DDR0_DQ28	DIO	-	DRAM0 data bus bit 28	VDDQ	NC
DDR0_DQ29	DIO	-	DRAM0 data bus bit 29	VDDQ	NC
DDR0_DQ30	DIO	-	DRAM0 data bus bit 30	VDDQ	NC
DDR0_DQ31	DIO	-	DRAM0 data bus bit 31	VDDQ	NC
DDR0_DQM0	DIO	-	DRAM0 data mask 0	VDDQ	To DRAM0
DDR0_DQM1	DIO	-	DRAM0 data mask 1	VDDQ	To DRAM0
DDR0_DQM2	DIO	-	DRAM0 data mask 2	VDDQ	NC
DDR0_DQM3	DIO	-	DRAM0 data mask 3	VDDQ	NC
DDR0_DQSN0	DIO	-	DRAM0 data strobe 0 complementary	VDDQ	To DRAM0
DDR0_DQSN1	DIO	-	DRAM0 data strobe 1 complementary	VDDQ	To DRAM0
DDR0_DQSN2	DIO	-	DRAM0 data strobe 2 complementary	VDDQ	NC
DDR0_DQSN3	DIO	-	DRAM0 data strobe 3 complementary	VDDQ	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
DDR0_ DQSP0	DIO	-	DRAM0 data strobe 0	VDDQ	To DRAM0
DDR0_ DQSP1	DIO	-	DRAM0 data strobe 1	VDDQ	To DRAM0
DDR0_ DQSP2	DIO	-	DRAM0 data strobe 2	VDDQ	NC
DDR0_ DQSP3	DIO	-	DRAM0 data strobe 3	VDDQ	NC
DDR0_ PVREF			DRAM0 reference voltage	VDDQ	To GND by ca-pacitor
DDR0_PZQ	A	-	DRAM0 reference pin for ZQ calibration	VDDQ	To GND by 240ohm
DDR0_RST	DO	-	DRAM0 DDR4/LPDDR4/LPDDR4X RSTn	VDDQ	NC
AVDD_ DDR0PLL	P	-	Analog power supply for DDR0PLL	-	To DDR VDDQ
DDR1					
DDR1_AC_ 0	DO	-	DDR PHY1 address/command/control signal bit 0	VDDQ	NC
DDR1_AC_ 1	DO	-	DDR PHY1 address/command/control signal bit 1	VDDQ	NC
DDR1_AC_ 2	DO	-	DDR PHY1 address/command/control signal bit 2	VDDQ	NC
DDR1_AC_ 3	DO	-	DDR PHY1 address/command/control signal bit 3	VDDQ	NC
DDR1_AC_ 4	DO	-	DDR PHY1 address/command/control signal bit 4	VDDQ	NC
DDR1_AC_ 5	DO	-	DDR PHY1 address/command/control signal bit 5	VDDQ	NC
DDR1_AC_ 6	DO	-	DDR PHY1 address/command/control signal bit 6	VDDQ	NC
DDR1_AC_ 7	DO	-	DDR PHY1 address/command/control signal bit 7	VDDQ	NC
DDR1_AC_ 8	DO	-	DDR PHY1 address/command/control signal bit 8	VDDQ	NC
DDR1_AC_ 9	DO	-	DDR PHY1 address/command/control signal bit 9	VDDQ	NC
DDR1_AC_ 10	DO	-	DDR PHY1 address/command/control signal bit 10	VDDQ	NC
DDR1_AC_ 11	DO	-	DDR PHY1 address/command/control signal bit 11	VDDQ	NC
DDR1_AC_ 12	DO	-	DDR PHY1 address/command/control signal bit 12	VDDQ	NC
DDR1_AC_ 13	DO	-	DDR PHY1 address/command/control signal bit 13	VDDQ	NC
DDR1_AC_ 14	DO	-	DDR PHY1 address/command/control signal bit 14	VDDQ	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
DDR1_AC_15	DO	-	DDR PHY1 address/command/control signal bit 15	VDDQ	NC
DDR1_AC_20	DO	-	DDR PHY1 address/command/control signal bit 20	VDDQ	NC
DDR1_AC_21	DO	-	DDR PHY1 address/command/control signal bit 21	VDDQ	NC
DDR1_AC_22	DO	-	DDR PHY1 address/command/control signal bit 22	VDDQ	NC
DDR1_AC_23	DO	-	DDR PHY1 address/command/control signal bit 23	VDDQ	NC
DDR1_AC_24	DO	-	DDR PHY1 address/command/control signal bit 24	VDDQ	NC
DDR1_AC_25	DO	-	DDR PHY1 address/command/control signal bit 25	VDDQ	NC
DDR1_AC_26	DO	-	DDR PHY1 address/command/control signal bit 26	VDDQ	NC
DDR1_AC_28	DO	-	DDR PHY1 address/command/control signal bit 28	VDDQ	NC
DDR1_AC_29	DO	-	DDR PHY1 address/command/control signal bit 29	VDDQ	NC
DDR1_AC_30	DO	-	DDR PHY1 address/command/control signal bit 30	VDDQ	NC
DDR1_AC_31	DO	-	DDR PHY1 address/command/control signal bit 31	VDDQ	NC
DDR1_AC_32	DO	-	DDR PHY1 address/command/control signal bit 32	VDDQ	NC
DDR1_AC_33	DO	-	DDR PHY1 address/command/control signal bit 33	VDDQ	NC
DDR1_AC_34	DO	-	DDR PHY1 address/command/control signal bit 34	VDDQ	NC
DDR1_AC_35	DO	-	DDR PHY1 address/command/control signal bit 35	VDDQ	NC
DDR1_AC_36	DO	-	DDR PHY1 address/command/control signal bit 36	VDDQ	NC
DDR1_AC_37	DO	-	DDR PHY1 address/command/control signal bit 37	VDDQ	NC
DDR1_AC_38	DO	-	DDR PHY1 address/command/control signal bit 38	VDDQ	NC
DDR1_DQ0	DIO	-	DRAM1 data bus bit 0	VDDQ	To DRAM1
DDR1_DQ1	DIO	-	DRAM1 data bus bit 1	VDDQ	To DRAM1
DDR1_DQ2	DIO	-	DRAM1 data bus bit 2	VDDQ	To DRAM1
DDR1_DQ3	DIO	-	DRAM1 data bus bit 3	VDDQ	To DRAM1
DDR1_DQ4	DIO	-	DRAM1 data bus bit 4	VDDQ	To DRAM1

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
DDR1_DQ5	DIO	-	DRAM1 data bus bit 5	VDDQ	To DRAM1
DDR1_DQ6	DIO	-	DRAM1 data bus bit 6	VDDQ	To DRAM1
DDR1_DQ7	DIO	-	DRAM1 data bus bit 7	VDDQ	To DRAM1
DDR1_DQ8	DIO	-	DRAM1 data bus bit 8	VDDQ	To DRAM1
DDR1_DQ9	DIO	-	DRAM1 data bus bit 9	VDDQ	To DRAM1
DDR1_DQ10	DIO	-	DRAM1 data bus bit 10	VDDQ	To DRAM1
DDR1_DQ11	DIO	-	DRAM1 data bus bit 11	VDDQ	To DRAM1
DDR1_DQ12	DIO	-	DRAM1 data bus bit 12	VDDQ	To DRAM1
DDR1_DQ13	DIO	-	DRAM1 data bus bit 13	VDDQ	To DRAM1
DDR1_DQ14	DIO	-	DRAM1 data bus bit 14	VDDQ	To DRAM1
DDR1_DQ15	DIO	-	DRAM1 data bus bit 15	VDDQ	To DRAM1
DDR1_DQ16	DIO	-	DRAM1 data bus bit 16	VDDQ	NC
DDR1_DQ17	DIO	-	DRAM1 data bus bit 17	VDDQ	NC
DDR1_DQ18	DIO	-	DRAM1 data bus bit 18	VDDQ	NC
DDR1_DQ19	DIO	-	DRAM1 data bus bit 19	VDDQ	NC
DDR1_DQ20	DIO	-	DRAM1 data bus bit 20	VDDQ	NC
DDR1_DQ21	DIO	-	DRAM1 data bus bit 21	VDDQ	NC
DDR1_DQ22	DIO	-	DRAM1 data bus bit 22	VDDQ	NC
DDR1_DQ23	DIO	-	DRAM1 data bus bit 23	VDDQ	NC
DDR1_DQ24	DIO	-	DRAM1 data bus bit 24	VDDQ	NC
DDR1_DQ25	DIO	-	DRAM1 data bus bit 25	VDDQ	NC
DDR1_DQ26	DIO	-	DRAM1 data bus bit 26	VDDQ	NC
DDR1_DQ27	DIO	-	DRAM1 data bus bit 27	VDDQ	NC
DDR1_DQ28	DIO	-	DRAM1 data bus bit 28	VDDQ	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
DDR1_DQ29	DIO	-	DRAM1 data bus bit 29	VDDQ	NC
DDR1_DQ30	DIO	-	DRAM1 data bus bit 30	VDDQ	NC
DDR1_DQ31	DIO	-	DRAM1 data bus bit 31	VDDQ	NC
DDR1_DQM0	DIO	-	DRAM1 data mask 0	VDDQ	To DRAM1
DDR1_DQM1	DIO	-	DRAM1 data mask 1	VDDQ	To DRAM1
DDR1_DQM2	DIO	-	DRAM1 data mask 2	VDDQ	NC
DDR1_DQM3	DIO	-	DRAM1 data mask 3	VDDQ	NC
DDR1_DQSN0	DIO	-	DRAM1 data strobe 0 complementary	VDDQ	To DRAM1
DDR1_DQSN1	DIO	-	DRAM1 data strobe 1 complementary	VDDQ	To DRAM1
DDR1_DQSN2	DIO	-	DRAM1 data strobe 2 complementary	VDDQ	NC
DDR1_DQSN3	DIO	-	DRAM1 data strobe 3 complementary	VDDQ	NC
DDR1_DQSP0	DIO	-	DRAM1 data strobe 0	VDDQ	To DRAM1
DDR1_DQSP1	DIO	-	DRAM1 data strobe 1	VDDQ	To DRAM1
DDR1_DQSP2	DIO	-	DRAM1 data strobe 2	VDDQ	NC
DDR1_DQSP3	DIO	-	DRAM1 data strobe 3	VDDQ	NC
DDR1_PVREF	0	0	DRAM1 reference voltage	VDDQ	To GND by capacitor
DDR1_PZQ	A	-	DRAM1 reference pin for ZQ calibration	VDDQ	To GND by 240ohm
DDR1_RST	DO	-	DRAM1 DDR4/LPDDR4/LPDDR4X RSTn	VDDQ	NC
AVDD_DDR1PLL	P	-	Analog power supply for DDR1PLL	-	To DDR VDDQ
Ethernet					
ENET_ATP	AIO	-	Ethernet PHY analog test pin	AVDD18_ENET	NC
ENET_EXTRES	A	-	Ethernet PHY external resistor connection	AVDD18_ENET	NC
ENET_RXN	AIO	-	Ethernet PHY receive date negative input	AVDD18_ENET	NC
ENET_RXP	AIO	-	Ethernet PHY receive data positive input	AVDD18_ENET	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
ENET_TXN	AIO	-	Ethernet PHY transmit data negative output	AVDD18_ ENET	NC
ENET_TXP	AIO	-	Ethernet PHY transmit data positive output	AVDD18_ ENET	NC
AVDD18_ ENET	AP	-	Analog 1.8V power supply for Ethernet module	-	To 1.8V
GPIOB- refer to Table 4-6 for functional multiplex information.					
GPIOB_0	DIO	Up	General purpose input/output bank B signal 0	VDDIO_B	NC
GPIOB_1	DIO	Up	General purpose input/output bank B signal 1	VDDIO_B	NC
GPIOB_2	DIO	Up	General purpose input/output bank B signal 2	VDDIO_B	NC
GPIOB_3	DIO	Up	General purpose input/output bank B signal 3	VDDIO_B	NC
GPIOB_4	DIO	Up	General purpose input/output bank B signal 4	VDDIO_B	NC
GPIOB_5	DIO	Up	General purpose input/output bank B signal 5	VDDIO_B	NC
GPIOB_6	DIO	Up	General purpose input/output bank B signal 6	VDDIO_B	NC
GPIOB_7	DIO	Up	General purpose input/output bank B signal 7	VDDIO_B	NC
GPIOB_8	DIO	Up	General purpose input/output bank B signal 8	VDDIO_B	NC
GPIOB_9	DIO	Down	General purpose input/output bank B signal 9	VDDIO_B	NC
GPIOB_10	DIO	Up	General purpose input/output bank B signal 10	VDDIO_B	NC
GPIOB_11	DIO	Down	General purpose input/output bank B signal 11	VDDIO_B	NC
GPIOB_12	DIO	Up	General purpose input/output bank B signal 12	VDDIO_B	NC
VDDIO_B	P	-	Power supply for GPIO bank B	-	To 1.8V or 3.3V
GPIOC- refer to Table 4-6 for functional multiplex information.					
GPIOC_0	DIO	Up	General purpose input/output bank C signal 0	VDDIO_C	NC
GPIOC_1	DIO	Up	General purpose input/output bank C signal 1	VDDIO_C	NC
GPIOC_2	DIO	Up	General purpose input/output bank C signal 2	VDDIO_C	NC
GPIOC_3	DIO	Up	General purpose input/output bank C signal 3	VDDIO_C	NC
GPIOC_4	DIO	Up	General purpose input/output bank C signal 4	VDDIO_C	NC
GPIOC_5	DIO	Up	General purpose input/output bank C signal 5	VDDIO_C	NC
GPIOC_6	DIO	Up	General purpose input/output bank C signal 6	VDDIO_C	NC
VDDIO_C	P	-	Power supply for GPIO bank C	-	To 1.8V or 3.3V
GPIOX- refer to Table 4-11 for functional multiplex information.					
GPIOX_0	DIO	Up	General purpose input/output bank X signal 0	VDDIO_X	NC
GPIOX_1	DIO	Up	General purpose input/output bank X signal 1	VDDIO_X	NC
GPIOX_2	DIO	Up	General purpose input/output bank X signal 2	VDDIO_X	NC
GPIOX_3	DIO	Up	General purpose input/output bank X signal 3	VDDIO_X	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
GPIOX_4	DIO	Up	General purpose input/output bank X signal 4	VDDIO_X	NC
GPIOX_5	DIO	Up	General purpose input/output bank X signal 5	VDDIO_X	NC
GPIOX_6	DIO	Down	General purpose input/output bank X signal 6	VDDIO_X	NC
GPIOX_7	DIO	Up	General purpose input/output bank X signal 7	VDDIO_X	NC
GPIOX_8	DIO	Up	General purpose input/output bank X signal 8	VDDIO_X	NC
GPIOX_9	DIO	Up	General purpose input/output bank X signal 9	VDDIO_X	NC
GPIOX_10	DIO	Up	General purpose input/output bank X signal 10	VDDIO_X	NC
GPIOX_11	DIO	Up	General purpose input/output bank X signal 11	VDDIO_X	NC
GPIOX_12	DIO	Up	General purpose input/output bank X signal 12	VDDIO_X	NC
GPIOX_13	DIO	Up	General purpose input/output bank X signal 13	VDDIO_X	NC
GPIOX_14	DIO	Up	General purpose input/output bank X signal 14	VDDIO_X	NC
GPIOX_15	DIO	Up	General purpose input/output bank X signal 15	VDDIO_X	NC
GPIOX_16	DIO	Up	General purpose input/output bank X signal 16	VDDIO_X	NC
GPIOX_17	DIO	Down	General purpose input/output bank X signal 17	VDDIO_X	NC
GPIOX_18	DIO	Up	General purpose input/output bank X signal 18	VDDIO_X	NC
GPIOX_19	DIO	HiZ	General purpose input/output bank X signal 19	VDDIO_X	NC
VDDIO_X	P	-	Power supply for GPIO bank X	-	To 1.8V or 3.3V
GPIOW- refer to Table 4-2 for functional multiplex information.					
GPIOW_0	OD_5V	HiZ	General purpose input/output bank W signal 0	-	NC
GPIOW_1	OD_5V (Input only)	HiZ	General purpose input bank W signal 1	-	NC
GPIOW_2	OD_5V	HiZ	General purpose input/output bank W signal 2	-	NC
GPIOW_3	OD_5V	HiZ	General purpose input/output bank W signal 3	-	NC
GPIOW_4	OD_5V	HiZ	General purpose input/output bank W signal 4	-	NC
GPIOW_5	OD_5V (Input only)	HiZ	General purpose input bank W signal 5	-	NC
GPIOW_6	OD_5V	HiZ	General purpose input/output bank W signal 6	-	NC
GPIOW_7	OD_5V	HiZ	General purpose input/output bank W signal 7	-	NC
GPIOW_8	OD_5V	HiZ	General purpose input/output bank W signal 8	-	NC
GPIOW_9	OD_5V (Input only)	HiZ	General purpose input bank W signal 9	-	NC
GPIOW_10	OD_5V	HiZ	General purpose input/output bank W signal 10	-	NC
GPIOW_11	OD_5V	HiZ	General purpose input/output bank W signal 11	-	NC
GPIOW_12	OD_5V	HiZ	General purpose input/output bank W signal 12	-	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
GPIOW_13	OD_5V	HiZ	General purpose input/output bank W signal 13	-	NC
GPIOW_14	OD_5V	HiZ	General purpose input/output bank W signal 14	-	NC
GPIOW_15	OD_5V	HiZ	General purpose input/output bank W signal 15	-	NC
GPIOW_16	OD_5V	HiZ	General purpose input/output bank W signal 16	-	NC
GPIOD- refer to Table 4-11 for functional multiplex information.					
GPIOD_0	DIO	Up	General purpose input/output bank D signal 0	VDDIO_D	NC
GPIOD_1	DIO	Up	General purpose input/output bank D signal 1	VDDIO_D	NC
GPIOD_2	DIO	Up	General purpose input/output bank D signal 2	VDDIO_D	NC
GPIOD_3	DIO	Up	General purpose input/output bank D signal 3	VDDIO_D	NC
GPIOD_4	DIO	Down	General purpose input/output bank D signal 4	VDDIO_D	NC
GPIOD_5	DIO	Up	General purpose input/output bank D signal 5	VDDIO_D	NC
GPIOD_6	DIO	Down	General purpose input/output bank D signal 6	VDDIO_D	NC
GPIOD_7	DIO	Down	General purpose input/output bank D signal 7	VDDIO_D	NC
GPIOD_8	DIO	Down	General purpose input/output bank D signal 8	VDDIO_D	NC
GPIOD_9	DIO	Down	General purpose input/output bank D signal 9	VDDIO_D	NC
GPIOD_10	DIO	Up	General purpose input/output bank D signal 10	VDDIO_D	NC
GPIOD_11	DIO	Down	General purpose input/output bank D signal 11	VDDIO_D	NC
GPIOD_12	DIO	HiZ	General purpose input/output bank D signal 12	VDDIO_D	NC
RESET_N	DIO	HiZ	System reset input		To RESET_N
TEST_N	DIO	Up	SOC test pin should be pulled up during normal power-on.		NC
VDDIO_D	P	-	Power supply for GPIO bank D	-	To 1.8V or 3.3V
GPIOE- refer to Table 4-11 for functional multiplex information.					
GPIOE_0	DIO	HiZ	General purpose input/output bank E signal 0	VDDIO_E	NC
GPIOE_1	DIO	HiZ	General purpose input/output bank E signal 1	VDDIO_E	NC
GPIOE_2	DIO	Down	General purpose input/output bank E signal 2	VDDIO_E	NC
GPIOE_3	DIO	HiZ	General purpose input/output bank E signal 3	VDDIO_E	NC
GPIOE_4	DIO	HiZ	General purpose input/output bank E signal 4	VDDIO_E	NC
GPIOE_5	DIO	HiZ	General purpose input/output bank E signal 5	VDDIO_E	NC
GPIOE_6	DIO	HiZ	General purpose input/output bank E signal 6	VDDIO_E	NC
VDDIO_E	P	-	Power supply for GPIO bank E	-	To 1.8V or 3.3V
GPIOZ- refer to Table 4-7 for functional multiplex information.					
GPIOZ_0	DIO	Up	General purpose input/output bank Z signal 0	VDDIO_Z	NC
GPIOZ_1	DIO	Up	General purpose input/output bank Z signal 1	VDDIO_Z	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
GPIOZ_2	DIO	Up	General purpose input/output bank Z signal 2	VDDIO_Z	NC
GPIOZ_3	DIO	Up	General purpose input/output bank Z signal 3	VDDIO_Z	NC
GPIOZ_4	DIO	Up	General purpose input/output bank Z signal 4	VDDIO_Z	NC
GPIOZ_5	DIO	Up	General purpose input/output bank Z signal 5	VDDIO_Z	NC
GPIOZ_6	DIO	Up	General purpose input/output bank Z signal 6	VDDIO_Z	NC
GPIOZ_7	DIO	Up	General purpose input/output bank Z signal 7	VDDIO_Z	NC
GPIOZ_8	DIO	Up	General purpose input/output bank Z signal 8	VDDIO_Z	NC
GPIOZ_9	DIO	Down	General purpose input/output bank Z signal 9	VDDIO_Z	NC
GPIOZ_10	DIO	Down	General purpose input/output bank Z signal 10	VDDIO_Z	NC
GPIOZ_11	DIO	Down	General purpose input/output bank Z signal 11	VDDIO_Z	NC
GPIOZ_12	DIO	Down	General purpose input/output bank Z signal 12	VDDIO_Z	NC
GPIOZ_13	DIO	Down	General purpose input/output bank Z signal 13	VDDIO_Z	NC
VDDIO_Z	P	-	Power supply for GPIO bank Z	-	To 1.8V or 3.3V
GPIOT- refer to Table 4-11 for functional multiplex information.					
GPIOT_0	DIO	Down	General purpose input/output bank T signal 0	VDDIO_T	NC
GPIOT_1	DIO	Down	General purpose input/output bank T signal 1	VDDIO_T	NC
GPIOT_2	DIO	Down	General purpose input/output bank T signal 2	VDDIO_T	NC
GPIOT_3	DIO	Down	General purpose input/output bank T signal 3	VDDIO_T	NC
GPIOT_4	DIO	Down	General purpose input/output bank T signal 4	VDDIO_T	NC
GPIOT_5	DIO	Down	General purpose input/output bank T signal 5	VDDIO_T	NC
GPIOT_6	DIO	Down	General purpose input/output bank T signal 6	VDDIO_T	NC
GPIOT_7	DIO	Down	General purpose input/output bank T signal 7	VDDIO_T	NC
GPIOT_8	DIO	Down	General purpose input/output bank T signal 8	VDDIO_T	NC
GPIOT_9	DIO	Down	General purpose input/output bank T signal 9	VDDIO_T	NC
GPIOT_10	DIO	Down	General purpose input/output bank T signal 10	VDDIO_T	NC
GPIOT_11	DIO	Down	General purpose input/output bank T signal 11	VDDIO_T	NC
GPIOT_12	DIO	Down	General purpose input/output bank T signal 12	VDDIO_T	NC
GPIOT_13	DIO	Down	General purpose input/output bank T signal 13	VDDIO_T	NC
GPIOT_14	DIO	Down	General purpose input/output bank T signal 14	VDDIO_T	NC
GPIOT_15	DIO	Down	General purpose input/output bank T signal 15	VDDIO_T	NC
GPIOT_16	DIO	Down	General purpose input/output bank T signal 16	VDDIO_T	NC
GPIOT_17	DIO	Down	General purpose input/output bank T signal 17	VDDIO_T	NC
GPIOT_18	DIO	Down	General purpose input/output bank T signal 18	VDDIO_T	NC
GPIOT_19	DIO	Down	General purpose input/output bank T signal 19	VDDIO_T	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
GPIOT_20	DIO	Down	General purpose input/output bank T signal 20	VDDIO_T	NC
GPIOT_21	DIO	Down	General purpose input/output bank T signal 21	VDDIO_T	NC
GPIOT_22	DIO	Down	General purpose input/output bank T signal 22	VDDIO_T	NC
GPIOT_23	DIO	Down	General purpose input/output bank T signal 23	VDDIO_T	NC
VDDIO_T	P	-	Power supply for GPIO bank T	-	To 1.8V or 3.3V
GPIOM- refer to Table 4-11 for functional multiplex information.					
GPIOM_0	DIO	Down	General purpose input/output bank M signal 0	VDDIO_M	NC
GPIOM_1	DIO	Down	General purpose input/output bank M signal 1	VDDIO_M	NC
GPIOM_2	DIO	Down	General purpose input/output bank M signal 2	VDDIO_M	NC
GPIOM_3	DIO	Down	General purpose input/output bank M signal 3	VDDIO_M	NC
GPIOM_4	DIO	Down	General purpose input/output bank M signal 4	VDDIO_M	NC
GPIOM_5	DIO	Down	General purpose input/output bank M signal 5	VDDIO_M	NC
GPIOM_6	DIO	Up	General purpose input/output bank M signal 6	VDDIO_M	NC
GPIOM_7	DIO	Up	General purpose input/output bank M signal 7	VDDIO_M	NC
GPIOM_8	DIO	Down	General purpose input/output bank M signal 8	VDDIO_M	NC
GPIOM_9	DIO	Down	General purpose input/output bank M signal 9	VDDIO_M	NC
GPIOM_10	DIO	Down	General purpose input/output bank M signal 10	VDDIO_M	NC
GPIOM_11	DIO	Down	General purpose input/output bank M signal 11	VDDIO_M	NC
GPIOM_12	DIO	Up	General purpose input/output bank M signal 12	VDDIO_M	NC
GPIOM_13	DIO	Up	General purpose input/output bank M signal 13	VDDIO_M	NC
VDDIO_M	P	-	Power supply for GPIO bank M	-	To 1.8V or 3.3V
GPIOY- refer to Table 4-14 for functional multiplex information.					
GPIOY_0	DIO	Down	General purpose input/output bank Y signal 0	VDDIO_Y	NC
GPIOY_1	DIO	Down	General purpose input/output bank Y signal 1	VDDIO_Y	NC
GPIOY_2	DIO	Down	General purpose input/output bank Y signal 2	VDDIO_Y	NC
GPIOY_3	DIO	Up	General purpose input/output bank Y signal 3	VDDIO_Y	NC
GPIOY_4	DIO	Up	General purpose input/output bank Y signal 4	VDDIO_Y	NC
GPIOY_5	DIO	Up	General purpose input/output bank Y signal 5	VDDIO_Y	NC
GPIOY_6	DIO	Up	General purpose input/output bank Y signal 6	VDDIO_Y	NC
GPIOY_7	DIO	Down	General purpose input/output bank Y signal 7	VDDIO_Y	NC
GPIOY_8	DIO	Down	General purpose input/output bank Y signal 8	VDDIO_Y	NC
GPIOY_9	DIO	Down	General purpose input/output bank Y signal 9	VDDIO_Y	NC
GPIOY_10	DIO	Up	General purpose input/output bank Y signal 10	VDDIO_Y	NC
GPIOY_11	DIO	Up	General purpose input/output bank Y signal 11	VDDIO_Y	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
GPIOY_12	DIO	Up	General purpose input/output bank Y signal 12	VDDIO_Y	NC
GPIOY_13	DIO	Up	General purpose input/output bank Y signal 13	VDDIO_Y	NC
GPIOY_14	DIO	Down	General purpose input/output bank Y signal 14	VDDIO_Y	NC
GPIOY_15	DIO	Up	General purpose input/output bank Y signal 15	VDDIO_Y	NC
GPIOY_16	DIO	Down	General purpose input/output bank Y signal 16	VDDIO_Y	NC
GPIOY_17	DIO	Up	General purpose input/output bank Y signal 17	VDDIO_Y	NC
GPIOY_18	DIO	Up	General purpose input/output bank Y signal 18	VDDIO_Y	NC
VDDIO_Y	P	-	Power supply for GPIO bank Y	-	To 1.8V or 3.3V
GPIOH- refer to Table 4-14 for functional multiplex information.					
GPIOH_0	DIO	Up	General purpose input/output bank H signal 0	VDDIO_H	NC
GPIOH_1	DIO	HiZ	General purpose input/output bank H signal 1	VDDIO_H	NC
GPIOH_2	DIO	Down	General purpose input/output bank H signal 2	VDDIO_H	NC
GPIOH_3	DIO	Up	General purpose input/output bank H signal 3	VDDIO_H	NC
GPIOH_4	DIO	Down	General purpose input/output bank H signal 4	VDDIO_H	NC
GPIOH_5	DIO	Down	General purpose input/output bank H signal 5	VDDIO_H	NC
GPIOH_6	DIO	HiZ	General purpose input/output bank H signal 6	VDDIO_H	NC
GPIOH_7	DIO	HiZ	General purpose input/output bank H signal 7	VDDIO_H	NC
VDDIO_H	P	-	Power supply for GPIO bank H	-	To 1.8V or 3.3V
HDMI RX					
HDMIRX_A_CLKN	AI	-	HDMIRX Port A TMDS clock negative input	AVDD33_HDMIRX	NC
HDMIRX_A_CLKP	AI	-	HDMIRX Port A TMDS clock positive input	AVDD33_HDMIRX	NC
HDMIRX_A_D0N	AI	-	HDMIRX Port A TMDS data0 negative input	AVDD33_HDMIRX	NC
HDMIRX_A_D0P	AI	-	HDMIRX Port A TMDS data0 positive input	AVDD33_HDMIRX	NC
HDMIRX_A_D1N	AI	-	HDMIRX Port A TMDS data1 negative input	AVDD33_HDMIRX	NC
HDMIRX_A_D1P	AI	-	HDMIRX Port A TMDS data1 positive input	AVDD33_HDMIRX	NC
HDMIRX_A_D2N	AI	-	HDMIRX Port A TMDS data2 negative input	AVDD33_HDMIRX	NC
HDMIRX_A_D2P	AI	-	HDMIRX Port A TMDS data2 positive input	AVDD33_HDMIRX	NC
HDMIRX_ARCTXN	AO	-	Audio Return Channel output	AVDD18_HDMIRX_EARCTX	NC
HDMIRX_ARCTXP	AO	-	Audio Return Channel output	AVDD18_HDMIRX_EARCTX	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
HDMIRX_B_CLKN	AI	-	HDMIRX Port B TMDS clock negative input	AVDD33_HDMIRX	NC
HDMIRX_B_CLKP	AI	-	HDMIRX Port B TMDS clock positive input	AVDD33_HDMIRX	NC
HDMIRX_B_D0N	AI	-	HDMIRX Port B TMDS data0 negative input	AVDD33_HDMIRX	NC
HDMIRX_B_D0P	AI	-	HDMIRX Port B TMDS data0 positive input	AVDD33_HDMIRX	NC
HDMIRX_B_D1N	AI	-	HDMIRX Port B TMDS data1 negative input	AVDD33_HDMIRX	NC
HDMIRX_B_D1P	AI	-	HDMIRX Port B TMDS data1 positive input	AVDD33_HDMIRX	NC
HDMIRX_B_D2N	AI	-	HDMIRX Port B TMDS data2 negative input	AVDD33_HDMIRX	NC
HDMIRX_B_D2P	AI	-	HDMIRX Port B TMDS data2 positive input	AVDD33_HDMIRX	NC
HDMIRX_C_CLKN	AI	-	HDMIRX Port C TMDS clock negative input	AVDD33_HDMIRX	NC
HDMIRX_C_CLKP	AI	-	HDMIRX Port C TMDS clock positive input	AVDD33_HDMIRX	NC
HDMIRX_C_D0N	AI	-	HDMIRX Port C TMDS data0 negative input	AVDD33_HDMIRX	NC
HDMIRX_C_D0P	AI	-	HDMIRX Port C TMDS data0 positive input	AVDD33_HDMIRX	NC
HDMIRX_C_D1N	AI	-	HDMIRX Port C TMDS data1 negative input	AVDD33_HDMIRX	NC
HDMIRX_C_D1P	AI	-	HDMIRX Port C TMDS data1 positive input	AVDD33_HDMIRX	NC
HDMIRX_C_D2N	AI	-	HDMIRX Port C TMDS data2 negative input	AVDD33_HDMIRX	NC
HDMIRX_C_D2P	AI	-	HDMIRX Port C TMDS data2 positive input	AVDD33_HDMIRX	NC
AVDD18_HDMIRX_EARCTX	AP	-	Analog Power supply 1.8V for HDMIRX and eARCTX	-	To 1.8V
AVDD08_HDMIRX	AP	-	Analog Power supply 0.8V for HDMI RX	-	To 0.8V
AVDD33_HDMIRX	AP	-	Power supply for HDMI RX analog 3.3V	-	To 3.3V
HDMI TX					
HDMITX_ARCRXN	AO	-	Audio Return Channel iutput	AVDD18_HDMITX_EARCRX	NC
HDMITX_ARCRXP	AO	-	Audio Return Channel iutput	AVDD18_HDMITX_EARCRX	NC
HDMITX_CLKN	AO	-	HDMI TMDS clock positive output	3.3V	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
HDMITX_ CLKP	AO	-	HDMI TMDS clock negative output	3.3V	NC
HDMITX_ D0N	AO	-	HDMI TMDS data0 positive output	3.3V	NC
HDMITX_ D0P	AO	-	HDMI TMDS data0 negative output	3.3V	NC
HDMITX_ D1N	AO	-	HDMI TMDS data1 positive output	3.3V	NC
HDMITX_ D1P	AO	-	HDMI TMDS data1 negative output	3.3V	NC
HDMITX_ D2N	AO	-	HDMI TMDS data2 positive output	3.3V	NC
HDMITX_ D2P	AO	-	HDMI TMDS data2 negative output	3.3V	NC
HDMITX_ REXT	A	-	HDMI output strength setting resistor	AVDD18_ HDMITX_ EARCRX	NC
AVDD18_ HDMITX_ EARCRX	AP	-	Analog Power supply 1.8V for HDMITX and eARCRX	-	To 1.8V
AVDD08_ HDMITX	AP	-	Analog Power supply 0.8V for HDMI TX	-	To 0.8V
AVDD33_ HDMITX	AP	-	Pin for decap, Only decap is needed	-	NC
AVSS_HPLL	AP	-	Ground of HDMI PLL	-	To GND
PCIe and USB					
USB_A_ OTG_DM	AIO	-	USB 2.0 Port A OTG negative data signal	AVDD33_ USB	NC
USB_A_ OTG_DP	AIO	-	USB 2.0 Port A OTG positive data signal	AVDD33_ USB	NC
USB_A_ OTG_ID	AI	-	USB 2.0 Port A ID detect signal, internal pull up to 1.8V	AVDD18_ USB_PCIE	NC
USB_A_ OTG_VBUS	AI	-	USB 2.0 Port A host cable power detection (1.8V input tolerance)	AVDD18_ USB_PCIE	NC
USB_B_ OTG_DM	AIO	-	USB 2.0 Port B OTG negative data signal	AVDD33_ USB	NC
USB_B_ OTG_DP	AIO	-	USB 2.0 Port B OTG positive data signal	AVDD33_ USB	NC
USB_B_ OTG_ID	AI	-	USB 2.0 Port B ID detect signal, internal pull up to 1.8V	AVDD18_ USB_PCIE	NC
USB_B_ OTG_VBUS	AI	-	USB 2.0 Port B host cable power detection (1.8V input tolerance)	AVDD18_ USB_PCIE	NC
USB20_ TXRTUNE	AIO	-	USB 2.0 PortA and Port B host output strength setting resistor	AVDD33_ USB	NC
USB30_ PCIE_REXT	AO	-	PCIe and USB3.0 port output strength setting resistor	AVDD18_ USB_PCIE	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
USB30_ RXN	AI	-	USB3.0 port B input negative signal	AVDD18_ USB_PCIE	NC
USB30_ RXP	AI	-	USB3.0 port B input positive signal	AVDD18_ USB_PCIE	NC
USB30_TXN	AO	-	USB3.0 port B output negative signal	AVDD18_ USB_PCIE	NC
USB30_TXP	AO	-	USB3.0 port B output positive signal	AVDD18_ USB_PCIE	NC
PCIE_CLK_ N	AO	-	PCIe reference clock negative signal	AVDD18_ USB_PCIE	NC
PCIE_CLK_ P	AO	-	PCIe reference clock positive signal	AVDD18_ USB_PCIE	NC
PCIE_RXN	AI	-	PCIe input negative signal	AVDD18_ USB_PCIE	NC
PCIE_RXP	AI	-	PCIe input positive signal	AVDD18_ USB_PCIE	NC
PCIE_TXN	AO	-	PCIe output negative signal	AVDD18_ USB_PCIE	NC
PCIE_TXP	AO	-	PCIe output positive signal	AVDD18_ USB_PCIE	NC
HCSL_ REXT	AIO	-	PCIe reference clk output strength setting resistor	AVDD18_ USB_PCIE	NC
AVDD0V8_ USB_PCIE	AP	-	Analog 0.8V power supply for USB and PCIe	-	To VDD_ EE
AVDD18_ USB_PCIE	AP	-	Analog 1.8V power supply for USB and PCIe	-	To 1.8V
AVDD33_ USB	P	-	3.3V Power supply for USB	-	To 3.3V
POR					
POR_OUT	AO	Down	Power on reset output	AVDD33_ POR	NC
AVDD33_ POR	AP	-	Power supply for POR	-	NC
SARADC					
SARADC_ CH0	AI	-	ADC channel 0 input	AVDD18_ SARADC	NC
SARADC_ CH1	AI	-	ADC channel 1 input	AVDD18_ SARADC	NC
SARADC_ CH2	AI	-	ADC channel 2 input	AVDD18_ SARADC	NC
SARADC_ CH3	AI	-	ADC channel 3 input	AVDD18_ SARADC	NC
SARADC_ CH6	AI	-	ADC channel 6 input	AVDD18_ SARADC	NC
AVDD18_ SARADC	P	-	Analog power supply for SARADC	-	To 1.8V

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
System Clock & PLL					
SYS_OSCIN	AI	-	24MHz crystal oscillator input	VDD18_AO	To XTAL
SYS_ OSCOUT	AO	-	24MHz crystal oscillator output	VDD18_AO	To XTAL
AVDD18_ PLL	AP	-	Analog power of System PLL	-	To 1.8V
AVSS_PLL	AP	-	Ground of System PLL	-	To GND
MCLK					
CM_MCLK1	AO	-	MCLK 1 output for camera	AVDD18_ MCLK	NC
CM_MCLK2	AO	-	MCLK 2 output for camera	AVDD18_ MCLK	NC
AVDD18_ MCLK	AP	-	Power supply 1.8V for MCLK	-	To 1.8V
Digital Power					
VDD_DDR	P	-	Core Power supply for DDR PHY	-	To VDD_ EE
VDD_EE	P	-	Power supply for core logic	-	To VDD_ EE
VDD_GPU	P	-	Power supply for GPU	-	To VDD_ GPU
VDD_NPU	P	-	Power supply for NNA	-	To VDD_ NPU
VDD18_AO	P	-	1.8V Power supply for Always On Domain	-	To VD-D18_ AO
VDDCPU_A	P	-	Power supply for CPU (Cortex A73)	-	To VDDCP-U_A
VDDCPU_B	P	-	Power supply for CPU (Cortex A53)	-	To VDDCP-U_B
VDDQ	P	-	DDR IO Power supply for DDR PHY	-	To VDDQ
VDDQLP	P	-	DDR IO Power supply for DDR PHY	-	To VDDQ
DVSS	P	-	Digital power ground	-	To GND
Display interface					
VX1_A_0N	AO	-	V-by-one A data0 or LVDS A data0 or MIPI DSI A data0 or eDP A Aux negative output	AVDD18_ DP	NC
VX1_A_0P	AO	-	V-by-one A data0 or LVDS A data0 or MIPI DSI A data0 or eDP A Aux positive output	AVDD18_ DP	NC
VX1_A_1N	AO	-	V-by-one A data1 or LVDS A data1 or MIPI DSI A data1 or eDP A data0 negative output	AVDD18_ DP	NC
VX1_A_1P	AO	-	V-by-one A data1 or LVDS A data1 or MIPI DSI A data1 or eDP A data0 positive output	AVDD18_ DP	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
VX1_A_2N	AO	-	V-by-one A data2 or LVDS A data2 or MIPI DSI A clk or eDP A data1 negative output	AVDD18_DP	NC
VX1_A_2P	AO	-	V-by-one A data2 or LVDS A data2 or MIPI DSI A clk or eDP A data1 positive output	AVDD18_DP	NC
VX1_A_3N	AO	-	V-by-one A data3 or LVDS A clk or MIPI DSI A data2 or eDP A data2 negative output	AVDD18_DP	NC
VX1_A_3P	AO	-	V-by-one A data3 or LVDS A clk or MIPI DSI A data2 or eDP A data2 positive output	AVDD18_DP	NC
VX1_A_4N	AO	-	V-by-one A data4 or LVDS A data3 or MIPI DSI A data3 or eDP A data3 negative output	AVDD18_DP	NC
VX1_A_4P	AO	-	V-by-one A data4 or LVDS A data3 or MIPI DSI A data3 or eDP A data3 positive output	AVDD18_DP	NC
VX1_A_5N	AO	-	V-by-one A data5 or LVDS B data0 negative output	AVDD18_DP	NC
VX1_A_5P	AO	-	V-by-one A data5 or LVDS B data0 positive output	AVDD18_DP	NC
VX1_A_6N	AO	-	V-by-one A data6 or LVDS B data1 negative output	AVDD18_DP	NC
VX1_A_6P	AO	-	V-by-one A data6 or LVDS B data1 positive output	AVDD18_DP	NC
VX1_A_7N	AO	-	V-by-one A data7 or LVDS B data2 negative output	AVDD18_DP	NC
VX1_A_7P	AO	-	V-by-one A data7 or LVDS B data2 positive output	AVDD18_DP	NC
VX1_ATP	AO	-	V-by-one B or LVDS or MIPI DSI or eDP test output	AVDD18_DP	NC
VX1_B_0N	AO	-	V-by-one B data0 or LVDS B clk or MIPI DSI B data0 or eDP B Aux negative output	AVDD18_DP	NC
VX1_B_0P	AO	-	V-by-one B data0 or LVDS B clk or MIPI DSI B data0 or eDP B Aux positive output	AVDD18_DP	NC
VX1_B_1N	AO	-	V-by-one B data1 or LVDS B data3 or MIPI DSI B data1 or eDP B data0 negative output	AVDD18_DP	NC
VX1_B_1P	AO	-	V-by-one B data1 or LVDS B data3 or MIPI DSI B data1 or eDP B data0 positive output	AVDD18_DP	NC
VX1_B_2N	AO	-	V-by-one B data2 or LVDS C data0 or MIPI DSI B clk or eDP B data1 negative output	AVDD18_DP	NC
VX1_B_2P	AO	-	V-by-one B data2 or LVDS C data0 or MIPI DSI B clk or eDP B data1 positive output	AVDD18_DP	NC
VX1_B_3N	AO	-	V-by-one B data3 or LVDS C data1 or MIPI DSI B data2 or eDP B data2 negative output	AVDD18_DP	NC
VX1_B_3P	AO	-	V-by-one B data3 or LVDS C data1 or MIPI DSI B data2 or eDP B data2 positive output	AVDD18_DP	NC
VX1_B_4N	AO	-	V-by-one B data4 or LVDS C data2 or MIPI DSI B data3 or eDP B data3 negative output	AVDD18_DP	NC
VX1_B_4P	AO	-	V-by-one B data4 or LVDS C data2 or MIPI DSI B data3 or eDP B data3 positive output	AVDD18_DP	NC

Net Name	Type	Default Pull Up/Dn	Description	Power Domain	If Unused
VX1_B_5N	AO	-	V-by-one B data5 or LVDS C clk negative output	AVDD18_ DP	NC
VX1_B_5P	AO	-	V-by-one B data5 or LVDS C clk positive output	AVDD18_ DP	NC
VX1_B_6N	AO	-	V-by-one B data6 or LVDS C data3 negative output	AVDD18_ DP	NC
VX1_B_6P	AO	-	V-by-one B data6 or LVDS C data3 positive output	AVDD18_ DP	NC
VX1_B_7N	AO	-	V-by-one B data7 negative output	AVDD18_ DP	NC
VX1_B_7P	AO	-	V-by-one B data7 positive output	AVDD18_ DP	NC
VX1_LPN	AO	-	V-by-one B or LVDS or MIPI DSI or eDP test output	AVDD18_ DP	NC
VX1_LPP	AO	-	V-by-one B or LVDS or MIPI DSI or eDP test output	AVDD18_ DP	NC
DIF_REXT	AO	-	eDP, MIPI DSI, LVDS and V-by-one reference resistor	AVDD18_ DP	NC
AVDD08_ DP	AP	-	Analog Power supply 0.8V for Display interface	-	To 0.8V
AVDD18_ DP	AP	-	Analog Power supply 1.8V for display interface	-	To 1.8V
AVDD18_ DDR_DP_ PLL	AP	-	Analog Power supply 0.8V for DDR and display interface PLL	-	To 0.8V
AVSS_DP	AP	-	Analog ground for diaplay interface	-	To VSS

Abbreviations:

- DI = Digital input pin
- DO = Digital output pin
- DIO = Digital input/output pin
- OD5V = 5V input tolerant open drain (OD) output pin, need external pull Up
- A = Analog setting or filtering pin
- AI = Analog input pin
- AO = Analog output pin
- AIO = Analog input/output pin
- P = Power pin
- AP = Analog power pin
- NC = No connection
- Up = Pull-Up
- Down = Pull-down
- COMB PIN = Combined Pin
- Z = High-Z

4.4 Pin Multiplexing Tables

Multiple usage pins are used to conserve pin consumption for different features. The device can be used in many different applications but each application will not utilize all the onchip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin as well.

Table 4-2 GPIOW_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOW_0	HDMIRX_A_HPD		
GPIOW_1	HDMIRX_A_5VDET		
GPIOW_2	HDMIRX_A_SDA	UART_AO_A_TX	HDMITX_SDA
GPIOW_3	HDMIRX_A_SCL	UART_AO_A_RX	HDMITX_SCL
GPIOW_4	HDMIRX_C_HPD		
GPIOW_5	HDMIRX_C_5VDET		
GPIOW_6	HDMIRX_C_SDA	UART_AO_A_TX	
GPIOW_7	HDMIRX_C_SCL	UART_AO_A_RX	
GPIOW_8	HDMIRX_B_HPD		
GPIOW_9	HDMIRX_B_5VDET		
GPIOW_10	HDMIRX_B_SDA	UART_AO_A_TX	
GPIOW_11	HDMIRX_B_SCL	UART_AO_A_RX	
GPIOW_12	CEC_A		
GPIOW_13	HDMITX_SDA		
GPIOW_14	HDMITX_SCL		
GPIOW_15	HDMITX_HPD_IN		
GPIOW_16	CEC_B		

Table 4-3 GPIOD_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOD_0	UART_AO_A_TX			
GPIOD_1	UART_AO_A_RX			
GPIOD_2	I2CM_AO_A_SCL	I2CS_AO_SCL	UART_AO_B_TX	
GPIOD_3	I2CM_AO_A_SDA	I2CS_AO_SDA	UART_AO_B_RX	
GPIOD_4	IR_OUT	RTC_CLK_IN	UART_AO_B_CTS	
GPIOD_5	IR_IN	PWM_AO_H		
GPIOD_6	JTAG_A_CLK	PWM_AO_C	PWM_AO_C_HIZ	IR_OUT
GPIOD_7	JTAG_A_TMS	PWM_AO_G	PWM_AO_G_HIZ	
GPIOD_8	JTAG_A_TDI	SPDIF_OUT		
GPIOD_9	JTAG_A_TDO	SPDIF_IN		

Pin Name	Func1	Func2	Func3	Func4
GPIOD_10	GEN_CLK_OUT	PWM_AO_H	UART_AO_B_RTS	
GPIOD_11	PWM_AO_G			
GPIOD_12	WD_RSTO			

Table 4-4 GPIOE_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOE_0	PWM_AO_A	I2CM_AO_A_SCL	
GPIOE_1	PWM_AO_B	I2CM_AO_A_SDA	
GPIOE_2	PWM_AO_C	CLK25M	
GPIOE_3	PWM_AO_D	I2CM_AO_B_SCL	
GPIOE_4	PWM_AO_E	I2CM_AO_B_SDA	CLK12M_24M
GPIOE_5	PWM_AO_F	RTC_CLK_OUT	
GPIOE_6	PWM_AO_G		

Table 4-5 GPIOB_x Multi-Function Pin

Pin Name	Func1	Func2
GPIOB_0	EMMC_D0	
GPIOB_1	EMMC_D1	
GPIOB_2	EMMC_D2	
GPIOB_3	EMMC_D3	SPIF_HOLD
GPIOB_4	EMMC_D4	SPIF_MO
GPIOB_5	EMMC_D5	SPIF_MI
GPIOB_6	EMMC_D6	SPIF_CLK
GPIOB_7	EMMC_D7	SPIF_WP
GPIOB_8	EMMC_CLK	
GPIOB_9		
GPIOB_10	EMMC_CMD	
GPIOB_11	EMMC_DS	
GPIOB_12		SPIF_CS

Table 4-6 GPIOC_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOC_0	SDCARD_D0	JTAG_B_TDO	SPI_B_MOSI
GPIOC_1	SDCARD_D1	JTAG_B_TDI	SPI_B_MISO
GPIOC_2	SDCARD_D2	UART_AO_A_RX	SPI_B_SCLK

Pin Name	Func1	Func2	Func3
GPIOC_3	SDCARD_D3	UART_AO_A_TX	SPI_B_SS0
GPIOC_4	SDCARD_CLK	JTAG_B_CLK	
GPIOC_5	SDCARD_CMD	JTAG_B_TMS	
GPIOC_6	GEN_CLK_OUT		

Table 4-7 GPIOZ_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOZ_0	ETH_MDIO	ISO7816_CLK		SPI_E_MOSI
GPIOZ_1	ETH_MDC	ISO7816_DATA		SPI_E_MISO
GPIOZ_2	ETH_RGMII_RX_CLK	TSIN_B_VALID		SPI_E_SCLK
GPIOZ_3	ETH_RX_DV	TSIN_B_SOP		SPI_E_SS0
GPIOZ_4	ETH_RXD0	TSIN_B_DIN0		SPI_F_MOSI
GPIOZ_5	ETH_RXD1	TSIN_B_CLK		SPI_F_MISO
GPIOZ_6	ETH_RXD2_RGMII	TSIN_B_FAIL	TSIN_C_VALID	SPI_F_SCLK
GPIOZ_7	ETH_RXD3_RGMII	TSIN_B_DIN1	TSIN_C_SOP	SPI_F_SS0
GPIOZ_8	ETH_RGMII_TX_CLK	TSIN_B_DIN2	TSIN_C_DIN0	
GPIOZ_9	ETH_TXEN	TSIN_B_DIN3	TSIN_C_CLK	
GPIOZ_10	ETH_TXD0	TSIN_B_DIN4	TSIN_D_VALID	
GPIOZ_11	ETH_TXD1	TSIN_B_DIN5	TSIN_D_SOP	
GPIOZ_12	ETH_TXD2_RGMII	TSIN_B_DIN6	TSIN_D_DIN0	
GPIOZ_13	ETH_TXD3_RGMII	TSIN_B_DIN7	TSIN_D_CLK	

Table 4-8 GPIOH_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOH_0	MIC_MUTE_KEY		
GPIOH_1	Mic_Mute_LED	PWM_VS	
GPIOH_2	I2CM_D_SCL	UART_F_TX	PCIECK_REQN
GPIOH_3	I2CM_D_SDA	UART_F_RX	
GPIOH_4	I2CM_E_SCL	UART_F_CTS	
GPIOH_5	I2CM_E_SDA	UART_F_RTS	
GPIOH_6	ETH_LINK_LED	I2CM_A_SDA	
GPIOH_7	ETH_ACT_LED	I2CM_A_SCL	

Table 4-9 GPIOM_x Multi-Function Pin

Pin Name	Func1	Func2
GPIOM_0	TDM_D12	PDM_DIN1
GPIOM_1	TDM_D13	PDM_DIN2
GPIOM_2	TDM_D14	PDM_DIN3
GPIOM_3	TDM_D15	PDM_DCLK
GPIOM_4	TDM_SCLK3	PDM_DIN0
GPIOM_5	TDM_FS3	PDM_DIN1
GPIOM_6	I2CM_D_SCL	
GPIOM_7	I2CM_D_SDA	
GPIOM_8	SPI_B_MOSI	UART_D_TX
GPIOM_9	SPI_B_MISO	UART_D_RX
GPIOM_10	SPI_B_SCLK	UART_D_CTS
GPIOM_11	SPI_B_SS0	UART_D_RTS
GPIOM_12	SPI_B_SS1	I2CM_C_SCL
GPIOM_13	SPI_B_SS2	I2CM_C_SDA

Table 4-10 GPIOX_x Multi-Function Pin

Pin Name	Func1	Func2
GPIOX_0	SDIO_D0	
GPIOX_1	SDIO_D1	
GPIOX_2	SDIO_D2	
GPIOX_3	SDIO_D3	
GPIOX_4	SDIO_CLK	
GPIOX_5	SDIO_CMD	
GPIOX_6	PWM_B	
GPIOX_7	PWM_C	
GPIOX_8	TDM_D0	
GPIOX_9	TDM_D1	
GPIOX_10	TDM_FS0	
GPIOX_11	TDM_SCLK0	
GPIOX_12	UART_C_TX	
GPIOX_13	UART_C_RX	
GPIOX_14	UART_C_CTS	CLK12M_24M
GPIOX_15	UART_C_RTS	
GPIOX_16	PWM_A	

Pin Name	Func1	Func2
GPIOX_17	I2CM_C_SDA	
GPIOX_18	I2CM_C_SCL	
GPIOX_19	PWM_D	

Table 4-11 GPIOT_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOT_0	MCLK_1		
GPIOT_1	TDM_SCLK1		
GPIOT_2	TDM_FS1		
GPIOT_3	TDM_D2	SPDIF_IN	
GPIOT_4	TDM_D3	SPDIF_OUT	
GPIOT_5	TDM_D4	ISO7816_CLK	
GPIOT_6	TDM_D5	ISO7816_DATA	SPI_D_MOSI
GPIOT_7	TDM_D6	TSIN_A_SOP	SPI_D_MISO
GPIOT_8	TDM_D7	TSIN_A_DIN0	SPI_D_SCLK
GPIOT_9	TDM_D8	TSIN_A_CLK	SPI_D_SS0
GPIOT_10	TDM_D9	TSIN_A_VALID	
GPIOT_11	TDM_D10		
GPIOT_12	TDM_D11		
GPIOT_13	MCLK_2		
GPIOT_14	TDM_SCLK2		
GPIOT_15	TDM_FS2		
GPIOT_16	I2CM_B_SCL		
GPIOT_17	I2CM_B_SDA		
GPIOT_18	SPI_A_MOSI		
GPIOT_19	SPI_A_MISO		
GPIOT_20	SPI_A_SCLK	I2CM_A_SCL	
GPIOT_21	SPI_A_SS0	I2CM_A_SDA	
GPIOT_22	SPI_A_SS1	I2CM_C_SCL	
GPIOT_23	SPI_A_SS2	I2CM_C_SDA	

Table 4-12 GPIOY_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOY_0	SPI_C_MOSI			
GPIOY_1	SPI_C_MISO		PWM_E	

Pin Name	Func1	Func2	Func3	Func4
GPIOY_2	SPI_C_SCLK			
GPIOY_3	SPI_C_SS0			
GPIOY_4	SPI_C_SS1	TSIN_C_SOP	HSYNC	
GPIOY_5	SPI_C_SS2	TSIN_C_DIN0	VSYNC	
GPIOY_6	UART_E_TX	TSIN_C_CLK		
GPIOY_7	UART_E_RX	TSIN_C_VALID		
GPIOY_8	UART_E_CTS	TSIN_D_SOP	PWM_F	
GPIOY_9	UART_E_RTS	TSIN_D_DIN0	3D_SYNC_OUT	
GPIOY_10	UART_D_CTS	TSIN_D_CLK	VX1_A_HTPDN	eDP_A_HPD
GPIOY_11	UART_D_RTS	TSIN_D_VALID	VX1_B_HTPDN	eDP_B_HPD
GPIOY_12	UART_D_TX		VX1_A_LOCKN	
GPIOY_13	UART_D_RX		VX1_B_LOCKN	
GPIOY_14			PWM_VS	
GPIOY_15	I2CM_E_SCL			
GPIOY_16	I2CM_E_SDA			
GPIOY_17	I2CM_F_SCL			
GPIOY_18	I2CM_F_SDA	PCIECK_REQN		

Table 4-13 CSI Multi-Function Pin

Pin Name	Mux
CSI_B_D0N	CSI_A_D2N
CSI_B_D0P	CSI_A_D2P
CSI_B_D1N	CSI_A_D3N
CSI_B_D1P	CSI_A_D3P
CSI_D_D0N	CSI_C_D2N
CSI_D_D0P	CSI_C_D2P
CSI_D_D1N	CSI_C_D3N
CSI_D_D1P	CSI_C_D3P

Table 4-14 VX1 Multi-Function Pin

Pin Name	LVDS	EDP	DSI
VX1_A_0N	LVDS_A_0N	EDP_A_AUXN	DSI_A_D0N
VX1_A_0P	LVDS_A_0P	EDP_A_AUXP	DSI_A_D0P
VX1_A_1N	LVDS_A_1N	EDP_A_0N	DSI_A_D1N
VX1_A_1P	LVDS_A_1P	EDP_A_0P	DSI_A_D1P

Pin Name	LVDS	EDP	DSI
VX1_A_2N	LVDS_A_2N	EDP_A_1N	DSI_A_CKN
VX1_A_2P	LVDS_A_2P	EDP_A_1P	DSI_A_CKP
VX1_A_3N	LVDS_A_CLKN	EDP_A_2N	DSI_A_D2N
VX1_A_3P	LVDS_A_CLKP	EDP_A_2P	DSI_A_D2P
VX1_A_4N	LVDS_A_3N	EDP_A_3N	DSI_A_D3N
VX1_A_4P	LVDS_A_3P	EDP_A_3P	DSI_A_D3P
VX1_A_5N	LVDS_B_0N		
VX1_A_5P	LVDS_B_0P		
VX1_A_6N	LVDS_B_1N		
VX1_A_6P	LVDS_B_1P		
VX1_A_7N	LVDS_B_2N		
VX1_A_7P	LVDS_B_2P		
VX1_B_0N	LVDS_B_CLKN	EDP_B_AUXN	DSI_B_D0N
VX1_B_0P	LVDS_B_CLKP	EDP_B_AUXP	DSI_B_D0P
VX1_B_1N	LVDS_B_3N	EDP_B_0N	DSI_B_D1N
VX1_B_1P	LVDS_B_3P	EDP_B_0P	DSI_B_D1P
VX1_B_2N	LVDS_C_0N	EDP_B_1N	DSI_B_CKN
VX1_B_2P	LVDS_C_0P	EDP_B_1P	DSI_B_CKP
VX1_B_3N	LVDS_C_1N	EDP_B_2N	DSI_B_D2N
VX1_B_3P	LVDS_C_1P	EDP_B_2P	DSI_B_D2P
VX1_B_4N	LVDS_C_2N	EDP_B_3N	DSI_B_D3N
VX1_B_4P	LVDS_C_2P	EDP_B_3P	DSI_B_D3P
VX1_B_5N	LVDS_C_CLKN		
VX1_B_5P	LVDS_C_CLKP		
VX1_B_6N	LVDS_C_3N		
VX1_B_6P	LVDS_C_3P		
VX1_B_7N			
VX1_B_7P			

Table 4-15 DDR Multi-Function Pin

Pin Name	LPDDR4/LPDDR4X	DDR4
DDR0_AC_0	CKEA0	CKE0
DDR0_AC_1	CKEA1	CKE1
DDR0_AC_2	CSA0	CS_N0
DDR0_AC_3	CSA1	NC

Pin Name	LPDDR4/LPDDR4X	DDR4
DDR0_AC_4	CLKA_T	BG0
DDR0_AC_5	CLKA_C	A10
DDR0_AC_6	NC	A8
DDR0_AC_7	NC	A11
DDR0_AC_8	CAA2	WE_N
DDR0_AC_9	CAA3	BG1
DDR0_AC_10	CAA1	A12
DDR0_AC_11	CAA0	RAS_N
DDR0_AC_12	CAA5	A3
DDR0_AC_13	CAA4	CAS_N
DDR0_AC_14	NC	A7
DDR0_AC_15	NC	A13
DDR0_AC_20	CKEB0	CLK1_T
DDR0_AC_21	CKEB1	CLK1_C
DDR0_AC_22	CSB1	NC
DDR0_AC_23	CSB0	NC
DDR0_AC_24	CLKB_T	BA1
DDR0_AC_25	CLKB_C	A4
DDR0_AC_26	NC	BA0
DDR0_AC_28	CAB1	ACT_N
DDR0_AC_29	CAB3	A0
DDR0_AC_30	CAB5	A9
DDR0_AC_31	CAB2	A1
DDR0_AC_32	CAB4	NC
DDR0_AC_33	CAB0	A6
DDR0_AC_34	NC	A2
DDR0_AC_35	NC	A5
DDR0_AC_36	NC	ODT0
DDR0_AC_37	NC	ODT1
DDR0_AC_38	NC	CS_N1
DDR1_AC_0	CKEA0	CKE0
DDR1_AC_1	CKEA1	CKE1
DDR1_AC_2	CSA0	CS_N0
DDR1_AC_3	CSA1	NC
DDR1_AC_4	CLKA_T	BG0

Pin Name	LPDDR4/LPDDR4X	DDR4
DDR1_AC_5	CLKA_C	A10
DDR1_AC_6	NC	A8
DDR1_AC_7	NC	A11
DDR1_AC_8	CAA2	WE_N
DDR1_AC_9	CAA3	BG1
DDR1_AC_10	CAA1	A12
DDR1_AC_11	CAA0	RAS_N
DDR1_AC_12	CAA5	A3
DDR1_AC_13	CAA4	CAS_N
DDR1_AC_14	NC	A7
DDR1_AC_15	NC	A13
DDR1_AC_20	CKEB0	CLK1_T
DDR1_AC_21	CKEB1	CLK1_C
DDR1_AC_22	CSB1	NC
DDR1_AC_23	CSB0	NC
DDR1_AC_24	CLKB_T	BA1
DDR1_AC_25	CLKB_C	A4
DDR1_AC_26	NC	BA0
DDR1_AC_28	CAB1	ACT_N
DDR1_AC_29	CAB3	A0
DDR1_AC_30	CAB5	A9
DDR1_AC_31	CAB2	A1
DDR1_AC_32	CAB4	NC
DDR1_AC_33	CAB0	A6
DDR1_AC_34	NC	A2
DDR1_AC_35	NC	A5
DDR1_AC_36	NC	ODT0
DDR1_AC_37	NC	ODT1
DDR1_AC_38	NC	CS_N1

4.5 Signal Description

Table 4-16 SD Card Interface Signal Description

Signal Name	Type	Description
SDCARD_D0	DIO	SD Card data bus bit 0 signal
SDCARD_D1	DIO	SD Card data bus bit 1 signal
SDCARD_D2	DIO	SD Card data bus bit 2 signal
SDCARD_D3	DIO	SD Card data bus bit 3 signal
SDCARD_CLK	DO	SD Card clock signal
SDCARD_CMD	DIO	SD Card command signal

Table 4-17 SDIO Interface Signal Description

Signal Name	Type	Description
SDIO_D0	DIO	SDIO data bus bit 0 signal
SDIO_D1	DIO	SDIO data bus bit 1 signal
SDIO_D2	DIO	SDIO data bus bit 2 signal
SDIO_D3	DIO	SDIO data bus bit 3 signal
SDIO_CLK	DO	SDIO clock signal
SDIO_CMD	DIO	SDIO command signal

Table 4-18 Clock Interface Signal Description

Signal Name	Type	Description
CLK12M_24M	DO	12MHz/24MHZ clock output
CLK25M	DO	25MHz clock output

Table 4-19 UART Interface Signal Description

Signal Name	Type	Description
UART_D_TX	DO	UART Port D data output
UART_D_RX	DI	UART Port D data input
UART_D_CTS	DI	UART Port D Clear To Send Signal
UART_D_RTS	DO	UART Port D Ready To Send Signal
UART_E_TX	DO	UART Port E data output
UART_E_RX	DIO	UART Port E data input
UART_E_CTS	DIO	UART Port E Clear To Send Signal
UART_E_RTS	DIO	UART Port E Ready To Send Signal
UART_A_TX	DIO	UART Port A data output
UART_A_RX	DIO	UART Port A data input
UART_A_CTS	DIO	UART Port A Clear To Send Signal
UART_A_RTS	DIO	UART Port A Ready To Send Signal
UART_AO_A_TX	DIO	UART Port A data output in AO domain

Signal Name	Type	Description
UART_AO_A_RX	DIO	UART Port A data input in AO domain
UART_AO_B_TX	DIO	UART Port B data output in AO domain
UART_AO_B_RX	DIO	UART Port B data input in AO domain
UART_AO_B_CTS	DIO	UART Port B Clear To Send Signal in AO domain
UART_AO_B_RTS	DIO	UART Port B Ready To Send Signal in AO domain
UART_C_TX	DIO	UART Port C data output
UART_C_RX	DIO	UART Port C data input
UART_C_CTS	DIO	UART Port C Clear To Send Signal
UART_C_RTS	DIO	UART Port C Ready To Send Signal
UART_F_TX	DIO	UART Port F data output
UART_F_RX	DIO	UART Port F data input
UART_F_CTS	DIO	UART Port F Clear To Send Signal
UART_F_RTS	DIO	UART Port F Ready To Send Signal

Table 4-20 ISO7816 Interface Signal Description

Signal Name	Type	Description
ISO7816_DATA	DIO	ISO7816 data signal
ISO7816_CLK	DO	ISO7816 clock signal

Table 4-21 TS In Interface Signal Description

Signal Name	Type	Description
TSIN_A_DIN0	DI	Serial TS input port A data
TSIN_A_CLK	DI	TS input port A clock
TSIN_A_SOP	DI	TS input port A start of stream signal
TSIN_A_VALID	DI	TS input port A date valid signal
TSIN_B_DIN0	DI	Serial/Parallel TS input port B data 0
TSIN_B_DIN1	DI	Parallel TS input port B data 1
TSIN_B_DIN2	DI	Parallel TS input port B data 2
TSIN_B_DIN3	DI	Parallel TS input port B data 3
TSIN_B_DIN4	DI	Parallel TS input port B data 4
TSIN_B_DIN5	DI	Parallel TS input port B data 5
TSIN_B_DIN6	DI	Parallel TS input port B data 6
TSIN_B_DIN7	DI	Parallel TS input port B data 7
TSIN_B_FAIL	DI	TS input port B fail signal
TSIN_B_CLK	DI	TS input port B clock
TSIN_B_SOP	DI	TS input port B start of stream signal

Signal Name	Type	Description
TSIN_B_VALID	DI	TS input port B date valid signal
TSIN_C_DIN0	DI	Serial TS input port C data
TSIN_C_CLK	DI	TS input port C clock
TSIN_C_SOP	DI	TS input port C start of stream signal
TSIN_C_VALID	DI	TS input port C date valid signal
TSIN_D_DIN0	DI	Serial TS input port D data
TSIN_D_CLK	DI	TS input port D clock
TSIN_D_SOP	DI	TS input port D start of stream signal
TSIN_D_VALID	DI	TS input port D date valid signal

Table 4-22 PWM Interface Signal Description

Signal Name	Type	Description
PWM_A	DO	PWM channel A output signal
PWM_B	DO	PWM channel B output signal
PWM_C	DO	PWM channel C output signal
PWM_D	DO	PWM channel D output signal
PWM_E	DO	PWM channel E output signal
PWM_F	DO	PWM channel F output signal
PWM_AO_A	DO	PWM A output signal in Always On domain
PWM_AO_B	DO	PWM B output signal in Always On domain
PWM_AO_C / PWMAO_C_HIZ	DO	PWM C output signal in Always On domain, or extended HiZ function of PWM_AO_C
PWM_AO_D	DO	PWM D output signal in Always On domain
PWM_AO_E	DO	PWM E output signal in Always On domain
PWM_AO_F	DO	PWM F output signal in Always On domain
PWM_AO_G / PWM_AO_G_HIZ	DO	PWM G output signal in Always On domain, or extended HiZ function of PWM_AO_G
PWM_AO_H	DO	PWM H output signal in Always On domain
PWM_VS	DO	

Table 4-23 I2C Interface Signal Description

Signal Name	Type	Description
I2CM_E_ SCL	DO	I2C bus group E clock output, master mode
I2CM_E_SDA	DIO	I2C bus group E data input/output, master mode
I2CM_A_SCL	DO	I2C bus group E clock output, master mode
I2CM_A_SDA	DIO	I2C bus group E data input/output, master mode
I2CM_B_SCL	DO	I2C bus group E clock output, master mode

Signal Name	Type	Description
I2CM_B_SDA	DIO	I2C bus group E data input/output, master mode
I2CM_C_SCL	DO	I2C bus group E clock output, master mode
I2CM_C_SDA	DIO	I2C bus group E data input/output, master mode
I2CM_D_SCL	DO	I2C bus group E clock output, master mode
I2CM_D_SDA	DIO	I2C bus group E data input/output, master mode
I2CM_AO_A_SCL	DIO	I2C bus group AO data input/output, master mode
I2CM_AO_A_SDA	DIO	I2C bus group AO data input/output, master mode
I2CM_AO_B_SCL	DIO	I2C bus group AO data input/output, master mode
I2CM_AO_B_SDA	DIO	I2C bus group AO data input/output, master mode
I2CS_AO_SCL	DI	I2C bus group AO data input, slave mode
I2CS_AO_SDA	DIO	I2C bus group AO data input, output slave mode

Table 4-24 eMMC Interface Signal Description

Signal Name	Type	Description
EMMC_D0	DIO	eMMC/NAND data bus bit 0 signal
EMMC_D1	DIO	eMMC/NAND data bus bit 1 signal
EMMC_D2	DIO	eMMC/NAND data bus bit 2 signal
EMMC_D3	DIO	eMMC/NAND data bus bit 3 signal
EMMC_D4	DIO	eMMC/NAND data bus bit 4 signal
EMMC_D5	DIO	eMMC/NAND data bus bit 5 signal
EMMC_D6	DIO	eMMC/NAND data bus bit 6 signal
EMMC_D7	DIO	eMMC/NAND data bus bit 7 signal
EMMC_CLK	DO	eMMC clock signal
EMMC_CMD	DIO	eMMC command signal
EMMC_DS	DI	eMMC data strobe

Table 4-25 HDMI Interface Signal Description

Signal Name	Type	Description
HDMIRX_A_HPD	OD_5V	HDMI RX port A hot plug in signal output
HDMIRX_A_5VDET	OD_5V	HDMI RX port A 5V power detection
HDMIRX_A_SDA	OD_5V	HDMI RX port A DDC_I2C interface data signal
HDMIRX_A_SCL	OD_5V	HDMI RX port A DDC_I2C interface clock signal
HDMIRX_B_HPD	OD_5V	HDMI RX port B hot plug in signal output
HDMIRX_B_5VDET	OD_5V	HDMI RX port B 5V power detection
HDMIRX_B_SDA	OD_5V	HDMI RX port B DDC_I2C interface data signal
HDMIRX_B_SCL	OD_5V	HDMI RX port B DDC_I2C interface clock signal

Signal Name	Type	Description
HDMIRX_C_HPD	OD_5V	HDMI RX port C hot plug in signal output
HDMIRX_C_5VDET	OD_5V	HDMI RX port C 5V power detection
HDMIRX_C_SDA	OD_5V	HDMI RX port C DDC_I2C interface data signal
HDMIRX_C_SCL	OD_5V	HDMI RX port C DDC_I2C interface clock signal
HDMITX_SDA	OD_5V	HDMI TX DDC_I2C interface data signal
HDMITX_SCL	OD_5V	HDMI TX DDC_I2C interface clock signal
HDMITX_HPD_IN	OD_5V	HDMI TX hot-plug in signal input
CEC_A	OD_5V	Customer Electronics Control signal
CEC_B	OD_5V	2nd pin of Customer Electronics Control signal

Table 4-26 SPIF Interface Signal Description

Signal Name	Type	Description
SPIF_CS	DO	SPIF chip select
SPIF_CLK	DO	SPIF Serial Clock
SPIF_MO	DIO	SPIF 1bit mode Output, 2/4 bit mode data I/O 0
SPIF_MI	DIO	SPIF 1bit mode Input, 2/4 bit mode data I/O 1
SPIF_WP	DIO	SPIF Write protection output, 4 bit mode data I/O 2
SPIF_HOLD	DIO	SPIF bus hold output, 4 bit mode data I/O 3

Table 4-27 SPDIF Interface Signal Description

Signal Name	Type	Description
SPDIF_IN	DI	SPDIF input signal
SPDIF_OUT	DO	SPDIF output signal

Table 4-28 PCIE Interface Signal Description

Signal Name	Type	Description
PCIECK_REQN	DI	PCIE clock request input

Table 4-29 SPI Interface Signal Description

Signal Name	Type	Description
SPI_A_MOSI	DIO	SPI master output, slave input A
SPI_A_MISO	DIO	SPI master input, slave output A
SPI_A_SCLK	DIO	SPI clock A
SPI_A_SS0	DIO	SPI slave select 0 A
SPI_A_SS1	DIO	SPI slave select 1 A
SPI_A_SS2	DIO	SPI slave select 2 A
SPI_B_MOSI	DIO	SPI master output, slave input B

Signal Name	Type	Description
SPI_B_MISO	DIO	SPI master input, slave output B
SPI_B_SCLK	DIO	SPI clock B
SPI_B_SS0	DIO	SPI slave select 0 B
SPI_B_SS1	DIO	SPI slave select 1 B
SPI_B_SS2	DIO	SPI slave select 2 B
SPI_C_MOSI	DIO	SPI master output, slave input C
SPI_C_MISO	DIO	SPI master input, slave output C
SPI_C_SCLK	DIO	SPI clock C
SPI_C_SS0	DIO	SPI slave select 0 C
SPI_C_SS1	DIO	SPI slave select 1 C
SPI_C_SS2	DIO	SPI slave select 2 C
SPI_D_MOSI	DIO	SPI master output, slave input D
SPI_D_MISO	DIO	SPI master input, slave output D
SPI_D_SCLK	DIO	SPI clock D
SPI_D_SS0	DIO	SPI slave select 0 D
SPI_E_MOSI	DIO	SPI master output, slave input E
SPI_E_MISO	DIO	SPI master input, slave output E
SPI_E_SCLK	DIO	SPI clock E
SPI_E_SS0	DIO	SPI slave select 0 E
SPI_F_MOSI	DIO	SPI master output, slave input F
SPI_F_MISO	DIO	SPI master input, slave output F
SPI_F_SCLK	DIO	SPI clock F
SPI_F_SS0	DIO	SPI slave select 0 F

Table 4-30 Remote Interface Signal Description

Signal Name	Type	Description
IR_IN	DI	IR remote control input
IR_OUT	DO	IR remote control output

Table 4-31 Time Division Multiplexing Signal Description

Signal Name	Type	Description
MCLK_1	DO	Master clock output 1, for I2S master mode
MCLK_2	DO	Master clock output 2, for I2S master mode
TDM_D0	DIO	Data input/output 0 of TDM
TDM_D1	DIO	Data input/output 1 of TDM
TDM_D2	DIO	Data input/output 2 of TDM

Signal Name	Type	Description
TDM_D3	DIO	Data input/output 3 of TDM
TDM_D4	DIO	Data input/output 4 of TDM
TDM_D5	DIO	Data input/output 5 of TDM
TDM_D6	DIO	Data input/output 6 of TDM
TDM_D7	DIO	Data input/output 7 of TDM
TDM_D8	DIO	Data input/output 8 of TDM
TDM_D9	DIO	Data input/output 9 of TDM
TDM_D10	DIO	Data input/output 10 of TDM
TDM_D11	DIO	Data input/output 11 of TDM
TDM_D12	DIO	Data input/output 12 of TDM
TDM_D13	DIO	Data input/output 13 of TDM
TDM_D14	DIO	Data input/output 14 of TDM
TDM_D15	DIO	Data input/output 15 of TDM
TDM_SCLK0	DIO	Bit clock output of TDM
TDM_FS0	DIO	Frame sync output of TDM (Word clock of I2S)
TDM_SCLK1	DIO	Bit clock output of TDM
TDM_FS1	DIO	Frame sync output of TDM (Word clock of I2S)
TDM_SCLK2	DIO	Bit clock output of TDM
TDM_FS2	DIO	Frame sync output of TDM (Word clock of I2S)
TDM_SCLK3	DIO	Bit clock output of TDM
TDM_FS3	DIO	Frame sync output of TDM (Word clock of I2S)

Table 4-32 PDM Signal Description

Signal Name	Type	Description
PDM_DIN0	DI	PDM input data 0 signal
PDM_DIN1	DI	PDM input data 1 signal
PDM_DIN2	DI	PDM input data 2 signal
PDM_DIN3	DI	PDM input data 3 signal
PDM_DCLK	DO	PDM output clock signal

Table 4-33 JTAG Interface Signal Description

Signal Name	Type	Description
JTAG_A_TDO	DO	JTAG data output channel A
JTAG_A _TDI	DI	JTAG data input channel A
JTAG_A_TMS	DI	JTAG Test mode select input channel A
JTAG_A_CLK	DO	JTAG Test clock input channel A

Signal Name	Type	Description
JTAG_B_TDO	DO	JTAG data output channel B
JTAG_B _TDI	DI	JTAG data input channel B
JTAG_B_TMS	DI	JTAG Test mode select input channel B
JTAG_B _CLK	DO	JTAG Test clock input channel B

Table 4-34 Ethernet Interface Signal Description

Signal Name	Type	Description
ETH_LINK_LED	DO	Ethernet link LED indicator
ETH_ACT_LED	DO	Ethernet active LED indicator
ETH_RGMII_RX_CLK	DI	Ethernet RGMII interface receive clock input
ETH_RGMII_TX_CLK	DIO	Ethernet RGMII transmit clock
ETH_TXEN	DIO	Ethernet RMII/RGMII Interface transmit enable
ETH_TXD3_RGMII	DIO	Ethernet RGMII interface transmit data 3
ETH_TXD2_RGMII	DIO	Ethernet RGMII interface transmit data 2
ETH_TXD1	DIO	Ethernet RMII/RGMII interface transmit data 1
ETH_TXD0	DIO	Ethernet RMII/RGMII interface transmit data 0
ETH_RX_DV	DI	Ethernet RMII/RGMII interface receive data valid signal
ETH_RXD3_RGMII	DI	Ethernet RGMII interface receive data 3
ETH_RXD2_RGMII	DI	Ethernet RGMII interface receive data 2
ETH_RXD1	DI	Ethernet RMII/RGMII interface receive data 1
ETH_RXD0	DI	Ethernet RMII/RGMII interface receive data 0
ETH_MDIO	DIO	Ethernet SMI interface management data input/output
ETH_MDC	DO	Ethernet SMI interface management clock

Note

IO interfaces supporting 200Mbps data rate or 100M clock and above must be powered by 1.8V instead of 3.3V. For example, eMMC (HS200/400 mode) or RGMII interface must be powered by 1.8V.

Table 4-35 Other Signal Description

Signal Name	Type	Description
RTC_CLK_OUT	DO	RTC32.768 KHz clock output
WD_RSTO	DO	WD_RSTO Watchdog output
MIC_MUTE_KEY	DI	MIC MUTE KEY detect signal
MIC_MUTE_LED	DIO	MIC MUTE state output signal
HSYNC	DIO	Horizontal synchronized signal
VSYNC	DIO	Vertical synchronized signal

Signal Name	Type	Description
3D_SYNC_OUT	DIO	3D sync signal for 3D Pnale
VX1_A_HTPDN	DI	VX1 channel A hot plug detect
VX1_B_HTPDN	DI	VX1 channel B hot plug detect
VX1_A_LOCKN	DI	VX1 channel A lock detect
VX1_B_LOCKN	DI	VX1 channel B lock detect
eDP_A_HPD	DI	eDP panel A hot plug detect
eDP_B_HPD	DI	eDP panel B hot plug detect

Table 4-36 Other Signal Description

Signal Name	Type	Description
GEN_CLK_OUT	DO	General clock output, for debug

5 Operating Conditions

5.1 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table 5-1 Absolute Maximum Ratings

Characteristic	Value	Unit
VDDCPU_A/B Supply Voltage	1.15	V
VDD_EE Supply Voltage	1.0	V
VDD_NPU Supply Voltage	1.0	V
VDD_GPU Supply Voltage	1.0	V
VDD_DDR Supply Voltage	1.0	V
VDDQ Supply Voltage	1.4	V
VDDQLP Supply Voltage	1.4	V
AVDD_DDR0PLL	1.98	V
AVDD_DDR1PLL	1.98	V
1.8V Supply Voltage	1.98	V
3.3V Supply Voltage	3.63	V
Input voltage, V_I	-0.3 ~ VDDIO+0.3	V
Junction Temperature	125	°C

5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDCPU	Voltage for Cortex CPU	0.68[1]	-	1.03[2]	V
VDD_EE and other 0.8V domain	Voltage for core logic	0.77	0.83	0.9[2]	V
VDD_GPU	Voltage for GPU	0.77	0.83	0.9[2]	V
VDD_NPU	Voltage for NNA	0.77	0.83	0.9[2]	V
VDD_DDR[6]	Voltage for DDR	0.77	0.80~-0.84	0.9	V
VDDQ	DDR IO Supply Voltage	1.06	-	1.26	V
VDDQLP[5]	DDR IO Supply Voltage	0.57	-	1.26	V
AVDD18	1.8V AVDD for HDMI, USB, SARADC, PCIe, AUDIO, MIPI_DSI, MIPI_CSI and ETHERNET phy.	1.74	1.80	1.89	V
VDD18_AO	1.8V VDD for XTAL, SARADC, efuse and IOVREF	1.74	1.80	1.89	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD_DDR0PLL and AVDD_ DDR1PLL	Analog power supply for DDRPLL module	1.06	-	1.89	V
AVDD33	3.3V AVDD for USB and HDMI RX	3.15	3.3	3.45	V
VDDIO	LV mode	1.71	1.80	1.89	V
	HV mode	3.0[3]	3.3	3.45	V
T_J	Operating Junction Temperature	0	-	105[4]	°C
T_A	Operating Ambient Temperature	0	-	70	°C

Note

1. Minimal VDDCPU_A/B voltage is for sleep mode while system runs at very low speed. Higher clock will need higher voltage. Considering the power supply may have 2% deviation, the minimal voltage in actual application should not be set to lower than min spec plus 0.02V.
2. Likewise, maximum VDDCPU_A/B voltage in actual application should not be higher than max spec minus 0.02V. Voltage of VDDCPU_A/B will affect CPU speed. Use lower voltage when CPU runs on lower speed to save power. Recommend to use +/-1.5% or higher precision DCDC.
3. GPIO cannot work if VDDIO voltage is out of the spec of LV / HV mode. GPIO output at HV mode will be weaker & max operating speed will be lower if VDDIO are design to 3.0V. Do not design VDDIO to lower than 3.0V in HV mode, recommend to use +/-1.5% or higher precision DCDC to supply power for VDDIO, actual voltage supplies to VDDIO (HV mode) should not be lower than 2.9V.
4. For operating temperature, good heat sink may be needed to guarantee T_J < max spec.
5. When not in LPDDRx mode, the VDDQLP supply pin should be tied to the VDDQ supply.
6. The minimum and typical voltage of VDD_DDR needs to be increased by 0.3V(Min 0.80V and Typ 0.83V) When the target rate is >3733Mbps for LPDDR4 and LPDDR4X mode.
7. The voltage requirements is for DC level.
8. IO interfaces supporting 200Mbps data rate or 100M clock and above must be powered by 1.8V instead of 3.3V. For example, eMMC (HS200/400 mode) or RGMII interface must be powered by 1.8V.

5.3 Ripple Voltage Specifications

Table 5-3 Ripple Voltage Specifications

Power	Max Ripple	Unit	Test State
VDDCPU_A	40	+/-mV	Run APK StabilityTest
VDDCPU_B	40	+/-mV	Run APK StabilityTest
VDD_EE and other 0.8V domain	40	+/-mV	Play 4K video
VDD_NPU	40	+/-mV	
VDD_GPU	70	+/-mV	Run APK Basemark ES 2.0 Taiji
DDR4 VDD_DDR	40	+/-mV	Kernel boot

Power	Max Ripple	Unit	Test State
LPDDR4/LPDDR4 VDD_DDR	32	+/-mV	Kernel boot
DDR4 VDDQ and AVDD_DDR0PLL, AVDD_DDR1PLL	60	+/-mV	Kernel boot
LPDDR4/LPDDR4X VDDQ and AVDD_DDR0PLL,AVDD_DDR1PLL	27.5	+/-mV	Kernel boot
LPDDR4 VDDQLP	45	+/-mV	Kernel boot
LPDDR4X VDDQLP	30	+/-mV	Kernel boot
AVDD18	30	+/-mV	Kernel boot
VDD18_AO_XTAL	30	+/-mV	Kernel boot
AVDD33	50	+/-mV	WIFI SCAN
VDDIO LV	60	+/-mV	Kernel boot
VDDIO HV	60	+/-mV	WIFI SCAN

Note

The ripple specifications are for reference only. Customers should perform pressure / performance / reliability tests (high / low temperature tests, wet / heat tests, functional tests, etc.) on the product to confirm system stability.

5.4 Thermal Resistance

Jedec 2P2S board 101.5mm*114.5mm, natural convection, ambient temperature 25°C.

Symbol	Parameter	Value(°C/ Watt)	Air Flow(m/s)
Θ_{JA}	Package junction-to- ambiance thermal resistance in nature convection	12.6	0
Θ_{JB}	Package junction-to-pcb thermal resistance in nature convection	2.9	0
Θ_{JC}	Package junction-to-case thermal resistance in nature convection	0.1	0

Note

1. Due to the thinness of the SOC, DRAM or capacitors placed close to SOC may prevent heat-sink touching SOC top side. A special convex shape heatsink is recommended.
2. For more information, check the following JEDEC standards:
   - JESD51-2A: Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
   - JESD51-8: Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board
   - JESD51-12: Guidelines for Reporting and Using Electronic Package Thermal Information
3. m/s = meters per second

5.5 DC Electrical Characteristics

5.5.1 Normal GPIO Specifications

Table 5-4 Normal GPIO Specifications (For DIO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{iH(VDDIO=3.3V)}$	High-level input voltage	IOVREF +0.37	-	VDDIO+0.3	V
$V_{iL(VDDIO=3.3V)}$	Low-level input voltage	-0.3	-	IOVREF-0.23	V
$V_{iH(VDDIO=1.8V)}$	High-level input voltage	IOVREF/2 +0.3	-	VDDIO+0.3	V
$V_{iL(VDDIO=1.8V)}$	Low-level input voltage	-0.3	-	IOVREF/2-0.3	V
$R_{PU/PD}$	Built-in pull up/down resistor	-	41K		ohm
IoL/IoH(DS=0)[4]	GPIO driving capability	0.5	-	-	mA
IoL/IoH(DS=1)	GPIO driving capability	2.5	-	-	mA
IoL/IoH(DS=2)	GPIO driving capability	3	-	-	mA
IoL/IoH(DS=3)	GPIO driving capability	4[1]	-	-	mA
VOH	Output high level with IoL/ IoH loading	VDDIO-0.5	-	-	V
VOL	Output low level with IoL/ IoH loading	-	-	0.4	V

Note

1. With Minimal IoL/IoH driving capability loading, IO is garanteed to meet Vol < 0.4V or VOH > (VDDIO-0.5V) spec.
2. Maximal GPIO loading is 6mA for application such as driving LED, which does not care about Vol/Voh spec. Please set DS=3 for such application.
3. VDD18_AO supplies power to IOVREF.
4. Do not use this setting, it's too weak for most applications.

5.5.2 Open Drain GPIO Specifications (For DIO_OD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{iH}(OD5V)	High-level input voltage	1.5		5.5	V
V_{iL}(OD5V)	Low-level input voltage	-0.3		0.8	V
$R_{PU/PD}$	No built-in pull up/down resistor on OD IO	-	-	-	ohm

Symbol	Parameter	Min.	Typ.	Max.	Unit
Io	OD IO driving low capability	4		6	mA
VOL	Output low level with min Io loading			0.4	V

Note

1. With Minimal IoL driving capability loading, IO is guaranteed to meet Vol<0.4V spec
2. Maximal GPIO loading is 6mA for application such as driving LED, which does not care about Vol spec
3. The V_{iL} / V_{iH} of OD PAD is irrelevant to VDDIO voltage.
4. “OD 5V” means that in applications such as I2C, use a resistor greater than 1Kohm to pull it up to 5V. Do not connect the pad directly to the 5V power supply.

5.5.3 DDR4/LPDDR4/LPDDR4X SDRAM Specifications

Table 5-5 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDQ	PHY supply voltage (DDR4)	1.14	1.20	1.26	V
VDDQ[1]	PHY supply voltage (LPDDR4)	1.06	1.1	1.17	V
VDDQ[1]	PHY supply voltage (LPDDR4X)	1.06	1.1	1.17	V
VDDQLP	IO supply voltage (DDR4)	1.14	1.20	1.26	V
VDDQL-P[2]	IO supply voltage (LPDDR4)	1.06	1.1	1.17	V
VDDQL-P[3]	IO supply voltage (LPDDR4X)	0.57	0.6	0.65	V
Vref	Input reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V

Note

1. The minimum and typical voltage of VDDQ needs to be increased by 0.3V(Min 1.09V and Typ 1.13V) When the target rate is >3733Mbps for LPDDR4 and LPDDR4X mode.
2. The minimum and typical voltage of VDDQLP needs to be increased by 0.3V(Min 1.09V and Typ 1.13V) When the target rate is >3733Mbps for LPDDR4 mode.
3. The minimum and typical voltage of VDDQLP needs to be increased by 0.3V(Min 0.60V and Typ 0.63V) When the target rate is >3733Mbps for LPDDR4X mode.

Table 5-6 Address and command DC specifications – DDR4 Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VdlVW_total	Rx Mask voltage-p-p total			136	mv
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	200	240	280	ohm
		100	120	140	
		67	80	93	
		50	60	70	
		42	48	56	
		34	40	46	
		28	34	40	

Table 5-7 Address and command DC Specifications – LPDDR4 Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOH	DC output logic high	0.9*VDDQ	-	-	V
VOL	DC output logic low	-	-	0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	216	240	264	ohm
		108	120	132	
		72	80	88	
		54	60	66	
		43.2	48	52.8	
		36	40	44	

Table 5-8 Address and command DC Specifications – LPDDR4X Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOH	DC output logic high	0.8*VDDQ	-	-	V
VOL	DC output logic low	-	-	0.2*VDDQ	V
RTT	Input termination resistance to VDDQ	216	240	264	ohm
		108	120	132	
		72	80	88	
		54	60	66	
		43.2	48	52.8	
		36	40	44	

5.6 Timing Information

5.6.1 I2C Timing Specification

The I2C master interface Fast/Standard mode timing specifications are shown below.

Figure 5-1 I2C Interface Timing Diagram, FS mode

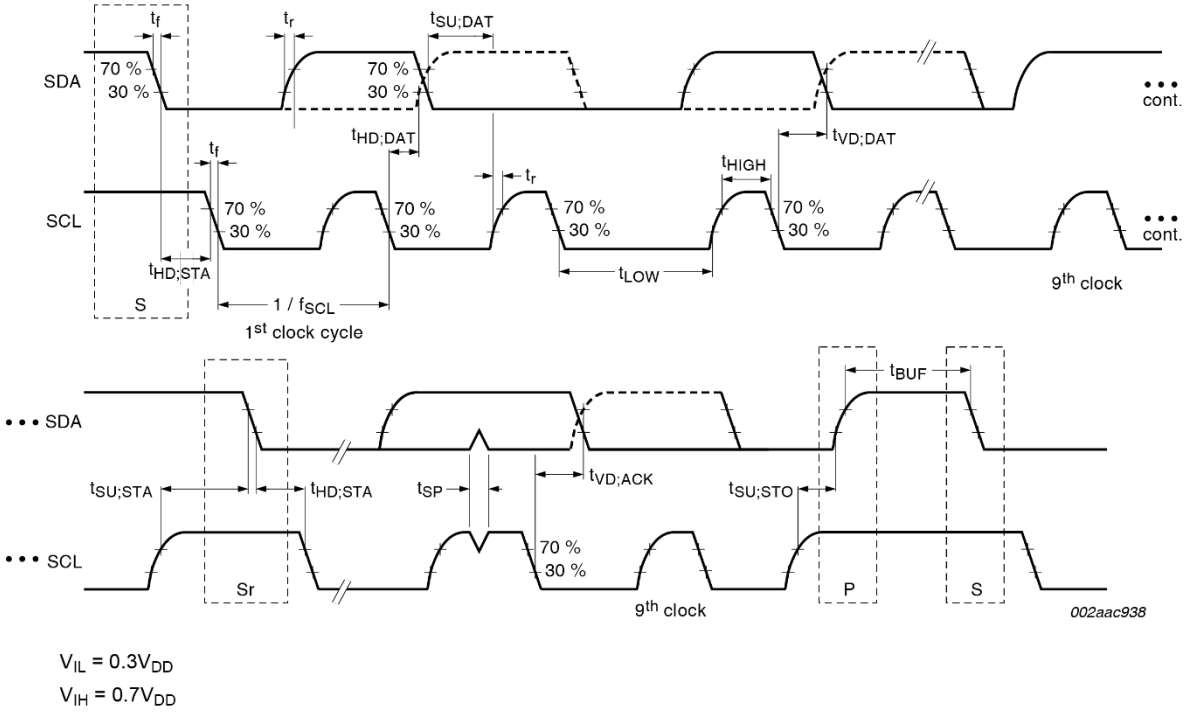


Table 5-9 I2C Interface Timing Specification, SF mode

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min.	Max	Min	Max	
tR	Rise time of SDA and SCL signals	-	1000	-	300	ns
tF	Fall time of SDA and SCL signals	-	300	-	300	ns
fSCL	SCL clock frequency	-	100	-	400	KHz
tLOW	LOW period of the SCL clock	4.7	-	1.3	-	μs
tHIGH	HIGH period of the SCL clock	4	-	0.6	-	μs
tSu;STA	Setup time for START	4.7	-	0.6	-	μs
tSu;DAT	Setup time for SDA	250	-	100	-	ns
tSu;STO	Setup time for STOP	4	-	0.6	-	μs

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min.	Max	Min	Max	
tHd;STA	Hold time for START	4	-	0.6	-	µs
tHd;DAT	Hold time for SDA	0	3.45	0	0.9	µs
tBuf	Bus free time between stop and start	4.7	-	1.3	-	µs

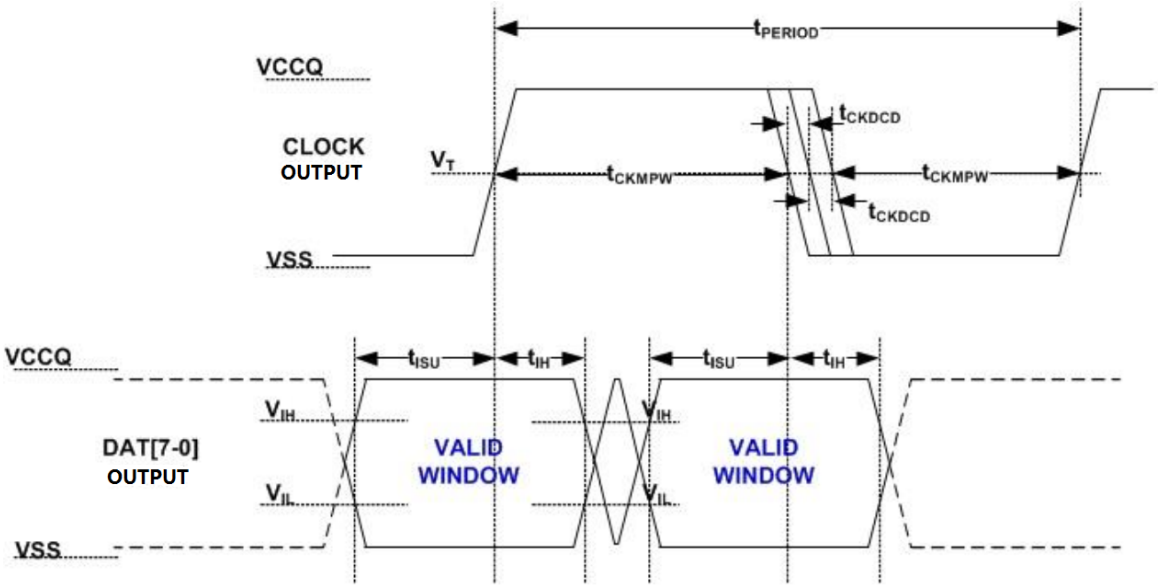
Note

Open drain does not support driver strength adjustment.

5.6.2 EMMC/SD Timing Specification

Timing specification for EMMC and SDIO are shown as below.

Figure 5-2 EMMC HS400 Data Output Timing



NOTE V_T = 50% of V_{CCQ}, indicates clock reference point for timing measurements.

Table 5-10 HS400 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
SR	Slew rate	1.125	-	V/ns
tCKDCD	Duty cycle distortion	0	0.3	ns
tCKMPW	Minimum pulse width	2.2	-	ns
tISU	input set-up time	1.4	-	ns
tIH	input hold time	0.8	-	ns

Symbol	Parameter	Min	Max	Unit
tISUddr	input set-up time	0.4	-	ns
tIHddr	input hold time	0.4	-	ns

Figure 5-3 EMMC HS200 Data Output Timing

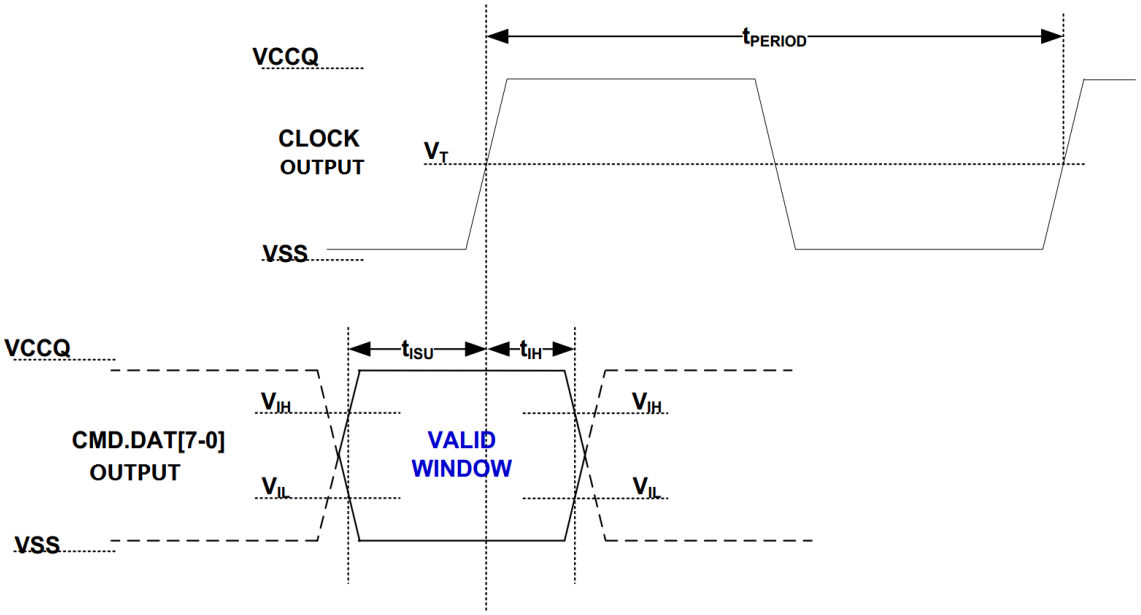


Table 5-11 HS200 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
tISU	output set-up time	1.4	-	ns
tIH	output hold time	0.8	-	ns

Figure 5-4 EMMC HS400 Data Input Timing

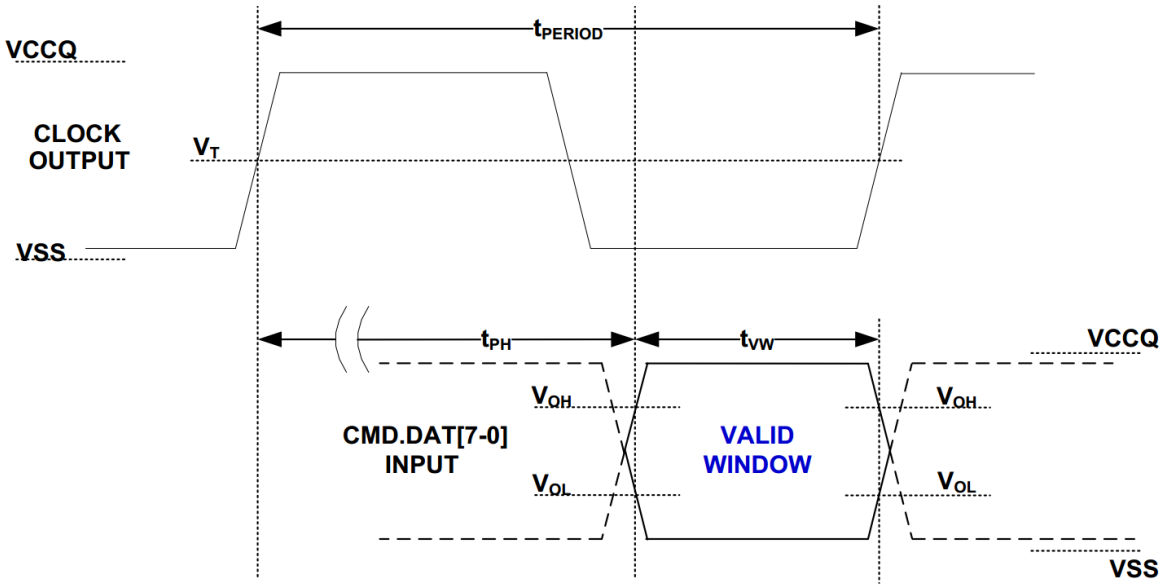


Table 5-12 HS400 Data Input Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
SR	Slew rate	1.125	-	V/ns
tCKDCD	Duty cycle distortion	0	0.2	ns
tCKMPW	Minimum pulse width	2	-	ns
tRQ	Input skew	-	0.4	ns
tRQH	input hold skew	-	0.4	ns

Figure 5-5 EMMC HS200 Data Input Timing

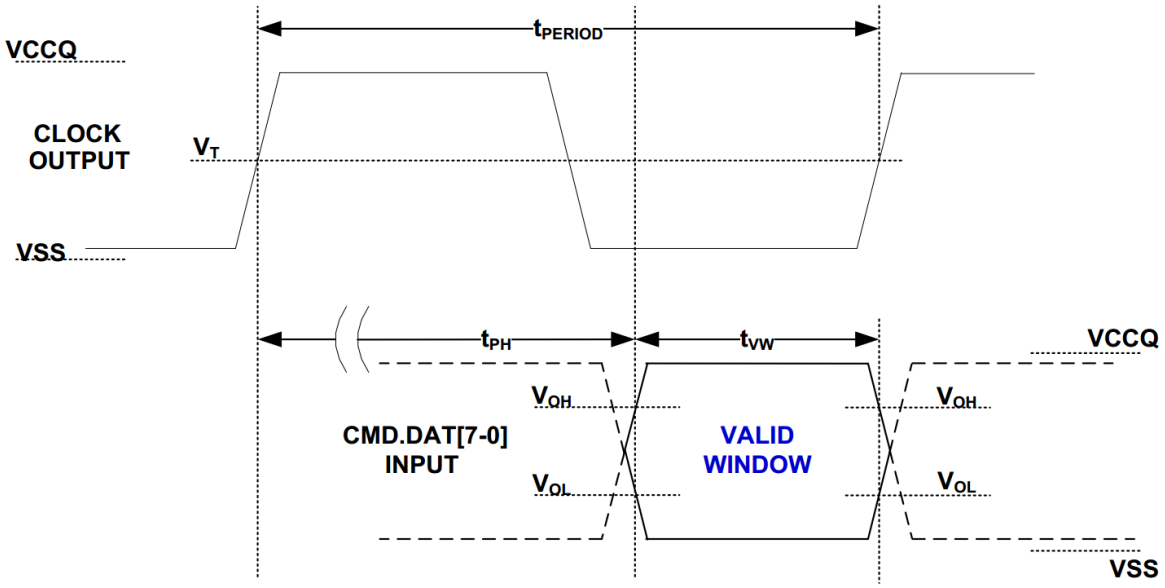


Table 5-13 HS200 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPH	Device output momentary phase from CLK input to CMD or DAT line output. Does not include a longterm temperature drift.	0	2	UI
ΔTPH	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (TVW) from last system Tuning procedure ΔTPH is 2600ps for ΔT from -25 °C to 125 °C during operation.	-350(ΔT=-20deg.C)	1550(ΔT=90deg.C)	ps
tVW	Valid Data Simple window	0.575	-	UI

Figure 5-6 SDIO (SDR104) Clock Signal Timing Diagram

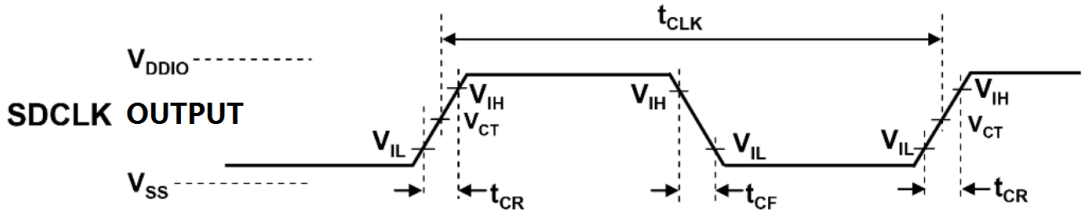


Table 5-14 SDIO (SDR104) Clock Timing Specification

Symbol	Parameter (SDR104 Mode)	Min	Max	Unit
tCLK	clock period Data Transfer Mode (PP)	4.8	-	ns
Duty	Clock Duty	30	70	%
tCR	clock rise time	-	0.96	ns
tCF	clock fall time	-	0.96	ns

Figure 5-7 SDIO (SDR104) Output Timing Diagram

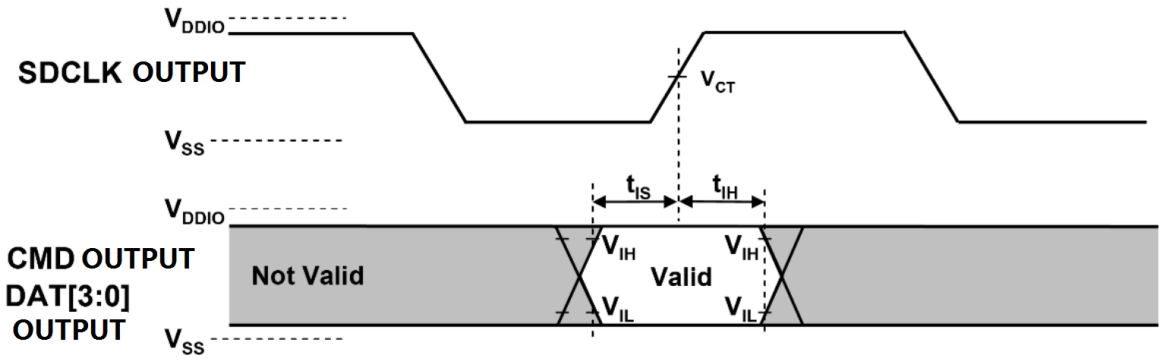


Table 5-15 SDIO (SDR104) Output Timing Specification

Inputs CMD, DAT (referenced to CLK)				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
tIS	input set-up time	1.4	-	ns
tIH	input hold time	0.8	-	ns

Note

SD card interface uses SDIO protocol.

5.6.3 NAND Timing Specification

Nand timing specifications are shown as below.

Figure 5-8 Async Waveform for Command/Address/Data Output Timing

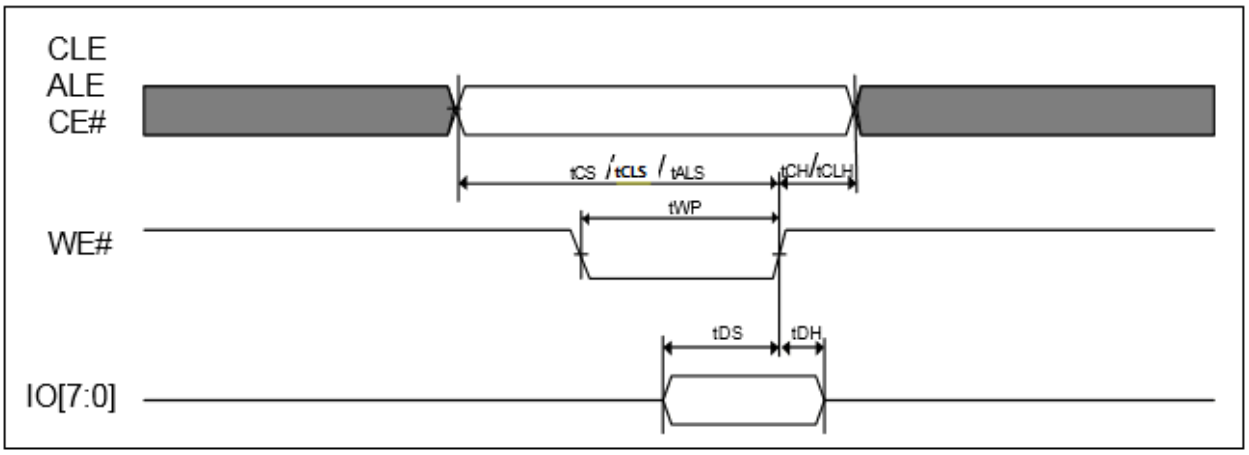


Figure 5-9 Async Waveform for Address Output Cycle

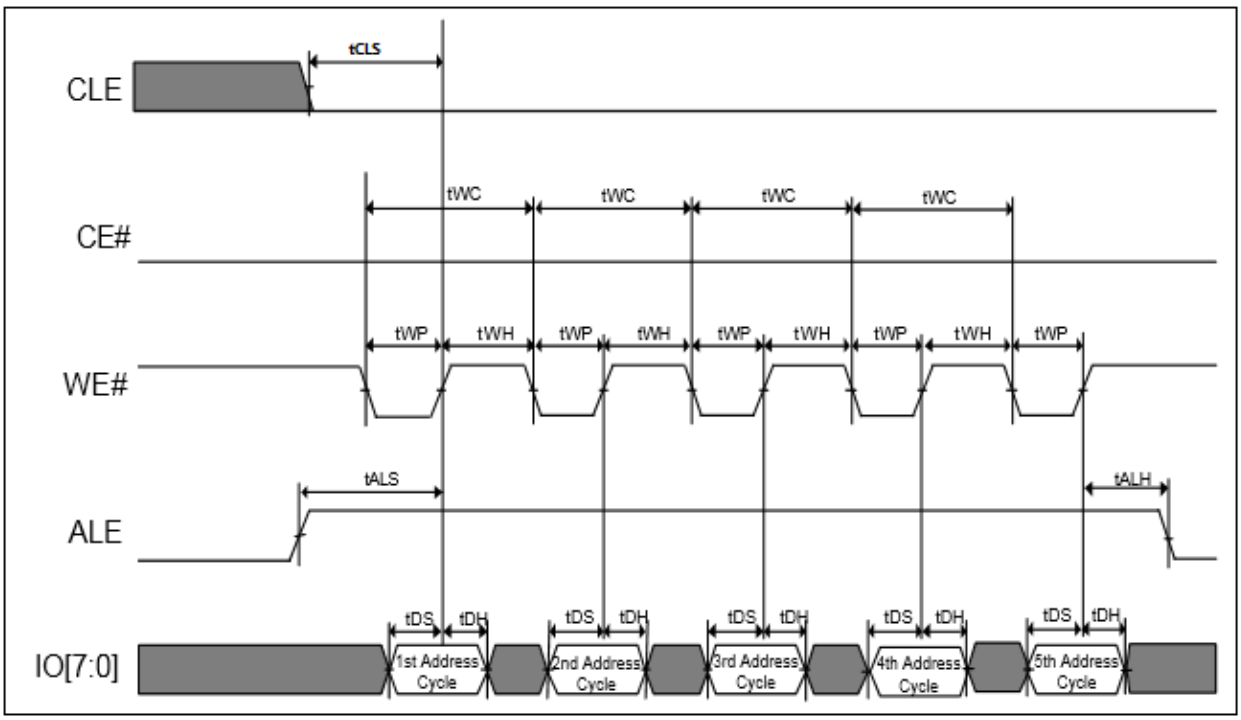


Figure 5-10 Async Waveform for Sequential Data Read Cycle(After Read)-EOD Mode

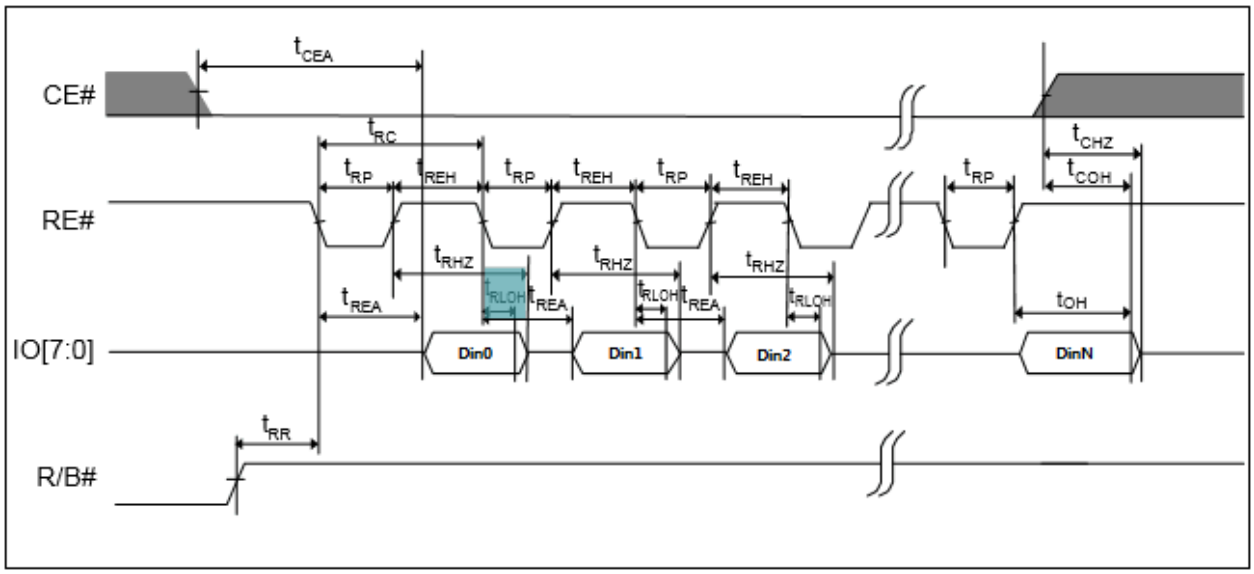


Table 5-16 Nand Timing Specifications

Symbol	Parameter (Asyn-chronous) (mode 5)	Min	Max	Unit
tCLS	CLE setup time	10	-	ns
tCLH	CLE hold time	5	-	ns
tALS	ALE setup	10	-	ns
tALH	ALE hold	5	-	ns
tDS	Data setup time	7	-	ns
tDH	Data hold time	5	-	ns
tWC	WE# cycle time	20	-	ns
tWP	WE# pulse width	10	-	ns
tWH	WE# high lold time	7	-	ns
tREA	RE# access time	-	16	ns
tOH	Data output hold time	15	-	ns
tRLOH	RE#-low to data hold time (EDO)	5	-	ns
tRP	RE# pulse width	10	-	ns
tREH	RE# high hold time	7	-	ns
tRC	RE# cycle time	20	-	ns

5.6.4 SPICC Timing Specification

Figure 5-11 SPICC Timing Diagram

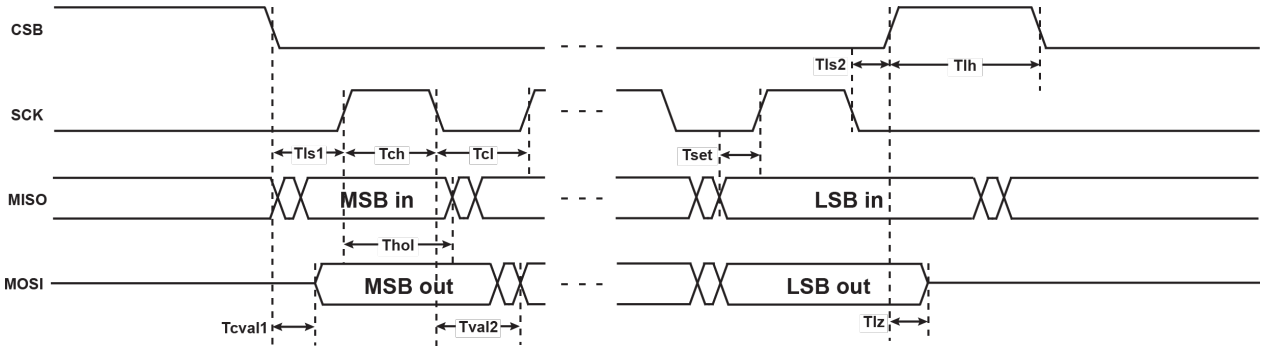


Table 5-17 SPICC Master Timing Specification

Symbol	Description	Min.	Max.	Unit
fCLK	Clock Frequency	1	80	MHz
TCH	Clock high time	5		ns
TCL	Clock low time	5		ns
TLS1	CS fall to First Rising CLK Edge	50		ns
TSET	Data input Setup Time	4		ns
THOL	Data input Hold Time	4		ns
TLH	Minimum idling time between transfers (minimum ss high time)	5		ns

5.6.5 SPIFC Timing Specification

Figure 5-12 SPIFC Serial Input Timing Diagram

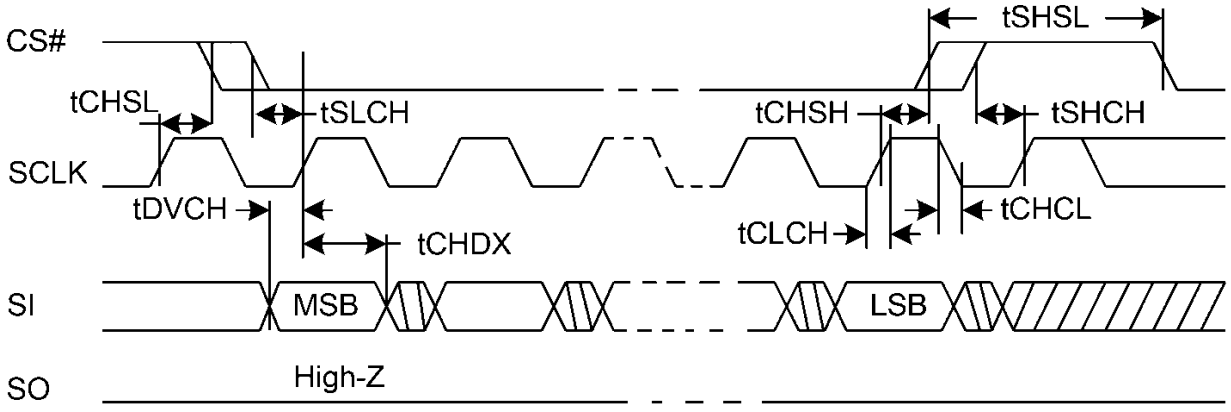


Figure 5-13 SPIFC Out Timing Diagram

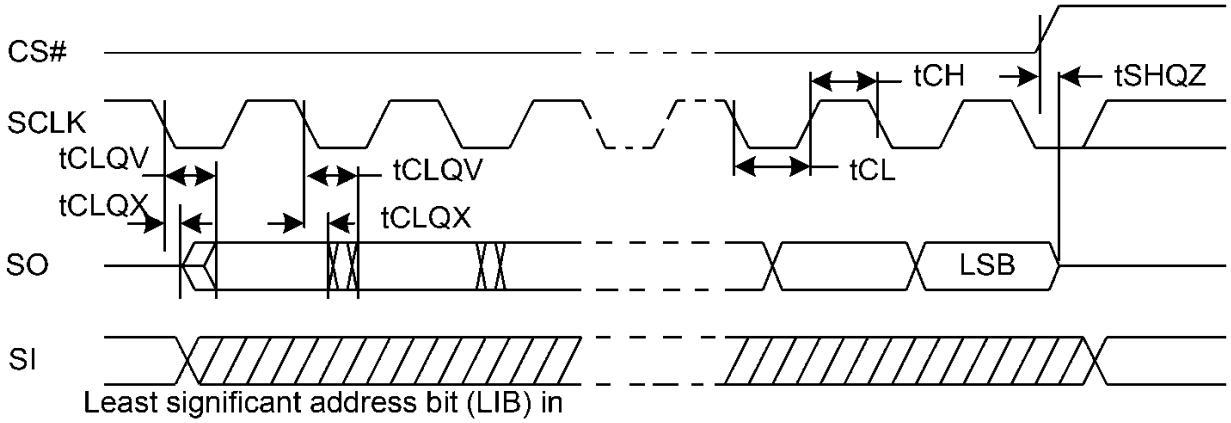


Table 5-18 SPIFC Master Timing Specification

Symbol	Parameter (Clock 41.7MHz)	Min	Max	Unit
fRSCLK	Clock Frequency for READ instructions		50	Mhz
tCH	Clock High Time	8		ns
tCL	Clock Low Time	8		ns
tCLCH	Clock Rise Time (peak to peak)	0.1		V/ns
tCHCL	Clock Fall Time (peak to peak)	0.1		V/ns
tSLCH	CS# Active Setup Time (relative to SCLK)	4	-	ns
tCHSH	CS# Active Hold Time (relative to SCLK)	4	-	ns
tDVCH	Data In Setup Time	2	-	ns
tCHDX	Data In Hold Time	3	-	ns
tSHQZ	Output Disable Time (relative to CS#)		8	ns
tCLQV	Clock Low to Output Valid		6	ns
tCLQX	Output Hold Time	1		ns

5.6.6 Ethernet Timing Specification

Figure 5-14 Management Data Timing Diagram

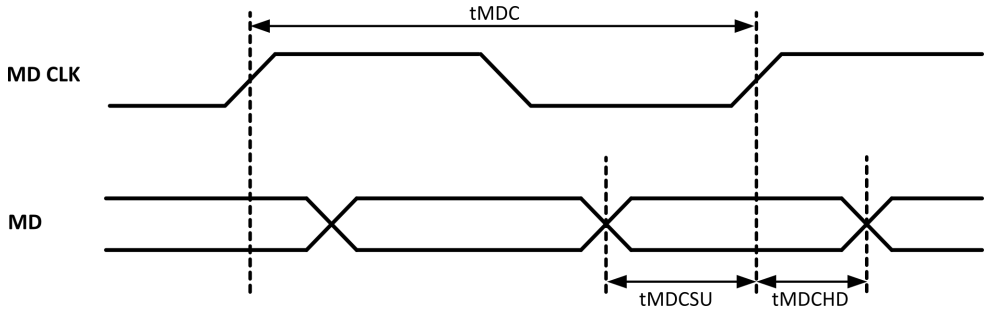


Table 5-19 Management Data Timing Specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
tMDC	MDC clock Period	400	500		ns	From MAC
tMDCSU	Setup time to rising edge of MDC	10			ns	
tMDCHD	Hold time to rising edge of MDC	10			ns	

Figure 5-15 RMII Timing Diagram

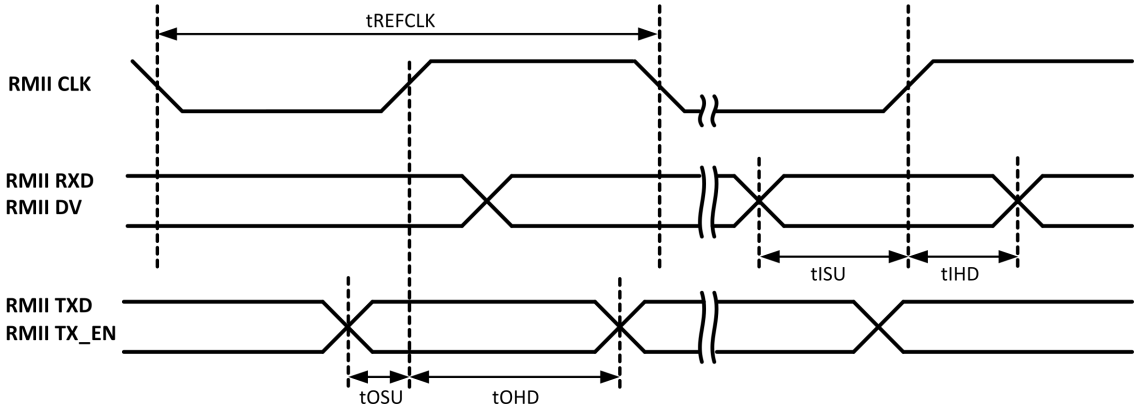


Table 5-20 RMII Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tREFCLK	RMII clock period		20		ns	50MHz from PHY
tOSU	TXD & TX_ EN setup time to rising edge of RMII clock	1.8	10		ns	To PHY
tOHD	TXD & TX_ EN hold time to rising edge of RMII clock	1.4	10		ns	To PHY
tISU	RXD & DV setup time to rising edge of RMII clock	1.0	10		ns	From PHY
tIHD	RXD & DV hold time to rising edge of RMII clock	1.0	10		ns	From PHY

Figure 5-16 RGMII Receive Timing Diagram

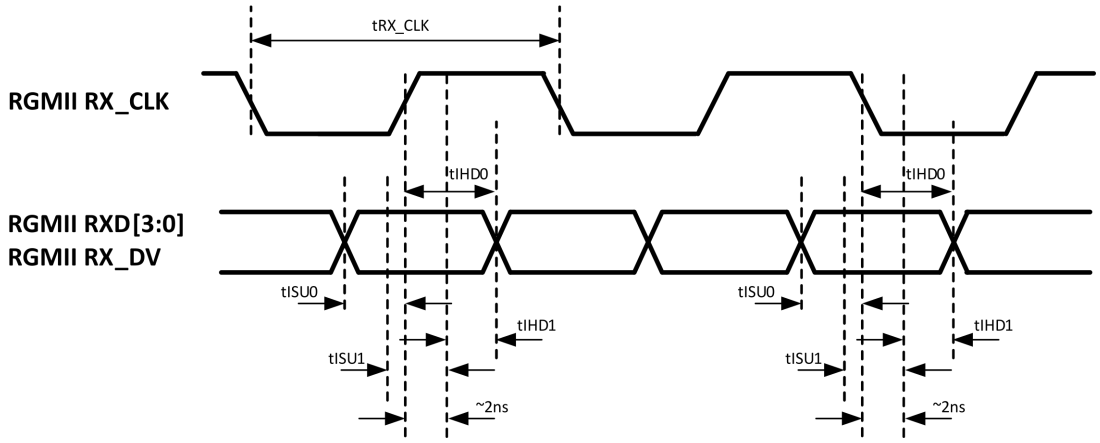


Table 5-21 RGMII Receive Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tRX_CLK	RGMII RX_ CLK clock period		8		ns	125MHz from PHY
tSETUP	RXD[3:0] & RX_DV setup time (PHY internal delay enabled)	1.2			ns	From PHY
tHOLD	RXD[3:0] & RX_DV hold time (PHY internal delay enabled)	1.2			ns	From PHY
tSKEW	RXD[3:0] & RX_DV skew between these 5 signals (PHY internal delay disabled)	-0.5		0.5	ns	From PHY

When PHY internal delay is enabled, check setup/hold timing.

When PHY internal delay is disabled, check signal skew.

Figure 5-17 RGMII Transmit Timing Diagram

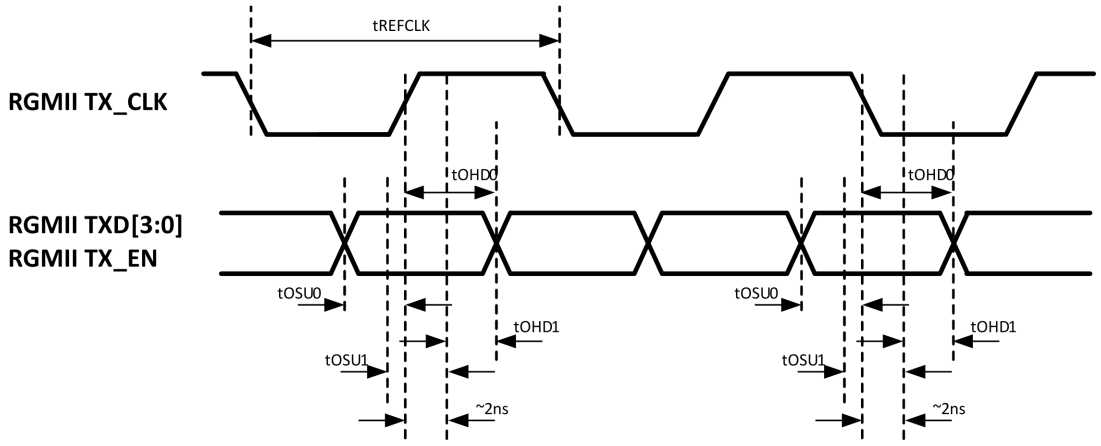


Table 5-22 RGMII Transmit Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tTX_CLK	RGMII TX_ CLK clock period		8		ns	125MHz to PHY
tOSU	TXD & TX_ EN setup time to rising edge of RGMII clock (no clock delay added)	1			ns	From PHY
	TXD & TX_ EN setup time to rising edge of RGMII clock (clock delay added)	-0.9			ns	From PHY
tOHD	RXD & DV hold time to rising edge of RGMII clock (no clock de-lay added)	0.8			ns	From PHY
	RXD & DV hold time to rising edge of RGMII clock (clock delay added)	2.7			ns	From PHY

5.6.7 Audio Timing Specification

There are two modes for the audio I2S/TDM interface: Master mode and Slave mode, as shown below.

Figure 5-18 I2S/TDM Timing Diagram, Master Mode

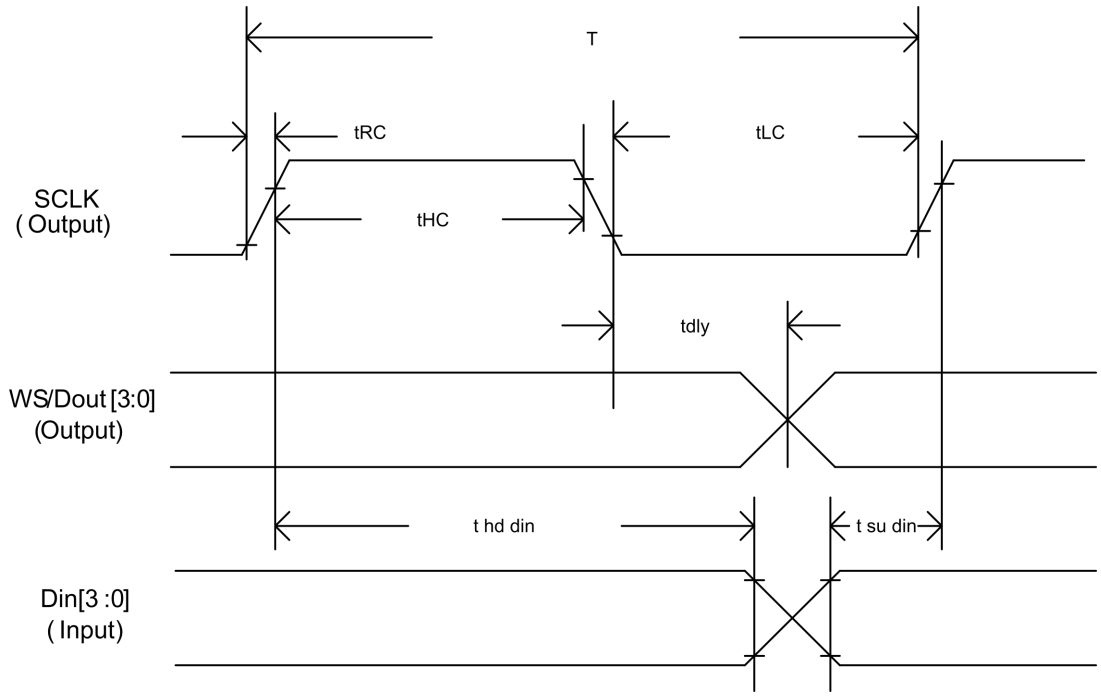


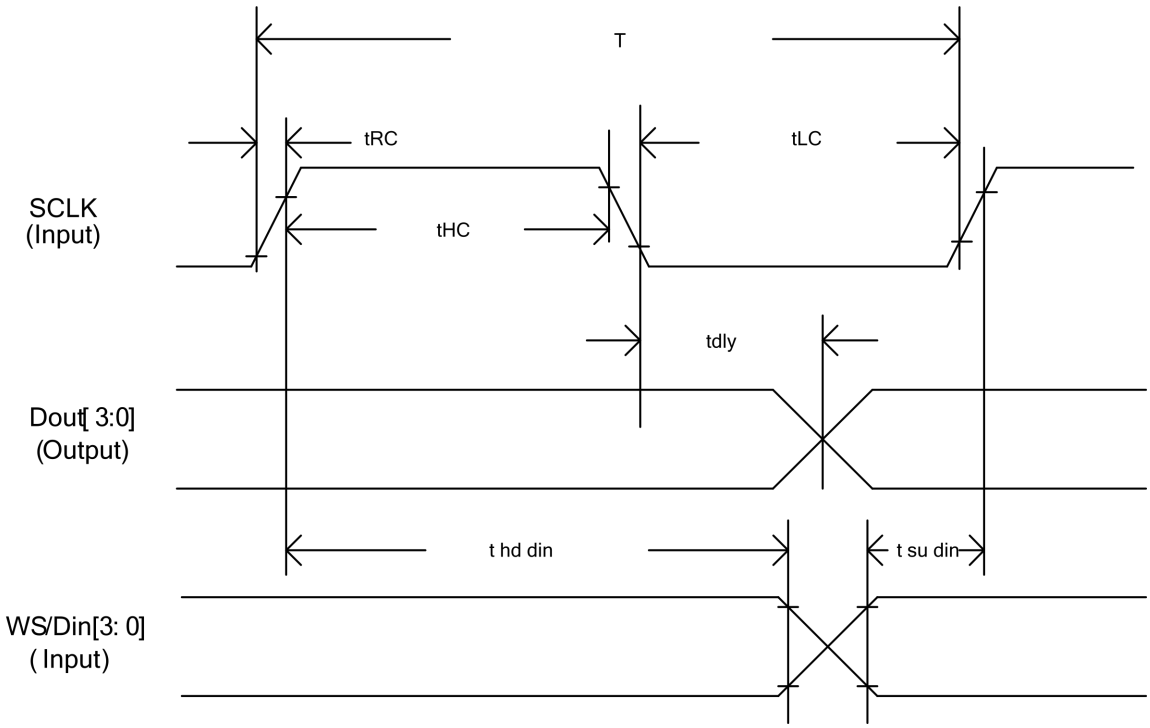
Table 5-23 Audio I2S/TDM Timing Specification, Transmitter, Master Mode

Transmitter (master mode)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
T	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.15	T
tdly	Delay from SCLK to WS	-2	3	5	
tsuin	Setup time of Din	4			ns
thdin	Hold time of Din	4			ns

Note

Measure Pointrefers to VIH, ViL parameter of Normal GPIO Specifications.

Figure 5-19 2S/TDM Timing Diagram, Slave Mode



Transmitter (slave mode)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**unit**
T(out)	Clock period	40			ns
T(in)	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tsu in	Setup time of WS/Din	4			ns
thd in	Hold time of WS/ Din	4			ns
tdly	Delay between SCLK and Dout	2	12	15	ns

Note

Measure Pointrefers to VIH, ViL parameter of Normal GPIO Specifications.

5.6.8 PDM Timing Specification

Figure 5-20 PDM Timing Diagram

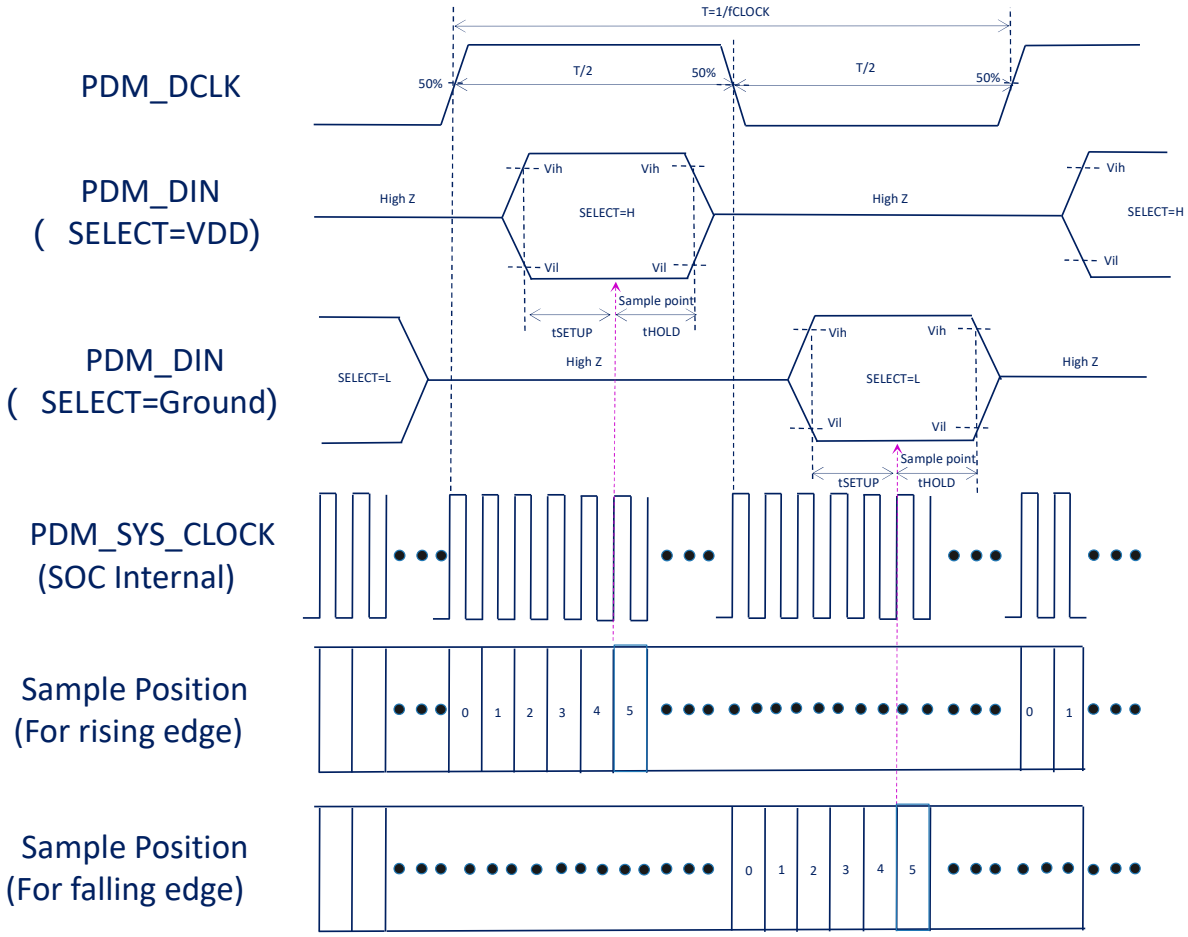


Table 5-24 PDM Timing Specification

Parameter	Symbol	Min.	Typ.	Max.	Units.
PDM clock period	tDCLK	200			ns
PDM clock duty cycle	tHIGH/tLOW	48%		52%	tDCLK
PDM Data setup time	tSETUP	20			ns
PDM Data hold time	tHOLD	20			ns
Sys clock period	tSYSCLK	5	7.5		ns

Note

1. Default PDM_SYS_CLOCK=133MHz.
2. For Sample position, please refer to PDM register PDM_CHAN_CTRL,PDM_CHAN_CTRL1.

5.6.9 UART Timing Specification

Figure 5-21 UART Timing Diagram

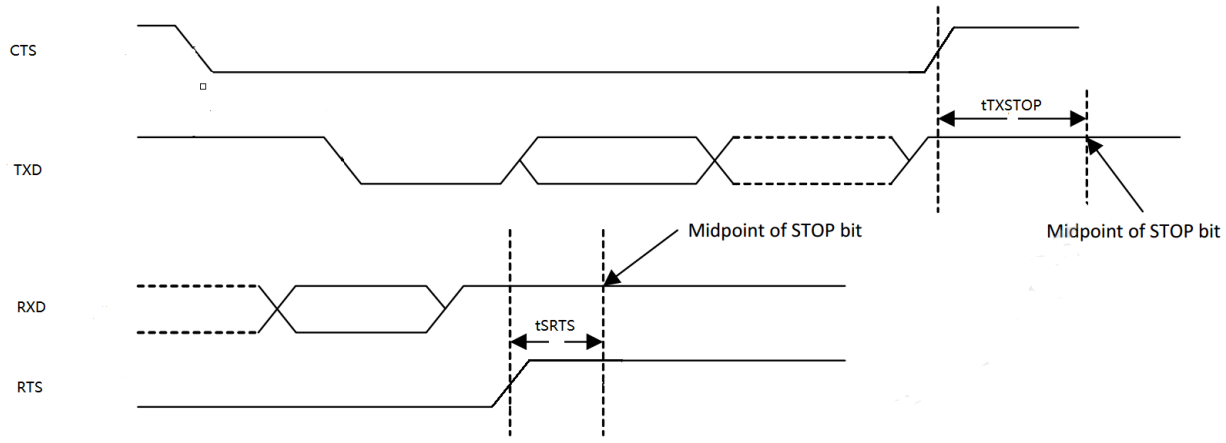


Table 5-25 UART Timing Specification

Parameter	Symbole	Min.	Max.	Units.
Delay time, CTS high before midpoint of stop bit	tTXSTOP	-	0.5	Bit Periods
Delay time, midpoint of stop bit to RTS hgih	tSRTS	-	0.5	Bit Periods

5.7 Recommended Oscillator Electrical Characteristics

The SoC requires the 24MHz oscillator for generating the main clock source.

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_o	Nominal Frequency		24		MHz	
$\Delta f/f_o$	Frequency Tolerance	-30		30	ppm	At 25 ℃
		-50		50	ppm	At -20~85 ℃
C_L	Load Capacitance	7.5	12	12.5	pF	
ESR	Equivalent Series Resistance			100	oHm	

Note

1. 10ppm Tolerance is preferred if 24MHz XTAL is also driving WIFI module.
2. For user external clock source, please connect input clock output to SYS_OSCIN , let SYS_ OSCOUT floating.
3. The threshold of Xin inverter is around 0.9V (Xin range: -0.45V to +2.1V). Therefore, Following suggestion for input clock.
   - Suggestion 1: Without DC blocking capacitor, use a higher Vpp output TCXO. The high voltage should be higher than 1.35V (VSWING >1.35V, 0V to >1.35V).
   - Suggestion 2: With DC blocking capacitor, re-bias the middle voltage at 0.9V, VSWING >2*0.45V.

5.7.1 Recommended RTC_CLK_IN Electrical Characteristics

Table 5-26 Requirement for RTC_CLK_IN

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_o	Nominal Frequency		32.768		KHz	
$\Delta f/f_o$	Frequency Tolerance	-20		20	ppm	At 25 ℃
Parabolic coefficient				-0.04	ppm/℃^{2}	

Note

If RTC_CLK_IN needs to be used for time counting, customers can choose a higher precision clk according to the error range acceptable to the actual application.

5.8 Recommended PDVFS Specification

For the CPU(A53,A73)dynamic voltage and frequency sacling specification is as follows.

freq[MHz]		500	666	1000	1200	1392	1512	1608	1704	1800	1896	2016	2208
Voltage-A73 [mV]	null	820	820	820	820	820	830	850	870	910	940	960	1010
	grp1	820	820	820	820	820	830	850	870	910	940	960	1010
	grp2	800	800	800	800	810	810	830	850	860	890	920	970
	grp3	790	790	790	790	810	810	820	830	850	860	880	920
Voltage-A53 [mV]	null	770	770	770	770	770	810	840	870	910	950	1010	
	grp1	770	770	770	770	770	810	840	870	910	950	1010	
	grp2	760	760	760	760	770	790	800	830	860	900	950	
	grp3	750	750	750	750	770	780	790	810	830	860	920	

5.9 Power On Configuration

3 Boot pins are used as power on configuration (POC) pins, to set the booting sequence.

POC setting is latched at the rising edge of reset signal.

3 POC pins are all pull high internal, CPU will try to boot from nand/eMMC first, if fails then try to boot from SD CARD, still fails then try to boot from USB (PC).

External 4.7K ohm pull down resistors can be used to change the POC setting. The resistors should be placed on right location, avoid stubs on high speed signals.

The SoC's power on configuration is listed as following:

Table 5-27 Power On Configuration Pin Table

POC	Boot Pin	Name	Pull low	Pull high
POC_2	GPIOB_2	SPINOR_FIRST	SPI NOR first	Default sequence
POC_4	GPIOB_4	SDCARD_FIRST	SDCARD boot first	Default sequence
POC_5	GPIOB_5	USB_FIRST	USB boot first	Default sequence

Table 5-28 Booting Sequence Diagram

No.	GPIOB_5 POC5	GPIOB_4 POC4	GPIOB_2 POC2	1st	2nd	3rd	4th
1	0	0	0	SD	SPINOR	eMMC	USB
2	0	0	1	SD	eMMC	SPINOR	USB
3	0	1	0	USB	SPINOR	eMMC	SD
4	0	1	1	USB	eMMC	SPINOR	SD
5	1	0	0	SD	SPINOR	eMMC	USB
6	1	0	1	SD	eMMC	SPINOR	USB
7	1	1	0	SPINOR	eMMC	SD	USB
8	1	1	1	eMMC	SPINOR	SD	USB

5.10 Power On Reset

The POR (Power On Reset) monitors VDDIO_AO power voltage and compares it to a threshold Voltage.

POR_OUT pin is low (SOC is reset mode) when VDDIO_AO is below threshold,

Note

1. Place 1nF capacitors on RESET_N Pin.
2. VDDIO_AO power pin is only support 3.3V, not allow to power off in sleep mode.

Figure 5-22 POR Wave Diagram

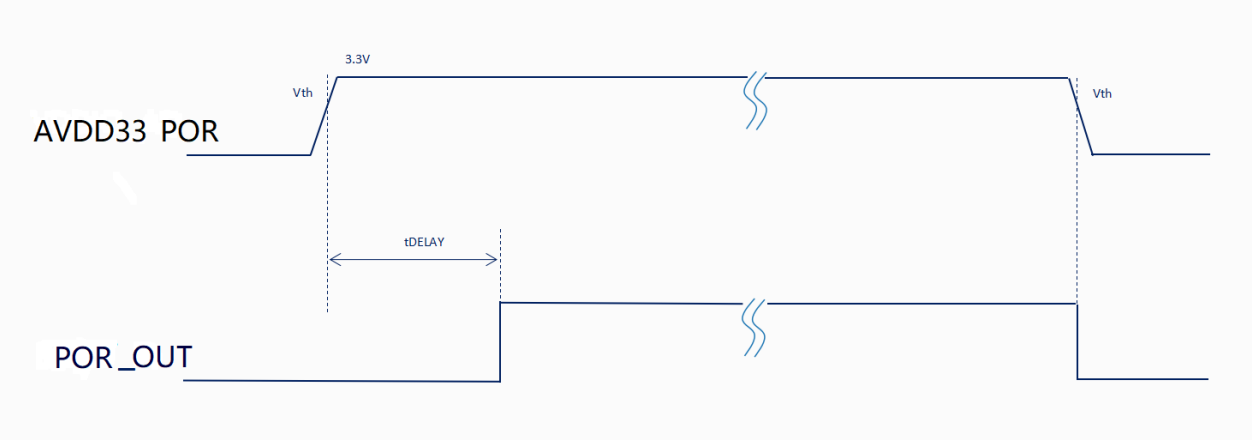


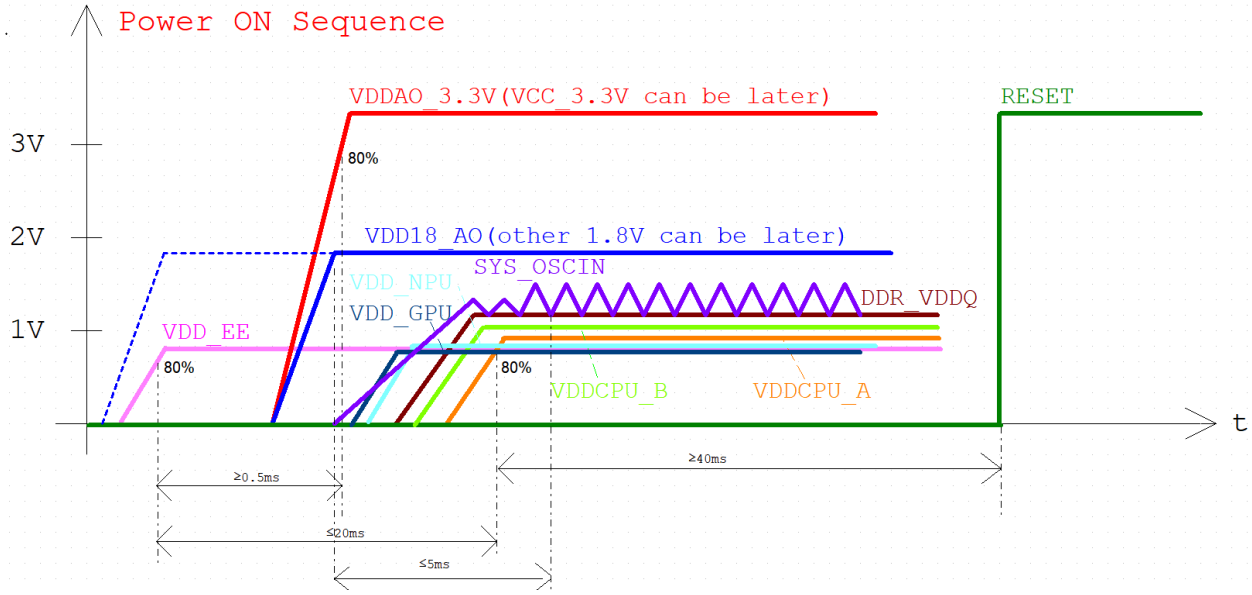
Table 5-29 POR Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset threshold for power up	Vth+	-	-	2.9	V
Reset threshold for power down	Vth-	2.5	-	-	V
Reset delay time	tDELAY	109	156	218	ms

5.11 Recommended Power On Sequence

The example of power on sequence is shown in the following figure.

Figure 5-23 Power On Sequence



Note

1. All test values refer to 80% of typical power voltage.
2. VDDAO_3.3V & VCC_3.3V should ramp up > 0.5ms later than VDD_EE.
3. All power sources should get stable within 20ms (except for DDR_VDDQ and VDD_QLP).
4. No sequence requirement between VDD18_AO and VDD_EE. No sequence requirement between VDDCPU_A & VDDCPU_B & VDD_NPU & VDD_GPU & VDDQ & VDD_QLP & VDD_DDR and other power source.
5. VDDIO_AO18 should ramps up earlier or at the same time with VDDAO_3.3V & VCC3.3V, VDDAO_3.3V & VCC3.3V should never be 2.5V higher than VDD18_AO.
6. In some designs, VDDCPU & VDD_EE are merged to VCC_CORE, the power on sequence should be same as VDD_EE.
7. RESET_n should keep low for at least 30ms after power up (except VDDQ and VDD_QLP).
8. System CLK(SYS_OSCIN pin) should be stable within in 5ms after VDD18_AO is stable.

5.12 Power Consumption

Note

Value listed here is estimated typical max value tested. Enough margin in circuit needs to be reserved.

Symbol	Maximum Current
VDD_DDR	1500
VDD_EE	3000
VDD_GPU	3000
VDD_NPU	3000
VDDCPU_A	4000
VDDCPU_B	2000
VDDQ	1500
VDDQLP	600

Symbol	Typical Current (mA)	Maximum Current (mA)	Note
AVDD_DDR0PLL	12.0		
AVDD_DDR1PLL	12.0		
AVDD08_DP	11.0		
AVDD08_HDMIRX	87.1		
AVDD08_HDMITX	11.1		At 6 Gbps mode
AVDD0V8_CSI	18.0		
AVDD0V8_USB_PCIE	54.0		

Symbol	Typical Current (mA)	Maximum Current (mA)	Note
AVDD18_MCLK	4.0		
AVDD18_DDR_ DP_PLL	4.7		
AVDD18_PLL	4.7		
AVDD18_SARADC	1.0		
VDD18_AO	3.0		Including VDD18_EFUSE, Max 100mA when Programming EFUSE
AVDD18_USB_ PCIE	85.0		
AVDD18_AUDIO	6.6		
AVDD18_CSI	9.0		
AVDD18_ENET	31.0		
AVDD18_HDMIRX_ EARCTX	23.5		
AVDD18_HDMITX_ EARCRX	22.3		
AVDD18_DP	210.0		
AVDD33_HDMIRX	90.0		Per connected channel
AVDD33_HDMITX	60.0		
AVDD33_POR	0.1		
AVDD33_USB	24.6		
VDDIO			

5.13 Storage and Baking Conditions

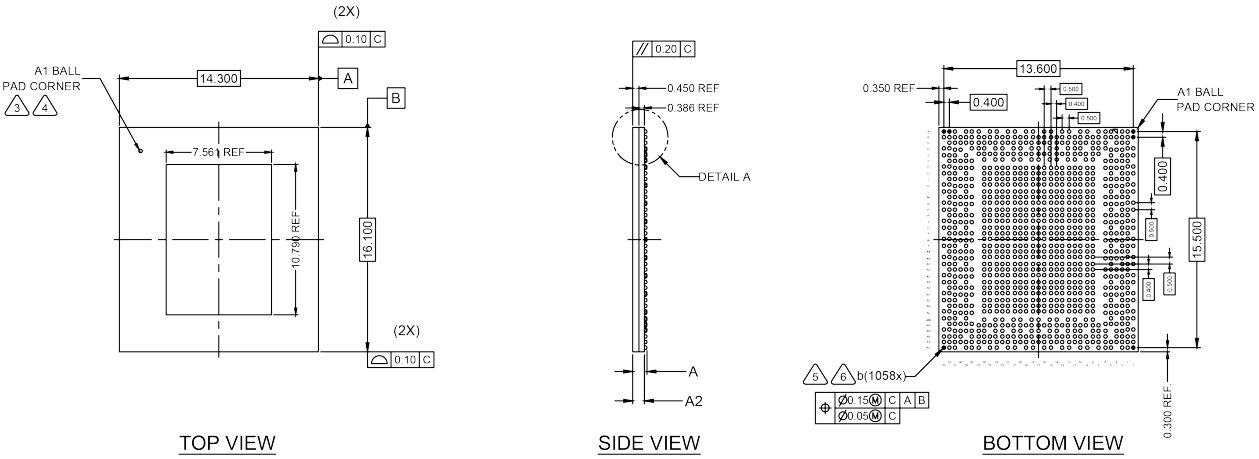
The processor is moisture-sensitive device of MSL level 3, defined by IPC/JEDEC J-STD-020. Please follow the storage and backing guidelines.

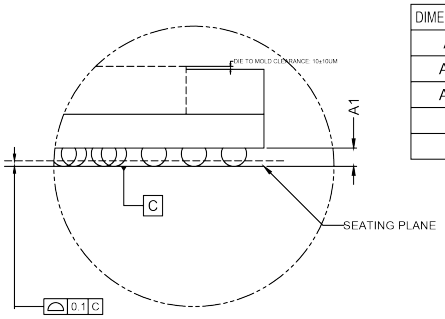
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
2. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must comply with either of the following principles.
   a. Mounted with 168 hours of factory conditions ≤30°C/60% RH
   b. Stored per J-STD-033
3. If the humidity indicator card reads >10%, devices should be baked before mounting.
4. If baking is required, see IPC/JEDEC J-STB-033 for baking process.

6 Mechanical Dimensions

The processor comes in a 14.30x16.10 ball matrix FCBGA RoHS package. The mechanical dimensions are shown as the following figures.

Figure 6-1 Dimensions





DETAIL A
ROTATED 90°

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.945	1.020	1.095
A1	0.134	0.184	0.234
A2	0.780	0.836	0.892
b	0.200	0.250	0.300
NUMBER OF BALL 1058			

7 Appendix

7.1 Net Length

The following table describes the length of all nets on the SoC.

Table 7-1 Net Length

Net Name	Net Length(um)
CSI_A_CLKN	5030.487
CSI_A_CLKP	4817.861
CSI_A_D0N	4711.585
CSI_A_D0P	4641.622
CSI_A_D1N	5211.345
CSI_A_D1P	5242.432
CSI_A_D2N	4639.844
CSI_A_D2P	4427.007
CSI_A_D3N	4653.205
CSI_A_D3P	4585.335
CSI_B_CLKN	4655.489
CSI_B_CLKP	4305.908
CSI_C_CLKN	4746.718
CSI_C_CLKP	4489.501
CSI_C_D0N	3502.054
CSI_C_D0P	3578.28
CSI_C_D1N	4059.798
CSI_C_D1P	3795.459
CSI_C_D2N	4346.695
CSI_C_D2P	3920.985
CSI_C_D3N	5064.898
CSI_C_D3P	4795.254
CSI_D_CLKN	5543.884
CSI_D_CLKP	5300.085
DDR0_AC_0	6399.3
DDR0_AC_1	6696.615
DDR0_AC_2	5038.469
DDR0_AC_3	6039.656
DDR0_AC_4	3918.165

Net Name	Net Length(um)
DDR0_AC_5	3929.111
DDR0_AC_6	3854.377
DDR0_AC_7	5378.488
DDR0_AC_8	7017.325
DDR0_AC_9	7211.078
DDR0_AC_10	5655.812
DDR0_AC_11	5389.325
DDR0_AC_12	6631.093
DDR0_AC_13	6215.168
DDR0_AC_14	6097.363
DDR0_AC_15	5612.287
DDR0_AC_20	3523.224
DDR0_AC_21	3500.304
DDR0_AC_22	3367.634
DDR0_AC_23	2940.266
DDR0_AC_24	5768.027
DDR0_AC_25	5929.304
DDR0_AC_26	4427.73
DDR0_AC_28	3227.357
DDR0_AC_29	4306.811
DDR0_AC_30	4369.684
DDR0_AC_31	5228.182
DDR0_AC_32	4015.173
DDR0_AC_33	5314.911
DDR0_AC_34	6854.232
DDR0_AC_35	5712.777
DDR0_AC_36	3944.826
DDR0_AC_37	1641.622
DDR0_AC_38	4189.761
DDR0_DQ0	6280.845
DDR0_DQ1	5166.292
DDR0_DQ2	5018.542
DDR0_DQ3	4418.469
DDR0_DQ4	3402.634
DDR0_DQ5	6233.136

Net Name	Net Length(um)
DDR0_DQ6	3823.584
DDR0_DQ7	5358.769
DDR0_DQ8	5946.746
DDR0_DQ9	3073.453
DDR0_DQ10	2543.422
DDR0_DQ11	4164.59
DDR0_DQ12	2715.204
DDR0_DQ13	3036.421
DDR0_DQ14	3232.893
DDR0_DQ15	4137.148
DDR0_DQ16	3360.979
DDR0_DQ17	3437.216
DDR0_DQ18	3321.299
DDR0_DQ19	3906.145
DDR0_DQ20	4272.024
DDR0_DQ21	4564.25
DDR0_DQ22	3755.071
DDR0_DQ23	3649.98
DDR0_DQ24	3815.958
DDR0_DQ25	3158.116
DDR0_DQ26	2963.749
DDR0_DQ27	4441.774
DDR0_DQ28	2131.234
DDR0_DQ29	2471.88
DDR0_DQ30	2877.104
DDR0_DQ31	3874.563
DDR0_DQM0	5024.362
DDR0_DQM1	3653.29
DDR0_DQM2	5294.813
DDR0_DQM3	3786.985
DDR0_DQSN0	4978.861
DDR0_DQSN1	4091.433
DDR0_DQSN2	3008.052
DDR0_DQSN3	3145.699
DDR0_DQSP0	5049.99

Net Name	Net Length(um)
DDR0_DQSP1	4162.587
DDR0_DQSP2	3220.211
DDR0_DQSP3	3224.322
DDR1_AC_0	4524.667
DDR1_AC_1	4270.125
DDR1_AC_2	5360.315
DDR1_AC_3	4796.72
DDR1_AC_4	3498.185
DDR1_AC_5	3385.999
DDR1_AC_6	4740.332
DDR1_AC_7	5654.689
DDR1_AC_8	5367.616
DDR1_AC_9	5087.63
DDR1_AC_10	6433.623
DDR1_AC_11	6384.632
DDR1_AC_12	4389.482
DDR1_AC_13	4968.912
DDR1_AC_14	6687.743
DDR1_AC_15	2391.553
DDR1_AC_20	5662.318
DDR1_AC_21	5536.219
DDR1_AC_22	5318.645
DDR1_AC_23	4745.42
DDR1_AC_24	3798.847
DDR1_AC_25	3783.427
DDR1_AC_26	8556.225
DDR1_AC_28	4621.285
DDR1_AC_29	2456.664
DDR1_AC_30	3850.486
DDR1_AC_31	4298.882
DDR1_AC_32	4000.001
DDR1_AC_33	4537.187
DDR1_AC_34	2765.553
DDR1_AC_35	2977.044
DDR1_AC_36	1828.854

Net Name	Net Length(um)
DDR1_AC_37	1587.874
DDR1_AC_38	4233.489
DDR1_DQ0	6467.507
DDR1_DQ1	4363.669
DDR1_DQ2	3529.762
DDR1_DQ3	4032.636
DDR1_DQ4	4709.173
DDR1_DQ5	6147.046
DDR1_DQ6	5173.892
DDR1_DQ7	4547.813
DDR1_DQ8	5402.701
DDR1_DQ9	3817.321
DDR1_DQ10	3717.225
DDR1_DQ11	4647.977
DDR1_DQ12	3280.81
DDR1_DQ13	2416.644
DDR1_DQ14	2152.137
DDR1_DQ15	4184.853
DDR1_DQ16	3347.275
DDR1_DQ17	4359.613
DDR1_DQ18	4859.07
DDR1_DQ19	5239.311
DDR1_DQ20	3643.34
DDR1_DQ21	4099.978
DDR1_DQ22	5347.057
DDR1_DQ23	4487.338
DDR1_DQ24	3715.342
DDR1_DQ25	2923.508
DDR1_DQ26	2622.058
DDR1_DQ27	3912.034
DDR1_DQ28	2721.158
DDR1_DQ29	2403.124
DDR1_DQ30	1922.521
DDR1_DQ31	4047.65
DDR1_DQM0	4793.601

Net Name	Net Length(um)
DDR1_DQM1	3320.179
DDR1_DQM2	5089.688
DDR1_DQM3	4554.696
DDR1_DQSN0	5372.125
DDR1_DQSN1	3806.477
DDR1_DQSN2	3229.741
DDR1_DQSN3	3489.591
DDR1_DQSP0	5443.279
DDR1_DQSP1	3752.942
DDR1_DQSP2	3370.435
DDR1_DQSP3	3506.484
ENET_RXN	3845.474
ENET_RXP	4081.691
ENET_TXN	4210.243
ENET_TXP	4466.105
GPIOB_0	2345.776
GPIOB_1	1849.83
GPIOB_2	1979.736
GPIOB_3	2088.165
GPIOB_4	2999.87
GPIOB_5	2703.343
GPIOB_6	3412.689
GPIOB_7	2960.572
GPIOB_8	3595.539
GPIOB_10	2083.686
GPIOB_11	2405.297
HDMIRX_ARCTXN	4966.187
HDMIRX_ARCTXP	5112.399
HDMIRX_A_CLKN	5624.866
HDMIRX_A_CLKP	5678.996
HDMIRX_A_D0N	5413.571
HDMIRX_A_D0P	5390.577
HDMIRX_A_D1N	5775.753
HDMIRX_A_D1P	5648.613
HDMIRX_A_D2N	6659.452

Net Name	Net Length(um)
HDMIRX_A_D2P	6444.356
HDMIRX_B_CLKN	5582.84
HDMIRX_B_CLKP	5245.85
HDMIRX_B_D0N	3781.092
HDMIRX_B_D0P	4138.724
HDMIRX_B_D1N	4626.73
HDMIRX_B_D1P	4496.135
HDMIRX_B_D2N	5178.643
HDMIRX_B_D2P	4997.941
HDMIRX_C_CLKN	6477.257
HDMIRX_C_CLKP	6304.805
HDMIRX_C_D0N	3187.457
HDMIRX_C_D0P	3271.665
HDMIRX_C_D1N	3767.361
HDMIRX_C_D1P	3739.942
HDMIRX_C_D2N	3423.348
HDMIRX_C_D2P	3466.655
HDMITX_ARCRXN	2223.555
HDMITX_ARCRXP	2064.952
HDMITX_CLKN	5014.033
HDMITX_CLKP	4858.154
HDMITX_D0N	4305.429
HDMITX_D0P	4133.65
HDMITX_D1N	4243.009
HDMITX_D1P	3985.343
HDMITX_D2N	3857.55
HDMITX_D2P	3444.897
PCIE_CLK_N	2837.101
PCIE_CLK_P	2590.389
PCIE_RXN	2827.673
PCIE_RXP	2767.197
PCIE_TXN	2031.891
PCIE_TXP	1928.492
USB30_RXN	4221.597
USB30_RXP	4260.951

Net Name	Net Length(um)
USB30_TXN	3499.622
USB30_TXP	3323.657
USB_A_OTG_DM	2948.228
USB_A_OTG_DP	2918.029
USB_B_OTG_DM	4237.569
USB_B_OTG_DP	4265.271
VX1_A_0N	2137.44
VX1_A_0P	2439.972
VX1_A_1N	3100.185
VX1_A_1P	3068.469
VX1_A_2N	4195.452
VX1_A_2P	4078.917
VX1_A_3N	2993.326
VX1_A_3P	2782.911
VX1_A_4N	3900.206
VX1_A_4P	4021.289
VX1_A_5N	1946.558
VX1_A_5P	1988.601
VX1_A_6N	3533.938
VX1_A_6P	3397.285
VX1_A_7N	2700.472
VX1_A_7P	2523.065
VX1_B_0N	3854.896
VX1_B_0P	4013.197
VX1_B_1N	2973.577
VX1_B_1P	2856.923
VX1_B_2N	3806.325
VX1_B_2P	3811.417
VX1_B_3N	3680.499
VX1_B_3P	3819.065
VX1_B_4N	2313.953
VX1_B_4P	2282.565
VX1_B_5N	2451.007
VX1_B_5P	2712.78
VX1_B_6N	2325.928

Net Name	Net Length(um)
VX1_B_6P	2450.613
VX1_B_7N	2061.203
VX1_B_7P	2082.518